

# Lab 1

## Task 1

[My Git repository](#)

## Task 2

### 1. Source code

```
architecture dataflow of gates is
begin
    f_o      <=    (not b_i and a_i) or (not c_i and not b_i);
    fnand_o  <=    not(not(not b_i and a_i) and not(not c_i and not b_i));
    fnor_o   <=    not(b_i or not a_i) or not(c_i or b_i);

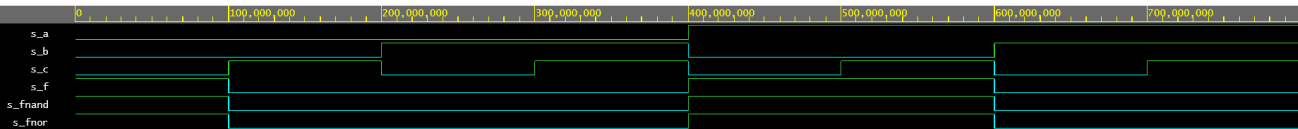
end architecture dataflow;
```

$f = !b*a + !c!*b$

NOR:  $!(b+!a)+!(c+b)$

NAND:  $!(!b*a*!c!*b)$

### 2. Screenshot of time course



a	b	c	f(a,b,c)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

a	b	c	f(a,b,c)
1	1	0	0
1	1	1	0

### 3. Link

[EDA Playground link](#)

## Task 3

### 1. Source code

```
architecture dataflow of gates is
begin
    f1_o <= (x_i and y_i) or (x_i and z_i);
    f2_o <= x_i and (y_i or z_i);
    f3_o <= (x_i or y_i) and (x_i or z_i);
    f4_o <= x_i or (y_i and z_i);

end architecture dataflow;
```

$$x*y + x*z = x*(y+z)$$

$$(x+y) * (x+z) = x + (y*z)$$

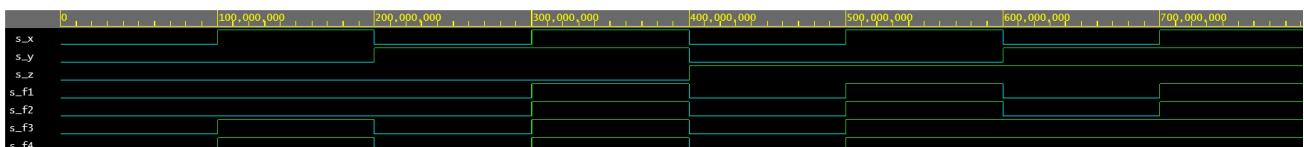
$$f1\_o = x*y + x*z$$

$$f2\_o = x*(y+z)$$

$$f3\_o = (x+y) * (x+z)$$

$$f4\_o = x + (y*z)$$

### 2. Screenshot of time course



x	y	z	f1	f2	f3	f4
0	0	0	0	0	0	0

x	y	z	f1	f2	f3	f4
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	1
1	0	0	0	0	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

### 3. Link

[EDA Playground link](#)