CMOS

0/1 point (ungraded)

A properly-designed CMOS gate has N inputs and one output, and is built using N-1 PFETs (as well as some NFETs). What conclusion can you draw? Select the best choice.

- C1) It uses NFETs in its pullup circuit.
- C2) Its output is always 0.
- C3) Its output is independent of at least one of the N inputs. ✔
- C4) It is not lenient. ✖
- C5) None of the above.

Explanation

A properly-designed CMOS gate has the same inputs going to both its pullup circuit and its pulldown circuit. Since the circuit is built using only N-1 PFETs, then at least one of the inputs is not being used in the pullup which also means that those same inputs are not used in the pulldown. Therefore, the output is only dependent on at most N-1 of the N inputs, so it is independent of at least one of its N inputs.

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Answers are displayed within the problem

CMOS

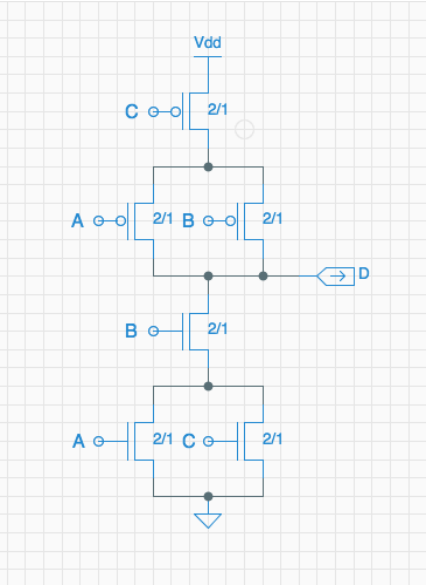
15/15 points (ungraded)

Note: In this problem, your answers for each section will be marked either all correct or all wrong.

Helena Handbasket, who barely passed 6.004, has been hired to design CMOS gates for Hapless Logic, Inc. Remembering something about PFETs in pullups and NFETs in pulldowns, her first design was a 3-input device whose circuit is shown below.

Helena's intent was that these devices compute some useful 3-input Boolean function D=F(A,B,C); unfortunately, the devices don't seem to work as planned. To make matters worse, she had 1,000,000,000 of the devices fabricated (thinking that the order to the fab must, of course, be in binary rather than decimal). The defective devices, known within HLI as the Gates of Helena, have become a subject of ridicule.

Helena has brought you in as a consultant. Your first task is to figure out how badly Helena blew the design of her 3-input logic device – in particular, whether it drives the output D to a valid logic level for every combination of the inputs A, B, and C.



(A) Are there logical (0/1) values of A, B, and C for which D is not driven at all? If so, enter 0 or 1 values for A, B, and C that leave D undriven; else enter NONE.

A = 1 ✔

B = 0 ✔

C = 1 ✔

Explanation

If B = 0, then D cannot be driven low. If C = 1, then D cannot be driven high. So if B = 0 and C = 1, then D is undriven.

(B) Are there logical values of A, B, and C for which D is pulled down and up simultaneously? If so, enter 0 or 1 values for A, B, and C that cause such a conflict; else enter NONE.

A = NONE ✔

B = NONE ✔

C = NONE ✔

Explanation
Examining the truth table for this circuit shows that all input combinations result in a 0, 1, or Not Driven output. None of the input combinations results in an output conflict.

A	B	C	D
0	0	0	1
0	0	1	$NotDriven$
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	$NotDriven$
1	1	0	0
1	1	1	0

Nora Nanda, Helena's assistant, suggests that the devices might be salvaged by using them to compute useful functions of fewer than 3 inputs. She proposes that a two-input function of X and Y, for example, might be computed by connecting each of the three inputs A, B, and C to either X, Y, or the logical constants 0 (ground) or 1 (vdd), and reading the output on D.

(C) Can Nora's approach be used to compute NAND of X and Y? If so, enter values (X, Y, 0, or 1) for each of A, B, and C such that D is NAND(X,Y); else enter NONE.

A = X ✔

B = Y ✔

C = 0 ✔

Explanation
If C = 0, then this circuit reduces to parallel A and B in pullup and series A and B in pulldown. This is equivalent to NAND(A, B). So if A = X and B = Y and C = 0, or if A = Y and B = X and C = 0, then this circuit is equivalent to NAND(X, Y).

(D) Can Nora's approach be used to compute NOR of X and Y? If so, enter values (X, Y, 0, or 1) for each of A, B, and C such that D is NOR(X,Y); else enter NONE.

A = X ✔

B = 1 ✔

C = Y ✔

Explanation
If B = 1, then this circuit reduces to series A and C in pullup and parallel A and C in pulldown. This is equivalent to NOR(A, C). So if A = X and B = 1 and C = Y, or A = Y and B = 1 and C = X, this circuit is equivalent to NOR(X, Y).

(E) Can Nora's approach be used to compute OR of X and Y? If so, enter values (X, Y, 0, or 1) for each of A, B, and C such that D is OR(X,Y); else enter NONE.

A = None ✔

B = None ✔

C = None ✔

Explanation
In order to produce the function OR(X, Y), it must be possible for the gate to produce a logical 0 if X = 0 and Y = 0. However, this gate will always produce a logical 1 if two of its inputs are 0, so it is not possible to make this gate compute OR(X, Y).

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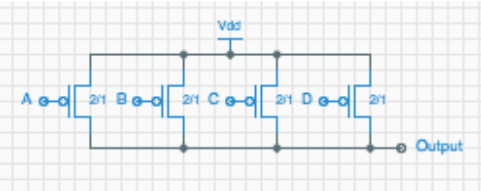
Answers are displayed within the problem

CMOS

1/1 point (ungraded)

Given the following pullup circuit, and assuming that the pulldown circuitry is designed correctly, the logic function implemented by this gate would be



- $(A \cdot B + C) \cdot D$
- $\overline{A + B + C + D}$
- $\overline{(A \cdot B + C) \cdot D}$
- $\overline{(A + B) \cdot C + D}$
- $\overline{A \cdot B \cdot C \cdot D}$
- $A \cdot B \cdot C \cdot D$

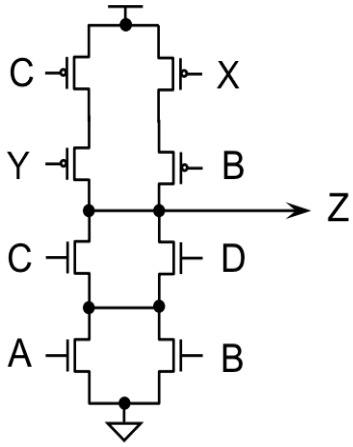
Submit

Correct (1/1 point)

CMOS

4/4 points (ungraded)

Hapless Logic, Inc has hired Helena Handbasket to get them out of a jam. They are about to order a huge number of 4-input CMOS gates that compute a boolean function Z = H(A,B,C,D), but their previous CMOS designer left and enrolled in Barista school without having quite completed the design. His unfinished circuit for the CMOS gate is shown below. The inputs labelled "X" and "Y" have been left disconnected.



The pulldown circuit is known to be correct, but Helena isn't sure that the pullup performs in the appropriately complementary way. Moreover, labels on two of the pullup inputs are missing, complicating the analysis. Ignoring the pullup circuit, you deduce the intended Boolean function H(A,B,C,D) from the pulldown alone.

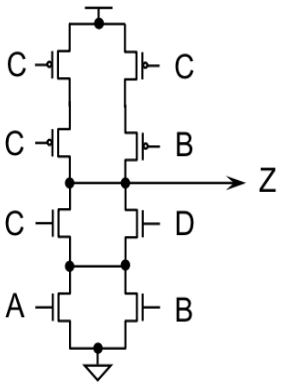
Can you supply the missing input labels in the diagram above such that the circuit computes H(A,B,C,D) properly? If so, choose the proper values for X and Y; otherwise, choose "not possible" for both X and Y.

X = A ✔ Answer: A Y = D ✔ Answer: D

Explanation

Pulldown and pullup circuits always have complementary logic. Since the pulldown circuit has parallel A and B in series with parallel C and D, the pullup circuit should have series A and B in parallel with series C and D.

Helena, unfortunately, isn't as smart as you. She simply connects the two unlabeled PFET inputs to C (as shown below), and sends off the order to fabricate millions of gates. When the gates return from the fab, she runs some tests to see what they do.



Helena finds that for certain combinations of input values A, B, C, and D, the miswired gates draw a lot of current until they burn up. Give a set of input values (0 or 1 for each of the four inputs) that would be likely to exhibit this behavior with Helena's miswired gates. Provide your four input values separated with spaces or commas between them.

A, B, C, D = 1 1 0 1 ✔

Explanation
If C is connected to 0, Z will always be connected to vdd. If D is 1 and at least one of A and B are connected to 1, Z will simultaneously be connected to gnd.

In a desperate attempt to salvage some minor use for her broken gates, Helena searches for a way to tie three of the inputs to constants (ground=0 or vdd=1), such that the devices will serve as an inverter for the remaining input. Assign values 0, 1, and P to the four inputs of the bad gates such that the output will be the inverse of P. Use 0, 1, or P separated by spaces or commas, and connect only one input to P.

A, B, C, D = 1 1 P 0 ✔

Explanation
We cannot constantly assign C to 1 or 0 (if C = 1 then Z can never be connected to vdd, and if C = 0 the Z is always connected to vdd), so we can instead use C as P. Then, if we assign D to 0 and assign either A or B to 1, Z will be the inverse of C.

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ℹ Answers are displayed within the problem

CMOS

1 point possible (ungraded)

The Boolean function F(A,B,C,D) of four inputs is implemented as a single CMOS gate which consists of a pullup circuit containing only PFETs and a puldown containing only NFETs. The output of F is known to depend on its inputs; i.e., F(A,B,C,D) is 0 for certain input combinations and 1 for others. What can you deduce about F(1,1,1,1)?

F(1, 1, 1, 1) = Select an option

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CMOS

1 point possible (ungraded)

How many transistors would you expect to use in a CMOS implementation of a 3-input OR?

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☑	C3) Its output is independent of at least one of the N inputs. correct What about N=1? does that choice work too?	5
💬	Interesting: about Helena's Gates! (So this is Helen(a)'s beautiful Gate that launched a thousand (uhm... billion) Chips!!!) Seriously tho...	2
💬	(A) of 2nd Question is badly worded There are two combinations of ABC that leaves output not driven but it is not clear that only one of...	2