Leniency

1/1 point (ungraded)

In lecture we saw that a 2-input NOR gate might obey the static discipline (i.e., be a valid combinational device) without being a lenient combinational device. Is it possible for an inverter to be a valid combinational device without being lenient?

- ○ Yes
- ◉ No
- ○ Can't Tell

✔

Explanation

A device is lenient if it will generate a glitch-free output using a minimal number of required inputs. A 1-input device such as an inverter depends on only 1 input, and nothing else, so therefore it is always lenient.

Submit

ℹ Answers are displayed within the problem

Leniency

0/1 point (ungraded)

A 2-input AND gate is made from a lenient CMOS 2-input NAND gate followed by a lenient CMOS inverter. Is the AND gate necessarily lenient?

- ○ Yes ✔
- ◉ No
- ○ Can't Tell

Explanation

A lenient AND gate will output 0 if any of its inputs is 0. A lenient NAND will output 1 if any of its inputs is 0, and the inverter will invert that output, so the resulting AND gate is lenient.

Submit

Answers are displayed within the problem

Leniency

1 point possible (ungraded)

If an inverter conforms to our definition of a combinational device, is it necessarily lenient?

- Yes
- No

Submit

Discussion

Hide Discussion

Topic: 3. CMOS / Tutorial : Leniency

Add a Post

Show all posts by recent activity

Why the inverter is lenient ? Why in the following questions we are considering inverter to be lenient? Usually in lenient devices...	6
Leniency tutorial - Problem 1 "Is it possible for an inverter to be a valid combinational device without being lenient?" Each invert...	6
The Number of Inputs not specified. In CMOS Tutorial, the last problem "If an inverter conforms to our definition of a combinational devi...	2