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Lab due Oct 24, 2016 21:59 -02 Past due

CMOS logic gates

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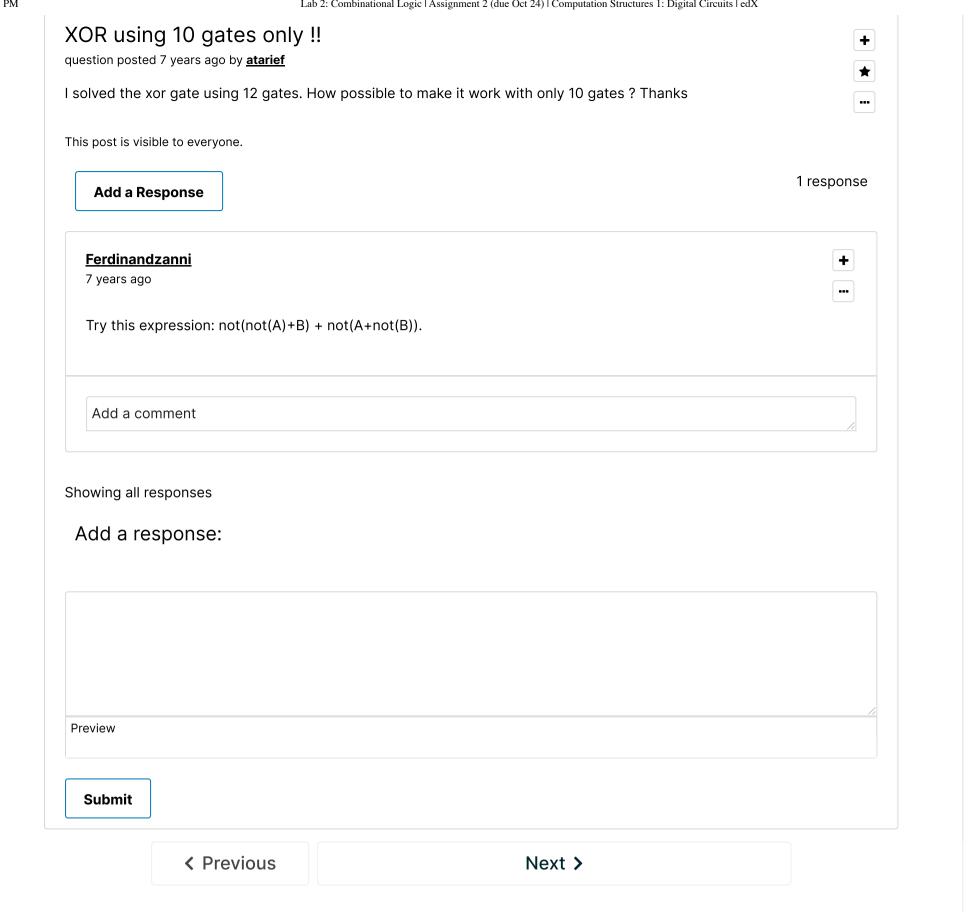
There are 16 possible 2-input combinational logic gates. The cost of implementing these gates varies dramatically, requiring somewhere between 0 and 10 mosfets depending on the gate. For example, it takes 2 mosfets to implement $F = \overline{A}$ but 4 mosfets (organized as two inverters) to implement F = A.

For each of the 2-input gates whose Karnaugh maps are given below, indicate the minimum number of mosfets required to implement the gate. You should only consider static fully-complementary circuits like those shown in the presentations; these implementations meet the following criteria:

- no static power dissipation
- ullet $V_{OL}=0V$, V_{OH} = power supply voltage
- NFETs appear only in pulldown circuits, PFETs appear only in pullup circuits
- the pullup and pulldown are complementary, i.e., when one path is "on", the other is "off"
- the pullup and pulldown circuits can be decomposed into series and parallel connections of mosfets
- all gate implementations restore incoming logic levels (so a wire connecting an input terminal to an output terminal would not be a legal gate implementation)

$egin{array}{c ccccccccccccccccccccccccccccccccccc$	Number of MOSFETs need to implement NOR:	4	Answer: 4
$egin{array}{c ccccccccccccccccccccccccccccccccccc$	Number of MOSFETs need to implement AND:	6	Answer: 6
$egin{array}{c ccccccccccccccccccccccccccccccccccc$	Number of MOSFETs need to implement XOR: Hint: see discussion in following design proble		Answer: 10
B O 1 1 1 1 0 0	Number of MOSFETs need to implement $\overline{m{B}}$:	2	Answer: 2
$egin{array}{c ccccc} A & & & & & \\ \hline A & & & & & \\ \hline B & & & & & \\ \hline B & & & & & \\ \hline 1 & & & & & \\ \hline \end{array}$	Number of MOSFETs need to implement $A\cdot \overline{B}$	<u> </u>	Answer: 6
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