LE14.1

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LE14.1.1 Average Memory Access Time

1/1 point (ungraded)

A particular cache design responds in 1 cycle on a cache hit, but takes an *additional* 20 clock cycles if there's a cache miss. If we want an average memory access time of 2 cycles or better, what is the minimal acceptable cache hit ratio?

minimum acceptable cache hit ratio:

0.95 ✔

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LE14.1.2 Multi-level cache AMAT

1/1 point (ungraded)

A hierarchical memory system consists of a two-level SRAM cache and a large DRAM main memory. The system first checks the L1 cache. If the access to L1 is a cache miss, the system then checks the L2 cache. If the access to L2 is a cache miss, an access is made to main memory.

For L1: the cache hit time is 1 ns, the hit ratio is 95%

For L2: the cache hit time is 4 ns, the hit ratio is 98%

For main memory: the access time is 40ns

What is the average memory access time in ns?

1.24 ✔

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