LE15.1

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For all Beta related questions, you should make use of the Beta documentation, the Beta Instruction Summary, the Unpipelined Beta Diagram and the Pipelined Beta Diagram.

LE15.1.1: Data Hazards

1.0/1.0 point (ungraded)

This problem concerns the 5-stage Beta pipeline with full bypass logic.

Consider the execution of the following sequence on the 5-stage pipelined Beta:

```
ADDC(R31, 44, R0)
SUBC(R0, 0, R1)
MULC(R0, 23, R4)
LD(R0, 0, R2)
XORC(R2, 1, R3)
```

For the following questions, we recommend first drawing out the pipeline diagram associated with this problem. Identify all the cycles where the situation described occurs, then check off all the instructions that appear in the RF stage of these cycles. If the situation never occurs, then select "NONE".

1. Are there points in the execution of the sequence when data is bypassed from the **ALU** stage back to the **RF** stage?

- [ ] ADDC
- [x] SUBC
- [ ] MULC
- [ ] LD
- [ ] XORC
- [ ] NONE

✔

2. Are there points in the execution of the sequence when data is bypassed from the **WB** stage back to the **RF** stage?

- [ ] ADDC
- [ ] SUBC
- [ ] MULC
- [x] LD
- [x] XORC
- [ ] NONE

✔

3. Are there points during the execution of the sequence when the pipeline is stalled?

- [ ] ADDC
- [ ] SUBC

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- [ ] MULC
- [ ] LD
- [x] XORC
- [ ] NONE

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Why does the XORC instruction need to stall while It can take data from WB state?

question posted 7 years ago by **xBach**

As title, I think the answer of question B which is just LD instruction.

This post is visible to everyone.

rhodesd (Community TA)
7 years ago - marked as answer 7 years ago by **rhodesd** (Community TA)

Hi xBach, XORC finds R2 from the bypass hardware in the WB stage of cycle 8 because the value written to R2 by LD isn't available in the register file until just after the rising clock edge at the beginning of cycle 9.

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