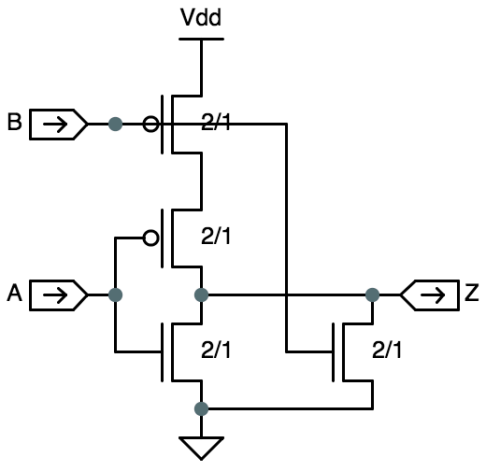
LE3.3.1: CMOS Truth Table

4/4 points (ungraded)

Here's another simple CMOS circuit with series PFETs for the pullup circuit and parallel NFETs for the pulldown circuit.



Please fill in the truth table below, giving the value of the output Z for the four possible combinations of the inputs values A and B.

A	B	Z	
0	0	1	✔ Answer: 1
0	1	0	✔ Answer: 0
1	0	0	✔ Answer: 0
1	1	0	✔ Answer: 0

Explanation

When either A or B is 1, the PFETs they control would be OFF and the NFETs they control would be ON. If at least one of the inputs is 1, the series PFET pullup is not conducting, but the parallel NFET pulldown is. So if at least one of inputs is 1, Z is pulled down to 0. When A=0 and B=0, both NFETs are OFF, but both PFETS are ON, so Z is pulled up to 1. This is a 2-input NOR gate.

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Answers are displayed within the problem

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STAFF line over the CMOS? 5

On the **top-left CMOS**, would not it be better(for clarity) to have the **line** from input B to t...