Tutorial: Caches

Bookmark this page

Caches: 2

2/2 points (ungraded)

Two otherwise-identical Beta systems have 1024-line two-way set-associative caches using LRU and FIFO replacement, respectively. For what programs does the **FIFO** cache show a higher hit ratio than the LRU cache?

FIFO outperforms on:

- ○ **ALL**
- ○ **MOST**
- ◉ **A FEW**
- ○ **NONE**

✔

Two otherwise-identical Beta systems have fully-associative LRU caches. One cache has four lines, each caching a single 32-bit word; the other cache has eight lines, each also holding a single 32-bit word. For what programs does the **smaller** cache show a higher hit ratio?

***Small* cache outperforms on (circle one):**

- ○ **ALL**
- ○ **MOST**
- ○ **A FEW**
- ◉ **NONE**

✔

Submit

Caches: 1

0/1 point (ungraded)

1. You are evaluating two tiny 4-line caches, each with a total storage of four data words. Model DM is direct-mapped, and model FA is fully associative (LRU). Each uses **word addressing** (hence consecutive addresses differ by 1, not 4 as in the Beta). The benchmark involves just six memory reads, starting with an empty (invalidated) cache. Finish the reference string given below to yield an access pattern that will give a **better hit rate on DM than on FA**. Fill in the final two additional memory addresses. **Use single-digit decimal addresses.**

   0, 1, 2, 3, 0 ✖ , 1 ✖

   Explanation
   With LRU replacement, the fully associative cache will always replace the 0 with the new element being requested because it is the least recently used element. However, in a direct mapped cache, the element replaced is predetermined by its address. So if the 6th memory address requested is a 0, then the DM cache will get a hit while FA cache misses provided that the 5th memory address requested did not replace the 0 element. This occurs when the 5th element is 5, 6, 7, or 9.

2. Same setup as above; this time give references that make FA look better. Again, **use single-digit decimal addresses.**

   0, 1, 2, 3, 5 , 1

   Explanation
   In order for the fully associative cache to perform better that the direct mapped cache, the direct ma

Calculator

cache must miss on its 5th and 6th request. This occurs if the 6th request maps to the same location in the direct mapped cached as the 5th request. This occurs for the request sequences (5,1), or (6,2), or (7,3), or (9,1). 8 cannot be the 5th request because that would replace the same element in both the FA and DM caches.

Submit

Answers are displayed within the problem

Caches: 2

9 points possible (ungraded)

You are considering three possible caches for use in a Beta-like computer system that uses 24-bit byte addresses to access 32-bit (4-byte) words in main memory – hence each word address is divisible by four (as in the Beta).

Each of the caches you are considering has a total of 64 cache lines, each holding one 32-bit data word. The three cache models are as follows:

Cache	Description
DM	Direct-mapped, 64 lines
4Way	4-way set associative: 16 sets of 4 lines each.
FA	Fully-associative: one set of 64 lines.

To compare caches, you have collected some additional parameters about each model and have run a tiny benchmark program to measure the performance of each. Your benchmark program is a tight loop that repeatedly accesses the **4** locations given by the **hex byte addresses**:

0×100, 0×200, 0×104, 0×108, 0×100, 0×200, 0×104, 0×108, 0×100, ...

You have been asked to complete the following table. Fill in blank entries; use “NA” (Not Applicable) for inapplicable parameters.

Assume that the incoming address from the CPU is A[23:0], that each cache stores the minimum number of address bits in the tag field for each line. The “# Lines for Mem[0]” column lists the number of lines in each cache that might hold the contents of main memory location zero, and the Hit Rate column reflects each cache’s steady-state performance on the little benchmark described above.

Cache Model	Bits of A[23:0] used to address cache	# Tag bits Per line	Replacement Strategy	# Lines for Mem[0]	Hit Rate
DM	A[7:2]		Select an option	1	
4Way	A[:]		LRU		
FA	NA	22	LRU		100%

Submit

Calculator

Discussion

Topic: 14. Caches and the Memory Hierarchy / Tutorial: Caches

Hide Discussion

Add a Post

All Posts

Problem 1 issue

discussion posted 8 years ago by **Yann_Garcia**

Hi All,

Regarding the first problem, I have some difficulties to understand what is requested, even with the answer! What are exactly the values to enter: a range of address or just the next address of the data to save in the cache?

Many thanks for your help,

Yann

This post is visible to everyone.

Add a Response

1 response

bensaccount
8 years ago

It's the next two addresses to be accessed (one in each box for each question).

Oh it's just it, thanks a lot, I think my english is not good enough sometime

Yann

posted 8 years ago by **Yann_Garcia**

It took me a while to figure it out too.

posted 8 years ago by **bensaccount**

Add a comment

Showing all responses

Add a response:

Preview

Previous Next

Calculator

edX

About
Affiliates
edX for Business
Open edX
Careers
News

Legal

Terms of Service & Honor Code
Privacy Policy
Accessibility Policy
Trademark Policy
Sitemap
Cookie Policy
Your Privacy Choices

Connect

Idea Hub
Contact Us
Help Center
Security
Media Kit

深圳市恒宇博科技有限公司 粤ICP备17044299号-2

Calculator