LE8.1

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LE8.1.1 Asymptotic Latency and Throughput

1/1 point (ungraded)

If we account for fan in limitations but ignore wire delays, what is the asymptotic latency of the fastest combinational N-input AND circuit we can build?

Asymptotic latency of N-input AND:

log(N) ✔ Answer: log(N)

You entered:

$$\log(N)$$

Explanation

Accounting for the fan in limitations means that if we have a gate with N inputs, we can't just assume that its propagation delay is the same as a 2-input gate. The way we model this is by turning an N-input gate into a tree of 2-input gates. The equivalent tree of 2-input AND gates would have log(N) levels in the tree in order to arrive at enough 2-input AND gates to allow for N inputs. Each level of the tree must complete its propagation delay before the next level can begin its computation, therefore the latency of the tree is log(N).

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LE8.1.2 Asymptotic Latency and Throughput

1/1 point (ungraded)

Is $\Theta(log_2 N)$ the same as $\Theta(log_{10} N)$

- (●) Yes
- ( ) No
- ( ) Only for some N

✔

Explanation

According to the base-change formula for logarithms, $Log_a(n) = \frac{Log_b(n)}{Log_b(a)}$. In other words, any base can be converted to any other base by multiplying by a constant. Since we ignore constant multiplicative factors in asymptotic notation, we can also ignore bases of logarithms.

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LE8.1.3 Asymptotic Latency and Throughput

2/2 points (ungraded)

A combinational multiplier is pipelined for maximum throughput. If the multiplier accepts two N-bit operands, what is the appropriate “order of” notation for its throughput and latency?

Throughput $\Theta(\ldots)$: 1 ✔ Answer: 1

Calculator

1

Latency $\Theta(\ldots)$: N ✔ Answer: N

N

Explanation

A combinatorial multiplier works by initially combining bits of the same order, and adding a step for each carry bit that needs to be considered. Those carrying steps can all happen in an isolated pipeline stage, and the inital combination of same-order bits can happen completely in parallel, so the throughput should never be affected by expanding the number of bits in each number that we are multiplying. However, the latency will be affected, because each additional bit in our operands requires an extra pipeline stage, putting the overall latency at $\Theta(N)$.

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Accounting for the fan in limitations

"... if we have a gate with N inputs, we can't just assume that its propagation delay is the same as a 2-input gate." why not? 4

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