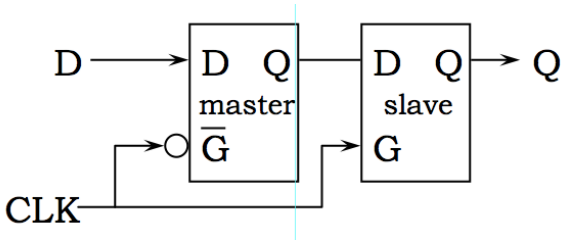
LE5.2.1 D-register Timing

4/5 points (ungraded)

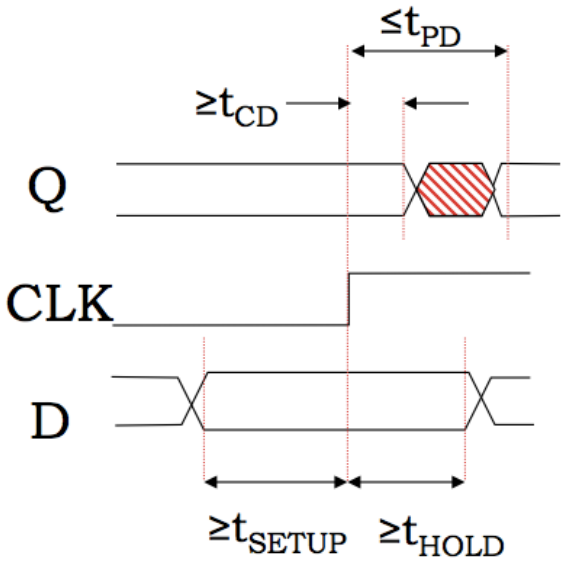
A D-register is constructed from two D-latches according to the schematic shown below.



The timing specifications for the master and slave latches are shown below.

	Master	**Slave**
t_{PD}	0.90 ns	1.30 ns
t_{CD}	0.17 ns	0.20 ns
t_{SETUP}	0.91 ns	0.82 ns
t_{HOLD}	0.20 ns	0.13 ns

Please determine the appropriate timing specifications for the register, selecting values for $t_{CD}, t_{PD}, t_{SETUP}, t_{HOLD}$, shown in the following figure.



Register contamination delay t_{CD} (ns): 0.2 ✔ Answer: 0.2

Register propagation delay t_{PD} (ns): 1.3 ✔ Answer: 1.3

Register setup time t_{SETUP} (ns): 0.91 ✔ Answer: 0.91

Register hold time t_{HOLD} (ns): 0.2 ✔ Answer: 0.2

Explanation
The register's setup and hold times are those of the master latch since that's where the D input connects. The register's contamination and propagation delays are those of the slave latch since that's where the Q output connects.

Suppose we're able to choose a faster time for the contamination delay t_{CD} for the master latch. What would be the smallest possible time we could choose and still have the register work correctly?

Smallest possible t_{CD} for master latch (ns): 0.2 ✖

Answer: 0.13

Explanation
The contamination delay of the master latch must be greater than or equal to the hold time of the slave latch so the smallest possible value for contamination delay of the master is 0.13 ns.

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  I'm confused about the specification chart provided for this question. As we've seen, in a latch, Ts...
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Propagation delay is defined as the delay from valid input to a valid output. When we consider a d r...

Tsetup and Thold ? 3

Hello , In the Question above we have considered the set up and hold times of the circuit equivalen...

slave register's tsetup 4

I dont get something. In the rising edge of the clock the contamination delay of the máster latch m...