LE17.1

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LE17.1.1: Interrupts

0.0/1.0 point (ungraded)

1. A busy Beta system spends about half of its CPU cycles servicing interrupts in the OS kernel. For what fraction of these interrupts would you expect the high-order bit of the XP register to be a 1 on entry to the interrupt handler?

- (•) 0% ✔
- ( ) 50%
- ( ) 100%

Explanation
Interrupts are only allowed on the beta when you are in user mode. In user mode PC[31] = 0. When an interrupt occurs the value of PC + 4 is stored into the XP register. This means that the most significant bit (MSB) of the XP register will be a 0, otherwise that would imply that you took an interrupt while you were already in supervisor mode.

2. A JMP instruction is executed on the Beta in Kernel mode. What are the possible values of the high-order PC bit immediately following the JMP?

Select best choice:

- ( ) only 1
- ( ) only 0
- (•) 1 or 0 ✔

Explanation
JMP is the only instruction that can take you out of supervisor mode. If you are in supervisor mode and the most significant bit (MSB) of your jump target is a 0 then you will set PC[31] = 0 and thus exit supervisor mode. If the jump target MSB is a 1 then you will remain in supervisor mode. If you are currently in user mode, then the MSB of the jump instruction is ignored.

3. An interrupt is taken while a Beta is executing application code in a user-mode program. What, if any, register contents of the interrupted application might be changed as a result of this device interrupt?

Select all that apply, or NONE if none apply:

- [ ] R0
- [ ] LP
- [ ] BP
- [x] XP ✔
- [ ] NONE

Explanation
When an interrupt occurs, the value of PC + 4 is stored in the XP register.

Calculator

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Answers are displayed within the problem

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