

Implementing FSM with Sequential Logic

Asked 11 months ago Modified 11 months ago Viewed 95 times

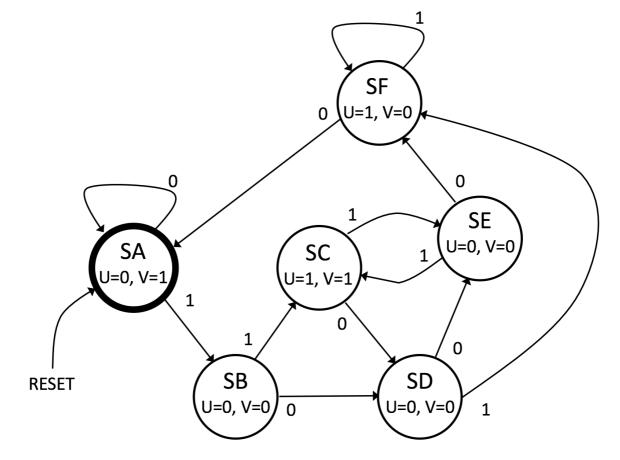


I am trying to complete Problem 4 of <u>this MIT Computation Structures lab</u>, which requires you to use a circuit simulator called Jade to build a sequential logic circuit that implements the below FSM:

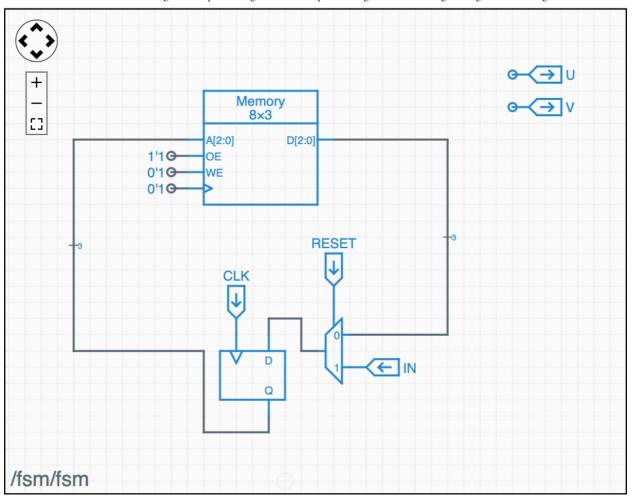






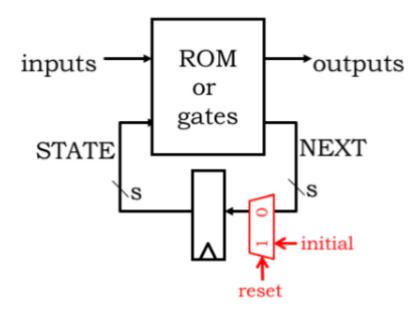


So far, the below is what I have:



I'm trying to implement this using the ROM/register combo that is referenced in the problem (and on the lecture slides the problem references).

However, I'm not sure how to connect the U and V outputs. The ROM/register combo shown in lecture looks a bit different, as it has a separate spot for inputs and outputs:



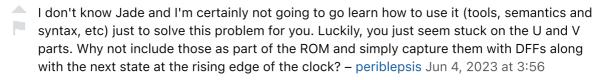
Does anyone have any thoughts on how I might be able to implement that in Jade?

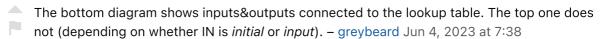
register | rom | sequential-logic

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asked Jun 3, 2023 at 17:28







Coder, Since you are non-responsive, I'll just hand you <u>an answer</u> but one that doesn't use a ROM. If you help us help you, I may write more in an answer. – periblepsis Jun 5, 2023 at 1:39

Appreciate the responses. Very busy day today so haven't had a chance to take another crack at this problem today but hope to have some time tomorrow. – Coder1913 Jun 5, 2023 at 3:14

@Coder1913 Okay. When you get a moment, then... – periblepsis Jun 5, 2023 at 21:31

1 Answer

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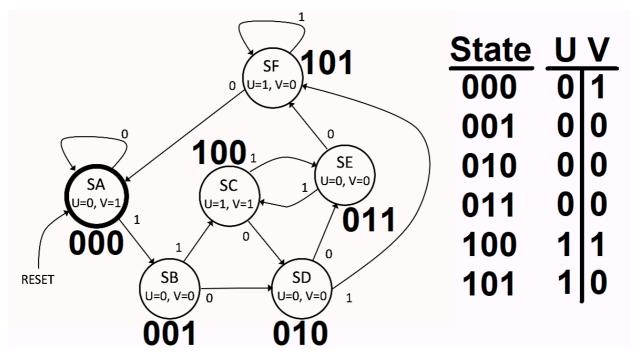
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Let's start by assigning state numbers to each state:





My reasoning here is that U is just a copy of the most significant DFF. That makes U easy to produce. Next, I decided that V=1 when both of the less significant DFFs are zero.

That's also easy to produce.

From here it is now possible to create a table:

	State	:	IN	Ne	ew St	ate
Q_C	Q_B	Q_A		Q_C	Q_B	Q_A
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	1	0	0
0	1	0	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	0	0	0
1	0	1	1	1	0	1
1	1	0	0	х	x	x
1	1	0	1	x	x	x
1	1	1	0	x	x	x
1	1	1	1	x	X	x

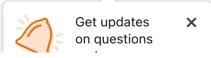
That table should be very easy to stick into a ROM along with the associated U and V values. You could either latch them from the ROM output at the time of the clock-driven state transition or else derive them from the current address presented at the ROM address bus prior to the next clock.

Alternately, you avoid the ROM and instead just produce the Karnaugh maps:

$Q_C D$	$\overline{Q_A}$ \overline{IN}	$\overline{Q_A}$ IN	Q_A IN	$Q_A \ \overline{IN}$
$\overline{Q_C Q_B}$	0	0	1	0
$Q_C Q_B$ $Q_C Q_B$	0	1	1	1
$Q_C Q_B$	x	X	X	x
$Q_C \overline{Q_B}$	0	0	1	0

$Q_B D$	$\overline{Q_A}$ \overline{IN}	$\overline{Q_A}$ IN	Q_A IN	Q_A
$Q_C Q_B$	0	0	0	
$ \begin{array}{c c} \hline Q_C & Q_B \\ \hline Q_C & Q_B \\ \hline Q_C & Q_B \end{array} $	1	0	0	
$Q_C Q_B$	x	x	X	
$Q_C \overline{Q_B}$	1	1	0	

$Q_A D$	$\overline{Q_A}$ \overline{IN}	$\overline{Q_A}$ IN	Q_A IN	$Q_A \ \overline{IN}$
$\overline{Q_C Q_B}$	0	1	0	0
$ \begin{array}{c c} \hline Q_C & Q_B \\ \hline Q_C & Q_B \\ \hline Q_C & Q_B \end{array} $	1	1	0	1
$Q_C Q_B$	x	X	x	x
$Q_C \overline{Q_B}$	0	1	1	0



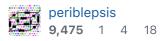
And work out the logic required for tha those tables.

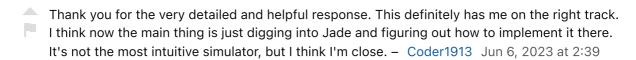
and answers

mizing logic from

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answered Jun 6, 2023 at 0:58





@Coder1913 Best wishes. I hope it does help you get where you need to go with it. :) You might consider posting up the resulting Jade code so that I can learn something about Jade from you.;) – periblepsis Jun 6, 2023 at 2:42 🖍