Power dissipation

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Lab due Oct 24, 2016 21:59 -02 Past due

Power dissipation

0.0/2.0 points (graded)

Almost all of the power dissipated by CMOS circuits goes into charging and discharging nodal capacitances. This power can be computed as CV^2F where C is the capacitance being switched, V is the change in voltage, and F is the frequency at which the switching happens. In CMOS circuits, nodes are switched between ground (0 volts) and the power supply voltage (V_{DD} volts), so V is either $+V_{DD}$ (for a $0 \rightarrow 1$ output transition) or $-V_{DD}$ (for a $1 \rightarrow 0$ output transition) and so $V^2 = V_{DD}^2$.

Suppose we have a device implemented in a technology where $V_{DD} = 5V$. If we have the option of reimplementing the device in a technology where $V_{DD} = 3.3V$, what sort of speedup (i.e., change in F) could be specified for the reimplementation assuming we want to keep the power budget unchanged?

Speedup (e.g., 2.0 would be twice as fast): 2.3 Answer: 2.3

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