# LE14.2.1 Cache Addresses

1/1 point (ungraded)

The contents of a small 4-line Direct Mapped cache is shown to the right. Note that some of the leading 0's in the Tag field value are not shown. The cache is part of the Beta's memory system. What is the main memory (byte) address for each of the 32-bit data words held in the cache? Please express the value in hex or write "CAN'T TELL" if the value cannot be determined.

| Line # | Tag | Data |
|---|---|---|
| 3 | 0×07 | 0×739F0083 |
| 2 | 0×07 | 0×73FF012C |
| 1 | 0×02 | 0×73FF029E |
| 0 | 0×10 | 0×627F0060 |

**Byte address of data word in cache line 0: 0x** 100 ✔ Answer: 100

Explanation
tag (addr bits [31:4]) = 0×0000010
index (addr bits [3:2]) = 0b00
offset (addr bits [1:0]) = 0b00
address = 0×00000100

**Byte address of data word in cache line 1: 0x** 024 ✔ Answer: 24

Explanation
tag (addr bits [31:4]) = 0×0000002
index (addr bits [3:2]) = 0b01
offset (addr bits [1:0]) = 0b00
address = 0×00000024

**Byte address of data word in cache line 2: 0x** 078 ✔ Answer: 78

Explanation
tag (addr bits [31:4]) = 0×0000007
index (addr bits [3:2]) = 0b10
offset (addr bits [1:0]) = 0b00
address = 0×00000078

**Byte address of data word in cache line 3: 0x** 07C ✔ Answer: 7C

Explanation
tag (addr bits [31:4]) = 0×0000007
index (addr bits [3:2]) = 0b11
offset (addr bits [1:0]) = 0b00
address = 0×0000007C

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Answers are displayed within the problem

## Discussion

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labeling cache lines
So, is it fair to say that if we are dealing with 8 line cache: the bottom line will always be 0 and the ... 2

Direct mapped caches
I don't understand slide 27. First, what are offset bits for? Are they used for something in mapping ... 3