LE13.3.1 Beta speedup?

1.0/1.0 point (ungraded)

1. In a standard Beta implementation, suppose you could speed up the generation of a single control signal ("Control Logic" output) in order to increase the Beta's clock frequency. Which signal would you choose to generate faster?

   Timing-critical Beta control signal:

   RA2SEL ✔

2. In a standard unpipelined Beta implementation, Ben Bitdiddle proposes using the signal ID[30] (bit 30 of the current instruction) in place of RA2SEL as the select input to the mux that determines the value of the RA2 input to the register file. Will the modified Beta design still work correctly in *all* circumstances?

   - (•) Yes
   - ( ) No

   ✔

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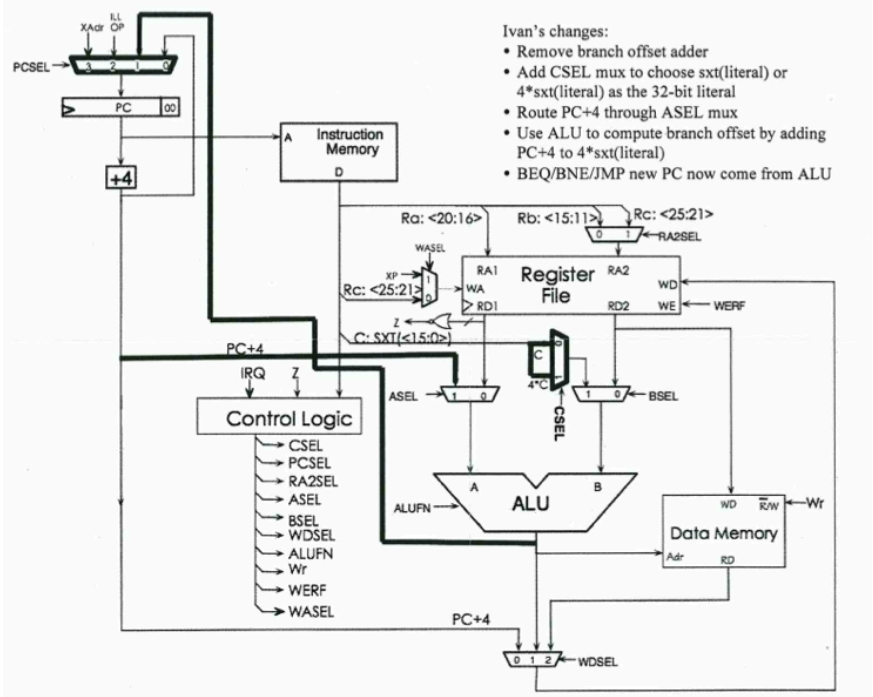
LE13.3.2 Better Beta?

1/1 point (ungraded)

Ivan Idea, a brilliant exchange student from the Moscow Institute of Technology, has decided to simplify the Beta data paths by eliminating the branch offset adder and using the ALU to perform the necessary arithmetic. His revised datapath diagram is shown below. At the same time, he noticed he could eliminate the JT input to the PCSEL mux and use the new path from the ALU output to the PCSEL mux to deliver the JMP address to the PC logic. He has outsourced to you the task of updating the Control ROM table, filling in the row for the new CSEL control signal as well as filling in the columns for JMP, BNE, BEQ and LDR to ensure the Beta operates as before.



Instr	ALUFN	WERF	BSEL	WDSEL	MOE	MWR	RA2SEL	P
ADD	A+B	1	0	1	-	0	0	0
ADDC	A+B	1	1	1	-	0	-	0
LD	A+B	1	1	2	1	0	-	0
ST	A+B	0	1	-	0	1	1	0
JMP	A ✔	1 ✔	- ✔	0 ✔	- ✔	0 ✔	- ✔	
BEQ	A+B	1	1	0	-	0	-	

BNE	A+B	1	1	0	-	0	-	
LDR	A+B	1	1	2	1	0	-	

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✔ Correct (1/1 point)