LE3.4

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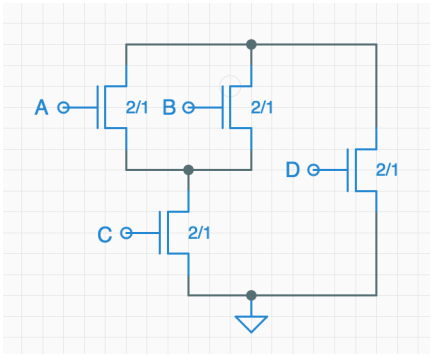
LE3.4.1: Complementary circuits

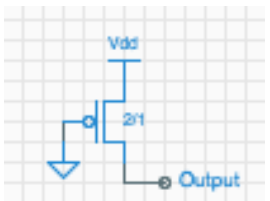
1/1 point (ungraded)

The following diagram shows a schematic for the pulldown circuitry for a particular CMOS logic gate.

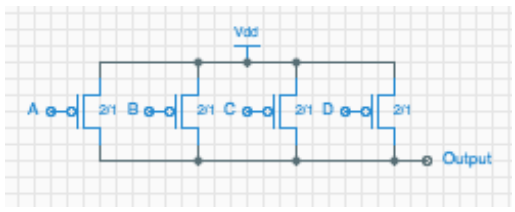


Which of the following would be the most likely schematic for the pullup circuitry?

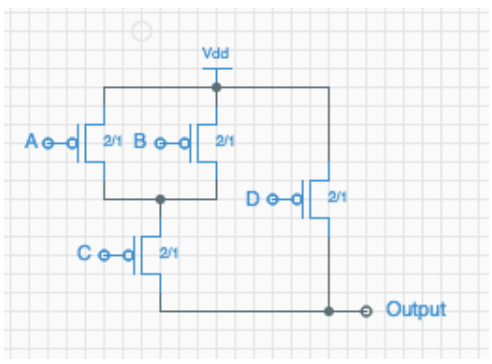
A)



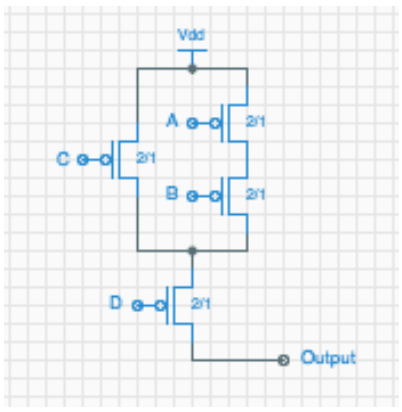
B)



C)



D)



E) None of the above

✔

Explanation

CMOS pullup circuits are the complement of their pulldown, so all series circuits are repaced with parallel and all parallel with series. In addition, all NFETs are replaced with PFETs.

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Answers are displayed within the problem

LE3.4.2: CMOS Recipe

Calculator

1 point possible (ungraded)

A single 3-input CMOS logic gate computes F(A,B,C). Its circuit has the property that every mosfet's gate is connected to one of A, B, or C. Which logic function might it compute?

- A) $A \cdot B \cdot C$
- B) $A + B \cdot C$
- C) $A + \overline{B \cdot C}$
- D) $\mathbf{XOR}\,(A, B, C)$
- E) $\overline{ABC}$
- F) None or several of the above (or can't tell)

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  I have watched every lecture in order to this point, and have not seen an explanation for what the answers to this problem represen...
- LE3.4.2 sample problem — 3
  Does "A single 3-input CMOS logic gate" uniquely define the layout? Are all these inputs connected to the same gate (I assume this...

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Calculator