LE15.3

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For all Beta related questions, you should make use of the Beta documentation, the Beta Instruction Summary, the Unpipelined Beta Diagram and the Pipelined Beta Diagram.

LE15.3.1: Exceptions

1/1 point (ungraded)

An ambitious 6.004x student has enhanced the 5-stage pipelined Beta to trigger an exception in the ALU stage when there's an attempt to divide by zero, i.e., when the B operand of the ALU is zero and the opcode of the instruction in the ALU stage is DIV or DIVC.

For each of the following control signals, indicate its value during the clock cycle when the divide-by-zero exception occurs.

1. $IRSrc^{IF}$

   1 ✔ Answer: 1
2. $IRSrc^{RF}$

   1 ✔ Answer: 1
3. $IRSrc^{ALU}$

   2 ✔ Answer: 2
4. $IRSrc^{MEM}$

   0 ✔ Answer: 0

Explanation

Since the exception occurs in ALU stage, that's the stage for which we want to capture the PC+4 of the instruction that triggered the exeption. So $IRSrc^{ALU}$ is 2.

When there's an exception in the ALU stage, we have to annul the instructions earlier in the pipeline, since in the program they came after the instruction that caused the fault and hence should not be executed. So $IRSrc^{IF}$ and $IRSrc^{RF}$ are both 1.

Instructions in later pipeline stages are unaffected by the exeception in the ALU stage. So $IRSrc^{MEM}$ is 0.

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Answers are displayed within the problem

LE15.3.2: Bypassing, stalls, annulment

0.0/1.0 point (ungraded)

The loop below has been executing for a while on our standard 5-stage pipelined Beta with full bypassing and speculation on branches (i.e., instruction in IF stage is annulled when there's a taken branch in the RF stage). The pipeline diagram below shows the opcode of the instruction in each pipeline stage during 9 consecutive cycles of execution.

```
       ...
LOOP:  LD(R0, 0, R2)
       SHLC(R1, 1, R1)
       ADD(R1, R2, R1)
       ADDC(R0, 4, R0)
       CMPEQC(R0, aend, R2)
       BNE(R2, LOOP)
       ST(R1, hash, R31)
       ...
```

Cycle #	200	201	202	203	204	205	206	207	208

IF	LD	SHLC	ADD	ADDC	ADDC	CMPEQC	BNE	ST	LD
RF	NOP	LD	SHLC	ADD	ADD	ADDC	CMPEQC	BNE	NOP
ALU	BNE	NOP	LD	SHLC	NOP	ADD	ADDC	CMPEQC	BNE
MEM	CMPEQC	BNE	NOP	LD	SHLC	NOP	ADD	ADDC	CMPEQC
WB	ADDC	CMPEQC	BNE	NOP	LD	SHLC	NOP	ADD	ADDC

1. For each cycle, specify whether or not a bypass path was used to get the data from a later pipeline stage to the RF stage. If multiple bypass paths are used in a particular cycle, then select all that apply.

Cycle 200:

- [ ] No bypass paths used
- [ ] Bypass from ALU to RF
- [ ] Bypass from MEM to RF
- [ ] Bypass from WB to RF

Cycle 201:

- [ ] No bypass paths used
- [ ] Bypass from ALU to RF
- [ ] Bypass from MEM to RF
- [ ] Bypass from WB to RF

Cycle 202:

- [ ] No bypass paths used
- [ ] Bypass from ALU to RF
- [ ] Bypass from MEM to RF
- [ ] Bypass from WB to RF

Cycle 203:

- [ ] No bypass paths used
- [ ] Bypass from ALU to RF
- [ ] Bypass from MEM to RF
- [ ] Bypass from WB to RF

Cycle 204:

- [ ] No bypass paths used
- [ ] Bypass from ALU to RF
- [ ] Bypass from MEM to RF
- [ ] Bypass from WB to RF

Cycle 205:

- [ ] No bypass paths used
- [ ] Bypass from ALU to RF
- [ ] Bypass from MEM to RF
- [ ] Bypass from WB to RF

Cycle 206:

- [ ] No bypass paths used
- [ ] Bypass from ALU to RF
- [ ] Bypass from MEM to RF
- [ ] Bypass from WB to RF

Cycle 207:

- [ ] No bypass paths used
- [ ] Bypass from ALU to RF
- [ ] Bypass from MEM to RF
- [ ] Bypass from WB to RF

Cycle 208:

- [ ] No bypass paths used
- [ ] Bypass from ALU to RF
- [ ] Bypass from MEM to RF
- [ ] Bypass from WB to RF

For the following questions think carefully about when a signal would be asserted in order to produce the effect you see in the pipeline diagram. Select all the cycles that apply, or select NONE if it never occurs.

2. During which cycle(s), if any, would the $IRSrc^{IF}$ signal be 1?

- [ ] 200
- [ ] 201
- [ ] 202
- [ ] 203
- [ ] 204
- [ ] 205
- [ ] 206
- [ ] 207
- [ ] 208
- [ ] NONE

3. During which cycle(s), if any, would the $IRSrc^{RF}$ signal be 1?

- [ ] 200
- [ ] 201
- [ ] 202
- [ ] 203
- [ ] 204
- [ ] 205
- [ ] 206
- [ ] 207
- [ ] 208
- [ ] NONE

4. During which cycle(s), if any, would the $IRSrc^{ALU}$ signal be 1?

- [ ] 200
- [ ] 201
- [ ] 202
- [ ] 203
- [ ] 204

- [ ] 205
- [ ] 206
- [ ] 207
- [ ] 208
- [ ] NONE

5. During which cycle(s), if any, would the STALL control signal be 1, i.e., cycle(s) when the IF and RF stages would be stalled?

- [ ] 200
- [ ] 201
- [ ] 202
- [ ] 203
- [ ] 204
- [ ] 205
- [ ] 206
- [ ] 207
- [ ] 208
- [ ] NONE

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