

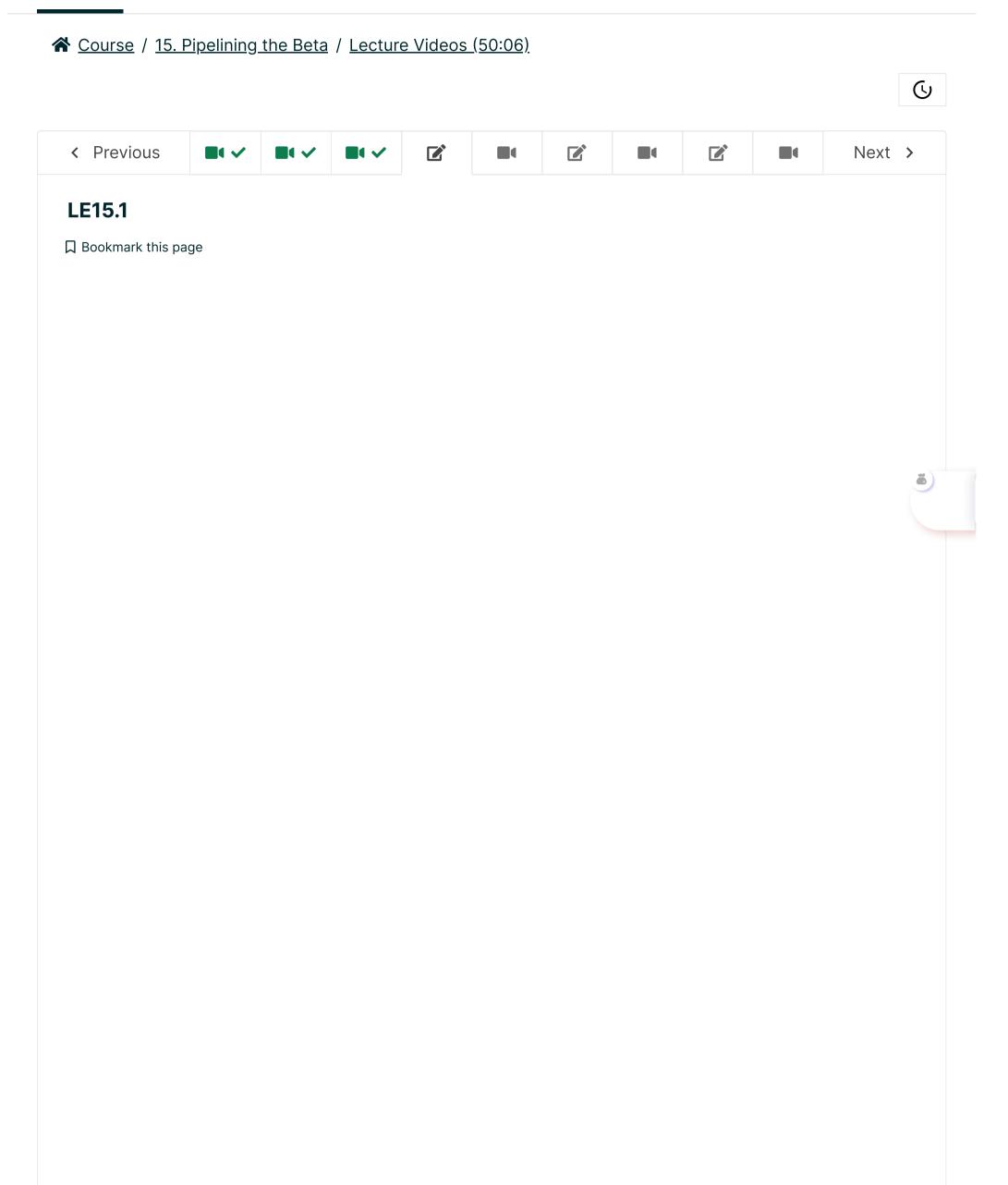
Computation Structures 3: Computer Organization

<u>Help</u>





<u>Course</u> <u>Progress</u> <u>Dates</u> <u>Discussion</u>



For all Beta related questions, you should make use of the <u>Beta documentation</u>, the <u>Beta Instruction</u> <u>Summary</u>, the <u>Unpipelined Beta Diagram</u> and the <u>Pipelined Beta Diagram</u>.

LE15.1.1: Data Hazards

1.0/1.0 point (ungraded)

This problem concerns the 5-stage Beta pipeline with full bypass logic.

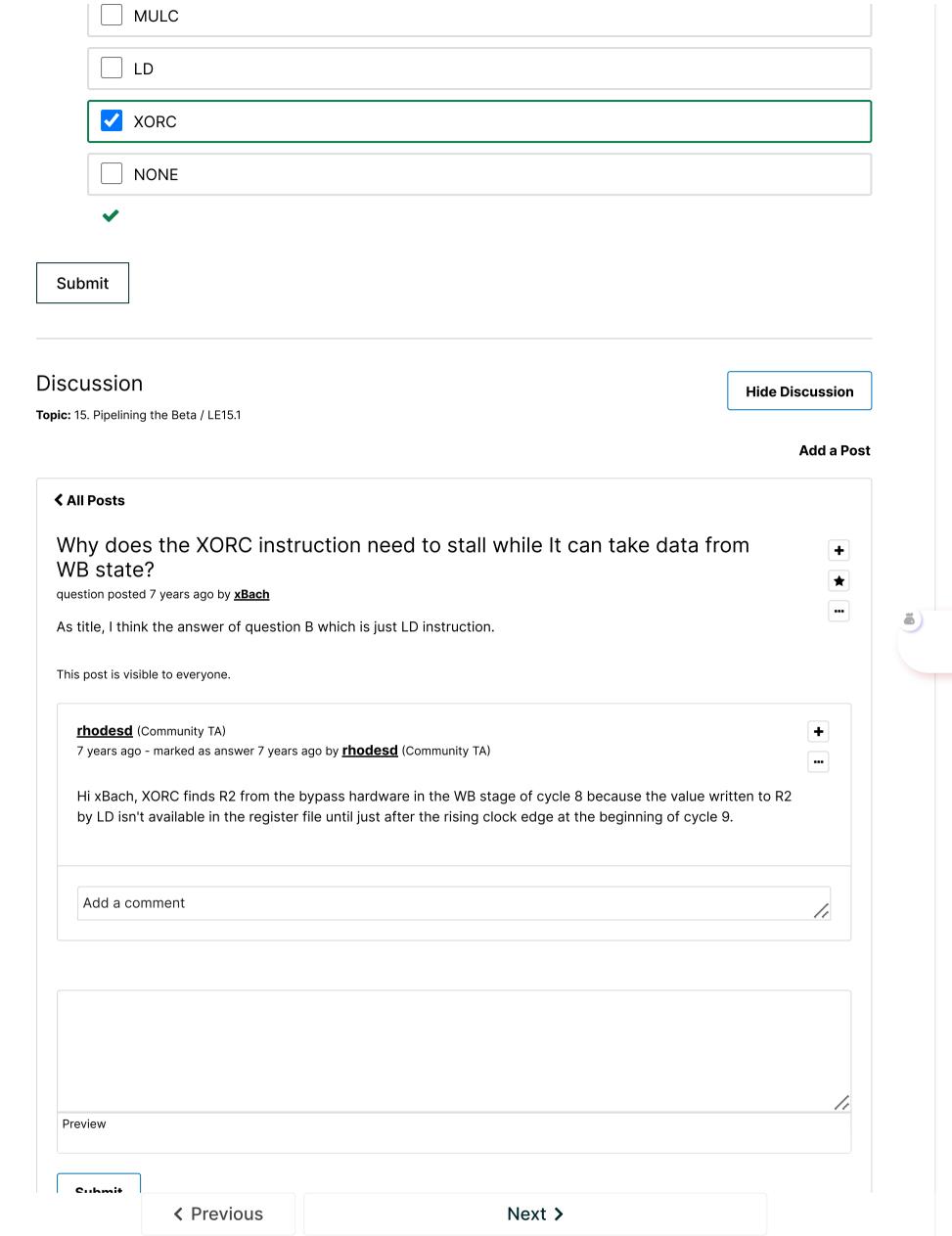
Consider the execution of the following sequence on the 5-stage pipelined Beta:

```
ADDC(R31, 44, R0)
SUBC(R0, 0, R1)
MULC(R0, 23, R4)
LD(R0, 0, R2)
XORC(R2, 1, R3)
```

For the following questions, we recommend first drawing out the pipeline diagram associated with this problem. Identify all the cycles where the situation described occurs, then check off all the instructions that appear in the RF stage of these cycles. If the situation never occurs, then select "NONE".

1. Are there points in the execution of the sequence when data is bypassed from the ALU stage back to the RF stage?	
	ADDC
✓	SUBC
	MULC
	LD
	XORC
	NONE
2. Are there points in the execution of the sequence when data is bypassed from the WB stage back to the RF stage?	
	ADDC
	SUBC
	MULC
~	LD
~	XORC
	NONE
✓ Are th	ere points during the execution of the sequence when the pipeline is stalled?
	ADDC
	SUBC

⊞ Calculator



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