6.004 | Spring 2017 | Undergraduate

Computation Structures

Menu

More Info

Calendar

This calendar reflects the campus schedule when this course was taught at MIT. The lab exercises are currently not included.

SES #	TOPICS	KEY DATES
L1	Unit 1: Basics of information: entropy, encodings, error correction	
L2	Unit 2: The digital abstraction: combinational logic, voltage-based encoding	
L3	Unit 3: CMOS: MOSFETs, gate design; timing	
L4	Unit 4: Combinational logic: canonical forms, synthesis, simplification	
L5	Unit 5: Sequential logic: latches, registers, timing	Lab 1 due
L6	Unit 6: Finite-state machines (FSMs); asynchronous inputs and metastability	
L7	Unit 7: Performance measures: throughput and latency, pipelining	
Quiz 1 (L1–L5)		
L8	Unit 8: Design tradeoffs: power, speed, area, throughput	
L9	Unit 9: von Neumann architectures, Beta instruction set	Lab 2 due
L10	Unit 10: Assmbly language	
L11	Unit 11: Compiling expressions and statements	Lab 3 due
L12	Unit 12: Stacks and procedures	
L13	Unit 13: Beta implementation	
Quiz 2 (L6–L12)		
L14	Unit 14: Multilevel memories: locality, performance, caches	
L15	Unit 14: Cache design issues (continued)	Lab 4 due
L16	Unit 15: Pipelining the Beta: pipeline diagrams, data hazards	
L17	Unit 15: Pipelining the Beta: control hazards, dealing with exceptions (continued)	Lab 5 due
L18	Unit 16: Virtual memory: mapping, protection, contexts	
Quiz 3 (L13–L17)		
L19	Unit 17: Virtual machines: timesharing, OS kernels, supervisor calls	
L20	Unit 18: Devices and interrupts; real-time	Lab 6 due
L21	Unit 19: Communicating processes: semaphores, synchronization, atomicity, deadlock	
L22	Unit 20: System-level communication	Lab 7 due
L23	Unit 21: Parallel processing: performance limits, data- and thread-level parallelism	
L24	Building a Better Beta: tips for the design project	
Quiz 4 (L18–L22); design project due in one week after the quiz		

Feedback

Open Learning