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Tutorial : Leniency

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Leniency

1/1 point (ungraded)

In lecture we saw that a 2-input NOR gate might obey the static discipline (i.e., be a valid combinational device) without being a lenient combinational device. Is it possible for an inverter to be a valid combinational device without being lenient?

☐ Yes

☒ No

☐ Can't Tell



Explanation

A device is lenient if it will generate a glitch-free output using a minimal number of required inputs. A 1-input device such as an inverter depends on only 1 input, and nothing else, so therefore it is always lenient.

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Answers are displayed within the problem

Leniency

0/1 point (ungraded)

A 2-input AND gate is made from a lenient CMOS 2-input NAND gate followed by a lenient CMOS inverter. Is the AND gate necessarily lenient?

☐ Yes

☒ No

☐ Can't Tell

Explanation

A lenient AND gate will output 0 if any of its inputs is 0. A lenient NAND will output 1 if any of its inputs is 0, and the inverter will invert that output, so the resulting AND gate is lenient.

Submit

Answers are displayed within the problem

Leniency

0/1 point (ungraded)

If an inverter conforms to our definition of a combinational device, is it necessarily lenient?

☒ Yes


☐ No

Explanation

A device is lenient if it will generate a glitch-free output using a minimal number of required inputs. A 1-input device such as an inverter depends on only 1 input, and nothing else, so therefore it is always lenient.

Calculator

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 Answers are displayed within the problem

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