WE3.2

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Video explanation of solution is provided below the problem.

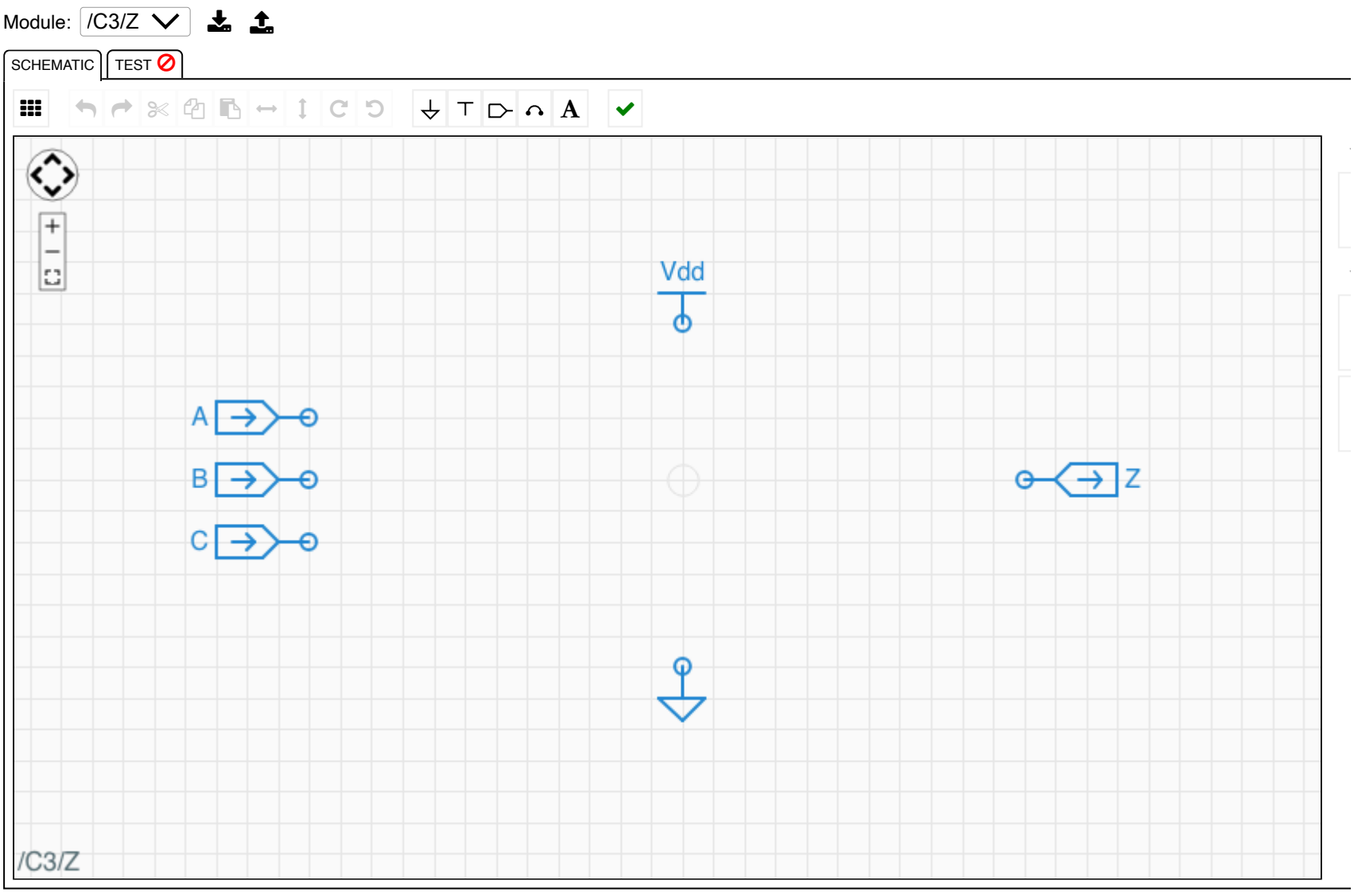
CMOS Logic Gates

1 point possible (ungraded)

Your mission is to design and test a circuit that implements the function $Z = \overline{(A + B) \cdot C}$ as a single CMOS gate. Recall that we want to use NFETs to build the gate's pulldown circuit and PFETs to build the gate's pullup circuit. The truth table for Z is shown below:

A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

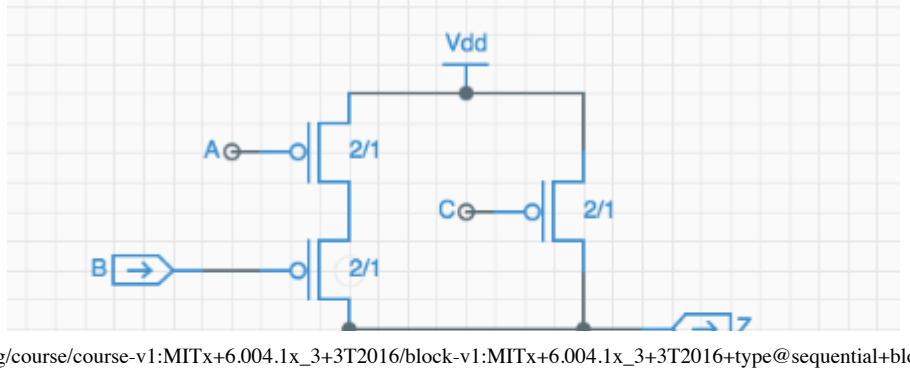
Here's an instance of Jade you can use to enter and test your circuit.



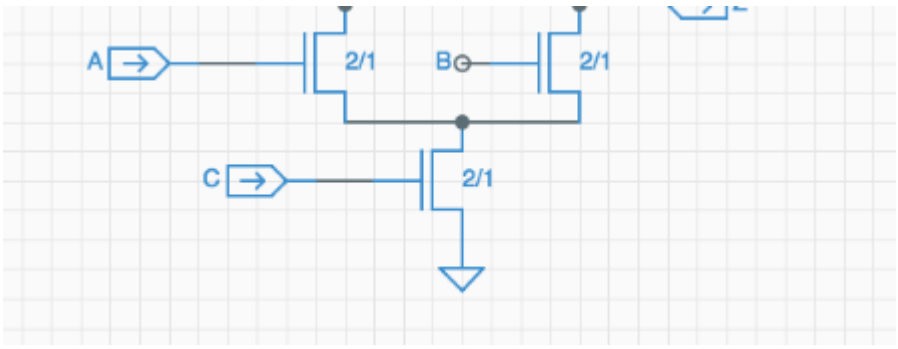
To complete the design problem, click the green checkmark in the Jade toolbar and the built-in tester will either report any discrepencies between the expected and actual outputs, or, if your design is correct, it will record the test passed so that clicking the Check below will give you credit for completing the problem.

Explanation

The circuit that implements the function Z is shown below.



Calculator



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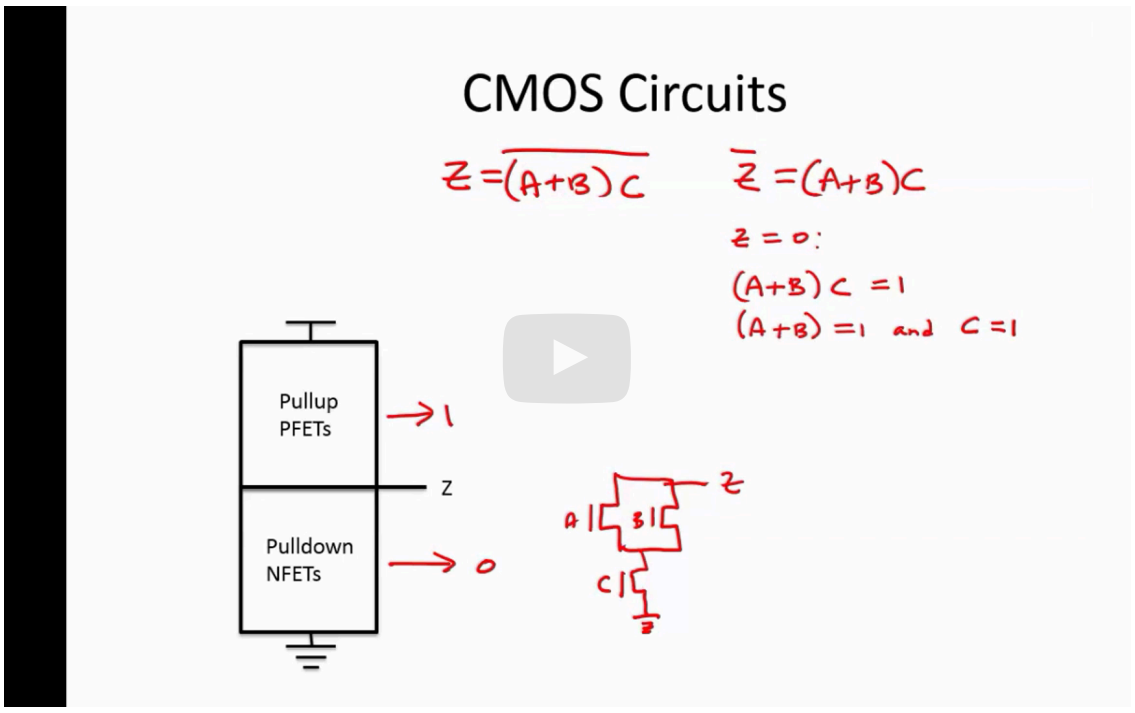
Answers are displayed within the problem

CMOS Logic Gates



1:33 / 3:00 1.0x

Video

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This occurs when ((A or B) and C) equals 1, so the pull-down circuitry should be on when ((A or B) and C) equals 1.

So (A OR B) = 1 and C = 1.

This means that we want a parallel(A,B) in series with C circuit for our pull-down.

The parallel(A,B) corresponds to (A OR B) = 1 because if either A or B equals 1 then we have a path from Z to the bottom of the parallel circuitry.

Then if C is also 1, we complete our path between Z and ground.

So, if either (A = 1 and C = 1) or (B = 1 and C = 1), Z is pulled down to ground and produces a 0 output.

To generate our pull-up, we simply replace parallel circuits with series, and series with parallel.

This will ensure that whenever our pull-down circuit is off, our pull-up circuit is on.

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Calculator

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