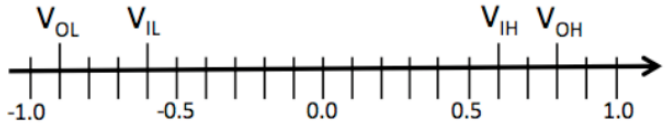
# LE2.3.1: Noise margins

1/2 points (ungraded)

A new family of logic devices uses signaling voltages in the range −1V to +1V. One proposed assignment of our voltage specification is shown below. Observe $V_{OL} = -0.9, V_{IL} = -0.6, V_{IH} = 0.6, V_{OH} = 0.8$.




The *noise immunity* of a signaling specification is the smaller of the two noise margins. What is the noise immunity for the signaling scheme proposed above? Please give a numeric answer to the nearest .1 volt. If it is impossible to tell what the noise immunity is, write "NONE".

Noise immunity (V): 0.2 ✔ Answer: 0.2

Explanation

The low noise margin is defined $V_{IL} - V_{OL}$. The high noise margin is defined as $V_{OH} - V_{IH}$. That means that the low noise margin is 0.3V and the high noise margin is 0.2V. Since noise immunity is defined as the smaller of the two noise margins, the noise immunity is 0.2 volts.

The output voltage of an inverter is measured to be 0.9V in the steady state. The inverter is a combinational device obeying the signaling specification shown above. What is the best characterization of the steady-state input voltage $V_{IN}$ of the inverter when the measurement was made? Please give a numeric answer to the nearest .1 volt. If it is impossible to characterize $V_{IN}$, write "NONE".

$V_{IN}\ (V) <$ -0.6 ✖ Answer: 0.6

Explanation

A 0.9 volt output is a high output. If we are producing a high output, all we can definitively say about the input voltage is that it is not a valid high input because in that case, the output would be low. So the constraint on the input voltage is that $V_{IN} < 0.6V$. Note that you cannot assume that the input voltage is a valid low which would be less than -0.6V just because the output happens to be high. In other words, input voltages in the forbidden zone could produce a valid high output.

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Answers are displayed within the problem

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| For the second question, the answer is wrong<br>For the second question, the answer is wrong. It should be -0.6 instead of 0.6. | 6 |
| VIN?<br>Hello, For an inverter with 0.9v **stady state** output which is considered logically high, then I wo... | 13 |
| Really struggling with this exercise<br>Hello! I am kind of struggling with the basis of the theory behind this. I can't give the answers to th... | 4 |
| V_IN in case of same static discipline for the circuit<br>> The output voltage of an inverter is measured to be 0.9V in the steady > state. The inverter is a ... | 2 |
| Noise margins<staff> | 2 |