Tutorial : Combinational Timing

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Combinational Timing

1/1 point (ungraded)

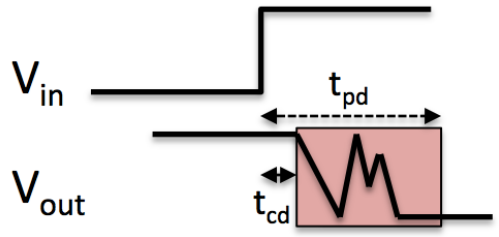
Is it possible for an inverter to have a contamination delay that is greater than it's propagation delay?

- ○ Yes
- ◉ No
- ○ Can't Tell

✔

Explanation

By definition, the contamination delay of any gate must be less than or equal to the propagation delay of that gate. Taking a look at an inverter specifically, you can visualize this using the following diagram.



If you think of the input changing instantaneously as shown here, and just think about what happens to your output, then its clear that $t_{CD} < t_{PD}$. t_{CD} measures the time from when the input changes to when the output might begin to change. t_{PD} measures the time from when the input changes to when the output becomes stable and valid with its new value. The output must enter the red zone (t_{CD}) before it can exit it (t_{PD}).

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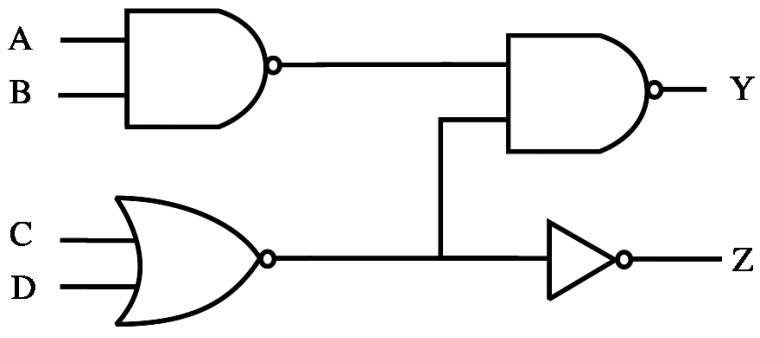
ℹ Answers are displayed within the problem

Combinational Timing

2 points possible (ungraded)



Here's a table showing the t_{CD} and t_{PD} for each of the components in the circuit above. Please compute t_{CD} and t_{PD} for the circuit as a whole.

	t_{CD}	t_{PD}
Inverter	0 ns	4 ns
NAND	1 ns	8 ns
NOR	4 ns	10 ns

Calculator

Contamination delay (ns):

Propagation delay (ns):

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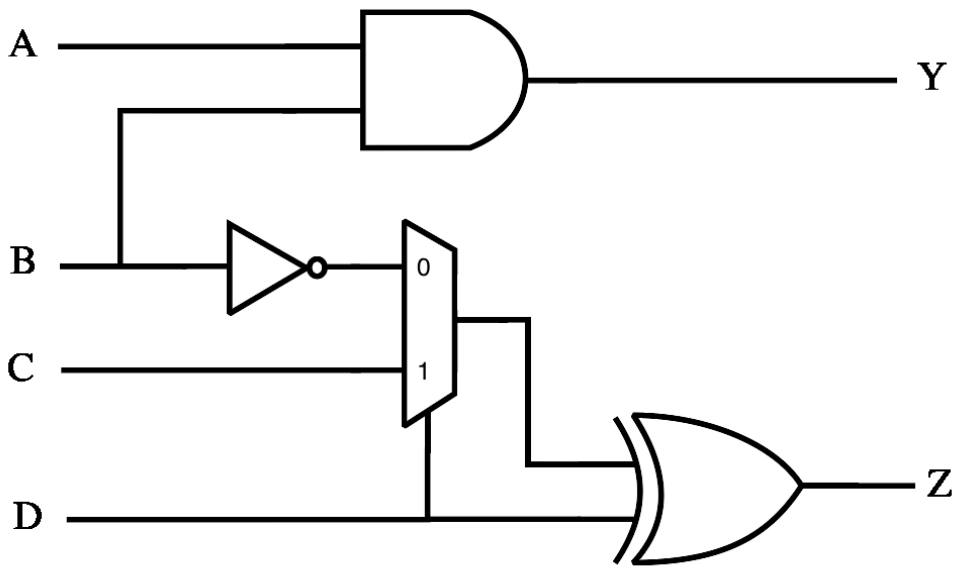
Combinational Timing

2 points possible (ungraded)



Here's a table showing the t_{CD} and t_{PD} for each of the components in the circuit above. Please compute t_{CD} and t_{PD} for the circuit as a whole.

	t_{CD}	t_{PD}
Inverter	0.1 ns	0.7 ns
AND2	0.3 ns	0.7 ns
XOR2	0.4 ns	2.2 ns
MUX2	0.1 ns	1.0 ns

t_{CD} (ns):

t_{PD} (ns):

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[STAFF] there is no E in 2nd graph! 2

Also too many paragraphs in the answer to 2nd circuit. It is a simple concept 2 paragraphs should be enough

Combinational Timing Part 1 6

Calculator

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Calculator