

[Course](#)

[Progress](#)

[Dates](#)

[Discussion](#)

[Course Notes](#)

 [Course](#) / [3. CMOS](#) / [Worked Examples](#)



< Previous



Next >

WE3.2

 Bookmark this page

 Calculator

Video explanation of solution is provided below the problem.



CMOS Logic Gates


1 point possible (ungraded)


Your mission is to design and test a circuit that implements the function $Z = \overline{(A + B)} \cdot C$ as a single CMOS gate. Recall that we want to use NFETs to build the gate's pulldown circuit and PFETs to build the gate's pullup circuit. The truth table for Z is shown below:

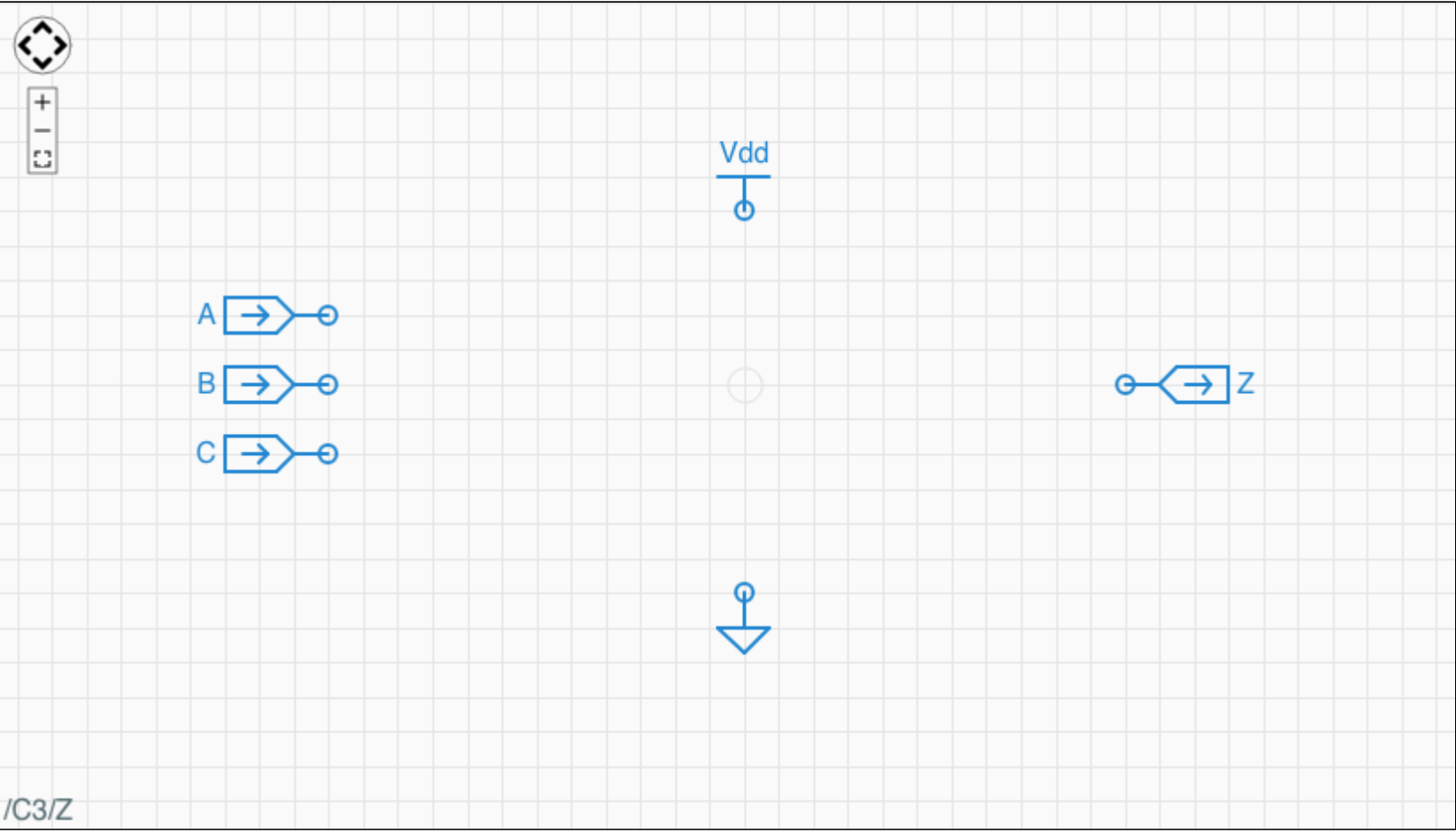
A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Here's an instance of Jade you can use to enter and test your circuit.

Module: /C3/Z  

SCHEMATIC 



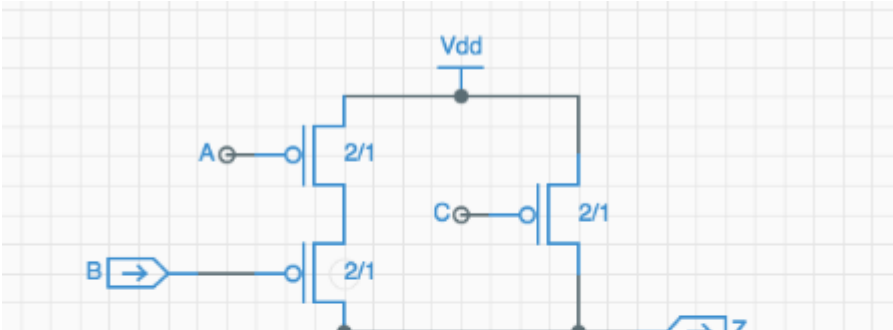


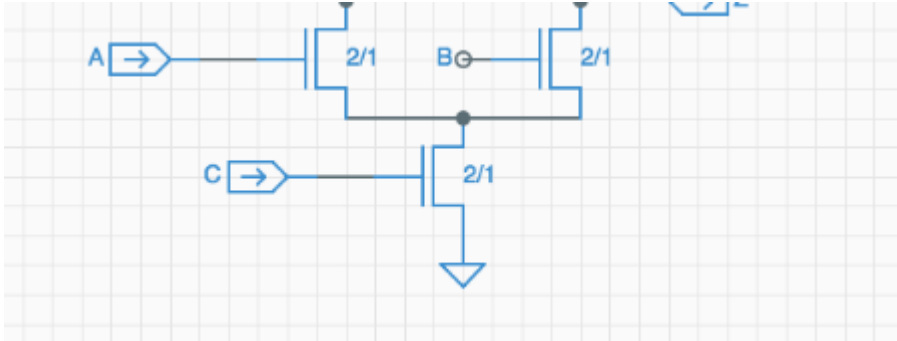
Copyright © MIT EECS 2011-2015 [Jade 2.2.46 \(2015\)](#)

To complete the design problem, click the green checkmark in the Jade toolbar and the built-in tester will either report any discrepancies between the expected and actual outputs, or, if your design is correct, it will record the test passed so that clicking the Check below will give you credit for completing the problem.

Explanation

The circuit that implements the function Z is shown below.





Submit

Answers are displayed within the problem

CMOS Logic Gates

CMOS Circuits

$Z = \overline{(A+B)C}$ $\bar{Z} = (A+B)C$

$Z = 0$:

$(A+B)C = 1$
 $(A+B) = 1$ and $C = 1$

This occurs when ((A or B) and C) equals 1, so the pull-down circuitry should be on when ((A or B) and C) equals 1.

So (A OR B) = 1 and C = 1.

This means that we want a parallel(A,B) in series with C circuit for our pull-down.

The parallel(A,B) corresponds to (A OR B) = 1 because if either A or B equals 1 then we have a path from Z to the bottom of the parallel circuitry.

Then if C is also 1, we complete our path between Z and ground.

So, if either (A = 1 and C = 1) or (B = 1 and C = 1), Z is pulled down to ground and produces a 0 output.

To generate our pull-up, we simply replace parallel circuits with series, and series with parallel.

This will ensure that whenever our pull-down circuit is off, our pull-up circuit is on



Video

Download video file

Transcripts

- Download SubRip (.srt) file
- Download Text (.txt) file

Discussion

Topic: 3. CMOS / WE3.2

Hide Discussion

Add a Post

All Posts

Jade chó chết

discussion posted 4 years ago by [mrvutuanhoang](#)

mả mẹ chúng mày Jade Jade con cặc ko chỉ cách dùng bắt bố mày vẽ bằng chân à

This post is visible to everyone.

- +
- ★
- ...

0 responses

Calculator

3/16/24, 12:47 PM

Worked Examples | 3. CMOS | Computation Structures 1: Digital Circuits | edX

Preview

Submit

< Previous

Next >

© All Rights Reserved



edX

- About
- Affiliates
- edX for Business
- Open edX
- Careers
- News

Legal

- Terms of Service & Honor Code
- Privacy Policy
- Accessibility Policy
- Trademark Policy
- Sitemap
- Cookie Policy
- Your Privacy Choices

Connect

- Idea Hub
- Contact Us
- Help Center
- Security
- Media Kit



© 2024 edX LLC. All rights reserved.
深圳市恒宇博科技有限公司 [粤ICP备17044299号-2](#)