Tutorial: Caches

Caches: 2

2/2 points (ungraded)

Two otherwise-identical Beta systems have 1024-line two-way set-associative caches using LRU and FIFO replacement, respectively. For what programs does the **FIFO** cache show a higher hit ratio than the LRU cache?

FIFO outperforms on:

- ○ **ALL**
- ○ **MOST**
- ◉ **A FEW**
- ○ **NONE**

✔

Explanation

Generally, the LRU replacement strategy will perform better than other replacement strategies. However, there are some cases where the behavior of FIFO replacement will happen to do better due to the way in which the data is accessed in the program.

Two otherwise-identical Beta systems have fully-associative LRU caches. One cache has four lines, each caching a single 32-bit word; the other cache has eight lines, each also holding a single 32-bit word. For what programs does the **smaller** cache show a higher hit ratio?

***Small* cache outperforms on (circle one):**

- ○ **ALL**
- ○ **MOST**
- ○ **A FEW**
- ◉ **NONE**

✔

Explanation

The larger cache has all the locations of the smaller cache so if the smaller cache hits, so will the larger cache.

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Answers are displayed within the problem

Caches: 1

0.0/1.0 point (ungraded)

1. You are evaluating two tiny 4-line caches, each with a total storage of four data words. Model DM is direct-mapped, and model FA is fully associative (LRU). Each uses **word addressing** (hence consecutive addresses differ by 1, not 4 as in the Beta). The benchmark involves just six memory reads, starting with an empty (invalidated) cache. Finish the reference string given below to yield an access pattern that will give a **better hit rate on DM than on FA**. Fill in the final two additional memory addresses. **Use single-digit decimal addresses.**

   0, 1, 2, 3, [ ] , [ ]

2. Same setup as above; this time give references that make FA look better. Again, **use single-digit decimal addresses.**

   0, 1, 2, 3, [ ] , [ ]

Calculator

0, 1, 2, 3, [ ] , [ ]

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Caches: 2

9 points possible (ungraded)

You are considering three possible caches for use in a Beta-like computer system that uses 24-bit byte addresses to access 32-bit (4-byte) words in main memory – hence each word address is divisible by four (as in the Beta).

Each of the caches you are considering has a total of 64 cache lines, each holding one 32-bit data word. The three cache models are as follows:

Cache	Description
DM	Direct-mapped, 64 lines
4Way	4-way set associative: 16 sets of 4 lines each.
FA	Fully-associative: one set of 64 lines.

To compare caches, you have collected some additional parameters about each model and have run a tiny benchmark program to measure the performance of each. Your benchmark program is a tight loop that repeatedly accesses the **4** locations given by the **hex byte addresses**:

0×100, 0×200, 0×104, 0×108, 0×100, 0×200, 0×104, 0×108, 0×100, ...

You have been asked to complete the following table. Fill in blank entries; use “NA” (Not Applicable) for inapplicable parameters.

Assume that the incoming address from the CPU is A[23:0], that each cache stores the minimum number of address bits in the tag field for each line. The “# Lines for Mem[0]” column lists the number of lines in each cache that might hold the contents of main memory location zero, and the Hit Rate column reflects each cache’s steady-state performance on the little benchmark described above.

Cache Model	Bits of A[23:0] used to address cache	# Tag bits Per line	Replacement Strategy	# Lines for Mem[0]	Hit Rate
DM	A[7:2]		Select an option	1	
4Way	A[:]		LRU		
FA	NA	22	LRU		100%

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Topic: 14. Caches and the Memory Hierarchy / Tutorial: Caches

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Problem 1 issue 4
Hi All, Regarding the first problem, I have some difficulties to understand what is requested, even with the answer! What are exactly...

Entering the hit rates. 2
For the hit rates in the CACHES: 2 question you can enter the rates as a percentage such as "23%" or as a decimal such as "0.23". ...

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