# LE18.5

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## LE18.5.1: Real-time Constraints

0.0/1.0 point (ungraded)

Three devices, D1, D2, and D3, are serviced by interrupt handlers in an interrupt system that may choose to use either strong (preemptive) priorities or weak (nonpreemptive) priorities. Their service times and maximum request rates are shown in the table below.

| Device | Service time | Maximum frequency | Deadline |
|---|---|---|---|
| D1 | 100us | 1/(1000us) | 300us |
| D2 | 150us | 1/(300us) | 240us |
| D3 | 250us | 1/(1000us) | 1050us |

1. Assuming each device were interrupting at its maximum rate, what fraction of the CPU time would be used to service **D1**? What fraction of the CPU time would be left for background computing? Answer in percent. Enter your response as "N%".

   **Give PERCENTAGE of CPU used to service D1:**

   10%  Answer: 10%

   **Give PERCENTAGE of unused CPU:**

   15%  Answer: 15%

   Explanation

   The service time for D1 is 100us and this occurs every 1000us so it uses 100/1000 = 10% of the CPU. D2 uses 150us every 300us so it uses 50% of the CPU. D3 uses 250us every 1000us, so it uses 25% of the CPU. So the unused CPU after processing D1, D2, and D3 is 100 - (10 + 50 + 25) = 15%.

2. Can the requirements given in the table above be met using a **weak** priority ordering among the interrupt requests? If so give priority ordering for D1, D2, D3 or select device(s) whose deadlines cannot be met. Select all that apply.

   **Weak priority ordering or list device(s) with possibly missed deadlines:**

   - [ ] D1 > D2
   - [ ] D1 > D3
   - [ ] D2 > D1
   - [ ] D2 > D3
   - [ ] D3 > D1
   - [ ] D3 > D2
   - [x] D1 misses deadline ✔
   - [x] D2 misses deadline ✔
   - [ ] D3 misses deadline

   Explanation

   In a weak priority system a running process does not get preempted even if it has a lower priority than the new interrupt. In this system, if D1 or D3 are running when a D2 interrupt arrives, then D2 could miss deadline. This can occur because D2's deadline of 240us is less than the service time of D1 plus D2

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its less than the service time of D3 plus D2. In addition, if D1 arrives while D3 is running, then D1 may miss its deadline.

3. Can the requirements given in the table above be met using a **strong** priority ordering among the interrupt requests? If so give priority ordering for D1, D2, D3 or select device(s) whose deadlines cannot be met. Select all that apply.

**Strong priority ordering or list device(s) with missed deadlines:**

- [ ] D1 > D2
- [x] D1 > D3 ✔
- [x] D2 > D1 ✔
- [x] D2 > D3 ✔
- [ ] D3 > D1
- [ ] D3 > D2
- [ ] D1 misses deadline
- [ ] D2 misses deadline
- [ ] D3 misses deadline

Explanation
In order to guarantee that the deadlines are all satisfied, D2 cannot be delayed by either D1 or D3 because its deadline is less than the service time of D1 or D3 plus its own service time. In addition, D1 cannot be delayed by D3 because its deadline is less than the service time of D3 plus that of D1. So the priority ordering is D2 > D1 > D3.

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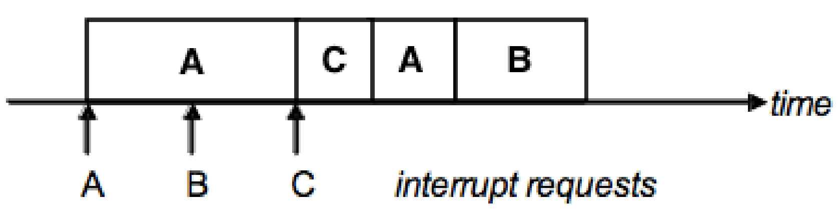
Answers are displayed within the problem

## LE18.5.2: Assigning Priorities

0.0/1.0 point (ungraded)
The following timeline shows how a processor executes interrupt handlers in response to interrupt requests (shown as ↑ in the diagram) from devices A, B and C. Assume that the processor is idle before the first interrupt request arrives.




1. Does the processor implement a weak priority system or strong priority system? If there's not enough information to decide, select "Can't Tell".

**Type of priority system (weak, strong, can't tell):**

- ( ) Weak

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- ◯ Strong
- ◯ Can't Tell

2. Indicate the relative priorities of A, B and C, e.g., select “A > B” if A has a higher priority than B. Select "None" if you can't tell. Select all that apply.

**Relative priorities of A, B and C:**

- ☐ A > B
- ☐ A > C
- ☐ B > A
- ☐ B > C
- ☐ C > A
- ☐ C > B
- ☐ None

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