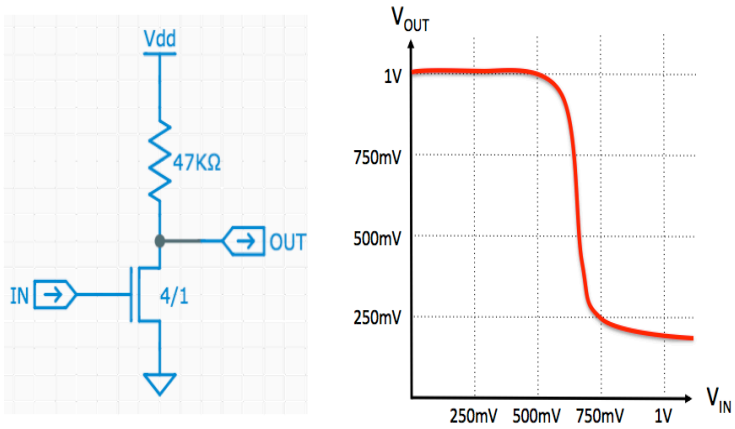
Tutorial : Static Discipline

Static Discipline

3/3 points (ungraded)

Before CMOS came on the scene, the industry tried using NMOS logic where the pulldown network was made of NFETs, but the pullup was a simple resistor. The schematic for an RTL inverter is shown below, along with a plot of its voltage transfer characteristic (VTC) in a system with a 1V power supply, using NFETs with a 0.5V threshold.



Using the information from the VTC please determine the appropriate digital signaling specification, one that provides for positive noise margins of at least 0.25V. Assume that VOL has already been chosen to be 250mV. Please give a numeric answer to the nearest .05 volt.

Voltage value for V_{OL} (V): 0.25

Voltage value for V_{IL} (V): 0.5 ✔

Voltage value for V_{IH} (V): 0.75 ✔

Voltage value for V_{OH} (V):

1 ✔

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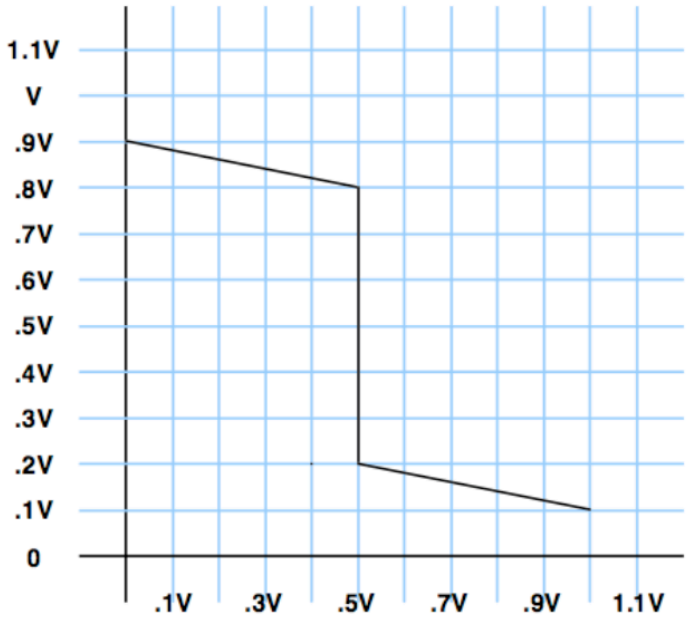
Static Discipline

3/3 points (ungraded)

Consider a device whose voltage transfer characteristic is specified as a function of the supply voltage V as follows:



Calculator

0 .2V .4V .6V .8V V

Note that the device has a sharp (infinite gain) threshold at 0.5V.

Using this device as an inverter, if V_{OL} is chosen to be 0.2V, what value for V_{IH} will maximize the high noise margin? Please give a numeric answer to the nearest .1 volt. If it is impossible to tell, write "NONE".

V_{IH} that maximizes high noise margin (V): 0.5 ✔

What is the maximum noise immunity that can be realized using this device as an inverter, with an appropriately chosen signaling specification? Please give a numeric answer to the nearest .1 volt. If it is impossible to tell, write "NONE".

Maximum noise immunity (V): 0.3 ✔

Suppose manufacturing variations for the above device now allow the threshold voltage to vary between 0.4V and 0.6V, rather than always being 0.5V exactly. If the signaling specifications were adjusted to accommodate this variation, what would be the maximum possible noise immunity? Please give a numeric answer to the nearest .1 volt. If it is impossible to tell, write "NONE".

Adjusted maximum noise immunity (V): 0.2 ✔

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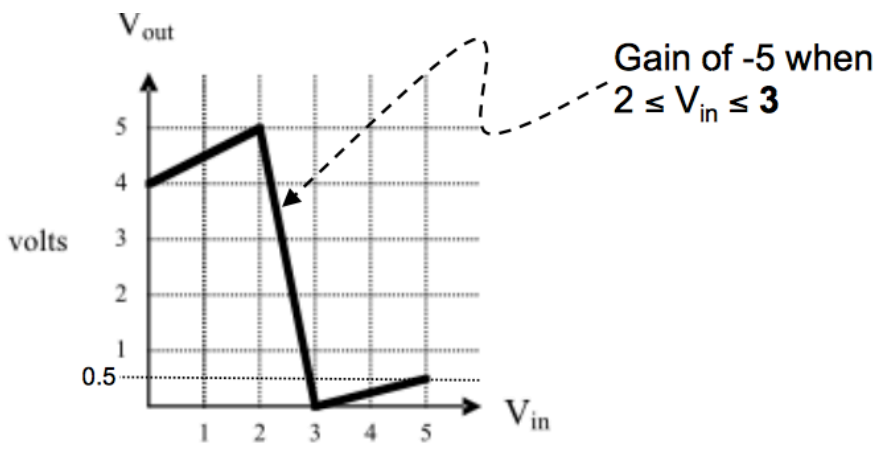
Static Discipline

9/9 points (ungraded)

BioBits, a Cambridge startup, has discovered how to synthesize a tiny virus, VIR1, which can be used as a single-input, single-output electronic component. They have observed the following voltage transfer relationship for their VIR1 component:



volts

BioBits proposes to use this device as an inverter in a system where signal voltages may vary between 0 (ground) and the 5V supply voltage.

(A) Give values of V_{OL}, V_{IL}, V_{IH}, and V_{OH} which yield at least 1-volt noise margins when this device is used as an inverter. Please give a numeric answer to the nearest .05 volt.

V_{OL}: 0.5 ✔

V_{IL}: 2 ✔

V_{IH}: 3 ✔

Calculator

V_{OH}: 4 ✔

(B) A related virus, VIR2, yields precisely the same voltage transfer curve as VIR1, except that its behavior is completely unpredictable for V_{in} between 2 and 3 volts. Not only do individual VIR2 devices differ within this range, but each VIR2 device seems to produce a different, random output between 0 and 5 volts when given V_{in} between 2 and 3 volts. Can the VIR2 device also be used as an inverter, with 1-volt noise margins?

- (●) Yes
- ( ) No
- ( ) Can't Tell

✔

(C) [NOTE: This question is a bit tricky. Don't work on this part until you're happy with your other answers!] Noise immunity is defined as the smaller of the two noise margins. Give values of V_{OL}, V_{IL}, V_{IH}, and V_{OH} which achieve the highest noise immunity you can manage for the VIR1 device used as an inverter. Please give a numeric answer to the nearest .1 volt.

V_{OL}: 1 ✔

V_{IL}: 2.2 ✔

V_{IH}: 2.8 ✔

V_{OH}: 4 ✔

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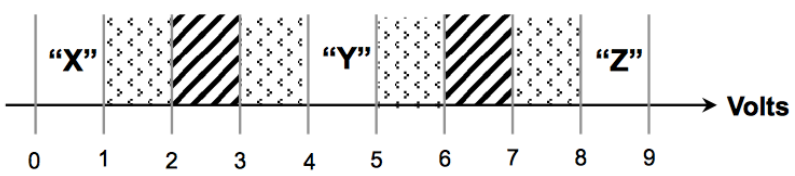
Static Discipline

5 points possible (ungraded)

A group of scientists have colonized Triton and are building combinational logic devices using a three- value or ternary logic system, rather than the 2-value (0 and 1) logic we use in 6.004. The three logic levels are designated X, Y, and Z; logic circuits on Triton represent each such logic value as a voltage between 0 and 9 volts, using the following convention for mapping voltages to logic levels, noise margins, or forbidden zones:



The boxes with bold diagonal lines correspond to the forbidden zones.

(A) What is the noise immunity of this representation scheme? Recall that noise immunity is defined as the smallest of the noise margins.

Noise immunity of Triton logic (V): Answer: 1

Calculator

Explanation
The noise margins correspond to the areas where the input value is considered valid but the output is not. This corresponds to the areas shaded with < and > signs. There are 4 noise margins in a ternary device and each of them is 1V, so the noise immunity is also 1V.

We've seen that there are 16 2-input Boolean functions using binary (2-valued) logic.

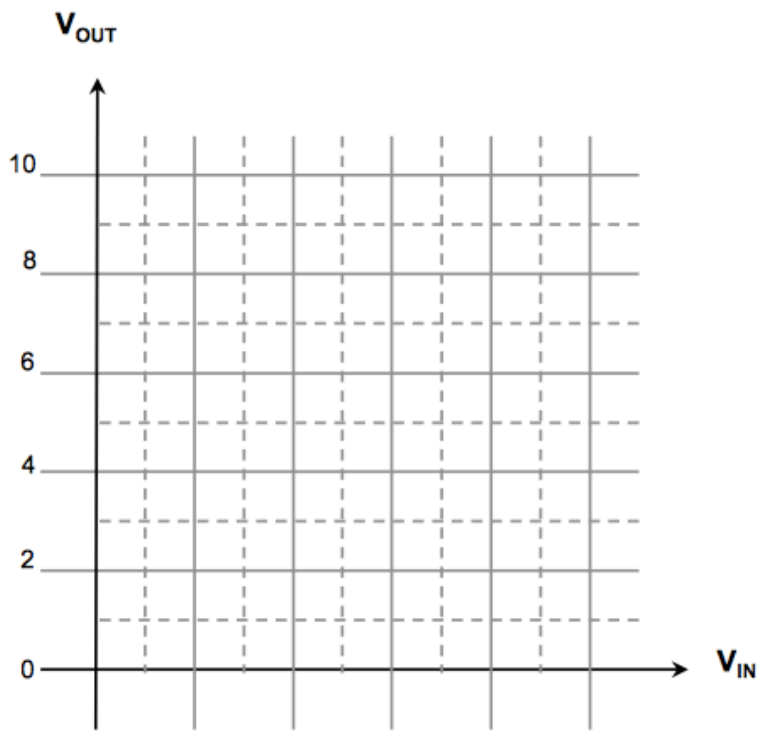
(B) How many ternary functions are there of two (ternary) inputs? You may answer with a number or a simple formula (you can use X^Y to represent X^Y).

Number of 2-input ternary functions: Answer: 3^9

Explanation
With two value logic, two inputs have $NumLogicValues^{NumInputs} = 2^2 = 4$ possible input combinations. Each unique set of outputs for those 4 inputs defines a distinct function. So the number of functions for two value, 2 input logic is $NumLogicValues^4 = 2^4 = 16$.
Using two input ternary (3) logic, there are $3^2 = 9$ possible input combinations. Each unique set of outputs for those 9 input combinations defines a distinct function. So the number of functions for three value, 2 input logic is 3^9.

In lecture, we observed that the voltage transfer curve for a 1-input, 1-output device that obeys the static discipline in our standard 2-value logic must not go through either of two disallowed regions of the Vout-Vin plane.

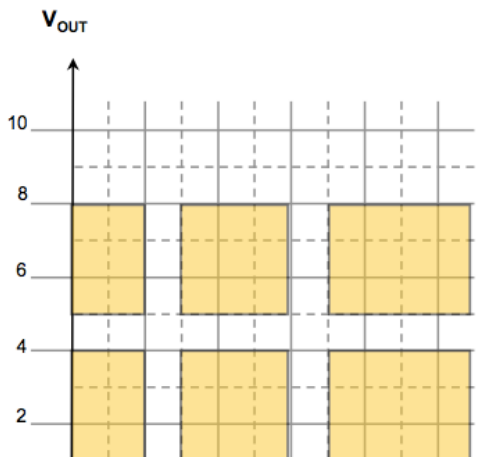
For the following questions, you may want to use graph paper to sketch regions disallowed by the above ternary logic convention, for your use in answering subsequent questions. Alternatively, you can print the following graph and sketch on it.



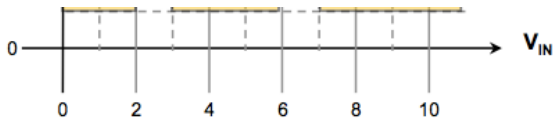
(C) How many regions are disallowed for 1-input, 1-output ternary devices which obey the static discipline?

Number of regions to avoid: Answer: 6

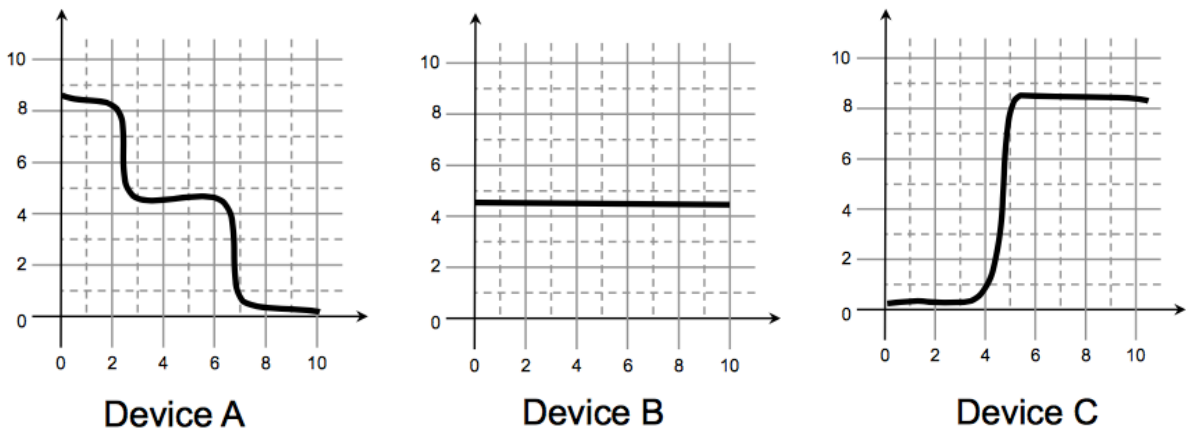
Explanation
As shown below, there are 6 areas through which the voltage transfer curve cannot pass if we want to produce a valid ternary logic device.



Calculator



Three electronic devices which are easy to manufacture from readily available elements on Triton have the following voltage transfer curves.

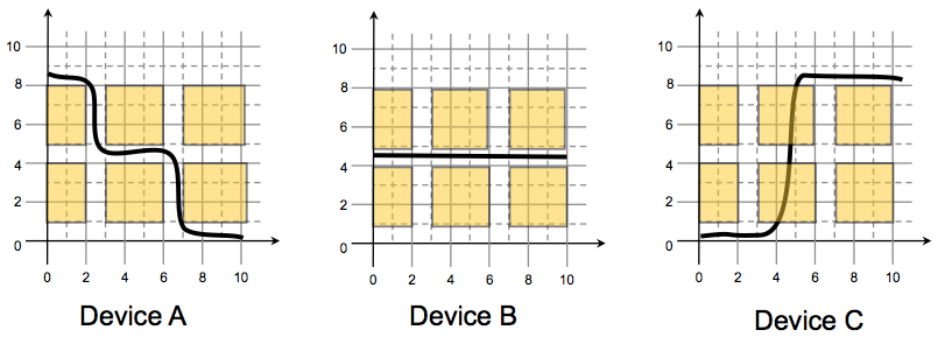


(D) Which of the above devices constitutes a valid ternary combinational device, using the voltage representation conventions given above? Select all that apply.

- [ ] Device A ✔
- [ ] Device B ✔
- [ ] Device C

Explanation

The voltage transfer curves for devices A-C are shown below transposed on top of the image that shows the disallowed regions for the voltage transfer curve.

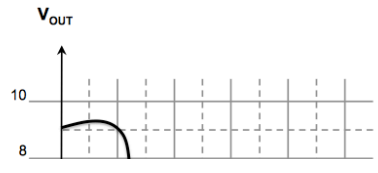


Device A describes a voltage transfer curve that is inverting (low inputs produce high outputs and high inputs produce low outputs valid inputs in the middle range produce outputs in the middle range).
Device B also describes a valid voltage transfer curve that avoids the regions that we are not permitted to cross, thus it too constitutes a valid ternary combinational device, however, it's output is uninteresting because it always produces the middle range output regardless of the input.
Device C passes through the disallowed regions, so it does not describe a valid ternary device.

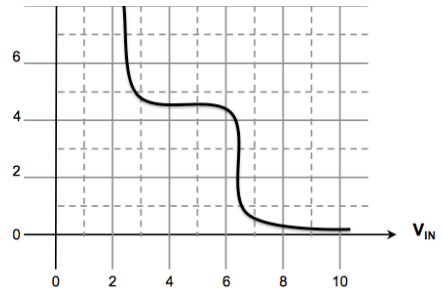
A ternary buffer is a 1-input 1-output ternary combinational device (obeying the static discipline dictated by the above voltage representation conventions) whose output settles, after a propagation delay, to the ternary logic value applied at its input. A truth table for a ternary buffer is shown below.

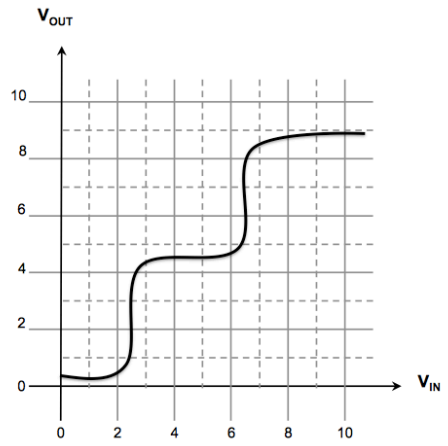
IN	OUT
X	X
Y	Y
Z	Z

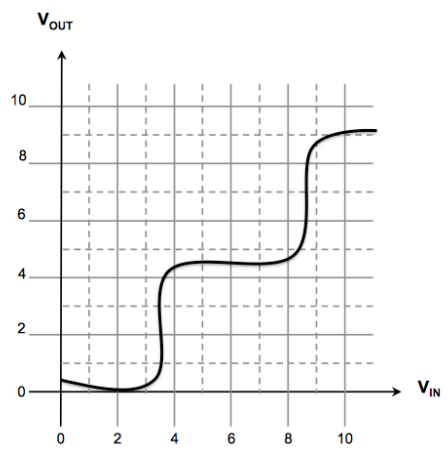
(E) Which of the following voltage transfer curves constitutes a valid ternary buffer using the above truth table and ternary logic representation conventions.



Calculator



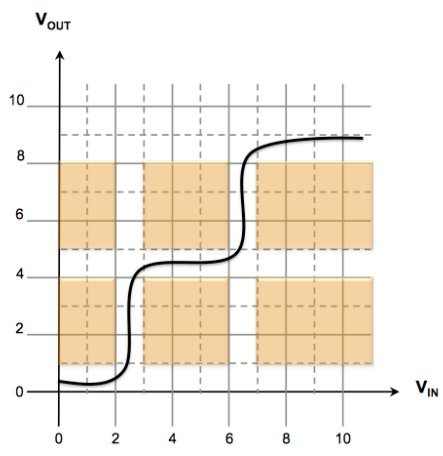




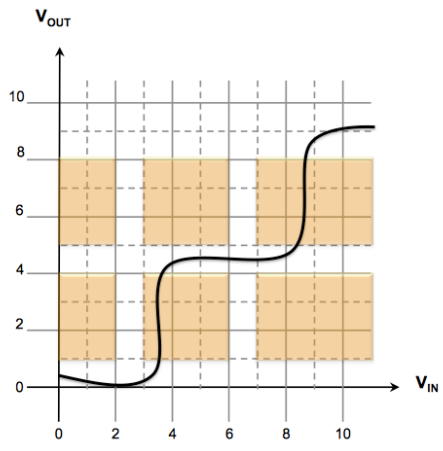
Explanation

Transfer curve A descibes an inverting function but the truth table is defining a non-inverting function, so A is false.

Transfer curve B describes a ternary non-inverting device which satisfies the truth table and the ternary logic conventions of this problem, as shown in the image below.



Transfer curve C describes a ternary non-inverting device, but its curve passes through the forbidden regions, as shown below, so C is false.



Calculator

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Answers are displayed within the problem

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☑	Regarding Static discipline Part A In the last question of part A when we are pushing Vil and Vih to forbidden region to maximise noise immunity , I can see that Vil ca...	2
💬	purpose of forbidden zone? In question 2, the device has a sharp (infinite gain) threshold at 0.5V. Since there is no forbidden zone between VIH and VIL, does t...	4
💬	Static Discipline - Question C Combinational devices should exhibit a gain higher than 1; Isn't it ? The VTC for device B doesn't seam to follow this rule. Any clarifi...	3
☑	Static Discipline - question b I still don't understand question B. By my reasoning, there are nine possible inputs (00,01,11,10,02,22,20,12,21). Any of these could yi...	4

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