

Computation Structures 3: Computer Organization

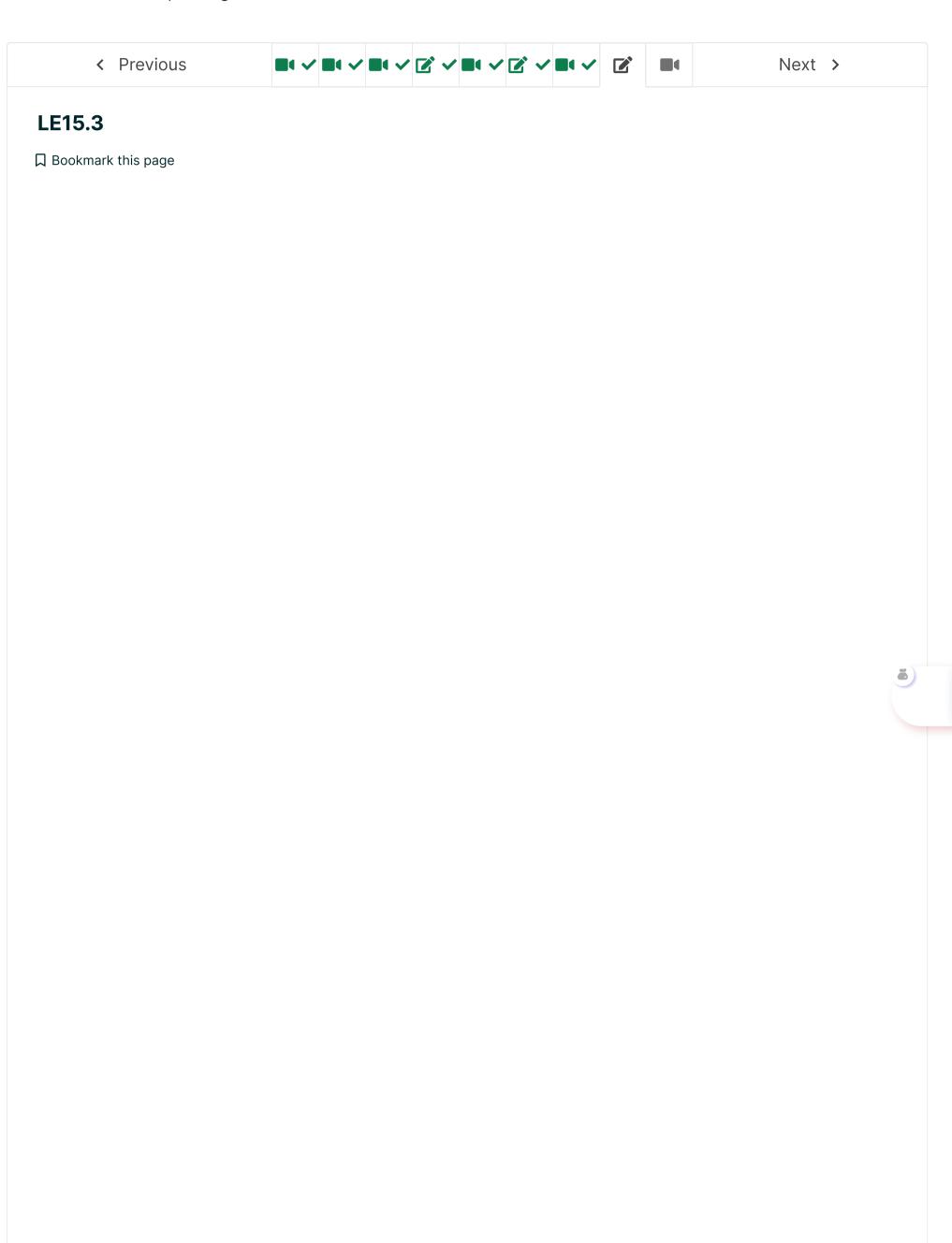
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☆ Course / 15. Pipelining the Beta / Lecture Videos (50:06)



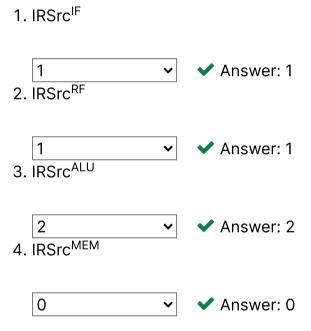
For all Beta related questions, you should make use of the <u>Beta documentation</u>, the <u>Beta Instruction</u> **Summary**, the **Unpipelined Beta Diagram** and the **Pipelined Beta Diagram**.

LE15.3.1: Exceptions

1/1 point (ungraded)

An ambitious 6.004x student has enhanced the 5-stage pipelined Beta to trigger an exception in the ALU stage when there's an attempt to divide by zero, i.e., when the B operand of the ALU is zero and the opcode of the instruction in the ALU stage is DIV or DIVC.

For each of the following control signals, indicate its value during the clock cycle when the divide-by-zero exception occurs.



Explanation

Since the exception occurs in ALU stage, that's the stage for which we want to capture the PC+4 of the instruction that triggered the exeption. So IRSrcALU is 2.

When there's an exception in the ALU stage, we have to annul the instructions earlier in the pipeline, since in the program they came after the instruction that caused the fault and hence should not be executed. So IRSrcIF and IRSrc^{RF} are both 1.

Instructions in later pipeline stages are unaffected by the exeception in the ALU stage. So IRSrcMEM is 0.

Submit

1 Answers are displayed within the problem

LE15.3.2: Bypassing, stalls, annulment

0.0/1.0 point (ungraded)

The loop below has been executing for a while on our standard 5-stage pipelined Beta with full bypassing and speculation on branches (i.e., instruction in IF stage is annulled when there's a taken branch in the RF stage). The pipeline diagram below shows the opcode of the instruction in each pipeline stage during 9 consecutive cycles of execution.

```
LOOP:
       LD(R0, 0, R2)
       SHLC(R1, 1, R1)
       ADD(R1, R2, R1)
       ADDC(R0, 4, R0)
       CMPEQC(R0, aend, R2)
       BNE(R2, L00P)
       ST(R1, hash, R31)
```

Cycle # 200 201 202 203 204 205 206 207 208

			Lecti	ure Videos (50	0:06) 15. Pip	elining the Beta I C	Computation Structu	res 3: Computer O	rganization edX
	LD	SHLC	ADD	ADDC	ADDC	CMPEQC	BNE	ST	LD
	NOP	LD	SHLC	ADD	ADD	ADDC	CMPEQC	BNE	NOP
	BNE	NOP	LD	SHLC	NOP	ADD	ADDC	CMPEQC	BNE
1	CMPEQC	BNE	NOP	LD	SHLC	NOP	ADD	ADDC	CMPEQC
	ADDC	CMPEQC	BNE	NOP	LD	SHLC	NOP	ADD	ADDC
t	o the RF sta		iple byp						a from a later pipeline stage elect all that apply.
		ss from ALU							
	Bypas	ss from MEI	M to RF						
	Bypas	ss from WB	to RF						
	Bypas	pass paths ss from ALL ss from MEI	J to RF						
	Bypas	ss from WB	to RF						
		pass paths ss from ALL							
	Bypas	ss from MEI	M to RF						
	Bypas	ss from WB	to RF						
C	Cycle 203:								
	No by	pass paths	used						
	Bypas	ss from ALU	J to RF						
	Bypas	ss from MEI	M to RF						

Cycle 204:

Bypass from WB to RF

	No bypass paths used
	Bypass from ALU to RF
	Bypass from MEM to RF
	Bypass from WB to RF
Cycle	205:
	No bypass paths used
	Bypass from ALU to RF
	Bypass from MEM to RF
	Bypass from WB to RF
Cycle	206:
	No bypass paths used
	Bypass from ALU to RF
	Bypass from MEM to RF
	Bypass from WB to RF
Cycle	207:
	No bypass paths used
	Bypass from ALU to RF
	Bypass from MEM to RF
	Bypass from WB to RF
Cycle	208:
	No bypass paths used
	Bypass from ALU to RF
	Bypass from MEM to RF
	Bypass from WB to RF

For the following questions think carefully about when a signal would be asserted in order to produce the effect you see in the pipeline diagram. Select all the cycles that apply, or select NONE if it never occurs.

2.	During	g which cycle(s), if any, would the IRSrc ^{IF} signal be 1?	
		200	
		201	
		202	
		203	
		204	
		205	
		206	
		207	
		208	
		NONE	
3.	Durino	g which cycle(s), if any, would the IRSrc ^{RF} signal be 1?	
		200	
		201	
		202	
		203	
		204	•
		205	
		206	
		207	
		208	
		NONE	
1	Durina	g which cycle(s), if any, would the IRSrc ^{ALU} signal be 1?	
•		200	
		201	
		202	
		203	
		204	

5. Duri	NONE ing which cycle(s), if any,	would the STALL contro	ol signal be 1, i.e., cyc	le(s) when the IF a	and RF stages
wou	uld be stalled?				
	201				
	202				
	203				
	204				
	205				
	206				
	207				
	208				
	NONE				
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