LE6.4

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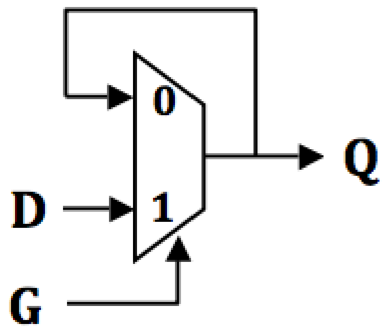
LE6.4.1 Metastability in latches

5/6 points (ungraded)



Assume that we have made a transparent latch using a lenient 2-input MUX as shown above. The lenient MUX has a propagation delay of t_{PD} and a contamination delay of t_{CD}.

A certain sequence of inputs -- violating the dynamic discipline -- has caused the Q output to assume an invalid voltage. You have observed the voltage at Q at this value for an interval many times larger than t_{PD}, despite valid stable inputs at D and G during this interval.

For each of the following statements, please indicate either TRUE or FALSE, assuming you are observing an invalid Q output after this relatively long interval of valid D and G inputs.

(A) The G input must be 0.

- ( ) True ✔
- (•) False

✖

Explanation
A invalid output can only persist when the latch is in "memory mode", i.e., when G is 0. When G is 1, the latch is a simple combinational device which will produce a valid and stable output within t_{PD} of a transition on the D input.

(B) The D input must be 1.

- ( ) True
- (•) False

✔

Explanation
The metastable condition is caused by entering memory mode when Q is near the metastable voltage, which can happen on both a rising or falling transition on D.

(C) Setting and holding G=1 (while D remains valid and stable) will assure a stable value at Q after a delay of t_{PD} .

- (•) True
- ( ) False

✔

Explanation
As mentioned in the explanation for (A), when G is 1, the latch is a simple combinational device which will produce a valid and stable output within t_{PD} of a transition on the D input.

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(D) Setting and holding G=1 for t_{PD} and returning it to 0 for another t_{PD} (while D remains valid and stable) will assure that the value at D appears at Q.

- [ ] True
- [x] False

✔

Explanation
The second 1-to-0 transition on G doesn't meet the latch's setup time, which may cause the latch to go metastable again. If G had been 1 for $2 \cdot t_{PD}$ then the value at D would have been guaranteed to be the value at Q.

(E) If the inputs remain unchanged (stable and valid) for an interval of T seconds, the probability of a valid Q output at the end of this interval increases exponentially with T.

- [x] True
- [ ] False

✔

Explanation
The probability of a positive feedback loop being metastable decreases exponentially with time.

(F) Assuming the valid stable inputs remain at D and G, once Q leaves the metastable state and reaches a valid logic level it is guaranteed to have the same value as D.

- [ ] True
- [x] False

✔

Explanation
A metastable latch can resolve to either of the two possible stable states, independently of the value of D. Bascially, metastability causes the latch to "forget" the D input value.

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