FSM implementation

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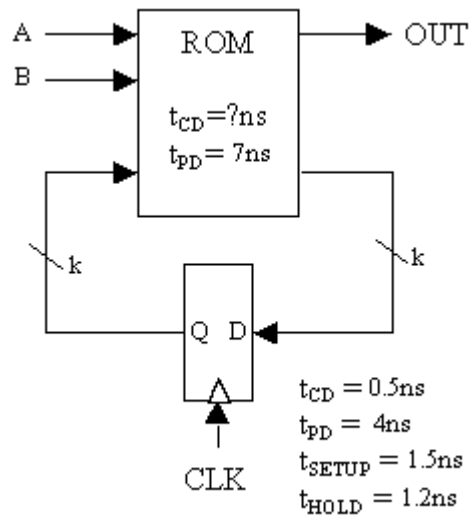
Lab due Oct 31, 2016 21:59 -02 Past due

FSM implementation

0.0/2.0 points (graded)

A possible implementation of a finite state machine with two inputs and one output is shown below.



1. If the register is 5 bits wide (i.e., k = 5) what is the appropriate size of the ROM? Give the number of locations and the number of bits in each location.

   Number of locations: Answer: 128

   Number of bits in each location: Answer: 6

2. If the register is 5 bits wide what is the maximum number of states in an FSM implemented using this circuit?

   Maximum number of states? Answer: 32

3. What is the smallest possible value for the ROM's contamination delay that still ensures the necessary timing specifications are met?

   Smallest possible value for t_{CD} (in ns): Answer: 0.7

4. Assume that the ROM's $t_{CD} = 3\text{ns}$. What is the shortest possible clock period that still ensures that the necessary timing specifications are met?

   Smallest clock period (in ns): Answer: 12.5

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Answers are displayed within the problem

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FSM implementation Q1.B

1.B) Number of bits in each location: N if the number of locations in memory are 2^N. But the grading system is showing wrong for ... 5

Calculator

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Calculator