

Computation Structures 2: Computer Architecture







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☆ Course / 9. Designing an Instruction Set / Lecture Videos (52:28)



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LE9.3.1: ALUC Instructions

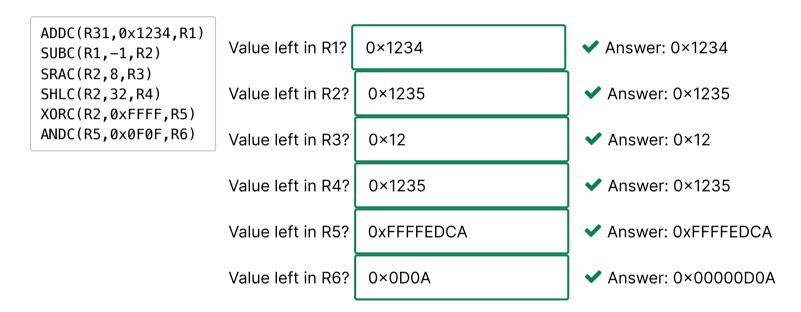
1/1 point (ungraded)

- Summary of Instruction Formats (PDF)
- Beta Documentation (PDF)

For the Beta instruction sequence shown below, indicate the 32-bit two's complement values of the specified registers after the sequence has been executed by the Beta. The effect of the instructions is cumulative, later instructions use the values stored by earlier instructions.

You can find detailed descriptions of each Beta instruction in the "Beta Documentation" handout -- see link above. Remember that register values and the ALU use a 32-bit two's complement representation.

Hint: You can enter answers in hex by specifying a "0x" prefix, *e.g.*, 17 could be entered as "0x11". Usually one would enter addresses, values in memory, etc. using hex. You can also use a "0b" prefix to enter a binary value, e.g., "0b10001".



Explanation

ADDC(R31, 0×1234 ,R1) adds 0 to $0 \times 1234 = 0 \times 1234$

SUBC(R1,-1,R2) 0×1234 - (-1) = 0×1235 . Subtracting -1 is the same as adding 1.

SRAC(R2,8,R3) shifting 0×1235 right by 8 bits gives 0×12 . Since the A operand was positive, the arithmetic right shift used 0 to fill in the vacated bits.

SHLC(R2,32,R4) The answer is 0×1235 , i.e., the value from R2 is unchanged. The insight here is that the shift instructions only use the bottom 5-bits of the B operand to determine the shift count. 32 = 0b100000, so the shift amount is 0.

 $XORC(R2,0\times FFFF,R5)$ the 0xFFFF second operand will be sign-extended to 0xFFFFFFF. XORing with all 1's gives the bit-wise complement of $0\times 00001235 = 0xFFFFEDCA$

ANDC(R5,0x0F0F,R6) ANDing 0xFFFFEDCA with 0×00000F0F gives 0×00000D0A. ANDC is often used to select particular groups of bits from the A operand, an operation called "masking".

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1 Answers are displayed within the problem

LE9.3.2: Do we need SUBC?

1/1 point (ungraded)

A 6.004 student here at MIT has proposed that all SUBC instructions of the form

SUBC(Rx,const,Ry)

can be replaced by an ADDC that uses the negative of the constant:

ADDC(Rx,-const,Ry)

Is the student on to something? Will this transformation work for all SUBC instructions?

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l (🔵) No. ther	
113, 1131	e are SUBC instructions with no ADDC equivalent
~	
Explanation	
-	SUBC instruction with no ADDC equivalent:
SUBO	C(Rx,0x8000,Ry)
field 0×8000 w of the ALUC si	vith the proposed transformation is that when executing an ALUC instruction, the 16-bit constan vill be sign-extended to 0xFFFF8000. The negative of this value is 0×00008000, which, because gn extension, cannot be represented in the 16-bit constant field in the proposed ADDC instruction 8000, Ry) adds 0xFFFF8000 to the value in register Rx, but SUBC(Rx, 0x8000, Ry) adds 0×00008000
Submit	
• Answers	are displayed within the problem
LE9.3.3: AI	UC Instruction Encoding?
0.0/1.0 point (ung	
	e 32-bit binary encoding for each of the ALUC instruction shown below.
"assembler") w	n translating the symbolic form of the ALUC instruction into binary, the program (called the version of the version will only use the low-order 16 bits of the value provided by the second operand, even if the
value requires	more than 16 bits to represent correctly. Our assembler is dumb :(
One other note symbols as sho	
One other note symbols as sho constant 17.	more than 16 bits to represent correctly. Our assembler is dumb :(e: we've been using the symbol R0 to represent register 0. The assembler knows to treat the Rx
One other note symbols as sho constant 17.	more than 16 bits to represent correctly. Our assembler is dumb :(e: we've been using the symbol R0 to represent register 0. The assembler knows to treat the Rx orthand for the decimal constant x, e.g., R17 is a more readable alternative to specifying the
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