

Playing by our pipelining rules, we always add a register to the output. To increase the throughput, we need to add another contour that bisects the circuit. The cheapest place to do this is just before the "4" module, requiring two additional registers.

(C) If we are required to add exactly 5 registers, what is the best throughput we can achieve?

Maximum throughput (1/ns):

✗ Answer: 1/5

Explanation

The best throughput we can achieve with 5 registers is 1/5: place 3 (!) registers on the output and two registers on the arcs leading to the "4" module. If we use 4 registers to divide the circuit between the "2" and "3" modules and place one on the output, the resulting throughput is 1/7.

(D) If we can add as many registers as we like, what is the upper bound on the throughput we can achieve?

Maximum throughput (1/ns):

✓ Answer: 1/4

Explanation

1/4, because the best we can do by just adding registers is to segregate the "4" module into its own pipeline stage.

(E) If we can add as many registers as we like, what is the lower bound on the latency we can achieve?

Minimum latency (ns):

✓ Answer: 9

Explanation

Lower bound on latency = 9. We can never make the latency less by adding pipeline registers; usually the latency increases.

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LE7.2.2 Pipelining Combinational Logic

2/2 points (ungraded)

A combinational circuit C, built entirely from 2-input NAND gates having a propagation delay of 2 ns, has a propagation delay of 20 ns. You pipeline C for maximum throughput using the minimum number of registers necessary; the registers have 1ns setup time and 1ns propagation delay. What would you expect for the latency of the resulting pipeline?

Latency of pipelined version (ns):

✓ Answer: 40

Throughput of pipelined version (1/ns):

✓ Answer: 1/4

Explanation

The problem tells us that the combinational propagation delay is 20 ns for a circuit that consists entirely of NAND gates whose propagation delay is 2 ns each. This means that the longest path through the circuit consists of 10 NAND gates. In order to pipeline the circuit for maximum throughput, we need to split the circuit into 10 pipeline stages each of which contains exactly one of these 10 NAND gates. So our longest path now looks like a NAND gate followed by a pipeline register repeated 10 times. The clock period of this pipelined circuit needs to allow sufficient time for the propagation delay of the pipeline register, the propagation delay of the NAND gate and the setup time of the next register. This means that the clock period = 1 + 2 + 1 = 4 ns and throughput is $1/\text{clock_period} = 1/4$. The latency of our pipelined circuit is the number of stages times the clock period which is $10 * 4 = 40$ ns.

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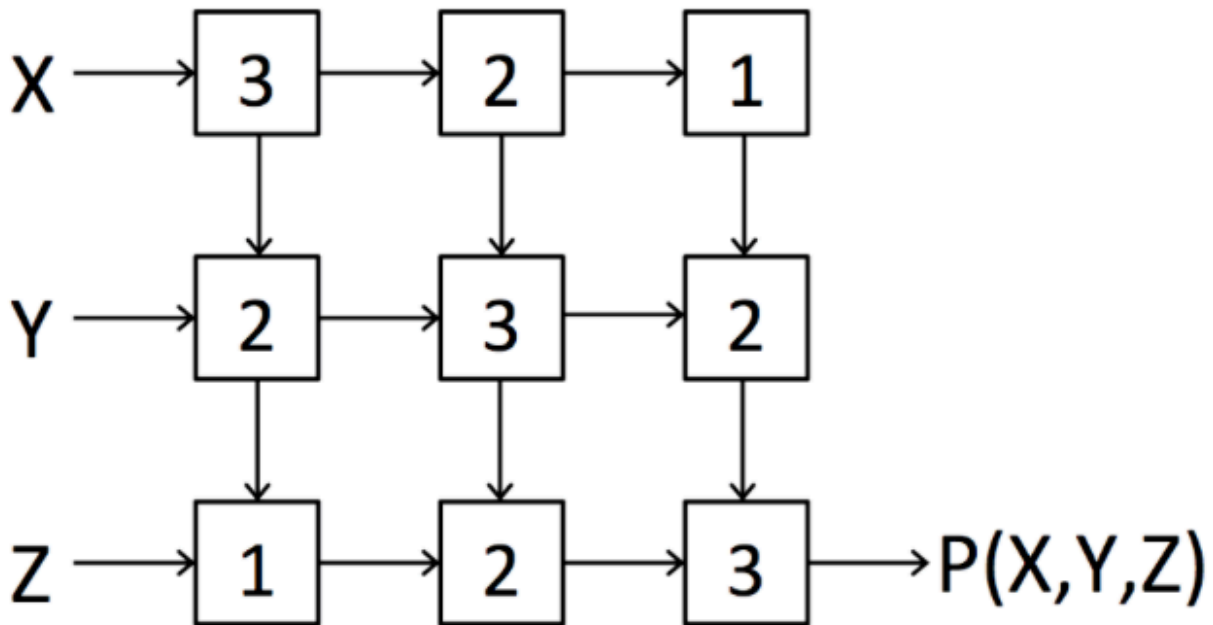
i Answers are displayed within the problem

LE7.2.3 Building a Pipeline

5 points possible (ungraded)

The top-secret diagram of the NSA's phone call tracking circuitry is shown below. We don't know what the boxes do, but we do know their t_{PD} (annotated inside each component) and how they are connected.

You've been hired to do a design study looking into pipelining the circuit above. Assume that the pipeline registers have $t_{CD} = 0$, $t_{PD} = 0$, $t_{SETUP} = 1$, $t_{HOLD} = 0$. Recall that using our pipelining convention, each pipelined circuit must have at least 1 register on the P(X,Y,Z) signal.

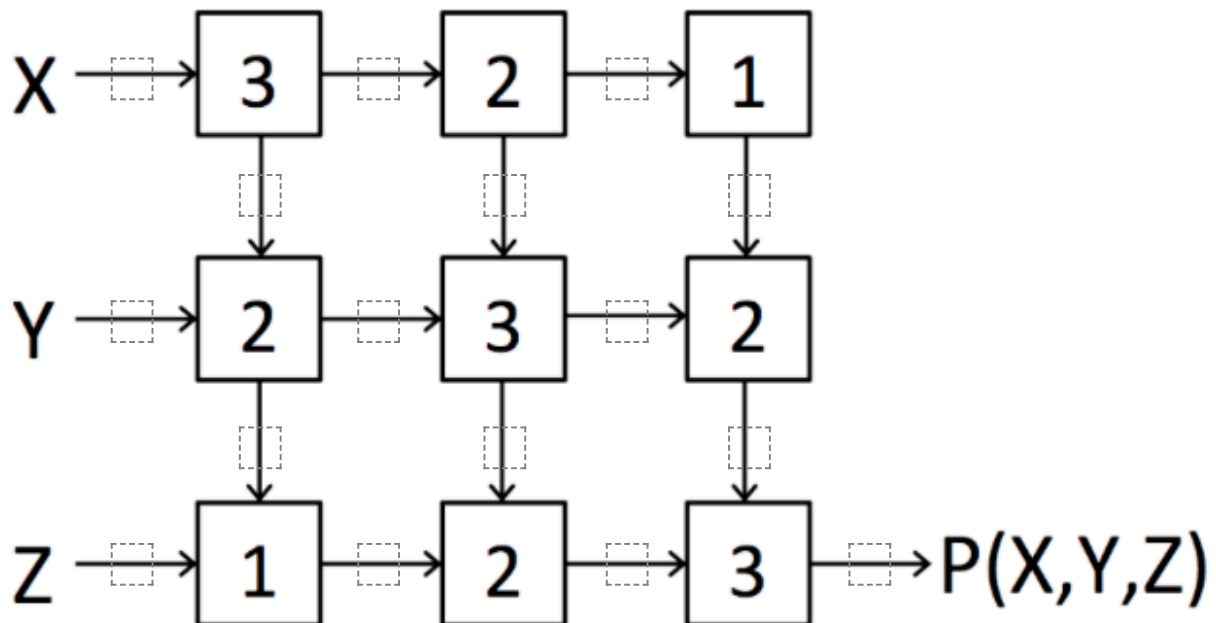


What are the latency and throughput of a 1-pipeline implementation?

Latency:

Throughput:

Add pipeline boundaries to the circuit, choosing the boundaries to achieve maximum throughput. Use the minimum number of registers necessary to achieve this throughput. Provide your answer by dragging the correct number of pipeline registers onto each of the dashed square boxes.





What are the latency and throughput of your pipelined circuit?

Latency:

Throughput:

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- 💬 If you need help 2

Watch this lecture if you need some help regarding methodology of pipelining <https://nptel.ac.in/co...>
- ? registers on the input of NSA's whatever.. 2

I got the question right but this contrary to what we have already learned, i.e we learned not to put...
- 💬 Why is it required to use a register in the final stage output of a pipeline? 4

I know it is required to use a register to remember the output in the pipeline middle stage, but why...
- ✓ Note that from every input to output path there must be exactly the same number of pipeline registers for your solution to be valid? 2

Why "Note that from every input to output path there must be exactly the same number of pipeline...
- ✓ [STAFF] How to calculate tclk and Tpd at various stages of pipelining ? 2

I am absolutely confused on how to calculate Tclk and Tpd at various pipelining stages..None of m...
- ✓ 7.2.1 c and d 2
- ✓ [[STAFF]] No. of reg. in pipelining 5

[[STAFF]] I can't figure out how we obtained number of registers during pipeline implementation
- 💬 count 10

he best throughput we can achieve with 5 registers is 1/5: place 3 (!) registers on the output and t...

✓	LE7.2.3 Pipelining	5
💬	TIS-100 The whole thing starts to look a lot like TIS-100 :) I find pipelines to be fairly easy to understand aft...	2