Tutorial : Combinational Timing

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Combinational Timing

1/1 point (ungraded)

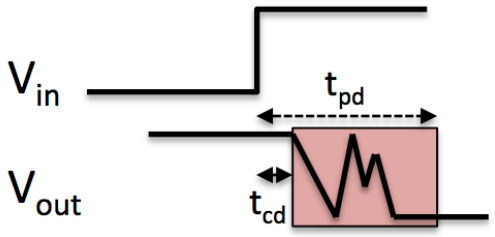
Is it possible for an inverter to have a contamination delay that is greater than it's propagation delay?

- ○ Yes
- ◉ No
- ○ Can't Tell

✔

Explanation

By definition, the contamination delay of any gate must be less than or equal to the propagation delay of that gate. Taking a look at an inverter specifically, you can visualize this using the following diagram.



If you think of the input changing instantaneously as shown here, and just think about what happens to your output, then its clear that $t_{CD} < t_{PD}$. t_{CD} measures the time from when the input changes to when the output might begin to change. t_{PD} measures the time from when the input changes to when the output becomes stable and valid with its new value. The output must enter the red zone (t_{CD}) before it can exit it (t_{PD}).

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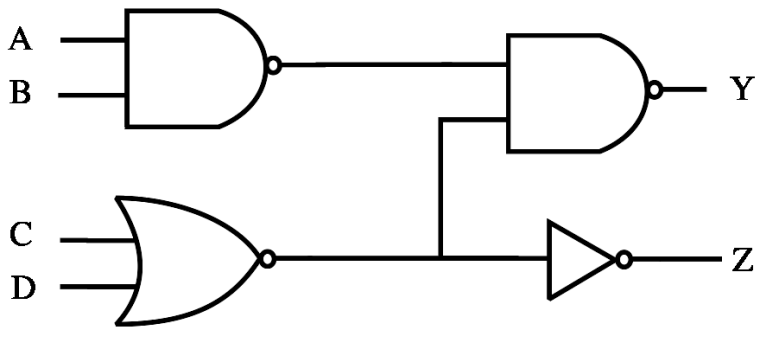
ℹ Answers are displayed within the problem

Combinational Timing

1/2 points (ungraded)



Here's a table showing the t_{CD} and t_{PD} for each of the components in the circuit above. Please compute t_{CD} and t_{PD} for the circuit as a whole.

	t_{CD}	t_{PD}
Inverter	0 ns	4 ns
NAND	1 ns	8 ns
NOR	4 ns	10 ns

Calculator

Contamination delay (ns): 4 ✖ Answer: 2

Propagation delay (ns): 18 ✔ Answer: 18

Explanation
The contamination delay of the circuit as a whole is the contamination delay of the shortest path through the circuit. Noting that the contamination delay of the inverter is less than that of the nand gate, the shortest path could either be from the A and B inputs through the two nand gates to Y, or from the C and D inputs through the nor and the inverter to Z. The path from A and B to Y has contamination delay 2*1, and the path from C and D to Z has 4 + 0. The overall contamination delay is the shortest of these two paths, which is 2 ns.

The propagation delay of the circuit as a whole is the propagation delay of the longest path through the circuit in terms of propagation delays. In this case this path is either from the A and B inputs through the two nand gates to Y, or from the C and D inputs through the nor gate and the nand gate to Y. The path from A and B has propagation delay 2*8 and the path from C and D has 10 + 8. The overall propagation delay is the longest of these two paths, which is 18 ns.

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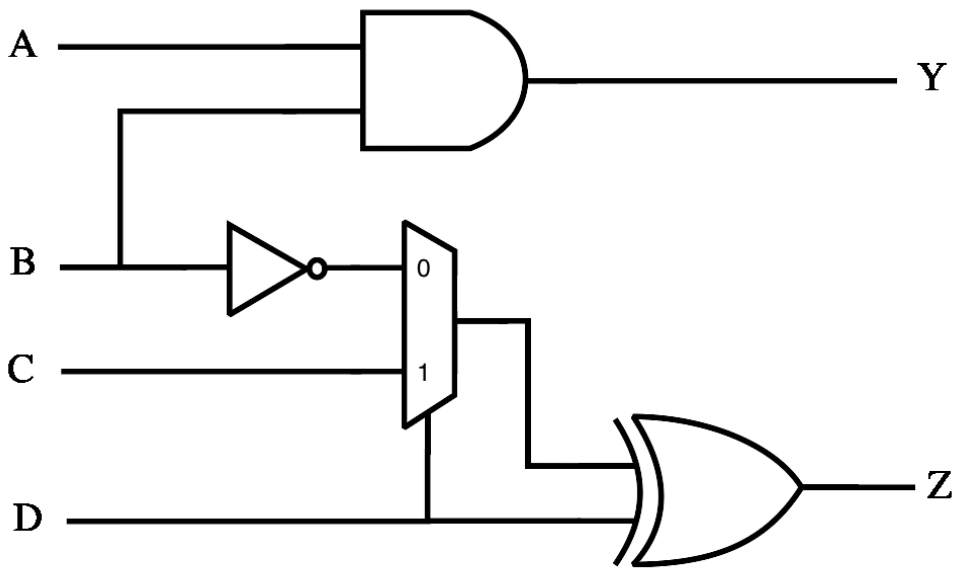
Answers are displayed within the problem

Combinational Timing

2 points possible (ungraded)



Here's a table showing the t_{CD} and t_{PD} for each of the components in the circuit above. Please compute t_{CD} and t_{PD} for the circuit as a whole.

	t_{CD}	t_{PD}
Inverter	0.1 ns	0.7 ns
AND2	0.3 ns	0.7 ns
XOR2	0.4 ns	2.2 ns
MUX2	0.1 ns	1.0 ns

t_{CD} (ns):

t_{PD} (ns):

Calculator

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- [STAFF] there is no E in 2nd graph! — 2
  Also too many paragraphs in the answer to 2nd circuit. It is a simple concept 2 paragraphs should be enough
- Combinational Timing Part 1 — 6

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Calculator