LE3.2

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LE3.2.1: CMOS Recipe

4/4 points (ungraded)

When creating CMOS circuits, NFETs can be used in your pullup and pulldown circuitry.

- ○ true
- ◉ false

✔

When creating CMOS circuits, PFETs should only be used in your pullup circuitry.

- ◉ true
- ○ false

✔

NFETs are on when their input is low (or 0).

- ○ true
- ◉ false

✔

PFETs are on when their input is low (or 0).

- ◉ true
- ○ false

✔

Explanation
In CMOS circuits, NFETs are used for your pulldown circuitry, and PFETs are used for your pullup circuitry. NFETs are on when their input, or gate, is high (1). PFETs are on when their input, or gate, is low (0).

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Answers are displayed within the problem

LE3.2.2: Inverter Rise and Fall Times

2/2 points (ungraded)

In the last video, we examined the CMOS inverter circuit consisting of a single PFET pullup connecting the output node to V_{DD} and single NFET pulldown connecting the output node to GROUND.

When the inverter's input is a digital 0, the PFET pullup is on and the NFET pulldown is off, so the voltage of the output Z rises until it reaches V_{DD}, a digital 1. The *rise time* of the output is defined as the amount of time it takes for the output voltage to rise from V_{OL} to V_{OH}.

When the inverter's input is a digital 1, the PFET pullup is off and the NFET pulldown is on, so the voltage of the output Z falls until it reaches GROUND, a digital 0. The *fall time* of the output is defined as the amount of time it takes for the output voltage to fall from V_{OH} to V_{OL}.

Calculator

In both cases, the transition time is inversely proportional to the I_{DS} of the conducting MOSFET switch: the greater I_{DS}, the smaller the transition time.

If a designer wanted to change the inverter's design to decrease the rise time, i.e., have output voltage transition more quickly to a digital 1 value, she could (select the best answer):

- decrease the WIDTH of the NFET pulldown
- increase the WIDTH of the NFET pulldown
- decrease the WIDTH of the PFET pullup
- **increase the WIDTH of the PFET pullup** ✔

If a designer wanted to change the inverter's design to decrease the fall time, i.e., have output voltage transition more quickly to a digital 0 value, she could (select the best answer):

- decrease the WIDTH of the NFET pulldown
- **increase the WIDTH of the NFET pulldown** ✔
- decrease the WIDTH of the PFET pullup
- increase the WIDTH of the PFET pullup

Explanation
To decrease the rise time, she needs to increase the I_{DS} through the PFET pullup. So she needs to increase the PFET's width. To a first approximation, the width of the NFET does not affect the rise time. Decreasing the NFET width will slightly decrease the capacitance of the NFET's drain node (i.e., the output node of the inverter) which would result in a small improvement of the rise time. But that effect is small compared to, say, doubling the width of the PFET pullup.
By the same reasoning, to decrease the fall time, she needs to increase the width of the NFET pulldown.

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Answers are displayed within the problem

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Why does increasing width increase gain? 6
I'm not sure why increasing width decreases rise/fall time. Is it because a wider electric field allows for more current or the depletio...

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