MITx 6.004.1x Ţ <u>Help</u> **Computation Structures 1: Digital Circuits Discussion Course Notes** <u>Course</u> <u>Progress</u> <u>Dates</u> ☆ Course / Assignment 3 (due Oct 31) / Lab 3: FSMs (< Previous</pre> Next > **State transition diagram** □ Bookmark this page

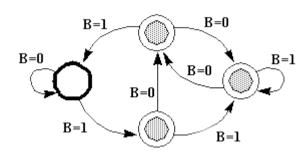
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Lab due Oct 31, 2016 21:59 -02 Past due

State transition diagram

0.0/2.0 points (graded)

Shown below is a state transition diagram for an FSM, F, with a single binary input B. The FSM has a single output, a light which is on for the three states marked by a gray dot. The starting state is marked by the heavy circle.



1. Is there a synchronizing sequence of inputs which will return this FSM from an unknown state to its starting state?

Synchronizing sequence:
00010 is such a sequence
O1010 is such a sequence
00000 is such a sequence
11101 is such a sequence
No such sequence exists

2. Does this FSM have a pair of equivalent states that may be merged to yield a 3-state FSM?

Equivalent states:

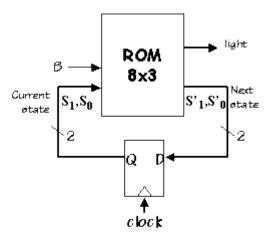
Yes; the two middle states (upper and lower) are equivalent.

Yes; the lower and rightmost states are equivalent.

Yes; the leftmost and rightmost states are equivalent.

No two states are equivalent; this FSM cannot be reduced.

3. The following circuit is used to implement the above 4-state FSM:



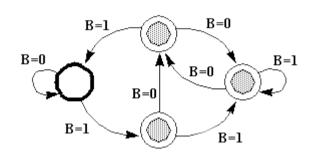
It is known that the starting state of the 4-state FSM corresponds to $S_1S_0=00$, and the **light** outp

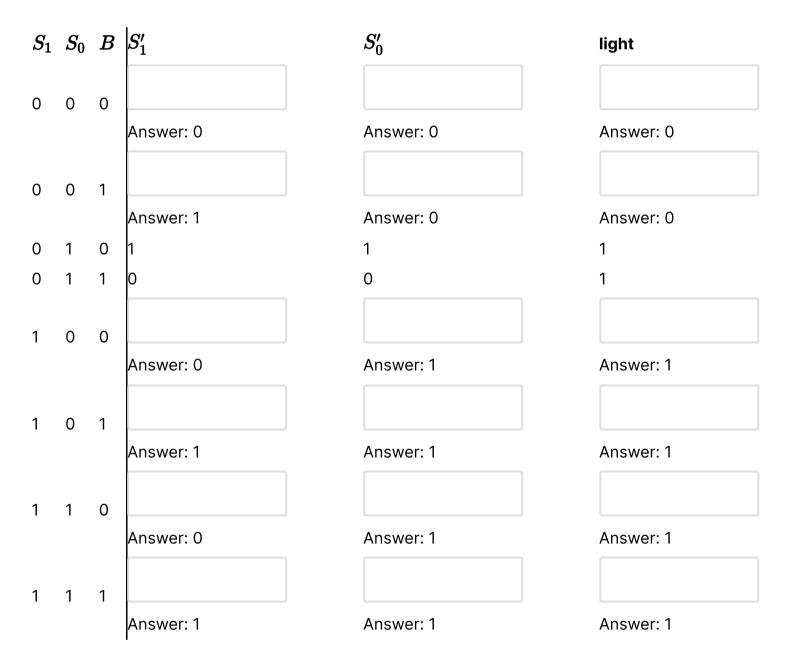
when the light is to be on. What is the value of the **light** output when all three inputs to the ROM are zero?

Value	Ωf	liaht	output
value	OΙ	Hym	output



4. Fill in the unspecified rows of the following truth table so that it implements the state transition diagram (repeated below). Remember the starting state is 00.





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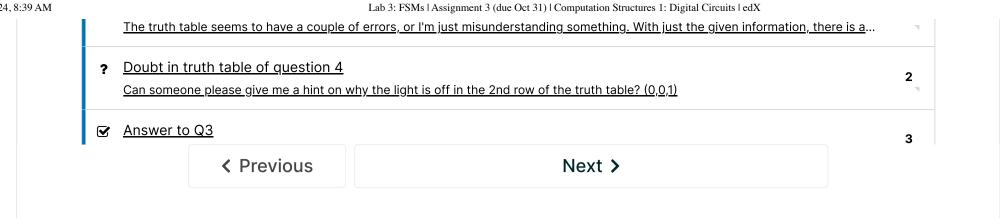
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▼ Truth table error for lab 3.2 FSM?

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