Previous Next

LE13.1

Bookmark this page

as shown at the end of the previous video. Please choose "do not care" if the value of control signal doesn't matter when executing the instruction.

(A) **Swap register contents with memory location**

```
Usage:     MSWP (Ra, literal, Rc)
Operation: PC ← PC + 4
           EA ← Reg[Ra] + SEXT(literal)
           tmp ← Mem[EA]
           Mem[EA] ← Reg[Rc]
           Reg[Rc] ← tmp
```

ALUFN	adder unit: A + B	✔ Answer: adder unit: A + B
BSEL	1	✔ Answer: 1
MOE	1	✔ Answer: 1
MWR	1	✔ Answer: 1
RA2SEL	1	✔ Answer: 1
WDSEL	2	✔ Answer: 2
WERF	1	✔ Answer: 1

Explanation
MSWP is a combination of LD and ST. Start with the control signals for LD and then add the ST signals: RA2SEL=1 (read Rc) and MWR=1 (write main memory).

(B) **Load indexed**

```
Usage:     LDX (Ra, Rb, Rc)
Operation: PC ← PC + 4
           Reg[Rc] ← Mem[Reg[Ra] + Reg[Rb]]
```

ALUFN	adder unit: A + B	✔ Answer: adder unit: A + B
BSEL	0	✔ Answer: 0
MOE	1	✔ Answer: 1
MWR	0	✔ Answer: 0
RA2SEL	0	✔ Answer: 0
WDSEL	2	✔ Answer: 2
WERF	1	✔ Answer: 1

Explanation
LDX is essential the LD instruction with the B operand of the ALU selected as the value of Rb register instead of the sign-extended constant. So BSEL=0. The remainining control signal value are the same as for LD.

Submit

Answers are displayed within the problem

Show all posts by recent activity

- Couldn't Build Beta — 2
  I couldn't complete my Lab#3 means I couldn't build my ALU or BETA inside. I am trying again, though I know it won't be accepted a...
- operation of MSWP(Ra,literal,Rc) — 3
  can someone explain how the ST control signals are added after the LD signals? is this instruction done in one clock cycle or two?
- ALUFN, BSEL, MOE, MWR, RA2SEL, WDSEL stands for what? — 2
  I know ALU is arithmetic logic unit. But what does FN mean? SEL for some kind of selection? I found WERF stands for write-enable r...
- [Staff] Lecture videos still problematic — 9
  I see the latest lecture videos continue the theme of not working properly when downloaded whereas worked example videos do. T...
- LE13.1.1 (B) - Why is 'LDX' NOT included in the beta ISA? — 6
  Regarding [this][1] thread in another discussion... Why is this $LDX\ (Ra, Rb, Rc)$ instruction __not__ included in the Beta ISA? If I'...

Previous Next

edX

edX

About
Affiliates
edX for Business
Open edX
Careers
News

Legal

Terms of Service & Honor Code
Privacy Policy
Accessibility Policy
Trademark Policy
Sitemap
Cookie Policy
Your Privacy Choices

Connect

Idea Hub
Contact Us
Help Center
Security
Media Kit