WE15.1

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Video explanation of solution is provided below the problem.

Pipelined Beta

8/8 points (ungraded)

A 5-stage pipelined Beta with full bypassing and annulment of branch delay slots has been running the program below for a while. A snapshot of the execution starting at cycle 1001 is shown in the pipeline diagram.

```
      ...
      CMOVE(0, R1)
LOOP: LD(R1, array, R0)
      ADDC(R1, 4, R1)
      CMPEQ(R0, R1, R2)
      BNE(R2, LOOP, R31)
      ST(R1, index, R31)
      ...
```

Cycle #	1001	1002	1003	1004	1005	1006	1007
IF	LD	ADDC	CMPEQ	BNE	BNE	ST	LD
RF	NOP	LD	ADDC	CMPEQ	CMPEQ	BNE	NOP
ALU	BNE	NOP	LD	ADDC	NOP	CMPEQ	BNE
MEM	CMPEQ	BNE	NOP	LD	ADDC	NOP	CMPEQ
WB	NOP	CMPEQ	BNE	NOP	LD	ADDC	NOP

1. The program reads from registers R0, R1 and R2. In a pipelined processor, sometimes the register contents come from the register file and sometimes from a bypass path. Select all registers whose contents came from the register file at least once during cycles 1001 through 1007.

   Select all registers whose contents are read from register file at least once:

   - [ ] R0
   - [x] R1
   - [ ] R2

   ✔

   Explanation

   Since the program has been running for a while, the LD instruction at label loop is reading the value that the previous iteration placed into R1 via the ADDC instruction. By the time the LD is in the RF stage, the ADDC from the previous iteration of the loop has already written its data back to the register file, so the LD reads R1 from the register file. For the same reason, the ADDC reads R1 from the register file. The CMPEQ instruction needs to read new values of R0 and R1 so they both come from bypass paths. The BNE also reads R2 from the bypass path. The ST is annulled. So the only register that is read directly from the register file is R1.

2. Referring to the cycle numbers at the top of the pipeline diagram, please indicate the cycle numbers for which the specified signal had the specified value. Select NONE if the signal did not have that value during any of cycles 1001 through 1007.

   Cycle(s) when STALL was 1:

   - [ ] 1001
   - [ ] 1002
   - [ ] 1003
   - [x] 1004

- [ ] 1005
- [ ] 1006
- [ ] 1007
- [ ] NONE

✔

Cycle(s) when $IRSrc^{IF}$ was not 0:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [ ] 1004
- [ ] 1005
- [x] 1006
- [ ] 1007
- [ ] NONE

✔

Cycle(s) when $IRSrc^{RF}$ was not 0:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [x] 1004
- [ ] 1005
- [ ] 1006
- [ ] 1007
- [ ] NONE

✔

Cycle(s) when $IRSrc^{ALU}$ was not 0:

- [ ] 1001
- [ ] 1002
- [ ] 1003

- [ ] 1004
- [ ] 1005
- [ ] 1006
- [ ] 1007
- [x] NONE

✔

Cycle(s) when either bypass was from ALU stage:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [ ] 1004
- [ ] 1005
- [x] 1006
- [ ] 1007
- [ ] NONE

✔

Cycle(s) when either bypass was from MEM stage:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [ ] 1004
- [x] 1005
- [ ] 1006
- [ ] 1007
- [ ] NONE

✔

Cycle(s) when either bypass was from WB stage:

- [ ] 1001
- [ ] 1002

- [ ] 1003
- [ ] 1004
- [x] 1005
- [ ] 1006
- [ ] 1007
- [ ] NONE

✔

Explanation
Cycles 1001 - 1003 proceed without any stalls, annullments, or the use of bypass paths.
In cycle 1004, the pipeline is stalled because the CMPEQ instruction needs to read the value of R0 that was loaded by the LD operation but the LD operation has not yet reached the WB stage.
In cycle 1005, the LD reaches the WB stage, so now CMPEQ can read both of its registers via bypass paths. R0 from the LD comes from the WB stage, and R1 from the ADDC comes from the MEM stage.
In cycle 1006, the BNE reads R2 from the CMPEQ via the bypass in the ALU stage. In addition, the ST that is fetched in this cycle, must be annulled. This is done by replacing the ST in the IF stage with a NOP operation.

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Answers are displayed within the problem

Pipelined Beta

Start of transcript. Skip to the end.

For this problem, assume that you have a fully functioning 5-stage pipelined beta with full bypassing and annulment of branch delay slots as presented in lecture.

This beta has been running the program shown here for a while.

The actual functionality of this program is not so important for this problem, but lets just review it quickly.

This program begins by initializing R1

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