For all Beta related questions, you should make use of the Beta documentation, the Beta Instruction Summary, the Unpipelined Beta Diagram and the Pipelined Beta Diagram.

Pipelined Beta: 1

0.9901960784313726/1 point (ungraded)

Assume a 5-stage Beta with full bypass paths, as presented in lecture. Remember that, in the pipelined Beta, the data read by loads becomes available in the writeback stage. Fill in the pipelining diagram below using the command names (e.g., LD, ST) that live in each stage. If no operation happens in a particular slot, enter the word EMPTY. In steady state, how many cycles does this code consume in the pipelined Beta?

```
LD(R0,0,R2)
LD(R1,0,R3)
ST(R2,0,R1)
ST(R3,0,R0)
```

	0	1	2	3	4	5	6	7	8	9	10	11
IF	LD	LD	ST	ST	ST	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
RF		LD	LD	ST	ST	ST	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
EXE			LD	LD	NOP	ST	ST	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
MEM				LD	LD	NOP	ST	ST	EMPTY	EMPTY	EMPTY	EMPTY
WB					LD	LD	NOP	ST	ST	EMPTY	EMPTY	EMPTY

If this code was executed repeatedly, how many cycles would it take in steady state?

Number of Cycles in Steady State:

5

Suppose a new instruction SWAP, SWAP(Ra, literal, Rc), was added to the Beta. SWAP swaps a register value and a memory location.. The behavior of this instruction is as follows:

```
tmp <-- Mem[Reg[Ra] + SEXT(literal)]
Mem[Reg[Ra] + SEXT(literal)] <-- Reg[Rc]
Reg[Rc] <-- tmp
```

Using this new instruction, the code sequence above can be rewritten as:

```
LD(R0,0,R2)
SWAP(R1,0,R2)
ST(R2,0,R0)
```

Assume that the SWAP instruction is implementable in the fully bypassed 5-stage Beta, and also returns data in the writeback stage. Fill in the pipelined timing diagram as above. Remember that SWAP(Ra,literal,Rc) reads and writes Rc (in the register file and writeback stages, respectively).

	0	1	2	3	4	5	6	7	8	9	10	11
IF	LD	SWAP	ST	ST	ST	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
RF		LD	SWAP	SWAP	SWAP	ST	ST	ST		EMPTY	EMPTY	EMPTY
EXE			LD	NOP	NOP	SWAP	NOP	NOP	ST	EMPTY	EMPTY	EMPTY
MEM				LD	NOP	NOP	SWAP	NOP	NOP	ST	EMPTY	EMPTY
WB					LD	NOP	NOP	SWAP	NOP	NOP	ST	EMPTY

If this code was executed repeatedly, how many cycles would it take in steady state?

Number of Cycles in Steady State:

7

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✱ Partially correct (0.99/1 point)

Discussion

Topic: 15. Pipelining the Beta / Pipelined Beta: 1

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Pipelined Beta 1 - LD,LD,ST,ST loop 5
The number of cycles at steady state is given in the answer as 5 due to the required stall. But if you executed the code repeatedly, as a loop, wouldn't you need two more st...

[STAFF] not sure about how to read question... 2
Hi Silvina, I'm not sure how to read "executed repeatedly" and "in steady state". In the first part, there's 2 LD and 2 ST instructions. If these 4 instructions are "executed rep...