LE3.6

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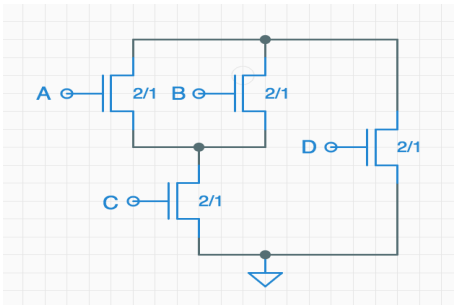
LE3.6.1: Leniency

1/1 point (ungraded)

The following diagram shows a schematic for the pulldown circuitry for a particular CMOS logic gate.



Assuming the pullup circuitry is designed correctly, is the CMOS gate above lenient?

- (●) Yes
- ( ) No
- ( ) Not enough information to tell

✔

Explanation

All CMOS gates are lenient because they produce a glitch-free output using a minimal number of required inputs.

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Answers are displayed within the problem

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  I have come across a few diagrams like this one which has only inputs and GROUND displayed without the output point. And I find t...
- lenient — 5
  I know the definition of the lenient, but I still not understand why "a glitch-free output using a minimal number of required inputs" is ...

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