

<u>Help</u>





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■ Calculator

Lab due Oct 24, 2016 21:59 -02 Past due

CMOS Basics

0.0/2.0 points (graded)

The following questions are multiple-choice. Using the "check" button, you can of course simply keep guessing until you get the right answer. But you'll be in a much better position to take the quizzes if you take the time to actually figure out the answers.

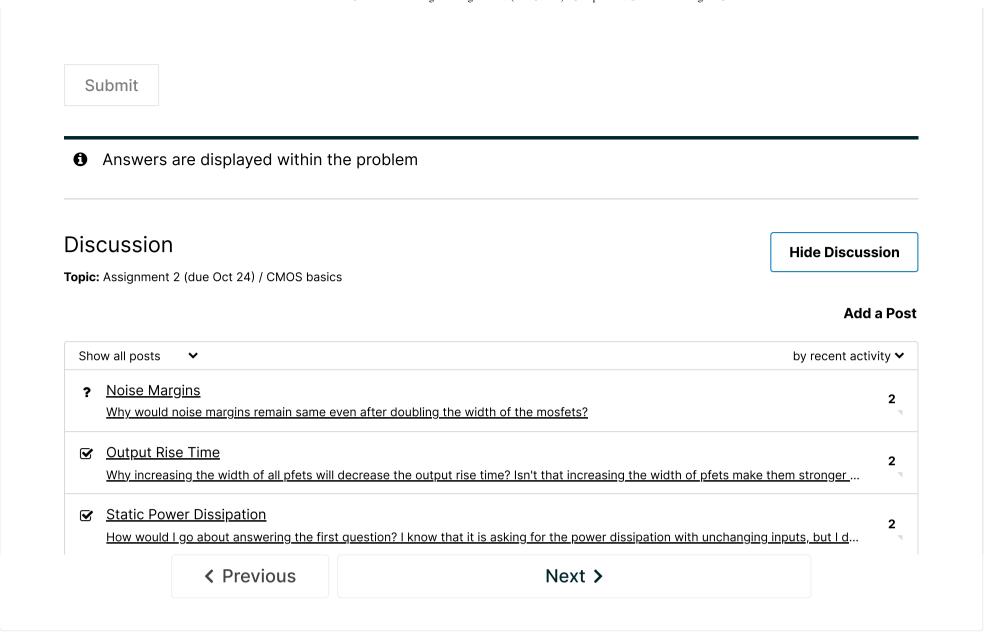
1. If we set the inputs of a particular CMOS gate to voltages that correspond to valid logic levels, we would expect the *static* power dissipation of the gate to be

		essentially zero
		depends on whether output voltage is low or high
		unknown with the facts given
		uring a particular CMOS device G, we find 1.5V noise margins. If the <i>width</i> of all mosfets inside of G doubled, we would expect the noise margins of the new gate to
		stay about the same
		increase noticeably
		decrease noticeably
		change noticeably, but can't tell which way
3.	To <i>de</i>	crease the output rise time of a CMOS gate one could
		increase the length of all pfets
		increase the width of all pfets ✓ ✓
		increase the length of all nfets
		increase the width of all nfets
		none of the above

4. The Boolean function F(A,B,C,D) of four inputs is implemented as a single CMOS gate whose output connects to a pullup circuit containing only PFETs and a pulldown containing only NFETs. The output of F is known to depend on its inputs; i.e., F(A,B,C,D) is 0 for certain input combinations and 1 for others. What can you deduce about F(1,1,1,1)?

F(1,1,1,1) will be 0	
$\bigcirc \ F(1,1,1,1)$ will be 1	

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