LE7.1

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LE7.1.1: Latency and Throughput

2 points possible (ungraded)

A synchronous pipeline has a latency of L and throughput of T. If we find a way to double the clock frequency by doubling the number of pipeline stages, what revised latency and throughput can we expect? Please provide your response as a function of L and T. (Note that multiplication must be explicitly stated, e.g., L*8, not 8L).

Latency:

L

Answer: L

L

Throughput:

2*T

Answer: 2*T

$2 \cdot T$

Explanation
The latency of a pipelined circuit is equal to the number of pipeline stages times the clock period. If you double the clock frequency, then your period is reduced by a factor of two. However, the number of pipeline stages needed to be doubled in order to be able to reduce the clock period, so the latency remains unchanged.
The throughput of a pipelined circuit is equal to 1/(clock period). Since the clock period goes down to half of its original value, that means that the throughput will double.

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Answers are displayed within the problem

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? Why do I get "Invalid input: T not permitted in answer"? 14

The system doesn't accept the correct 2*T as an answer for the new throughput.

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