LE5.3

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Calculator

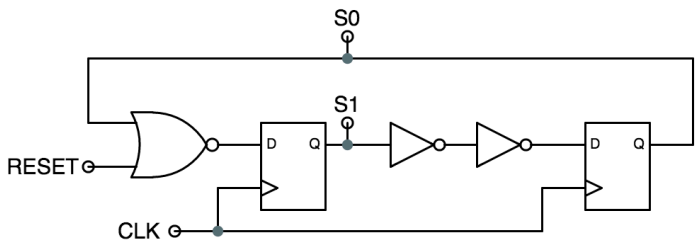
1.7 + 1.7 + 1.6 [ ] 5.0

Calculator Instructions

LE5.3.1 Sequential Logic Timing

2/3 points (ungraded)

You are given the sequential circuit and component specs shown below.



Inverter	
t_{pd}	1.7ns
t_{cd}	0.2ns

NOR-2	
t_{pd}	1.9ns
t_{cd}	0.3ns

Register	
t_{pd}	3.5ns
t_{cd}	0.5ns
t_s	1.6ns
t_h	0.4ns

Minimum clock period (ns): 8.5 ✔ Answer: 8.5

Explanation

For every path from one register to another, the following constraint must be met:

$$t_{clk} \geq t_{pd} + t_{pdL} + t_s$$

Where t_{pd} is the propagation delay of the registers, t_s is the setup time of the registers, t_{pdL} is the propagation delay of the logic between the registers, and t_{clk} is the clock period.

First look at the path from the left-most register to the right-most. The t_{pdL} for this section is twice the propagation delay of an inverter, so $t_{pdL} = 2 * 1.7 = 3.4$. The propagation delay of the registers is 3.5ns and the setup time is 1.6ns. So the minimum clock period is $3.5 + 3.4 + 1.6 = 8.5$.

Now look at the path from the right-most register back to the left-most. The t_{pdL} between these two registers is just the propagation delay of a NOR-2 gate, which is 1.9ns. So the minimum clock period for this section is $3.5 + 1.9 + 1.6 = 7.0$.

Since there can be only one clock period, the minimum clock period for the whole circuit is the greater of the two minimum clock periods for each section. So the answer is 8.5ns.

Setup time for RESET relative to CLK rising edge (ns): 3.5 ✔ Answer: 3.5

Hold time for RESET relative to CLK rising edge (ns): 0.1 ✖

Answer: 0.10000000000000003

Explanation

Consider all paths from a system input (e.g., RESET) to register inputs (e.g., D input of left register). For each path compute the sum of the propagation delays of combinational logic along that path plus the setup time of the register. The setup time of the system input is maximum sum over all the paths.

$t_{PD,NOR2} + t_{SETUP,REG} = 3.5\text{ns}$

Considering the same paths, compute the hold time of register minus the sum of the contamination delays along the path. The hold time of the system input is a maximum over all the paths.

$t_{HOLD,REG} - t_{CD,NOR2} = 0.10000000000000003\text{ns}$

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tH,INPUT

question posted 7 years ago by **IanWRandman**

I still don't understand why tH,INPUT = tH,R - tCD,L.

This post is visible to everyone.

silvinahw (Staff)
7 years ago - marked as answer 7 years ago by **silvinahw** (Staff)

The hold time for the register specifies how long after the rising edge of the clock, the input to the register must remain stable and valid. In order to ensure that the setup and hold times of the register are met, we must think about what constraints are placed on the stability of our input signals. We know, however, that after our input changes, the change will not be reflected at the input to the register until after tCD of the combinational logic between the input and the register has elapsed. This means that if the input to the register must be stable until time T + tHold,R, the input (Reset) could change until time T + tHold,R - tCD,L and still satisfy the requirement that hte input to the regiser won't change until time T + tHold,R.

We call the tPD of register tco (t_clock_to_output) usually.

posted 7 years ago by **sieg70**

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