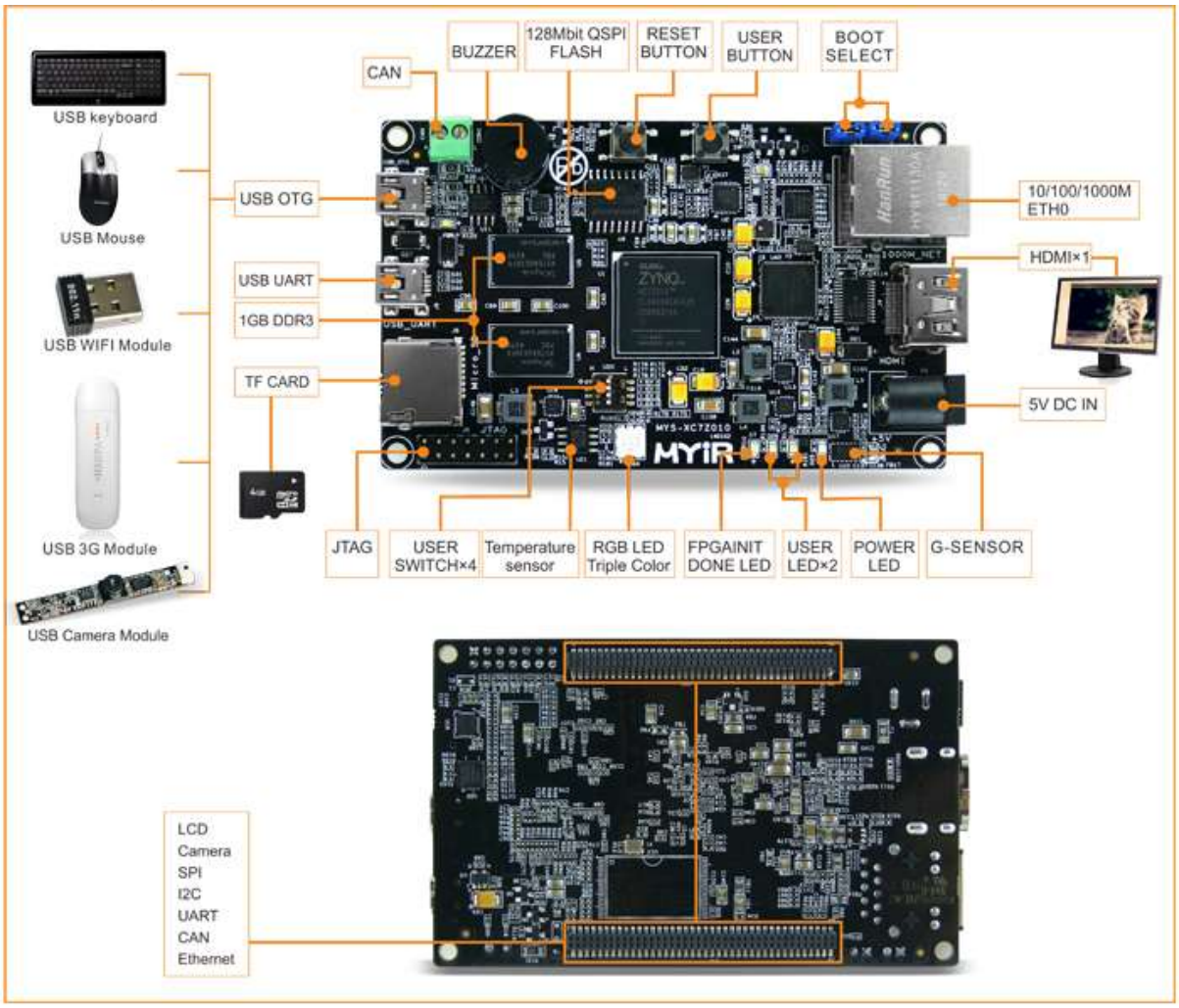
# 零点工作室

**标题:** 【原创】Z-turn Board 的SD卡启动问题 [打印本页]

**作者:** dastan **时间:** 2016-8-12 09:51
**标题:** 【原创】Z-turn Board 的SD卡启动问题
前段时间入手了一块ZYNQ开发板，ARM+FPGA，异构计算，XC7Z020的芯片85K可编程逻辑，比我上一块板子大了10倍有余，我想要的全都有。




硬件参数 Hardware Parameters

想了解板子可以看这里：
http://www.myir-tech.com/product/z-turn_board.htm

板子提供的资料有点少，而且太浅显了，我觉得搞ZYNQ就是要刨根问底，绝不是搭起开发环境，跑个流水灯就算是精通了。

Vivado已经更新到2016.2 了，我也换了最新版本。为什么不和教程上一样用2014.3版本呢？
因为Vivado 本身还不完善，存在很多BUG，新版本做了很好的修复，所以对于Vivado，还是尽量用新版本。

那么问题就来了


图 1-19

文档里说FSBL的SD驱动2.3版本有问题，降回2.2版本就能正常使用。这么草率的解决方法，太不喜欢了。如果说驱动真有问题，Debug一下不行吗？
而且在vivado 2016.2 ，SD驱动版本已经到2.8了，不可能再倒回2.2版本。而且2.8版本的驱动依然无法用SD卡启动板子，我想如果驱动有Bug，也早该修复了才对。

我打开了FSBL的串口调试功能，通过串口可以看到一些信息：

[Bash shell] 纯文本查看 复制代码

```
Xilinx First Stage Boot Loader

Release 2014.4 Apr 8 2015-14:07:23

Devcfg driver initialized

Silicon Version 3.1

Boot mode is SD

SD: rc= 0

XSdPs_Change_ClkFreq: Config.InputClockHz: 125000000 SelFreq=400000

XSdPs_CfgInitialize: XSdPs_Change_ClkFreq: Status=1

SD: Unable to open file BOOT.BIN: 3

                                    SD_INIT_FAIL

FSBL Status = 0xA009
```

剩下的问题就简单了，到google上百度一下，相似的问题就找到了：
**Re: Boot from SD Card Vivado 2014.4**
« **Reply #6 on:** June 05, 2015, 01:39:34 PM »
Hi

please make sure that MIO pullups in PS7 config for SDIO pins are all DISABLED. we are updating board part files and reference projects. This issue does not make problems with many SD cards, but some cards may either not boot at all, or have random issues.

https://wiki.trenz-electronic.de/display/PD/SD+Card+Interface

we will add info there when the board part files and ref designed are update to disable those pullups on MIO lines.

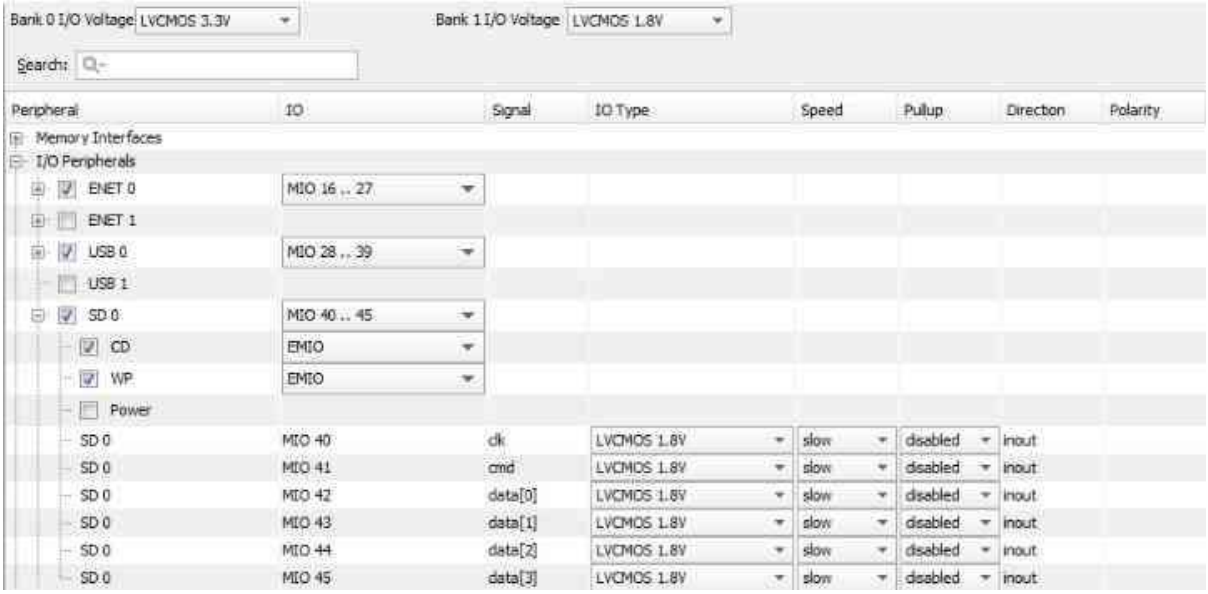
Please not that those software pullups on MIO40..45 have much more impact on the SD card boot than the R43 resistor on CMD line.
« *Last Edit: June 05, 2015, 01:51:04 PM by Antti Lukats* »

# SD Card Interface

Skip to end of metadata
Created by Antti Lukats, last modified on 31 08, 2015
Go to start of metadata

## Zynq PS SDIO

SDIO MIO Settings in PS7 IP Configuration if external level shifter is used:
· speed (slew rate): slow
· pullup: disabled
It is important to disable the pull-ups, otherwise some SD card may exhibit systematic or random problem at initialization.
itialization.




### SDIO Peripheral Clock

This clock may as of Xilinx default sometimes be set to 125MHz, this would cause Xilinx FSBL to fail on clock lookup when setting SD clock to 400KHz. SDIO peripheral clock should be set to 100MHz or 50MHz.

### Level shifter

Modules that expose SDIO Interface on the B2B Connector from 1.8V VCCIO bank need SD Level shifter IC on the baseboard.

When using TXS02612 as SDIO level shifter external pullups should not be used on CMD and DAT lines.
TE0701 and TE0703 have pullup resistor on CMD line, which has been removed since:

| Base | CMD pullup Resistor R43 | Removed since |
|---|---|---|
| TE0701 | | TE0701-05 Serial number: TBD |
| TE0703 | | TE0703-04 Serial number: TBD |

This extra pullup may cause problems in some special cases with some SD Cards. As example hama micro-SD Card when used with PS7 SDIO MIO pullups enabled and R43 loaded had sporadic initialization problems on TE0703, removing R43 solved the issue.
Some other designs and boards that use TXS02612 may have pullup on CMD, this is incorrect as per TXS02612 datasheet. Xilinx ZC702 board that uses SDIO level shifter with similar technology has the CMD pullup in schematic with marking "DNP" do not populate.
When using SDIO level shifter from other vendors, or other level shifting technology then requirements listed in the vendor datasheet and application notes should be followed.

## References

· TXS02612 Documentation from TI
· ZC702 Documentation from Xilinx

https://forums.xilinx.com/t5/Embedded-Development-Tools/Zynq-FSBL-won-t-read-boot-bin-from-SD-card-with-CD-disabled/m-p/587926

## Re: Zynq FSBL won't read boot.bin from SD card with CD disabled

Options
04-08-2015 03:09 PM
… I found the bug in the 2014.4 FSBL code.

The default SD clock frequency is 125000000

Changing the clock freqency to 25000000 in XSdPs_CfgInitialize will correct the problem. This is a hack to get the
FSBL to work and if the BSP is regenerated it will overwrite the BSP files.

---
Xilinx First Stage Boot Loader
Release 2014.4 Apr 8 2015-14:07:23
Devcfg driver initialized
Silicon Version 3.1
Boot mode is SD
SD: rc= 0
XSdPs_Change_ClkFreq: Config.InputClockHz: 125000000 SelFreq=400000
XSdPs_CfgInitialize: XSdPs_Change_ClkFreq: Status=1
SD: Unable to open file BOOT.BIN: 3
SD_INIT_FAIL
FSBL Status = 0xA009

This Boot Mode Doesn't Support Fallback

In FsblHookFallback function
---

XSdPs_CfgInitialize will fail:

Changing xsdps.c Line 165 to:
Status = XSdPs_Change_ClkFreq(InstancePtr, 25000000);

And the FSBL now works.

```
int XSdPs_CfgInitialize(XSdPs *InstancePtr, XSdPs_Config *ConfigPtr,
                        u32 EffectiveAddr)
{
    …
    /*
     * Change the clock frequency to 400 KHz
     */

    //Status = XSdPs_Change_ClkFreq(InstancePtr, XSDPS_CLK_400_KHZ);
    // 400000 is too small. The clock change API will fail
    //
    Status = XSdPs_Change_ClkFreq(InstancePtr, 25000000);
    xil_printf("XSdPs_CfgInitialize: XSdPs_Change_ClkFreq: Status=%d \r\n",
Status);
   if (Status != XST_SUCCESS) {
        Status = XST_FAILURE;
        goto RETURN_PATH ;
    }
  …
}
```

---
--- Called by XSdPs_CfgInitialize ---
--- Fails with ClkLoopCnt = 9 ----
---

```
int XSdPs_Change_ClkFreq(XSdPs *InstancePtr, u32 SelFreq)
{
    /*
     * Calculate divisor
     */
    DivCnt = 0x1;
    for(ClkLoopCnt = 0; ClkLoopCnt < XSDPS_CC_MAX_NUM_OF_DIV;
        ClkLoopCnt++) {
        if( ((InstancePtr->Config.InputClockHz)/DivCnt) <= SelFreq) {
            Divisor = DivCnt/2;
            Divisor = Divisor << XSDPS_CC_DIV_SHIFT;
            break;
        }
        DivCnt = DivCnt << 1;
    }

    if(ClkLoopCnt == 9) {

        /*
         * No valid divisor found for given frequency
         */
        xil_printf("XSdPs_Change_ClkFreq: Config.InputClockHz: %d SelFreq=%d
\r\n", InstancePtr->Config.InputClockHz, SelFreq);
```

```
            Status = XST_FAILURE;
            goto RETURN_PATH;
        }

    }
```

---

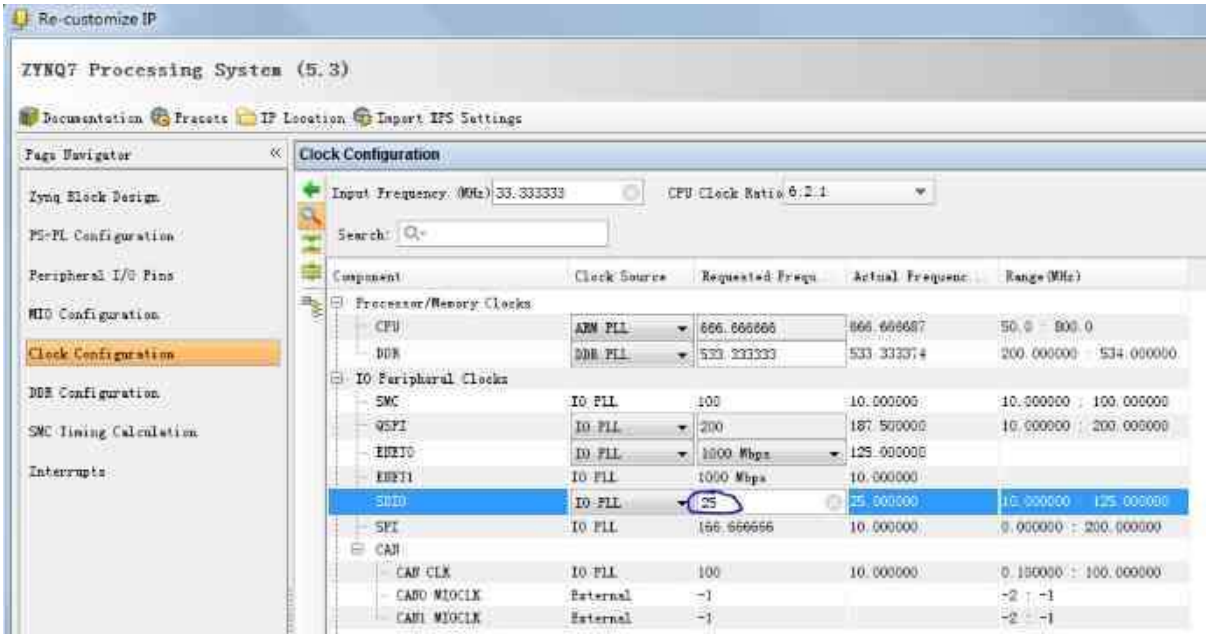
```
Xilinx First Stage Boot Loader
Release 2014.4 Apr 8 2015-14:12:54
Devcfg driver initialized
Silicon Version 3.1
Boot mode is SD
SD: rc= 0
XSdPs_CfgInitialize: XSdPs_Change_ClkFreq: Status=0
SD Init Done
Flash Base Address: 0xE0100000
Reboot status register: 0x60400000
Multiboot Register: 0x0000C000
Image Start Address: 0x00000000
Partition Header Offset:0x00000C80
Partition Count: 4
Partition Number: 1
Header Dump
Image Word Len: 0x0016CFC8
Data Word Len: 0x0016CFC8
Partition Word Len:0x0016CFC8
Load Addr: 0x00000000
Exec Addr: 0x00000000
Partition Start: 0x000065D0
Partition Attr: 0x00000020
Partition Checksum Offset: 0x00000000
Section Count: 0x00000001
Checksum: 0xFFBB2866
Bitstream
In FsblHookBeforeBitstreamDload function
PCAP:StatusReg = 0x40000A30
PCAP:device ready
PCAP:Clear done
Level Shifter Value = 0xA
Devcfg Status register = 0x40000A30
PCAP:Fabric is Initialized done
PCAP register dump:
PCAP CTRL 0xF8007000: 0x4C00E07F
PCAP LOCK 0xF8007004: 0x0000001A
PCAP CONFIG 0xF8007008: 0x00000508
PCAP ISR 0xF800700C: 0x0802000B
PCAP IMR 0xF8007010: 0xFFFFFFFF
PCAP STATUS 0xF8007014: 0x00001A30
PCAP DMA SRC ADDR 0xF8007018: 0x00100001
PCAP DMA DEST ADDR 0xF800701C: 0xFFFFFFFF
PCAP DMA SRC LEN 0xF8007020: 0x0016CFC8
PCAP DMA DEST LEN 0xF8007024: 0x0016CFC8
PCAP ROM SHADOW CTRL 0xF8007028: 0xFFFFFFFF
PCAP MBOOT 0xF800702C: 0x0000C000
PCAP SW ID 0xF8007030: 0x00000000
PCAP UNLOCK 0xF8007034: 0x757BDF0D
PCAP MCTRL 0xF8007080: 0x30800100
```

DMA Done !
FPGA Done !
In FsblHookAfterBitstreamDload function
Partition Number: 2
Header Dump
Image Word Len: 0x00014871
Data Word Len: 0x00014871
Partition Word Len:0x00014871
Load Addr: 0x04000000
Exec Addr: 0x04000000
Partition Start: 0x001735A0
Partition Attr: 0x00000010
Partition Checksum Offset: 0x00000000
Section Count: 0x00000001
Checksum: 0xF7E4EE9B
Application
Partition Number: 3
Header Dump
Image Word Len: 0x0000072F
Data Word Len: 0x0000072F
Partition Word Len:0x0000072F
Load Addr: 0x00000000
Exec Addr: 0x00000000
Partition Start: 0x00A80000
Partition Attr: 0x00000010
Partition Checksum Offset: 0x00000000
Section Count: 0x00000001
Checksum: 0xFF57E7F1
Application
Handoff Address: 0x04000000
In FsblHookBeforeHandoff function
SUCCESSFUL_HANDOFF
FSBL Status = 0x1
---

https://forums.xilinx.com/t5/Welcome-Join/Unable-to-boot-FSBL-from-Micro-SD-on-a-custom-designed-board/td-p/597842

## Re: Unable to boot FSBL from Micro SD on a custom designed board!!!

Options
05-05-2015 06:38 PM
Thank you for your replying!
My problem has been solved.
I revised SDIO Clock Configuration:50MHz == > 25MHz.




# 总结一下

国外几个Xilinx论坛上都有这个问题，上面有一个提到修改驱动软件代码，我试了没什么作用，而且我觉得软件方面不会有问题，后来几个帖子提到了SD相关IO和时钟的硬件配置，他们SDIO时钟用的25M，而我看了一下我的板子：125M，频率好高啊，按照上面两张图配置SD IO和时钟，问题解决了。

问题看似解决了，但我还不知道为什么解决了，我拿了另外一块ZYNQ板子，它的配置是50MHz，或许和SD卡的品质有关系吧，我暂时这么猜测。

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**作者:** 13电信-王小平　**时间:** 2016-8-12 14:12

好高大上啊。。

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**作者:** dastan　**时间:** 2016-8-12 15:33

> 13电信-王小平 发表于 2016-8-12 14:12
> 好高大上啊。。

还好吧，没那么高端。ZYNQ的硬件灵活性很好，可以自己用逻辑做硬件，作为ARM的片上外设。

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