

VLSI Design and Testing Laboratory Manual (CSC52201)



DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Name :

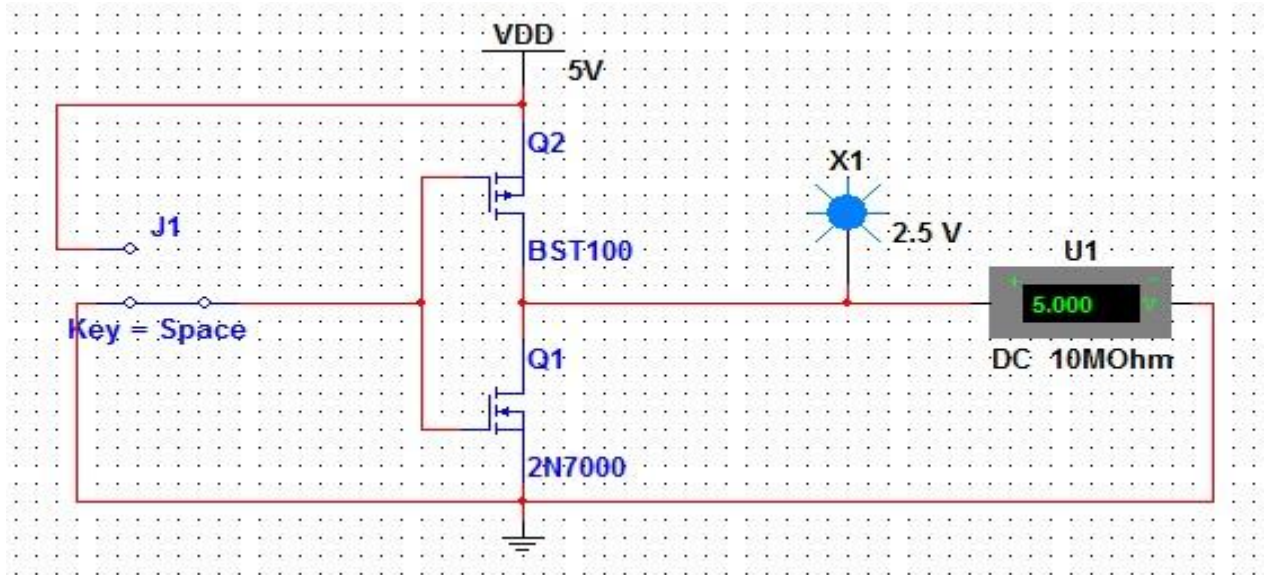
Adm. No. :

Session 2014-15

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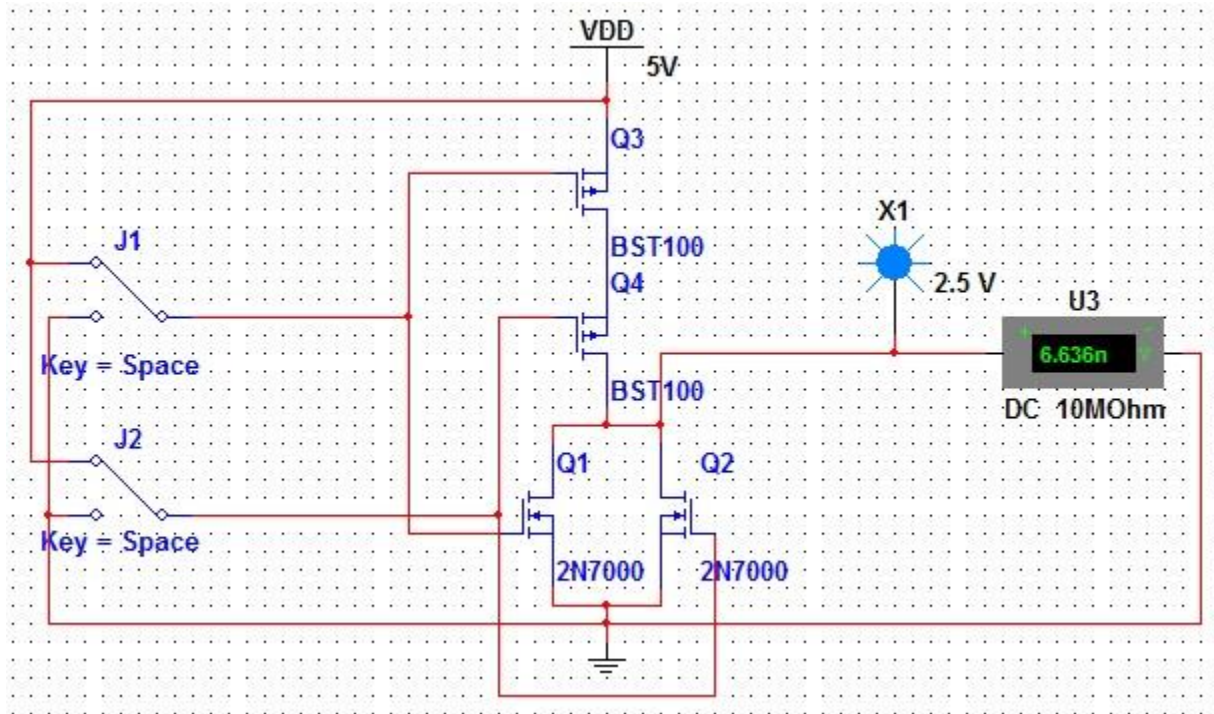
Sl. No.	Circuit Name	Date of Implementation	Signature	Remarks
1.	CMOS NOT Gate			
2.	CMOS NOR Gate			
3.	CMOS NAND Gate			
4.	CMOS OR Gate			
5.	CMOS AND Gate			
6.	CMOS XOR Gate			
7.	CMOS XNOR Gate			
8.	CMOS HALF ADDER			
9.	CMOS HALF SUBTRACTER			
10.	CMOS FULL ADDER			
11.	CMOS FULL SUBTRACTER			
12.	Pseudo NMOS AND GATE			
13.	Dynamic CMOS NOR GATE			

1. CMOS NOT Gate



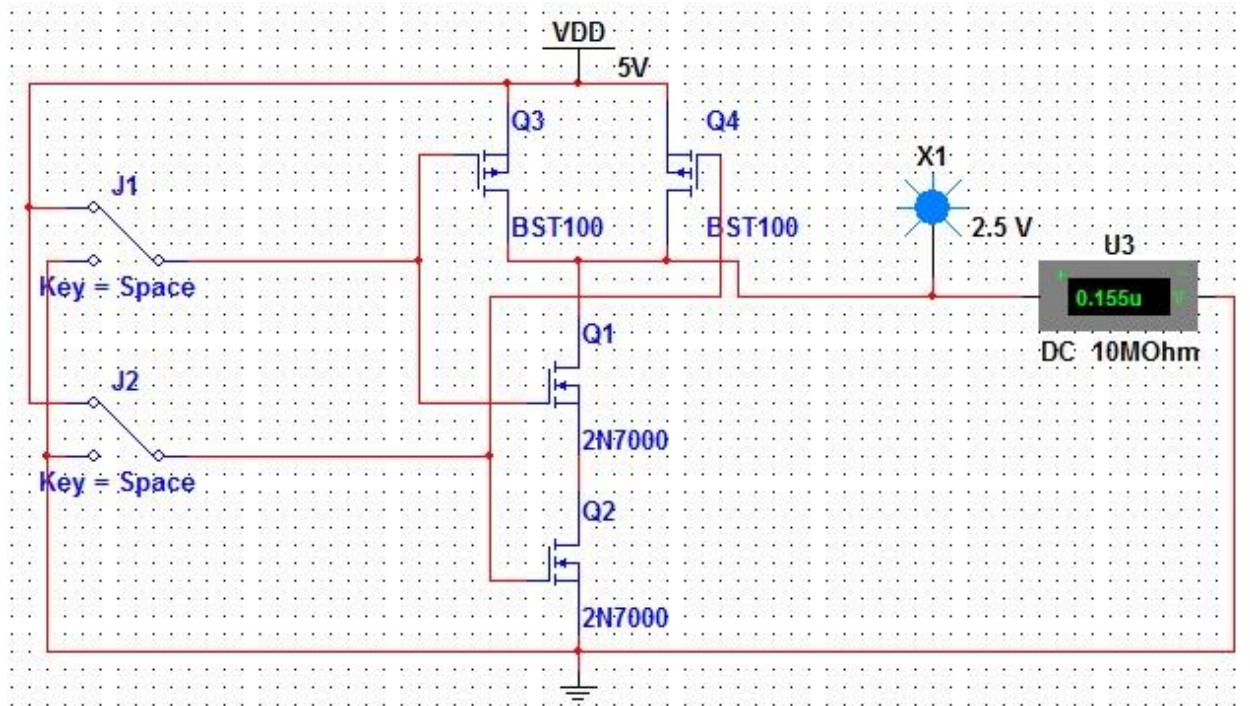
Circuit Diagram

2. CMOS NOR Gate



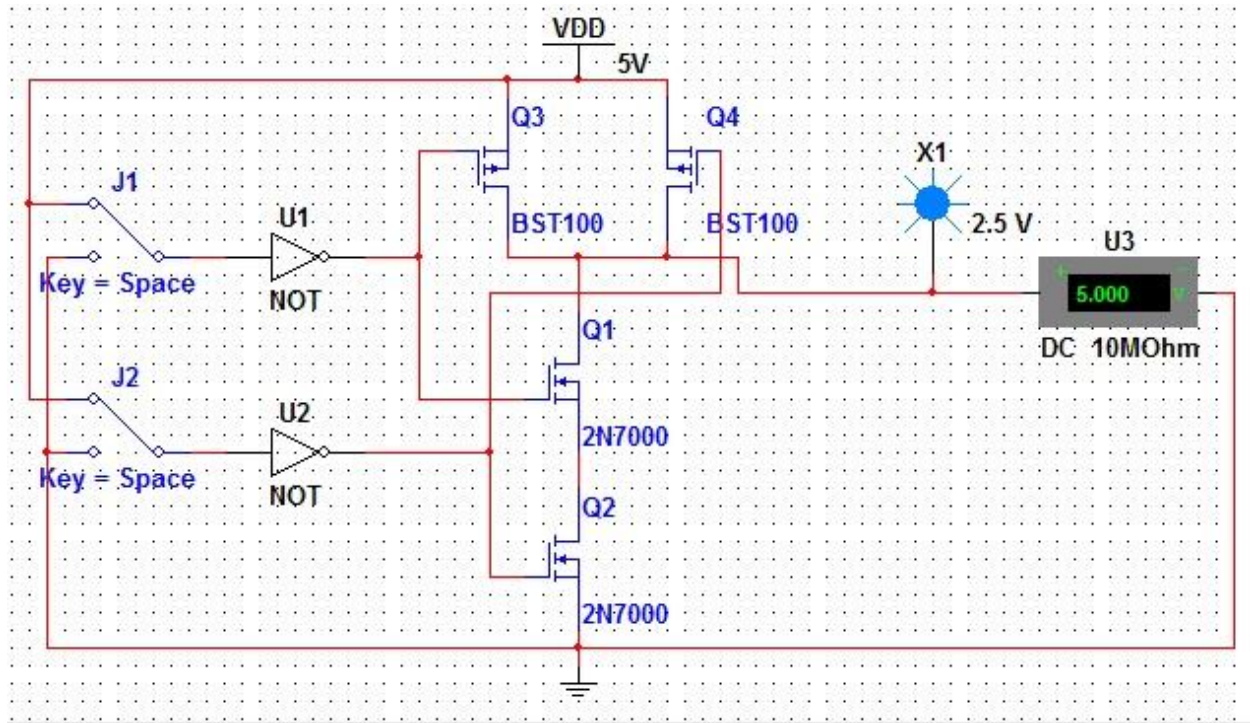
Circuit Diagram

3. CMOS NAND Gate



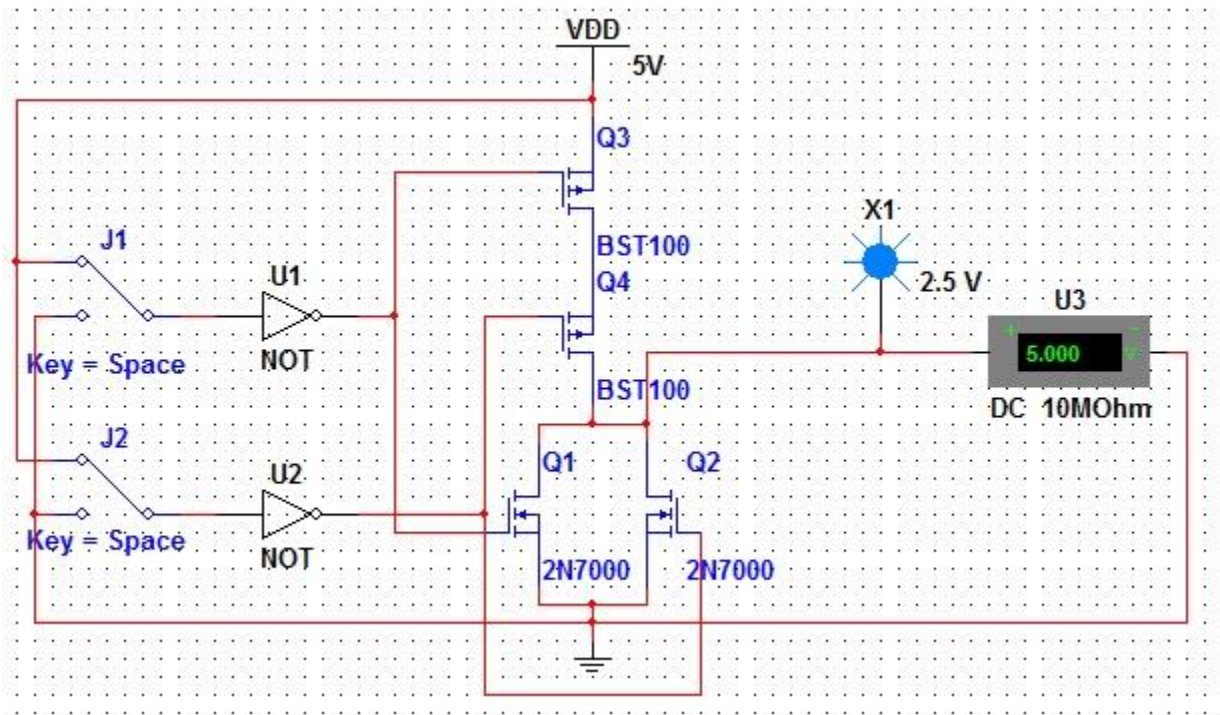
Circuit Diagram

4. CMOS OR Gate



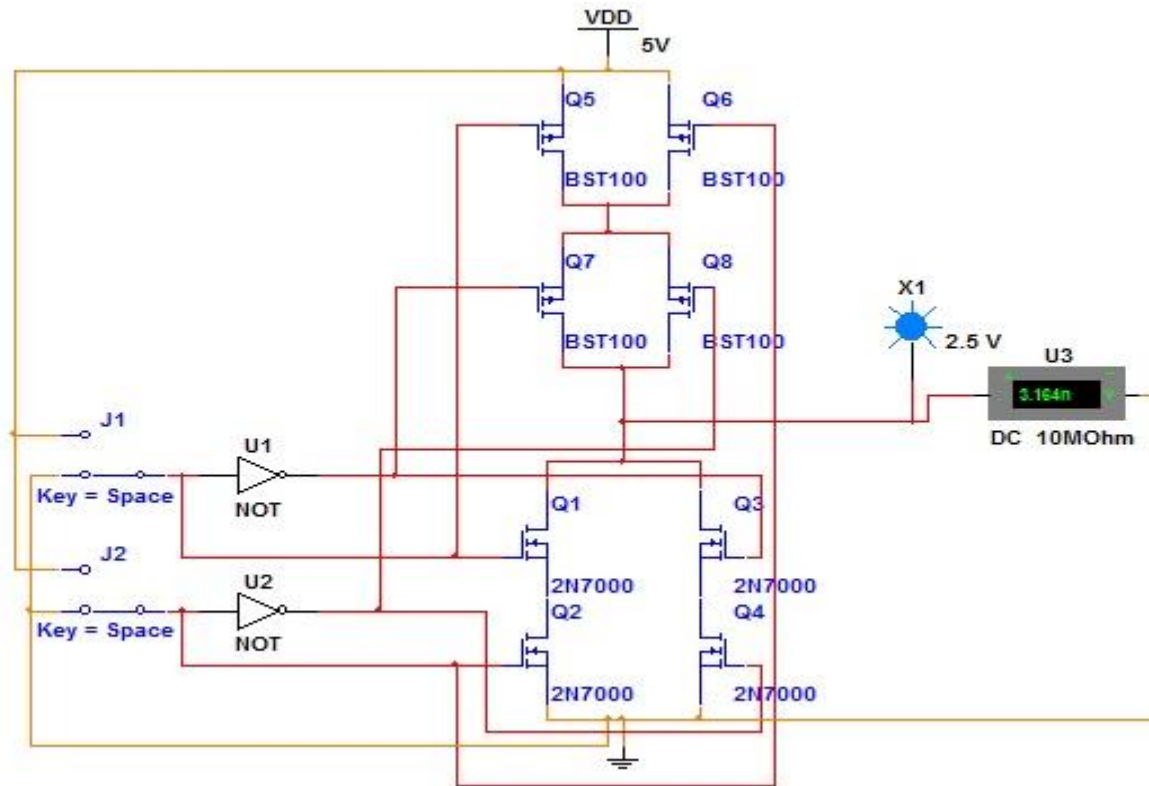
Circuit Diagram

5. CMOS AND Gate



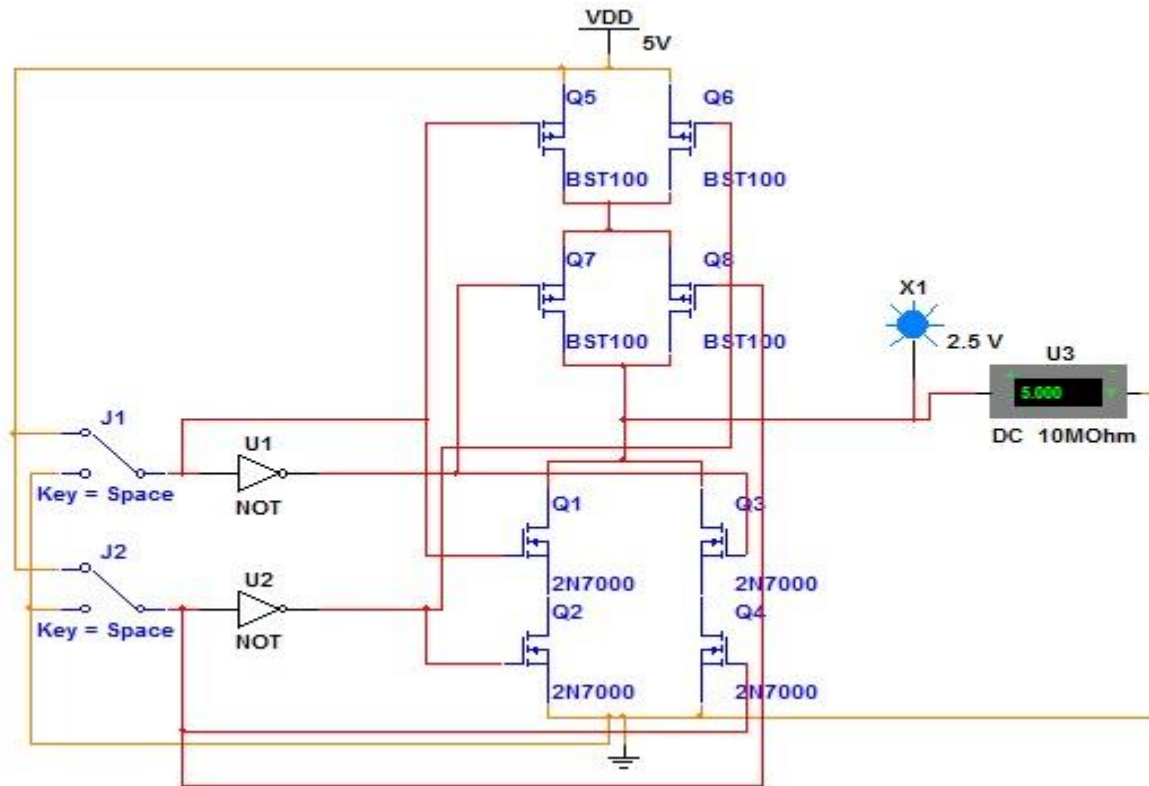
Circuit Diagram

6. CMOS XOR Gate



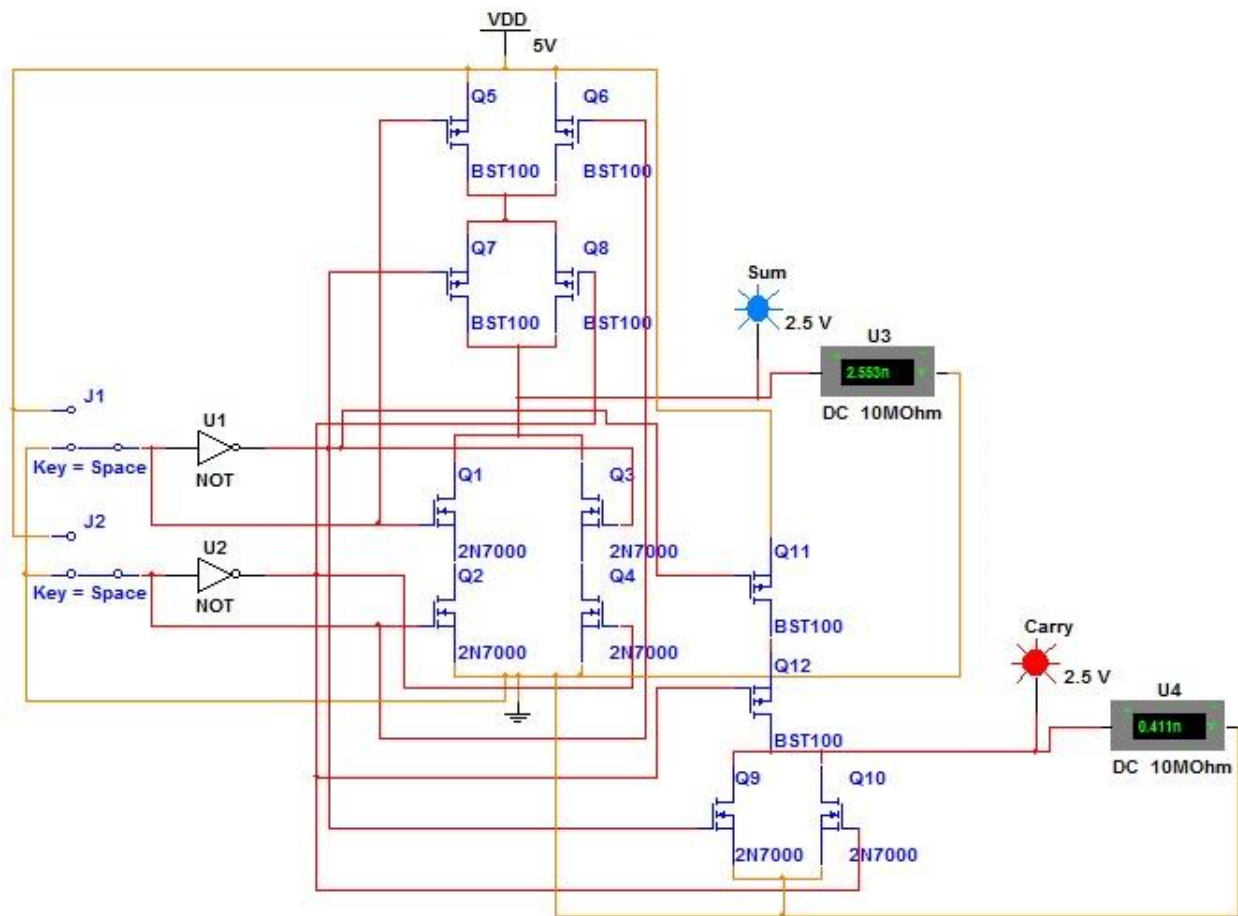
Circuit Diagram

7. CMOS XNOR Gate



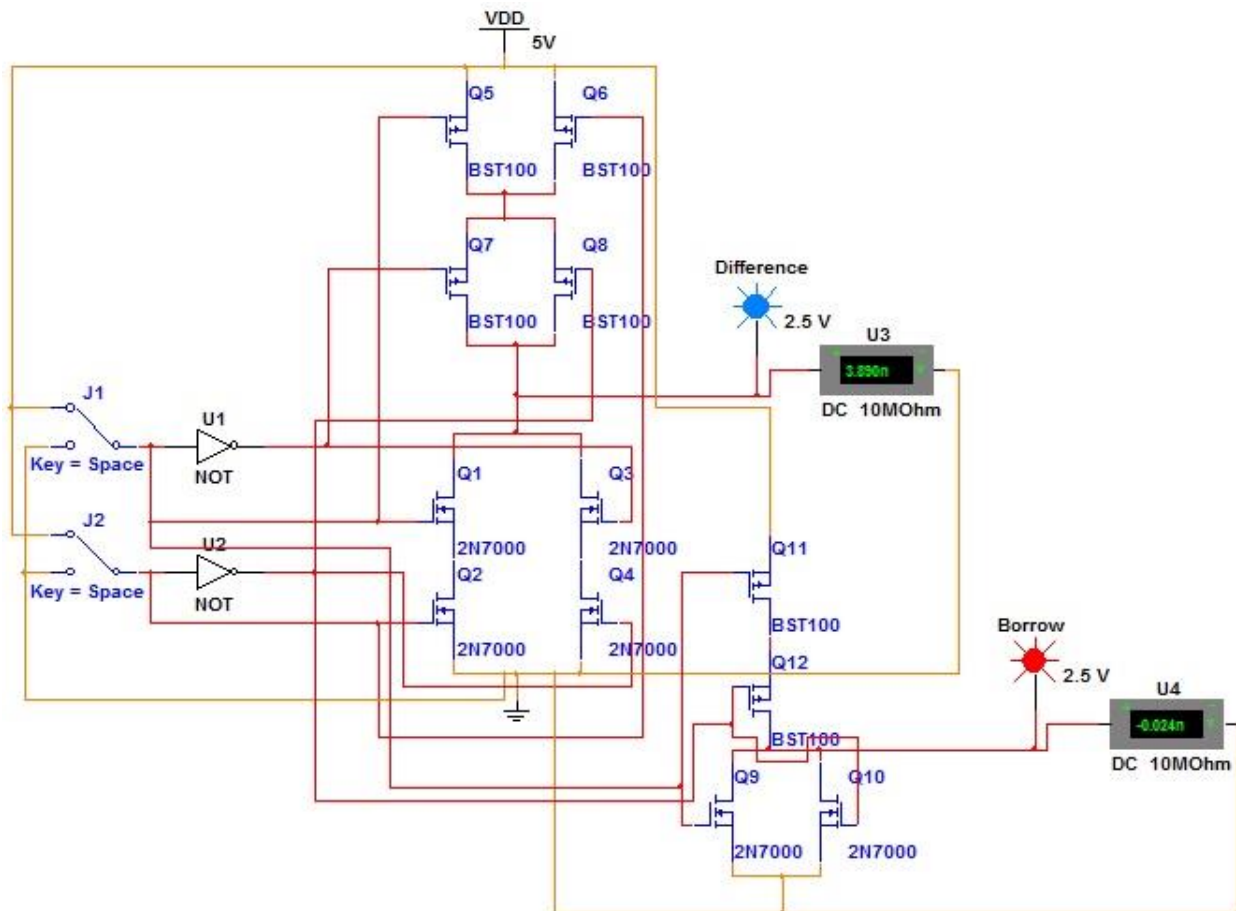
Circuit Diagram

8. CMOS Half Adder



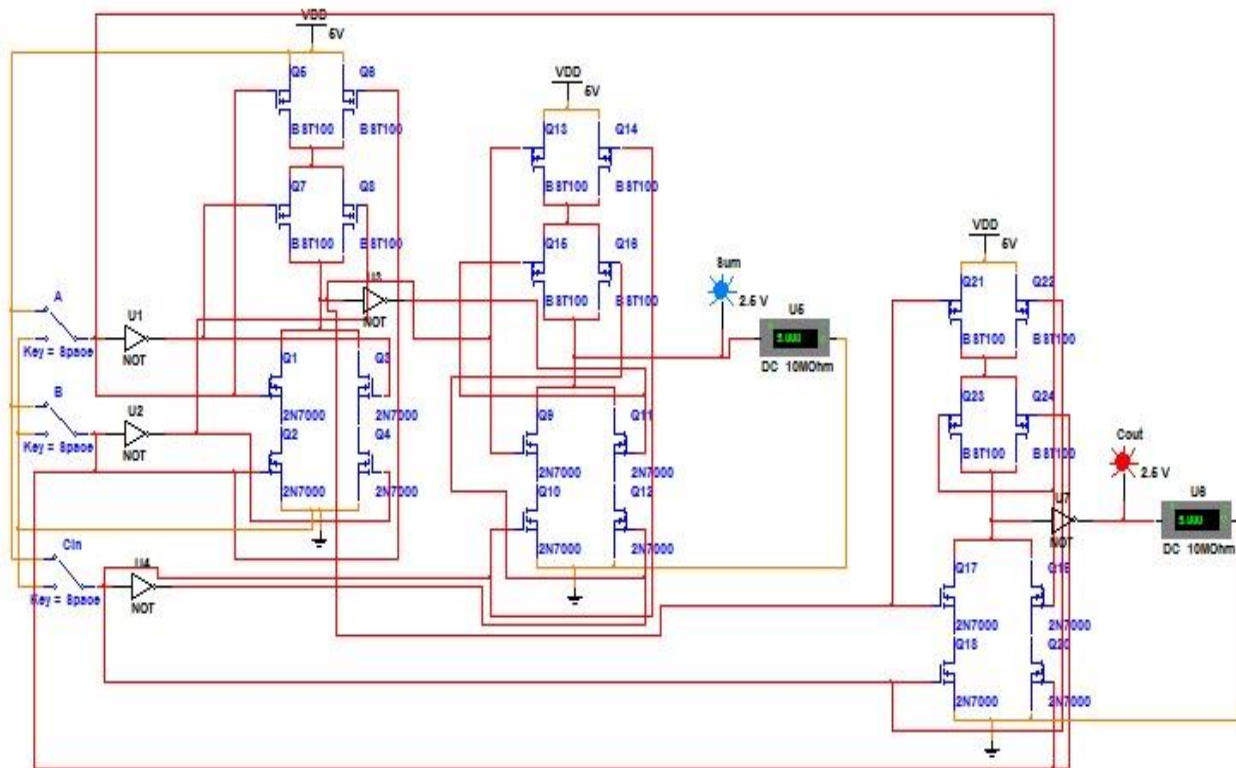
Circuit Diagram

9. CMOS Half Subtractor



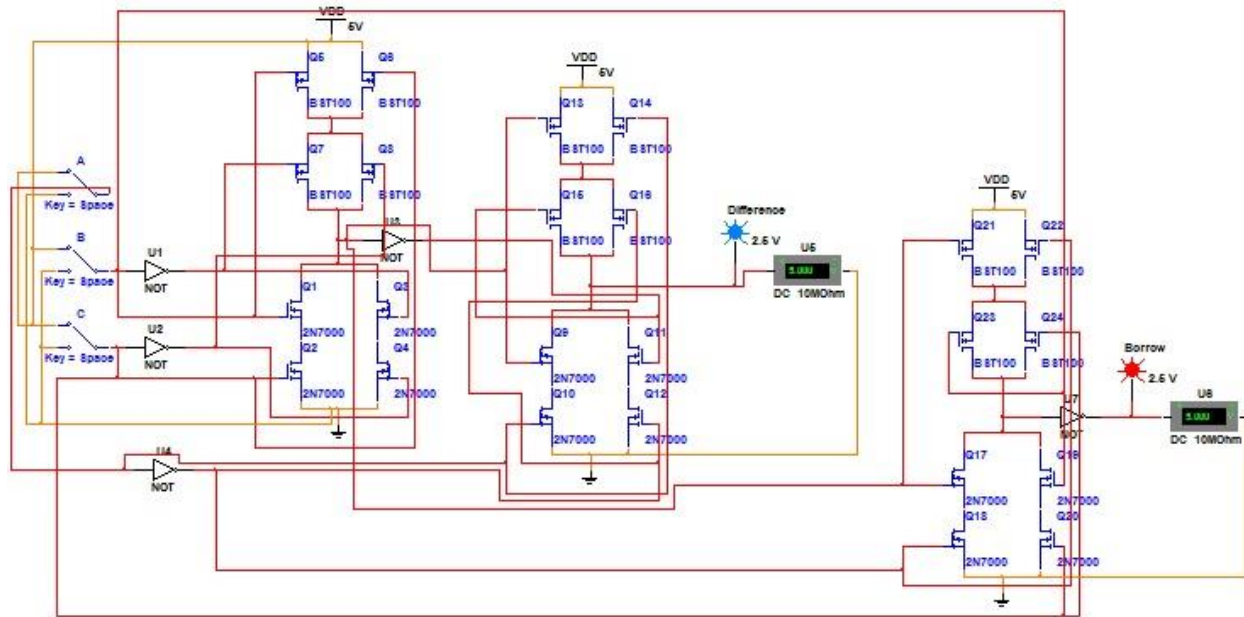
Circuit Diagram

10. CMOS Full Adder



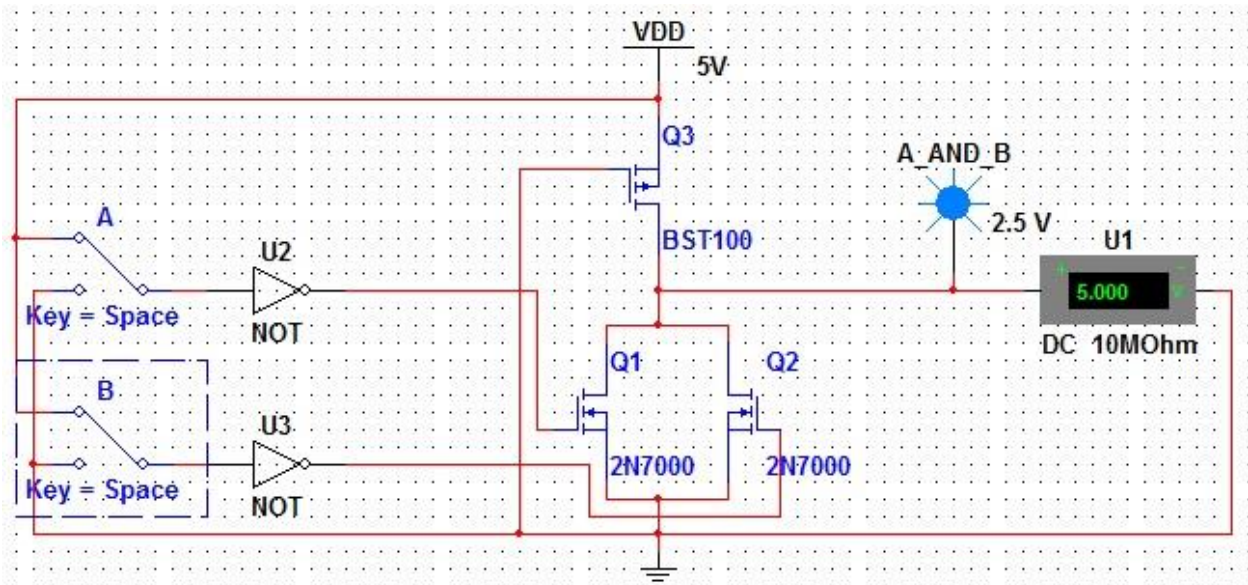
Circuit Diagram

11. CMOS Full Subtractor



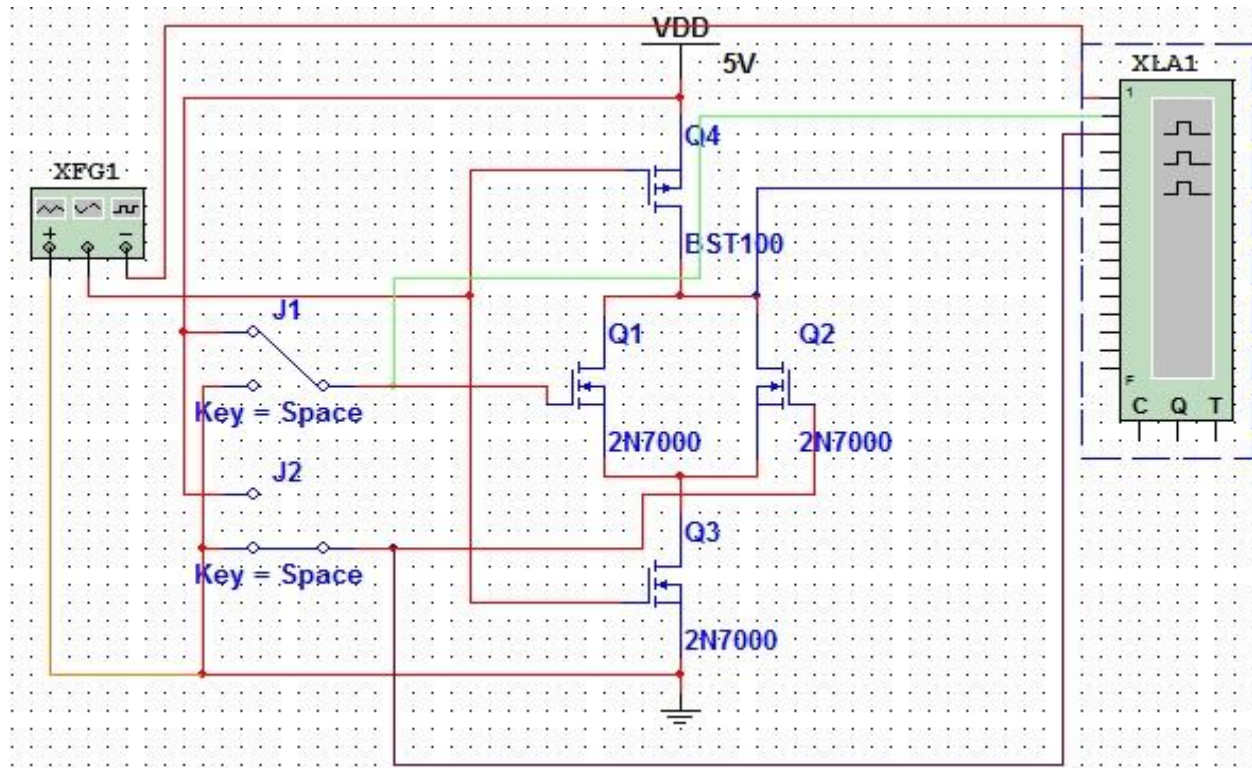
Circuit Diagram

12. Pseudo NMOS AND Gate



Circuit Diagram

13. Dynamic CMOS NOR Gate



Circuit Diagram