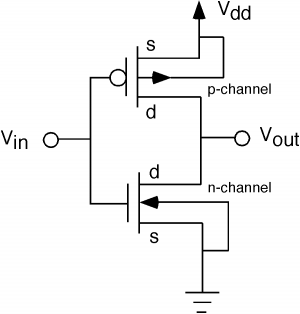
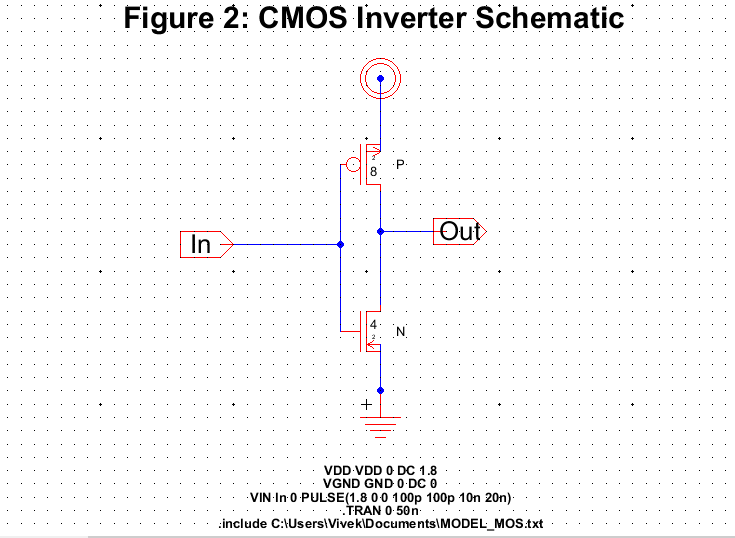
**Introduction**

The inverter is a basic building block in digital electronics. Multiplexers, decoders, state machines, and other complex devices use inverters. Inverter also has the most basic design with two transistors. Inverter uses a P-mos and N-mos transistors in series. Source of the p-mos is connected to voltage source and the source of the n-mos connected to the voltage. A voltage input is introduced to the gate of these two transistors.

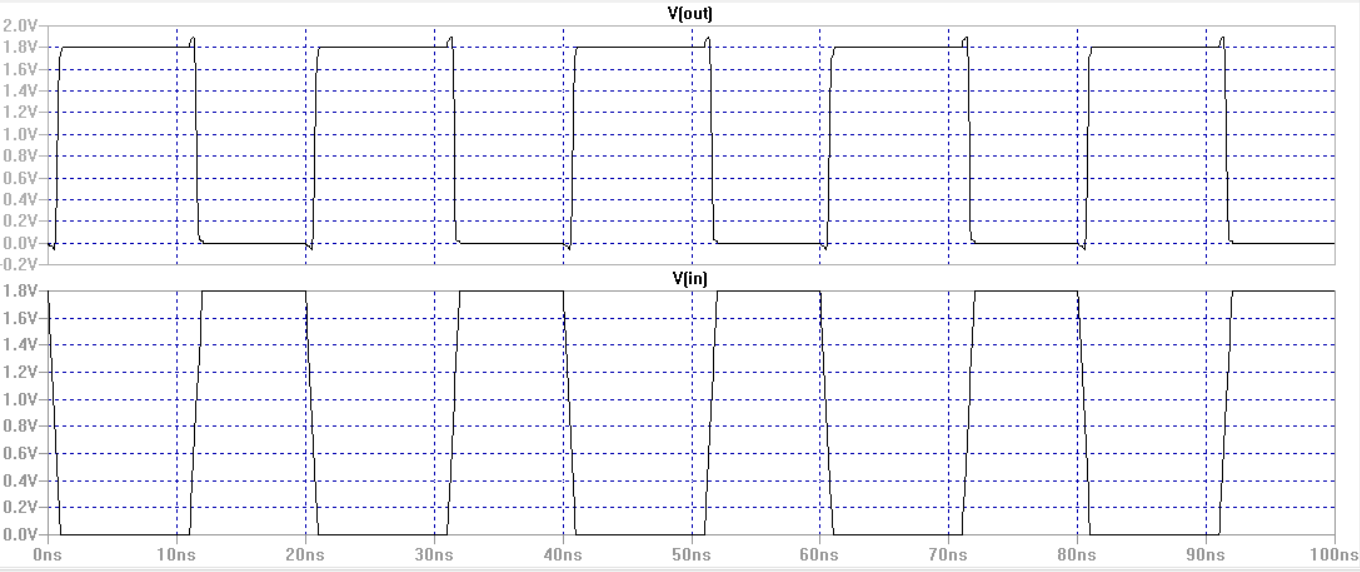
**Figure1: Inverter Circuit**



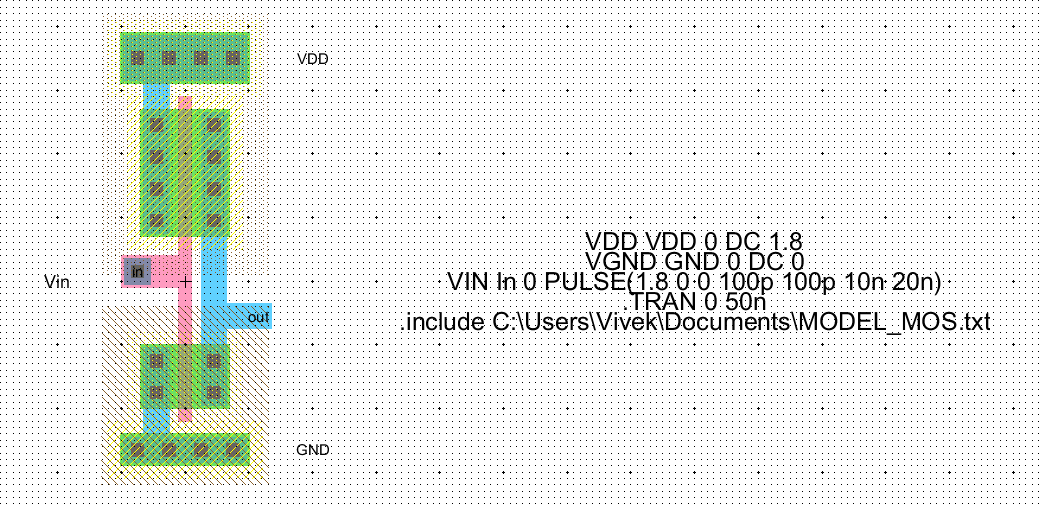
In the case of input to be high, the transistors act like switch with the p-mos not allowing the current and the n-mos is closed causing the voltage output to be low. If the voltage input is low p-mos acts like a closed switch causing current to flow and sets the voltage output to be high, while n-mos is open.



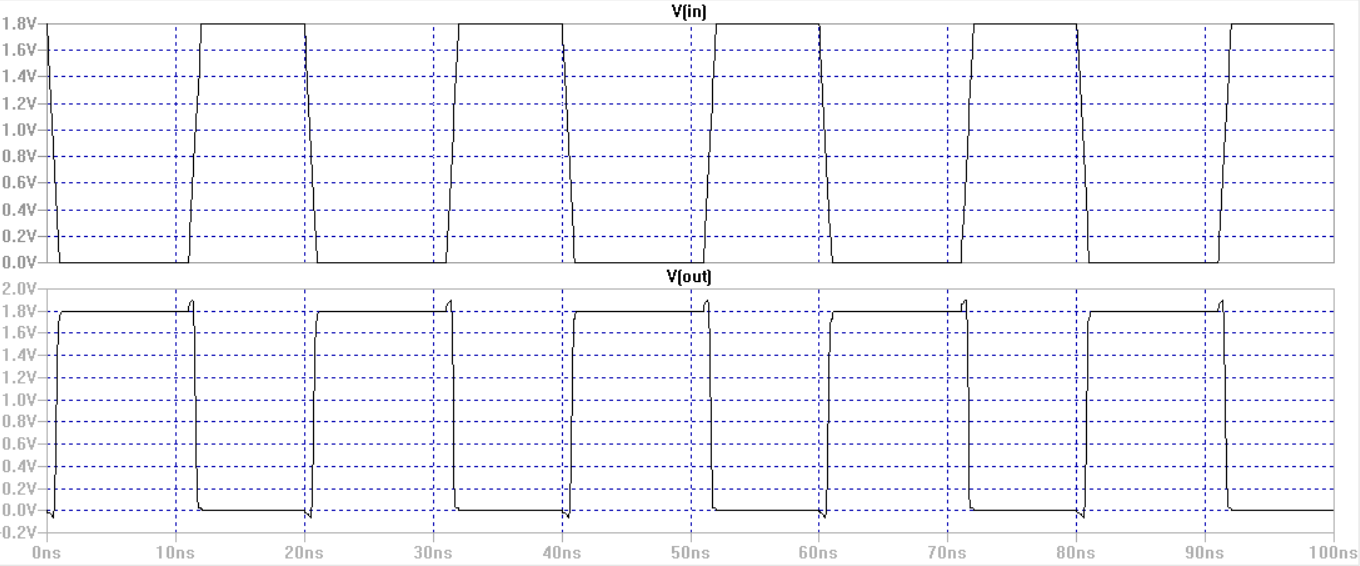
**Figure 3: LTSpice simulation of Inverter Schematic**

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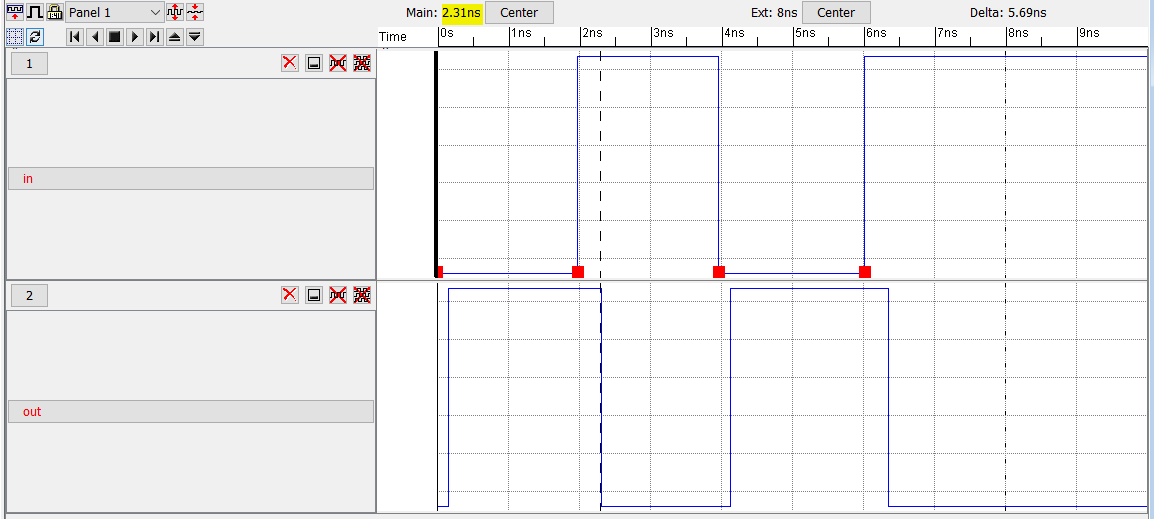
**Figure 4: Inverter Layout**

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**Figure 5: LTSpice simulation of Inverter Layout**

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**Figure 6: IRSIM of Inverter Layout**

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As seen above in the figure, the inverter takes the input signal and outputs the opposite of the input signals. From 0 to 2ns(nanoseconds) input is low and output is high, from 2ns to 4ns input is high and output is low. The IRSIM also indicates the delay in input and output signals. As shown in the graph, the input high is at 2ns but the output doesn't change till 2.31ns(shown in yellow highlight and dotted line). This is due to the delay in processing the input signal by the inverter.

**Conclusion**

Logic inverters are the basic building block in digital electronics. It is made up of P-mos and N-mos transistors in series connection. Logic inverters takes the input signal and outputs the inverse signal. That is, if the input Voltage is 0 output voltage is 1 and if the input Voltage is 1 the output voltage is 0. As seen in the schematics simulation graph, there is a tiny time delay between input and output about few nanoseconds. This is due the time it takes for the transistors to turn on and off.

**Explanation of Results:**

In the graphs of both CMOS inverter layout and schematics there is a time delay in the output. That is, when the input triggers the inverter it takes some time for the inverter to respond. There is a time delay in the fall and rise of the inverter output pulse. The delays can be represented by tr and tf. The delay is due to the small resistance within the P-mos and N-mos transistors in the inverter circuit. These resistance are called Rn for n-mos and Rp for p-mos. They are very small resistance and causes time delays in the scale of couple of nanoseconds. We have to deal with these delays in real life transistors and circuits.