8 bit sram spice code

VDD VDD 0 DC 3.3

VGND GND 0 DC 0

VIN1 CS 0 DC 3.3

VIN2 WE 0 DC 3.3

VIN3 D0 0 DC 0

VIN4 D1 0 DC 0

VIN5 D2 0 DC 0

VIN6 D3 0 DC 0

VIN7 D4 0 DC 0

VIN8 D5 0 PULSE(3.3 0 0 100p 100p 10n 20n)

VIN9 D6 0 PULSE(3.3 0 0 100p 100p 10n 20n)

VIN10 D7 0 PULSE(3.3 0 0 100p 100p 10n 20n)

VIN11 OutputEn 0 DC 3.3

.TRAN 0 50n

.include C:\Users\Vivek\Documents\MODEL\_MOS.txt

16 bit sram spice code

VDD VDD 0 DC 3.3

VGND GND 0 DC 0

VIN1 OutputEna 0 DC 3.3

VIN2 WritEna 0 DC 3.3

VIN3 Da0 0 DC 3.3

VIN4 Da1 0 DC 0

VIN5 Da2 0 DC 0

VIN6 Da3 0 DC 0

VIN7 Da4 0 DC 0

VIN8 Da5 0 DC 0

VIN9 Da6 0 DC 0

VIN10 Da7 0 DC 0

VIN11 RegA 0 DC 3.3

.TRAN 0 100n

.include C:\Users\Vivek\Documents\MODEL\_MOS.txt