MID 18 ii

Write a program to do the following in 8051 assembly language.

Create a square wave of 50% duty cycle on bit 0 of port 1.

Assume that register A has packed BCD, Write a program to convert packed BCD to two ASCII numbers and place them in R2 and R6. Use ANL and RR instruction.

Explain various addressing modes in 8051, with example.

What are the different forms of Jump Instruction in 8051. Discuss with example, with each form.

Explain RAM Memory space allocation in 8051 microcontroller.

Explain different application, specific architecture in 8051 microcontroller.

What are different specific requirement of an Embedded system. Explain, with example, the state transition behavior decomposition, exception with PSM model and spec chart language.

Specify answer behavior of telephone answering machine with PSM and specified language.

MID 19 i

Discuss the characteristics of embedded systems. List the various application areas of embedded system and give examples of each application area.

Distinguish between Harvard and Von-Neuman Processor/controller architecture.

What are the advantages of hierarchical FSMs over Traditional “flat” FSMs. Also, list merits and demerits of hierarchical Concurrent FSM.

Why data flow graph is a weak candidate for modeling embedded systems. List the difference between flowchart and structure chart.

Define characteristics of conceptual models in Embedded Systems.

MID 19 ii

Compare VHDL and spec charts with respect to their ability to support the following conceptual model characteristics.

- Synchronization
- Communication
- Timings

Describe the major difference between a functional specification of a system and its structural implementation. What are the useful aspects of each?

Specify a traffic light controller with Spec charts and with statecharts.

MID 22

Addressing modes of 8051 microcontroller.

RAM allocation in 8051 microcontroller and program status world that is flag register.

Explain the behavior of embedded system, whose utilization results with respect to clock is given.

The estimated and actual measured value are given, for the quality metric for four design implementation. Compute the fidelity of estimated use.

Apply the operator used method to estimate the number of control steps that the set of VHDL atatements below will be scheduled into. Assume that the clock cycle is 25ns, And that one multiplier (100 bs delay) and 2 Adder (15 ns delay) will be used to implement the design.

A = B + (C + 3);

B = B + C + D;

E = A * A;

X = C + D + Y;

D = A + E;

Estimate. The average lifetime and clock utilization to compute the following second order differential equation 5x^4 - x^3 - y^2 + x + 3 Using the maximum operator delay (MOD) method. Assume delay for adder, subtracted. In multiplier, is 55 60 and 160 ns?

For the following we as real equations. Construct a control flow graph with probabilities.

Analyze the edge probabilities and determine the execution frequency of each individual nodes.

Answer the following related to system partitioning.

What are the main draw backs of structural partitioning approach?

What are the advantages of functional partitioning over structural partitioning approach?

Give an non-weighted graph. apply an iterative Bisection partition algorithm (KL algorithm) for the balanced partition and determine the minimum cut size.

The description of sequential behavior is mentioned below using fork And Join statements. Write the process statement for the concurrent behavior of process A B C of X.

More ETE Questions

Specify the monitor behavior Of telephone answering machine with state starts.

Table given below shows the occurrence of various operations. In the description of a behavior, the delays of the functional units that implement the operations are also given estimate the clock cycle, using the maximum operator delay method and slack minimization method. Also compute the clock utilization for each of the two estimates.

Write a 8051 program to generate the table of two and display on the seven segment display.

Explain all flags in program, status word, register, Which flags in PSW may affect by ad by an ad instruction. What is the value of those flags after second instruction is executed.

MOV A,#3FH

ADD A, #D3H

What will happen when an interrupt event occurs and an interrupt flag for that event is enabled in 8051 microcontroller.

What happened when the two or more interrupt occurs at the same time in 8051 microcontroller.

Suppose that the interrupt priority IP register is configured as

MOV IP,#00001100B.

What will they be the priority order of the following default interrupts?

Timer1 timer0 int() int1 Serial

Draw the binary decision diagram for a + b. Then multiply with additional input c

Draw the binary decision diagram for a 4-bit, parity generator and 4 bit Parity checker.

Given the performance versus bus width trade-offs as shown. What are the constraints that need to be followed to select the desired bandwidth and clock for the optimized behavior for the process?

Explain click partitioning.