ELECTRONIC VOTING MACHINE

Hardware Design Document

Submitted by Group 54

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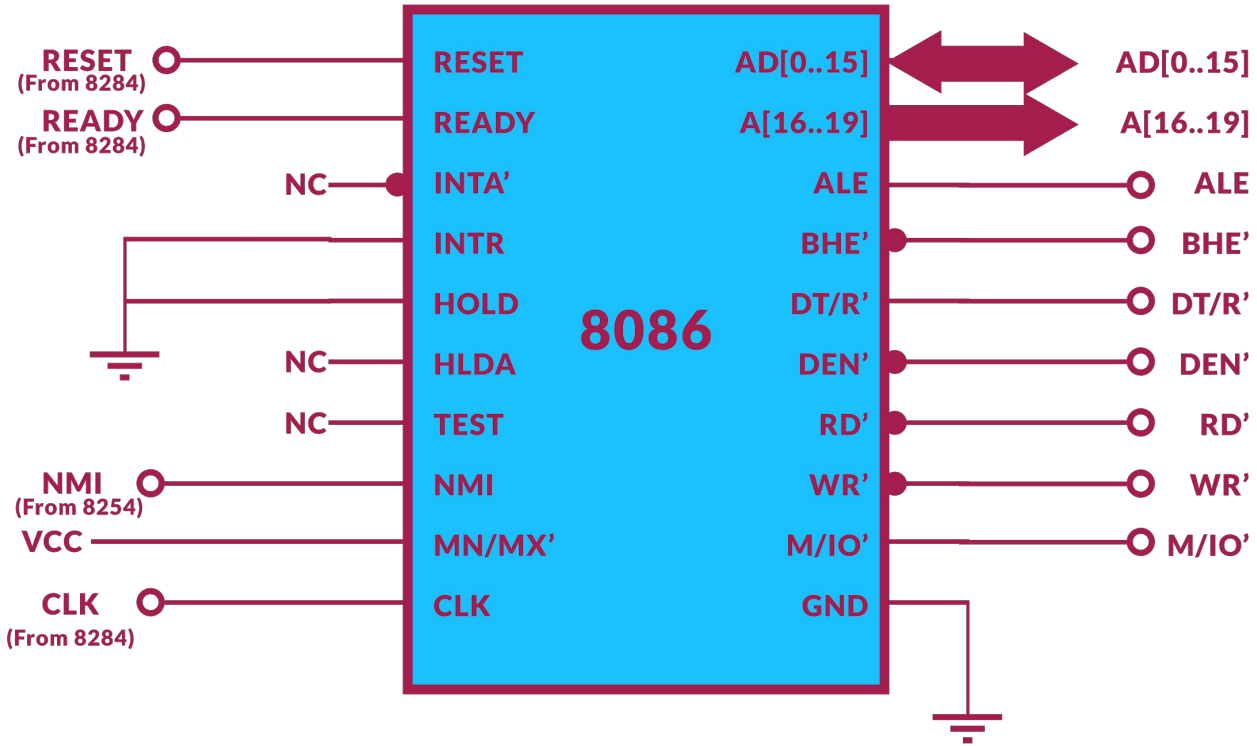
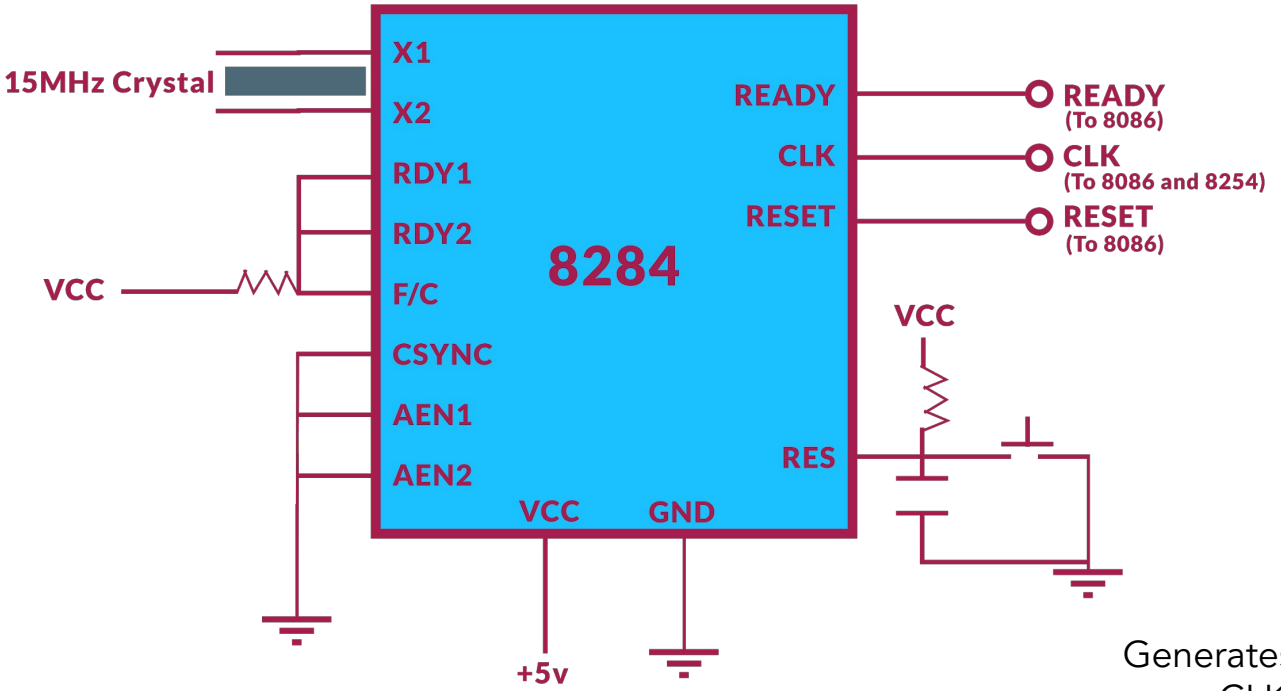


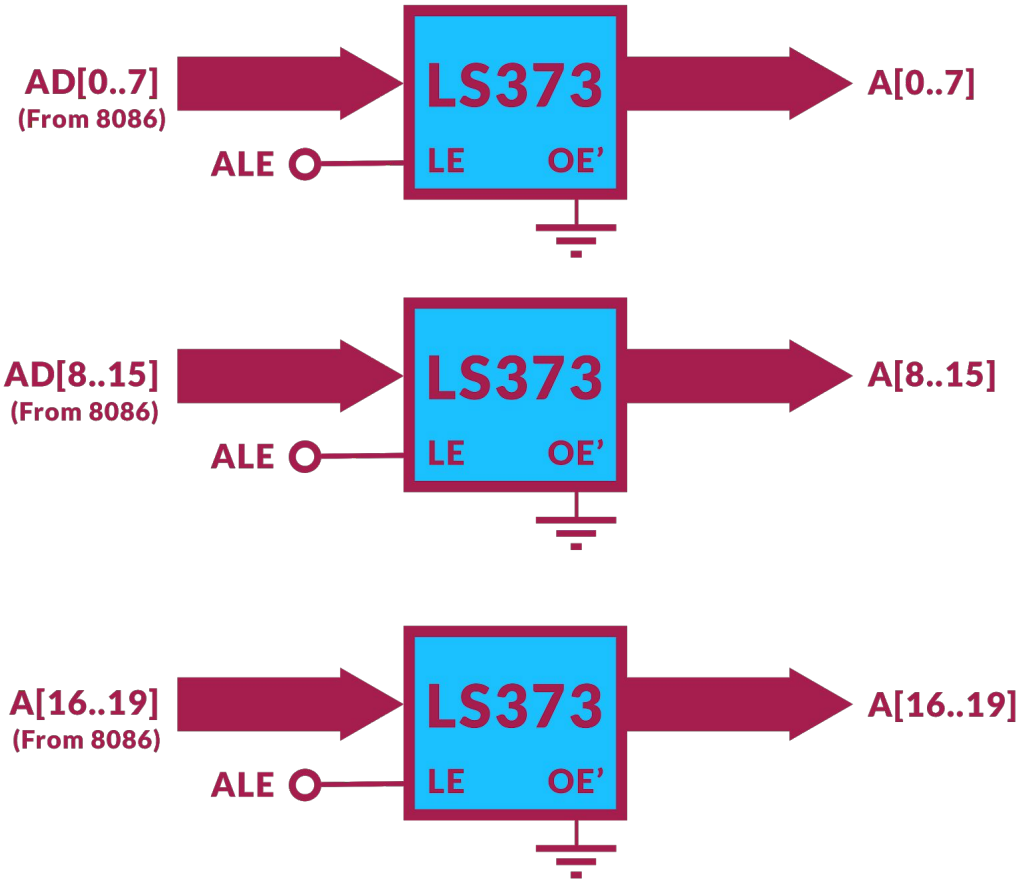
8086 Microprocessor with required connections



8284 Clock Generator

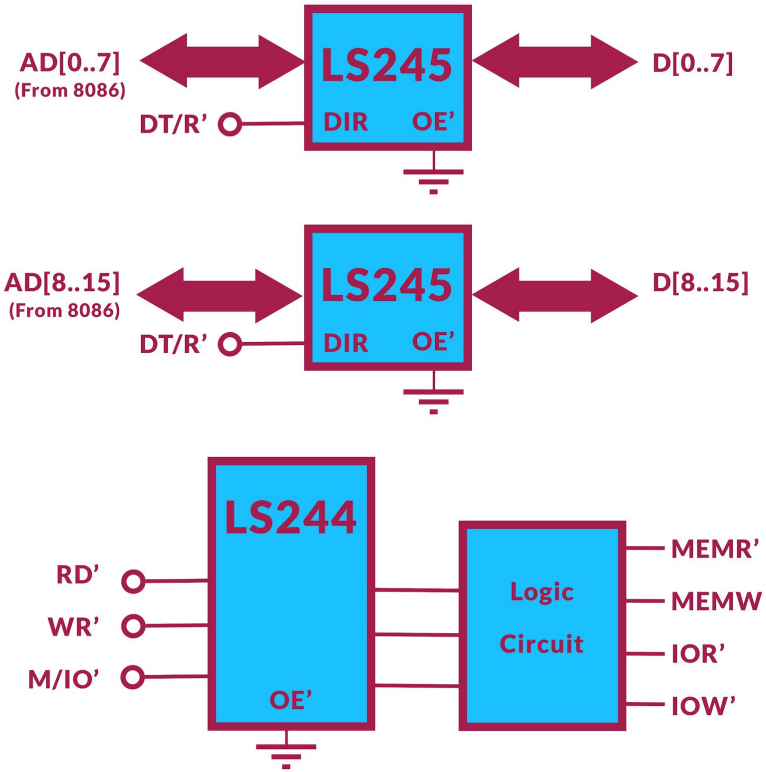
Generates:

- CLK @5Mhz
- PCLK @2.5Mhz
- RESET Signal on switch press

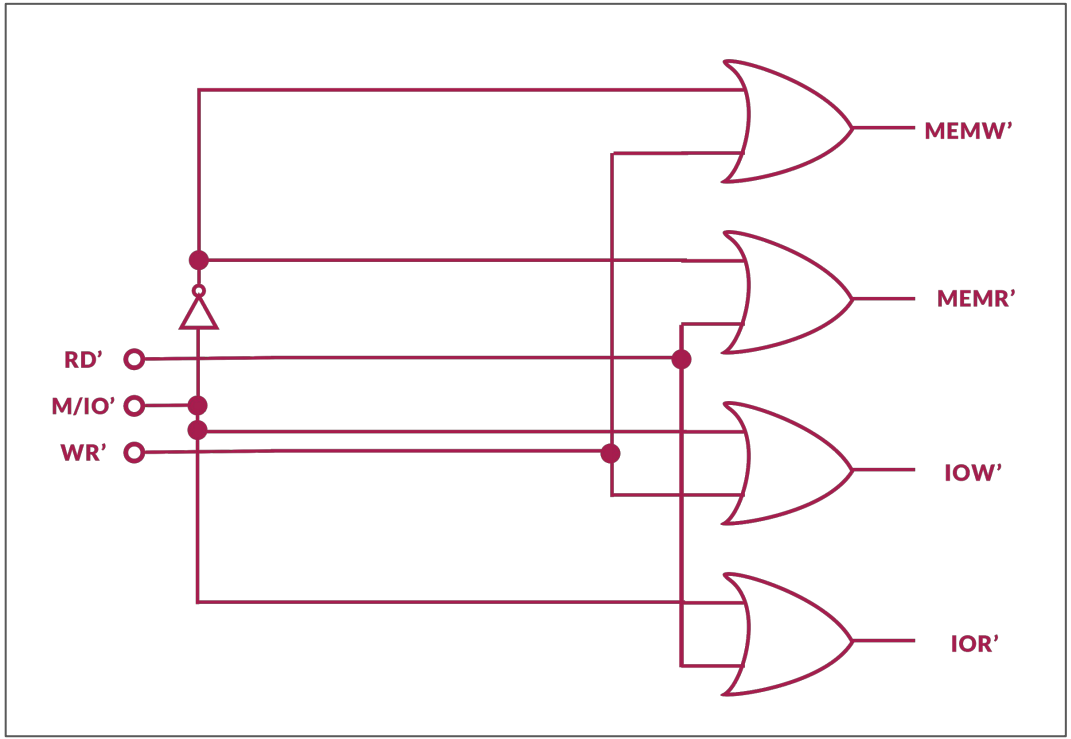


Address line Demultiplexing

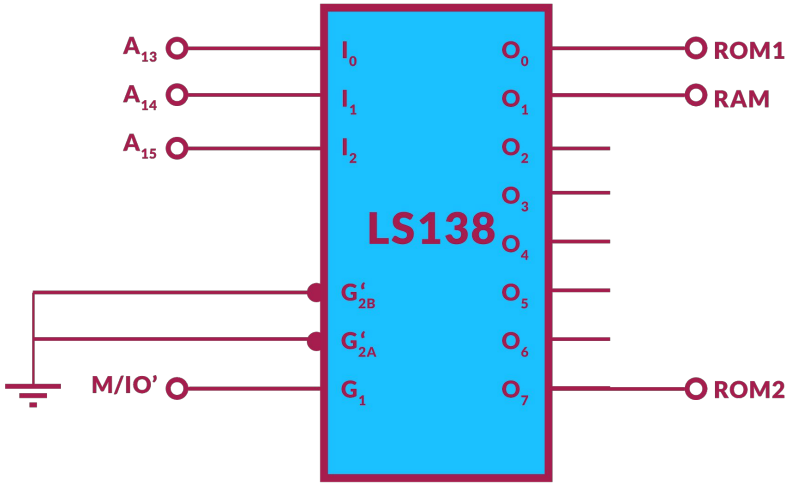
Data line Demultiplexing



Control Line generation

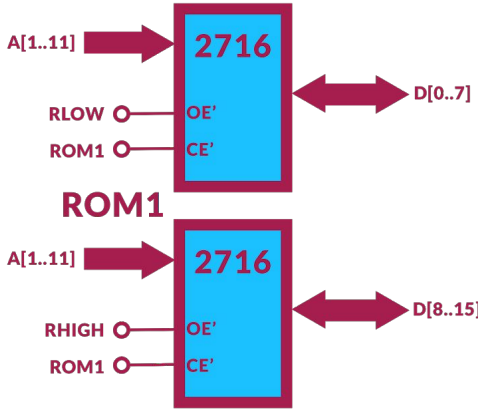


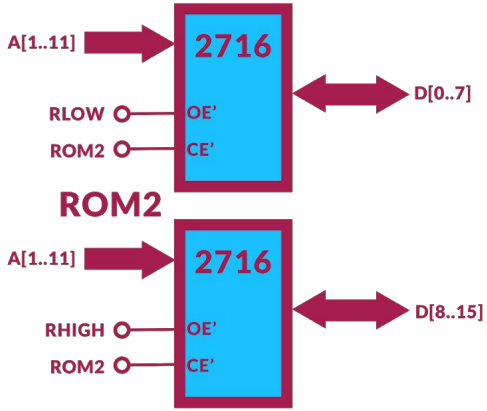
Logic Circuit as used

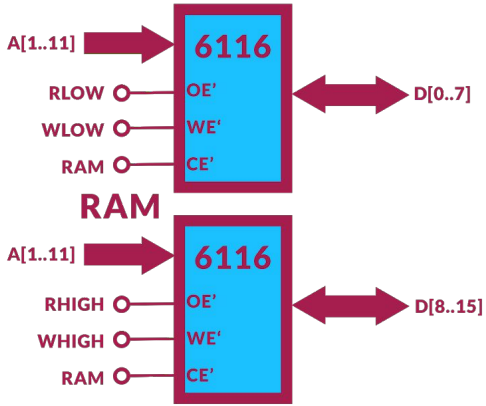


Memory Decoder

Control Line generation







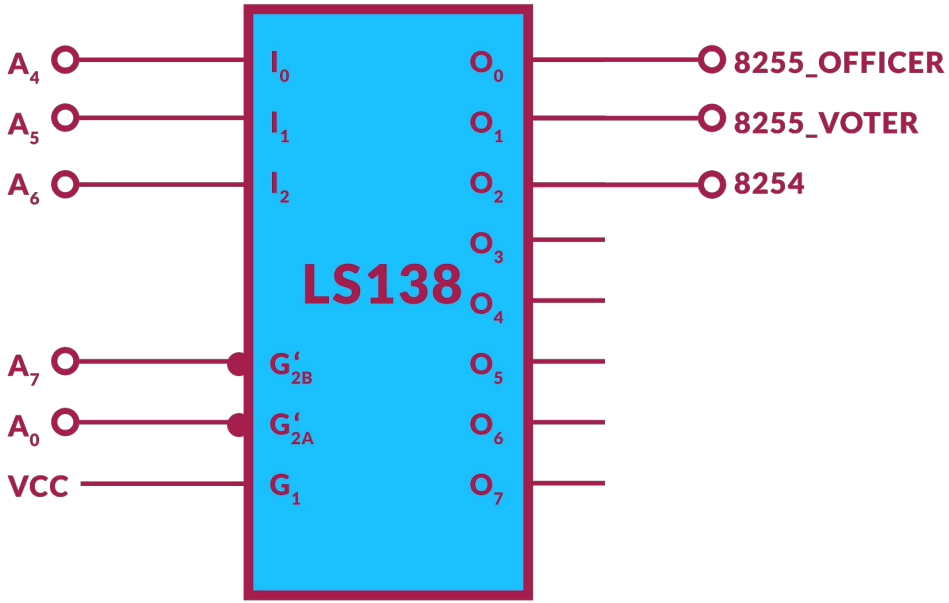
Memory Chips

Memory Addresses:

ROM1: 00000h to 00FFFh

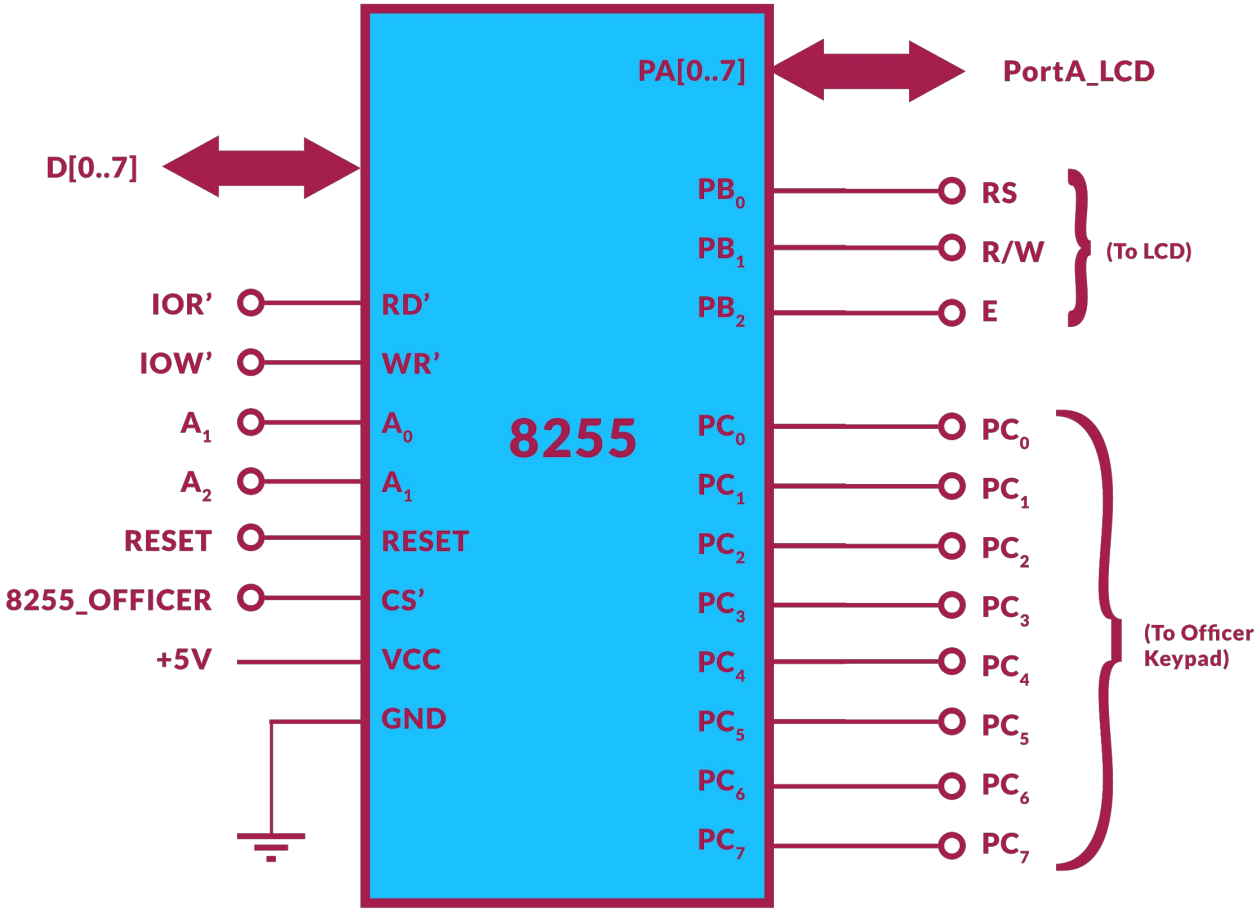
ROM2: 02000h to 02FFFh

RAM: FF000h to FFFFFh



I/O Decoder

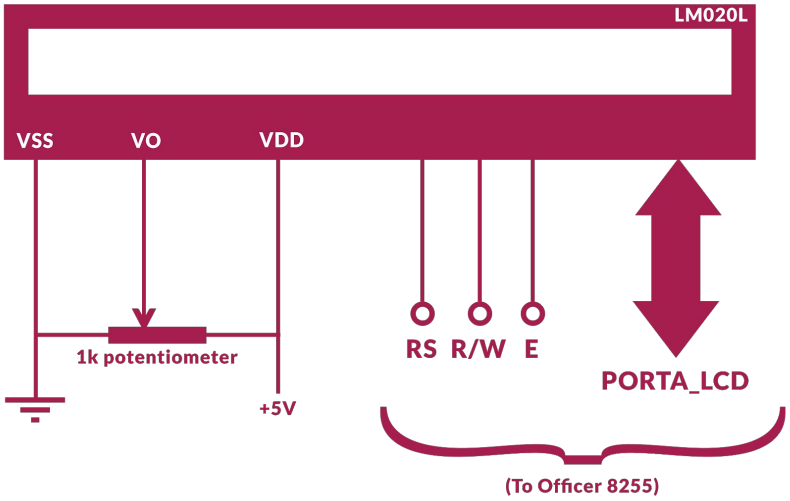
IO Addresses:
Officer Side 8255: 00h to 06h
Voter Side 8255: 10h to 16h
8254: 20h to 26h



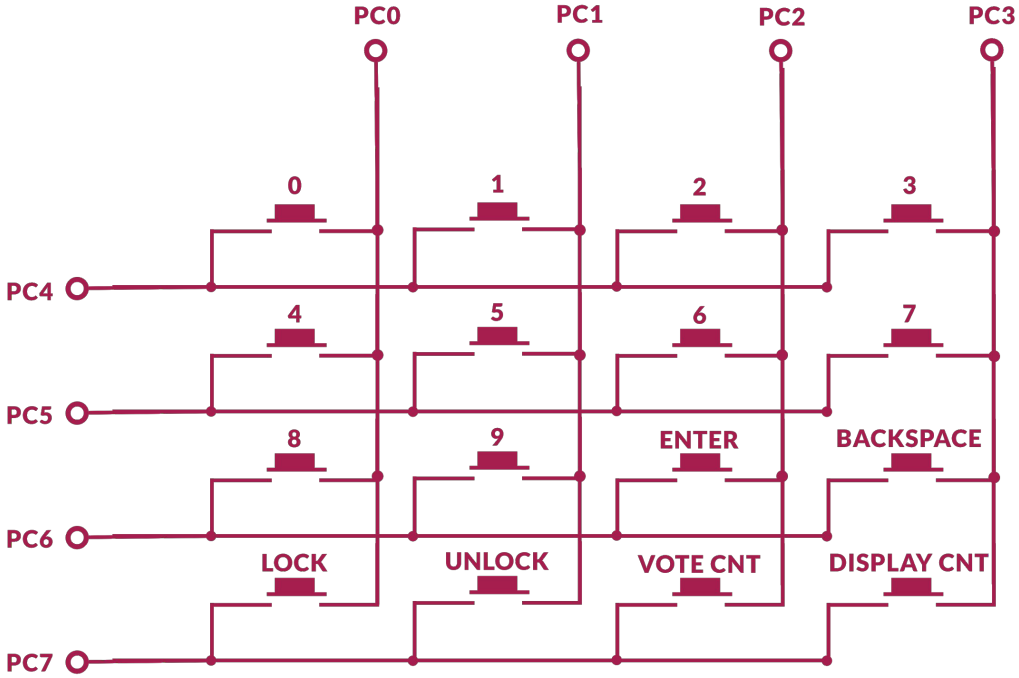
Officer Side 8255

Addresses:
Port A @ 00h
Port B @ 02h
Port C @ 04h
Control Reg @ 06h

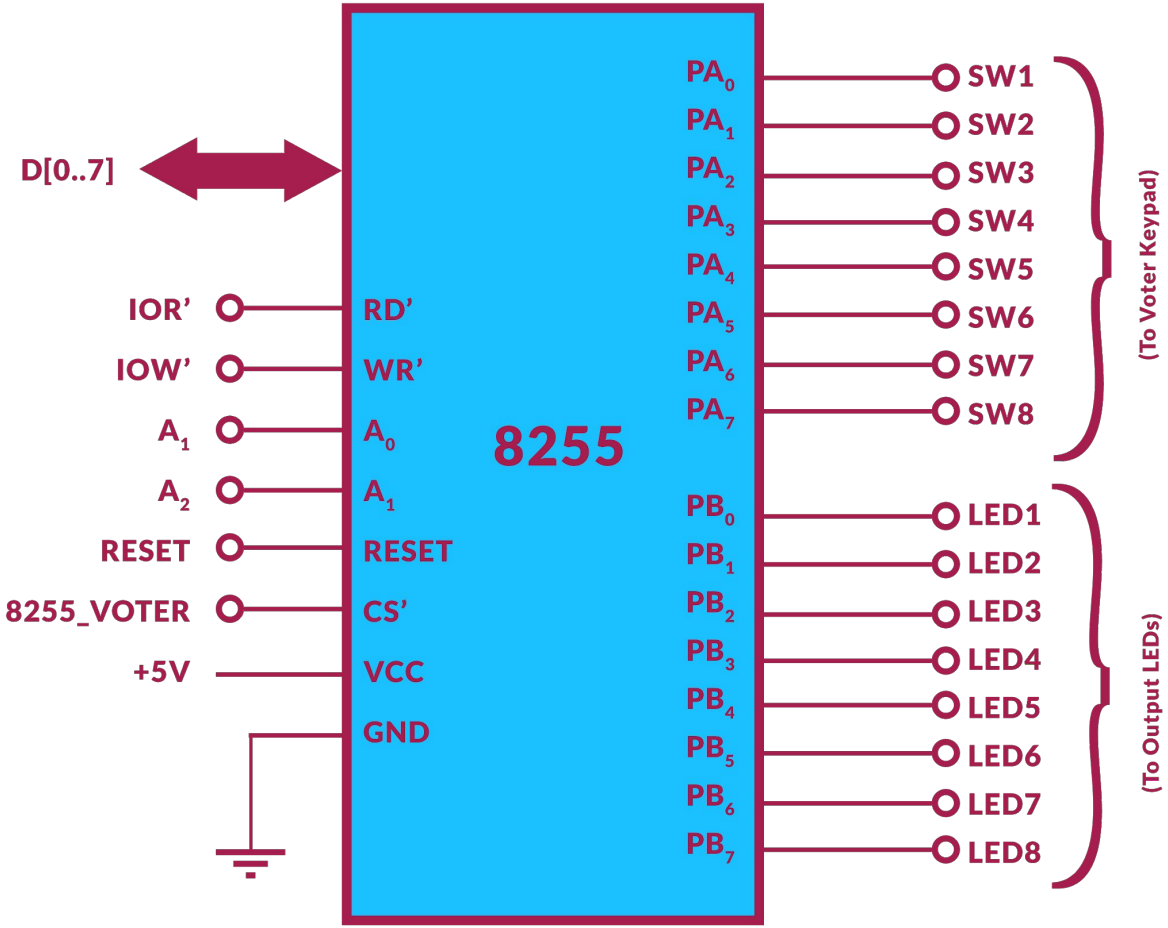
I/O Devices:
Port A: LCD Data-lines
Port B: LCD Control-Lines
Port C: Officer's Hex Keypad



16x1 LCD Display (to Port A and B of Officer 8255) (LM020L)



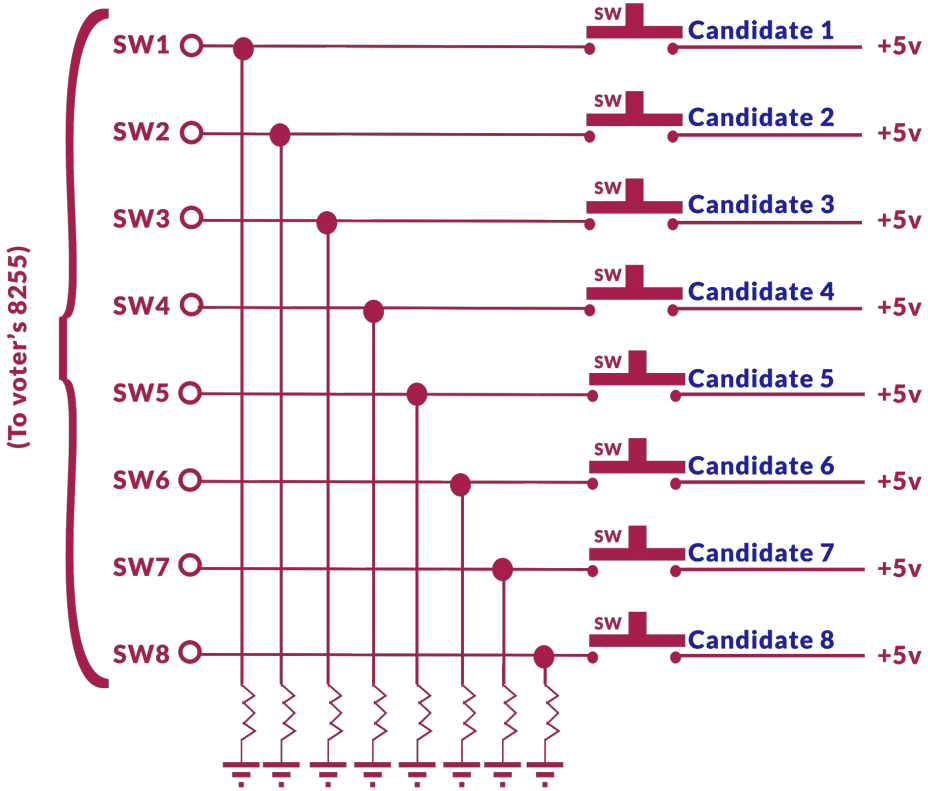
Officer's Hex Keypad (to Port C of Officer 8255)



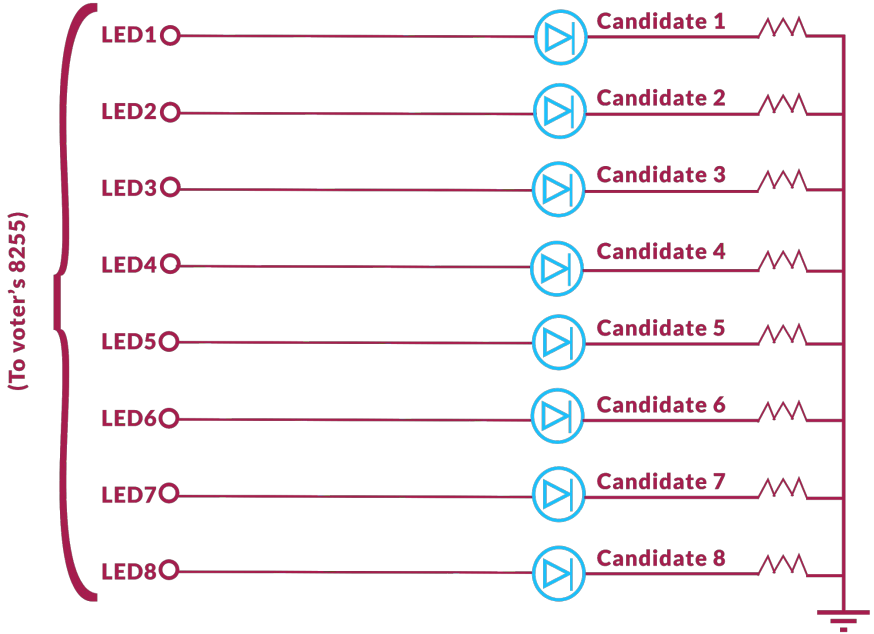
Voters' side 8255

Addresses:
Port A @ 10h
Port B @ 12h
Port C @ 14h
Control Reg @ 16h

I/O Devices:
Port A: One-hot voter buttons
Port B: One-hot Output LEDs
Port C: *unused*



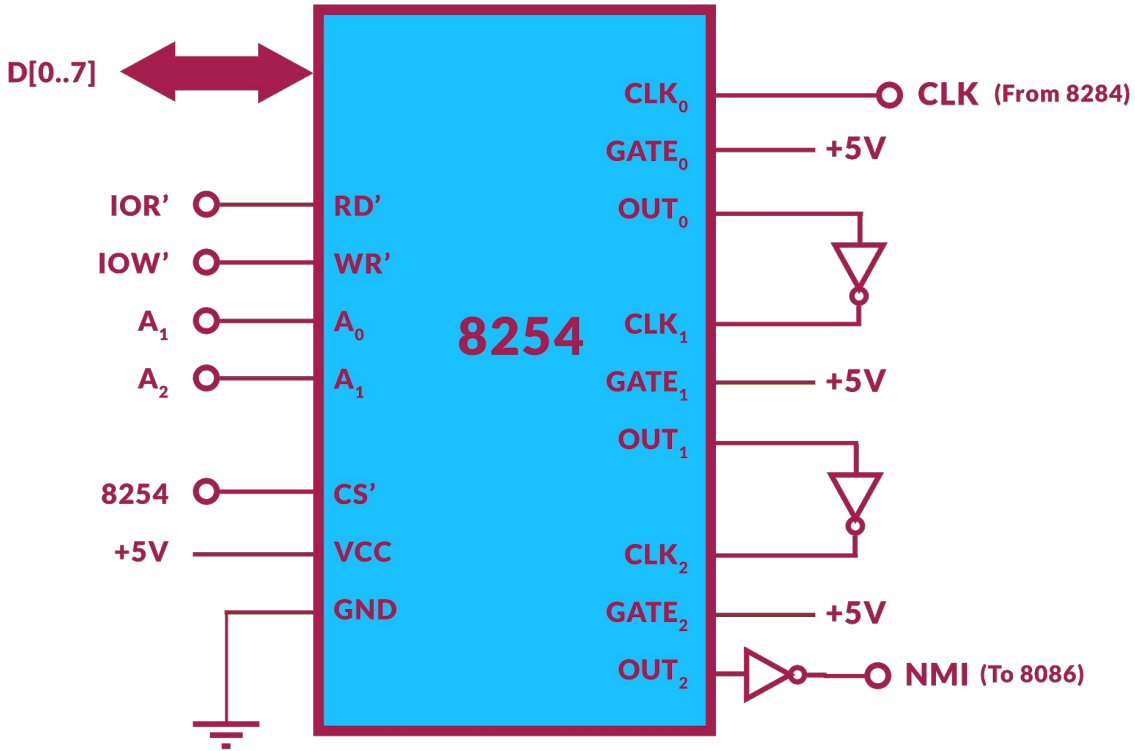
Voter's Input buttons (to Port A of Voter's 8255)



Output LEDs (to Port B of Voter's 8255)

Configuration:
Counter 0: Mode 2 (Count=50,000d)
Counter 1: Mode 2 (Count=100d)
Counter 2: Mode 0 (Count=36,000d)

Outputs:
OUT 0 @ 100Hz
OUT 1 @ 1Hz
OUT 2 @ 1/10 Hours



8254 Counter Chip

Addresses:
Counter 0 @ 20h
Counter 1 @ 22h
Counter 2 @ 24h
Control Reg @ 26h