

Acknowledgements

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Preface

Nonlinear dynamical systems exhibit many counterintuitive phenomenon and phenomenon like chaos and stochastic resonance challenge our everyday intuitions. In this book we explore the *application of nonlinear systems in the design of computing devices*. Specifically, we study the possibility of utilizing the phenomenon of stochastic resonance in bistable or multi-stable nonlinear dynamical systems to implement memory and logic function. This phenomenon has commonly been referred to as ``Logical Stochastic Resonance (LSR)". We demonstrate how noise enables a bistable system to behave as a memory device, as well as a logic gate for sub-threshold input signals. We show how this system can implement memory using noise constructively to store information. Namely, in some optimal range of noise, the system can operate flexibly, both as a AND/OR gate and a Set-Reset latch, on variation of an asymmetrizing bias.

Then we examine the intriguing possibility of obtaining dynamical behavior equivalent to LSR in a noise-free bistable system, subjected only to periodic forcing, such as a sinusoidal driving or rectangular pulse trains. We find that such a system, despite having no stochastic influence, also yields phenomenon analogous to LSR, in an appropriate window of frequency and amplitude of the periodic forcing. The results have been corroborated by electronic circuit experiments.

Next we demonstrate that the width of optimal noise window can be increased by utilizing the constructive interplay of noise and periodic forcing, namely, noise in conjunction with a periodic drive enables the system to yield consistent logic outputs for all noise strengths below a certain threshold. Thus, we establish that in scenarios where noise level is below the minimum threshold required for LSR (or stochastic resonance in general), we can add a periodic forcing to obtain the desired effects. We have also shown that the periodic forcing results in lower latency effects and reduces the switching time, leading to faster operation of the devices. Further, if a LSR element is coupled to another LSR element with a lower potential barrier, then it is able to adapt to varying noise intensity, so that its operation remains robust even under high noise conditions.

Lastly, we test these concepts in vertical-cavity surface-emitting lasers (VCSELs) which are widely used for high-bit-rate data transmission because of their various advantages over conventional edge emitting lasers like low threshold current, single-longitudinal-mode operation, higher modulation bandwidth and circular output beam profile. We attempt to enhance the operational range of VCSEL based stochastic logic gate by adding a periodic signal. The enhancement is observed in form of decrease in the minimum bit time necessary for successful operation or increase of size of the optimal noise window.

In the last chapter of the thesis, we conclude our findings and summarize the important results of all the chapters. We also list some possible extensions of the works presented in this book.

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Chapter 1

Introduction

A system that evolves with time is called a dynamical system and such dynamical systems are often modeled by differential equations

$$\dot{X} = F(X) \quad (1.1)$$

where $X(t) = \{x_1(t), x_2(t), \dots, x_n(t)\}$ is a vector of state variables, t is time and $F(X) = \{f_1(X), f_2(X), \dots, f_n(X)\}$ is vector of functions that encode the dynamics [1]. If time is discrete, then the evolution is given by a map

$$X_{n+1} = F(X_n) \quad (1.2)$$

where X is state vector and F is a set of functions determining the flow of the phase point. If F is a nonlinear function in these coupled differential/difference equations then the system is referred to as nonlinear dynamical system.

Such nonlinear dynamical systems are hard to solve analytically, but the rapid rise in computing power has helped us to understand their behavior by employing numerical analysis techniques. Through numerical simulation of the dynamical equations, it has been found that even very simple dynamical systems can exhibit a range of dynamical behaviours from fixed points and limit cycles to very complex and counterintuitive behaviours like chaos and fractals [2].

An ubiquitous feature of real systems is the presence of noise. Noise has tra-

ditionally been considered a nuisance and something which one should get rid off. Lately, noise has been shown to play not only beneficial but crucial role in many biological and engineering systems. The cooperative interplay of noise and nonlinearity in dynamical systems has attracted the attention of researchers from diverse fields ranging from electronic systems to geologists. Phenomenon such as stochastic resonance (SR), that is, the enhancement of response of a nonlinear system to a weak signal with the assistance of noise have been studied extensively [3, 4].

Stochastic resonance has been observed in a large variety of systems, including bistable ring lasers [5], semiconductor devices [6, 7, 8], chemical reactions [9], neuronal ensembles [10], vertical cavity surface emitting lasers [11], delayed feedback systems [12], geomagnetic polarity reversals [13] models of opinion formation [14] and mechano-receptor cells in the tail fan of a crayfish [15]. The phenomenon of stochastic resonance has been utilized in realizing logic gates [16], information transmission and storage [17, 18], harvesting vibrational energy and genetic switches [19]. It has also been observed with different types of noise like colored noise [20, 21, 22, 23], combination of multiplicative and additive noise [24, 25], pinning noise [26] and in periodic potentials [27, 28].

1.1 Stochastic Resonance in double-well potential

The standard equation of a double-well potential is:

$$V(x) = -a_1x^2/2 + a_2x^4/4 \quad (1.3)$$

where $a_1, a_2 > 0$. The height and width of the energy barrier are $h = a_1^2/4a_2$ and $w = 2\sqrt{a_1/a_2}$ respectively. The force field corresponding to this potential barrier is $F(x) = -dV(x)/dx = a_1x - a_2x^3$. If we neglect inertia and consider the over-damped limit, then the stochastic differential equation (SDE) governing the dynamics is

$$\dot{x} = F(x) + A\sin(\Omega t) + D\eta(t) \quad (1.4)$$

where $\eta(t)$ is Gaussian noise and $\sin(\Omega t)$ is the driving force with amplitude A . In numerical integration schemes, the Gaussian noise is band-limited by the integration time step dt to a Nyquist frequency $f_{NQ} = 1/(2dt)$. Noise is quantified by its mean squared amplitude or noise power $\sigma^2 = 2Df_{NQ}$ where $2D$ is the height of the one sided noise spectrum. In absence of driving force ($A = 0$), the mean escape time from either potential well is given by:

$$1/\tau_K = r_K = (\omega_b\omega_0/2\pi)\exp(-h/D) \quad (1.5)$$

where r_K is the Kramer's rate and $\omega_0^2 = 2a_1$ and $\omega_b^2 + a_1$ represent the angular frequencies at the potential minima and at the top of the barrier.

At very low noise strength, mean escape time τ_K is very large, so the effective frequency $1/2\tau_K \ll \Omega$ and the periodic part is not detectable. Similarly, for large D , $1/2\tau_K \gg \Omega$ and periodic part is not perceptible. SR takes place when both frequencies are close, i.e.

$$T_\Omega \equiv 2\pi/\Omega = 2\tau_K(D) = (2\sqrt{2}\pi/k_1^2)\exp(k_1^2/4Dk_2) \quad (1.6)$$

In this case even when $A < h$, the inter-well switching frequency is close to the frequency of the driving force and this resonance of the two frequencies is called as SR. So the output signal-to-noise ratio (SNR) is maximum for some nonzero noise[29].

1.2 Stochastic Resonance in computing systems

Noise in physical systems is one of the biggest challenge for people engaged in design and development of computing devices. The rapid shrinking of computing platforms with smaller power supplies has brought with it problems of smaller noise margins and higher error rates. So wide ranging research efforts in recent years have focused on the issue of reliable operations in the presence of a noise floor[18, 30].

In this context, it was shown that a noisy nonlinear system, when driven by two

square waves encoding two logical inputs, consistently goes to a state that mirrors a logical combination of the two inputs (such as AND/NAND and OR/NOR logic) in some optimal range of noise. That is, the probability of getting the correct logical response increases to unity with increase in the intensity of noise and then decreases again when noise exceeds the optimal range. Further one can vary the threshold (or bias) and morph the output into different logical functions.

This concept, named ``Logical Stochastic Resonance'' (LSR) [16, 31], helps one gain understanding of the counter-intuitive interplay between noise and nonlinearity [3, 32, 4]. Further, from the applied viewpoint, this idea can potentially lead to the design of flexible logic gates with enhanced performance in noisy environments. The main feature of LSR is the capability of the nonlinear device to work optimally in a range of environmental noise; hence LSR is a practical and reasonable answer for computational devices wherein the noise-floor cannot be suppressed. The relevance of LSR has been established in physical systems, ranging from electrical [33] and nanomechanical [34] to optical systems [35, 36]. It has also been found to occur in chemical [37] and biological [38, 39] scenarios.

Now we briefly discuss the general principle of LSR.

1.3 General Principle of LSR

Consider a general nonlinear system,

$$\dot{x} = F(x) + b + I_{in} + D\eta(t) \quad (1.7)$$

where $F(x)$ is a generic nonlinear function obtained via the negative gradient of a potential with two distinct stable wells. I_{in} is the input signal which encodes the logic inputs, b is bias to asymmetrize the two potential wells, and $\eta(t)$ is an additive zero-mean Gaussian noise with unit variance, with D being the amplitude(intensity) of the noise.

A logical input-output can be obtained by driving the system with two trains of

Logic inputs	OR	AND	NOR	NAND
0,0	0	0	1	1
0,1	1	0	0	1
1,0	1	0	0	1
1,1	1	1	0	0

Table 1.1: Relationship between the two logic inputs and the output of the fundamental OR, AND, NOR and NAND logic operations. On addition, the four distinct possible input sets $(0, 0)$, $(0, 1)$, $(1, 0)$ and $(1, 1)$ reduce to three conditions, as $(0, 1)$ and $(1, 0)$ are symmetric. Note that *any* logical circuit can be constructed by combining the NOR (or the NAND) gates [40, 41].

aperiodic square pulses: $I_1 + I_2$, encoding the two logic inputs. For logic operations such as OR/NOR and AND/NAND, we consider the inputs to take value I when the logic input is 1, and value $-I$ when the logic input is 0, where input strength I is: $0 < I < 1$. Since, the binary logic inputs can be either 0 or 1, they produce 4 sets of binary input: $(0, 0)$, $(0, 1)$, $(1, 0)$, $(1, 1)$. These four input conditions give rise to three distinct values of I_{in} . Hence, the input signal I_{in} generated, is a 3-level aperiodic wave form.

The state of this system, can be interpreted as logic output 1 when $x > x^*$ and logic output 0 when $x < x^*$, where x^* is roughly given by the position of the barrier between the two wells. Such an interpretation allows one to consistently obtain logical responses, such as OR and AND (see Table 1.1, when noise intensity D is in an optimal band. Complementary gates, NOR and NAND, can also be obtained in a straight-forward manner, by the alternate output determination : $x < x^*$ corresponding to logic output 1, and 0 otherwise.

In rest of this book, we extend the theoretical and applied aspects of LSR and demonstrate how stochastic resonance in bistable or multi-stable nonlinear dynamical systems can be utilized to implement memory and logic function. We show how a general nonlinear dynamical system can operate flexibly, both as a NAND/AND gate and a Set–Reset latch, by variation of an asymmetrizing bias. We also examine the possibility of obtaining dynamical behavior equivalent to LSR in a noise-free bistable system, subjected only to periodic forcing, such as sinusoidal driving or rectangular pulse trains.

Then we demonstrate how the width of the optimal noise window can be increased by utilizing the constructive interplay of noise and periodic forcing, namely noise in conjunction with a periodic drive yields consistent logic outputs for all noise strengths below a certain threshold. Thus we establish that in scenarios where noise level is below the minimum threshold required for logical stochastic resonance (or stochastic resonance in general), we can add a periodic forcing to obtain the desired effects.

We also verify our concepts in Vertical-cavity surface-emitting lasers (VCSELs) which are widely used for high-bit-rate data transmission because of their various advantages over conventional edge emitting lasers like low threshold current, single-longitudinal-mode operation, higher modulation bandwidth and circular output beam profile.

In chapter 2 we shall see how LSR elements can be used as memory devices and demonstrate noise-free LSR in chapter 3. In chapters 4 and 5 enhancement of optimal noise window using a periodic forcing is shown.

Chapter 2

Logic and memory from a sub threshold signal

2.1 Introduction

In this chapter we examine the possibility of utilizing a noisy nonlinear system, not just as a logic gate, but also *directly as a memory device*, i.e., we explore if the system can behave as a latch in some optimal range of noise¹.

A latch is a system that has two stable states and can be used to store state information. The system can be made to change state by signals applied to one or more control inputs, as shown in the truth table (Table 2.1). Latches are fundamental building blocks of a computing machine, and is omnipresent in computers and communication systems. So proposals of implementations of a latch, that are more efficient from the point of view of space or operational time, have far-reaching consequences.

Latches can be built around a pair of cross-coupled inverting elements, such as vacuum tubes, bipolar transistors, field effect transistors, inverters, and inverting logic gates. Specifically, for instance, conventional latches are constructed out of two cross coupled NAND or alternately NOR gates. Here, unlike traditional latches built by concatenating two logic elements, we will use only *one* element to implement

¹Results have been published in [42]

the latch truth table. Our proposal does not require cross-coupling the logic gates, nor does it involve many clock cycles. So the direct realization of the latch here has the potential to save both space and time costs.

In the next sections, we shall demonstrate how the Set-Reset latch operation can be obtained consistently in an optimal window of noise i.e. when the noisy bistable system is fed with a low amplitude input signal, consisting of two aperiodic pulses encoding two logic inputs, the output consistently mirrors a latch output (as displayed in Table 2.1). We also show how one can use a bias to get different types of responses from the same system, thereby obtaining an element that is easily *reconfigurable* to yield, not only gates, but a memory device as well. That is, in an optimal range of noise, by varying the bias, the *same* system will yield logic functions like AND, OR etc. as well as give latch operations directly.

2.2 Theoretical framework

Consider the general nonlinear system,

$$\dot{x} = F(x) + b + I_{in} + D\eta(t) \quad (2.1)$$

where $F(x)$ is a generic nonlinear function representing the force field of a potential with two distinct stable wells. I_{in} is the input signal which encodes the logic inputs, b is bias to asymmetrize the two potential wells, and $\eta(t)$ is an additive zero-mean Gaussian noise with unit variance, with D being the amplitude(intensity) of the noise.

A logical input-output correspondence is obtained by driving the system with two trains of aperiodic square pulses: $I_1 + I_2$, encoding the two logic inputs. For logic operations such as OR/NOR and AND/NAND, we consider the inputs to take value I when the logic input is 1, and value $-I$ when the logic input is 0, where input strength I is: $0 < I < 1$. Since, the binary logic inputs can be either 0 or 1, they produce 4 sets of binary input: $(0, 0)$, $(0, 1)$, $(1, 0)$, $(1, 1)$. These four input conditions give rise to three distinct values of I_{in} . Hence, the input signal I_{in} generated, is a 3-level

aperiodic wave form.

The state of this system, is interpreted as logic output 1 when $x > x^*$ and logic output 0 when $x < x^*$, where x^* is roughly given by the position of the barrier between the two wells. Such an interpretation allows one to consistently obtain logical responses, such as OR and AND, when noise intensity D is in an optimal band. Complementary gates, NOR and NAND, can also be obtained in a straight-forward manner, by the alternate output determination : $x < x^*$ corresponding to logic output 1, and 0 otherwise.

Now, to use this element as a Set-Reset latch, we need to modify the encoding of input values, so that we can distinguish between $(0, 1)$ and $(1, 0)$ states, as the latch truth table is *asymmetric* with respect to inputs unlike the usual logic gates. A simple way to accomplish this is to have the following asymmetric input encoding: the first input I_1 takes the value $-I$ when the logic input is 0 and I when the logic input is 1, while the second input I_2 takes the value I when the logic input is 0 and $-I$ when the logic input is 1, where $0 < I < 1$.

Equivalently, instead of the asymmetric input association described above, we can consider symmetric input associations (as in the logic operations), and apply a NOT operation to the second input I_2 . This will also yield the same physical input signal I_{in} . Namely, corresponding to the 4 sets of binary inputs (I_1, I_2) : $(0, 0)$, $(0, 1)$, $(1, 0)$, $(1, 1)$, the input signal I_{in} takes the values 0, -1 , 1, and 0 respectively. Out of these four sets, the input corresponding to $(1, 1)$ is a restricted set and does not occur in the truth table. So we are left with three input sets, each one giving rise to a *distinct* value of I_{in} . Hence the input signal I_{in} generated, is again a 3-level aperiodic wave form. The other way is to implement a latch with different input-output correspondence. The truth table of such a latch is shown in Table 2.2. We call it a *Stochastic Resonance Latch* and this latch can be implemented with same input encoding as for the logic gates.

Logic response from output can be obtained, as in logic operations, by defining a threshold value x^* . If $x > x^*$, i.e., when the system is in the potential well x_+ , then the logic output is taken to be 1, and 0, if $x < x^*$ and the system is in other well. Thus, the logic output toggles as the state of the system switches from one well to another.

Set (I_1)	Reset (I_2)	Latch
0	0	No change(maintain the previous state)
0	1	0
1	0	1
1	1	Restricted Set

Table 2.1: Relationship between the two inputs and the output of Set-Reset latch.

I_1	I_2	Latch
0	0	0
0	1	No change(maintain the previous state)
1	0	No change(maintain the previous state)
1	1	1

Table 2.2: Relationship between the two inputs and the output of a Stochastic Resonance latch.

2.3 Numerical simulations

We now demonstrate latch functionality, using numerical simulation of a simple non-linear system:

$$\dot{x} = 2x - 2x^3 + b + I_{in} + D\eta(t) \quad (2.2)$$

where D is amplitude of the Gaussian noise, b is asymmetrizing bias and the potential energy function is bistable (see Fig. 2.1). The input signal, $I_{in} = I_1 + I_2$, where I_1 and I_2 encode the two logic inputs, with the encoding associations for the logic operations and the set-reset latch being different. The bias b , for different operations, is set as displayed in Table 2.3.

Operation	Bias
Set-Reset Latch	0
AND/NAND	-0.5
OR/NOR	0.5

Table 2.3: Representative values of the asymmetrizing bias b in Eqn. 2 that yields the Set-Reset latch operation, OR/NOR logic operation and AND/NAND logic operation. Here $I = 0.5$.

Also note that the nonlinear function above, is efficiently realized by a linear resistor, linear capacitor, and a small number of CMOS transistors [33]. Further, it is capable of operating in very high frequency regimes, and such a system may be implemented with integrated circuits and nanoelectronic devices. Other forms of the nonlinear function $F(x)$ in Eqn. 1 may be realized in optical [35, 43, 36], nanomechanical [34], chemical [37] and biological systems [38, 38].

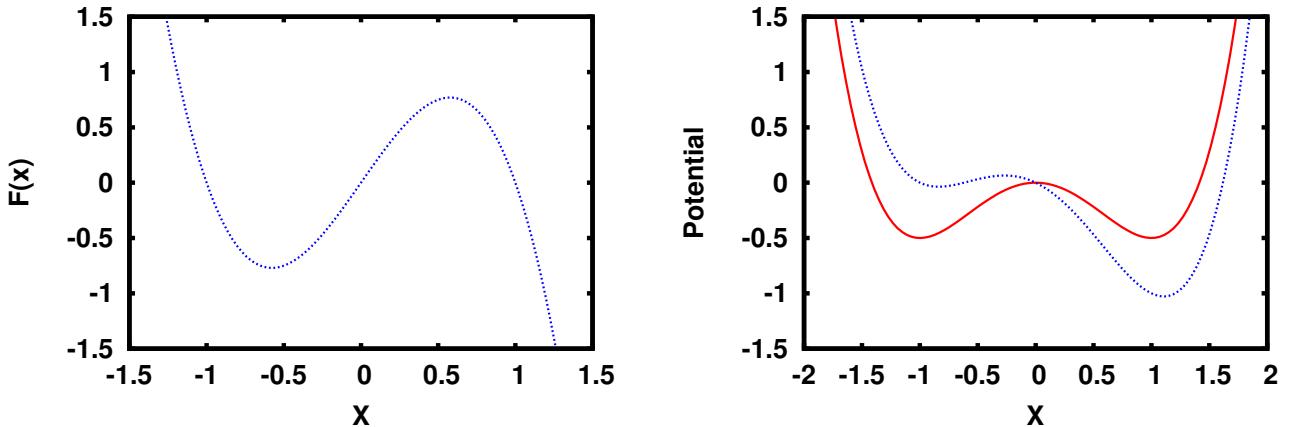


Figure 2.1: For the system described by Eqn.2: (left) the function $F(x) = 2x - 2x^3$ with $b = 0$ and (right) the effective potential obtained by integrating the function $F(x)$ in Eqn.2, with bias $b = 0$ (red solid line) and $b = -0.5$ (dashed blue line).

Input pulses are given to the system in such a way that *all* possible combination of transitions are presented to the system, in *random sequence* (see the top 3 panels of Fig.2.2). The threshold for output determination, x^* , is 0 here. So to obtain the desired logic response, we interpret the state $x > 0$ as logic output 1 and $x < 0$ as the logic output 0. It is clearly evident from Fig. 2.2, that for moderate noise the system consistently yields the Set-Reset latch input-output association, while it fails to do so for very small noise and large noise.

Note that the system holds its output steady, while the input signal is held constant, over long times ($\sim 10^3$ in our simulations). Namely, the system manages to maintain its state, which is in a local equilibrium of the potential, for reasonably small noise intensity D and large barrier height ΔV . This is because the Kramer's rate for escaping from the potential well (i.e., the inverse of the average switching rate induced by noise alone), given by $\sim \exp(-\Delta V/D)$, is very small here. So the system does not switch wells under the influence of noise alone. Rather it needs both signal and noise to effect a change. However, it is evident (for instance from Fig. 2.2) that

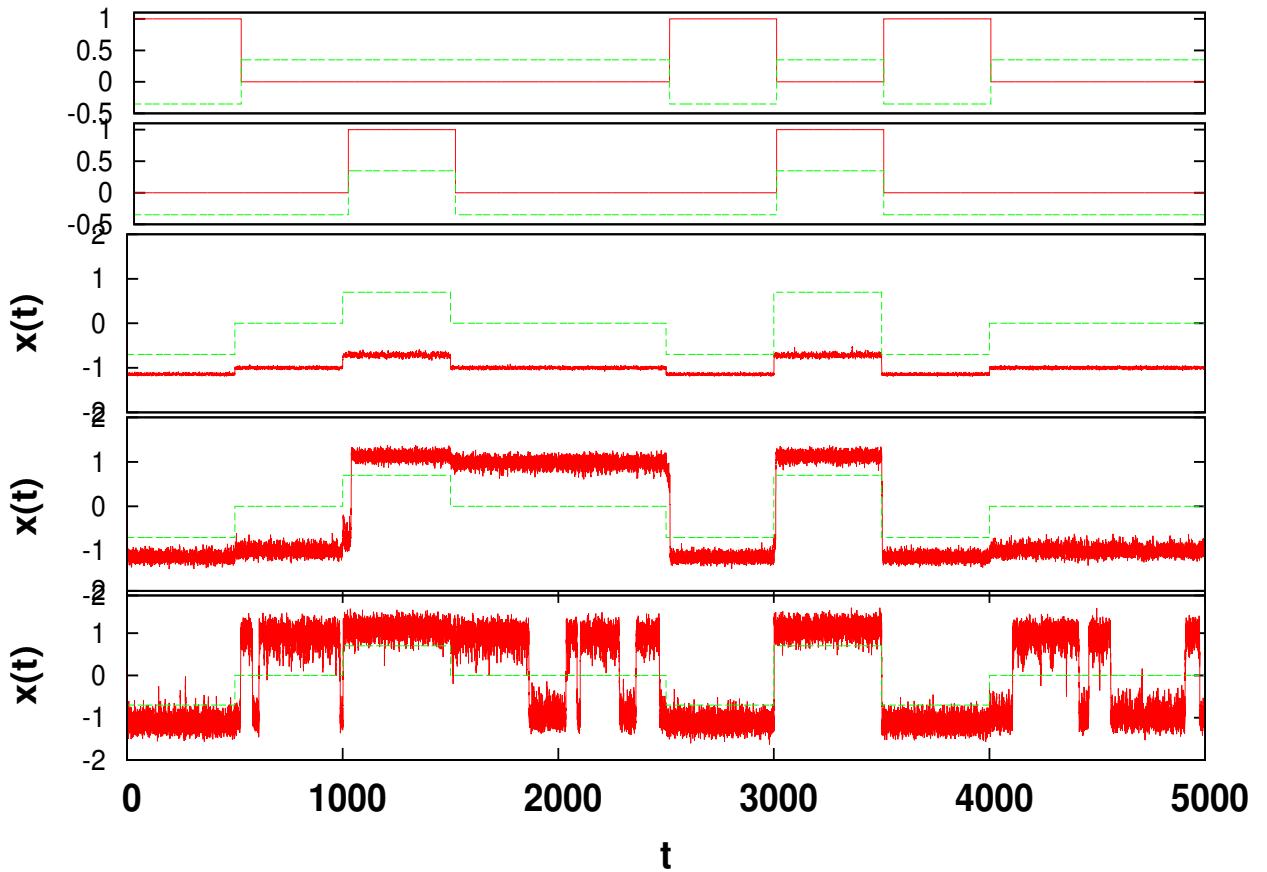


Figure 2.2: Panels 1 and 2 show streams of the two inputs. The input strength is 0.35. The logical value of the input is shown as a solid red line and the actual value as a dashed green line. For I_1 we have -0.35 when logic input is 0 and 0.35 when logic input is 1. For I_2 we have 0.35 when logic input is 0 and -0.35 when logic input is 1. Panels 3-5 show the outputs $x(t)$ corresponding to $D = 0.05$, $D = 0.25$, $D = 0.5$. Here bias $b = 0$, and the input signal $I_{in} = I_1 + I_2$ is indicated by the green line. Clearly, we get the desired output only when noise is within some optimal range (in this case panel 4 i.e. $D = 0.25$)

as noise increases, the probability of random noise-induced well hopping increases, leading to loss of robustness for noise levels beyond the optimal window.

We can quantify the consistency (or reliability) of obtaining a given logic output by calculating the probability of obtaining the desired logic output for different sets of inputs, namely the ratio of successful runs where the desired logic output is obtained (after transience), to the total number of runs.

The system was simulated by keeping the value of one input set constant over 1000 time units, and we simulated the system over a sequence of 500 such sets. Unless

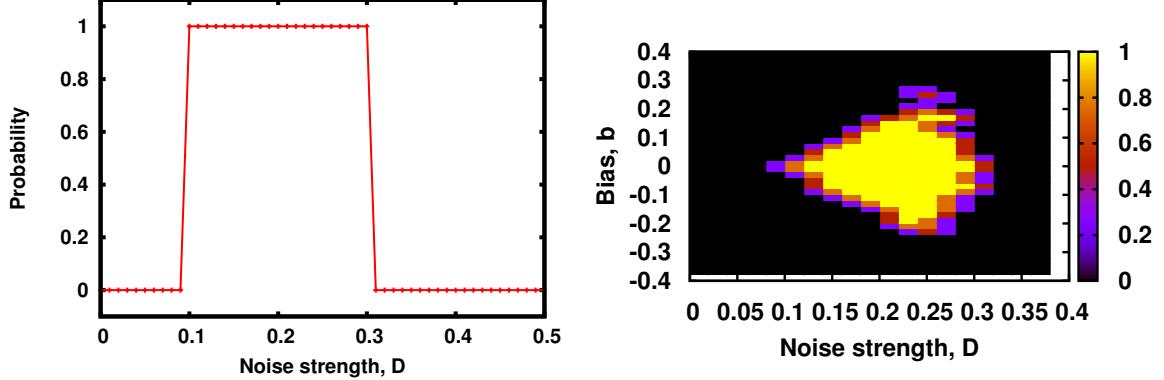


Figure 2.3: Probability for obtaining the Set-Reset latch operation for different values of noise strength, with bias $b = 0$ (left). Right panel shows the region for different bias (y axis) and noise strength (x axis). Evidently we get the Set-Reset latch operation only within an optimal window of noise strength.

otherwise stated, we allow a latency of 100 in the calculation of $P(logic)$. The values of inputs I_1 and I_2 were chosen to be randomly distributed so that $I_{in} = I_1 + I_2$ switched levels in an uncorrelated aperiodic manner. Thus the probability is one only if we get the desired response for all the 500 input sets.

It is evident from Fig. 2.3 that we obtain consistent memory operation in an optimal window of noise. So the system behaves as a Set-Reset latch even for *sub-threshold input signals*, utilizing noise to store the information. This can lead to development of low power consuming memory devices. Further, one can manipulate the potential function to obtain robust operation in any given noise window (see Fig. 2.4)

We also observed *reduction in latency* with increasing noise. This is evident in Fig. 2.5. Clearly, the system responds faster to inputs when noise intensity is higher. That is, the desired hopping between wells happens more rapidly under the influence of stronger noise. This is yet another feature where noise aids performance (see Fig. 2.6).

Further, it is evident from Fig. 2.7 that this system can also yield the logic response of a AND/NAND gate and a OR/NOR gate, by changing the bias b in Eqn. 2. This suggests that within an optimal window of noise strength, we can morph the circuit to act either as a logic gate or as a memory device, by simply adjusting the value of bias, i.e., one can easily switch from Set-Reset latch operation to AND/NAND or

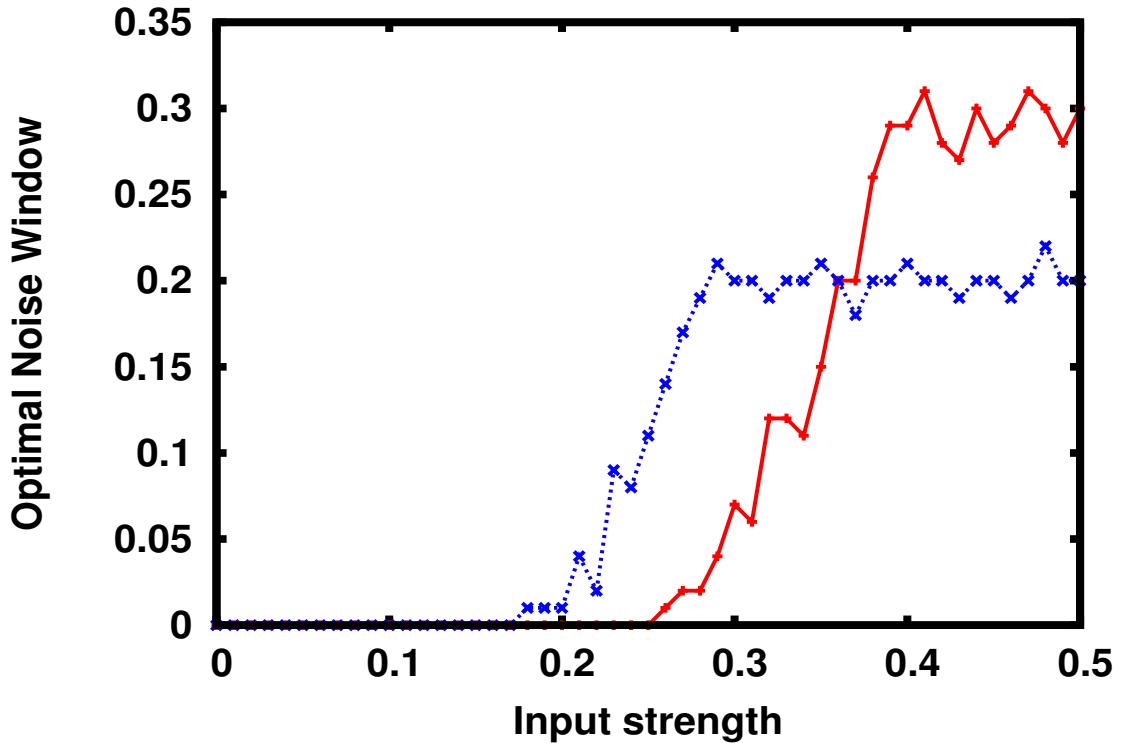


Figure 2.4: Size of the noise window of optimal Set-Reset latch operation for non-linear function $F(x) = 2x - 2x^3$ (red) and $F(x) = 2x - 4x^3$ (blue), for different values of input signal.

OR/NOR logic operation (see Table 2.3). This is made possible by the change in the symmetry and depths of the potential wells with change of bias b .

Note that the noise region of optimal operation depends on the form of the non-linear function $F(x)$ in Eqn. 1, as well as on the input signal strength, as displayed in Figs. 2.8. In order to obtain an overlapping window of optimal noise strength for the different operations, one can adjust the input strength appropriately or choose a nonlinear function that yields the desired operational window for the given noise floor.

2.4 Discussion

We have explicitly shown that a nonlinear system functioning in a noisy environment, can produce a completely consistent Set-Reset latch operation on two inputs, streaming in any random sequence. We observed that for very small or very large

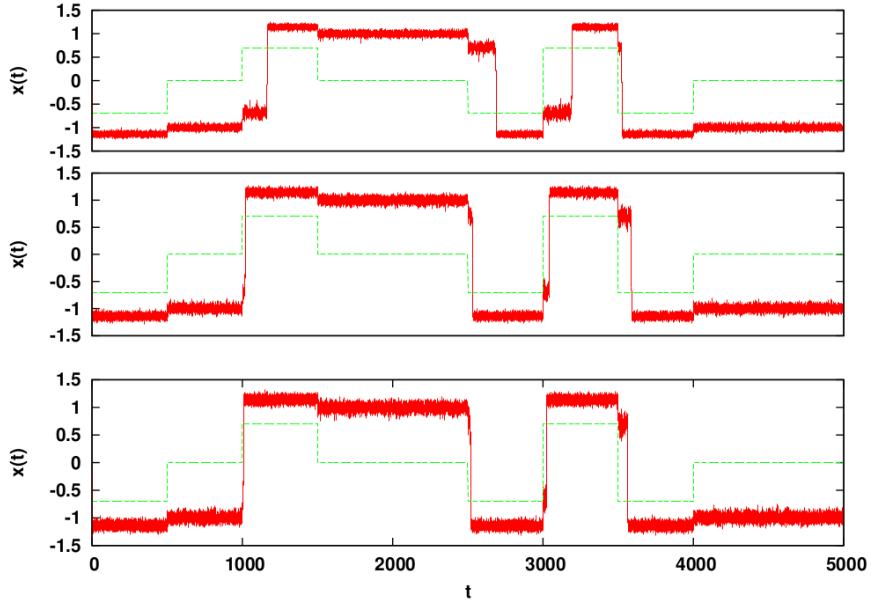


Figure 2.5: Panels 1-3 display the output $x(t)$ corresponding to $D = 0.10$, $D = 0.12$ and $D = 0.15$ (from top to bottom). The stream of inputs $I_{in} = I_1 + I_2$, with $I = 0.35$, is indicated by the green line in the figures. Clearly panel 3 has the shortest transients after input switches.

noise strengths the system does not yield a reliable output. However, in a reasonably wide band of moderate noise strength, the system produces the desired output very consistently. Furthermore, the response of the system could be easily switched from memory to logic operations by varying the bias in the system. Lastly, it was observed that noise reduced latency in the response of the system.

So it is evident that "LSR Elements" can reliably function as memory devices even for sub-threshold signals, thus consuming very low power. Further, the same elements can be used to produce outputs corresponding to, not only latches, but logic gates as well. Thus these "LSR Elements" can potentially act as building blocks of futuristic "Smart Computing Devices".

Potentially, such devices will not only operate robustly in noisy environments, but will also be capable of optimal utilization of their resources by configuring their "LSR Elements" into latches, or any of the logic gates, depending on the requirements of the task being performed. For example, if we are performing tasks requiring more computational power like running a program, then these computing devices will

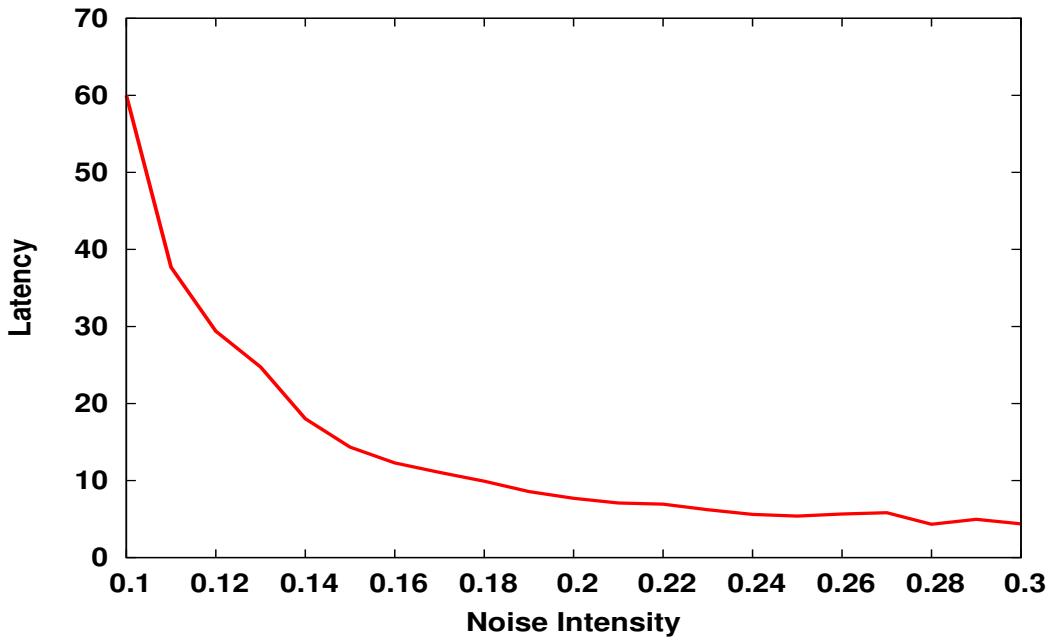


Figure 2.6: Latency (averaged over a random stream of inputs) as a function of noise strength. Here latency has been defined as the time taken to reach the barrier from a well, upon change in the input necessitating a change in the output.

morph most of the LSR elements to logic gates, whereas in case of tasks requiring memory like plotting large values of data, LSR elements will be morphed into memory enabling efficient use of resources. Furthermore, it is conceivable that devices based on such elements can potentially help in reducing boot times thus achieving what is commonly called ``instant boot''. This can be accomplished by morphing large number of LSR elements into memory at the time of shut down and start up. This significant increase in memory will enable us to keep most of the data required for the applications readily accessible, paving way for faster boot times.

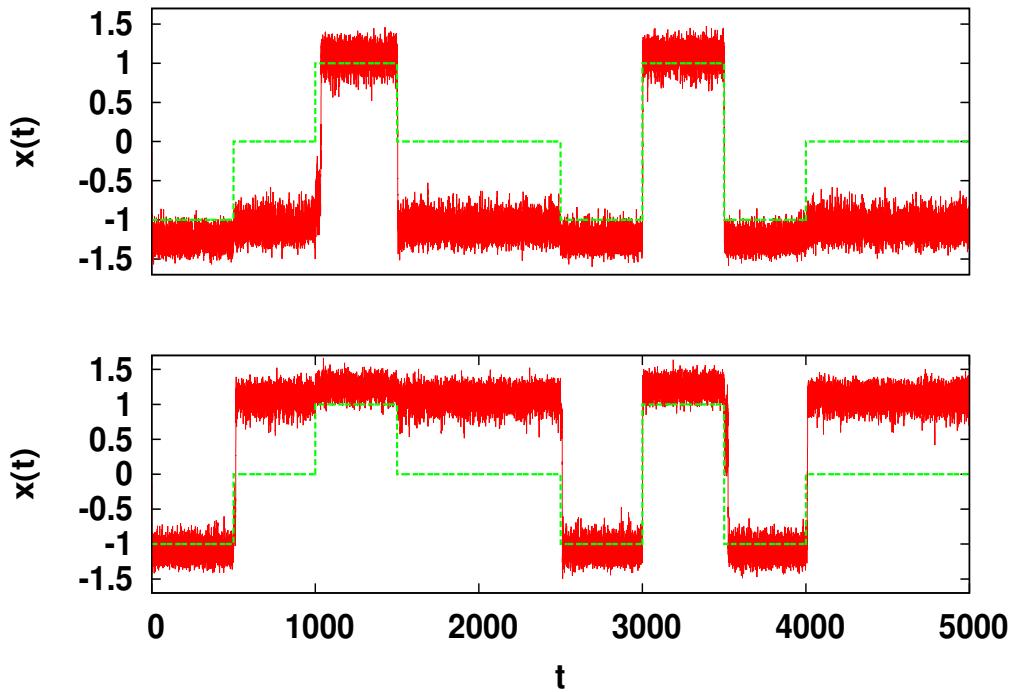


Figure 2.7: Panels showing output $x(t)$ corresponding to bias $b = -0.5$ (top panel) and $b = 0.5$ (bottom panel), with the green line indicating the input signal $I_{in} = I_1 + I_2$. Clearly, by adjusting the bias value we obtain logic output corresponding to AND gate (top) and OR gate (bottom). Here $I = 0.5$ and $D = 0.38$.

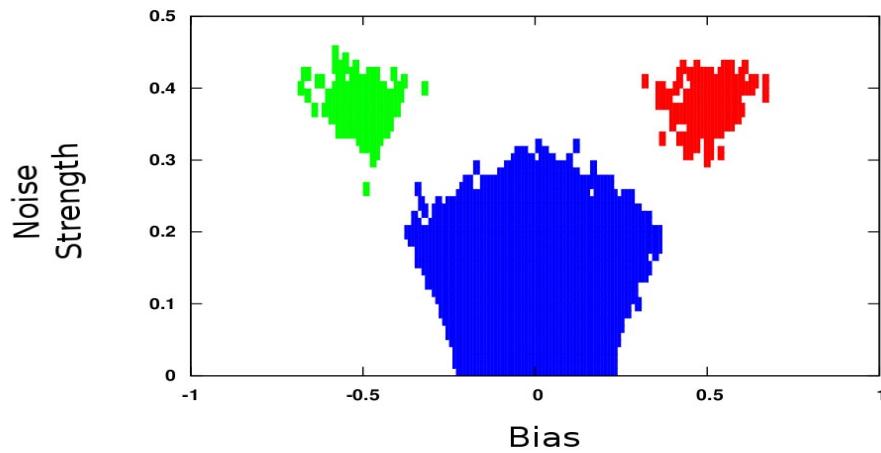


Figure 2.8: Points marking the region where the Set-Reset latch operation (blue), OR/NOR logic (red) and AND/NAND logic (green) are obtained with probability 1, for nonlinear function $F(x) = 2x - 2x^3$ with input signal strength 0.5 for different values of bias (x axis) and noise strength (y axis).

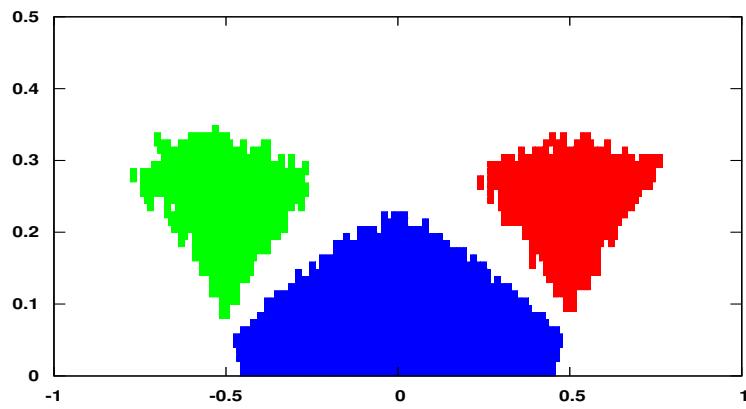


Figure 2.9: Points marking the region where the Set-Reset latch operation (blue), OR/NOR logic (red) and AND/NAND logic (green) are obtained with probability 1, for nonlinear function $F(x) = 2x - 4x^3$ (right), with 0.75 for different values of bias (x axis) and noise strength (y axis).

Chapter 3

Logical stochastic resonance in noiseless environment

3.1 Introduction

In this chapter we examine the possibility of LSR in noiseless environment by driving a two-state system with periodic forcing instead of random noise. The central question is this: if the driving is completely regular, such as sinusoidal forcing, or a periodic train of pulses, would we still observe LSR? Namely, is noise a necessary ingredient of LSR?

Here we will demonstrate how LSR is indeed possible in a noiseless environment, i.e. we will show that when a nonlinear bistable system is presented a low amplitude input signal, consisting of (aperiodic) pulses encoding logic inputs, accompanied with periodic forcing, the state of the system accurately and consistently mirrors the output of a logic gate. We also show how one can reconfigure the type of logic response obtained by variation of a readily adjustable bias¹.

¹Results of this chapter have been published in [44]

3.2 LSR in noiseless environment

First we lay out the general principle of LSR when there is no or negligible noise in the environment. Consider a nonlinear system under periodic forcing:

$$\dot{x} = F(x) + b + I + Df(\omega t) \quad (3.1)$$

where $F(x)$ is a generic nonlinear function obtained via the negative gradient of a potential with two distinct stable energy wells at x_+ and x_- . The bias b has the effect of asymmetrizing the two potential wells. I is the low amplitude input, typically aperiodic, signal. The functional form of the periodic forcing is f , with ω being the frequency and D being the amplitude (intensity) of the forcing.

As before, a logical input-output association (cf. Table 1.1) can be obtained by feeding the system with an input signal $I = I_1 + I_2$, where I_1 and I_2 are two (aperiodic) trains of square pulses encoding the two logic inputs. Without loss of generality, consider the inputs to take value 0.5 when the logic input is 1, and value -0.5 when the logic input is 0. The logic inputs being 0 or 1, produce 4 sets of binary inputs (I_1, I_2) : $(0, 0)$, $(0, 1)$, $(1, 0)$, $(1, 1)$. These four distinct input conditions give rise to three distinct values of I . Hence, the input signal $I = I_1 + I_2$, is a 3-level aperiodic wave form.

The *logic output* is determined by the state x , and can be defined by a threshold value x^* , obtained from the position of the barrier between the two potential wells. If $x > x^*$, i.e., when the system is around the potential well x_+ , then logic output is 1. The logic output is 0 if $x < x^*$, i.e. when the system is in the other well. Thus the output toggles as the state of the system switches between wells.

3.3 Numerical Simulation Results

We now explicitly demonstrate LSR in noiseless environment, by utilizing a sinusoidal forcing, for a system with cubic nonlinearity:

$$\dot{x} = 2x - 4x^3 + b + I_1 + I_2 + r(t) \quad (3.2)$$

where $r(t) = D \sin(\omega t)$.

For this system the threshold value x^* , defining the output, is 0. So, we interpret the state $x > 0$ as logic output 1 and $x < 0$ as the logic output 0. Alternately, complementary gates can be obtained by interpreting the output as 1 when $x < 0$, and as 0 when $x > 0$.

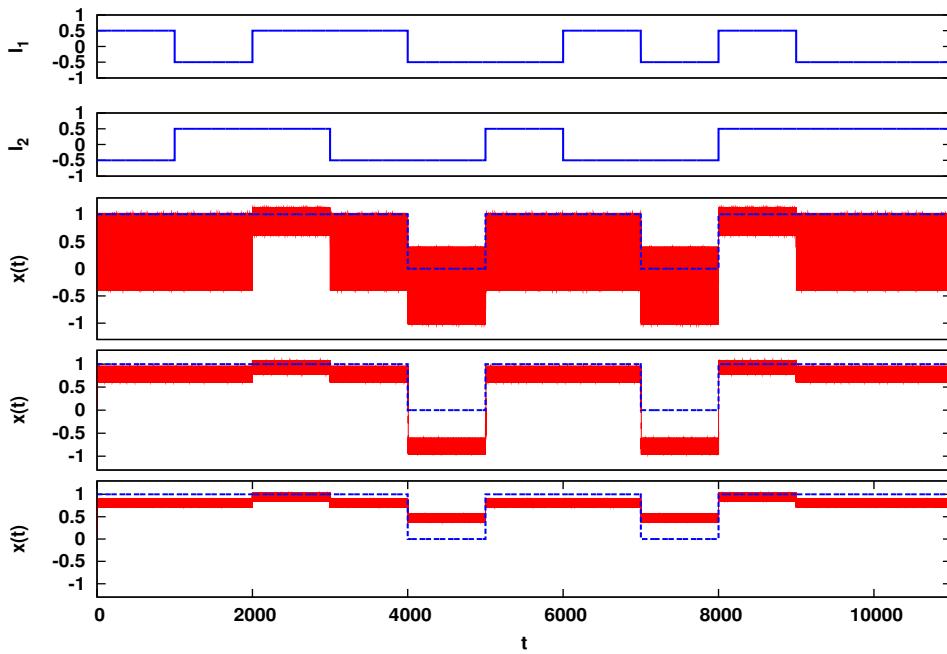


Figure 3.1: Panels top to bottom show (a) streams of inputs I_1 and (b) I_2 (which take value -0.5 when logic input is 0 and value 0.5 when logic input is 1), and output $x(t)$ for forcing frequencies (cf. Eq. 3.2): (c) $\omega = 2$, (d) $\omega = 10$ and (e) $\omega = 20$. Here, $b = 0.5$ and $D = 2$. The dashed blue line in panels (c-e) indicates the expected OR logic output (with state $x > 0$ being logic output 1, and $x < 0$ being logic output 0). Clearly, only when $\omega = 10$, we get the desired OR gate consistently.

3.4 Results

The response of the system under different angular frequencies of sinusoidal forcing is displayed in Fig.3.1. Interestingly we observe, that in order to produce a robust logical combination of the inputs, the system requires an appropriate forcing frequency, which is neither too small nor too large. Namely, for a given value of bias b and amplitude of forcing D , we get the desired logical output *only for some suitable range of ω* .

Note that by simply changing the bias we can easily switch to another logic operation. In this case, when bias b is changed from 0.5 to -0.5 , we morph from OR logic to AND logic. This is clearly evident from the timing sequences displayed in Fig.3.2. This effect arises from the change in the symmetry and depths of the potential wells due to changing b . The complementary logic gates, namely NOR and NAND, can be straight-forwardly obtained by the alternate output interpretation.

We can quantify the consistency of obtaining a given logic output as follows: first we calculate the probability of obtaining the desired logic output for different sets of input, i.e. the ratio of the number of successful runs (namely a run where the desired logic output is obtained) to the total number of runs. We then define a very stringent measure P reflecting the reliability of the system as a logic gate: when the probability defined above is ~ 1 (i.e. when the logic operation is correctly obtained for all given input sets) we take P to be 1, and 0 otherwise. Namely, partial success, where certain combinations of inputs fail to give the correct logic output, leads to $P = 0$, since we want the logic response to be obtained for *all* random combinations of inputs. From the point of view of applications, anything less is not useful, and our measure of successful gate operation P reflects this stringent requirement.

Fig.3.3 shows the variation of P for logic operations AND and OR with respect to drive frequency. It is clearly evident that we obtain a window of angular frequency for which our system consistently gives the desired logic response as output, i.e. for $\omega_{low} < \omega < \omega_{high}$ the system yields perfect gate operations. Forcing at angular frequencies lower than ω_{low} acts like a quasi-static ``signal'', akin to a bias, as the timescale of the drive is too slow and does not vary much vis-a-vis the natural timescale of the system. Frequencies larger than ω_{high} do not achieve the desired

response, as the drive then varies so fast that the system effectively responds to an averaged force field. Variation of optimal window of sinusoidal frequency and noise strength for various input strengths is shown in Fig. 3.4. We see that as we increase the input strength, the size of optimal window increases and saturates afterwards. Further, we observe in Fig.3.5 that by increasing the amplitude of sinusoidal forcing (D) the optimal window we get for ω , widens and shifts to the higher end. Namely, the lower and upper thresholds of optimal angular frequency (ω_{low} and ω_{high}) increases for increased value of D .

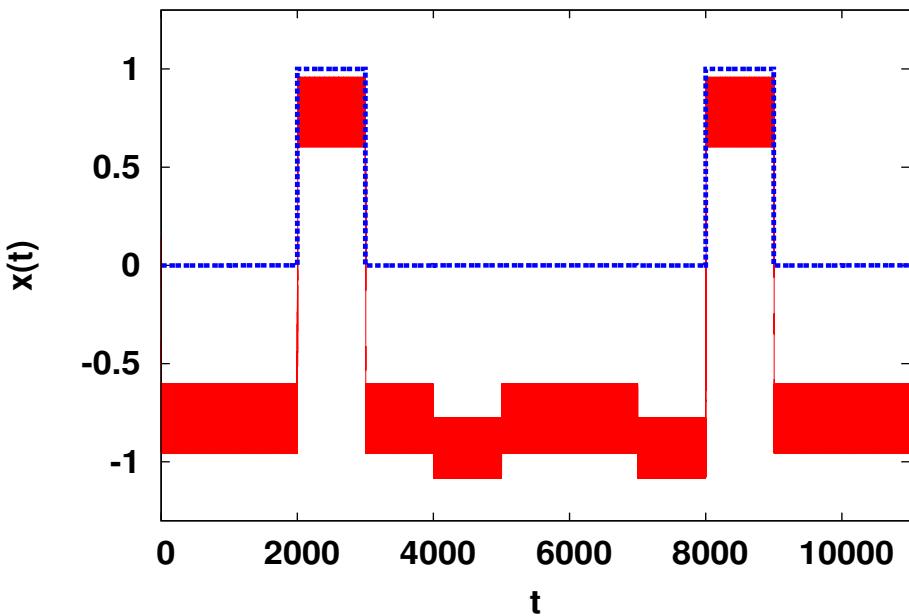


Figure 3.2: Waveform of $x(t)$ (cf. Eq. 3.2) with angular frequency $\omega = 10$, $b = -0.5$ and $D = 2$. The bold blue line indicates the expected AND logic output. By changing bias b from 0.5 to -0.5 , we were able to switch from OR (cf. Fig.3.1) to AND gate.

In order to demonstrate the generality of our results, we now drive the system with a periodic rectangular waveform, and show that this too allows us to obtain a LSR like response. So consider the system in Eq.2 above, now forced with a rectangular wave, where $r(t)$ switches periodically between the values 1 and -1 , with time period $T = 2\pi/\omega$, where ω is the angular frequency, D is amplitude of rectangular pulse, and b is the asymmetrizing bias. In this system too, we observe that reliable logic output is obtained for intermediate frequencies.

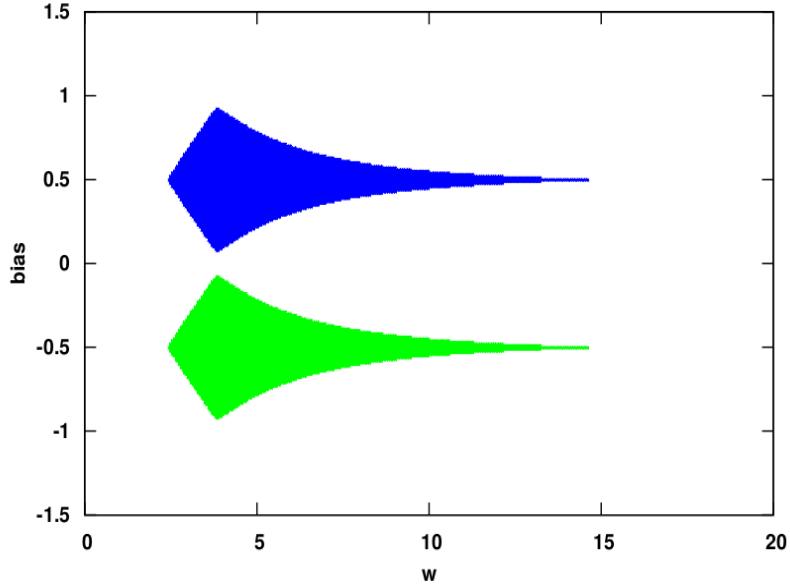


Figure 3.3: The shaded areas indicate where the probability P of obtaining the OR (top blue) and AND (bottom green) logic operation is 1, as functions of angular frequency (x -axis) and bias (y -axis). In both the cases, $D = 2$.

Further it is evident from Fig. 3.5 that driving with rectangular pulses is more efficient, as the system can function as a logic gate for lower amplitudes D , as well as over larger ranges of forcing frequencies for fixed D . We also investigated the logic response under increasingly low input strengths. We found that rectangular forcing allows logic behaviour for lower input strengths than sinusoidal forcing, again demonstrating the efficiency of driving with rectangular waveforms.

In the examples above, we have thus shown that noise is not a necessary condition to obtain a consistent logic response. It is possible to have phenomena completely analogous to LSR, without noise. So the forcing that induces the desired hopping in response to inputs does not have to be random noise, but can be a sine wave or even a cyclic set of pulses. The system needs only appropriate pushes sufficiently often, in order to change its state to the desired well. The timescale of the forcing is crucial, while its form can range from noise to sinusoidal forcing or rectangular pulses.

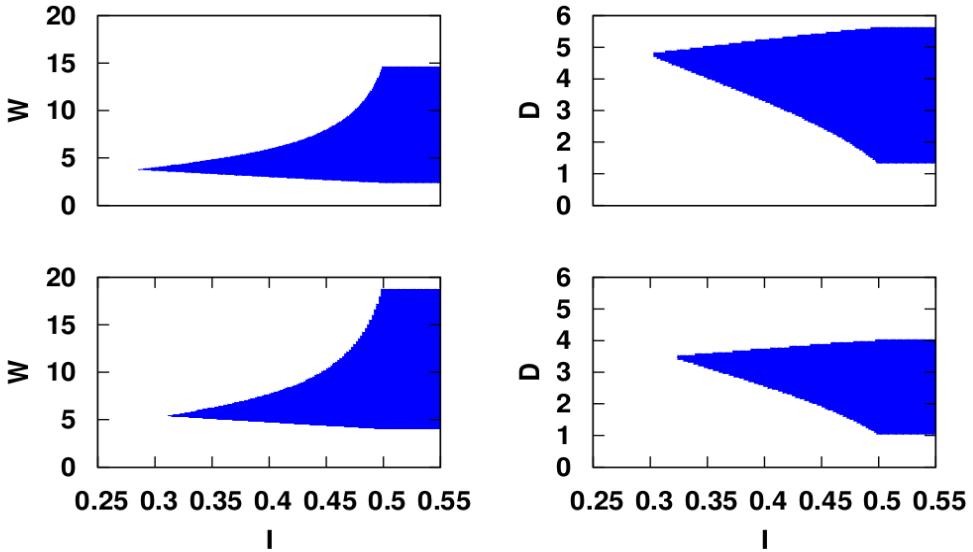


Figure 3.4: The shaded areas indicate where the probability P of obtaining the logic operation is 1, as functions of angular frequency (left) and noise intensity (right) with input strength for fixed noise intensity D (left) and angular frequency ω (right)

An explanation for the optimal band of frequencies is obtained by examining the time taken by the system to cross over the barrier from the bottom of the wells under the input signal encoding the logic inputs $(0, 1)$ or $(1, 0)$, which is the most difficult and sensitive case to satisfy consistently. The inverse of this time is analogous to the Kramer's rate representing the characteristic escape rate from a stable state of a potential, and determines the band of forcing frequencies and amplitudes that allow robust logic response. Now, in order to obtain a consistent logic response, the system must simultaneously satisfy certain conditions. First, the driving frequency should be more than the frequency at which the stream of inputs switch. Secondly, for a fixed value of amplitude D , the following has to be ensured: when the input signal encodes the logic input set $(0, 1)$ or $(1, 0)$ (i.e. $I = I_1 + I_2 = 0$), the system should be in the appropriate well. For instance, for OR logic, under net zero input signal the system should be in the higher well. So it should be able to cross the barrier from the lower to the upper side. At the same time, the reverse crossing should not occur. These two conditions set the two limits on forcing frequency (see Fig. 3.6).

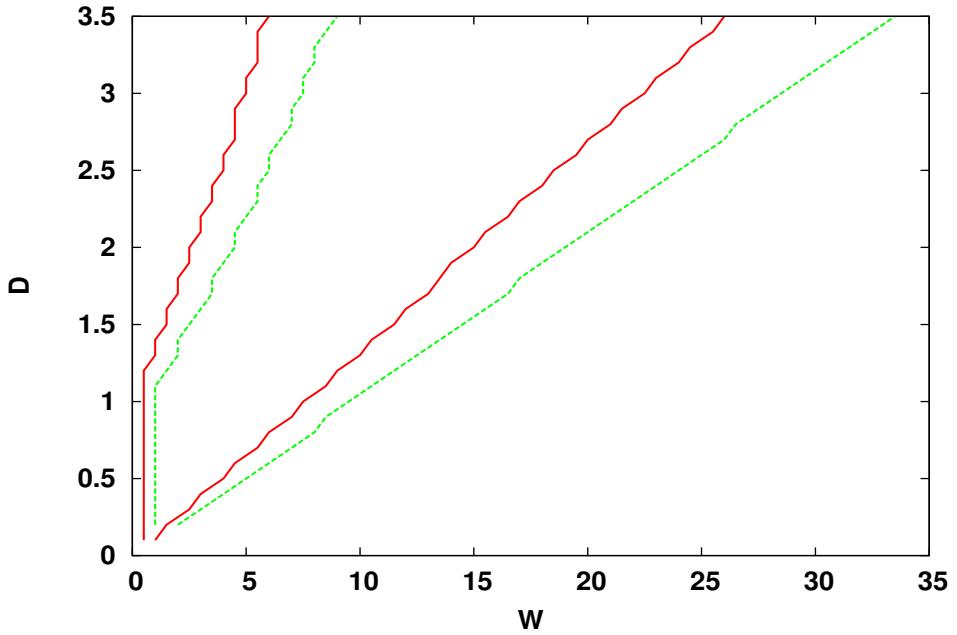


Figure 3.5: The curves indicate the limiting forcing frequencies ω_{low} and ω_{high} , for varying amplitude D , for sinusoidal forcing (red solid line) and rectangular forcing (green dashed line). Here $b = 0.5$ and the probability of obtaining the OR logic operation (leaving small transience after the switching of inputs) is 1 for the values of D and ω lying between the two lines, i.e. the lines mark the highest and lowest forcing frequencies yielding robust logic for different forcing amplitudes (and analogously the highest and lowest driving amplitudes for different frequencies).

Further, the forcing frequency should not be so high that system is unable to respond to it, i.e. the time for which the driving force pushes the system in the requisite direction should be more than the time that the system takes to shift from one well to other. The amount of time taken by the system to cross over to the desired well in response to a new input signal, namely the transience (which determines latency), should also be sufficiently high so that system has enough time to make the passage. Further, for very low frequency forcing, the system may have long transience as the transient period must include at least one full cycle of forcing.

Lastly, we present the realization of these results in electronic circuit experiments. In Fig.3.7, the analog simulation circuit for Eq.(2) is depicted. The input sinusoidal signal is denoted as $f(t)$. The amplitude of the sinusoidal signal is fixed at 2V and the frequency values range from 500 Hz to 30 KHz. $I(t)$ corresponds to logic input signal

$(I_1 + I_2)$, where the logic input signals I_1 and I_2 take value $-0.5V$ when logic input is 0 and value $0.5V$ when logic input is 1. The bias voltage V_c corresponds to bias b in Eq.(2). We set V_c equal to $0.5V$ and $-0.5V$ for the different logic operations. The output node voltage (V_O) of operational amplifier OA2 correspond to $x(t)$ of Eq.(2).

Representative results of circuit realizations of sinusoidal forcing are displayed in Fig.3.8. Comparison with Fig.3.1 clearly shows that the same phenomenon is observed in these experiments. Namely, only with sinusoidal forcing with moderate frequency, equal to 10 KHz, do we get the desired logic gate operation reliably.

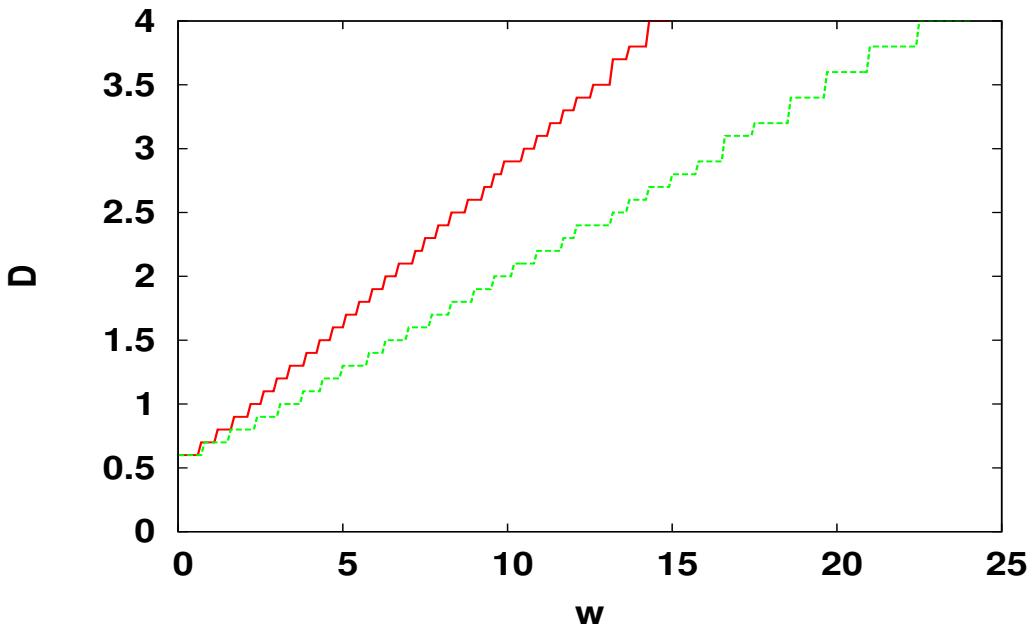


Figure 3.6: Lines indicating the limiting forcing frequencies for which the system crosses the barrier, when driven by a rectangular wave of amplitude D . Specifically for all frequencies ω and amplitudes D above the lines, the system crosses over with probability 1, within 100 time steps, from upper to lower well (solid red line), and from lower well to upper well (dashed green line). Here bias $b = 0.5$ (appropriate for OR logic) and input signal $I = 0$ (namely encoding logic input set $(1, 0)/(0, 1)$). The area inside these curves give the allowed forcing frequency and amplitude band, as it allows the crossing from the lower to the upper well, but not the reverse. These curves mirror the ones displayed in Fig.3.5.

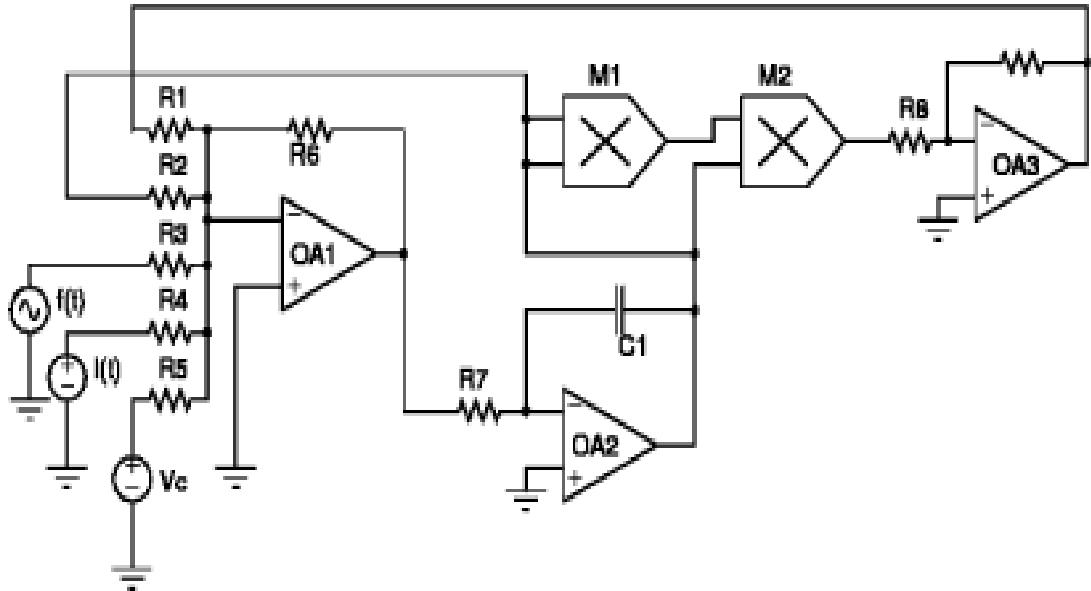


Figure 3.7: Circuit diagram: here OA1, OA2 and OA3 are operational amplifiers (AD712). M1 and M2 are analog multipliers(AD633). The resistor values are fixed as $R_1 = R_3 = R_4 = R_5 = R_6 = R_8 = 100 \text{ k}\Omega$. $R_2 = 50 \text{ K}\Omega$, $R_7 = 10 \text{ K}\Omega$, $R_9 = 400 \text{ k}\Omega$. The capacitor value is fixed as $C_1 = 0.01 \mu\text{F}$.

3.5 Conclusion

In summary, we have explicitly shown through numerics and circuit experiments, that it is possible to obtain a logic response exactly similar to LSR, without the presence of noise. Using only a periodically driven bistable system, we are able to produce a logical combination of two inputs streaming in any random sequence. For very small or very large forcing frequencies the system does not yield any consistent logic output, but in a wide band of moderate frequencies the system produces the desired logical output very reliably. Furthermore, the logic response of the system can be easily switched from one logic gate to another by varying the bias in the system. Thus it is evident that ‘‘Noise Free LSR’’ indeed exists, and noise is not a necessary ingredient to facilitate changes of state that reliably mirror logical outputs.

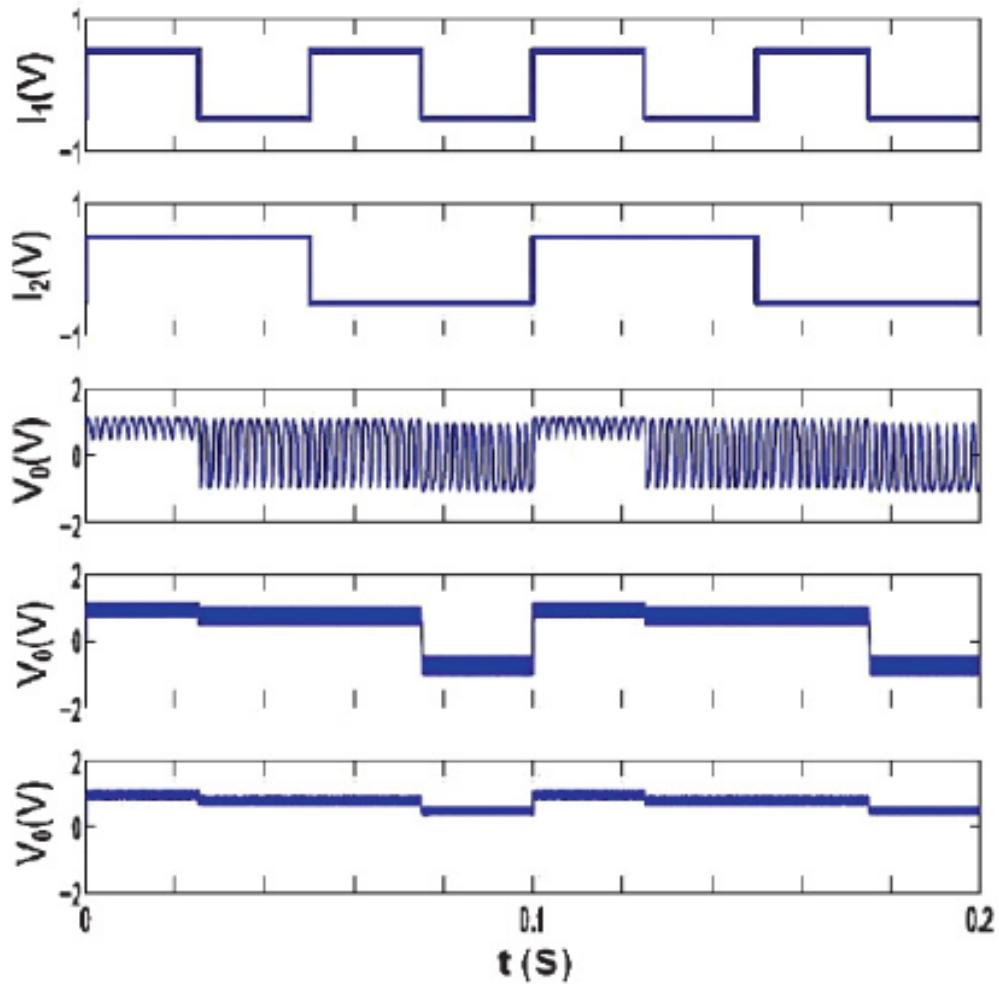


Figure 3.8: From top to bottom: panels a-b show streams of inputs I_1 and I_2 , which take value -0.5 when logic input is $0V$ and value $0.5V$ when logic input is 1 ; panels c-e show the waveforms of the output voltage, with angular frequencies: $\omega = 2$ KHz, $\omega = 10$ KHz and $\omega = 20$ KHz. Here, $b = 0.5V$, $D = 2V$. The bold blue line indicates the expected OR logic output. Clearly, only when $\omega = 10$ KHz, we get the desired OR gate consistently.

Chapter 4

Logical Stochastic Resonance in sub optimal noise

4.1 Introduction

In the previous chapters, the phenomena of *logical stochastic resonance* (LSR) was demonstrated: namely, when a bistable system is driven by two inputs it consistently yields a response mirroring a logic function of the two inputs in an optimal window of moderate noise. In chapter 2, it was shown that the same LSR elements can also be morphed into memory devices in a reasonably wide band of noise.

The noise in a system doesn't stay at the same level. Since LSR works in an optimal range, it is possible that the noise in the system is not sufficient to drive the system, i.e. the noise is below the minimum threshold of the optimal noise window. For instance, in case of thermal noise fluctuations in the environment such as ambient temperature, or certain internal processes, such as the work load of the device, may change the level of noise present in the system. So under weak load or in cold environments the system may not operate robustly.

In chapter 3, it was shown that dynamical behavior equivalent to LSR can be obtained in a *noise-free* bistable system, subjected only to periodic forcing, such as sinusoidal driving or rectangular pulse trains. This opens up the possibility of study-

ing the behavior of bistable elements subjected to both a periodic signal, as well as noise. In this chapter, we will demonstrate how periodic forcing and noise interact constructively, thereby allowing us to obtain consistent logic and memory operations over a *much larger noise window*. Thus, by adding a periodic signal to a noisy nonlinear system we can obtain LSR consistently even if noise level is lower than the minimum threshold required to obtain LSR. Further, we can use two coupled bistable systems in which the output of one bistable system controls the amplitude of the periodic forcing fed into the other system. This suggests a way in which to *adaptively adjust the strength of periodic forcing depending on the noise level present in the system*¹

4.2 Theoretical framework for LSR in sub optimal noise

Consider the general nonlinear dynamical system,

$$\dot{x} = F(x) + b + I + D\eta(t) + A f(\omega t) \quad (4.1)$$

where $F(x)$ is a generic non linear function obtained via the negative gradient of a potential with two distinct stable energy wells. I is the input signal which is the sum of two square pulses encoding the two logic inputs, b is bias to asymmetrize the two potential wells, $\eta(t)$ is an additive zero-mean Gaussian noise with unit variance and D is the amplitude(intensity) of noise. The functional form of the periodic forcing is f , with ω being the frequency and A being the amplitude of the forcing.

A logical input- output correspondence can be obtained by driving the system with two trains of aperiodic square pulses: $I = I_1 + I_2$, where I_1 and I_2 encode the two logic inputs. Logic output can be obtained from the state x by defining a threshold value x^* . If $x > x^*$, then the logic output is interpreted to be 1, and 0 otherwise.

¹Results of this chapter have been published in [45]

4.3 Numerical simulation results

We now explicitly demonstrate this phenomena in the system given by:

$$\dot{x} = a_1(x - a_2x^3) + b + I_1 + I_2 + A \sin(\omega t) + D\eta(t) \quad (4.2)$$

where D is the amplitude of noise, b the asymmetrizing bias and the functional form of periodic forcing is sinusoidal with A being the amplitude of the sinusoidal forcing. The parameters a_1 and a_2 control the height of the potential barrier and the location of potential minima. In absence of other terms, the height of potential barrier is $a_1/4a_2$ and the wells are at $\pm\sqrt{1/a_2}$ as shown in figure 4.1. Here we have taken $a_1 = 4$, and $a_2 = 5$. This function $F(x)$ is reasonably insensitive to noise and its two stable states are close to the encoded values of inputs. This helps to *cascade the gates, and feed the output directly as input, without any scaling factors.*

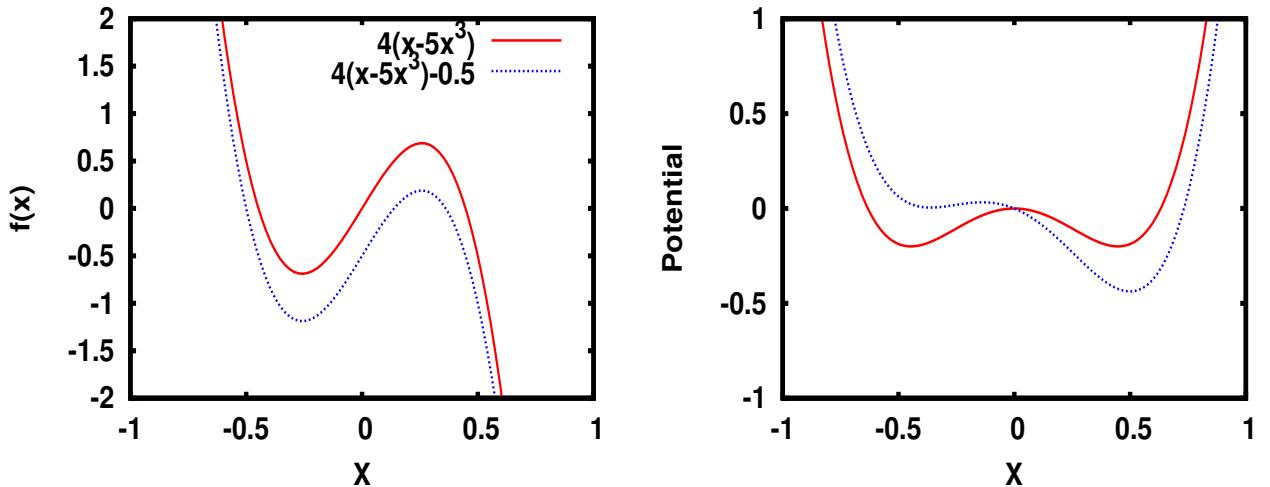


Figure 4.1: For the system (2): (left) the function $F(x)$ and (right) the effective potential obtained by integrating the function $F(x)$, for different bias: (a) $b = 0$ (red solid) and (b) $b = -0.5$ (blue dashed line).

The logic inputs are presented to the system with I_1 and I_2 switching levels in an uncorrelated aperiodic manner. The inputs being 0 or 1, produce 4 sets of binary inputs (I_1, I_2) : $(0, 0)$, $(0, 1)$, $(1, 0)$, $(1, 1)$. These four distinct input conditions gives rise to three distinct values of I . Without loss of generality, consider the inputs to take value 0.5 when the logic input is 1, and value -0.5 when the logic input is 0. Hence, the input signal I , generated is a 3-level aperiodic wave form.

We choose 0 as our output determination threshold. If $x > 0$, i.e., when the system is in the positive potential well, then the logic output is interpreted to be 1, and 0 otherwise. Thus the logic output toggles as the system switches wells.

We simulated the system in equation 4.2 for various possible frequencies and amplitude of the sinusoidal forcing and at various noise strengths. We used $b = -0.5$, so the system is biased to function as *AND* gate. We know that by changing the bias, we can easily switch to another logic operation. In this case, when bias is changed from -0.5 to 0.5 , we obtain the *OR* gate. When bias is reduced to zero, we get a memory device. This effect arises from change in the symmetry and depths of the potential wells due to changing b . For brevity, we will show the results only for the representative *AND* gate.

We observe that for low noise strengths the system doesn't give the correct logical response in absence of periodic forcing as expected. However, as we apply some periodic forcing, the system gives the desired response. Notice that this response is obtained through interplay of noise and periodic forcing, as in absence of any one of these the system does not yield the desired response. *Only when both are present simultaneously, do we get the requisite output*, as shown in figure 4.2.

So when the noise level is low, it is not sufficient to induce the desired switch from one well to the other. Similarly, for high frequency or low amplitude, the sinusoidal forcing cannot drive the required hopping. However, when both are present, they aid each other to give the appropriate switching. Thus at low noise, the periodic forcing helps the system to switch wells in the desired fashion, in response to the inputs.

We can quantify the consistency (or reliability) of obtaining a given logic output by calculating the probability of obtaining the desired logic output for different states of input. The probability, here, is the ratio of number of successful runs, i.e. when the desired logic output is obtained, to the total number of runs. In every run, we simulate the system for 7 different possible combinations of I_1 and I_2 such that we get all possible transitions of the inputs. Thus, any run is counted as successful only if the system is in the desired well for all seven possible combinations of the inputs, allowing for a small transience. Here we have chosen the transience time to be equal to 10 percent of the time for which an input is applied. Thus the system must remain in for 90 percent of the input time.

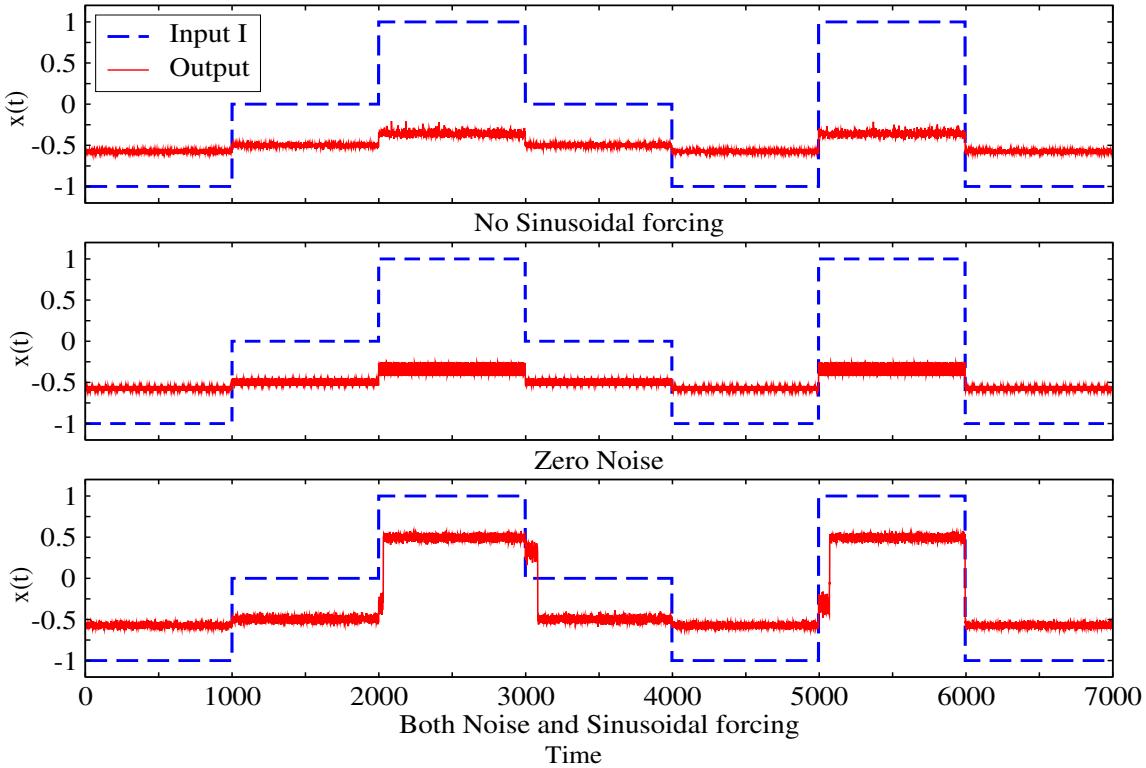


Figure 4.2: The panels show the waveforms of $x(t)$ obtained from simulating the system (2). In the top panel the amplitude of periodic forcing is zero and there is only noise in the system, with the noise intensity being below the minimum threshold required for LSR. In the middle panel the system is driven by periodic forcing only, and its amplitude and frequency are such that it alone can't drive the system to act as a robust logic gate. Only when there are both noise and periodic forcing, we get the desired AND gate (panel 3). The specific values of inputs used are $b = -0.5$, $D = 0.08$, $\omega = 4$ and $A = 0.5$. Dashed blue line shows the input I ($I_1 + I_2$) and red line shows $x(t)$.

Now we vary the noise strength and amplitude of periodic forcing keeping the frequency of the sinusoidal forcing constant. We observe that when the amplitude of sinusoidal forcing is low, we get the correct logical response only when there is some noise in the system. For very low or very high values of the noise intensity, we get erroneous results. For higher amplitudes of sinusoidal forcing, periodic forcing alone can drive the system to the desired well, even in absence of noise. Notice that as we keep on increasing the amplitude of sinusoidal forcing, the maximum noise intensity for which we obtain correct logical response decreases slightly. This is expected as the interplay of noise and periodic forcing is likely to worsen the response at higher values of noise strengths, as now the state of the output starts hopping randomly between the two wells as shown in figure 4.3.

Next we keep the amplitude of periodic forcing constant, and vary the frequency of the sine wave. We observe that for low frequencies we obtain the desired response for low noise levels and as the frequency is increased the optimal window reduces and slowly shifts upwards as seen in figure 4.4. One can rationalize this as follows: when the frequency is higher, the system gets little time to respond to the sinusoidal forcing, thus limiting its effect. This is also evident from the bottom panel of figure 4.4 which clearly shows that if the noise level is constant, then as the frequency of periodic forcing is increased, we need higher and higher values of its amplitude to get the desired response.

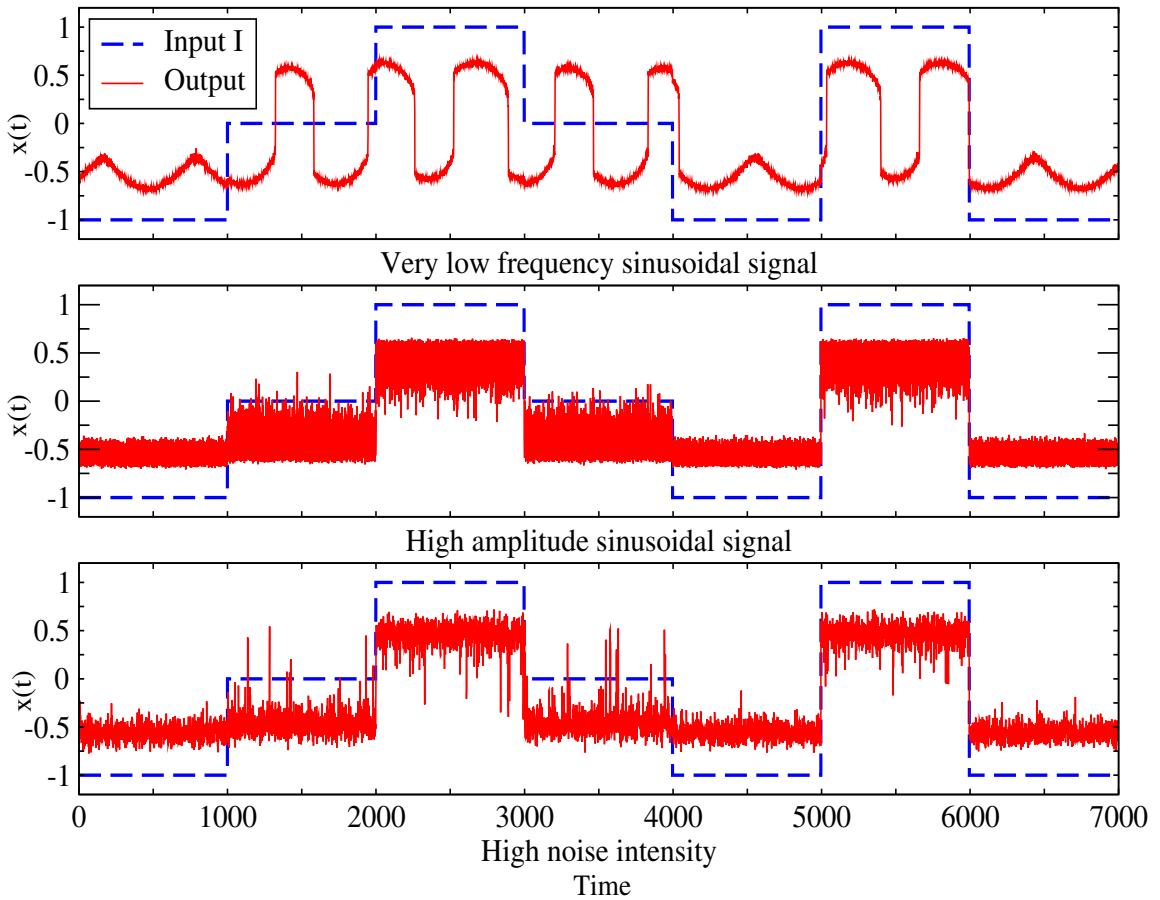


Figure 4.3: This figure shows how decreasing the frequency of periodic forcing to very low value $\omega = .01$ (top panel) or increasing the amplitude of periodic forcing to very high value $A = 2.0$ (middle panel) or very high noise intensity $D = 0.40$ can result in random hopping between the wells, leading to erratic response. Red line is the output of the system and dashed blue line is the sum of the two inputs that was fed into the system as defined in eq. 4.2.

Further, the addition of periodic forcing also results in lower switching times. We calculated the time the output takes to switch from low to high levels, or vice versa,

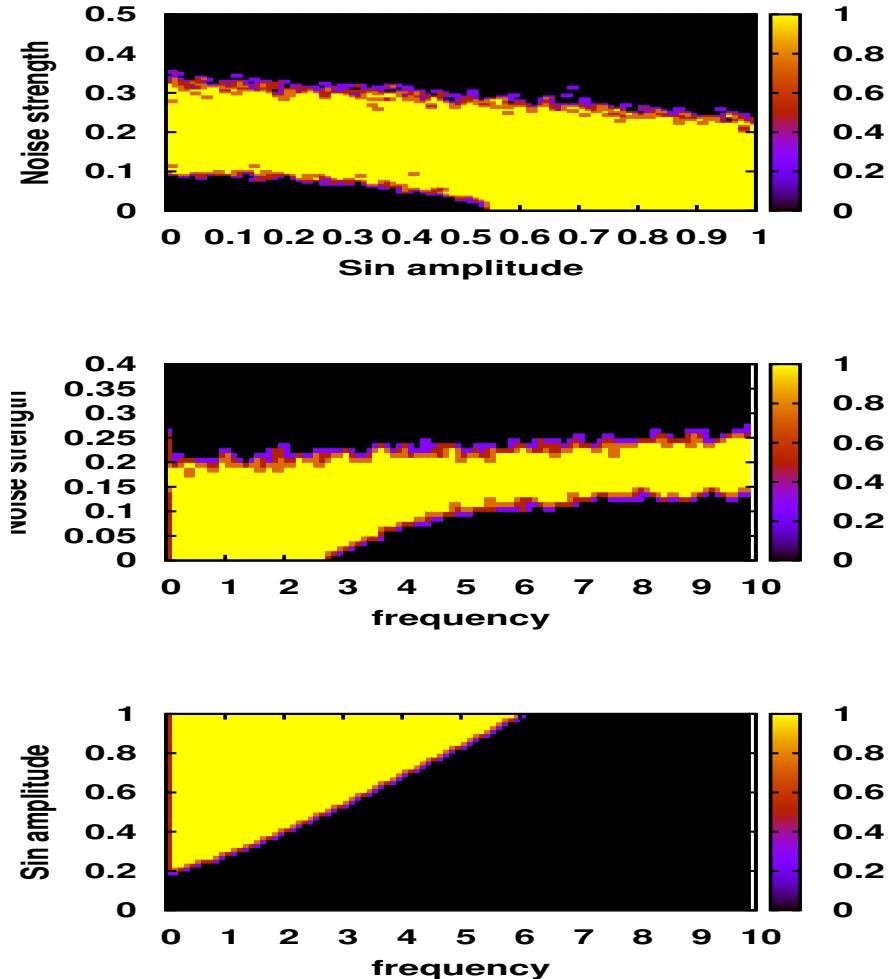


Figure 4.4: Probability of obtaining the AND logic operation with $b = -0.5$. Here $\omega = 4$ for left panel, $A = 0.5$ for middle panel and $D = 0.08$ for right panel. The system was simulated for 100 random combinations of the two inputs. The transience was set at 10 percent of the input timescale.

in response to change in the input signal, and averaged it over 1000 such switches. We observed that for low noise intensities there is sharp reduction in the average switching time when a periodic signal is added (see figure 4.5). For faster operation of the logic gate, it is desirable that time of an input or bit time be as low as possible. This can be done by setting the bit time equal to the minimum switching time plus time required for reading the state of the output. This gives us the minimum time for which an input should be applied so that we get robust operation of the logic gate. We explored the minimum switching time for various combinations of modulation frequencies, modulation amplitude and noise strengths. We found that systems driven by a periodic forcing of appropriate frequency and amplitude can function robustly

for bit times as low as one time unit (e.g by setting $A = 1$ and $\omega = 2.7$).

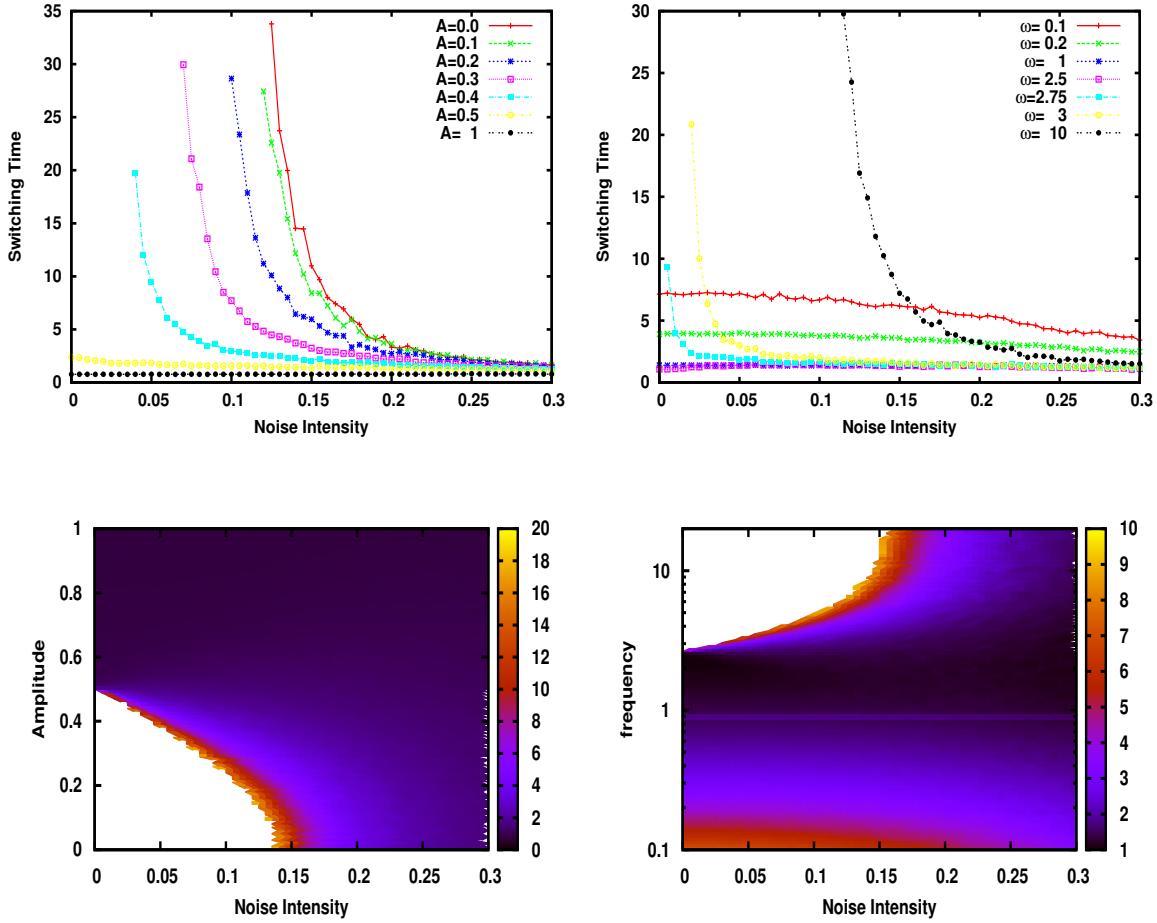


Figure 4.5: Switching time averaged over 1000 switches of output for the AND gate operation, over a range of noise strengths, amplitudes and frequencies. Here $b = -0.5$, $\omega = 2.7$ (left) and $A = 0.5$ (right). Note that for low amplitudes we don't get robust AND operation for low noise intensities. In the density plots, the colors represent the switching time, the white area corresponds to the range where the operation of the logic gate is not robust, and the frequency is plotted on a log scale in the density plot on the right.

4.4 Adaptive Logical Stochastic Resonance

In the above results we have seen that noise and a periodic forcing interfere constructively and aid the switching of the system between the two wells. This on one hand, helps to obtain desired responses at lower noise strengths but at the same time the response deteriorates slightly at higher values of noise intensity. This deterioration is not so significant and is at the higher noise boundary where one typically does not

operate. Still, if we want to ensure robust operation even in the higher noise window, one way to accomplish this would be to keep monitoring the noise levels in the system and then adjusting either the frequency or amplitude of periodic forcing, if the noise level crosses some threshold level. That is to say, we switch off the periodic forcing if the noise level is within the optimal window.

This approach will work fine if the changes in the noise strengths occur only occasionally. On the other hand, if the fluctuations in noise levels are quite frequent, then it will be better if the system could *automatically adapt itself to the changing noise levels for robust operation*.

Now we will show that by coupling two bistable systems we can enable robust operation of LSR elements over large spectrum of noise intensities. Here one of the bistable systems will be used to control the amplitude or frequency of the periodic forcing that is fed to the other system.

Consider the coupled systems:

$$\dot{x} = a_1(x - a_2x^3) + b + I_1 + I_2 + Ay \sin(\omega t) + D\eta(t) \quad (4.3)$$

$$\dot{y} = a_3(y - a_4y^3) + D\eta(t) \quad (4.4)$$

Here the output of second system modulates the sinusoidal forcing applied to the first system. The working principle in this form of coupling is that the second system has a lower potential barrier as compared to the first. When the noise is very low, the output of the second system will stay in the same well. Thus it will act as a constant signal and the sinusoidal forcing will simply be scaled by a factor, and the frequency of periodic forcing fed into first system will be same as that of the sinusoidal signal. This sinusoidal forcing then enables the operation of LSR elements even in low noise conditions, as was shown in chapter 3.

When the noise level increases, y jumps between the two wells according to the Kramer's rate, essentially behaving like a signal of high frequency as shown in figure 4.6 . As the modulating signal has a high frequency, the signal fed into the first system has a frequency much greater than the frequency of the sinusoidal signal. Thus the system doesn't get sufficient time to respond to this signal and hence the sinusoidal

forcing doesn't lead to random hops. The minimum frequency that we can choose for the sinusoidal forcing is governed by the transience time in which the system must reach the desired state. This is so because within this time the system should receive at least one full cycle of the periodic forcing. As mentioned earlier, we set the potential barrier for the second system much lower compared to first by selecting appropriate values of a_3 and a_4 . Further, the parameters chosen are such that the frequency of sinusoidal forcing is lower than the frequency obtained from Kramer's rate for noise strengths where noise alone is sufficient for robust operation of the LSR elements.

We simulated the system as given by equations 4.3 and 4.4 for 100 different initial conditions. In particular, we choose $a_1 = 4$, $a_2 = 5$, $a_3 = 2$, $a_4 = 8$, $\omega = 0.05$, $A = 0.6$ and calculate the range of D over which we get the robust logic operation. As before, in each run we took 7 different possible combinations of I_1 and I_2 . A run was counted as successful if and only if the time series matched the desired output 100 percent of the time, leaving out a small transient period. Then the ratio of successful runs to the total number of runs was defined as the probability of obtaining the correct logic. As shown in figure 4.7, we find that the probability of correct logic is 1 for much larger noise windows. Specifically, it is one for *all* noise intensities less than the maximum noise intensity for which correct logic was obtained in the absence of periodic forcing. Additionally the lower limit on noise intensity now no longer exists, and we can obtain robust logic operations even in noise-free case.

Moreover, if we use a slightly relaxed criteria for correct logic, that is, if we assume that logic is correct even if time series matches for a little less than 100 percent, then the critical noise intensity upto which correct logic is obtained increases further, as seen in the second and third panel of figure 4.7.

It is evident from figure 4.7 that the noise intensity upto which we get robust operations is slightly lower than that obtained in absence of periodic forcing. This arises from the enhancement of random hopping due to the added effect of periodic drive and noise.

Lastly, we consider adaptively changing the amplitude of sinusoidal forcing in-

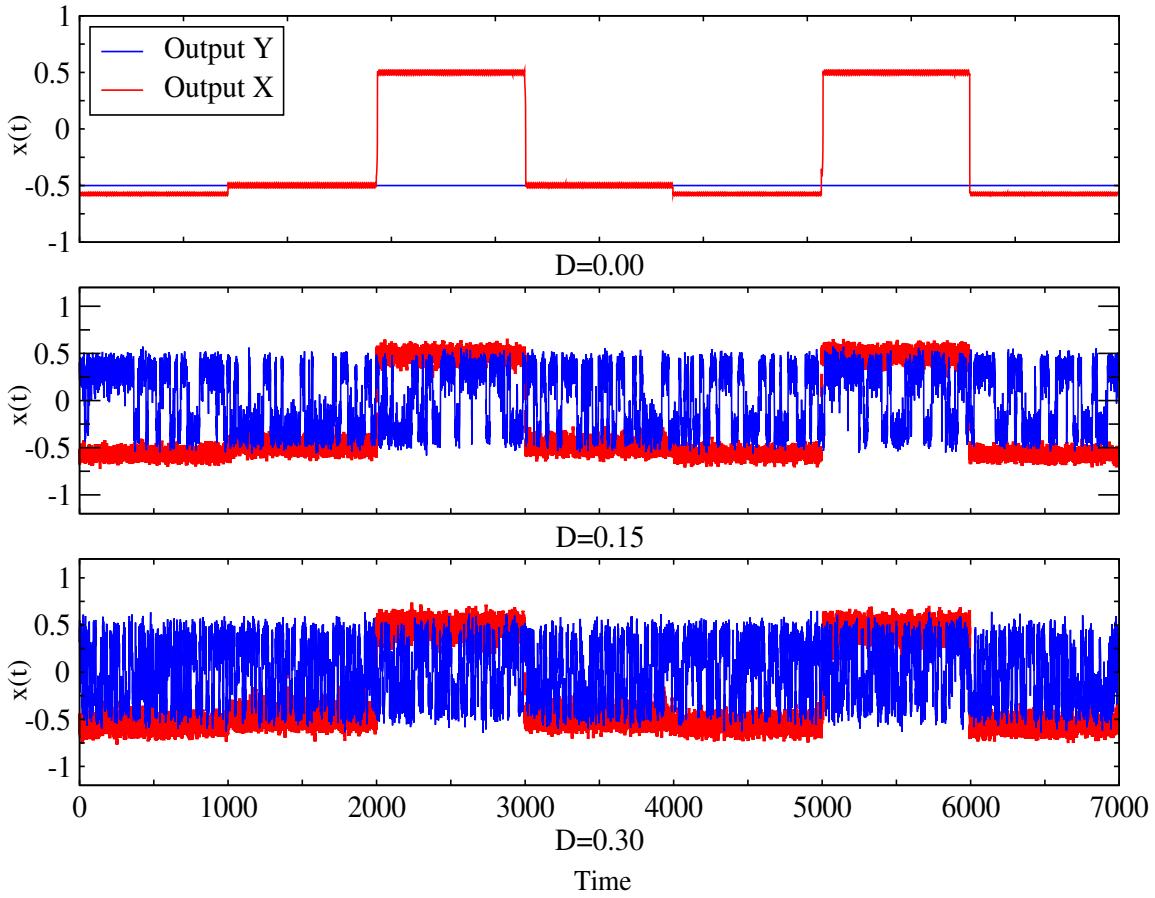


Figure 4.6: Time series for y (blue) and output (red) for the system given by eq. 4.3 and eq. 4.4 for noise intensities $D = 0$ (top), $D = 0.15$ (middle) and $D = 0.3$ (bottom).

stead of the frequency. For this, consider the system given by:

$$\dot{x} = a_1(x - a_2x^3) + b + I_1 + I_2 + A \langle y \rangle \sin(\omega t) + D\eta(t) \quad (4.5)$$

$$\dot{y} = a_3(y - a_4y^3) + D\eta(t) \quad (4.6)$$

where $\langle y \rangle$ is the average of y over a short interval of time. This kind of coupling is particularly relevant in chemical and biological systems, where the instantaneous state of the system is not easily detectable, but a short-time average is more accessible. Here instead of instantaneous value of y , its average over previous few values is fed back to the coupled system. When the noise in the system is low, the average value of its state will be equal to that of the potential well in which it is lying. When the noise level increases, the system jumps between the two wells according to the Kramer's rate. As the two wells are symmetric about zero, the average value approaches zero as the hopping rate increases, as shown in figure 4.8. Thus the amplitude of sinusoidal

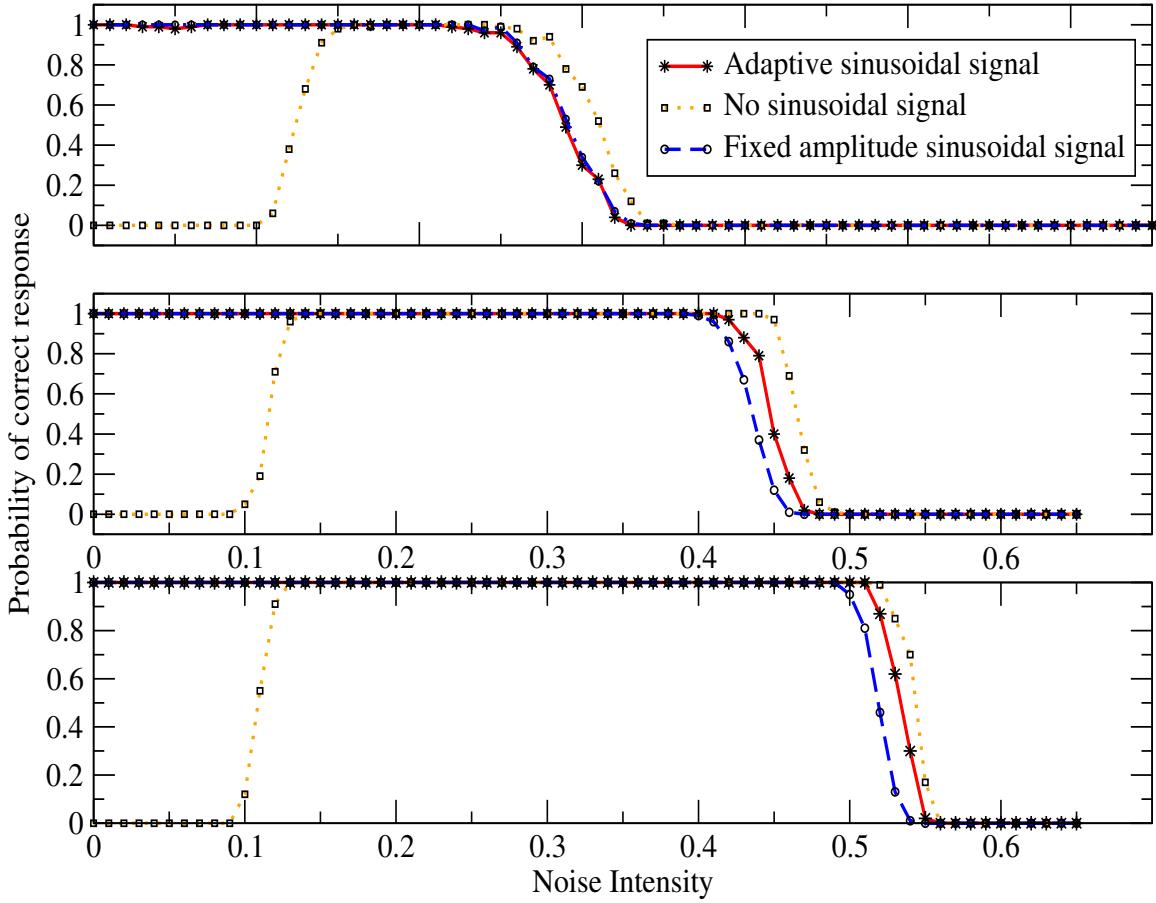


Figure 4.7: Probability of obtaining the AND logic operation with $b = -0.5$. Here $\omega = 0.05$, $A = 0.6$. The red line corresponds to simulations as given by eq. 4.3 and 4.4. Dashed orange and blue lines are obtained taking $A = 0$ and $A = 0.35$ in eq. 4.2. The system was simulated for 100 runs where each run was combination of seven different possible input sets of the two inputs. A run was taken to be successful if the time series matched the expected output 100 percent (top), 98 percent (middle) and 95 percent (bottom) of the time, after leaving out transience.

signal is reduced to zero.

We simulated the coupled systems given by equations 4.5 and 4.6 by averaging the value of y over 100 time units (the time for which an input is applied). Further, when the average is taken over a larger time interval, the response of these coupled systems will be better, provided that this time is smaller than the timescale over which the noise strength itself changes. The results are shown in figures 4.9. We see that in this case, not only does the lower limit on optimal noise window vanish, but for higher noise intensities too the results match with those obtained in absence of a periodic forcing.

The results are qualitatively the same even if there is some delay in propagation

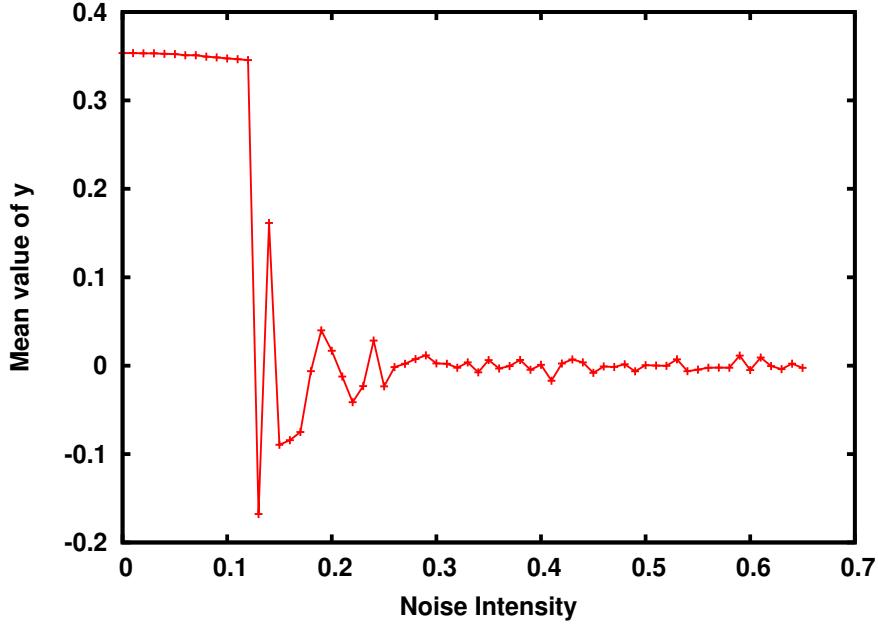


Figure 4.8: Every point represents mean value of y over previous 100 time units for that particular noise intensity, for the system given by eq. 4.6.

of $\langle y \rangle$, provided it not so large that noise intensity itself changes in this time. Additionally, similar results were obtained if we use a moving or running average of y . This is particularly helpful in electronic systems where a running average is far more easy to implement vis-a-vis a normal average which may involve a lot more computations and consequently result in delays.

4.5 Conclusion

In conclusion, we have explicitly shown that by utilizing the constructive interplay of noise and periodic forcing it is possible to obtain a logic response similar to LSR even when the strength of noise is lower than the minimum threshold. This enables us to use the LSR elements in sub-threshold noise conditions. Further, by coupling the LSR element to another LSR element with a lower potential barrier we can make the systems adapt to varying noise intensity, so that its operation is robust even in high noise conditions. The results presented here are quite general, and can potentially be extended to other systems which show enhanced performance in the presence of noise, such as typically observed in generalized stochastic resonance phenomena.

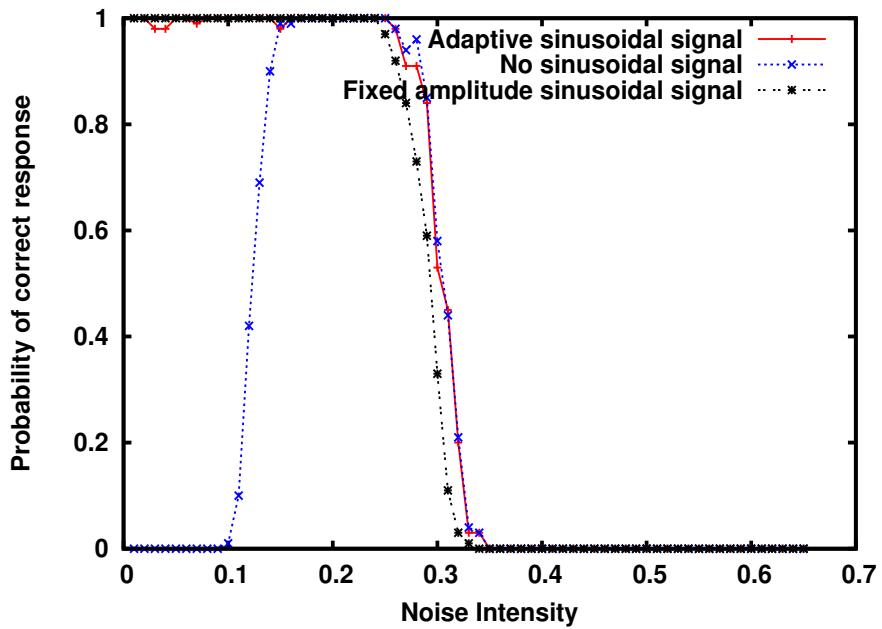


Figure 4.9: Probability of obtaining the AND logic operation, for the system given by eqs. 4.5 – 4.6. Further we show the case with no sinusoidal forcing and the case where the amplitude of the periodic forcing is constant. The system was simulated for 100 runs where each run was combination of seven different possible input sets of the two inputs. A run was taken to be successful if the time series matched the expected output 100 percent of the time, after transience.

Chapter 5

Performance enhancement of VCSEL based stochastic logic gates

5.1 Introduction

Vertical-cavity surface-emitting lasers (VCSELs) are widely used for high-bit-rate data transmission because of their various advantages over conventional edge emitting lasers like low threshold current, single-longitudinal-mode operation, higher modulation bandwidth and circular output beam profile. They emit linearly polarized light whose direction can change with change in operating conditions like temperature or the injection current [46]. It involves switching between the two orthogonal linearly polarized modes. More dynamical features emerge when there is optical feedback, current modulation or optical injection [47]. This polarization-bistability of VCSELs has been used to build optical buffer memories [48].

Zamora-Munt et al demonstrated the phenomenon of LSR in VCSEL by encoding the logic inputs in an aperiodic signal which directly modulates the laser bias current [35]. The probability of correct response was observed to be ~ 1 in a wide region of noise strengths. They associated LSR with optimal noise-activated polar-

ization switchings (the so-called “inter-well” dynamics if one considers the VCSEL as a bistable system described by a double-well potential) and optimal sensitivity to spontaneous emission in each polarization (the “intra-well” dynamics in the double-well potential picture).

In another work [43], by encoding the logic inputs in the strength of the light injected into the suppressed polarization mode of the VCSEL (the so-called ‘orthogonal’ injection), and by decoding the output logic response from the polarization state of the emitted light, Perrone et al demonstrated an all-optical stochastic logic gate. It was observed that correct logic output response can be obtained for as short as 5 ns bit times thus lowering the the minimum bit time for successful operation from 30-40 ns observed in the opto-electronic stochastic logic gate [35],[43].

In chapter 3 of this book, it was shown that in absence of noise a behaviour similar to LSR can be observed by addition of a periodic forcing (sinusoidal or rectangular). As in case of LSR, robust operation is obtained only when the amplitude and frequency of the periodic forcing is within an optimal range. Further, when noise is also present, this periodic forcing interacts cooperatively and in situations when noise is below the minimum threshold of optimal range, the periodic forcing allows us to operate successfully even under sub threshold noise conditions. At the higher end of optimal noise window, this periodic forcing leads to slight deterioration in performance. We can then couple another bistable system to control the effective amplitude or frequency of the periodic forcing so that we obtain robust operation for all noise intensities below the maximum threshold (see chapter 4).

In this chapter, we explore the possibility of enhancing the operational range of VCSEL based stochastic logic gate by addition of a periodic signal. The enhancement can be either in form of decrease in the minimum bit time necessary for successful operation or in terms of increasing the optimal window of noise in which this logic gate can function robustly. We try this with both opto-electronic as well as the all optical configuration. Specifically, we try by adding periodic forcing as $E_{\text{injection}}$ in the opto-electronic configuration. In the all optical configuration, we explore the effect of periodic forcing in two ways: firstly, by modulating the bias current and secondly, by adding it as $E_{\text{injection}}$ as in the opto-electronic configuration.

We discuss the model rate equations used to simulate the VCSEL in the next

section and report our results in the subsequent section and then discuss the results and the conclusions drawn in the last section.

5.2 Model Equations

We use the spin-flip model [49] to simulate the polarization dynamics of VCSELs. This model is a set of six ordinary differential equations describing the evolution of the real and imaginary parts of two complex optical fields (associated with two orthogonal polarizations) as well as two carrier densities with opposite spin. The model has been extended to take into account Y-polarized optical injection. The equations are

$$\begin{aligned} dE_x/dt &= \kappa(1 + i\alpha)[(N - 1)E_x + inE_y] - (\gamma_a + i(\gamma_p + \Delta\omega))E_x \\ &\quad + \sqrt{\beta_{sp}\gamma_N N}\xi_x \\ dE_y/dt &= \kappa(1 + i\alpha)[(N - 1)E_y - inE_x] + (\gamma_a + i(\gamma_p - \Delta\omega))E_y \\ &\quad + \sqrt{\beta_{sp}\gamma_N N}\xi_y + \kappa E_{inj} \\ dN/dt &= \gamma_N[\mu - N(1 + |E_x|^2 + |E_y|^2) - in(E_yE_x^* - E_xE_y^*)] \\ dn/dt &= -\gamma_s n - \gamma_N(n|E_x|^2 + |E_y|^2) + iN(E_yE_x^* - E_xE_y^*) \end{aligned}$$

where E_x and E_y are linearly polarized slowly-varying complex amplitudes, N is the total carrier population, and n is the population difference between the carrier densities with positive and negative spin values, κ is the field decay rate, γ_N is the decay rate of the total carrier population, γ_s is the spin-flip rate, α the linewidth enhancement factor, γ_a and γ_p are linear anisotropies representing dichroism and birefringence, μ is the injection current parameter normalized such that the threshold in the absence of anisotropies is at $\mu_{th} = 1$, and $\xi_{x,y}$ are uncorrelated Gaussian white noises with zero mean and unit variance[43].

The optical power injected into the Y polarization is represented by $P_{inj} = E_{inj}^2$. The model equations are written in the reference frame of the injected field, and

thus the detuning $\Delta\omega$ is the difference between the optical frequency of the injected field and the frequency intermediate between the X and the Y polarization. Without optical injection and with $\gamma_a = 0$, the angular optical frequencies of the X and the Y polarizations are $-\gamma_p$ and γ_p respectively, and therefore, $\Delta\omega = -\gamma_p$ ($+\gamma_p$) means that the injected field is resonant with the X (Y) polarized mode of the solitary VCSEL [43].

5.3 Results

5.3.1 Optoelectronic Configuration

We use the opto-electronic configuration as in [35] for using VCSEL as a stochastic logic gate. In this configuration, the two logic inputs are encoded in a three-level aperiodic modulation directly applied to the laser pump current. The laser response is determined by the polarization of the emitted light. The parameters are chosen such that the laser emits either the x or the y polarization and the parameter regions where there is anti-correlated polarization coexistence or elliptically polarized light are avoided. The laser response is considered a logical 1 if, for instance, the x polarization is emitted, and a logical 0, if the y polarization is emitted. One can obtain the complementary logic gate by detecting the orthogonal polarization.

In fig 5.1 we plot E_x vs μ for different rates of change of μ .

We observe hysteresis in both the cases. Further, as μ varies at a fast rate we observe oscillations.

In fig 5.2, we find that this system functions as a stochastic logic gate for optimal values of noise intensity. For low or high noise strengths, the percentage of power emitted in specific polarization doesn't switch with changes in the input signal. When noise intensity is low, polarization switching is delayed whereas a high noise intensity results in emission in both polarization modes.

We calculate the probability of correct logical response by evaluating the response of this gate for large number of input bits. To decide whether the response is right or

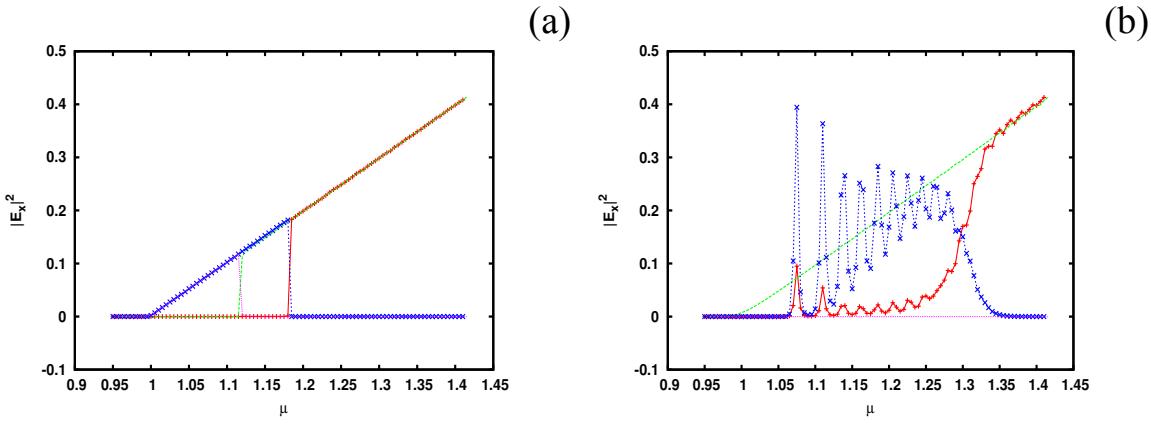


Figure 5.1: Intensities of x and y polarizations when the injection current increases and decreases linearly from $\mu_i = 0.9$ to $\mu_f = 1.4$ slowly (top) and fast (bottom). The parameters are $\kappa = 300\text{ns}^{-1}$, $\alpha = 3$, $\gamma_N = 1\text{ns}^{-1}$, $\gamma_a = 0.5\text{ns}^{-1}$, $\gamma_p = 50\text{radns}^{-1}$ and $D = 10^{-6}\text{ns}^{-1}$.

wrong, we calculate the fraction of power emitted in any one polarization state. If the polarization state corresponds to correct response and percentage of power emitted in this polarization is more than the threshold P_{th}^{max} value, we call it as correct response. Alternately, we also define P_{th}^{min} as the minimum threshold and power emitted should be lower than this threshold if this is wrong polarization. In our simulations, we evaluate the responses at three different thresholds, 70%, 80% and 90%. The results are displayed in fig. 5.3. It can be seen that for relaxed criteria i.e. 70%, the probability of correct operation is higher. Further, we get $P = 1$ for intermediate values of noise strength.

Next, we apply a periodic forcing as E_{inj} to the opto-electronic configuration to see if the performance of VCSEL based stochastic logic gate can be improved. As we can see in fig. 5.3, the performance of the stochastic logic gate is enhanced for low noise intensities and decreases for high noise intensities when periodic forcing is added. Again from fig. 5.3, we can see that noise free morphing is also possible.

As we can see that at low noise intensities, orthogonal injection improves the performance of this system. So the next logical question is to see if the logic operations can be realized even in absence of noise and using only the orthogonal injection as shown in fig. 5.4.

Now we study the effect of orthogonal injection on the minimum bit time necessary for successful operation. As can be seen in fig. 5.5, for low noise intensities,

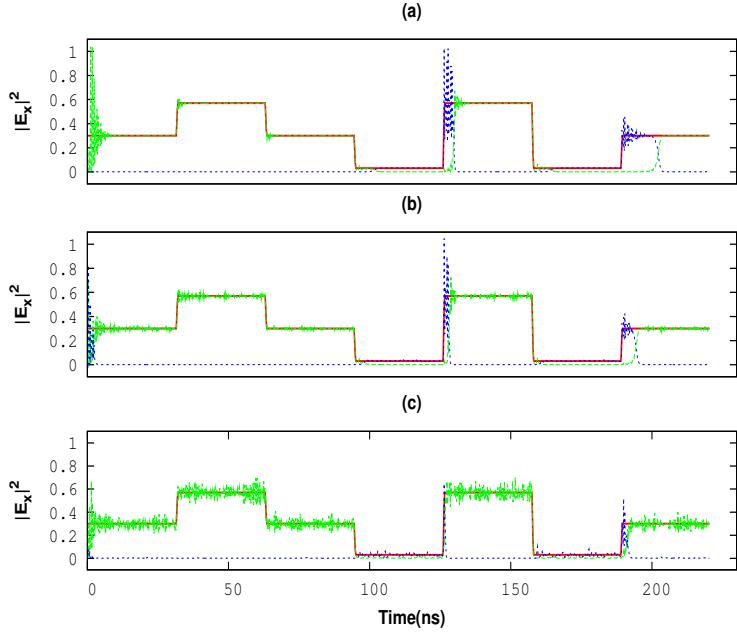


Figure 5.2: Time traces of the x polarization (solid green), y polarization (dotted blue), and the injection current $\mu - 1$ for different noise intensities (a) $D = 5 \times 10^{-7}$ (b) $D = 4 \times 10^{-4}$ and (c) $D = 6 \times 10^{-3}$. The parameters are $T = 31.5\text{ns}$, $\mu_0 = 1.3$, $\Delta\mu = 0.27$, $\kappa = 300\text{ns}^{-1}$, $\alpha = 3$, $\gamma_N = 1\text{ns}^{-1}$, $\gamma_a = 0.5\text{ns}^{-1}$ and $\gamma_p = 50\text{radns}^{-1}$.

there is marked decrease in the minimum bit time necessary for successful operation. At higher noise intensities, the orthogonal injection doesn't affect much.

These observed behaviours can be explained by considering that just like the noise, periodic forcing also facilitates the switchings between the polarizations and when noise is low or insufficient to result in polarization switching by itself, then periodic frequency aids the polarization switchings in such cases.

5.3.2 All-optical configuration

In this section, we analyze the performance of the stochastic logic gate in the all optical configuration. In this configuration, the logic inputs are encoded in the strength of the light injected into the suppressed polarization mode of the VCSEL and the output logic response is decoded from the polarization state of the emitted light[43]. We consider addition of periodic forcing in two ways: first by small fluctuations in modulation current μ and secondly by adding a small periodic forcing to E_{inj} . We explored the minimum bit times for different values of modulation current and when

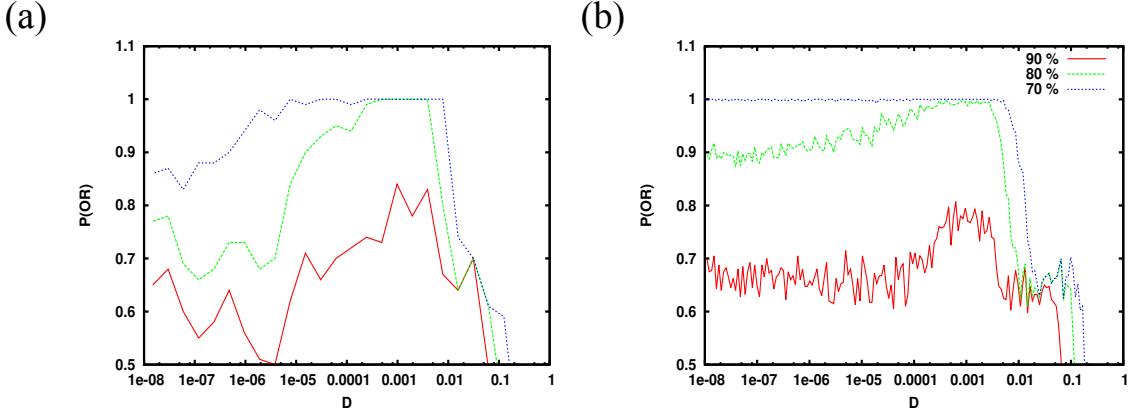


Figure 5.3: The probability of correct operation of stochastic logic gate vs noise intensity in the optoelectronic configuration when periodic forcing is added as E_{inj} in the orthogonal LP mode. Left figure shows the results in absence of periodic forcing. Clearly there is performance enhancement of the gate for low noise intensities. Here $T_{bit} = 31.5\text{ns}^{-1}$

the modulation current varied between two levels. The results are displayed in fig 5.6. We can see that by adjusting the current modulation, we can obtain robust operations in different noise conditions. The results for injection current modulation are presented next.

First we plot the probability of correct response vs noise intensity (see fig 5.7) and then vs bit time (see fig 5.8) for the all optical configuration. From the figures, it is clear that probability of correct response increases for the 80% threshold criteria. At higher noise intensities, the performance degrades for all the cases. Similarly, the bit times improve for 70% criteria but degrade for 90% threshold criteria. So we can tune the periodic frequency to obtain best response in the desired noise window and under the particular threshold criteria.

5.4 Conclusion

In this work we have demonstrated that the performance of a VCSEL based stochastic logic gate can be enhanced by addition of a periodic signal in the orthogonal LP mode. This enhancement was observed for both the optoelectronic configuration as well as the all optical configuration and both in form of increase in the optimal noise window as well as decrease in minimum bit time. By tuning the amplitude and frequency of

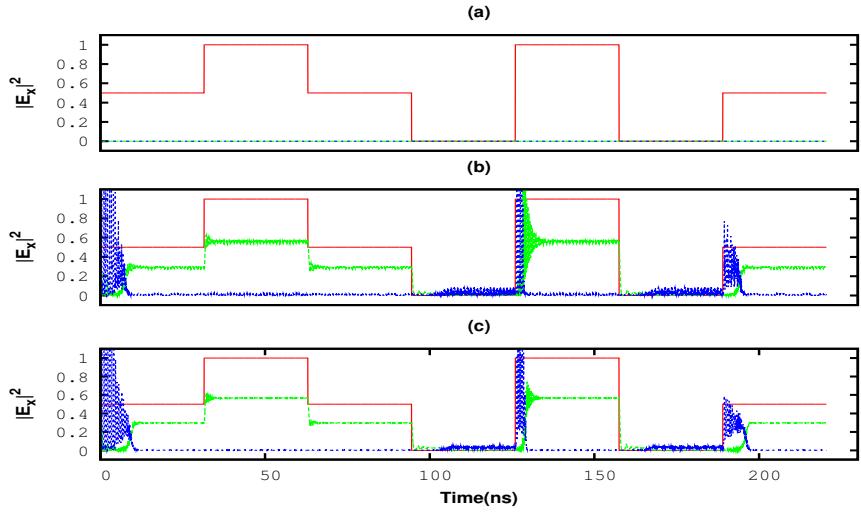


Figure 5.4: Noise Free morphing i.e. when $D = 0$ and (a) No sinusoidal forcing (b) With sinusoidal forcing with $\omega = 0.5$ and $A = 0.02$ and (c) With a sinusoidal forcing of low frequency $\omega = 0.2$ and $A = 0.01$. The sinusoidal forcing has been added as the E_{inj} . All other parameters are same as in fig 5.2

the periodic forcing we can have better control over the stochastic logic gate and can improve its response in the desired noise window with a particular threshold criteria.

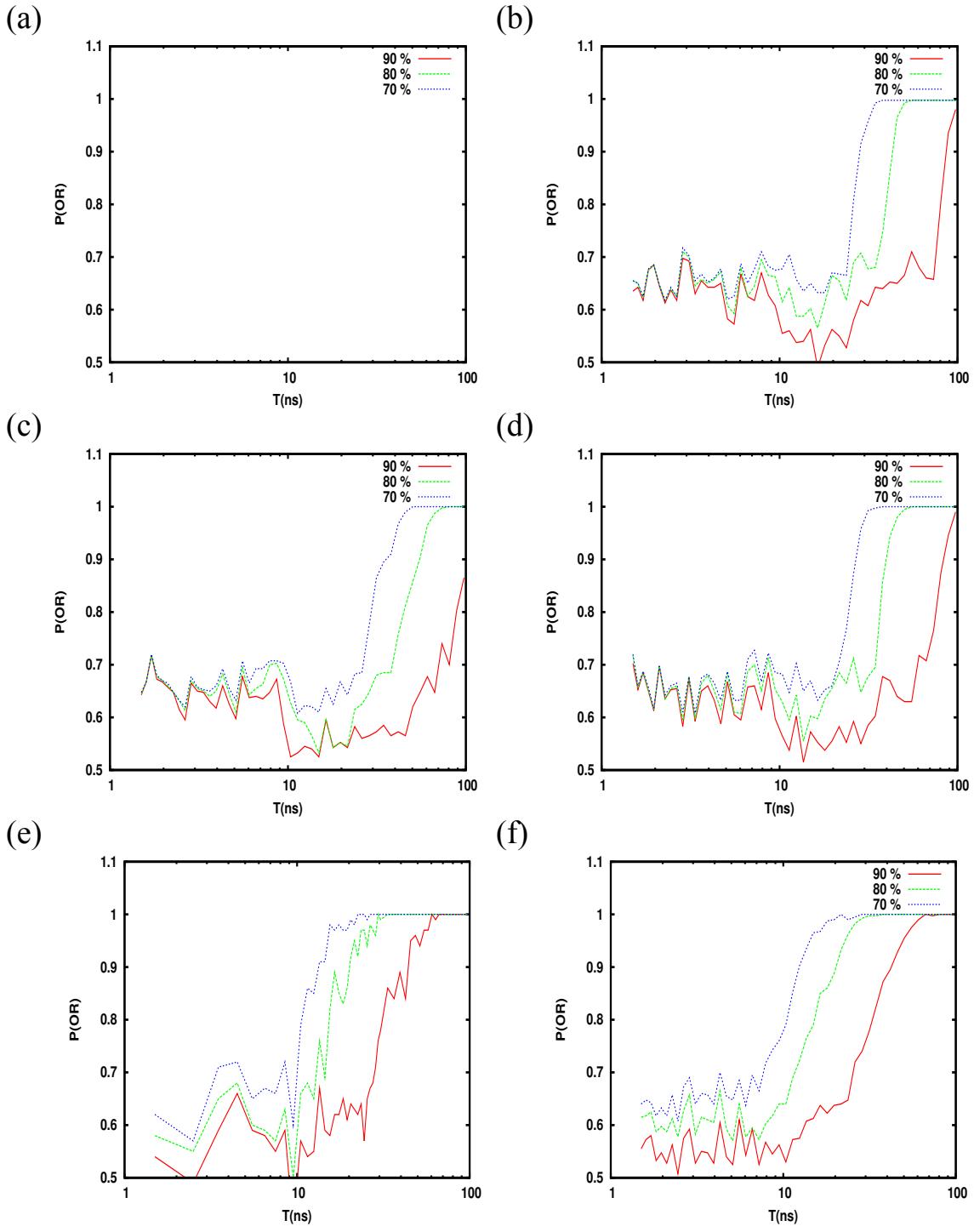


Figure 5.5: The probability of correct operation of stochastic logic gate vs bit time in the optoelectronic configuration when periodic forcing is added as E_{inj} in the orthogonal LP mode. Left figure shows the results in absence of periodic forcing. Clearly there is performance enhancement of the gate for low noise intensities. Here $D = 0.00$ for (a), (b) $D = 10^{-7}$ for (c), (d) and $D = 0.0004$ for (e), (f). In (a) the probability is zero at all points.

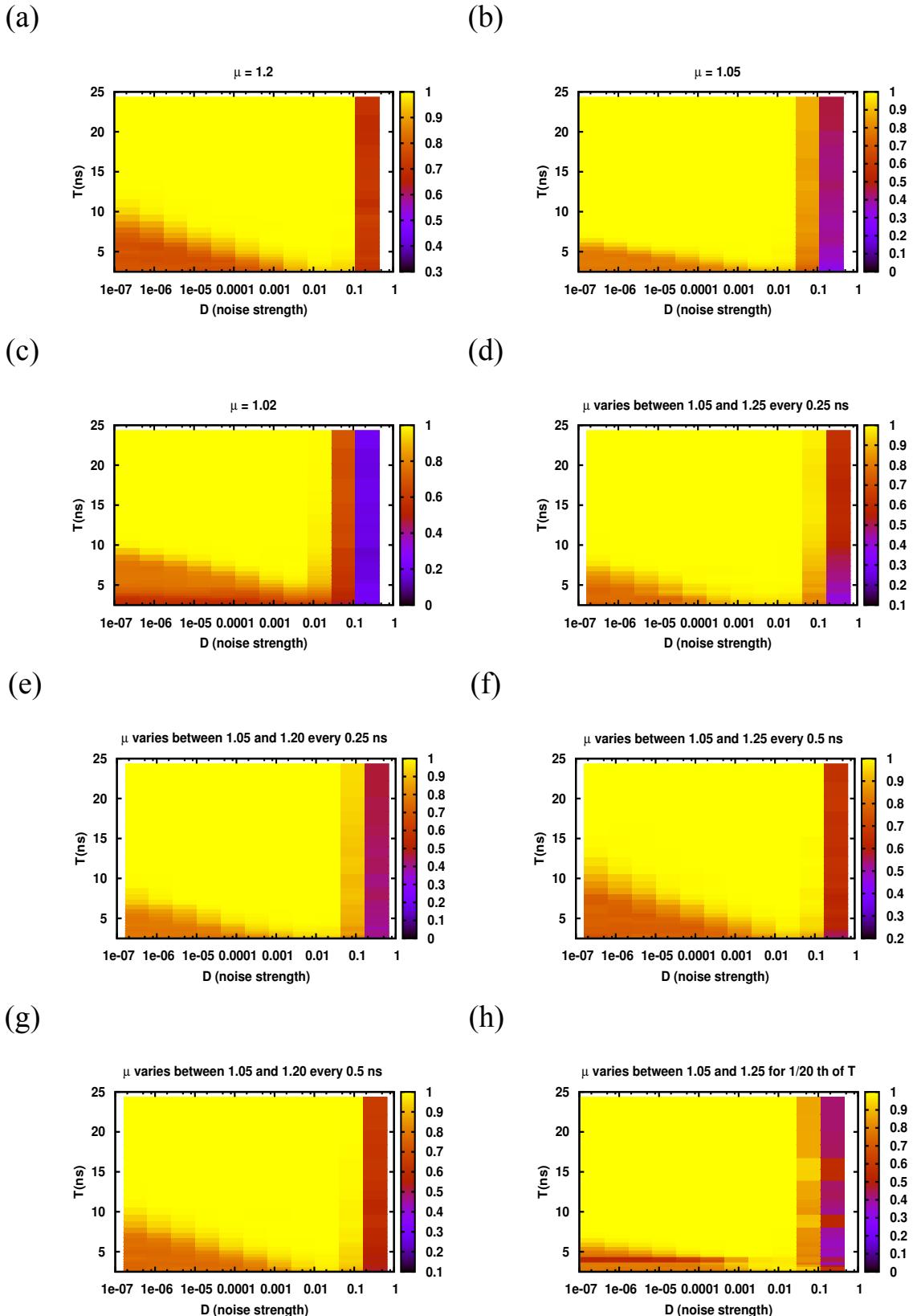


Figure 5.6: Minimum bit time required for successful operation for the all optical configuration for various noise intensities and pump currents.

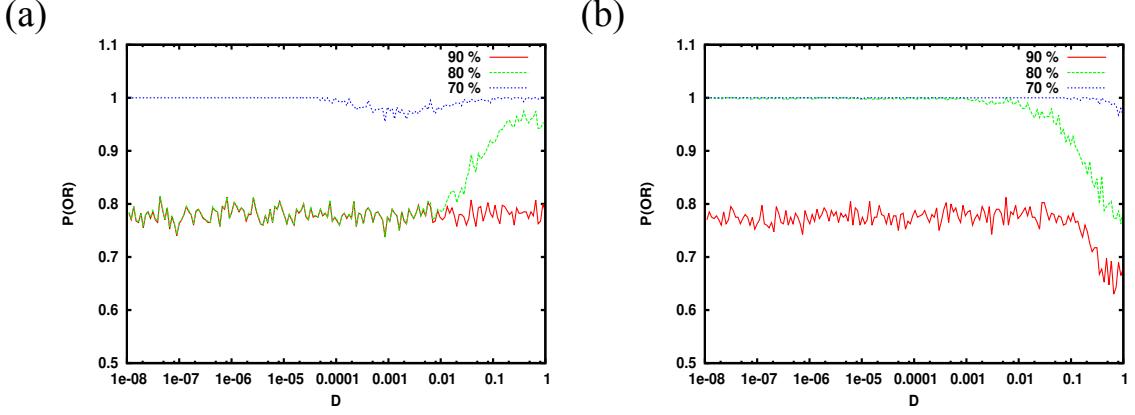


Figure 5.7: The probability of correct operation of stochastic logic gate vs noise intensity in the all optical configuration when periodic forcing is added as E_{inj} in the orthogonal LP mode. Left figure shows the results in absence of periodic forcing. The performance is enhanced for low noise intensities for the 80 percent criteria. Here $T_{bit} = 5.5 \text{ ns}^{-1}$

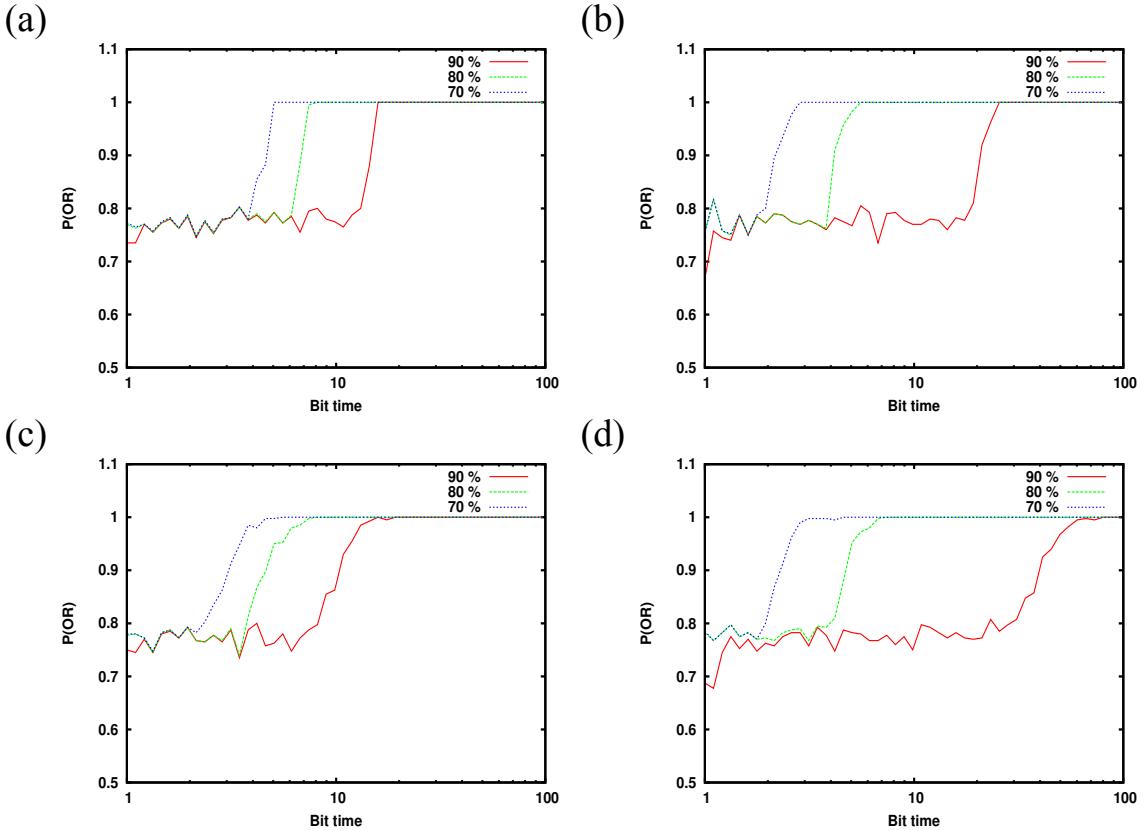


Figure 5.8: The probability of correct operation of stochastic logic gate vs bit time in the all optical configuration when periodic forcing is added as E_{inj} in the orthogonal LP mode. Left figure shows the results in absence of periodic forcing. Here $D = 10^{-5}$ for (a), (b) and $D = 0.1$ for (c), (d).

Chapter 6

Conclusions and future directions

In this book, we have studied the emergent patterns in nonlinear systems and the possible use of nonlinear dynamical systems in designing computing systems capable of functioning robustly in noisy environments. We have explicitly shown that a nonlinear system can produce a completely consistent logic as well as Set-Reset latch operation on two inputs, streaming in any random sequence. We have found that for very small or very large noise strengths the system does not yield a reliable output. However, in a reasonably wide band of moderate noise strength, the system produced the desired output very consistently. Furthermore, the response of the system could be easily switched from memory to logic operations by varying the bias in the system. It has been shown that noise can reduce the latency in the response of the system to switched inputs.

We have also shown through numerics and circuit experiments, that it is possible to obtain a logic response exactly similar to LSR, without the presence of noise. Using only a periodically driven bistable system, we have produced a logical combination of two inputs streaming in any random sequence. For very small or very large forcing frequencies the system did not yield any consistent logic output, but in a wide band of moderate frequencies the system produced the desired logical output very reliably. Furthermore, the logic response of the system could be easily switched from one logic gate to another by varying the bias in the system. Thus it has been shown that noise

is not a necessary ingredient to facilitate changes of state that reliably mirror logical outputs.

Further, we have explicitly shown that by utilizing the constructive interplay of noise and periodic forcing it is possible to obtain a logic response similar to LSR even when the strength of noise is lower than the minimum threshold. This enables us to use the LSR elements in sub-threshold noise conditions. Moreover, by coupling the LSR element to another LSR element with a lower potential barrier we can make the systems adapt to varying noise intensity, so that its operation is robust even in high noise conditions. The results that we have presented are quite general, and can potentially be extended to other systems which show enhanced performance in the presence of noise, such as typically observed in generalized stochastic resonance phenomena.

We have also demonstrated that the performance of a VCSEL based stochastic logic gate can be enhanced by addition of a periodic signal in the orthogonal LP mode. This enhancement has been observed for both the optoelectronic configuration as well as the all optical configuration and both in form of increase in the optimal noise window as well as decrease in minimum bit time.

So it is evident that ``LSR Elements'' can reliably function as logic and memory devices even for sub-threshold signals, thus consuming very low power. These ``LSR Elements'' can potentially act as building blocks of futuristic ``Smart Computing Devices''. Potentially, such devices will not only operate robustly in noisy environments, but can also be capable of optimal utilization of their resources by configuring their ``LSR Elements'' into latches, or any of the logic gates, depending on the requirements of the task being performed. For example, if we are performing tasks requiring more computational power like running a code, then these computing devices will morph most of the LSR elements to logic gates, whereas in case of tasks requiring memory like plotting large values of data, LSR elements will be morphed into memory enabling efficient use of resources. Furthermore, it is conceivable that devices based on such elements can potentially help in reducing boot times thus achieving what is commonly called ``instant boot''. This can be accomplished by morphing large number of LSR elements into memory at the time of shut down and start up. This significant increase in memory will enable us to keep most of the data

required for the applications readily accessible, paving way for faster boot times.

In future, one can demonstrate LSR in other bistable and multi-stable systems and realize some other basic operations like adder. Different operations in parallel by measuring the state of different state variables can be obtained. LSR appears to be a fairly generic phenomenon and one can examine study the behavior when noise is replaced by chaotic signals.

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