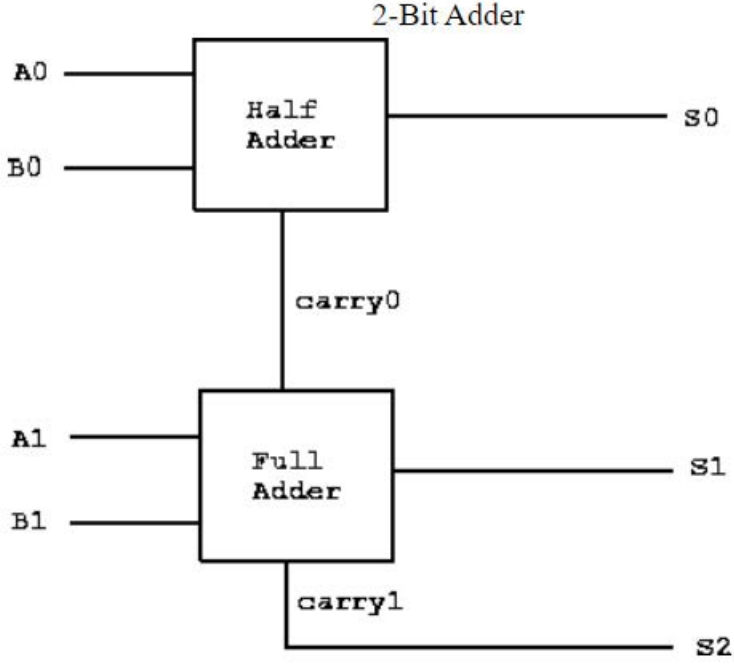
2-Bit Adder
A0
B0
Half
Adder
S0
carry0
A1
B1
Full
Adder
S1
carry1
S2

Homework - [D:/Soft/Xilinx/vivado save files/Homework/Homework.xpr] - Vivado 2022.2

File Edit Flow Tools Reports Window Layout View Run Help Quick Access

Synthesis and Implementation Out-of-date details

Default Layout

Flow Navigator

- **PROJECT MANAGER**
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- **IP INTEGRATOR**
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- **SIMULATION**
  - Run Simulation
- **RTL ANALYSIS**
  - Open Elaborated Design
- **SYNTHESIS**
  - Run Synthesis
  - Open Synthesized Design
- **IMPLEMENTATION**
  - Run Implementation
  - Open Implemented Design
- **PROGRAM AND DEBUG**
  - Generate Bitstream
  - Open Hardware Manager

SIMULATION - Behavioral Simulation - Functional - sim_1 - two_bit_adder

Scope Sources Objects Protocol Instances

full_adder.v | two_bit_adder.v * | half_adder_behav.wcfg*

D:/Soft/Xilinx/vivado save files/Homework/Homework.srcs/sources_1/new/two_bit_adder.v

```
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21
22
23 module two_bit_adder(input clr,[1:0]x, [1:0]y, output [2:0]z );
24
25 half_adder hf1(clr,x[0],y[0],z[0],w1);
26 full_adder fl1(clr,x[1],y[1],w1,z[1],z[2]);
27
28 endmodule
29
```

Tcl Console | Messages | Log

29:1 Insert Sim Time: 6 us Verilog

Homework - [D:/Soft/Xilinx/vivado save files/Homework/Homework.xpr] - Vivado 2022.2

File Edit Flow Tools Reports Window Layout View Run Help Quick Access

Synthesis and Implementation Out-of-date details

Default Layout

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IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Open Elaborated Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager

SIMULATION - Behavioral Simulation - Functional - sim_1 - two_bit_adder

Scope Sources Objects Protocol Instances

full_adder.v | two_bit_adder.v * | half_adder_behav.wcfg*

Name	Value
clr	0
x[1:0]	11
y[1:0]	11
z[2:0]	000

1,012.030 ns

1,000.000 ns 2,000.000 ns 3,000.000 ns 4,000.000 ns 5,000.000 ns 6,000.000 ns 7

x[1:0]: 11 | 00 | 10 | 11

y[1:0]: 11 | 00 | 01 | 11 | 10

z[2:0]: 000 | 011 | 110 | 101 | 000

Tcl Console Messages Log

Sim Time: 7 us

Homework - [D:/Soft/Xilinx/vivado save files/Homework/Homework.xpr] - Vivado 2022.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Synthesis and Implementation Out-of-date details

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Open Elaborated Design
  - Report Methodology
  - Report DRC
  - Report Noise
  - Schematic
  - Open Dataflow Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

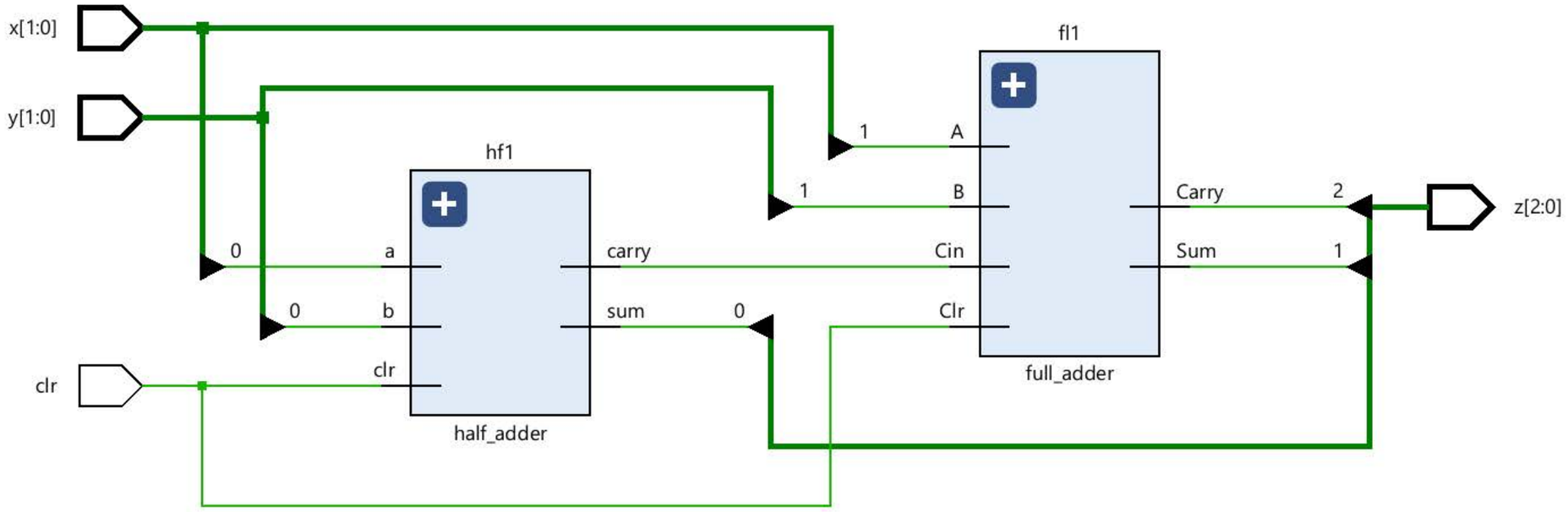
IMPLEMENTATION

ELABORATED DESIGN - xc7a35tcpg236-1

Sources Netlist Simulation Object Properties

Project Summary | Schematic | full_adder.v | two_bit_adder.v *

2 Cells 8 I/O Ports 9 Nets



Tcl Console Messages Log Reports Design Runs

Homework - [D:/Soft/Xilinx/vivado save files/Homework/Homework.xpr] - Vivado 2022.2

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Synthesis Complete

Default Layout

Flow Navigator

- Schematic
- Open Dataflow Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Set Up Debug
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

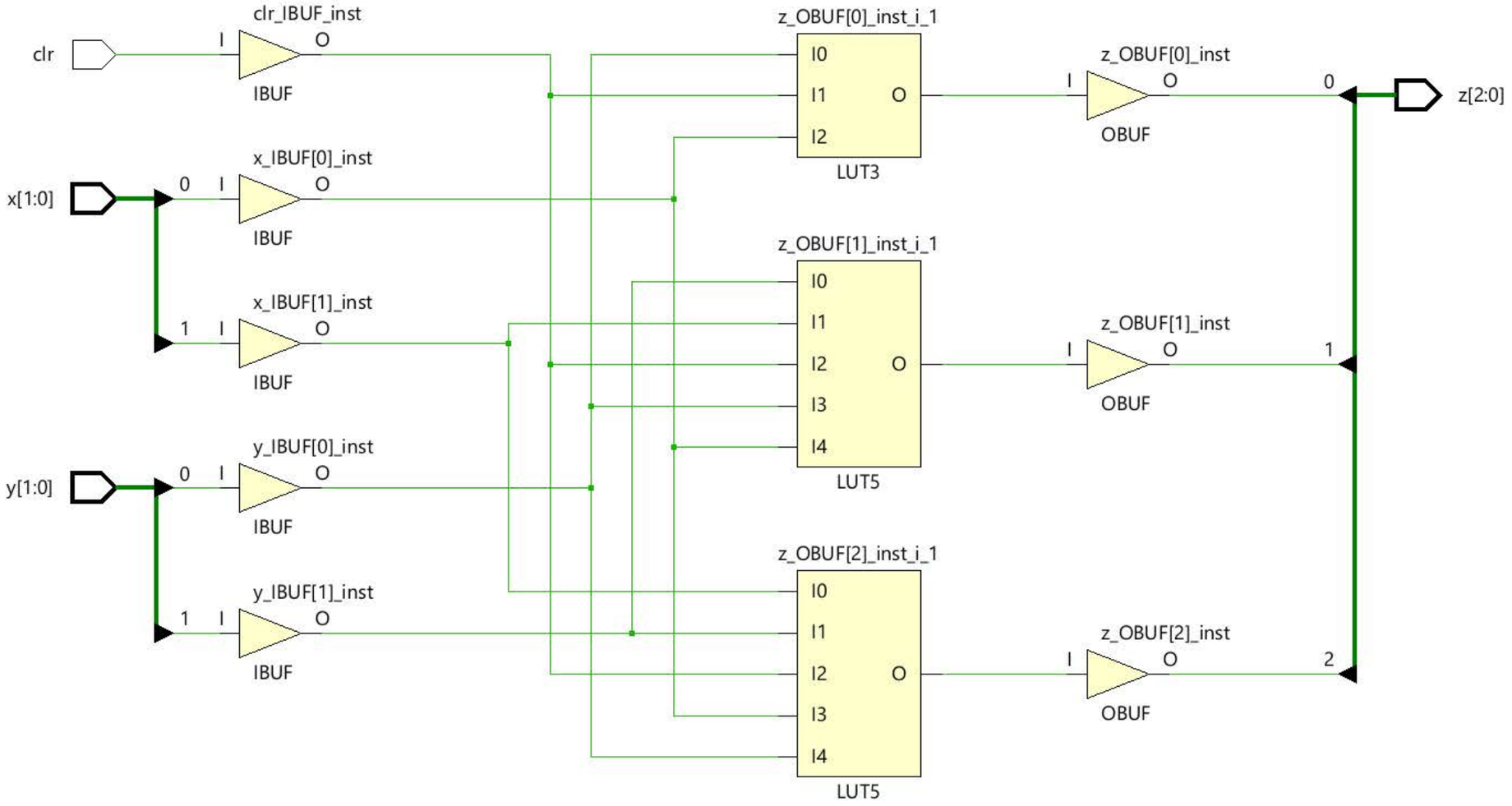
- Generate Bitstream
- Open Hardware Manager

SYNTHESIZED DESIGN - xc7a35tcpg236-1

Sources Netlist Properties

Project Summary | Device | full_adder.v | two_bit_adder.v | Schematic

11 Cells 8 I/O Ports 16 Nets



Tcl Console | Messages | Log | Reports | Design Runs