**PART A**

1. 100.73 us
2. “rClk” and “tClk” are generated from the system clock through the system “clk” turning to the on position and causing the cascading system of other processes generating “rClk “ and “tClk”.
3. The function of the signal tdSReg is to change the transmitter register to different states between: “Idle”, “Next”, “Shift”, “Transfer”, and “Reset”.
4. The bits [1:8] in tdSReg are loaded with data from DBIN.
5. The other bits are used to determine if DBIN is a parity error, one is a stop bit and the other is a start bit.
6. The maximum frame rate is 1612.903 frames per second.
7. The bit rate of the data achieved is 12903.226 bits per second.

The Transmitter state machine starts in the idle state with shift, load, and tClkRst all equal to ‘0’. If the reset is ‘0’ then the next state will be transfer. In the transfer state load is ‘1’ and tClkrst is ‘1’, then the machine will immediately move to the shift state. In the shift state, shift is equal to ‘0’ and until tCtr is equal to 12 then the machine will remain in the shift state. When tCtr is equal to 12 then the machine will move back to the idle state and restart.

**PART B**

1. The function of rdSReg is to shift the received data, and send the received data to be checked for a parity and to the rdReg.
2. The function of the rdReg is to take the first 8 bits of the shifted received data from rdSreg to output as the DBOUT.
3. The function of dataCtr is to count up while shift is equal to ‘1’ until it reaches 10, then the receiver would move on to the next state.
4. The UART has the capabilities to both transmit and receive data at the same time.

The Receiver state machine begins in the idle state and moves to the eight delay state if the counter reset is enabled and the RXD and FEint are disabled. In the eight delay state, the machine remains in that state till the counter reaches 7, then the counter reset and data reset are both enabled. When all those conditions are achieved, then the machine moves to the get data state. The machine remains in the get-data state till the counter reaches 14 then the machine will move to the shift state, and if the data counter reaches 10 then the machine will move to the checkstop state. In the Shift state, the counter reset and the shift are enabled and the machine returns back to the get-data state. In the checkstop stop the machine enables the clock to load the rdReg and flag registers.

**PART C**

1. The received data pattern is “11111010”.
2. The UART is checking for an odd parity.
3. The UART is generating an even parity.
4. The receiver checks for a parity through the shifted data from rsdReg and the transmitter computes the parity bit to send by xor-ing every bit in the DBIN.
5. The received data pattern is “10101010”.
6. This occurred because the expected stop bit was supposed to be ‘1’ when it was actually ‘0’.
7. Yes
8. The UART will only transmit and receive the error slower to account for the 4% error but will still receive the data correctly.
9. “10001111”
10. In the simulation there is a slight delay between the sample and UART beginning it processes.
11. The simulation takes the sample at a faster rate causing differences in the flags.