VLSI DESIGN [EE618]

ASSIGNMENT – 3

Submitted By-
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Q1. Assume that your library contains components with delays as given below:

Inverter 100 ps
NAND gate 150 ps
NOR gate 150 ps
A+B.C 200 ps
Tiny XOR 200 ps
Half Adder (carry) 250 ps
Half Adder (sum) 200 ps
Full Adder (carry) 400 ps
Full Adder (sum) 400 ps

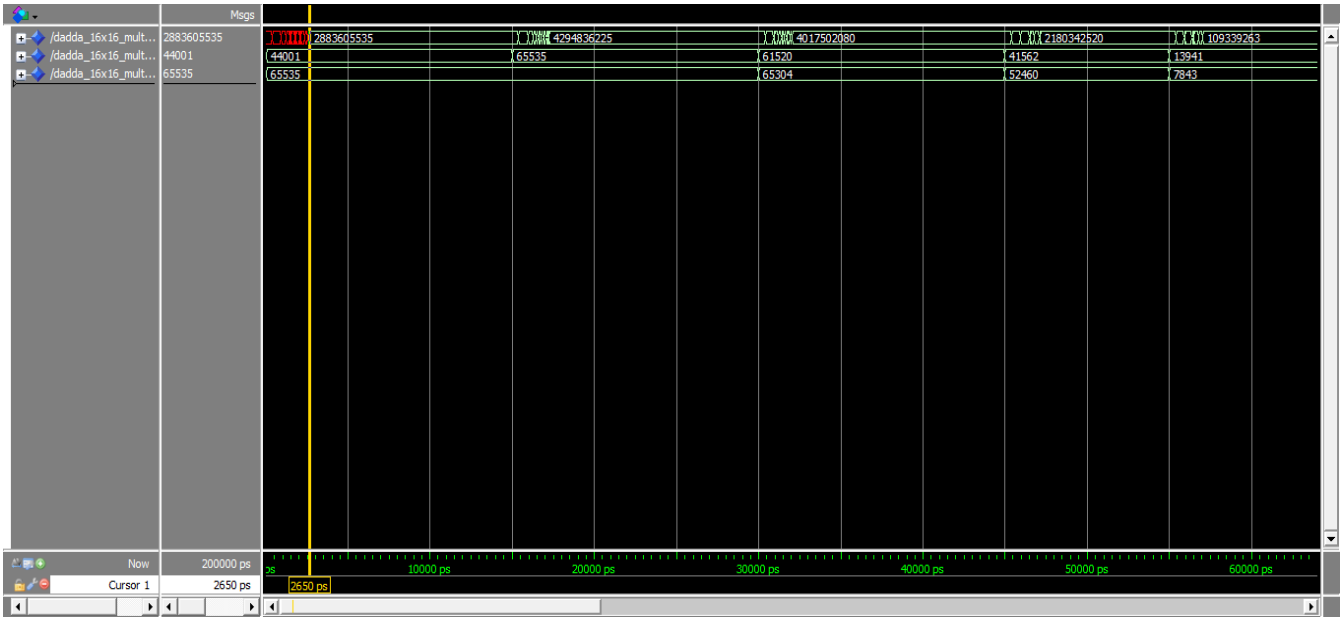
a) Design a Dadda multiplier for unsigned 16x16 bit multiplication with a Brent Kung adder for the final addition. Write its hardware description in synthesizable VHDL (without delays) and show its correct working using a test bench with appropriate test vectors.Critical path diagram:

Case1: Worst case delay input output: In this case delays are attached only in brent-kung code only. No delays in Half adder, Full adder, Dadda code.

Single input-output to see maximum delay: in this case input is show in decimal format. In next case same input is shown in hexadecimal format.

Over all delay = 2650 ps

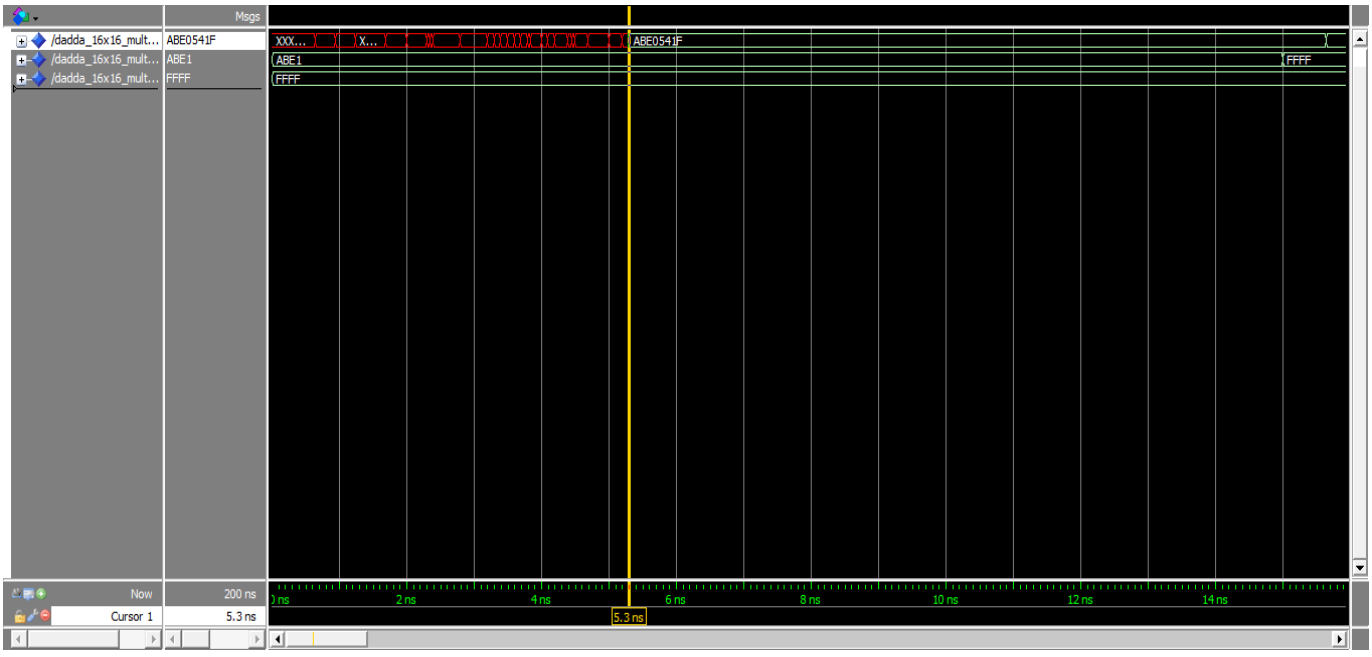
For multiple input-output:



b) Now back annotate the delays for costituent components and re-simulate the cir-cuit. What is its critical path? In how much time can you guarantee that the multiplication will be complete?

Case2: Worst case delay input output: In this case delays are attached with Half adder, Full adder, Dadda code also.

Single input-output to see maximum delay: In this case input is shown in hexadecimal format. It is the same input as used in above case.



For multiple input-output:

Over all delay = 5300 ps

- So over all multiplication will be completed for maximum delay 5300ps as I am getting maximum delay for hex input ABE1 multiplied by FFFF.
- And over all multiplication will be completed theoretically in 5500ps.

- Critical path diagram for dadda multiplier without brent-kung adder.