# INSTRUCTION DECODE

## Course Number:

- **CSE 5381/7381 Fall 2015**

## Group D Team Members:


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## Status Report of Instruction Decode

- **Report Submission Date: November 21, 2015**

## A. Milestones and Deliverables with Summary of Progress

| Phase | Milestone | Deliverable | Summary of Progress |
|---|---|---|---|
| I | 10/31 | Register file and decoder: start tests | - |
| II | 11/7 | Register file and decoder: pass tests | Register File – Start Design<br>Other Hardware Components – Start Design |
| III | 11/14 | Decode Instruction: start tests | Mips Software with Mars Tool – Start Design |
| IV | 11/21 | Decode Instruction: pass tests<br>Intermediate status report | Register File – End Design<br>Mips Software – End Design<br>Intermediate Status Reports |
| V | 11/28 | Read and write from registers in register file: start tests | |
| VI | 12/5 | Read and write from registers in register file: pass tests | |
| VII | 12/12 | Final project report due | |

Note: As of now, we are sticking to the original design and team duties. We did have some doubts regarding the hardware design, but they were all resolved after some discussion with the client, i.e. Dr. Manikas.

However, we did make some changes in the initial proposal plan. In the original plan, we planned to have the testing phase in between the hardware and software design, which we later realized go hand in hand. And, the testing can only be performed after both of them have been substantially developed and later integrated.

As of now, we haven't had any challenges or major difficulties. We use GroupMe for Textual group Communication and Trello for Checklists and Task Management. We have completed 3 phases of our project. The penultimate phase will be the integration testing and unit testing. And the final phase will be the Project Report.

The current progress of the software development component is described as follows. Software was written in MIPS assembly language, and was compiled and run using the MARS tool. It was then given, in its binary format, to the test engineers to test its execution using the hardware built to simulate instruction decode. Two programs have been written so far. One was written with a few very basic operations to make sure that the ID hardware effectively decodes the formats, operations, and registers of the instructions, and the other contains Fibonacci code. The Fibonacci code in the file ***'Fibonacci.asm'*** is what will be used to test the completed product, so this is the ultimate goal that we are moving toward. Accurate decoding of the first program will be completed before the Fibonacci code is attempted. The code for that first program is attached with the the Project Status Report, in a file called ***'Mips_Code1.asm'*** The Verilog File for Hardware Implementation: ***'register_file.v'*** has also been attached with this Project Status Report.

## B. Revised Schedule of Upcoming Milestones and Deliverables

| Phase | Milestone | Deliverable |
|---|---|---|
| **VI** | 11/28 | Hardware Design - 2nd Pass<br><br>Hardware Testing(Read and Write From Registers) – Start<br><br>Software Testing – Start |
| **VII** | 12/5 | Software Testing – Complete<br>Hardware Testing – Complete<br>Unit Testing – Complete<br>Integration Testing – Complete |
| **VIII** | 12/12 | **Project Report Submission** |

**11/28] Phase VI –** By, this phase, we will have enough units and components designed and integrated to begin performing designed tests with test cases on both the software and the Hardware Components

**12/5] Phase VII –** By, this time, we will be done with testing the individual components, i.e. (Unit Testing) and also the integrated Instruction Decoding Unit (Integration Testing) other than the regular Software and Hardware Tests.

**12/12] Phase VIII -** By this time, Our Instruction Decoding Unit would not only be complete and ready for use, but our Project Report about the same will also be completed.