INSTRUCTION DECODE

William O'Connor – Abdullah Albadri – Vivek Sanghi Jain – Manas Churi – Simin Wang – Ling He

CSE 7381 FALL 2015 10/31/15

A. General Project Description

During the Instruction Decode (ID) stage, which, as the name suggests, is used to decode instructions, input from the IF stage is fetched, its instruction format is calculated looking by at the first 6 bits, and the instruction is then decoded to decide what an instruction does, including storing the register values in temporary registers as desired. It is this stage when the processor decides the instruction format, chooses the operation to be performed (Add, Subtract, etc.) and gets the register values ready for next stage (EX stage). For example, if you have an add instruction that adds the contents of register 1 and 2, and places the result in a register, then the values of register 1 and 2 need to be fetched to perform the addition. However, for an addi operation, you fetch one register, and you sign-extend an immediate value and those two values are added. The CPU must know when it sees an add instruction to get two values from the registers, but when it sees an addi instruction, it must get the value from one register and a sign-extended immediate value. This is the overall idea of decoding an instruction.

We plan to use a Register File, Sign-Extend and Immediate and a copy of NPC and IR Registers. Instruction Decode takes the Instruction passed on to it from the Instruction Fetch Stage and then it decodes all the fields in the instruction (like the op,rs,rt,etc.)

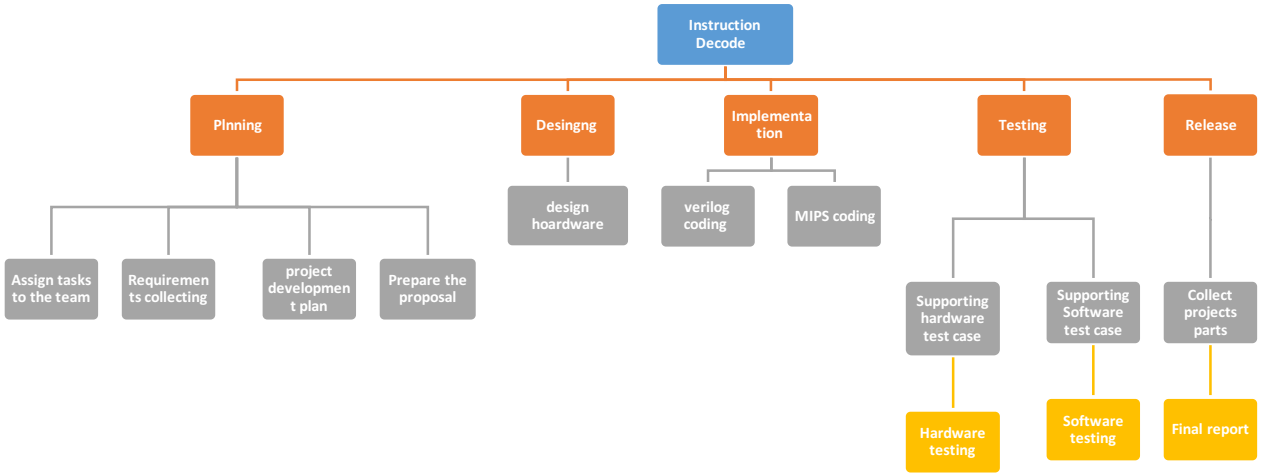
One more function that the Instruction Decode Unit will be performing is extending the 16-bit constant value in certain instructions to a 32 bit number so that operations can be performed on it.

Using Verilog we will develop the Instruction Decode stage of the MIPS pipeline. This will include development of the register file and other related components. We will use the Fibonacci machine code for testing this stage. We plan to develop supporting hardware and software to test the operation of this stage, including the development of the register file and decoder, decoding the instructions themselves, and reading and writing from registers.

B. Specific Implementation Plan

Our team, *"Team-D"*, consists of 6 members. In this project, we will practice how to work as a team to achieve a common goal. Every team member has been assigned a specific role, but we plan to contribute with each other in order to accomplish our tasks and improve our knowledge by learning different concepts and skills from each other. This is a good opportunity to learn how to manage a team project and follow the instructions of a team leader.

In this project we will learn how design, code, and test computer architecture components. We will practice Verilog tools to simulate an industrial working environment.



There are five parts of this project to complete.

1. The first function is to distinguish illegal instruction. If a fetched instruction is not R-type, I-type or J-type, it will raise an error. Even if type of this instruction is distinguished, we should still check whether the instruction can be recognized.

2. The second function is to determine the type of instruction. Before we decode it, we need to determine its format, so we can know meaning and domain of a field.

3. The third function is to figure out what kind of instruction this is and what would be the output of the corresponding opcode to ALU. For eg. We should know whether it is sub operation, an XOR operation, add or something else in this stage.

4. The forth function is to sign-extend immediate values and read values from registers.

5. The last part is to finish related part which is necessary to test. For example register file, ALU port, IF port and etc.

The project will be implemented in 5 phases:

i. Planning

This is the first stage of any project development. In this phase we will collect the project requirements, assign tasks to each member based on individual strength, develop the project plan for execution and prepare the project proposal.

ii. Designing

We will write down the logic and initiate the design process beginning with the block diagram for those logics. Then, we verify if the logic we are looking for, fits perfectly in the diagram and then proceed to the next step.

iii. Implementation

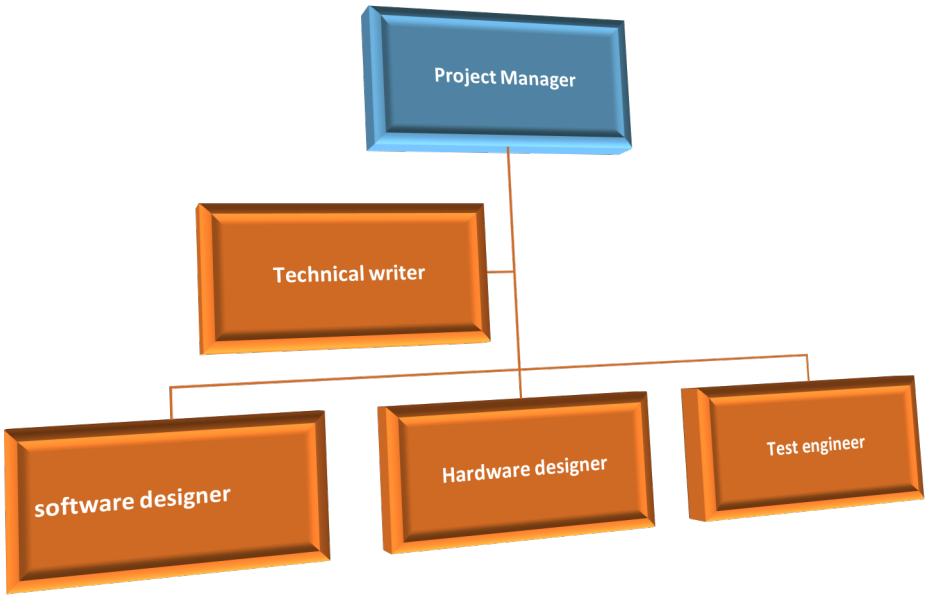
In the implementation phase, we will use Verilog tools for designing the logic which was established from previous stage and cover all the components required for ID stage from the block diagram.

iv. Testing

In the testing phase; we plan to prepare supporting test cases for hardware and software and some test scenarios, after which we will test our project code and components.

v. Release

Finally, we will collect and coalesce the contributions from all team members to prepare the final project release and final report with full documentation.



C. Milestones & Deliverables

Milestone	Deliverable
10/31	Register file and decoder: start tests
11/7	Register file and decoder: pass tests
11/14	Decode Instruction: start tests
11/21	Decode Instruction: pass tests Intermediate status report
11/28	Read and write from registers in register file: start tests
12/5	Read and write from registers in register file: pass tests
12/12	Final project report due

D. Team Roles & Responsibilities

Role	Member 1	Member 2
Project Manager	Vivek Sanghvi Jain	
Technical Writer	Manas Churi	Abdullah Albadri
Software Designer	William O'Connor	
Hardware Designer	Ling He	Manas Churi
Test Engineer	Abdullah Albadri	Simin Wang

#	Roles	Responsibilities
1	**Project Manager**	• Review and approve all project deliverables (Initiation Plan, Detailed Plan, Testing etc.) • Provide overall project oversight and work with Software and Hardware Designers to keep project on track. • Work with Test Engineers to ensures that the project passes all test cases
2	**Technical Writer**	• Produces all required documentations • Collaborates with other software and hardware designers and compose technical
3	**Software Designer**	• Develop MIPS Code to perform Instruction Decoding and all the aspects that it encompasses
4	**Hardware Designer**	• Design any and all required Hardware Components • Develop Hardware Design with help of Verilog
5	**Test Engineer**	• Design Test Cases and Test Benchmarks according to Requirements. • Collaborate with Hardware and Software Designers to ensure that both the software and hardware components of the project meets all the said requirements.

E. References

[1] Fetch, Execute, Decode [Online]
Available:
http://www.cs.umd.edu/class/sum2003/cmsc311/Notes/CompOrg/fetchDecode.html

[2] Synthesis Lectures on Computer Architecture : Processor Microarchitecture - Antonio Gonzalez, Fernando Latorre [Online]
Available::
http://site.ebrary.com.proxy.libraries.smu.edu/lib/smulibraries/detail.action?docID=10530769

[3] Project Team Member Roles and Responsibilities
Available:
https://sp.princeton.edu/ipp/templates/Documents/Project%20Team%20Member%20Roles%20and%20Responsibilities.docx