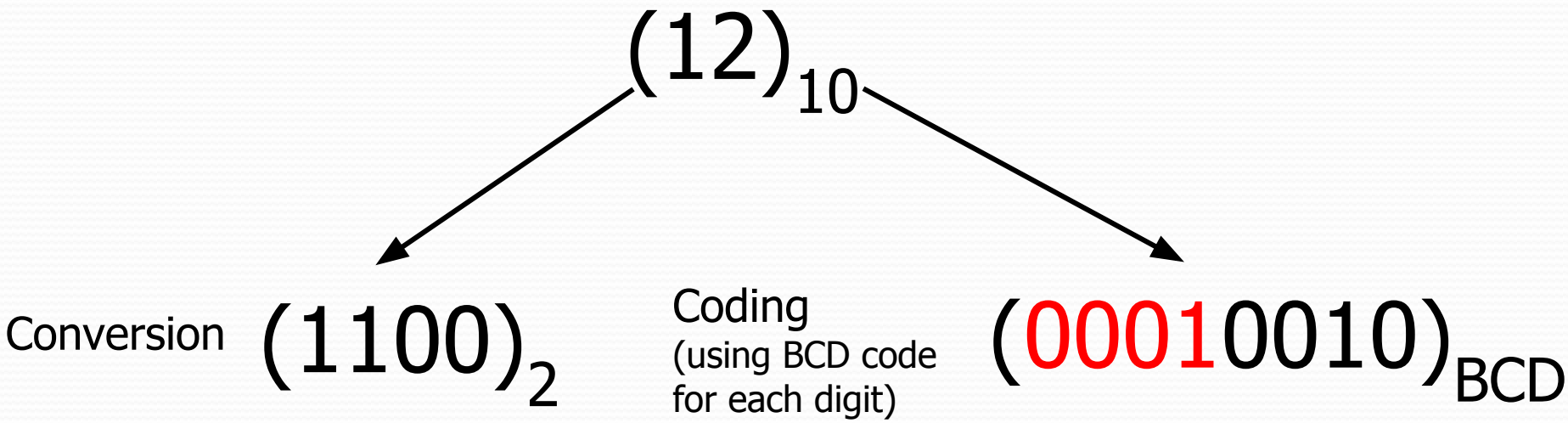
Conversion and Coding



BCD Adder

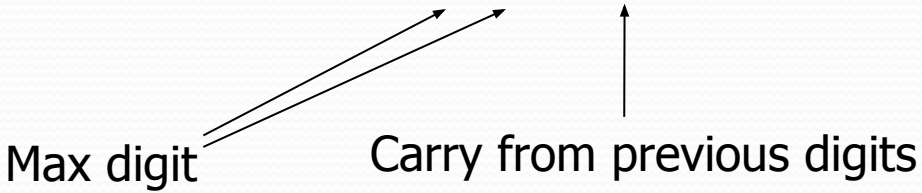
Design a circuit that calculates the Arithmetic addition of two decimal digits.

$$\begin{array}{rr} & 9 \\ + & 3 \\ \hline 1 & 2 \end{array}$$

carry

BCD Adder

- Maximum sum is 9+9 + 1 = 19



BCD adder (sum up to 9)

Number	C	S3	S2	S1	S0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1

The sum is the same with BCD adder

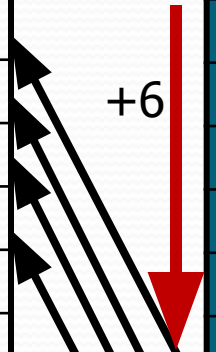
BCD adder (sum is 10 to 19)

Number	C	S3	S2	S1	S0
10	1	0	0	0	0
11	1	0	0	0	1
12	1	0	0	1	0
13	1	0	0	1	1
14	1	0	1	0	0
15	1	0	1	0	1
16	1	0	1	1	0
17	1	0	1	1	1
18	1	1	0	0	0
19	1	1	0	0	1

BCD adder (sum is 10 to 19)

BCD adder sum

Number	C	S3	S2	S1	S0
10	1	0	0	0	0
11	1	0	0	0	1
12	1	0	0	1	0
13	1	0	0	1	1
14	1	0	1	0	0
15	1	0	1	0	1
16	1	0	1	1	0
17	1	0	1	1	1
18	1	1	0	0	0
19	1	1	0	0	1



Binary sum

K	Z3	Z2	Z1	Z0
0	1	0	1	0
0	1	0	1	1
0	1	1	0	0
0	1	1	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	0	0
1	0	0	0	1
1	0	0	1	0
1	0	0	1	1

Algorithm for BCD Adder

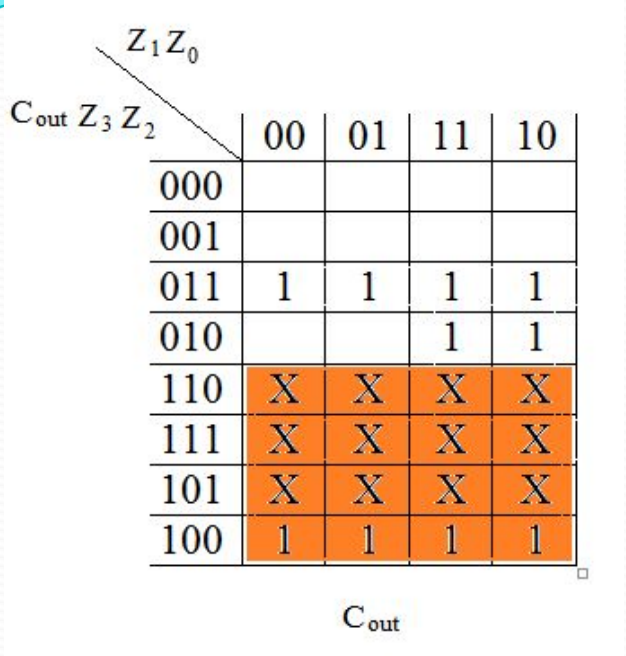
- If sum is up to 9
  - Use the regular Adder.
- If the sum > 9
  - Use the regular adder and **add 6** to the result

When is the result > 9

Binary sum

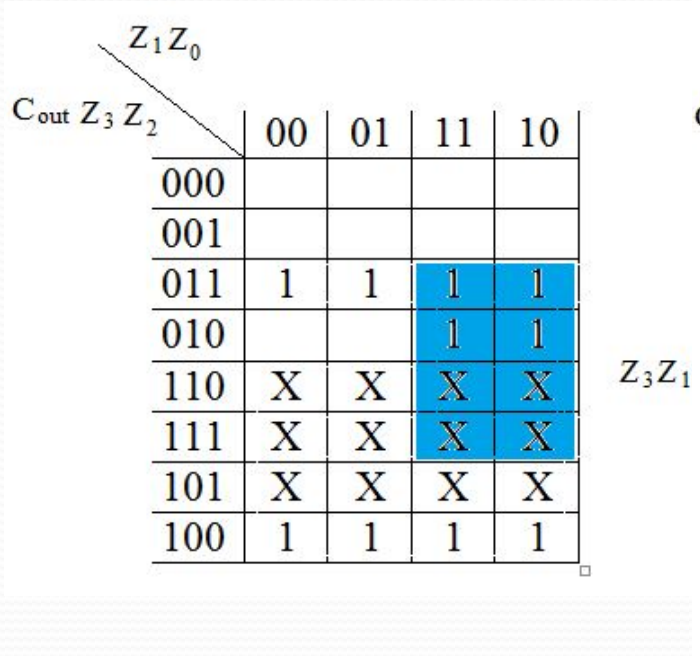
Number	Correction	C_{out}	Z3	Z2	Z1	Z0
10	1	0	1	0	1	0
11	1	0	1	0	1	1
12	1	0	1	1	0	0
13	1	0	1	1	0	1
14	1	0	1	1	1	0
15	1	0	1	1	1	1
16	1	1	0	0	0	0
17	1	1	0	0	0	1
18	1	1	0	0	1	0
19	1	1	0	0	1	1

$C_{out} Z_3 Z_2$ \ $Z_1 Z_0$	00	01	11	10
000				
001				
011	1	1	1	1
010			1	1
110	X	X	X	X
111	X	X	X	X
101	X	X	X	X
100	1	1	1	1



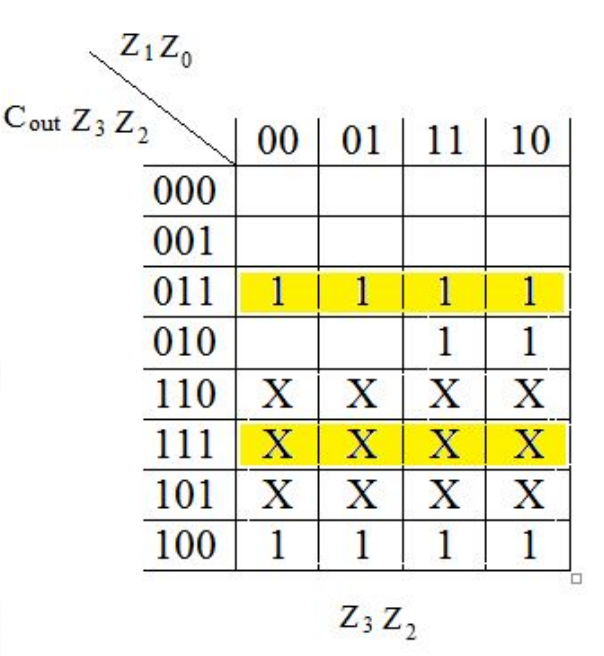
$C_{out}\ Z_3\ Z_2$ \ $Z_1 Z_0$	00	01	11	10
000				
001				
011	1	1	1	1
010			1	1
110	X	X	X	X
111	X	X	X	X
101	X	X	X	X
100	1	1	1	1

C_{out}



$C_{out}\ Z_3\ Z_2$ \ $Z_1 Z_0$	00	01	11	10
000				
001				
011	1	1	1	1
010			1	1
110	X	X	X	X
111	X	X	X	X
101	X	X	X	X
100	1	1	1	1

$Z_3 Z_1$

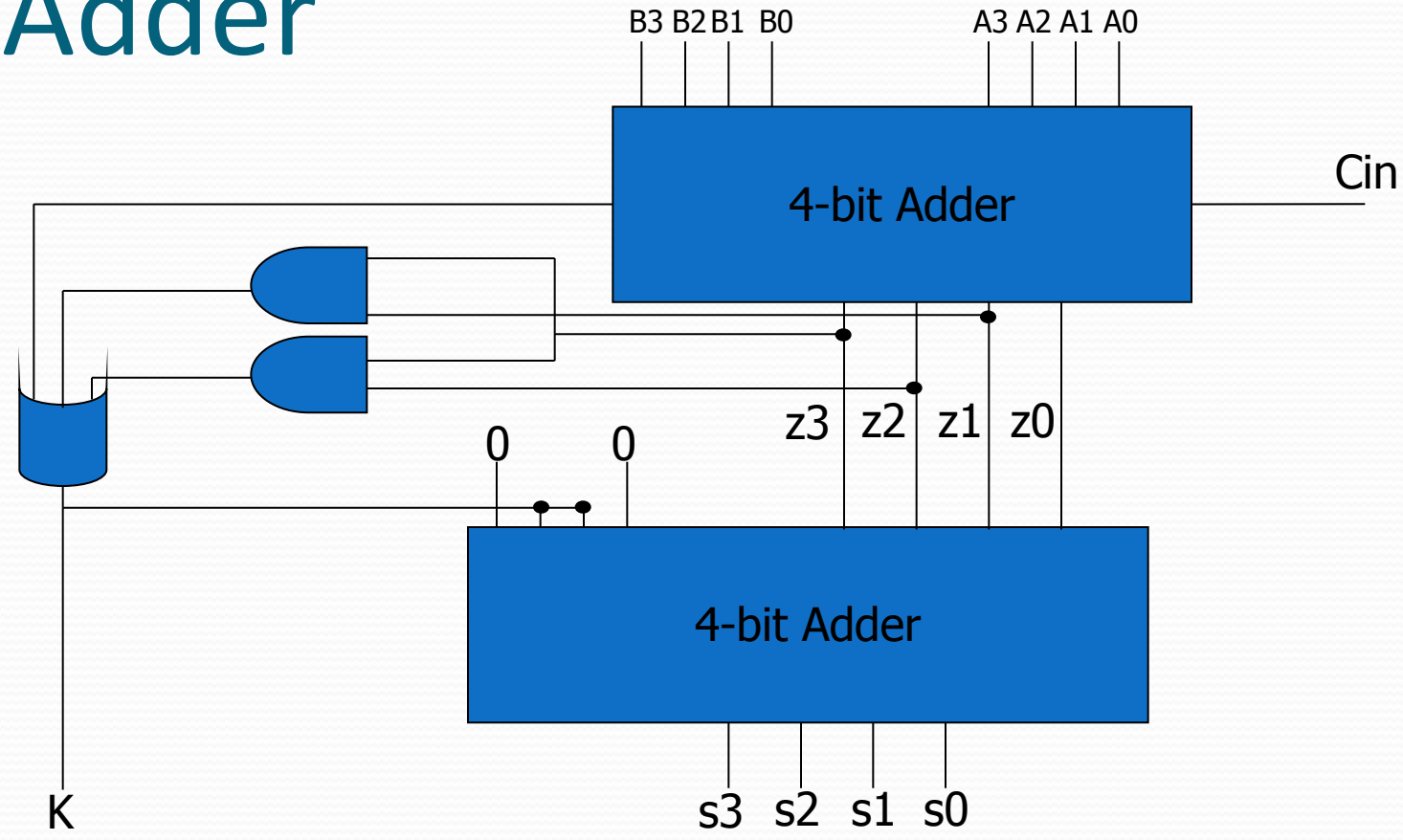


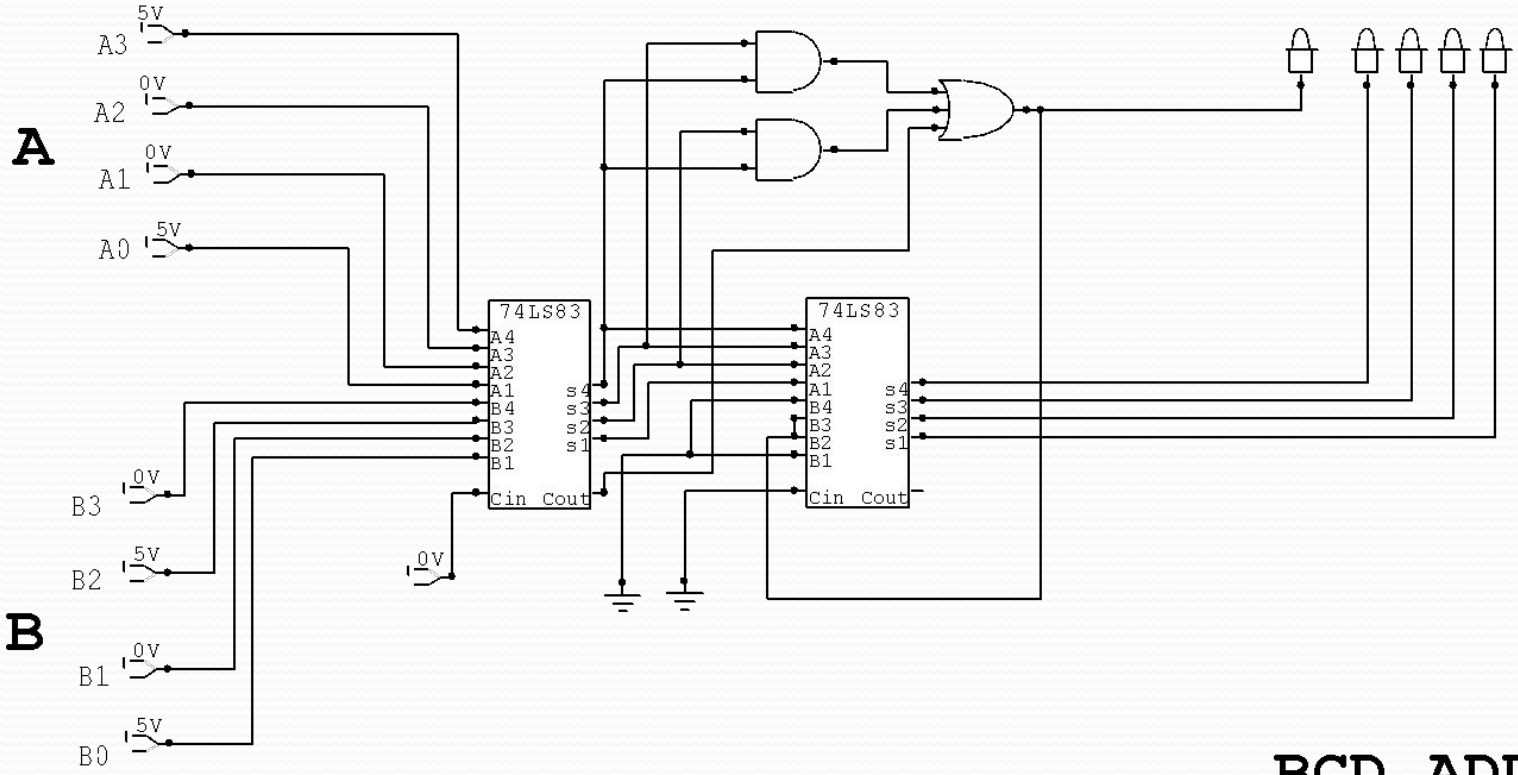
$C_{out}\ Z_3\ Z_2$ \ $Z_1 Z_0$	00	01	11	10
000				
001				
011	1	1	1	1
010			1	1
110	X	X	X	X
111	X	X	X	X
101	X	X	X	X
100	1	1	1	1

$Z_3 Z_2$

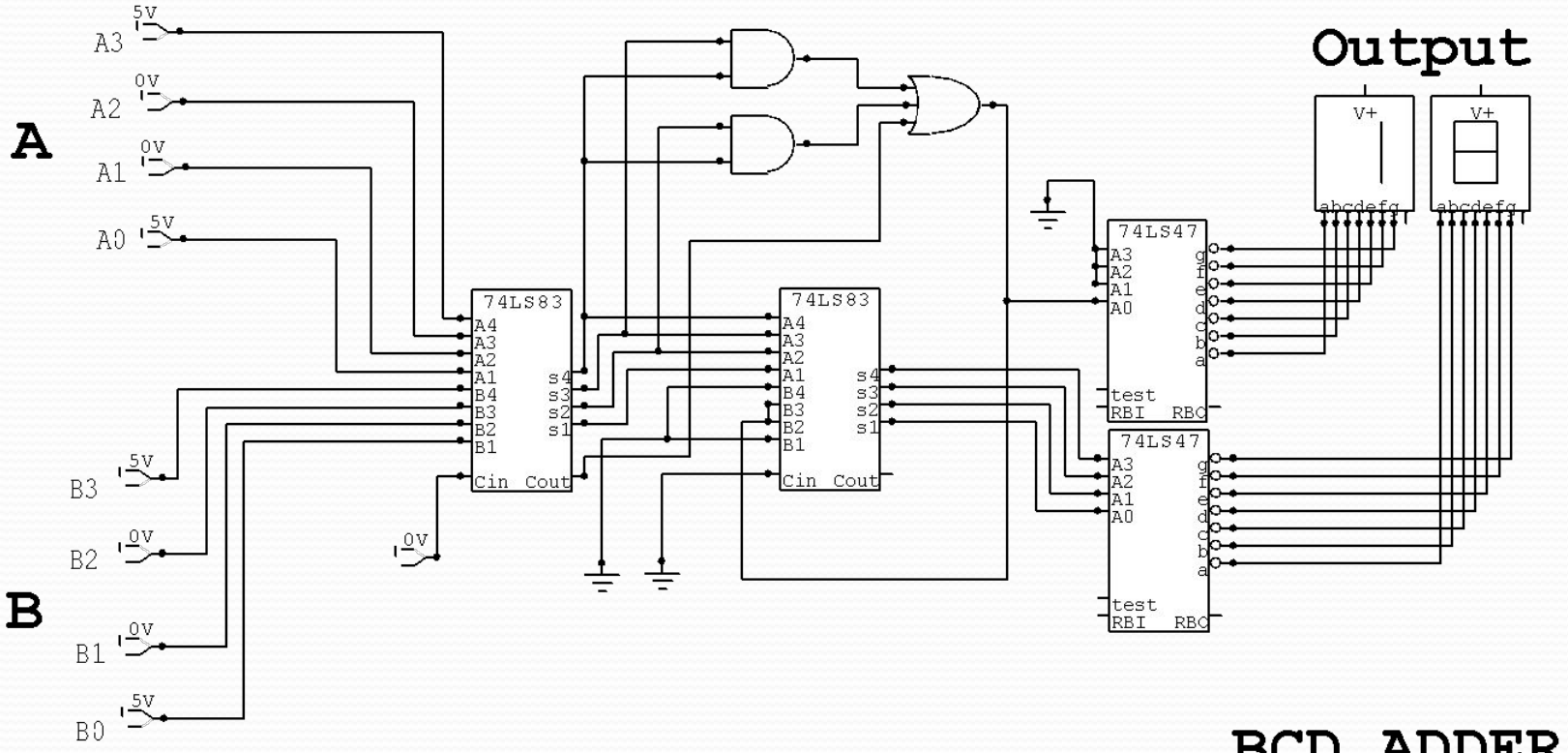
Correction = $C_{out} + Z_3Z_1 + Z_3Z_2$

BCD Adder


B3 B2 B1 B0
A3 A2 A1 A0
4-bit Adder
Cin
z3 z2 z1 z0
0 0
4-bit Adder
K
s3 s2 s1 s0


A
A3
A2
A1
A0
5V
0V
0V
5V
B
B3
B2
B1
B0
0V
5V
0V
5V
74LS83
A4
A3
A2
A1
B4
B3
B2
B1
Cin
Cout
s4
s3
s2
s1
74LS83
A4
A3
A2
A1
B4
B3
B2
B1
Cin
Cout
s4
s3
s2
s1
0V

BCD ADDER


A
A3
A2
A1
A0
5V
0V
0V
5V
B
B3
B2
B1
B0
5V
0V
0V
5V
74LS83
A4
A3
A2
A1
B4
B3
B2
B1
Cin
Cout
s4
s3
s2
s1
74LS83
A4
A3
A2
A1
B4
B3
B2
B1
Cin
Cout
s4
s3
s2
s1
74LS47
A3
A2
A1
A0
test
RBI
RBO
g
f
e
d
c
b
a
74LS47
A3
A2
A1
A0
test
RBI
RBO
g
f
e
d
c
b
a
Output
V+
abcdefg
V+
abcdefg
BCD ADDER