Digital Electronic circuit

EC(EE)302

Analog and Digital Converter

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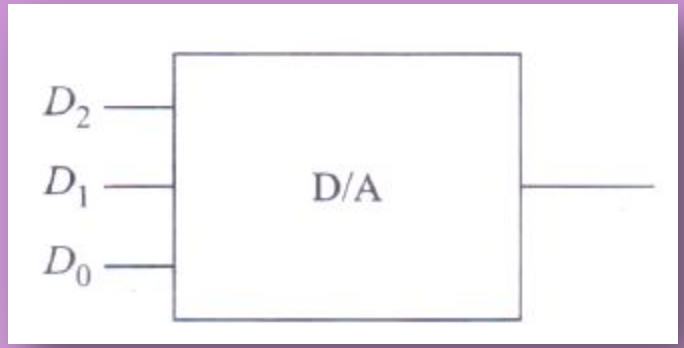


Fig 1: Block Diagram of 3 bit DAC

Let us assume the output analog signal is in the range of 0 to 1V and the input combinations are 000 to 111. Its equivalent analog is given in Table 1 and the relation between the digital signal input and the analog signal output is shown in Fig. 2

Table 1: Digital input and its equivalent analog

Digital signal	*Analog signal*
000	0 V
001	1/8 V
010	2/8 V
011	3/8 V
100	4/8 V
101	5/8 V
110	6/8 V
111	7/8 V

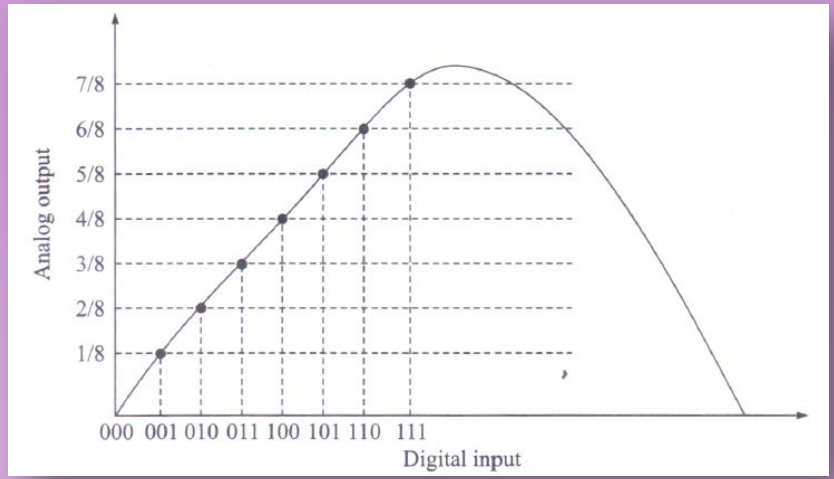


Fig 2: The relation between digital input and analog output

From the above table 1 and Fig. 2,

1. The value of LSB is $\frac{V_m}{2^n}$ 2. The value of second LSB is $\frac{2^1.V_m}{2^n}$

3. The value of n^{th} LSB is $\frac{2^{n-1}.V_m}{2^n}$ 4. Full scale output = V_m - Value of LSB

where *n is the number of bits of a digital signal and* V_m *is the maximum amplitude.* The output analog voltage V_A *is*

$$V_A = \frac{V_m\left[V_{D0}2^0 + V_{D1}2^1 + V_{D2}2^2 + \ldots\ldots + V_{Dn-1}2^{n-1}\right]}{2^n}$$

Example 1: ***Calculate the values of the LSB, MSB, and the full-scale output*** for an 8-bit DAC for 0 to 10 V analog output range.

Solution

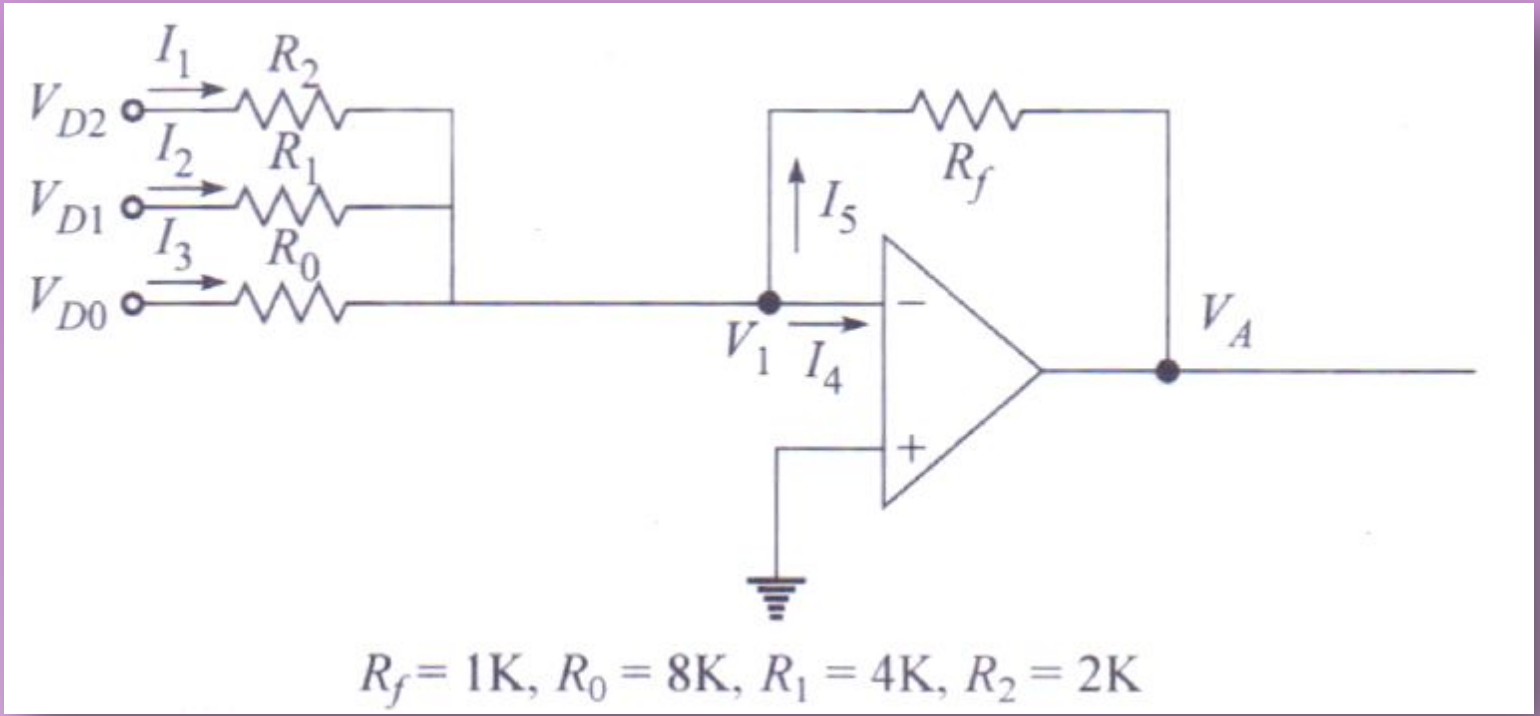
Given data: $n = 8,\ V_m = 10\ V$

$$\text{Value of LSB} = \frac{V_m}{2^n} = \frac{10}{2^8} = \frac{10}{256} = 0.039V$$

$$\text{Value of MSB} = \frac{2^{n-1}.V_m}{2^n} = \frac{2^7.10}{2^8} = \frac{128.10}{256} = 5V$$

Full Scale Output = V_m - *Value of LSB* = *10 – 0.039 = 9.961 V*

Resistor divider DAC



A weighted DAC requires a wide range of resistor values. As the length of binary inputs increases, the range of resistor values needed also increases. For an 8-bit DAC, the larger values of resistor are 128 times the value of the smallest resistor.

Analysis of circuit

Assume the op-amp is ideal. The voltage at the inverting terminal is equal to the voltage at the non-inverting terminal. The input current of op-amp is zero (I_4 =0), since the non-inverting terminal is grounded, $V_1 = O$.

Applying KCL to node 1,

$$I_1 + I_2 + I_3 = I_4 + I_5$$

$$I_1 + I_2 + I_3 = I_5 \qquad \therefore \; Since\, I_4 = 0$$

$$\frac{V_{D2} - V_1}{R_2} + \frac{V_{D1} - V_1}{R_1} + \frac{V_{D0} - V_1}{R_0} = \frac{V_1 - V_A}{R_f}$$

$$\frac{V_{D2}}{R_2} + \frac{V_{D1}}{R_1} + \frac{V_{D0}}{R_0} = -\frac{V_A}{R_f} \qquad \therefore Since\, V_1 = 0$$

$$V_A = R_f\left(\frac{V_{D2}}{R_2}+\frac{V_{D1}}{R_1}+\frac{V_{D0}}{R_0}\right) \qquad \text{[taking only the magnitude]}$$

Assume $V_{D2} = V_{DI} = V_{DO} = V_D = 1V$

For the input 001, the output $\dfrac{V_m}{2^n} = \dfrac{1}{2^3} = \dfrac{1}{8}$

So, $\dfrac{1}{8} = R_f \dfrac{1}{R_0}$

$$\boxed{R_0 = 8R_f}$$

For the input 010, the output $\dfrac{2^1.V_m}{2^n} = \dfrac{2}{2^3} = \dfrac{1}{4}$

So, $\dfrac{1}{4} = R_f \dfrac{1}{R_1}$

$$\boxed{R_1 = 4R_f}$$

For the input 100, the output $\frac{2^2.V_m}{2^n} = \frac{4}{2^3} = \frac{1}{2}$

So, $\frac{1}{2} = R_f \frac{1}{R_2}$

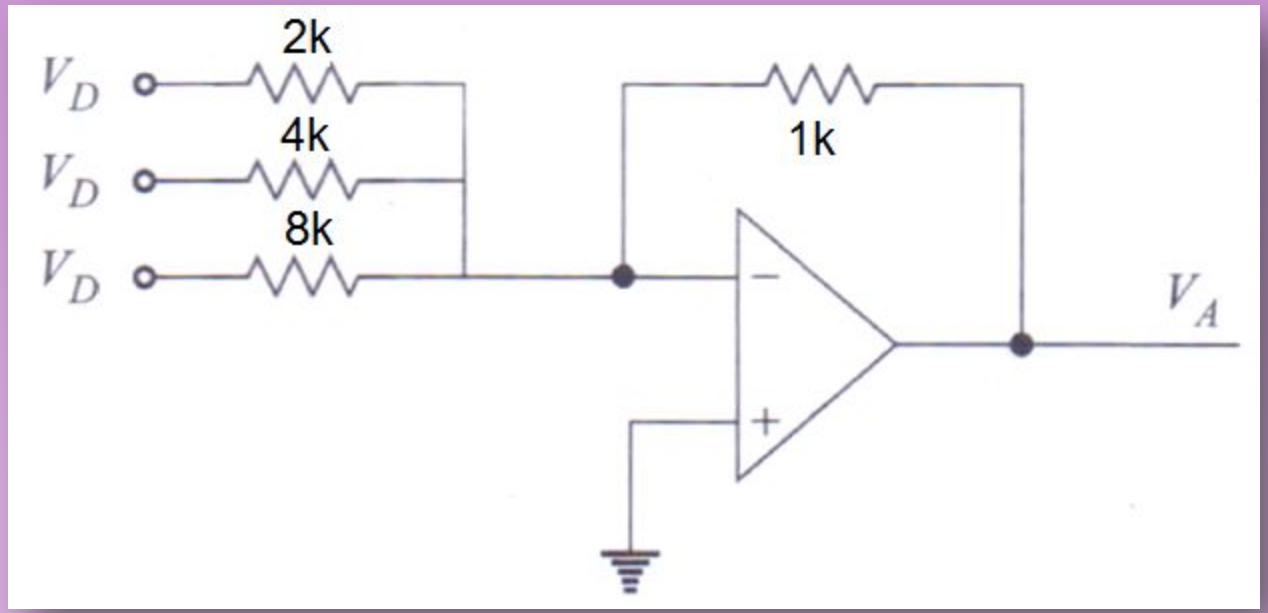
$$\boxed{R_2 = 2R_f}$$

If $R_f = 1k$

then $R_0 = 8k$

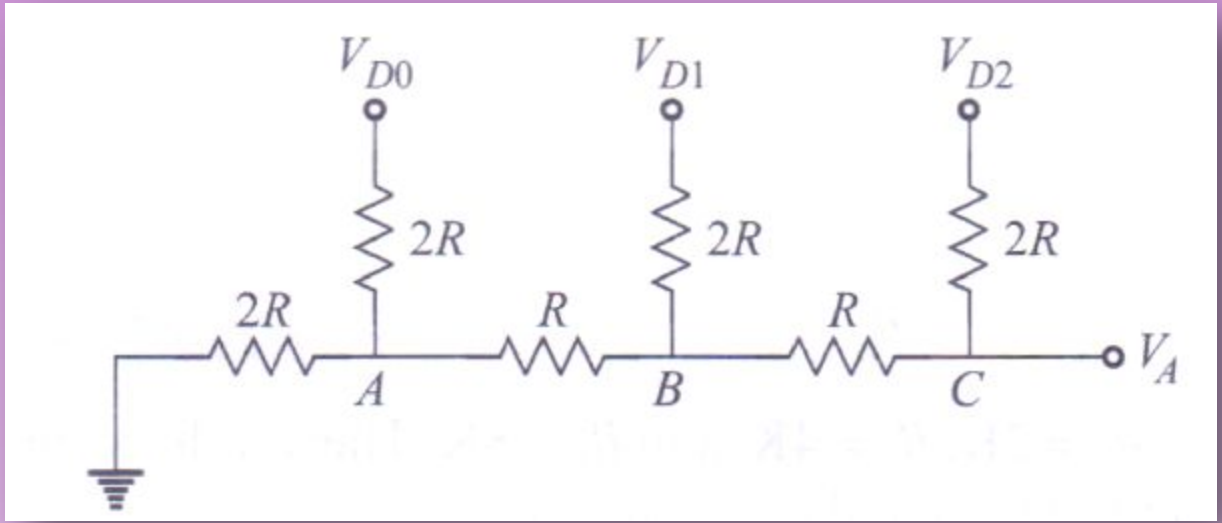
$R_1 = 4k$

and $R_2 = 2k$



R/2R ladder network DAC

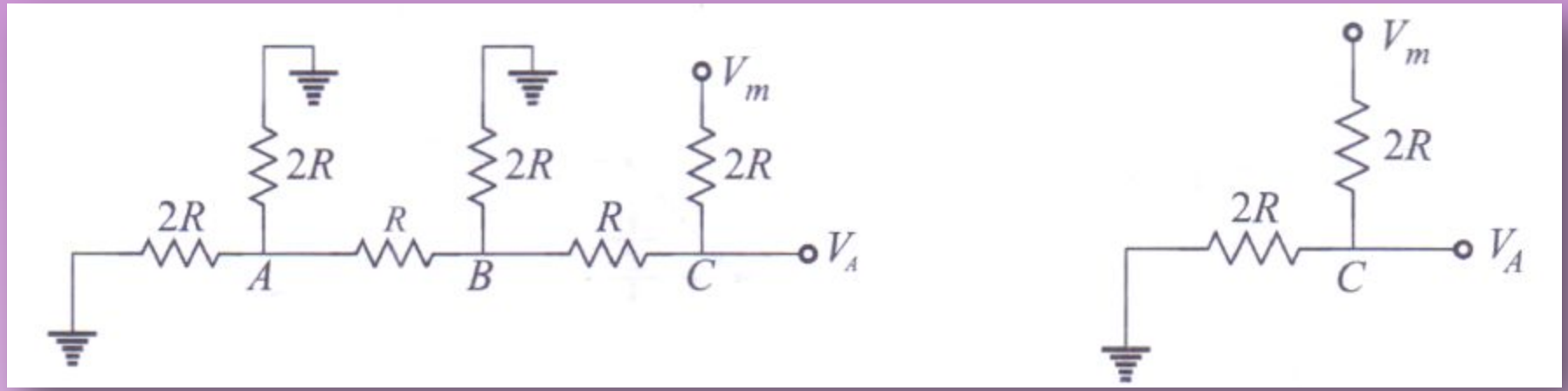
The major drawback of a resistor divider DAC is the requirement of a wide range of resistor values. In contrary, R-2R ladder DAC uses only two resistor values, i.e. R and 2R. The R/2R ladder network is shown in Fig.



In Fig, V_{D2}, V_{DI} *and* V_{DO} *are the 3-bit digital inputs voltage levels and* V_A *is* the analog output.

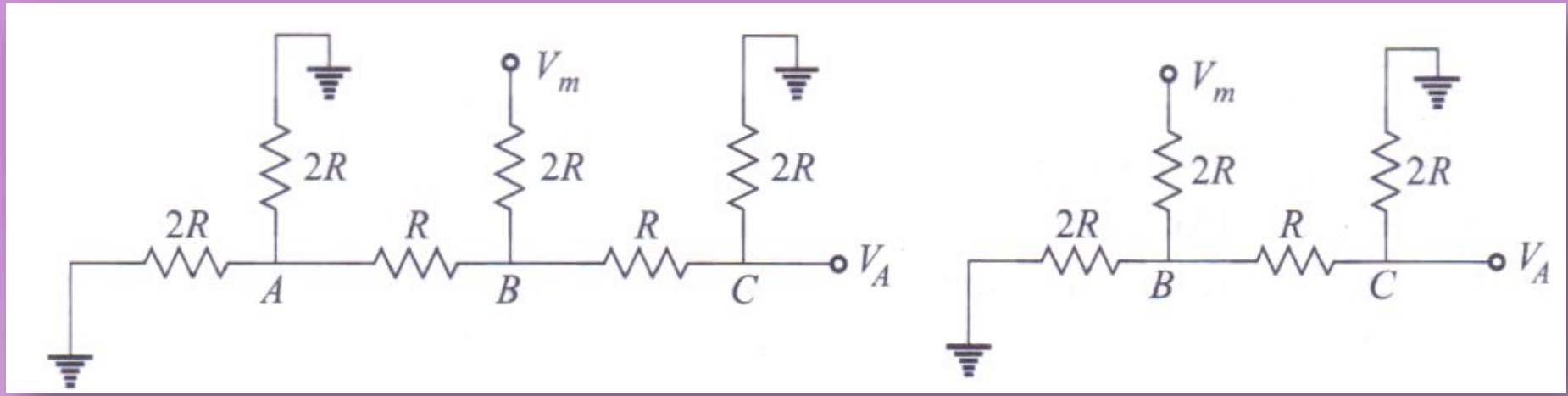
Analysis

Let us assume the voltage corresponding to logic level 1 is V_m. For the digital input 100, the circuit diagram of R/2R ladder network is shown in Fig. 1(a) and its equivalent circuit is shown in Fig. 1(b). For the digital input signal 100, the output analog voltage is,

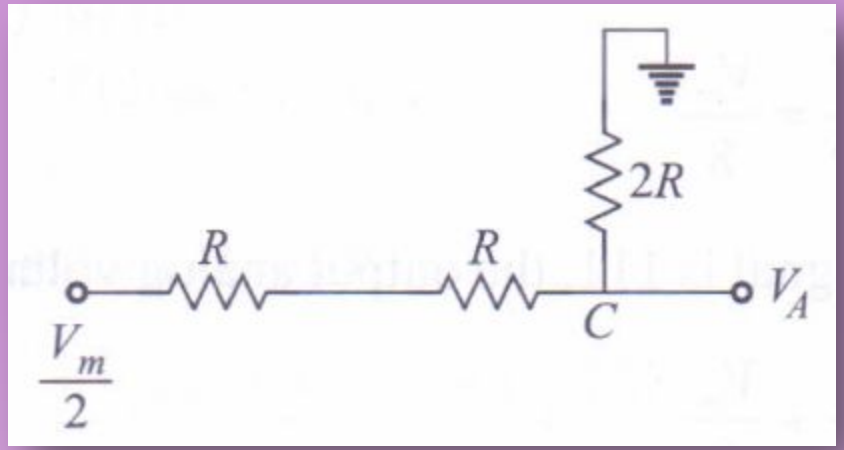


$$V_A = \frac{V_m \times 2R}{2R + 2R} = \frac{V_m}{2}$$

For the digital input 010, the circuit diagram of *R/2R ladder network is shown* in Fig. 2(a) and its equivalent circuit is shown in Fig. 2(b).



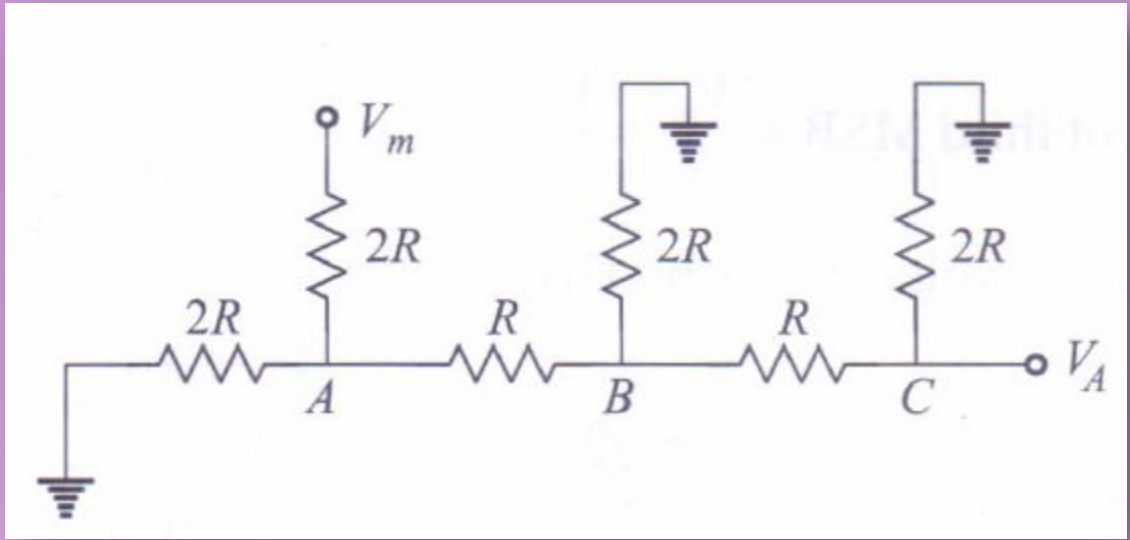
The left-hand side network of node *B is replaced with its Thevenin' s equivalent* and it is shown in Fig. 2(c).



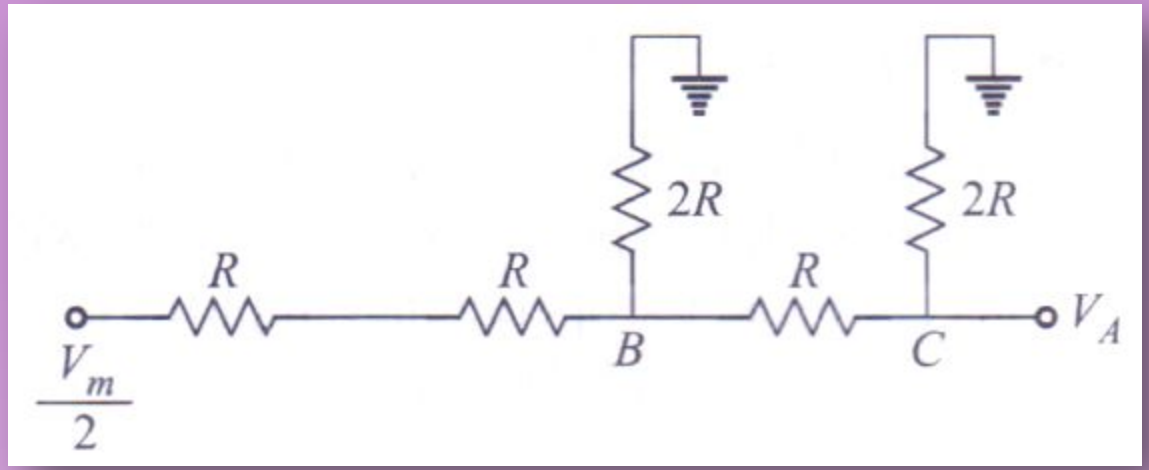
For the digital input signal 010, the output analog voltage is,

$$V_A = \frac{V_m}{2} \times \frac{2R}{2R+2R} = \frac{2V_m}{8} = \frac{V_m}{4}$$

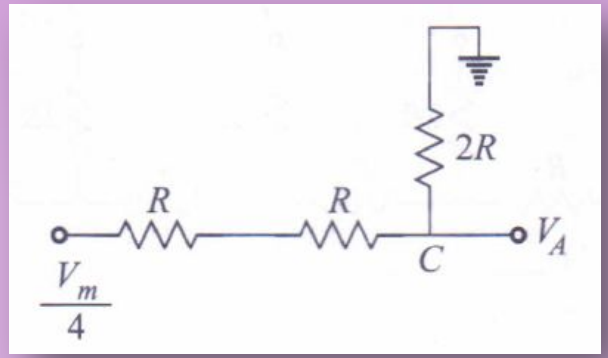
For the digital input 001, the circuit diagram of R/2R ladder network is shown in Fig. 3(a).



The left-hand side network of node A is replaced with its Thevenin' s equivalent and it is shown in Fig. 3(b).



The left-hand side network of node B is replaced with its Thevenin's equivalent and it is shown in Fig. 3(c).



For the digital input signal 001, the output analog voltage is,

$$V_A = \frac{\frac{V_m}{4} \times 2R}{2R + 2R} = \frac{V_m}{8}$$

When the applied signal is 111, the output analog voltage will be,

$$V_m = \frac{V_m}{2} + \frac{V_m}{4} + \frac{V_m}{8}$$

From the analysis, it is observed that for a 3-bit DAC,

- *The value of MSB* = $V_m/2$
- *The value of second MSB* = $V_m/4 = V_m/2^2$
- The value of third MSB = $V_m/8 = V_m/2^3$

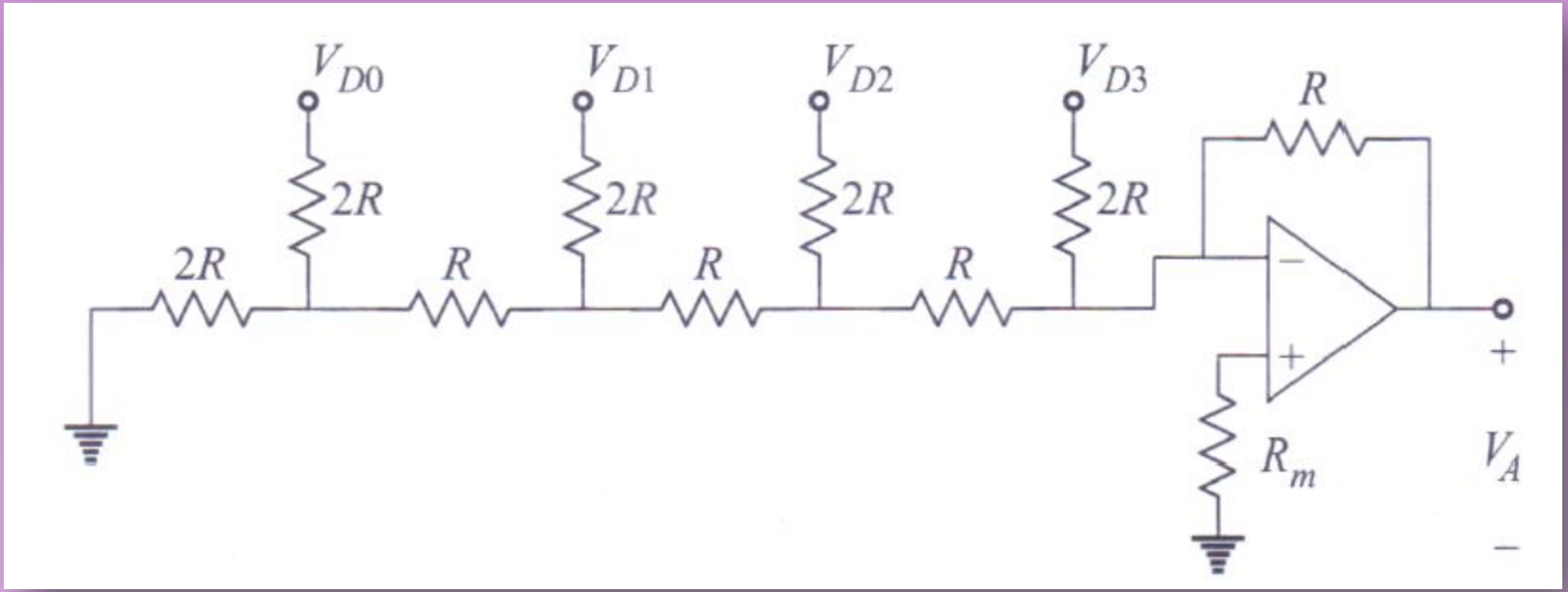
The output analog voltage of n-bit DAC is,

$$V_A = \frac{V_m}{2} + \frac{V_m}{4} + \frac{V_m}{8} + \ldots + \frac{V_m}{2^n}$$

$$= \frac{V_m[V_{Dn-1}\,2^{n-1} \ldots + V_{D3}2^3 + V_{D2}2^2 + V_{D1}2^1 + V_{D0}2^0]}{2^n}$$

where V_{D0}, V_{D1}, V_{D2}, ..., V_{Dn-1} are the digital voltage levels.

The circuit shown in Fig. 1 works as a DAC, under the assumption that load resistance is high. If it is low, the output of ladder network will be an incorrect value. Therefore, it is needed to use the operational amplifier as a buffer to connect the output of ladder network to the load. The circuit of a 4-input DAC with an opamp is shown in Fig.



Specifications of DAC

The specifications of a DAC which are generally specified by the designers are:

- Accuracy
- Resolution
- Linearity
- Settling time
- Temperature sensitivity

Accuracy

It is a measure of how close the actual voltage is to the theoretical output value. **Absolute accuracy defines the maximum deviation of the output from the ideal value**. The accuracy of a DAC depends upon the accuracy of the precision resistor used in the resistor divider or ladder network and the precision of the reference voltage. It is specified as a percentage of full-scale or maximum output voltage.

For example, suppose the theoretical output voltage is 10 V for a full-scale digital input and accuracy is ± 5 percent, it means that the output voltage of DAC for the same digital input lies between 9.5 V to 10.5 V.

The accuracy specifies the maximum error that can occur in a output voltage.
For example, suppose the full-scale output voltage is 10 V and accuracy is ± 0.1 percent, then the maximum error will be 10 mV (i.e. 0.001 x 10 V).

Resolution

It defines the smallest possible change in the output analog voltage due to the change in digital input. The resolution is always equal to the weight of LSB, and it is also known as the *step size. It is a function of the number of bits in the digital input. The* resolution of an *n-bit DAC using divider is* $V_m/2^n$ *and using ladder network, it is* $V_m/2^n$ *in volts.*

Linearity

In a DAC, the relation between digital input and analog output should be linear. That is, an equal increment in the numerical significance of the digital input should result in equal increments in the analog output voltage. Due to the errors in resistor values, the input-output relationship is not linear. The linearity error for a digital input is the difference between the expected voltage and the voltage obtained at the output of DAC.

Settling time

When digital inputs of a DAC change, the analog output does not change instantly. Due to the active and passive elements of the circuit, an oscillation occurs at the output. The time required to settle the output within ± *1/2 LSB of the final value,* after the change in the digital inputs, is referred to as the *settling time,*

Temperature sensitivity

The components used in a circuit of DAC such as resistors, reference voltage source, and op-amp are sensitive to temperature. Due to the change in temperature, the characteristics of an op-amp, the values of resistor and reference voltage may change. Therefore, the analog output voltage for any fixed digital input varies with temperature. This change in values with the temperature is known as the *temperature sensitivity. It is specified in terms of* ± *ppm/°C.*

Example: Find the output voltage of a 4-bit ladder, having the following digital inputs
V_m = 10 V

(a) 1010 (b) 0110
(c) 1001 (d) Full-scale input

Solution

Assume logic 0 = 0V and logic 1 = 10V

$$V_A = \frac{V_m\left[V_{D0}2^0 + V_{D1}2^1 + V_{D2}2^2 + V_{D3}2^3\right]}{2^4}$$

(a) Digital input 1010

$$V_A = \frac{10\left[0\times 2^0 + 1\times 2^1 + 0\times 2^2 + 1\times 2^3\right]}{2^4}$$

$$= \frac{10\left[2+8\right]}{16} = 6.25$$

(b) Digital input 0110

$$V_A = \frac{10\left[0\times 2^0 + 1\times 2^1 + 1\times 2^2 + 0\times 2^3\right]}{2^4}$$

$$= \frac{10[2+4]}{16} = 3.75$$

(c) Digital input 1001

$$V_A = \frac{10\left[1\times 2^0 + 0\times 2^1 + 0\times 2^2 + 1\times 2^3\right]}{2^4}$$

$$= \frac{10[1+8]}{16} = 5.625$$

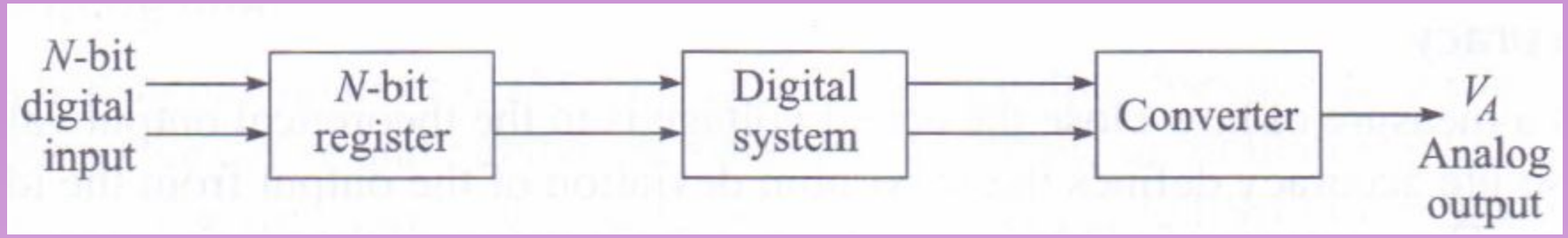
(d) Digital input 1111

$$V_A = \frac{10\left[1\times 2^0 + 1\times 2^1 + 1\times 2^2 + 1\times 2^3\right]}{2^4}$$

$$= \frac{10[1+2+4+8]}{16} = 9.375$$

DAC

Either a ladder or a resistive divider network can be used as a DAC. The complete block diagram of a DAC is shown in Fig.

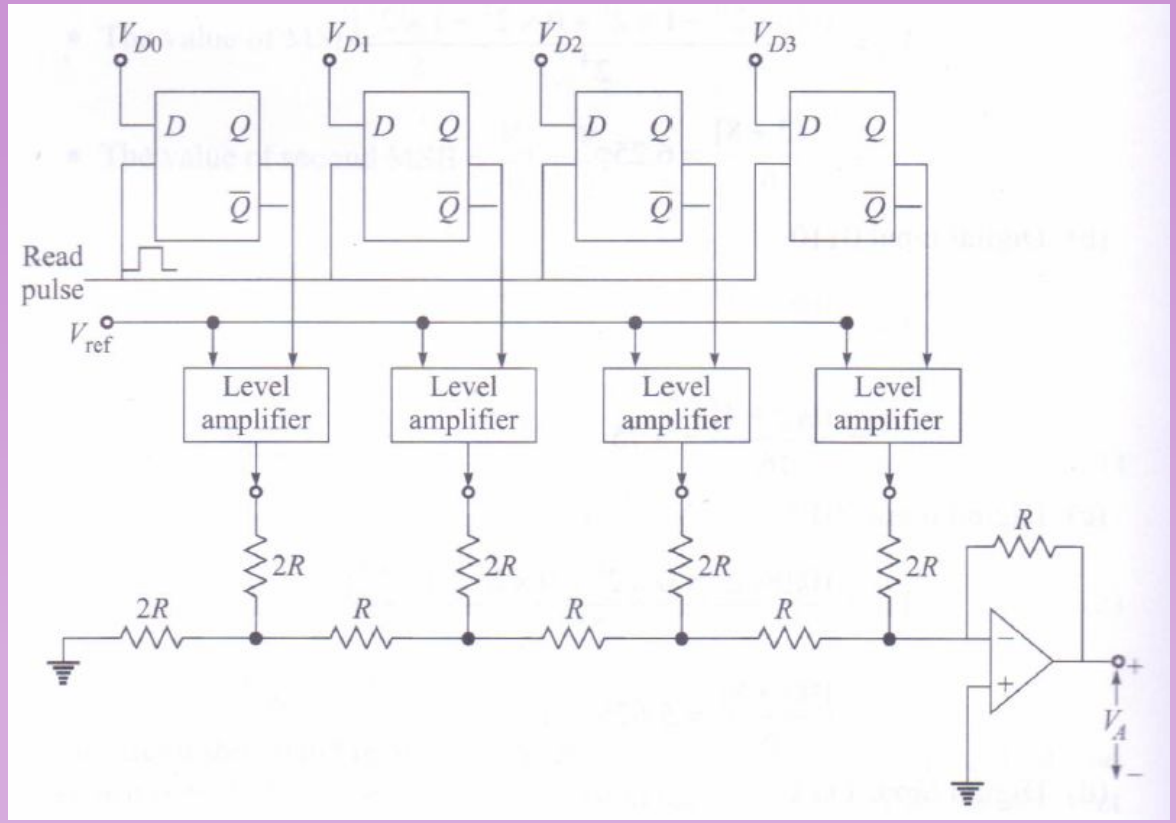


Complete block diagram of DAC

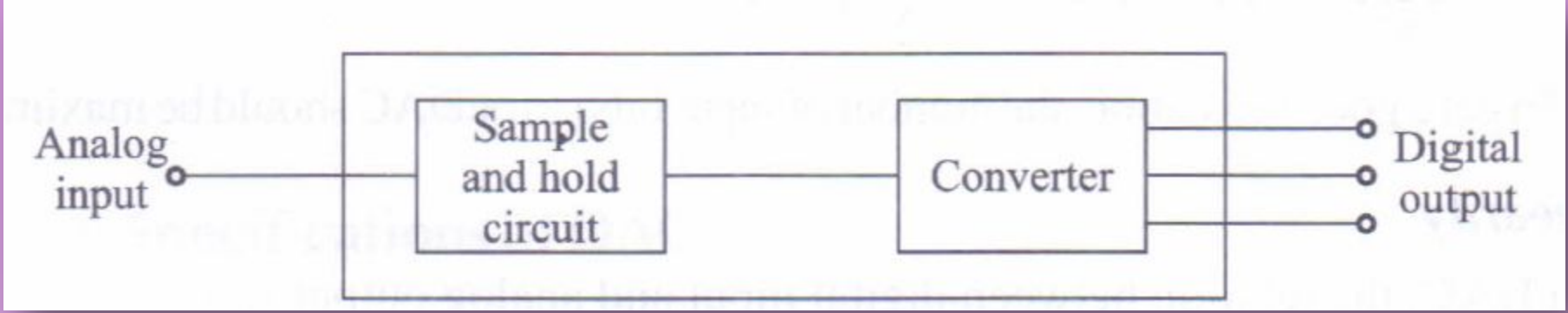
The *N-bit register is used to store the digital information. The D flip-flop can* be used as a basic element of a register. The number of flip-flops define the size of a register, one flip-flop stores l-bit data. Digital data is loaded into a flip-flop with a clock pulse. The output of flip-flop is logic 1 or logic 0, values of logic 1 and logic 0 may not be same.

To provide the same level voltage for logic 1s and logic 0s, the level amplifier are used. The level amplifier has two inputs; one is the reference voltage from an external voltage source and the other input is the output of the flip-flop.

The amplifier works such that, when the input from a flip- flop is high, the output of the amplifier is V_{ref} *and when the input from the flip-flop is low, the output is 0 V.*
The schematic of a 4-bit DAC is shown in Fig.



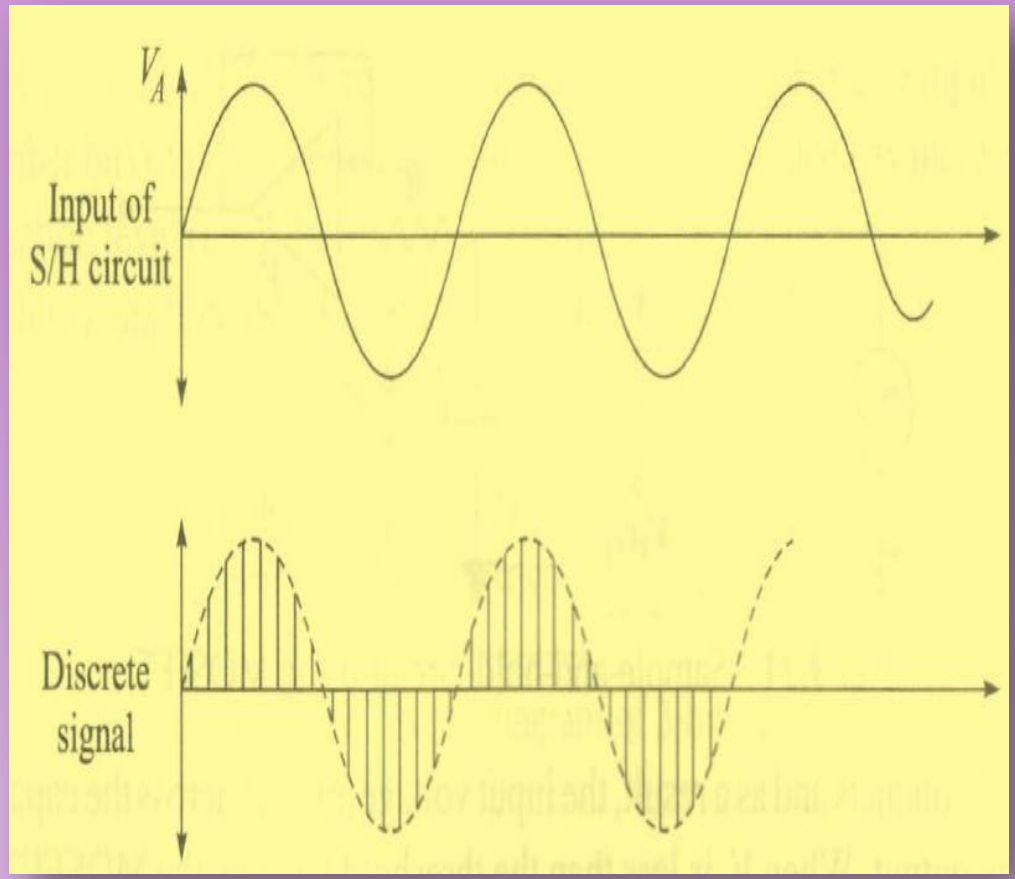
BASIC PRINCIPLE OF ADC



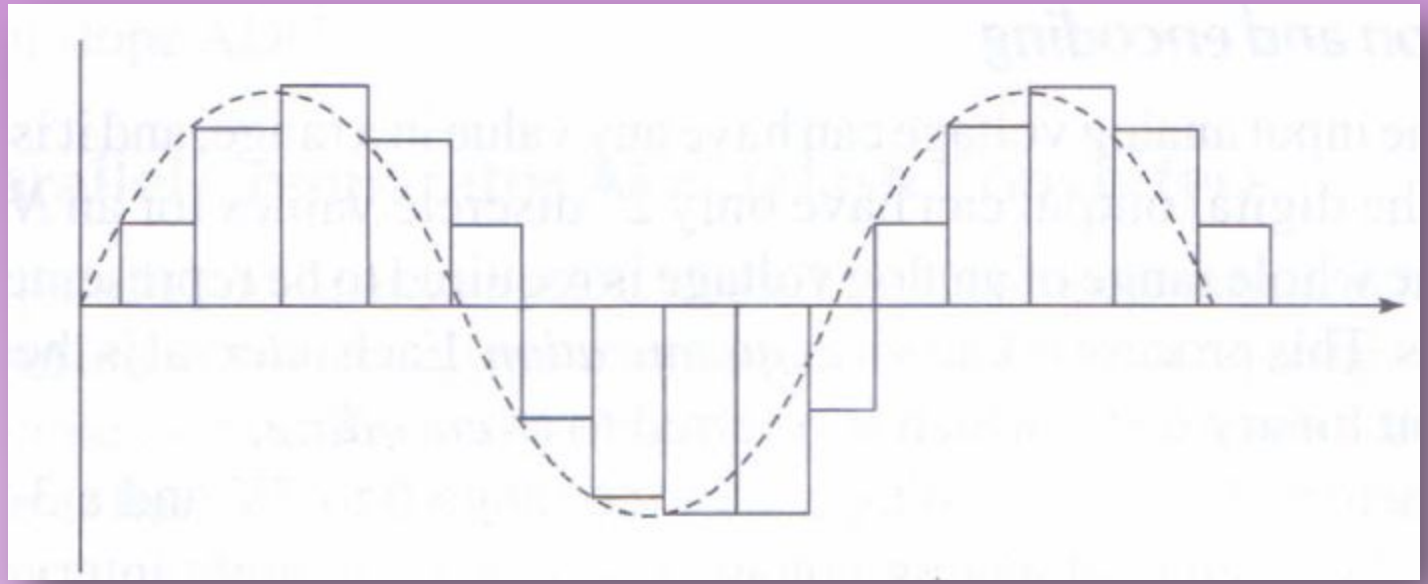
An ADC does the inverse function of a DAC. In a DAC, the possible number of digital inputs is fixed. For example, in a 4-bit DAC, there are 16 possible inputs. But in case of an ADC, the input analog voltage can have any value in a range and the digital output can have only 2^N *discrete values for an N-bit ADC. The ADC* process includes sampling of input analog signal and then, each sample is converted into its binary equivalent. The block diagram of an ADC is shown in Fig.

Sample-and-hold circuit

The sample-and-hold circuit captures the sample after a fixed delay. The fixed delay $T = 1/f_s$ *where* f_s *is a sampling frequency. As per the sampling theorem, the* sampling frequency should be greater than or equal to twice the band limited frequency of the signal. The result of the sampling process is a series of sampling instants and the amplitude of the signal at that instant of time, i.e. output of the sample circuit is a discrete time signal of different amplitudes, as shown in Fig



The discrete signal is converted to binary with the help of a converter. The discrete signal, as shown in previous Fig., is present for a small instant and hence, the converter cannot convert it into binary. There is a need to hold the sample at least for the duration of conversion time. The sample-and-hold circuit captures the sample and holds it, as shown in Fig.



A simple sample-and-hold circuit is shown in Fig. In this circuit, the voltage across the capacitor follows the input signal voltage *Vi when the switch S is closed.* The capacitor holds the instantaneous value of the signal voltage attained just before the
switch is opened. Thus for every T_s *the* switch is closed for a short duration and then opened. The dc voltage across the capacitor gives the value of the signal at the instant when the switch is opened. We can say that the sample is captured after a fixed delay T_s, This dc voltage represents a sample of the signal and is converted to digital signal using ADC circuit during the hold period.

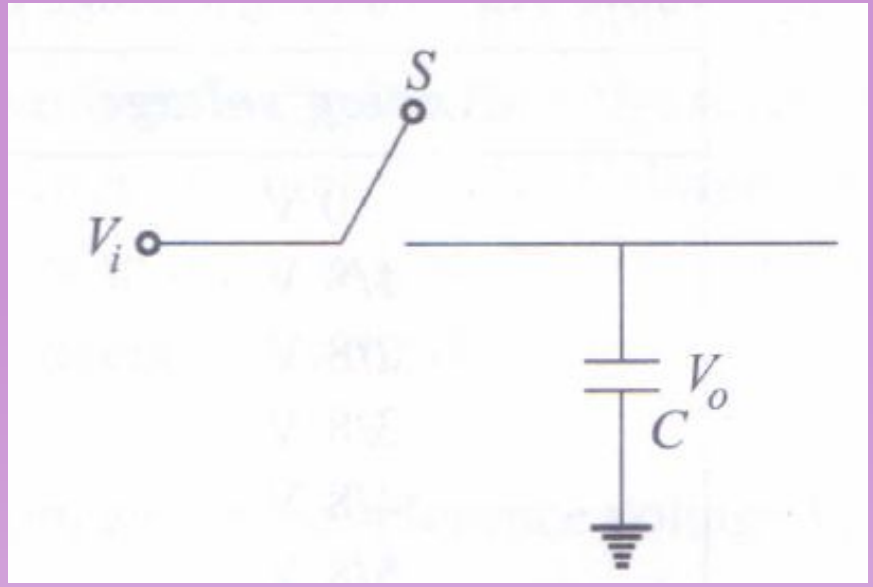
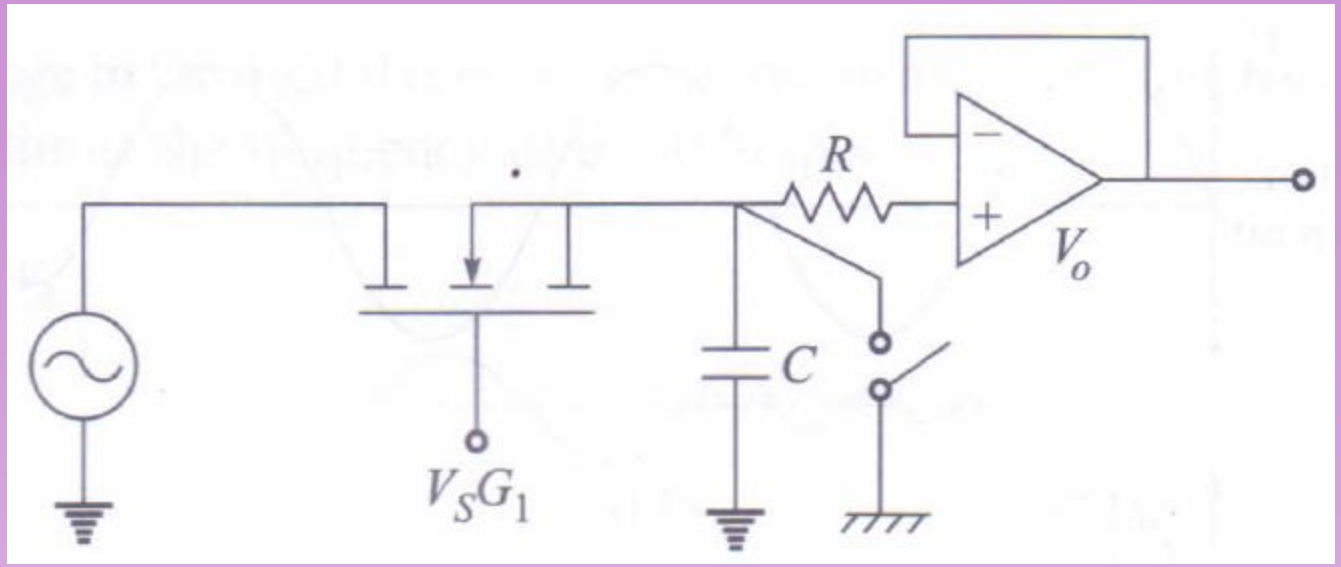


Figure shows a sample-and-bold circuit using MOSFET. In this circuit, an enhancement mode MOSFET is used as a switch, which is controlled by a control voltage V_s.



The op-amp is used to avoid the discharge of capacitor due to the loading effect of ADC. During the positive value of Vs (higher than the threshold voltage), the MOSFET conducts and as a result, the input voltage appears across the capacitor

C and at the output. When V_s is less than the threshold voltage, the MOSFET is cut off (switch open) and the voltage across C is retained because the input resistance of the op-amp is very high.

The accuracy of the circuit depends upon the holding of the charge in the capacitor, therefore a capacitor with very low leakage must be used. A capacitor with polycarbonate, polyethylene is preferred. Most of the other capacitors do not retain the stored charge for a long duration due to the polarization phenomenon.

Quantization and encoding

In an ADC, the input analog voltage can have any value in a range, and it is a function of time, but the digital output can have only 2^N discrete values for an N-bit ADC. Therefore, the whole range of analog voltage is required to be represented suitably in 2^N intervals. This process is known as **quantization**. Each interval is then assigned a unique N-bit binary code, which is referred to as **encoding**.

Let us consider the analog voltage is in the range 0 to 7V and a 3-bit digital output. The whole range of analog voltage is divided into eight intervals (2^3) of step size S = 1/8. Each interval is assigned a 3-bit binary value. The interval of the analog voltage and their corresponding digital values assigned are given in Table. These levels are known as the ***quantization level***.

Analog voltage and their corresponding digital values

Analog voltage	*Digital value*
0V	000
1/8 V	001
2/8 V	010
3/8 V	011
4/8 V	100
5/8 V	101
6/8 V	110
7/8 V	111

ADC Circuits

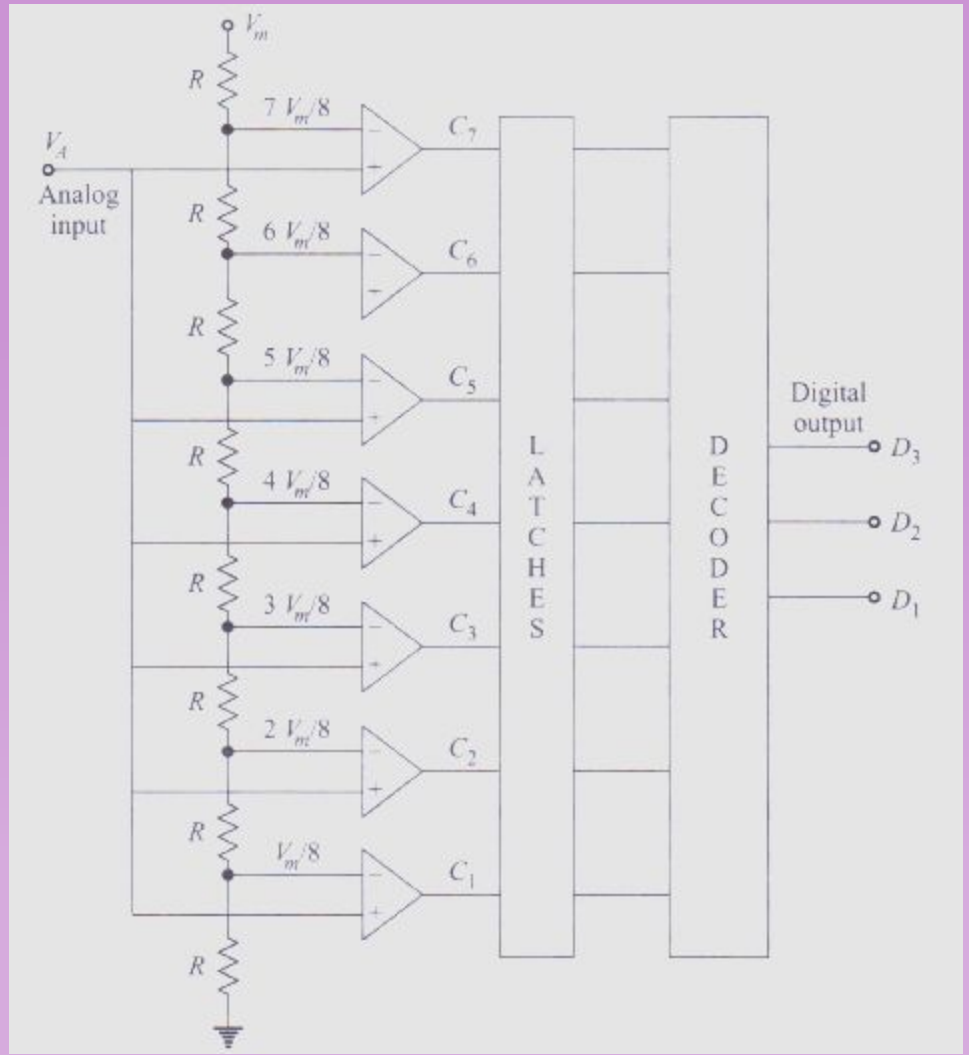
Different methods have been developed to convert an analog signal into its equivalent digital signal. Commonly used ADCs are:

(a) Parallel comparator ADC (Flash ADC)
(b) Counter type ADC
(c) Continuous type ADC
(d) Successive approximation ADC (Constant conversion time)
(e) Dual slope ADC (High Accuracy)

Parallel Comparator ADC (Flash Converter)

The n-bit parallel comparator ADC uses $(2^n - 1)$ comparators. Each comparator compares an unknown analog input voltage with its reference voltage and provides an appropriate output. The comparison is performed simultaneously, hence it is also known as flash type ADC.

In a circuit diagram, the op-amp is used in open loop. The open loop op-amp acts as a comparator; it compares the input voltage with the reference voltage (fixed voltage) and the output of op-amp is $+V_{sat}$ *or* $-V_{sat}$. *We can say that the output of* comparator is high or low (logic 1 or logic 0). The reference voltages are generated using a simple resistive network and a voltage source V_R *and given to the inverting* terminal of op-amp. The analog input signal is connected to the non-inverting terminal of op-amp. **When the analog input voltage is greater than the reference voltage, the output of comparator is high** and **when the analog input voltage is less than the reference voltage, then the output of comparator is low**. The output of the comparator (1 or 0) is loaded into the latch and decoded by the decoder, and we get the digital output at D_3, D_2 *and* D_1.



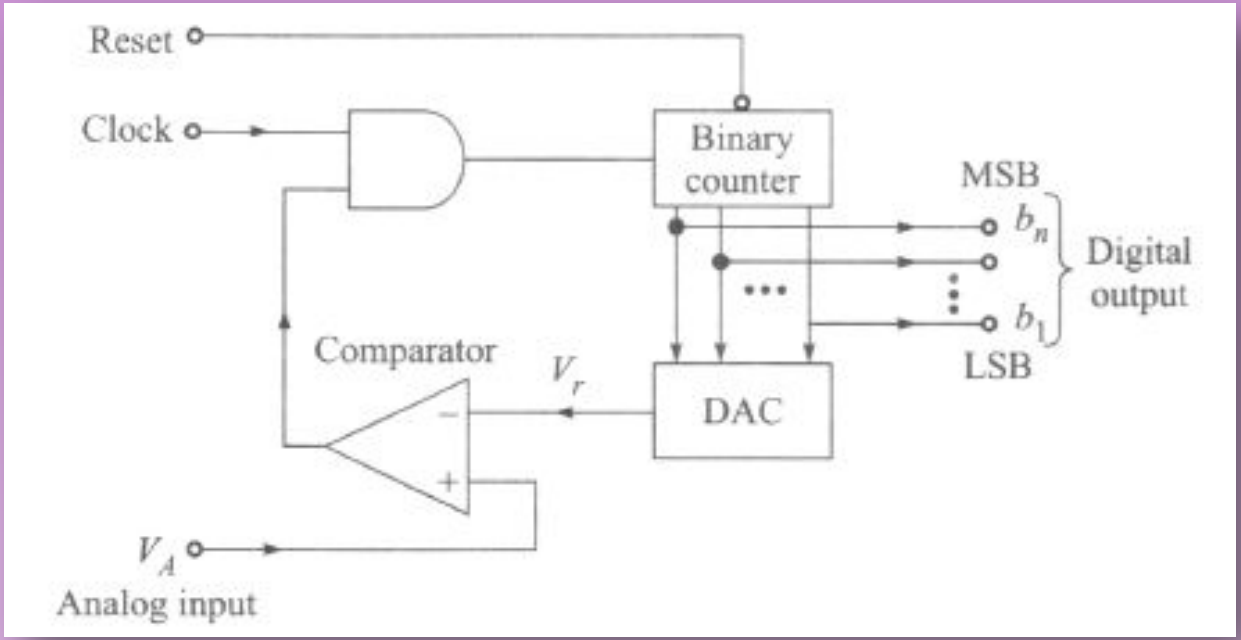
Fastest ADC

The principle of parallel comparator ADC is the simplest in concept and its typical conversion time is 100 ns. **But it requires a large number of comparators, which increases the cost and size of the circuit**.

Analog input	*O/P comparators*							*O/P of decoder*		
V_A	C_7	C_6	C_5	C_4	C_3	C_2	C_1	D_3	D_2	D_1
$0 < V_A < 1/8$	0	0	0	0	0	0	0	0	0	0
$1/8 < V_A < 2/8$	0	0	0	0	0	0	1	0	0	1
$2/8 < V_A < 3/8$	0	0	0	0	0	1	1	0	1	0
$3/8 < V_A < 4/8$	0	0	0	0	1	1	1	0	1	1
$4/8 < V_A < 5/8$	0	0	0	1	1	1	1	1	0	0
$5/8 < V_A < 6/8$	0	0	1	1	1	1	1	1	0	1
$6/8 < V_A < 7/8$	0	1	1	1	1	1	1	1	1	0
$7/8 < V_A < V_m$	1	1	1	1	1	1	1	1	1	1

Counter Type ADC

It is a high-resolution ADC that uses a comparator with variable reference voltage. The variable reference voltage can be obtained by a sequence or binary counter and a DAC. The block diagram of a 4-bit counter type ADC is shown in Fig.



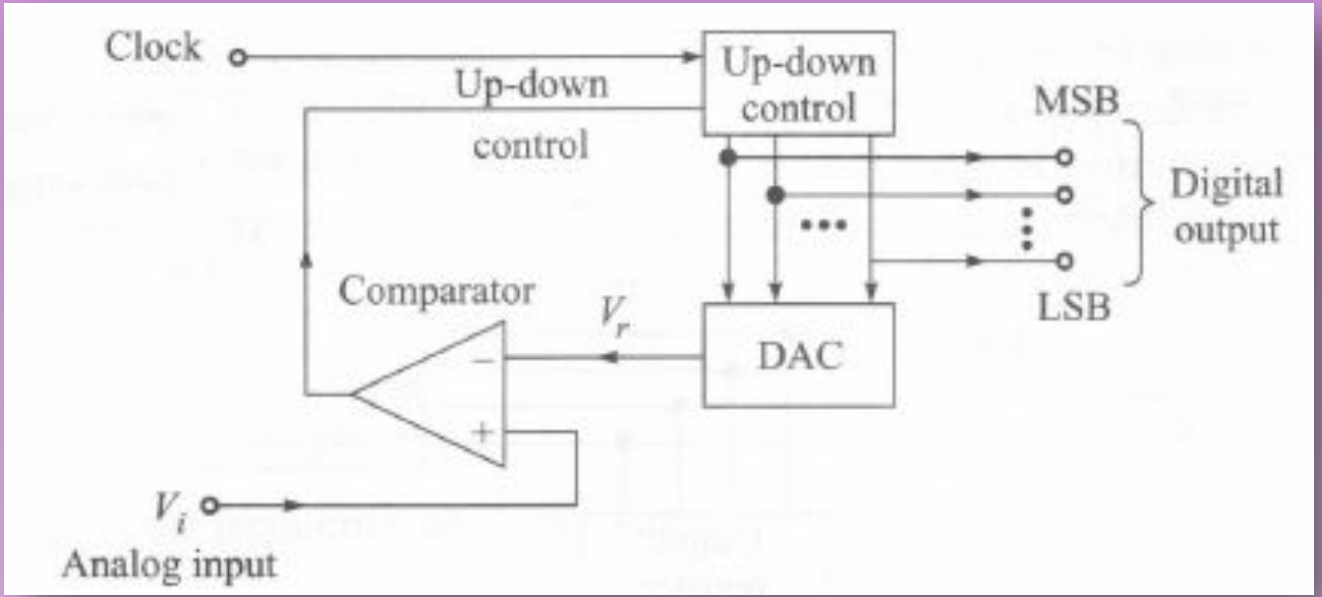
The block diagram consists of a DAC, a comparator, an AND gate, and a binary counter. The DAC converts the digital data into analog signal, which is given as one of the input to the comparator. The op-amp is used in open loop. It acts as a comparator and compares the analog input, which has to be converted to digital with the analog output of DAC. The AND gate provides the clock to the binary counter whenever the output of comparator is high.
When the reset signal goes low, the binary counter will be set to 0, and the output of DAC is zero (Vr = 0). When the reset signal goes high, the clock pulse is given to the binary counter through the AND gate; it is counted by the binary counter. The DAC converts the digital output to an analog voltage and connects it to the input of comparator. The output of comparator enables the AND gate to pass the clock. The output of DAC increases with time and the analog output voltage waveform is a rising staircase,

The comparator compares this analog voltage with the analog input voltage $V_{A.}$ When $V_A > V_r$ *the output of comparator is high, enable the AND gate to pass the* clock. When $V_A \leq V_r$ *the output of comparator is low, disable the AND gate to* pass the clock. The binary counter stops counting, and the digital output of DAC represents the analog input voltage.

Clock	*Digital signal*	V_r	V_A		*Description*
1	0000	0	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
2	0001	1/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
3	0010	2/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
4	0011	3/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
5	0100	4/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
6	0101	5/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
7	0110	6/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
8	0111	7/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
9	1000	8/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
10	1001	9/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
11	1010	10/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
12	1011	11/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
13	1100	12/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
14	1101	13/16	13/16	$V_A < V_r$	Disable the AND gate to pass the clock

Continuous Type ADC

The long conversion time of a counter type ADC can be eliminated by counting from the previously counted value, instead of resetting the counter for each conversion. The block diagram a 4-bit of continuous type ADC is shown in Fig.



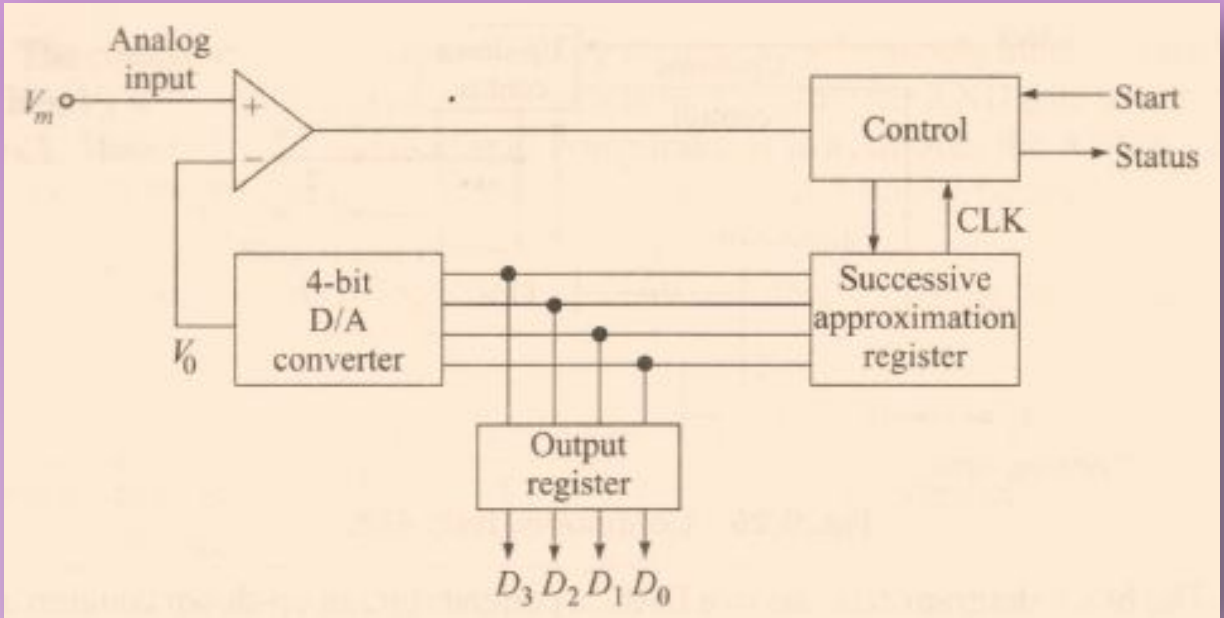
The block diagram consists of a DAC, a comparator, an up-down counter, and a control circuit. The DAC converts the digital data into analog signal, which is given to the inverting terminal of the comparator, and the non-inverting input of the comparator is connected to the unknown analog input voltage V_A. The op-amp is used in open loop. It acts as a comparator and compares the analog input that has to be converted into digital with the analog output of DAC. The control circuit controls the direction of up/down counter based on the result of comparator.

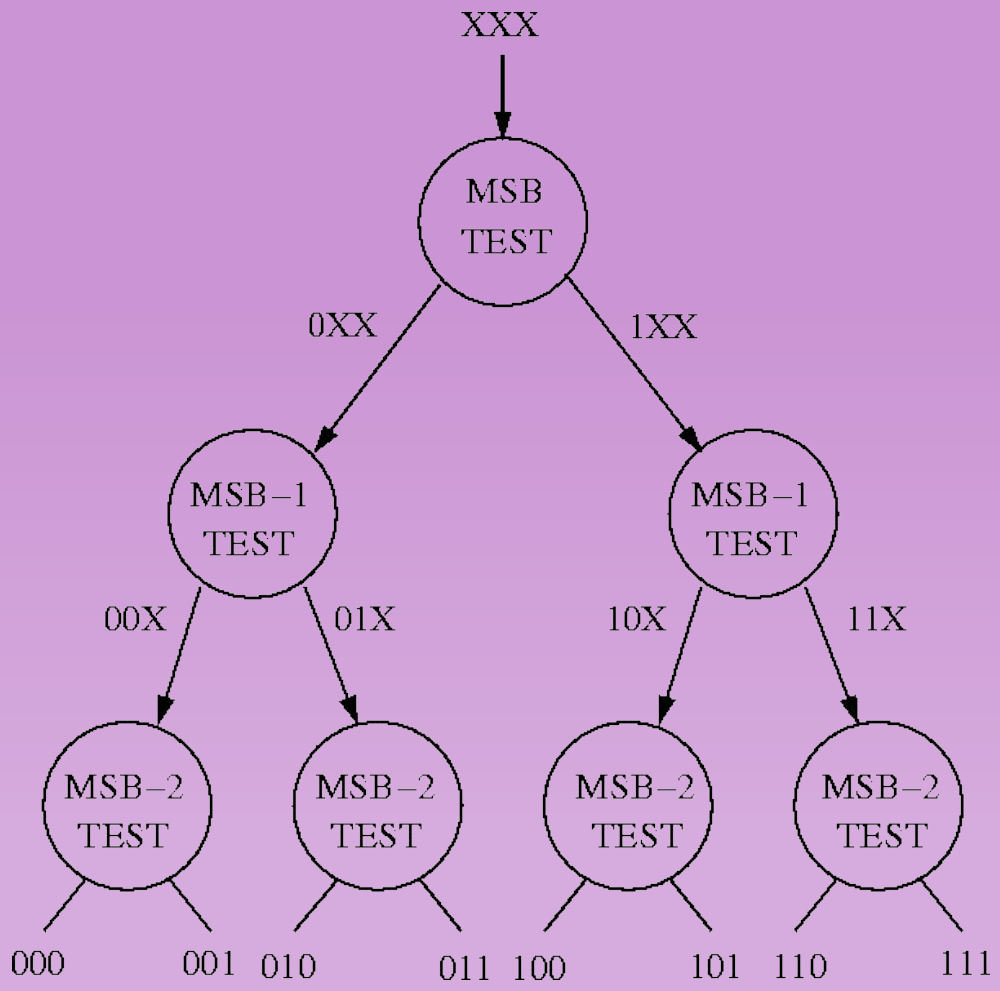
When $V_A > Vr$, the output of comparator is in high state. The counter is then made to count UP and the DAC output increases. The new input data is converted and compared with an unknown analog voltage. This process of counting-up continues, until Vr, is less than V_A.

When $V_A < Vr$, the output of comparator is in low state. The counter is then made to count DOWN and the DAC output decreases. The new input data is converted and compared with an unknown analog voltage. This process of counting down continues, until Vr, is greater than V_A

Successive-approximation ADC

It is a high-resolution ADC that uses only one comparator with a variable reference voltage. The variable reference voltage can be obtained by a sequence or binary counter and a DAC. The basic principle of this ADC is that the unknown analog input voltage is approximate against an *n-bit digital value by trying one bit at time,* beginning with the MSB.

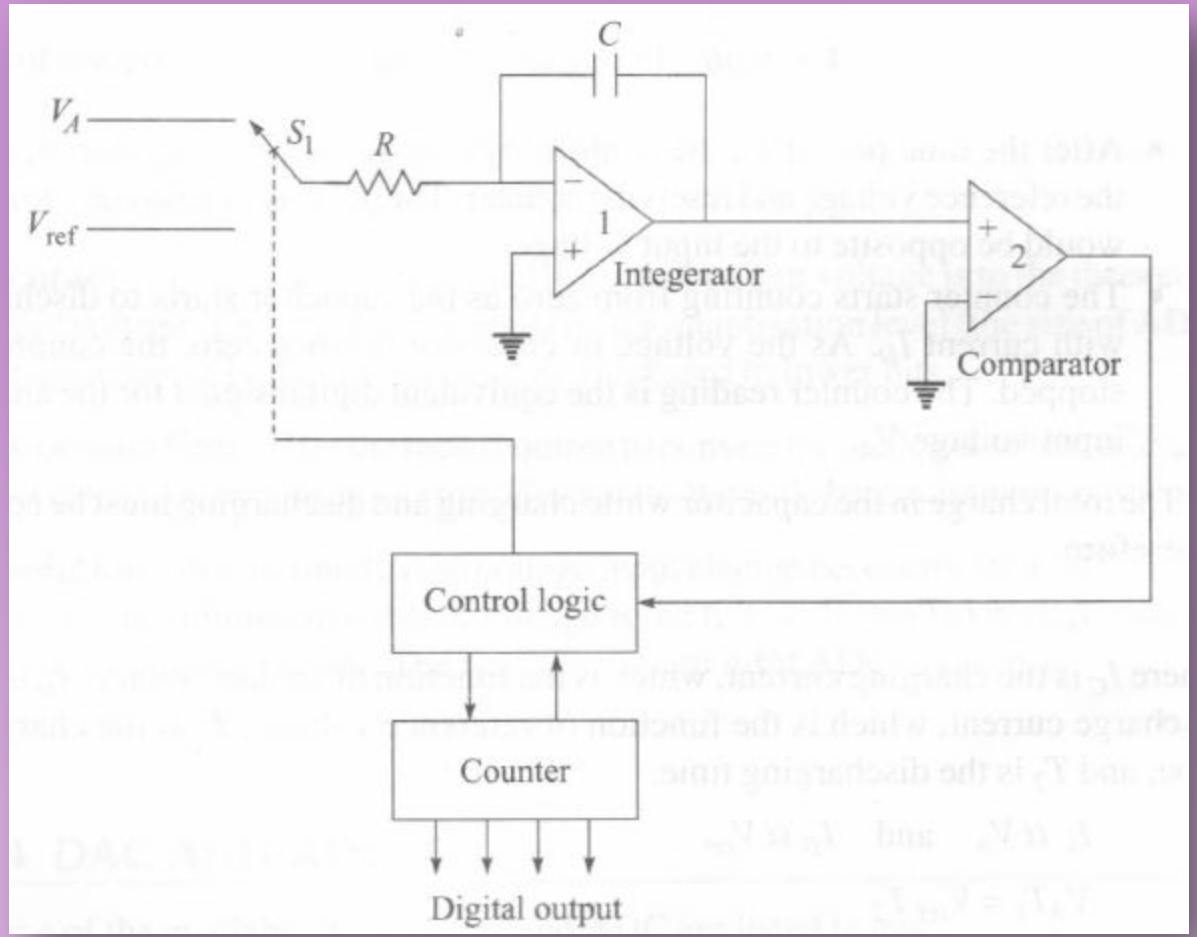




CONSTANT CONVERSION TIME ADC

Dual Slope ADC

In a dual slope ADC, the integrator generates two different ramps-one with an unknown analog input voltage V_A as the input, and another with a known reference voltage V_{ref} as the input. Hence, it is known as the dual slope ADC. The basic principle of a dual slope ADC is that, an analog signal is converted into a proportional time period, which is then measured using a digital counter. The block diagram of a typical dual slope ADC is shown in Fig.

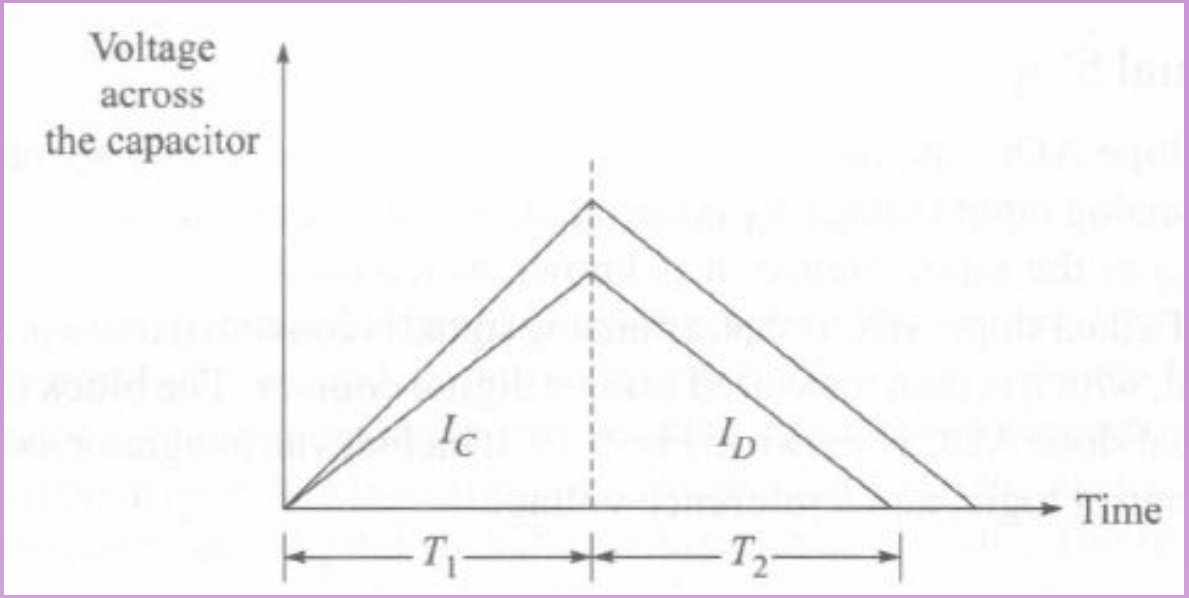


Op-amp 1 with resistor R and capacitor C acts as an integrator and when the input of integrator is connected to the analog input, the capacitor is charged linearly. The voltage across the capacitor depends on the amplitude of the analog input voltage and duration T.
Op-amp 2 is used in open loop. It acts as a comparator and compares the output of integrator with the reference input. The reference voltage is zero and the comparator acts as a zero crossing detector. The output of the comparator is high or low depending on the voltage. across the capacitor. When the voltage across the capacitor reaches zero, the output of the comparator is $-V_{sat}$, which is given to the control logic and the control logic stops the counting of counter.

The conversion process follows three steps.

- The switch S_1 connects the analog voltage V_A as the input to the integrator for a fixed period T_1. During this period, the capacitor of the integrator is charged up to a certain voltage with charging current Ic, which is the function of analog input voltage.

After the time period T_1, the control logic switches the integrator input to the reference voltage and resets the counter. The polarity of reference voltage would be opposite to the input voltage.



The counter starts counting from zero as the capacitor starts to discharge with current I_D. As the voltage of capacitor reaches zero, the counter is stopped. The counter reading is the equivalent digital signal for the analog input voltage VA

Total charge in the capacitor while charging and discharging must be equal.
Therefore,

$$I_C T_1 = I_D T_2$$

where I_C is the charging current, which is the function of analog voltage; I_D is the discharge current, which is the function of reference voltage; T_1 is the charging time; and T_2 is the discharging time.

$$I_C \alpha V_A \quad \text{and} \quad I_D \alpha V_{\text{ref}}$$

$$V_A T_1 = V_{\text{ref}} T_2$$

$$T_2 = \frac{T_1}{V_{\text{ref}}} \times V_A$$

The period T_1 and the reference voltage V_{ref} are constant.

$$\left(\frac{T_1}{V_{\text{ref}}}\right) = K$$

Using this $T_2 = KV_A$

Thus, time period T_2 is proportional to analog voltage VA and the counter measures the period T_2 . Hence, the content of counter is the equivalent digital signal for the analog input V_A . The accuracy of this ADC is high as compared to a successive-approximation ADC, but its speed is slow.

ACCURACY IS VERY HIGH


Thank you for
listening