

A/D AND D/A CONVERTERS

Chapter Outline

- Basic concepts of analog-to-digital conversion and vice versa
- Types of ADC and DAC
- Examples of ADC and DAC

9.1 INTRODUCTION

Real world processes produce analog signals that carry information. An analog signal is defined over a continuous period of time and its amplitude may assume a continuous range of values. It is difficult to store, compare, calculate, and manipulate this information with good accuracy using purely analog technology.

Digital signal processing technology has a number of advantages over analog signal processing. Therefore in most of the applications, digital systems are preferred over analog systems. But it is found that most of the real data available is in analog form, for example, voice signal, output of the sensors, etc. Therefore it is necessary to convert analog signals into digital signals. An analog-to-digital converter (ADC) is used for this purpose. After processing these digital data by a digital system, it is given to a control device or transmitted through an analog channel or measured by an analog equipment. And hence, the output of a digital system should be converted into an analog signal. A digital-to-analog converter (DAC) is used for this purpose. The block diagram of a digital system with analog input and output is shown in Fig. 9.1.

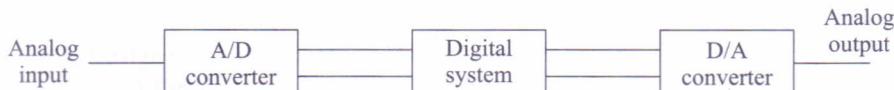


Fig. 9.1 Block diagram of a digital system with analog input and output

This chapter discusses the most common A/D and D/A conversion techniques.

9.2 BASIC PRINCIPLE OF DAC

The digital-to-analog (D/A) conversion involves translating digital information into its equivalent analog information. After processing the digital data by a digital system, it is given to an analog control device to drive the cursor arms of a plotter or transmitted through an analog channel or measured by an analog equipment. Hence the output of a digital system should be converted into analog signal. The DAC is used to convert digital signals into analog signals.

Figure 9.2 shows a block diagram of a 3-bit DAC. It has three input lines, D_2 , D_1 , and D_0 , and one output line which provides the analog signal. A 3-bit digital signal has eight combinations, from 000 to 111. The output analog voltage level is a function of the input combinations of 0 and 1; it is minimum for 000 and maximum for 111. Let us assume the output analog signal is in the range of 0 to 1V and the input combinations are 000 to 111. Its equivalent analog is given in Table 9.1 and the relation between the digital signal input and the analog signal output is shown in Fig. 9.3.

Table 9.1 Digital input and its equivalent analog

Digital signal	Analog signal
000	0 V
001	1/8 V
010	2/8 V
011	3/8 V
100	4/8 V
101	5/8 V
110	6/8 V
111	7/8 V

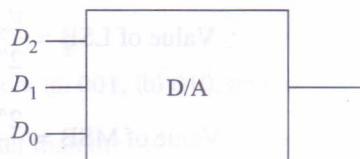


Fig. 9.2 Block diagram of 3-bit DAC

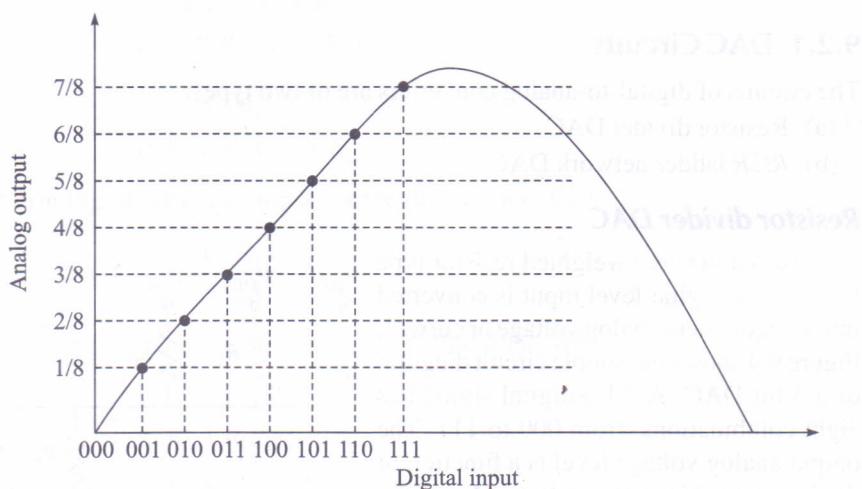


Fig. 9.3 The relation between digital input and analog output

From the above table and Fig. 9.3,

1. The value of LSB is $\frac{V_m}{2^n}$
2. The value of second LSB is $\frac{2^1 \cdot V_m}{2^n}$
3. The value of N th LSB is $\frac{2^{n-1} \cdot V_m}{2^n}$
4. Full scale output = $V_m - \text{Value of LSB}$

where n is the number of bits of a digital signal and V_m is the maximum amplitude. The output analog voltage V_A is

$$V_A = \frac{V_m[V_{D0}2^0 + V_{D1}2^1 + V_{D2}2^2 + \dots + V_{Dn-1}2^{n-1}]}{2^n}$$

where $V_{D0}, V_{D1}, V_{D2}, \dots, V_{Dn-1}$ are the digital inputs of n -bit DAC.

Example 9.1 Calculate the values of the LSB, MSB, and the full-scale output for an 8-bit DAC for 0 to 10 V analog output range.

Solution

Given data: $n = 8, V_m = 10 \text{ V}$

$$\text{Value of LSB} = \frac{V_m}{2^n} = \frac{10}{2^8} = \frac{10}{256} = 0.039 \text{ V}$$

$$\text{Value of MSB} = \frac{2^{n-1} \cdot V_m}{2^n} = \frac{2^{8-1} \cdot 10}{2^8} = 5 \text{ V}$$

$$\begin{aligned}\text{Full-scale output} &= V_m - \text{Value of LSB} \\ &= 10 - 0.039 = 9.961 \text{ V}\end{aligned}$$

9.2.1 DAC Circuits

The circuits of digital-to-analog converters are of two types:

- Resistor divider DAC
- $R/2R$ ladder network DAC

Resistor divider DAC

It is also known as a weighted resistor type DAC. Each digital level input is converted into an equivalent analog voltage or current. Figure 9.4 shows the simple circuit diagram of a 3-bit DAC. A 3-bit digital signal has eight combinations, from 000 to 111. The output analog voltage level is a function of the input combinations of 0 and 1 and the amplitude or reference voltage; it is minimum for 000 and maximum for 111.

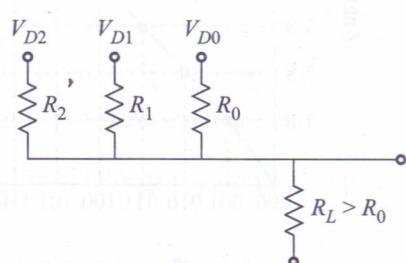


Fig. 9.4 3-bit DAC

In Fig. 9.4, V_{D2} , V_{D1} , and V_{D0} are the 3-bit digital inputs reference voltages and V_A is the analog output. Assume logic 0 corresponds to 0V and logic 1 corresponds to 7V. For the input 001, the output should be $V_m/2^n = 7/2^3 \cong 1$ V; for the input 010, the output should be $2^1 \cdot V_m/2^n = 2^1 \cdot 7/2^3 \cong 2$ V, and for the input 100, the output should be $2^2 \cdot V_m/2^n = 2^2 \cdot 7/2^3 \cong 4$ V. Let us consider that the digital input signals 001, 010, and 100 are applied to the network, as shown in Figs 9.5 (a), (b), and (c), respectively, and assume $V_{D2} = V_{D1} = V_{D0} = V_D$.

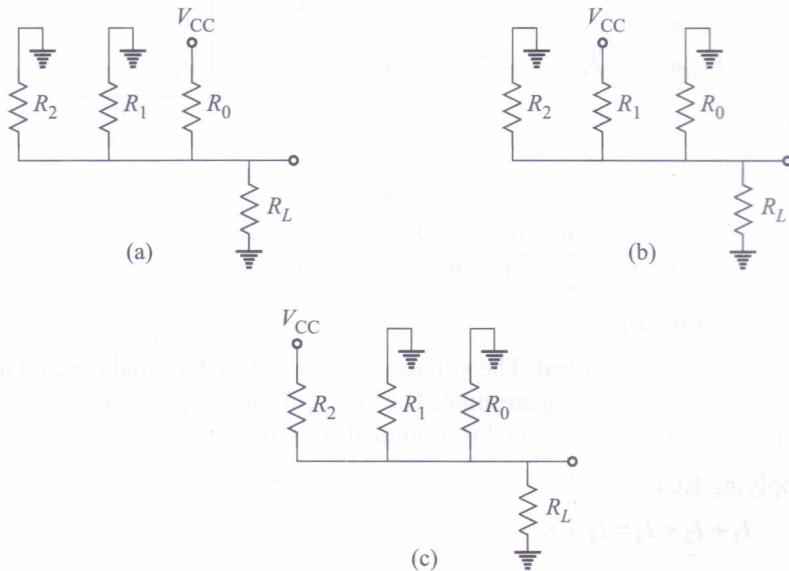


Fig. 9.5 Digital input applied to the network (a) 001, (b) 010, and (c) 100

Assume that the load resistance R_L is greater than the output resistance of the network.

From Fig. 9.5(a), the output for the digital input 001,

$$1 \text{ V} = \frac{V_D R_1 R_2 / (R_1 + R_2)}{R_0 + R_1 R_2 / (R_1 + R_2)} \quad (9.1)$$

$$1 \text{ V} = \frac{V_D R_1 R_2}{R_0 R_1 + R_0 R_2 + R_1 R_2}$$

From Fig. 9.5(b), the output for the digital input 010,

$$2 \text{ V} = \frac{V_D R_0 R_2}{R_0 R_1 + R_0 R_2 + R_1 R_2} \quad (9.2)$$

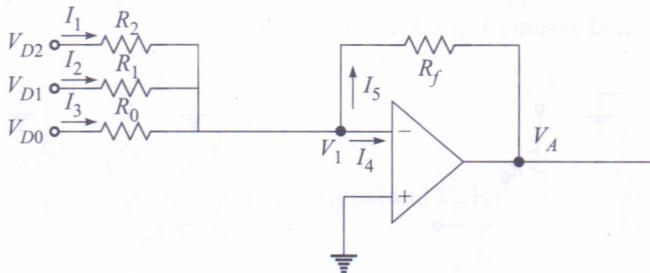
From Fig. 9.5(c), the output for the digital input 100,

$$4 \text{ V} = \frac{V_D R_1 R_0}{R_2 R_0 + R_1 R_2 + R_1 R_0} \quad (9.3)$$

Simplifying Eqs (9.1), (9.2), and (9.3),

$$R_1 = R_0/2 \text{ and } R_2 = R_0/4$$

The circuit will work as a DAC and provide more accurate result under the assumption that the load resistance is higher than the output resistance of the circuit. If it is low, the circuit cannot provide accurate result. To avoid this problem, an op-amp is used which isolates the load from the resistive network. The circuit of a DAC with op-amp is shown in Fig. 9.6.



$$R_f = 1\text{K}, R_0 = 8\text{K}, R_1 = 4\text{K}, R_2 = 2\text{K}$$

Fig. 9.6 3-bit DAC

Analysis of circuit

Assume the op-amp is ideal. The voltage at the inverting terminal is equal to the voltage at the non-inverting terminal. The input current of op-amp is zero ($I_4 = 0$), since the non-inverting terminal is grounded, $V_1 = 0$.

Applying KCL to node 1,

$$I_1 + I_2 + I_3 = I_4 + I_5$$

$$I_1 + I_2 + I_3 = I_5 \quad (\text{since } I_4 = 0)$$

$$\frac{V_{D2} - V_1}{R_2} + \frac{V_{D1} - V_1}{R_1} + \frac{V_{D0} - V_1}{R_0} = \frac{V_1 - V_A}{R_f}$$

$$\frac{V_{D2}}{R_2} + \frac{V_{D1}}{R_1} + \frac{V_{D0}}{R_0} = -\frac{V_A}{R_f}$$

$$V_A = R_f \left(\frac{V_{D2}}{R_2} + \frac{V_{D1}}{R_1} + \frac{V_{D0}}{R_0} \right) \quad (\text{Considering the magnitude only})$$

Assume $V_{D2} = V_{D1} = V_{D0} = V_D = 7\text{V}$

$$\text{For the input 001, the output } V_A = \frac{V_m}{2^n} = \frac{7}{2^3} = \frac{7}{8}$$

$$\frac{7}{8}\text{V} = R_f \left(\frac{V_{D0}}{R_0} \right) = \frac{7R_f}{R_0} \quad (9.4)$$

For the input 010, the output,

$$V_A = \frac{2^2 \cdot V_m}{2^n} = \frac{2^1 \cdot 7}{2^3} = \frac{14}{8} = \frac{7}{4}$$

$$\frac{7}{4}V = R_f \left(\frac{V_{D1}}{R_1} \right) = \frac{7R_f}{R_1} \quad (9.5)$$

For the input 100, the output,

$$V_A = \frac{2^2 \cdot V_m}{2^n} = \frac{2^1 \cdot 7}{2^3} = \frac{28}{8} = \frac{7}{2}$$

$$\frac{7}{2}V = R_f \left(\frac{V_{D2}}{R_2} \right) = \frac{7R_f}{R_2} \quad (9.6)$$

If $R_f = 1K$, then $R_2 = 2K$, $R_1 = 4K$, and $R_0 = 8K$. These values are obtained from Eqs (9.4), (9.5), and (9.6), and the circuit is used to convert the digital data inputs into analog current signal outputs.

The DAC output is the multiplying reference voltage by the signal data. Therefore if the reference voltage is variable, then the DAC is called a multiplying DAC. The n -bit DAC circuit shown in Fig. 9.7. It uses negative reference voltage, thus producing a positive voltage.

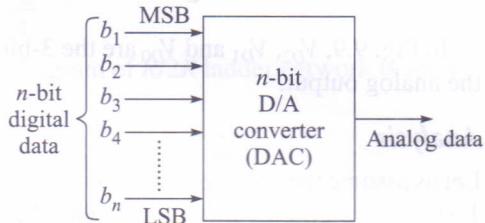


Fig. 9.7 n -bit DAC

The analog output voltage waveform of a 3-bit resistor divider DAC for the digital word, 000, 001, ..., 111, is shown in Fig. 9.8.

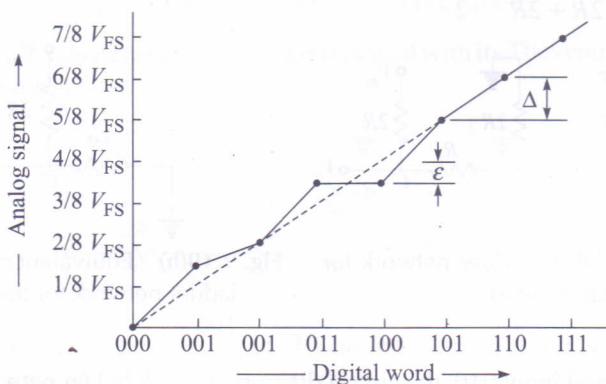


Fig. 9.8 Analog output voltage waveform for a 3-bit resistor divider DAC

Higher the value of n , finer the resolution of conversion and less is the step size of staircase. The accuracy and stability of DAC are based on the accuracy of the resistors and their temperature dependence.

A weighted DAC requires a wide range of resistor values. As the length of binary inputs increases, the range of resistor values needed also increases. For an 8-bit DAC, the larger values of resistor are 128 times the value of the smallest resistor.

R/2R ladder network DAC

The major drawback of a resistor divider DAC is the requirement of a wide range of resistor values. In contrary, R-2R ladder DAC uses only two resistor values, i.e. R and $2R$. The R/2R ladder network is shown in Fig. 9.9.

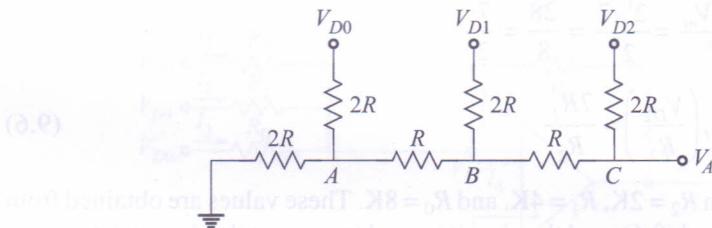


Fig. 9.9 The R/2R ladder network

In Fig. 9.9, V_{D2} , V_{D1} and V_{D0} are the 3-bit digital inputs voltage levels and V_A is the analog output.

Analysis

Let us assume the voltage corresponding to logic level 1 is V_m . For the digital input 100, the circuit diagram of R/2R ladder network is shown in Fig. 9.10(a) and its equivalent circuit is shown in Fig. 9.10(b). For the digital input signal 100, the output analog voltage is,

$$V_A = \frac{V_m \times 2R}{2R + 2R} = \frac{V_m}{2} \quad (9.7)$$

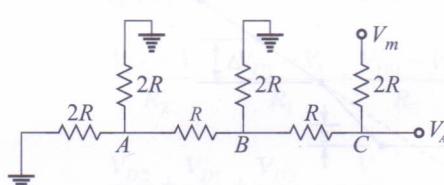


Fig. 9.10(a) R/2R ladder network for the digital input 100

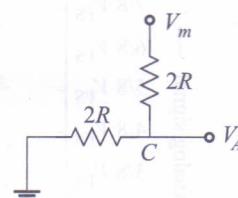


Fig. 9.10(b) Equivalent circuit of R/2R ladder network for the digital input 100

For the digital input 010, the circuit diagram of R/2R ladder network is shown in Fig. 9.11(a) and its equivalent circuit is shown in Fig. 9.11(b).

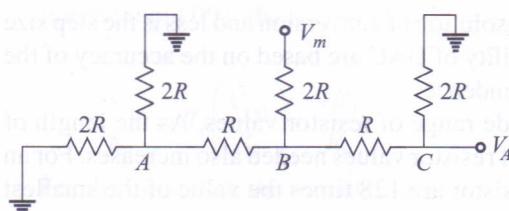


Fig. 9.11(a) R/2R ladder network for 010

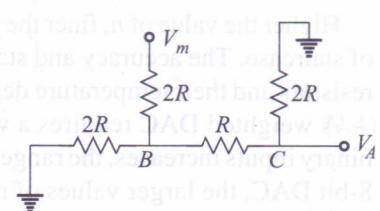


Fig. 9.11(b) Equivalent circuit of R/2R ladder network for 010

The left-hand side network of node B is replaced with its Thevenin's equivalent and it is shown in Fig. 9.11(c).

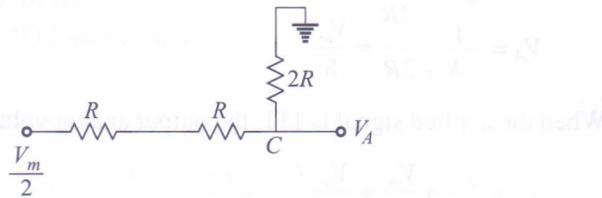


Fig. 9.11(c) Equivalent of Fig. 9.12(b) with Thevenin's equivalent of left-hand side network of node B

For the digital input signal 1010, the output analog voltage is,

$$V_A = \frac{V_m}{2} \times \frac{2R}{2R+2R} = \frac{2V_m}{8} = \frac{V_m}{4} \quad (9.8)$$

For the digital input 001, the circuit diagram of $R/2R$ ladder network is shown in Fig. 9.12(a).

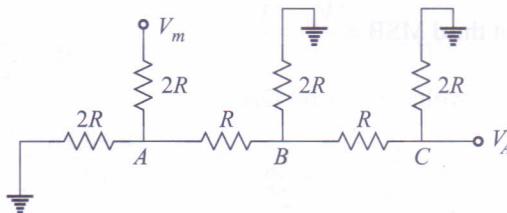


Fig. 9.12(a) $R/2R$ ladder network for 001

The left-hand side network of node A is replaced with its Thevenin's equivalent and it is shown in Fig. 9.12(b).

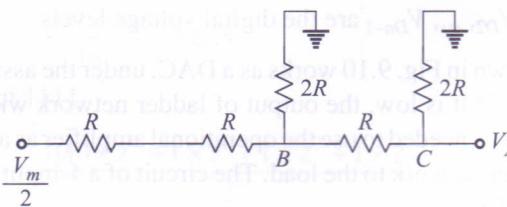


Fig. 9.12(b) Equivalent of Fig. 9.12(a) with Thevenin's equivalent of left-hand side network of node A

The left-hand side network of node B is replaced with its Thevenin's equivalent and it is shown in Fig. 9.12(c).

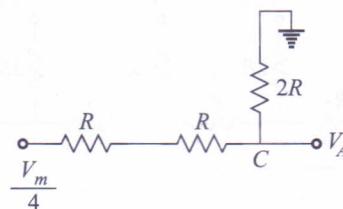


Fig. 9.12(c) Equivalent of Fig. 9.13(b) with Thevenin's equivalent of left-hand side network of node B

For the digital input signal 001, the output analog voltage is,

$$V_A = \frac{\frac{V_m}{4} \times 2R}{2R + 2R} = \frac{V_m}{8} \quad (9.9)$$

When the applied signal is 111, the output analog voltage will be,

$$V_A = \frac{V_m}{2} + \frac{V_m}{4} + \frac{V_m}{8} \quad (9.10)$$

From the analysis, it is observed that for a 3-bit DAC,

- The value of MSB = $\frac{V_m}{2}$

- The value of second MSB = $\frac{V_m}{4} = \frac{V_m}{2^2}$

- The value of third MSB = $\frac{V_m}{8} = \frac{V_m}{2^3}$

The output analog voltage of n -bit DAC is,

$$V_A = \frac{V_m}{2} + \frac{V_m}{4} + \frac{V_m}{8} + \dots + \frac{V_m}{2^n} \quad (9.11)$$

$$= \frac{V_m[V_{Dn-1}2^{n-1} + V_{D3}2^3 + V_{D2}2^2 + V_{D1}2^1 + V_{D0}2^0]}{2^n} \quad (9.12)$$

where $V_{D0}, V_{D1}, V_{D2}, \dots, V_{Dn-1}$ are the digital voltage levels.

The circuit shown in Fig. 9.10 works as a DAC, under the assumption that load resistance is high. If it is low, the output of ladder network will be an incorrect value. Therefore, it is needed to use the operational amplifier as a buffer to connect the output of ladder network to the load. The circuit of a 4-input DAC with an op-amp is shown in Fig. 9.13.

In Fig. 9.13, the op-amp is used in inverting mode. The amplifier acts as an inverting current to the voltage converter. The output voltage $V_A = -IR$. The analysis of the circuit is same as above.

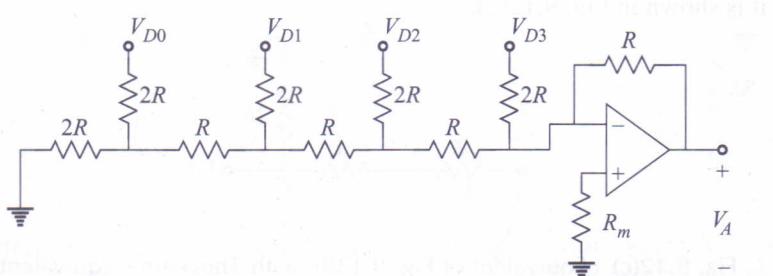


Fig. 9.13 4-inputs R/2R ladder network DAC with op-amp

Example 9.2 Find the output voltage of a 4-bit ladder, having the following digital inputs $V_m = 10\text{ V}$

- (a) 1010
- (b) 0110
- (c) 1001
- (d) Full-scale input

Solution

Assume logic 0 = 0V and logic 1 = 10V

$$V_A = \frac{V_m[V_{D_0}2^0 + V_{D_1}2^1 + V_{D_2}2^2 + V_{D_3}2^3]}{2^4}$$

- (a) Digital input 1010

$$\begin{aligned} V_A &= \frac{10[0 \times 2^0 + 1 \times 2^1 + 0 \times 2^2 + 1 \times 2^3]}{2^4} \\ &= \frac{10[2 + 8]}{16} = 6.25 \end{aligned}$$

- (b) Digital input 0110

$$\begin{aligned} V_A &= \frac{10[0 \times 2^0 + 1 \times 2^1 + 1 \times 2^2 + 0 \times 2^3]}{2^4} \\ &= \frac{10[2 + 4]}{16} = 3.75 \end{aligned}$$

- (c) Digital input 1010

$$\begin{aligned} V_A &= \frac{10[0 \times 2^0 + 0 \times 2^1 + 0 \times 2^2 + 1 \times 2^3]}{2^4} \\ &= \frac{10[1 + 8]}{16} = 5.625 \end{aligned}$$

- (d) Digital input 1111

$$\begin{aligned} V_A &= \frac{10[0 \times 2^0 + 1 \times 2^1 + 1 \times 2^2 + 1 \times 2^3]}{2^4} \\ &= \frac{10[1 + 2 + 4 + 8]}{16} = 9.375 \end{aligned}$$

9.2.2 DAC

Either a ladder or a resistive divider network can be used as a DAC. The complete block diagram of a DAC is shown in Fig. 9.14.

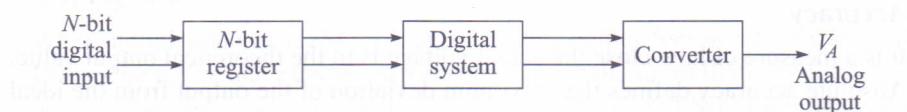


Fig 9.14 Complete block diagram of DAC

The N -bit register is used to store the digital information. The D flip-flop can be used as a basic element of a register. The number of flip-flops define the size of a register, one flip-flop stores 1-bit data. Digital data is loaded into a flip-flop with a clock pulse. The output of flip-flop is logic 1 or logic 0, values of logic 1 and logic 0 may not be same.

To provide the same level voltage for logic 1s and logic 0s, the level amplifiers are used. The level amplifier has two inputs; one is the reference voltage from an external voltage source and the other input is the output of the flip-flop. The amplifier works such that, when the input from a flip-flop is high, the output of the amplifier is V_{ref} and when the input from the flip-flop is low, the output is 0 V.

The schematic of a 4-bit DAC is shown in Fig. 9.15.

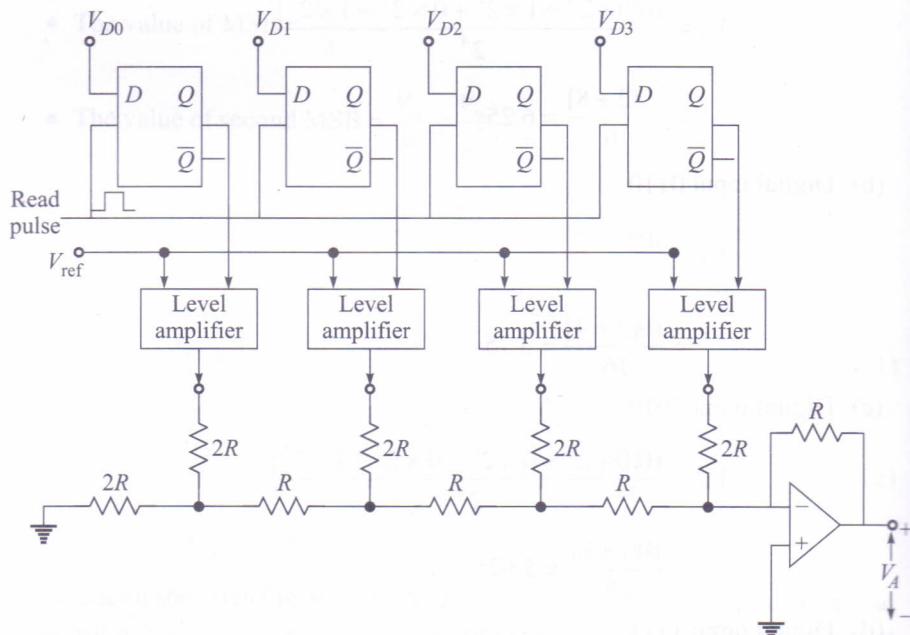


Fig. 9.15 Schematic of 4-bit DAC

9.2.3 Specifications of DAC

The specifications of a DAC which are generally specified by the designers are:

- Accuracy
- Resolution
- Linearity
- Settling time
- Temperature sensitivity

Accuracy

It is a measure of how close the actual voltage is to the theoretical output value. Absolute accuracy defines the maximum deviation of the output from the ideal value. The accuracy of a DAC depends upon the accuracy of the precision resistor used in the resistor divider or ladder network and the precision of the reference voltage. It is specified as a percentage of full-scale or maximum output voltage.

For example, suppose the theoretical output voltage is 10 V for a full-scale digital input and accuracy is ± 5 percent, it means that the output voltage of DAC for the same digital input lies between 9.5 V to 10.5 V.

The accuracy specifies the maximum error that can occur in a output voltage. For example, suppose the full-scale output voltage is 10 V and accuracy is ± 0.1 percent, then the maximum error will be 10 mV (i.e. 0.001×10 V).

Resolution

It defines the smallest possible change in the output analog voltage due to the change in digital input. The resolution is always equal to the weight of LSB, and it is also known as the *step size*. It is a function of the number of bits in the digital input. The resolution of an n -bit DAC using divider is $V_m/2^n$ and using ladder network, it is $V_m/2^n$ in volts.

In a 4-bit DAC using a ladder, if the full-scale voltage 16 V, then the resolution is $16/2^4 = 1$ V. Thus, the output voltage changes in a step of 1 V. If it is desired to produce 5.3 V using this converter, the actual output voltage would be 5 V. Similarly, if it is desired to produce 9.6 V, the actual output voltage would be 10 V.

It is more useful to express the resolution as a percentage. The percentage resolution is given by,

$$\text{Percentage resolution} = \frac{\text{step size}}{\text{full-scale}} \times 100 \quad (9.13)$$

The percentage resolution can be calculated as,

$$\text{Percentage resolution} = \frac{1}{\text{number of steps}} \times 100 \quad (9.14)$$

For an n -bit input,

$$\text{Percentage resolution} = \frac{1}{2^{n-1}} \times 100 \quad (9.15)$$

To get a good resolution, the number of input bits (n) of DAC should be maximum.

Linearity

In a DAC, the relation between digital input and analog output should be linear. That is, an equal increment in the numerical significance of the digital input should result in equal increments in the analog output voltage. Due to the errors in resistor values, the input-output relationship is not linear. The linearity error for a digital input is the difference between the expected voltage and the voltage obtained at the output of DAC.

Settling time

When digital inputs of a DAC change, the analog output does not change instantly. Due to the active and passive elements of the circuit, an oscillation occurs at the output. The time required to settle the output within $\pm 1/2$ LSB of the final value,

after the change in the digital inputs, is referred to as the *settling time*, as shown in Fig. 9.16. It limits the frequency of digital input.

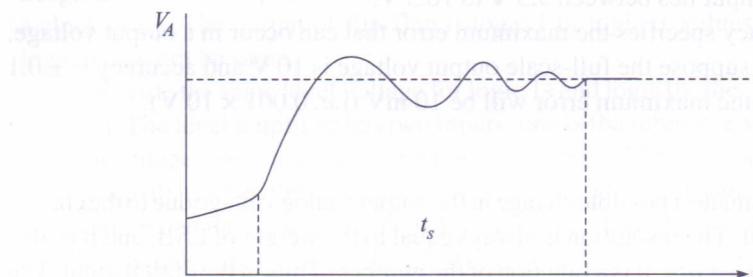


Fig. 9.16 Settling time

Temperature sensitivity

The components used in a circuit of DAC such as resistors, reference voltage source, and op-amp are sensitive to temperature. Due to the change in temperature, the characteristics of an op-amp, the values of resistor and reference voltage may change. Therefore, the analog output voltage for any fixed digital input varies with temperature. This change in values with the temperature is known as the *temperature sensitivity*. It is specified in terms of \pm ppm/ $^{\circ}$ C.

9.3 BASIC PRINCIPLE OF ADC

An ADC does the inverse function of a DAC. In a DAC, the possible number of digital inputs is fixed. For example, in a 4-bit DAC, there are 16 possible inputs. But in case of an ADC, the input analog voltage can have any value in a range and the digital output can have only 2^N discrete values for an N -bit ADC. The ADC process includes sampling of input analog signal and then, each sample is converted into its binary equivalent. The block diagram of an ADC is shown in Fig. 9.17.

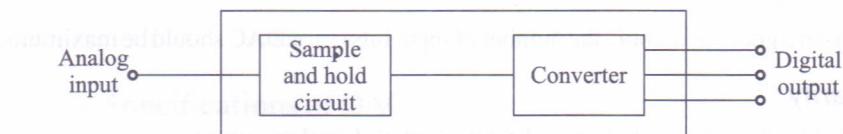


Fig. 9.17 Block diagram of ADC

Sample-and-hold circuit

The sample-and-hold circuit captures the sample after a fixed delay. The fixed delay $T = 1/f_s$ where f_s is a sampling frequency. As per the sampling theorem, the sampling frequency should be greater than or equal to twice the band limited frequency of the signal. The result of the sampling process is a series of sampling instants and the amplitude of the signal at that instant of time, i.e. output of the sample circuit is a discrete time signal of different amplitudes, as shown in Fig. 9.18. A discrete signal is one that is defined at discrete points of time only. The amplitude of a discrete signal is a continuous range of values, i.e. a discrete signal is the signal that is discrete in time but continuous in amplitude.

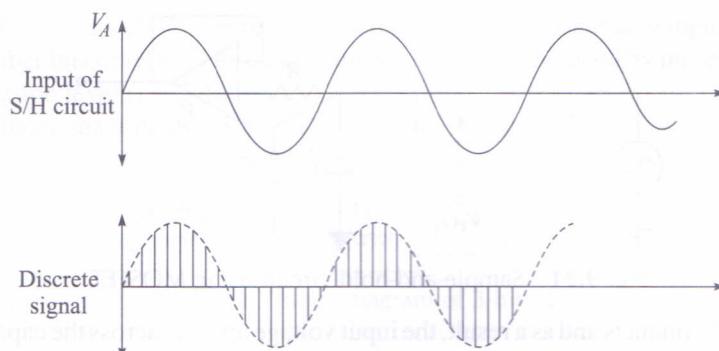


Fig. 9.18 Discrete signal

The discrete signal is converted to binary with the help of a converter. The discrete signal, as shown in Fig. 9.18, is present for a small instant and hence, the converter cannot convert it into binary. There is a need to hold the sample at least for the duration of conversion time. The sample-and-hold circuit captures the sample and holds it, as shown in Fig. 9.19.

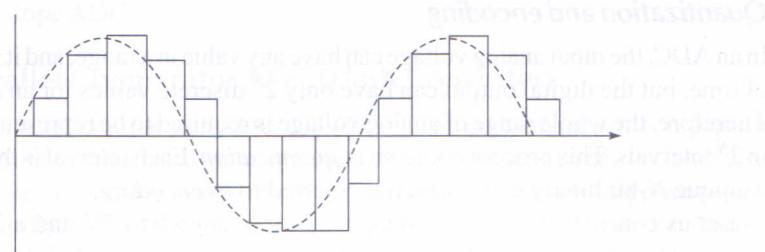


Fig. 9.19 Hold discrete signal

A simple sample-and-hold circuit is shown in Fig. 9.20. In this circuit, the voltage across the capacitor follows the input signal voltage V_i when the switch S is closed. The capacitor holds the instantaneous value of the signal voltage attained just before the switch is opened. Thus for every T_s , the switch is closed for a short duration and then opened. The dc voltage across the capacitor gives the value of the signal at the instant when the switch is opened. We can say that the sample is captured after a fixed delay T_s . This dc voltage represents a sample of the signal and is converted to digital signal using ADC circuit during the hold period.

Figure 9.21 shows a sample-and-hold circuit using MOSFET. In this circuit, an enhancement mode MOSFET is used as a switch, which is controlled by a control voltage V_s .

The op-amp is used to avoid the discharge of capacitor due to the loading effect of ADC. During the positive value of V_s (higher than the threshold voltage), the

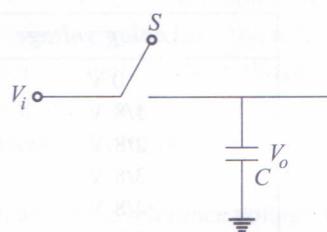


Fig. 9.20 Sample-and-hold circuit

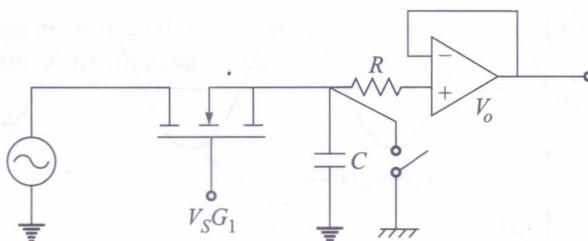


Fig. 9.21 Sample-and-hold circuit using MOSFET

MOSFET conducts and as a result, the input voltage appears across the capacitor C and at the output. When V_s is less than the threshold voltage, the MOSFET is cut off (switch open) and the voltage across C is retained because the input resistance of the op-amp is very high.

The accuracy of the circuit depends upon the holding of the charge in the capacitor, therefore a capacitor with very low leakage must be used. A capacitor with polycarbonate, polyethylene is preferred. Most of the other capacitors do not retain the stored charge for a long duration due to the polarization phenomenon.

Quantization and encoding

In an ADC, the input analog voltage can have any value in a range, and it is a function of time, but the digital output can have only 2^N discrete values for an N -bit ADC. Therefore, the whole range of analog voltage is required to be represented suitably in 2^N intervals. This process is known as *quantization*. Each interval is then assigned a unique N -bit binary code, which is referred to as *encoding*.

Let us consider the analog voltage is in the range 0 to 7V and a 3-bit digital output. The whole range of analog voltage is divided into eight intervals (2^3) of step size $S = 1/8$. Each interval is assigned a 3-bit binary value. The interval of the analog voltage and their corresponding digital values assigned are given in Table 9.2. These levels are known as the *quantization level*.

Table 9.2 Analog voltage and their corresponding digital values

Analog voltage	Digital value
0 V	000
1/8 V	001
2/8 V	010
3/8 V	011
4/8 V	100
5/8 V	101
6/8 V	110
7/8 V	111

During the process of conversion, the amplitude of a discrete signal is first converted to its nearest value of quantization level and then, it is encoded. The process of converting the amplitude of a discrete signal to its nearest value of quantization level is referred as *quantization*.

The process of quantization introduces error. This error is referred to as the *quantization error*. The maximum quantization error for any analog voltage is

$\pm 1/2 \times V_m/2^n = \pm V_m/2^{n+1}$ where V_m is the maximum value of analog input and n is the number bits of ADC. The quantization error will be reduced by increasing the quantization level (i.e. 2^n).

The block diagram of a 3-bit ADC is shown in Fig. 9.22.

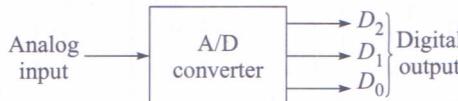


Fig. 9.22 Block diagram of 3-bit ADC

9.3.1 ADC Circuits

Different methods have been developed to convert an analog signal into its equivalent digital signal. Commonly used ADCs are:

- (a) Parallel comparator ADC
- (b) Counter type ADC
- (c) Continuous type ADC
- (d) Successive approximation ADC
- (e) Dual slope ADC

9.3.2 Parallel Comparator ADC (Flash Converter)

The n -bit parallel comparator ADC uses $2^n - 1$ comparators. Each comparator compares an unknown analog input voltage with its reference voltage and provides an appropriate output. The comparison is performed simultaneously, hence it is also known as flash type ADC. Figure 9.23 shows a 3-bit parallel comparator ADC.

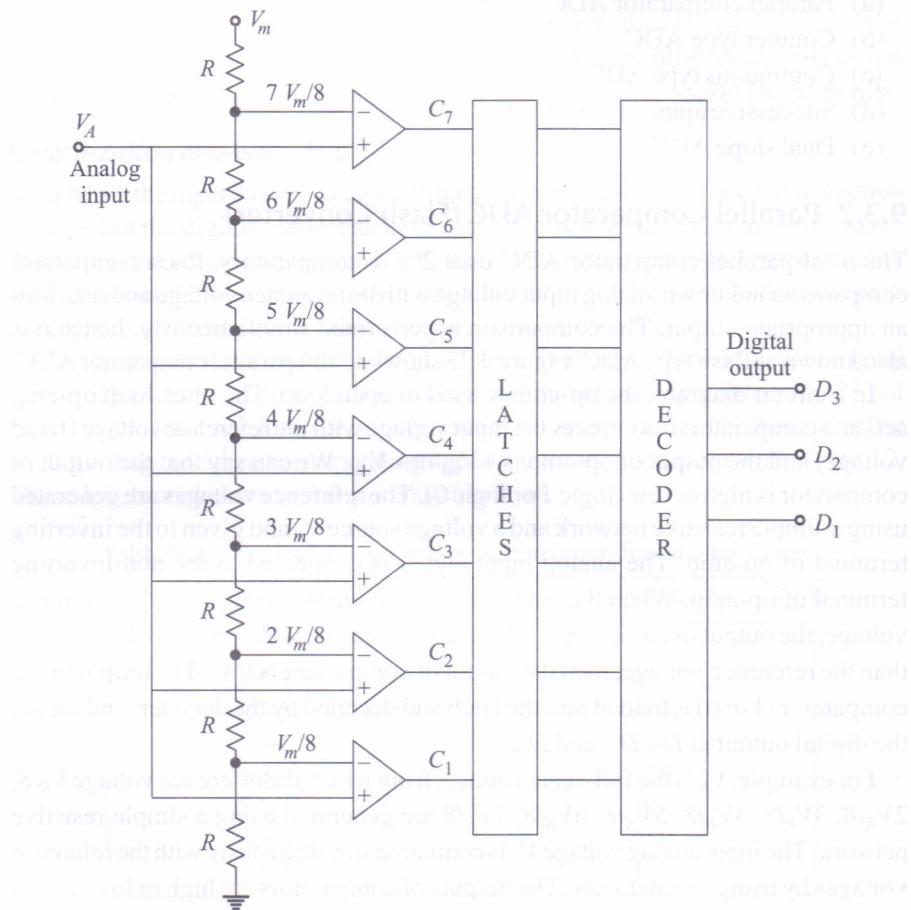
In a circuit diagram, the op-amp is used in open loop. The open loop op-amp acts as a comparator; it compares the input voltage with the reference voltage (fixed voltage) and the output of op-amp is $+V_{\text{sat}}$ or $-V_{\text{sat}}$. We can say that the output of comparator is high or low (logic 1 or logic 0). The reference voltages are generated using a simple resistive network and a voltage source V_R and given to the inverting terminal of op-amp. The analog input signal is connected to the non-inverting terminal of op-amp. When the analog input voltage is greater than the reference voltage, the output of comparator is high and when the analog input voltage is less than the reference voltage, then the output of comparator is low. The output of the comparator (1 or 0) is loaded into the latch and decoded by the decoder, and we get the digital output at D_2 , D_1 , and D_0 .

For example, V_R is the full-scale voltage, from which the reference voltage $V_R/8$, $2V_R/8$, $3V_R/8$, $4V_R/8$, $5V_R/8$, $6V_R/8$, $7V_R/8$ are generated using a simple resistive network. The input analog voltage V_A is compared simultaneously with the reference voltages by using comparators. The outputs of comparators are high or low, which is a function of the input analog voltage. A 7-bit output is obtained from the comparators, which is stored in latches. The decoder circuit converts this 7-bit digital signal into a 3-bit output.

The comparator output and the digital output of a 3-bit parallel comparator ADC is given in Table 9.3. Assume $V_R = 1$ V.

Table 9.3 Comparator output and digital output of parallel comparator ADC

Analog input	O/P comparators							O/P of decoder		
	C_7	C_6	C_5	C_4	C_3	C_2	C_1	D_3	D_2	D_1
$0 < V_A < 1/8$	0	0	0	0	0	0	0	0	0	0
$1/8 < V_A < 2/8$	0	0	0	0	0	0	1	0	0	1
$2/8 < V_A < 3/8$	0	0	0	0	0	1	1	0	1	0
$3/8 < V_A < 4/8$	0	0	0	0	1	1	1	0	1	1
$4/8 < V_A < 5/8$	0	0	0	1	1	1	1	1	0	0
$5/8 < V_A < 6/8$	0	0	1	1	1	1	1	1	0	1
$6/8 < V_A < 7/8$	0	1	1	1	1	1	1	1	1	0
$7/8 < V_A < V_m$	1	1	1	1	1	1	1	1	1	1

**Fig. 9.23** 3-bit parallel comparator ADC

The principle of parallel comparator ADC is the simplest in concept and its typical conversion time is 100 ns. But it requires a large number of comparators, which increases the cost and size of the circuit.

9.3.3 Counter Type ADC

It is a high-resolution ADC that uses a comparator with variable reference voltage. The variable reference voltage can be obtained by a sequence or binary counter and a DAC. The block diagram of a 4-bit counter type ADC is shown in Fig. 9.24.

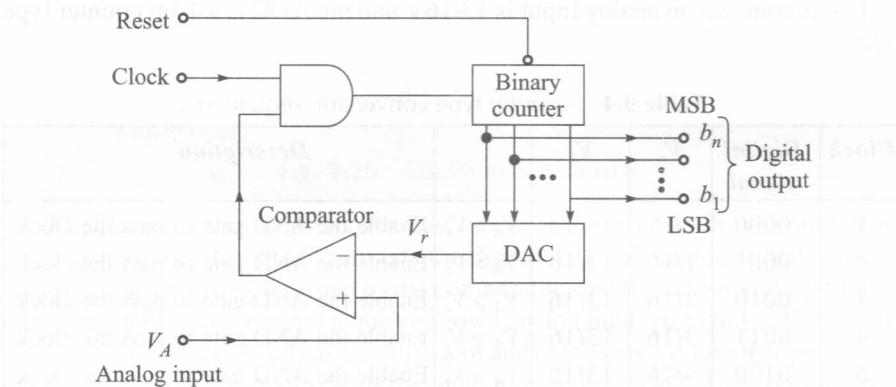


Fig. 9.24 Counter type ADC

The block diagram consists of a DAC, a comparator, an AND gate, and a binary counter. The DAC converts the digital data into analog signal, which is given as one of the input to the comparator. The op-amp is used in open loop. It acts as a comparator and compares the analog input, which has to be converted to digital with the analog output of DAC. The AND gate provides the clock to the binary counter whenever the output of comparator is high.

When the reset signal goes low, the binary counter will be set to 0, and the output of DAC is zero ($V_r = 0$). When the reset signal goes high, the clock pulse is given to the binary counter through the AND gate; it is counted by the binary counter. The DAC converts the digital output to an analog voltage and connects it to the input of comparator. The output of comparator enables the AND gate to pass the clock. The output of DAC increases with time and the analog output voltage waveform is a rising staircase, as shown in Fig. 9.25.

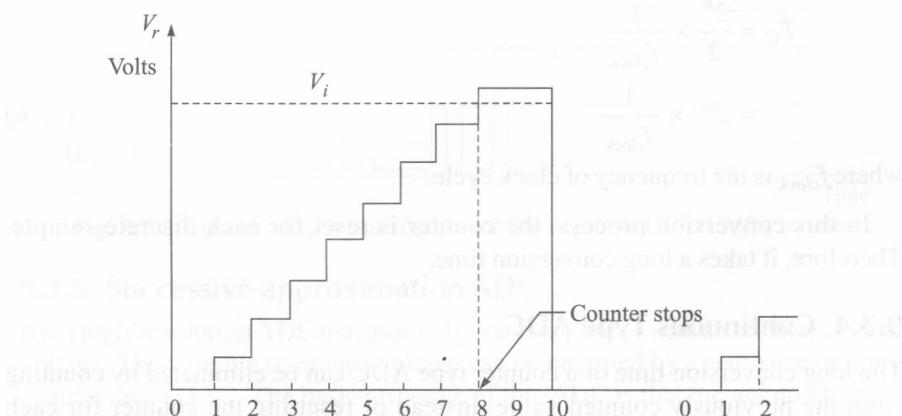


Fig. 9.25 Analog output voltage waveform of DAC

The comparator compares this analog voltage with the analog input voltage V_A . When $V_A > V_r$, the output of comparator is high, enable the AND gate to pass the clock. When $V_A \leq V_r$, the output of comparator is low, disable the AND gate to pass the clock. The binary counter stops counting, and the digital output of DAC represents the analog input voltage.

Let us consider an analog input is 13/16V and the ADC is a 4-bit counter type ADC.

Table 9.4 Counter type conversion sequence

Clock	Digital signal	V_r	V_A		Description
1	0000	0	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
2	0001	1/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
3	0010	2/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
4	0011	3/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
5	0100	4/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
6	0101	5/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
7	0110	6/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
8	0111	7/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
9	1000	8/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
10	1001	9/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
11	1010	10/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
12	1011	11/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
13	1100	12/16	13/16	$V_A > V_r$	Enable the AND gate to pass the clock
14	1101	13/16	13/16	$V_A < V_r$	Disable the AND gate to pass the clock

In this ADC, the counter advances by one count for every clock pulse, therefore the clock speed decides the conversion speed. The conversion time is variable and it is proportional to the amplitude of the analog input voltage. The average conversion time of an n -bit ADC is,

$$T_C = \frac{2^n}{2} \times \frac{1}{f_{\text{clock}}} \\ = 2^{n-1} \times \frac{1}{f_{\text{clock}}} \quad (9.16)$$

where f_{clock} is the frequency of clock cycle.

In this conversion process, the counter is reset for each discrete sample. Therefore, it takes a long conversion time.

9.3.4 Continuous Type ADC

The long conversion time of a counter type ADC can be eliminated by counting from the previously counted value, instead of resetting the counter for each conversion. The block diagram a 4-bit of continuous type ADC is shown in Fig. 9.26.

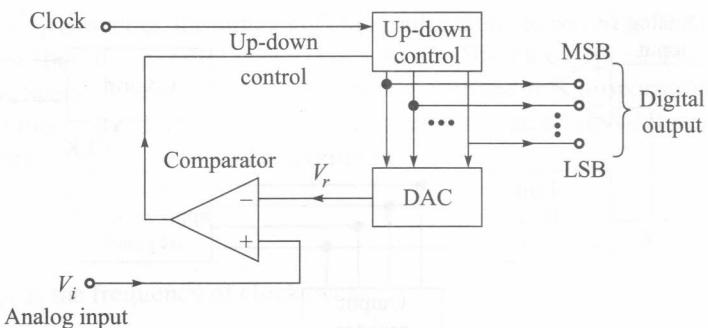


Fig. 9.26 Continuous type ADC

The block diagram consists of a DAC, a comparator, an up-down counter, and a control circuit. The DAC converts the digital data into analog signal, which is given to the inverting terminal of the comparator, and the non-inverting input of the comparator is connected to the unknown analog input voltage V_A . The op-amp is used in open loop. It acts as a comparator and compares the analog input that has to be converted into digital with the analog output of DAC. The control circuit controls the direction of up/down counter based on the result of comparator.

When $V_A > V_r$, the output of comparator is in high state. The counter is then made to count UP and the DAC output increases. The new input data is converted and compared with an unknown analog voltage. This process of counting-up continues, until V_r is less than V_A .

When $V_A < V_r$, the output of comparator is in low state. The counter is then made to count DOWN and the DAC output decreases. The new input data is converted and compared with an unknown analog voltage. This process of counting-down continues, until V_r is greater than V_A . Figure 9.27 shows the analog input signal and the input to up-down counter.

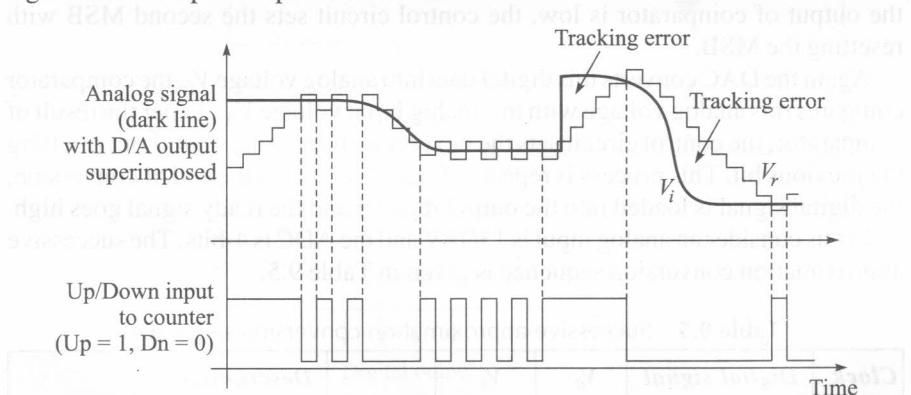


Fig. 9.27 The analog input signal and the input to UP/DOWN counter

9.3.5 Successive-approximation ADC

It is a high-resolution ADC that uses only one comparator with a variable reference voltage. The variable reference voltage can be obtained by a sequence or binary counter and a DAC. The basic principle of this ADC is that the unknown analog input voltage is approximate against an n -bit digital value by trying one bit at time, beginning with the MSB. The block diagram of a 4-bit successive-approximation ADC is shown in Fig. 9.28.

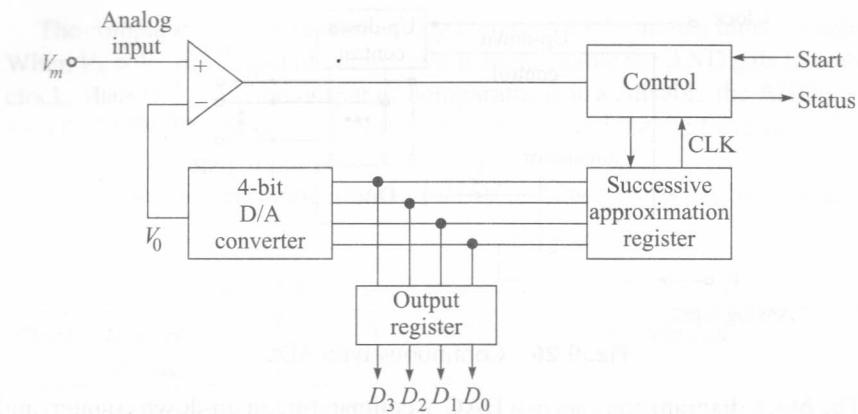


Fig. 9.28 Successive-approximation ADC

The block diagram consists of a DAC, a comparator, a successive-approximation register, a control circuit, and an output register. The DAC converts the digital data into analog signal, which is given as one of the input to the comparator. The op-amp is used in open loop. It acts as a comparator and compares the analog input that has to be converted into digital with the analog output of ADC. The result of the comparator may be $+V_{sat}$ or $-V_{sat}$, i.e. high or low (logic 1 or 0) which controls the control circuit. The control circuit changes the data of successive-approximation register as per the output signal of the comparator, as discussed below.

When the start signal is provided by a user, the MSB of successive-approximation register is set and other bits are reset with a clock pulse. The DAC converts this digital data into analog voltage V_0 , the comparator compares this analog voltage with the analog input voltage V_A . When $V_A > V_0$, the output of comparator is high, the control circuit sets the second MSB without resetting the MSB. When $V_A < V_0$, the output of comparator is low, the control circuit sets the second MSB with resetting the MSB.

Again the DAC converts this digital data into analog voltage V_0 , the comparator compares this analog voltage with the analog input voltage V_A . As per the result of comparator, the control circuit sets the next bit with resetting or without resetting the previous bit. This process is repeated for all the bits. At the end of conversion, the digital signal is loaded into the output register and the ready signal goes high.

Let us consider an analog input is 13/16V and the ADC is 4-bits. The successive approximation conversion sequence is given in Table 9.5.

Table 9.5 Successive-approximation conversion sequence

Clock	Digital signal	V_0	V_A		Description
1	1000	8/16	13/16	$V_A > V_0$	Set the MSB
2	1100	12/16	13/16	$V_A > V_0$	Set the second bit without resetting the MSB
3	1110	14/16	13/16	$V_A < V_0$	Set the next bit without resetting the previous bit
4	1101	13/16	13/16	$V_A = V_0$	Set the next bit with resetting the previous bit

Digital output is 1101.

For an N -bit converter, the number of clock pulse required would be N and hence, it is slower than the parallel comparator ADC. The clock speed decides the conversion speed. The conversion time is constant and it is proportional to the number of bits in the digital output. The conversion time of an N -bit successive approximation analog-to-digital converter is

$$T_C = N \times \frac{1}{f_{\text{clock}}} \quad (9.17)$$

where f_{clock} is the frequency of clock cycle.

9.3.6 Dual Slope ADC

In a dual slope ADC, the integrator generates two different ramps—one with an unknown analog input voltage V_A as the input, and another with a known reference voltage V_{ref} as the input. Hence, it is known as the dual slope ADC. The basic principle of a dual slope ADC is that, an analog signal is converted into a proportional time period, which is then measured using a digital counter. The block diagram of a typical dual slope ADC is shown in Fig. 9.29. It includes an integrator, comparator, counter, control logic, and a reference voltage.

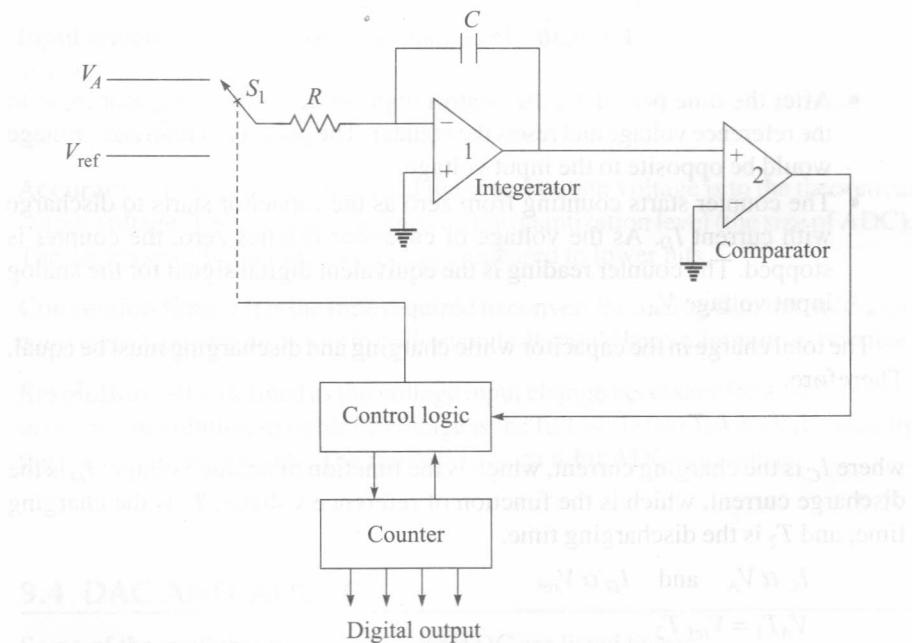


Fig. 9.29 Block diagram of a dual slope ADC

Op-amp 1 with resistor R and capacitor C acts as an integrator and when the input of integrator is connected to the analog input, the capacitor is charged linearly. The voltage across the capacitor depends on the amplitude of the analog input voltage and duration T .

Op-amp 2 is used in open loop. It acts as a comparator and compares the output of integrator with the reference input. The reference voltage is zero and the

comparator acts as a zero crossing detector. The output of the comparator is high or low depending on the voltage across the capacitor. When the voltage across the capacitor reaches zero, the output of the comparator is $-V_{sat}$, which is given to the control logic and the control logic stops the counting of counter.

The conversion process follows three steps.

- The switch S_1 connects the analog voltage V_A as the input to the integrator for a fixed period T_1 . During this period, the capacitor of the integrator is charged up to a certain voltage with charging current I_C , which is the function of analog input voltage, as shown in Fig. 9.30.

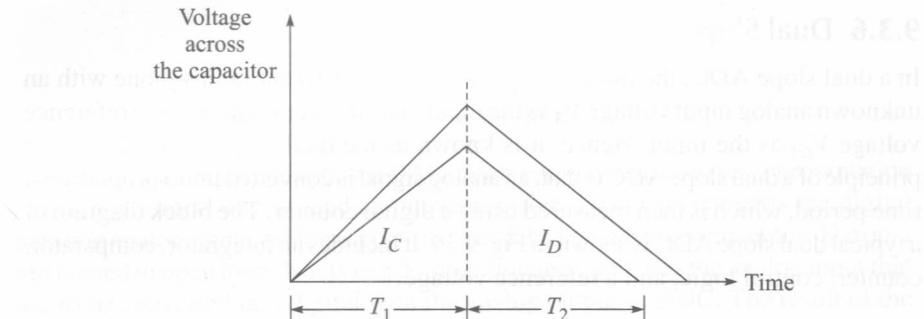


Fig. 9.30 Dual ramp waveform

- After the time period T_1 , the control logic switches the integrator input to the reference voltage and resets the counter. The polarity of reference voltage would be opposite to the input voltage.
- The counter starts counting from zero as the capacitor starts to discharge with current I_D . As the voltage of capacitor reaches zero, the counter is stopped. The counter reading is the equivalent digital signal for the analog input voltage V_A .

The total charge in the capacitor while charging and discharging must be equal. Therefore,

$$I_C T_1 = I_D T_2$$

where I_C is the charging current, which is the function of analog voltage; I_D is the discharging current, which is the function of reference voltage; T_1 is the charging time; and T_2 is the discharging time.

$$I_C \propto V_A \quad \text{and} \quad I_D \propto V_{ref}$$

$$V_A T_1 = V_{ref} T_2$$

$$T_2 = \frac{T_1}{V_{ref}} \times V_A \quad (9.17)$$

The period T_1 and the reference voltage V_{ref} are constant.

$$\Rightarrow \left(\frac{T_1}{V_{ref}} \right) = K$$

Using this in Eq. (9.17), we get

$$T_2 = KV_A \quad (9.18)$$

Thus, time period T_2 is proportional to analog voltage V_A and the counter measures the period T_2 . Hence, the content of counter is the equivalent digital signal for the analog input V_A .

The accuracy of this ADC is high as compared to a successive-approximation ADC, but its speed is slow.

9.3.7 Specifications for ADC

The following specifications are usually specified by the manufacturers of ADC.

- Range of input voltage
- Input impedance
- Accuracy
- Conversion time
- Resolution
- Differential linearity

Range of input voltages The input signal given to the ADC is an analog signal. The amplitude of a signal is the function of time. The range of the input voltage is defined by the maximum and minimum amplitude of an analog signal, which can be applied to the ADC for reliable operation.

Input impedance ADC is mainly used to interface the analog circuit with a digital system. To avoid the problem of loading, the output impedance of analog circuit should be matched with the input impedance of an ADC and hence, it is required to specify the input impedance of an ADC.

Accuracy It measures how closed the actual output voltage is to the theoretical output voltage. The accuracy depends on the quantization level (the size of ADC). The accuracy of higher bits is more as compared to lower bits.

Conversion time It is the time required to convert the analog data into its digital equivalent. Conversion time is in milliseconds. It should be as minimum as possible.

Resolution It is defined as the voltage input change necessary for a 1-bit change in output. Resolution in terms of voltage is the full-scale input voltage divided by the total number of levels. The resolution of an n -bit ADC is given as,

$$\text{Resolution} = V/(2^n - 1) \quad (9.19)$$

9.4 DAC AND ADC ICs

Some of the available ICs of DAC and ADC are listed below.

IC number	Description
AD DAC 80	12-bit DAC
AD 7522	10-bit DAC
AD 558	8-bit DAC
ADC 0809	8-bit ADC
AD ADC 80	12-bit ADC
ADC-7109	12-bit binary ADC

9.5 ADC 0809 (8-BIT ADC)

Introduction

The ADC 0809 data acquisition component is a monolithic CMOS device with an 8-bit ADC, an 8-channel multiplexer, and a microprocessor-compatible control logic. The 8-bit ADC uses successive approximation as the conversion technique. The converter features a high-impedance chopper-stabilized comparator, a 256R voltage divider with analog switch tree and a successive-approximation register. The 8-channel multiplexer can directly access any one of the 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TIL TRI-STATE outputs. Incorporating the most desirable aspects of several A/D conversion techniques has optimized the design of ADC 0809. It offers high-speed, high-accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited from applications from process and machine control to consumer and automotive applications.

Features

1. Easy interface to all microprocessors
2. Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
3. No zero or full-scale adjustment required
4. 8-channel multiplexer with address logic
5. 0 V to 5 V input range with single 5 V power supply
6. Outputs meet TTL voltage level specifications
7. Standard hermetic or molded 28-pin DIP package
8. 28-pin molded IC carrier package
9. Resolution 8 bits
10. Total unadjusted error $\pm 1/2$ LSB and ± 1 LSB
11. Single supply 5 V_{DC}
12. Low power 15 mW
13. Conversion time 100 μ s

Functional block diagram of ADC 0809

Figure 9.31 shows the block diagram of ADC 0809.

Multiplexer

The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table 9.6 shows the input states for the address lines to select any channel. The address is latched into the decoder on low-to-high transition of the address latch enable signal.

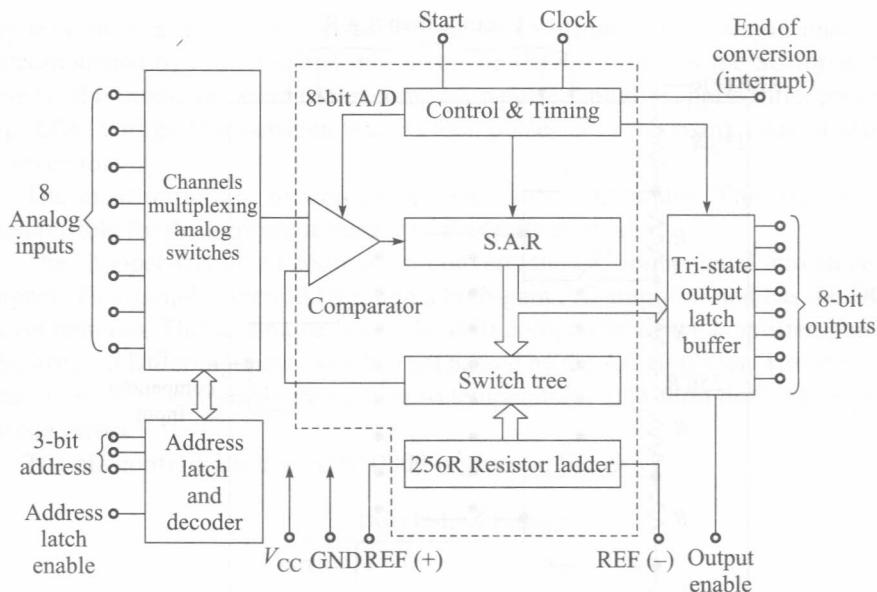


Fig. 9.31 Block diagram of ADC 0809

Table 9.6 Input states for the address lines to select channel

Selected analog channel	Address line		
	C	B	A
IN0	0	0	0
IN1	0	0	1
IN2	0	1	0
IN3	0	1	1
IN4	1	0	0
IN5	1	0	1
IN6	1	1	0
IN7	1	1	1

Converter characteristics

The heart of this single IC data acquisition system is its 8-bit ADC. The converter is designed to provide fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into three major sections, the 256R ladder network, the successive-approximation register, and the comparator.

The 256R ladder network approach shown in Fig. 9.32 was chosen over the conventional $R/2R$ ladder network because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in Fig. 9.32 are not the same value as the remainder of the network. The difference in these resistors causes the output characteristics to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has

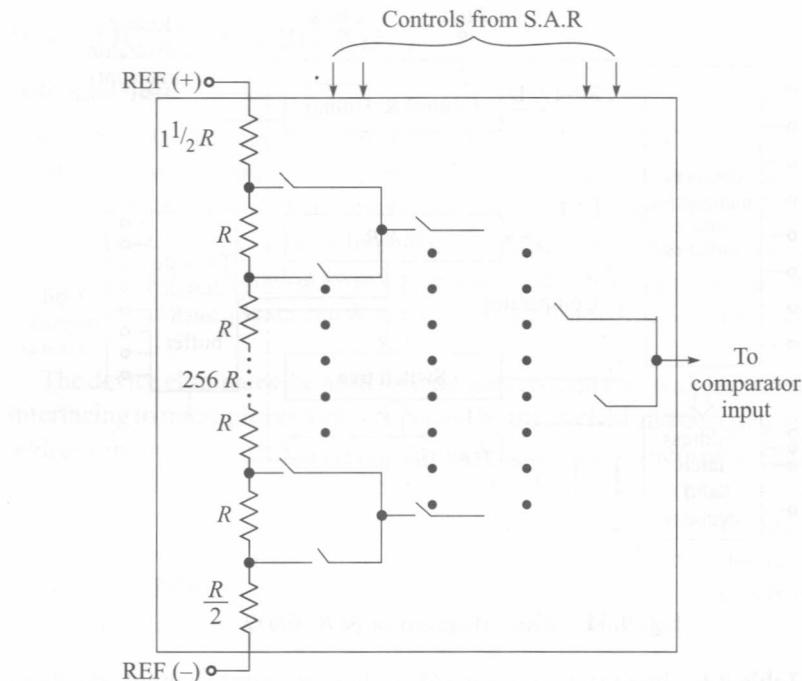


Fig. 9.32 256R ladder network approach

reached $+1/2$ LSB and the succeeding output transition occurs every 1 LSB up to full-scale.

The successive approximation register (SAR) performs eight iterations to approximate the input voltage. For any type SAR converter, n -iterations are required for an n -bit converter. Figure 9.33 shows a typical example of a 3-bit converter. In ADC 0809, the approximation technique is extended to 8-bits using the 256R network.

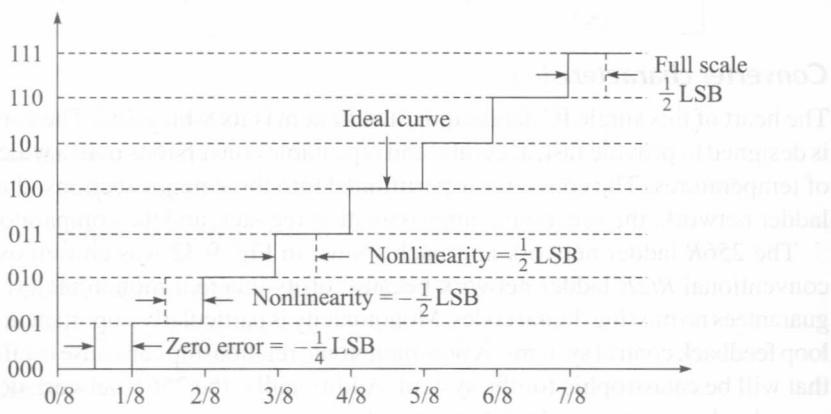


Fig. 9.33 3-bit transfer curve

The ADC successive approximation register (SAR) of ADC is reset on the positive edge of the start conversion (SC) pulse. The conversion process starts at the falling edge of the start conversion pulse. A conversion process will be interrupted

by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output of the SC input. If used in this mode, an external start conversion pulse should be applied after power up. EOC will go low between 0 to 8 clock pulses after the rising edge of start conversion.

The most important section of an ADC is its comparator. This section is responsible for the ultimate accuracy of the entire converter.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high-gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier, since the drift is a DC component, which is not passed by the AC amplifier. This makes the entire ADC extremely insensitive to temperature, long-term drift, and input offset errors.

The pin configuration of ADC 0809 is given in Fig. 9.34.

Dual-In-Line Package	
IN3	1
IN4	2
IN5	3
IN6	4
IN7	5
Start	6
EOC	7
2^{-5}	8
Output Enable	9
Clock	10
V_{CC}	11
$V_{Ref}(+)$	12
GND	13
2^{-7}	14
0809	
IN2	28
IN1	27
IN0	26
ADD A	25
ADD B	24
ADD C	23
ALE	22
2^{-1} MSB	21
2^{-2}	20
2^{-3}	19
2^{-4}	18
2^{-8} LSB	17
$V_{Ref}(-)$	16
2^{-6}	15

Fig. 9.34 Pin configuration of ADC 0809

The timing diagram is given in Fig. 9.35.

9.6 ADC-7109 (12-BIT BINARY ADC)

Introduction

The IC L 7109 is a high performance, low power integrating 12-bit ADC, designed to easily interface with microprocessors.

The output data (12-bits), polarity, and over-range may be directly accessed under the control of two byte enable inputs and an IC select input for a simple parallel bus interface. A UART handshake mode is provided to allow the IC 7109 to work with industry-standard UARTs in providing serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

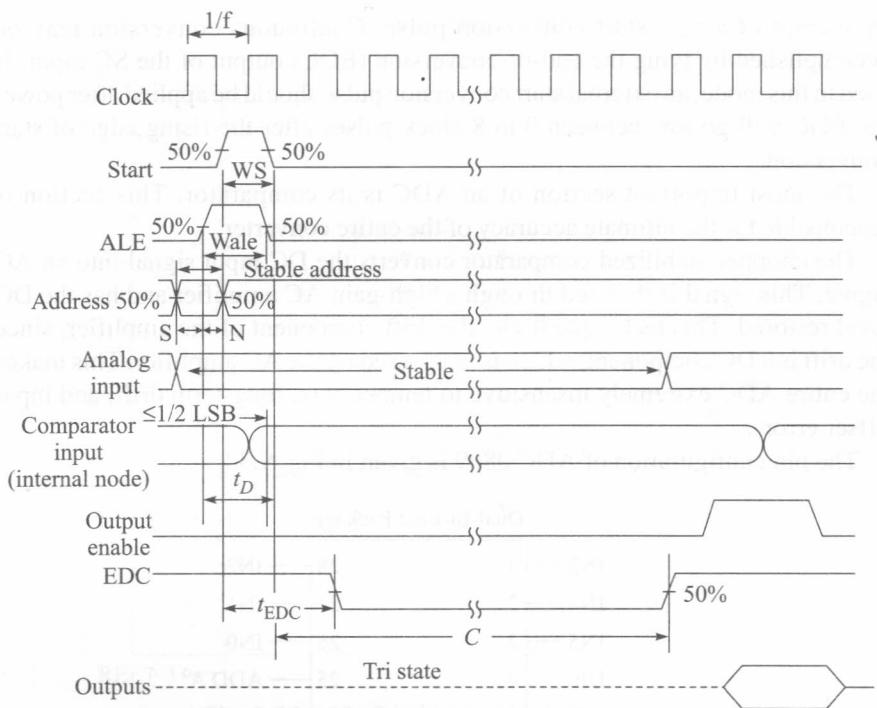


Fig. 9.35 Timing diagram of ADC 0809

IC 7109 provides the user with high accuracy, low noise, low drift, versatility, and economy of the dual-slope integrating ADC. Features like true differential input and reference, less than $1\mu\text{V}/^\circ\text{C}$ drift, maximum input bias current of 10 pA , and typical power consumption of 20 mW make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

Features

1. 12-bit binary (plus polarity and over-range) dual-slope integrating ADC.
2. Byte-organized TTL compatible 3-state outputs and UART handshake mode for simple, parallel, or serial interfacing to microprocessor systems.
3. RUN/HOLD input and STATUS output can be used to monitor and control conversion timing.
4. True differential input and differential reference.
5. Low noise—typically $15\text{ }\mu\text{V}$ p-p.
6. 1 pA typical input current.
7. Operates at up to 30 conversions per second.
8. On-IC oscillator operates with inexpensive 3.58 MHz TV crystal giving 7.5 conversions per second for 60 Hz rejections. May also be operated as RC oscillator for other clock frequencies.
9. Fabricated using MAX-CMOS technology combining analog and digital functions on a single low-power LSI CMOS IC.
10. All inputs are fully protected against static discharge, no special handling precautions necessary.

Figure 9.36 shows the pin configuration and test circuit of IC 7109.

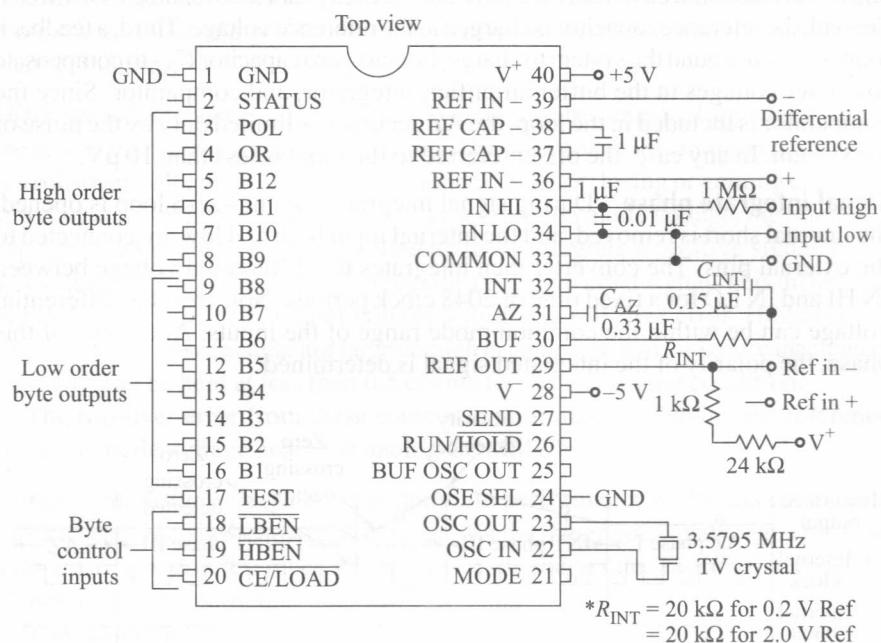


Fig. 9.36 Pin configuration and test circuit of IC 7109

Functional block diagram of IC 7109

Analog section Figure 9.37 shows the equivalent circuit of the analog section of IC 7109. When the RUN/HOLD input is left open or connected to V⁺, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases, as shown in Fig. 9.38. They are (i) Auto-zero (AZ), (ii) Signal integrate (INT), and (iii) De-integrate (DE).

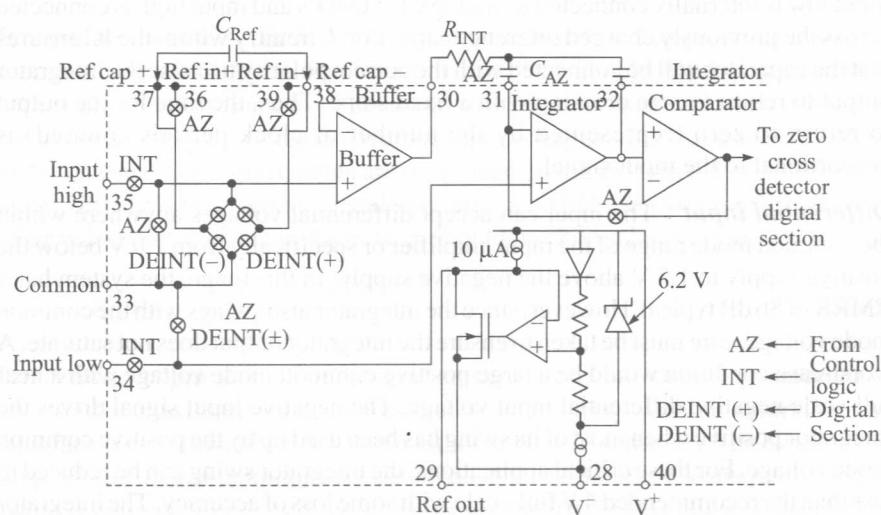


Fig. 9.37 Analog section of IC 7109

Auto-zero phases During auto-zero, three things happen. First, the input high and low are disconnected from their pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than $10 \mu V$.

Signal integrate phase During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time of 2048 clock periods. Note that this differential voltage can be within the common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

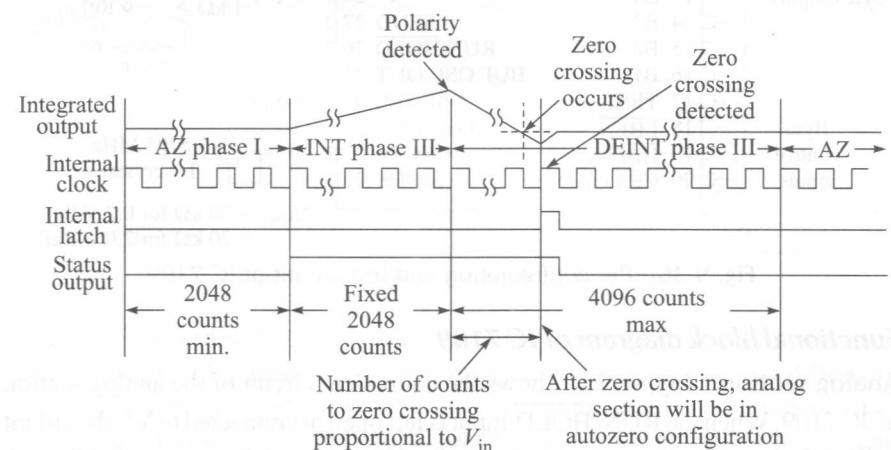


Fig. 9.38 Conversion timing RUN/HOLD pin high

De-integrate phase The final phase is de-integrated, or reference integrated. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the IC ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing with a fixed slope. Thus, the time for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

Differential input The input can accept differential voltages anywhere within the common mode range of the input amplifier or specifically from 1.0 V below the positive supply to 1.5 V above the negative supply. In this range, the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be taken to ensure the integrator output does not saturate. A worst-case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications, the integrator swing can be reduced to less than the recommended 4 V full-scale with some loss of accuracy. The integrator output can swing within 0.3 V of either supply without loss of linearity.

The IC7109 has however been optimized for operation with analog COMMON near digital ground. With power supplies of + 5 V and -5 V, it allows a 4 V full-scale integrator swing positive or negative, maximizing the performance of the analog section.

Differential reference The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor, losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge when called up to de-integrate a positive signal, but it loses charge when called up to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held at less than 0.5 counts for the worst-case condition.

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

Component value selection For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing be as large as possible. For example, with ± 5 V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ± 4 V. Since the integrator output can go to 0.3 V from either supply without significantly affecting linearity, a 4 V integrator output swing allows 0.7 V for variations in output swing due to component value and oscillator tolerances. With ± 5 V supplies and a common mode range of ± 1 V required, the component values should be selected to provide ± 3 V integrator output swing. Noise and roll-over errors will be slightly worse than in the ± 4 V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and roll-over errors. To improve the performance, supplies of ± 6 V may be used.

Integrating resistor Both the buffer amplifier and the integrator have a class A output stage with $100\ \mu\text{A}$ of quiescent current. They supply $20\ \mu\text{A}$ of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough so that undue leakage requirements are not placed on the PC board. For 4.096 V full scale, $200\ \text{k}\Omega$ is near optimum and similarly, a $20\ \text{k}\Omega$ for a 409.6 mV scale. For other values of full-scale voltage, R_{INT} should be chosen by the relation,

$$R_{\text{INT}} = \frac{\text{Full-scale voltage}}{20\ \mu\text{A}} \quad (9.20)$$

Integrating capacitor The integrating capacitor C_{INT} should be selected to provide the maximum integrator output voltage swing without saturating the integrator approximately 0.3 V from either supply. For the ICL7109 with ± 5 V supplies and analog common connected to GND, a ± 3.5 to ± 4 V integrator output swing is nominal. For $7^{1/2}$ conversions per second (61.72 kHz clock frequency) as provided by the crystal oscillator, the nominal values for C_{INT} and C_{AZ} are $0.15\ \text{mF}$.

and 0.33 mF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of C_{INT} is given by,

$$C_{INT} = \frac{(2048 \times \text{clock period})(20 \mu\text{A})}{\text{integrator output voltage swing}} \quad (9.21)$$

An additional requirement of the integrating capacitor is that it has low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. For the military temperature range, Teflon capacitors are recommended.

Auto-zero capacitor The size of auto-zero capacitor has some influence on the noise of the system—a big capacitor produces less noise. However, it cannot be increased without limits since it, in parallel with the integrating capacitor, forms an R-C time constant that determines the speed of recovery from overloads and more important, the error that exists at the end of an auto-zero cycle. For 409.6 mV full-scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096 V full-scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended. For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon or equivalent capacitors are recommended above 85°C for their low leakage characteristics.

Reference capacitor A 1 μF capacitor gives good results in most applications. However, where a large common mode voltage exists and a 409.6 μV scale is used, a larger value is required to prevent roll-over error. Generally 10 μF will hold the roll-over error to 0.5 count in this instance. Again, Teflon or equivalent capacitors should be used for temperatures above 85°C for their low leakage characteristics.

Reference voltage The analog input required to generate a full-scale output of 4096 counts is $V_{IN} = 2V_{REF}$. Thus for a normalized scale, a reference of 2.048 V should be used for a 4.096 V full-scale, and 204.8 mV should be used for a 0.4096 V full-scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682 V. Instead of dividing the input down to 409.6 mV, the input voltage should be measured directly and a reference voltage of 0.341 V should be used. Suitable values for integrating resistor and capacitor are 34 K and 0.15 mF. This avoids a divider on the input. Another advantage of this system is when a zero reading is desired for a non-zero input. Temperature and weight measurements with an offset are the examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling subtraction digitally using software.

Digital section The digital section includes the clock oscillator and a scaling circuit, a 12-bit binary counter with output latches and TTL compatible 3-state output driver's polarity, over-range and control logic, and UART handshake logic, as shown in Fig. 9.39.

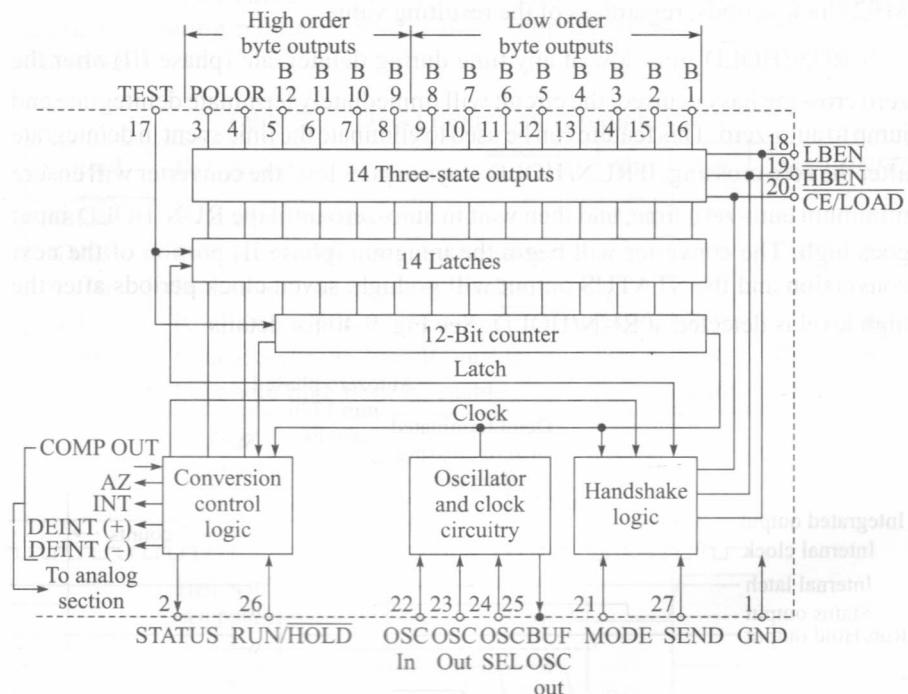


Fig. 9.39 Digital section of IC 7109

Throughout this description, logic levels will be referred to as *low* or *high*. For minimum power consumption, all inputs should swing from GND (low) to V^+ (high). Inputs driven from TTL gates should have $3.5\text{ k}\Omega$ pull-up resistors added for maximum noise immunity.

MODE input The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pull-down resistor to ensure a low level when the pin is left open), the converter is in its *direct* output mode, where the output data is directly accessible under the control of the IC and byte enables inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to *direct* mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle.

STATUS output During a conversion cycle, the STATUS output goes high at the beginning of signal integrate (phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Fig. 9.36 for details of this timing. This signal may be used as a *data valid* flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/HOLD input When the RUN/HOLD input is high or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the deintegrate (phase III) portion of the conversion cycle (see Fig. 9.36). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If RUN/HOLD goes low at any time during deintegrate (phase III) after the zero crossing has occurred, the circuit will immediately terminate deintegrate and jump to auto-zero. This feature can be used to eliminate the time spent in deintegrate after the zero crossing. If RUN/HOLD stays or goes low, the converter will ensure minimum auto-zero time, and then wait in auto-zero until the RUN/HOLD input goes high. The converter will begin the integrate (phase II) portion of the next conversion and the STATUS output will go high, seven clock periods after the high level is detected at RUN/HOLD. See Fig. 9.40 for details.

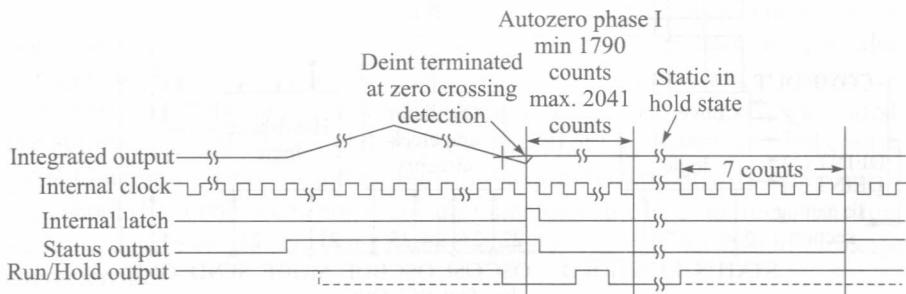


Fig. 9.40 RUN/HOLD operation

Using the RUN/HOLD input, in this manner, allows an easy *convert on demand* interface to be used. The converter may be held at idle in auto-zero with RUN/HOLD low. When RUN/HOLD goes high, the conversion is started, and when the STATUS output goes low, the new data is valid (or transferred to the UART, see Handshake Mode). RUN/HOLD may now go low terminating deintegrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion.

Alternately, RUN/HOLD can be used to minimize the conversion time by ensuring that it goes low during deintegrate, after zero crossing and goes high after the hold point is reached. The required activity on the RUN/HOLD input can be provided by connecting it to the Buffered Oscillator Output. In this mode, the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A032 for a discussion of the effects this will have on auto-zero performance.

If the RUN/HOLD input goes low and stays low during auto-zero (phase I), the converter will simply stop at the end of auto-zero and wait for RUN/HOLD to go high. As above, integrate (phase II) begins seven clock periods after the high level is detected.

Direct mode When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low-order byte, bits 9 through 12, polarity and over-range high-order

byte) are accessible under the control of the byte and IC enable terminals as inputs. These three inputs are all active low, and are provided with pull-up resistors to ensure an inactive high level when left open. When the IC enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-started on). This allows a variety of parallel data accessing techniques to be used. The timing requirements for these outputs are shown in Fig. 9.41 and Table 9.6.

Table 9.6 Direct mode timing requirements

Symbol	Description	Min	Typ	Max	UNITS
tBEA	Byte enable width	350	220		ns
tDAB	Data access time from byte enable		210	350	ns
tDHB	Data hold time from byte enable		150	300	ns
tCEA	IC enable width	400	260		ns
tDAC	Data access time from IC enable		260	400	ns
tDHC	Data hold time from IC enable		240	400	ns

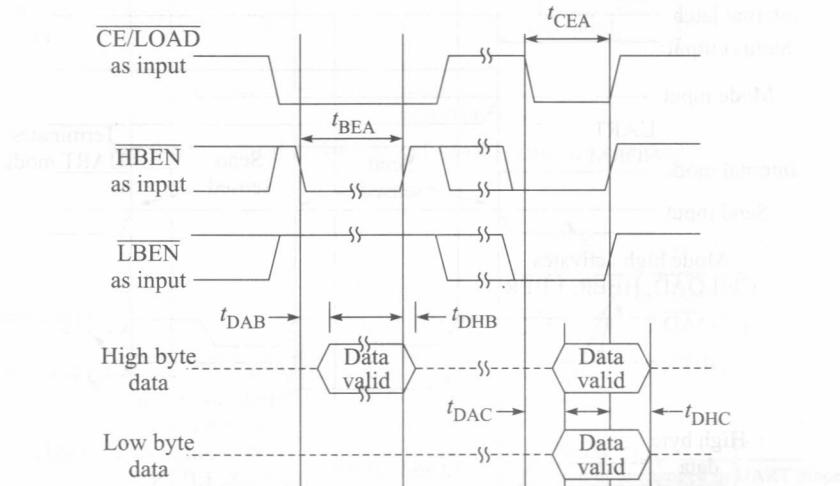


Fig. 9.41 Direct mode output timing

It should be noted that these control inputs are asynchronous with respect to the converter clock—the data may be accessed any time. Thus, it is possible to access the data while it is being updated, which can lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

Handshake mode The handshake output mode is provided as an alternative means of interfacing the IC 7109 to digital systems, where the ADC becomes active in controlling the flow of data instead of passively responding to IC and byte enable inputs. This mode is specifically designed to allow a direct interface between the IC 7109 and industry standard UARTs (such as the intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the IC 7109 provides all the control and flag signals necessary to sequence

the two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, IC 7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (see Figs. 9.42 and 9.43). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode.

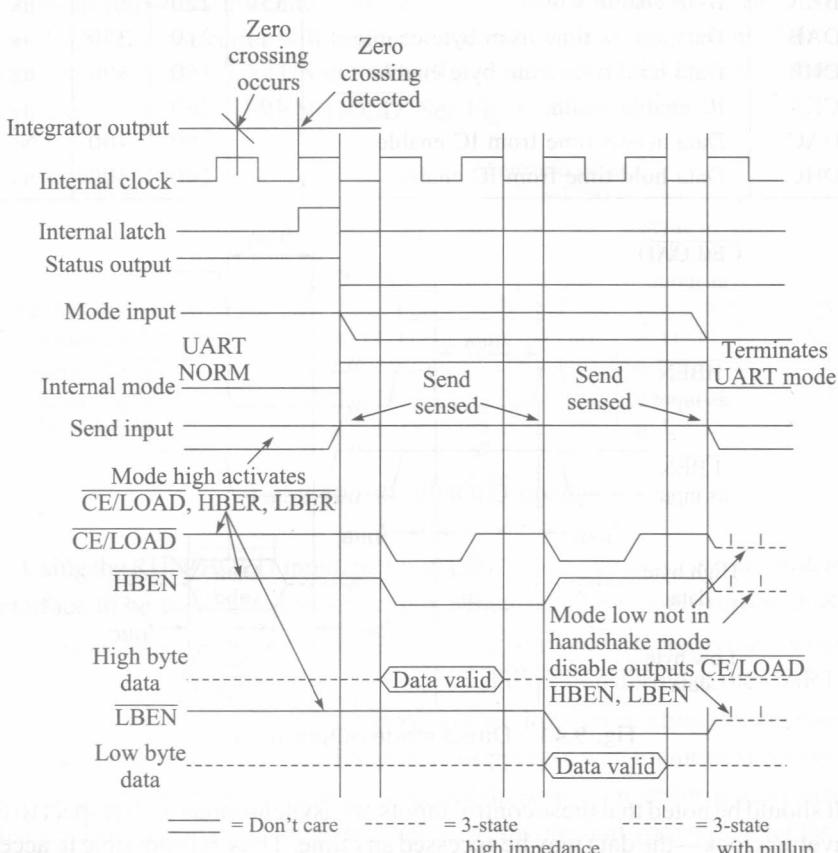
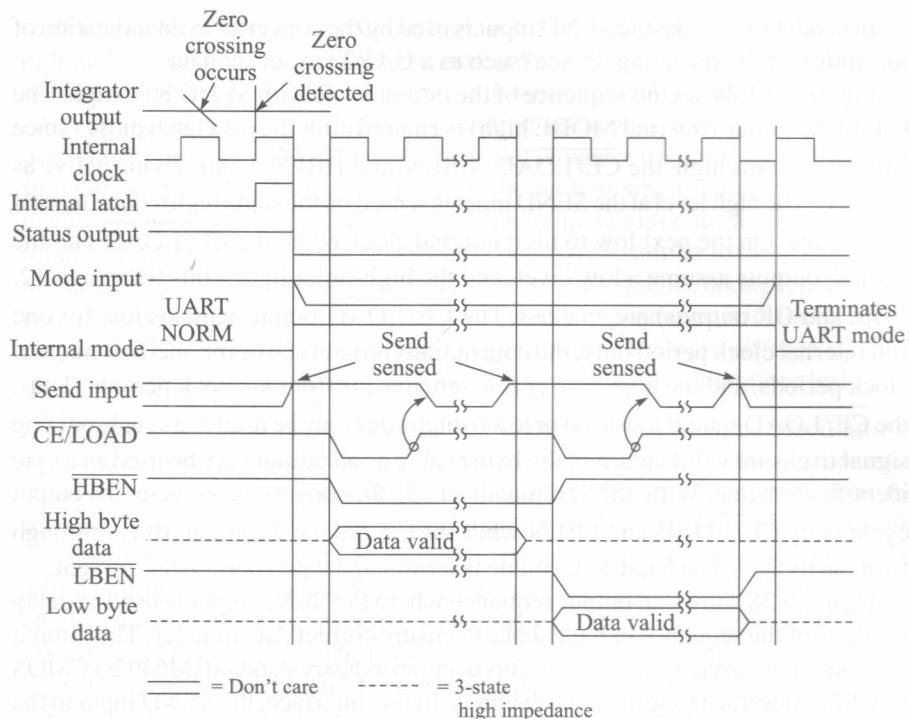
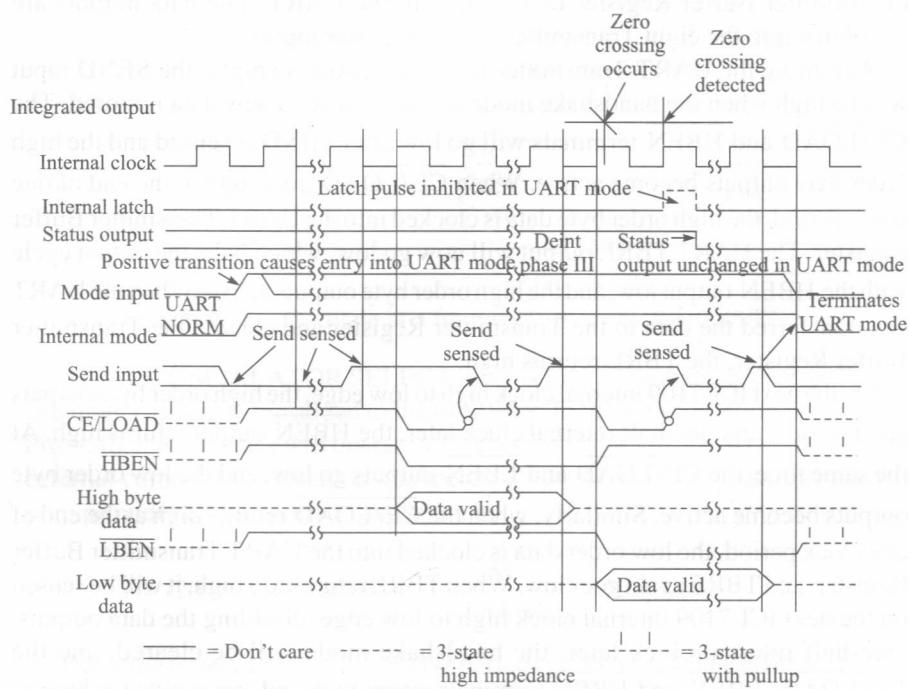


Fig. 9.42 Handshake with SEND held positive

If this pulse occurs while a new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (see Fig. 9.44) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the IC and byte enable terminals become TTL compatible outputs, which provide the control signals for the output cycle (see Figs. 9.43, 9.44, and 9.45).

**Fig 9.43** Handshake typical UART interface timing**Fig. 9.44** Handshake triggered by mode

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

Figure 9.42 shows the sequence of the output cycle with SEND held high. The handshake mode (internal MODE high) is entered after the data latch pulse (since MODE remains high, the CE/LOAD, LBEN and HBEN terminals are active as outputs). The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the CE/LOAD and the HBEN outputs assume a low level, and the high-order bytes (bits 9 through 12, POL, and OR outputs) are enabled. The CE/LOAD output remains low for one full internal clock period only, the data outputs remain active for one-half internal clock periods, and the high byte enable remains low for two clock periods. Thus, the CE/LOAD output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high, the converter completes the output cycle using CE/LOAD and LBEN while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 9.38 shows an output sequence where the SEND input is used to delay portions of the sequence or handshake to ensure correct data transfer. This timing diagram shows a relationship that occurs using an industry standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the CE/LOAD terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after a new data is stored. The CE/LOAD and HBEN terminals will go low after SEND is sensed and the high order byte outputs become active. When CE/LOAD goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the HBEN output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high.

On the next ICL7109 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the HBEN output returns high. At the same time, the CE/LOAD and LBEN outputs go low, and the low order byte outputs become active. Similarly, when the CE/LOAD returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high, it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the CE/LOAD, LBEN and HBEN terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9.42 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/HOLD input functioning normally. The only difference is that new data will not be latched when in handshake mode and is therefore lost.

Oscillator IC 7109 is provided with a versatile three-terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

When the OSCILLATOR SELECT input is high or left open, the input is provided with a pull-up resistor, the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Fig. 9.45. The circuit will oscillate at a frequency given by $f = 0.45/RC$. A 100 k Ω resistor is recommended for useful ranges of frequency. For optimum 60 Hz line rejection, the capacitor value should be chosen such that 2048 clock period is close to an integral multiple of the 60 Hz period (but not less than 50 pF).

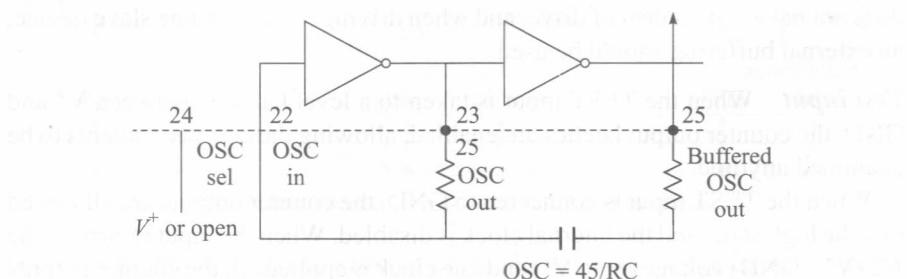


Fig. 9.45 Oscillate at a frequency given by $f = 0.45/RC$

When the OSCILLATOR SELECT input is low, a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Fig. 9.46, the oscillator will operate with crystals in the 1 to 50 MHz range with no external components. Using an inexpensive 3.58 MHz TV crystal, this division ratio provides an integration time given by,

$$T = (2048 \text{ clock periods}) \times \left(\frac{58}{3.58 \text{ MHz}} \right) = 33.18 \text{ ms} \quad (9.22)$$

This time is very close to two 60 Hz periods or 33.33 ms. The error is less than one percent, which will give better than 40 dB 60 Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8 kHz.

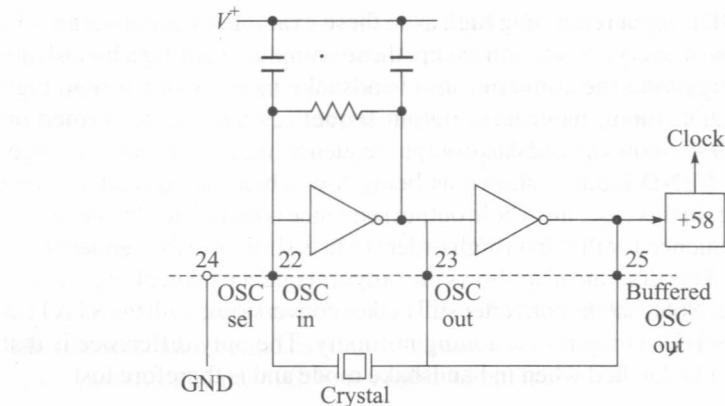


Fig. 9.46 Oscillator with feedback

If at any time, the oscillator is to be overdriven, the over-driving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle and phase as the input signal when the OSCILLATOR SELECT is left open. When the OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL 7109 with the IM6403 UART, it is possible to use one 3.58 MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive, and when driving more than one slave device, an external buffering should be used.

Test input When the TEST input is taken to a level halfway between V^+ and GND, the counter output latches are enabled, allowing the counter contents to be examined anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the $1/2(V^+ - \text{GND})$ voltage (or to V^+) and one clock is applied, all the counter outputs will be clocked to the low state. This allows easy testing of the counter and its outputs.

Interfacing

Direct mode Figure 9.47 shows some of the combinations of IC enable and byte enable control signals, which may be used when interfacing the ICL7109 with parallel data lines. The CE/LOAD input may be tied low, allowing either byte to be controlled by its own enable, as in Fig. 9.47(a). Figure 9.47(b) shows a configuration where the two byte enables are connected together. In this configuration, the CE/LOAD serves as an IC enable, and the HBEN and LBEN may be connected to GND or serve as a second IC enable. The 14 data outputs will all be enabled simultaneously. Figure 9.47(c) shows the HBEN and LBEN as flag inputs, and CE/LOAD as a master enable, which could be the READ strobe available from most microprocessors.

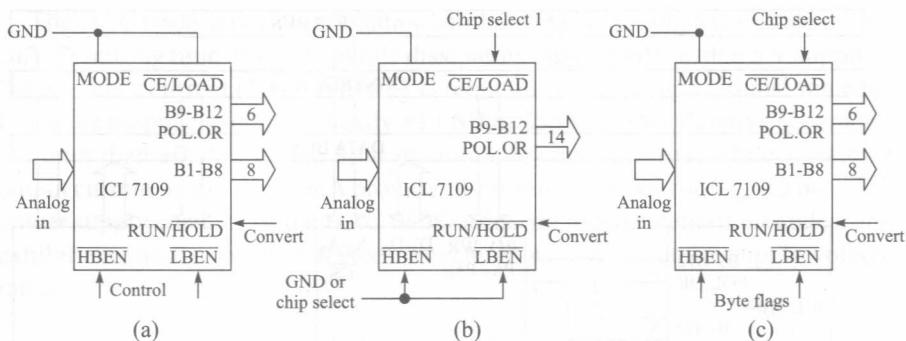


Fig. 9.47 Direct IC mode and byte enable combinations

Figure 9.48 shows an approach of interfacing several ICL7109 to a bus, ganging the HBEN and LBEN signals to several converters together, and using the CE/LOAD inputs (perhaps decoded from an address) to select the desired converter.

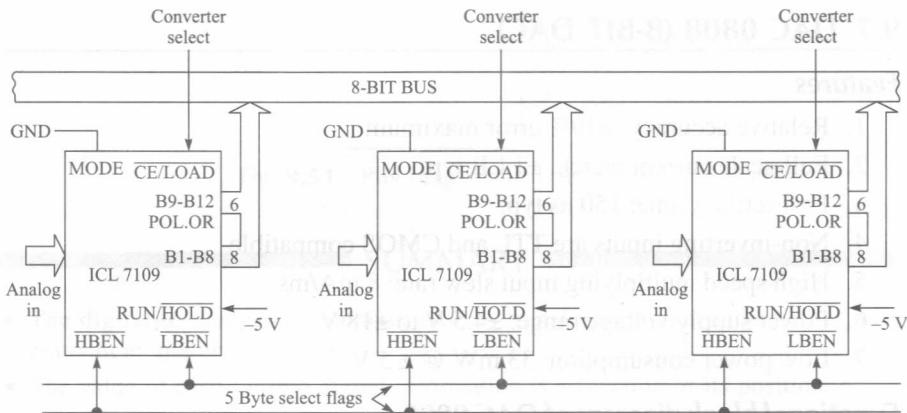


Fig. 9.48 Interfacing several ICL7109 to a bus

Handshake mode The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by using the edge of CE / LOAD and the byte enables may be used as byte identification flags or as load enables.

Figure 9.49 shows a handshake interface to intel microprocessors, again using an 8255 PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL 7109, and using the CE/LOAD to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobe into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ICL 7109 to sequence into the next byte. This figure shows the MODE input to the ICL 7109 connected to a control line on the PPI.

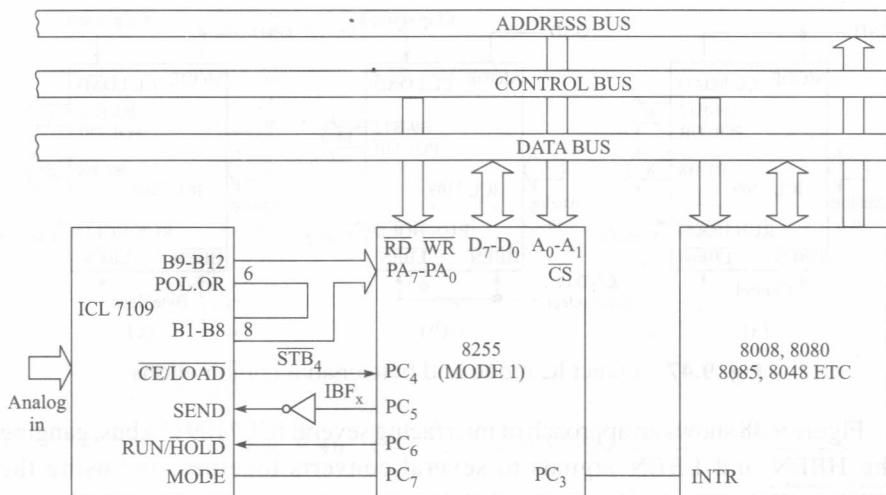


Fig. 9.49 Handshake interface to Intel microprocessors

9.7 DAC 0808 (8-BIT DAC)

Features

1. Relative accuracy: $\pm 19\%$ error maximum
2. Full-scale current match: ± 1 LB typ.
3. Fast settling time: 150 ns typ.
4. Non-inverting inputs are TTL and CMOS compatible
5. High speed multiplying input slew rate: 8 mA/ms
6. Power supply voltage range: ± 4.5 V to ± 18 V
7. Low power consumption: 33 mW @ ± 5 V

Functional block diagram of DAC 0808

The block diagram of DAC 0808 is shown in Fig. 9.50 and its pin configuration is shown in Fig. 9.51.

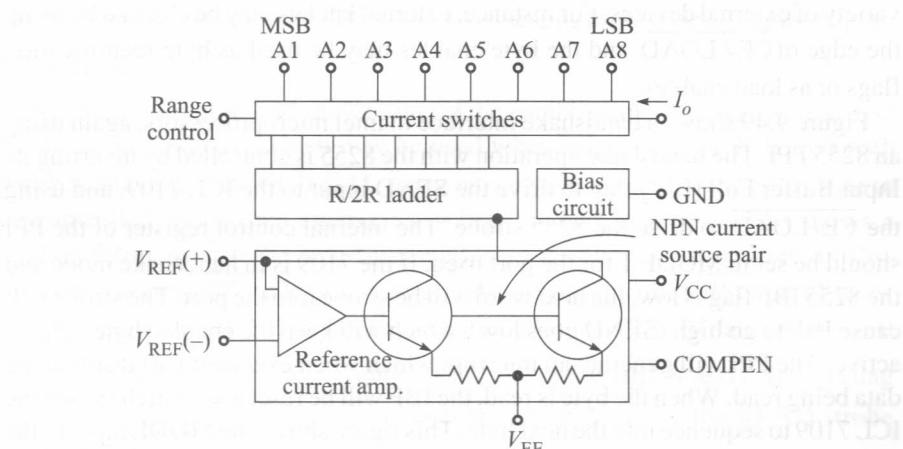


Fig. 9.50 Block diagram of DAC 0808

The DAC 0808 series is an 8-bit monolithic DAC featuring a full-scale output current settling time of 150 ns, while dissipating only 33 mW with ± 5 V supplies. No reference current (I_{REF}) trimming is required for most applications, since the full-scale output current is typically ± 1 LSB of $255 I_{REF}/256$. Relative accuracies of better than $\pm 0.19\%$ assure 8-bit monotonicity and linearity, while zero level output current of less than 4 mA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC 0808 series are independent of bit codes, and exhibit essentially constant device characteristics over the entire supply voltage range.

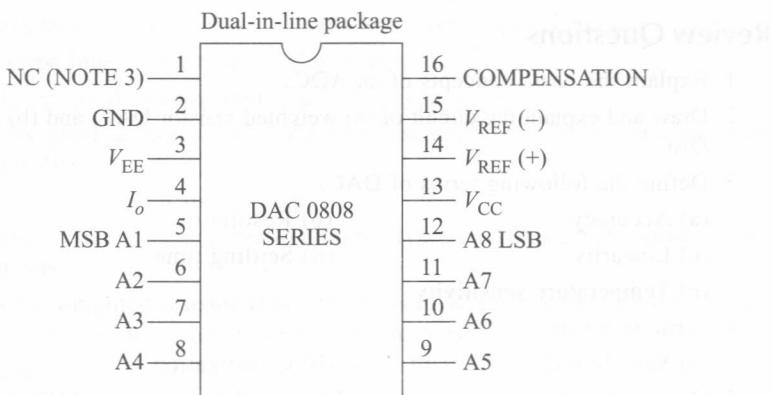


Fig. 9.51 PIN diagram of DAC 0808

SUMMARY

- The digital-to-analog conversion involves translating digital information into equivalent analog information.
- The value of each bit in a digital information is a function of its position.

$$1. \text{ The value of LSB is } \frac{V_m}{2^n}$$

$$2. \text{ The value of second LSB is } \frac{2^1 \cdot V_m}{2^n}$$

$$3. \text{ The value of } N\text{th LSB is } \frac{2^{N-1} \cdot V_m}{2^n}$$

where n is the number of bits of a digital signal and V_m is the maximum amplitude. The output analog voltage V_A is

$$V_A = \left[V_{D0} 2^0 + V_{D1} 2^1 + V_{D2} 2^2 + \dots + V_{D(n-1)} 2^{n-1} \right] \frac{V_m}{2^n}$$

where $V_{D0}, V_{D1}, V_{D2}, \dots, V_{D(n-1)}$ are the digital inputs of n -bit DAC.

- The circuits of DAC are two types: (a) resistor divider DAC, and (b) R/2R ladder network DAC.

- The characteristics of a DAC which are generally specified by the designers are
 - (a) Accuracy, (b) Resolution, (c) Linearity, (d) Settling time, and (e) Temperature sensitivity.
- In case of an ADC, the input analog voltage can have any value in a range and the digital output can have only 2^N discrete values for an N -bit ADC.
- Commonly used ADCs are: (a) Parallel comparator ADC, (b) Successive approximation ADC, and (c) Dual slope ADC.

EXERCISE

Review Questions

- Explain the basic concepts of an ADC.
- Draw and explain the circuit of (a) weighted resistor DAC, and (b) $R-2R$ ladder DAC.
- Define the following terms of DAC.

(a) Accuracy	(b) Resolution
(c) Linearity	(d) Settling time
(e) Temperature sensitivity	
- Write notes on

(a) Sample-and-hold circuit	(b) Quantization
-----------------------------	------------------
- Draw and explain the circuit of (a) 4-bit parallel comparator ADC (b) Successive approximation ADC, and (c) Dual slope ADC.
- Calculate the values of LSB, MSB, and full-scale output for an 8-bit DAC for 0–12V range.
- Find the output voltage for a 4-bit ladder, having the digital inputs

(a) 1010	(b) 0110	(c) 1001	(d) Full-scale output
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 Assume logic 0 = 0V and logic 1 = 12V.

Multiple-Choice Questions

- Among the following, the slowest ADC is

(a) parallel-comparator (i.e. Flash) type	(b) successive-approximation type
(c) integrating type	(d) counting type
- The number of comparisons carried out in a 4-bit Flash type ADC is

(a) 16	(b) 15	(c) 4	(d) 4
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- A 10-bit converter is used to digitize an analog signal in the 0 to 5V range. The maximum peak-to-peak ripple voltage that can be allowed in the dc supply voltage is

(a) nearly 100 mV	(b) nearly 50 mV
(c) nearly 25 mV	(d) nearly 5 mV
- The number of comparators in a parallel conversion type 8-bit ADC is

(a) 8	(b) 16	(c) 255	(d) 256
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5. An analog voltage in the range of 0 to 8 V is divided in eight equal intervals for conversion to 3-bit digital output. The maximum quantization error is
 (a) 0 V (b) 0.5 V (c) 1 V (d) 2 V
6. The resolution of a DAC is approximately 0.4% of its full-scale range. It is
 (a) 8-bit converter (b) 10-bit converter
 (c) 12-bit converter (d) 16-bit converter
7. A 12-bit ADC is operating with a 1-microsec clock period and the total conversion time is seen to be 14 microsec. The ADC must be of
 (a) Parallel-comparator type (b) Counting type
 (c) Integrating type (d) Successive-approximation type
8. Dual slope integration type ADC provides
 (a) Higher speed as compared to all other types of ADCs
 (b) Very good accuracy without putting extreme requirement on component stability
 (c) Poor rejections of supply hum
 (d) Better resolution compared to all other types of ADCs for the same number of bits
9. In a 4-bit weighted resistor DAC, the resistor value corresponding to LSB is 32 k Ω . The resistor value corresponding to MSB will be
 (a) 32 K (b) 16 K (c) 8 K (d) 4 K
10. The resolution of a 12-bit DAC using a binary ladder with 10 V as the full-scale output will be
 (a) 2.44 mV (b) 3.50 mV (c) 4.32 mV (d) 5.12 mV
11. A DAC uses a ladder of 10 V full-scale output. The number of bits required of its input for a resolution of 5 mV will be
 (a) 7 (b) 8 (c) 15 (d) 16
12. For successive approximation with N output bits, the number of clocks required is
 (a) $N + 2$ or N (b) $2N + 1$ (c) 2^N (d) $2^N - 1$
13. Which of the following is a D/A conversion technique?
 (a) Successive approximation (b) Weighted resistor
 (c) Dual slope technique (d) Single slope technique

Answers

- | | | | |
|---------|---------|---------|---------|
| 1. (d) | 2. (b) | 3. (d) | 4. (c) |
| 5. (b) | 6. (a) | 7. (d) | 8. (b) |
| 9. (d) | 10. (a) | 11. (d) | 12. (a) |
| 13. (b) | | | |