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ECE 5385: VLSI Design

December 3, 2025

8-Bit Booth Multiplier: Final Project Report

Recall that in this course, Homework 2 involved implementing a four-bit adder utilizing the ripple-carry adder topology and hierachal design from a half-adder and full adder to make the one-bit, two-bit, and then four-bit adder. Homework 3 took the half and full adders and implemented a four-bit multiplier utilizing these adders in a grid-like structure, mimicking the method of multiplication that is typically done by hand and easy to understand. However, this method of multiplication is very slow due to the slow speed of the adder topology chosen as well as the number of additions required to complete this method. As a result, these methods are typically not sufficient for larger bits of binary multiplication. Booth's algorithm employs a method of multiplication that reduces the number of additions required, which significantly speeds up the multiplication process and allows the multiplier to be more suitable for larger numbers. Doing this while implementing a new adder algorithm beyond the ripple-carry adder that reduces the time for the carry bit to propagate improves the overall multiplication process significantly in comparison to previous homework assignments.

This report demonstrates the design and implementation of an eight-bit signed (two's complement) multiplier integrated circuit, utilizing Booth's algorithm in Cadence Virtuoso with VLSI (very large-scale integration) techniques.

Design and Implementation

The design of this multiplier begins with the addition algorithm. One of the largest issues with the ripple-carry adder is that the speed of the propagation of the carry-out bit ($Cout$) is limited by the amount of gate delays required. However, the adder itself in this algorithm generates the sum in a reasonable timeframe. As a result, the carry lookahead adder (CLA) topology was chosen to specifically improve the speed of the carry bit while keeping the same ripple-carry structure to generate the sum bit. In this adder, a Manchester Carry Chain (MCC) was chosen as the method to reduce the timing of the carry propagation to one gate delay by employing propagate, generate, and delete bits that control when a carry-out bit is set or cleared. Note that in the schematic below, the propagate bit is the XOR of A and B (the two eight-bit numbers that will be multiplied together), the generate bit is the NAND of A and B, and the delete bit is the NOR of A and B.

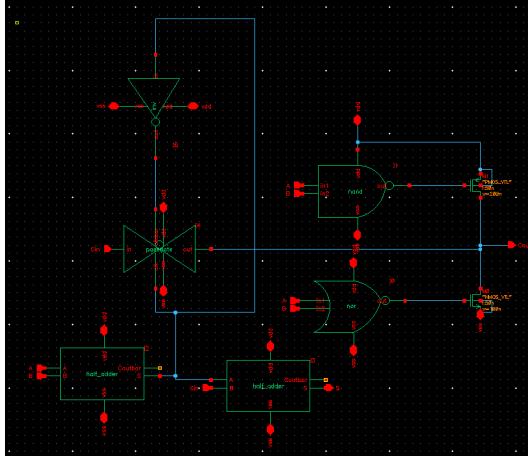


Figure 1: One-Bit CLA with Static MCC Schematic Implementation.

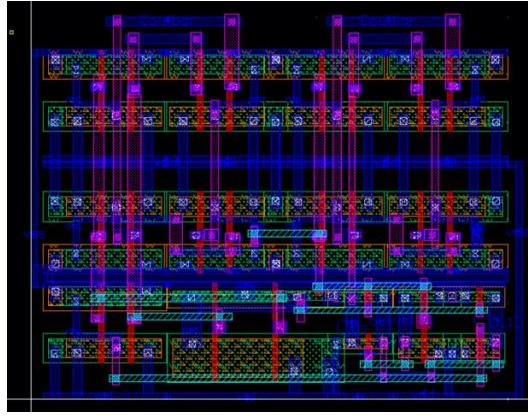


Figure 2: One-Bit CLA with Static MCC Layout Implementation.

Using hierarchical design, the four-bit, twelve-bit, and sixteen-bit adders were designed while accounting for fanout in the final design. This was achieved by buffering the end of the four-bit adder to account for the ideal fanout being four gates or less.

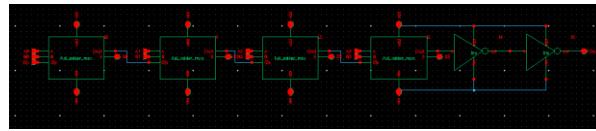


Figure 3: Four-Bit CLA with MCC Schematic Implementation.

While many other addition methods could have been employed for even faster speeds, these are too complex than necessary for eight-bit multiplication (although could be useful in higher-bit multiplications) and require a greater cost in area that is not worth the trade-off for in this eight-bit case.

Then, Booth's algorithm was utilized to form the components that make up the full eight-bit multiplier. Booth's algorithm fundamentally works by systematically using consecutive ones within one of the two multiplied numbers to transform the number into an equivalent form that

requires less additions once partial products are generated. In particular, this uses the radix-4 method within Booth's algorithm, which processes two bits at a time (grouping into base 4, hence, the radix-4 name) while creating overlap to avoid difficult multiplication in binary (by removing the ability to multiply by 3). This method allows the choice of multiplying by -2, -1, 0, 1, or 2, which can all be done simply with shifts in binary rather than a slower addition or inefficient multiplication. In order to modify B so that it can be encoded properly for these multiplication choices, the following table is utilized:

Table 1: Booth Encoding Table					
Bi+1	Bi	Bi-1	Normal Multiplication	Booth Operation	Booth Representation
0	0	0	x0	x0	00
0	0	1	x1	+ x1	01
0	1	0	x2	+ x1	01
0	1	1	x3	+ x2	10
1	0	0	x0	- x2	(~1)0
1	0	1	x1	- x1	0(~1)
1	1	0	x2	- x1	0(~1)
1	1	1	x3	x0	00

This table showcases how B is modified to determine when A is used. For example, the fourth row of this table suggests that the addition of A after being doubled should be performed, while row five suggests that the addition of the two's complement of A should be performed. The result of utilizing this encoding method is shown in the circuit below, where buffers were once again used accordingly to handle fanout issues.

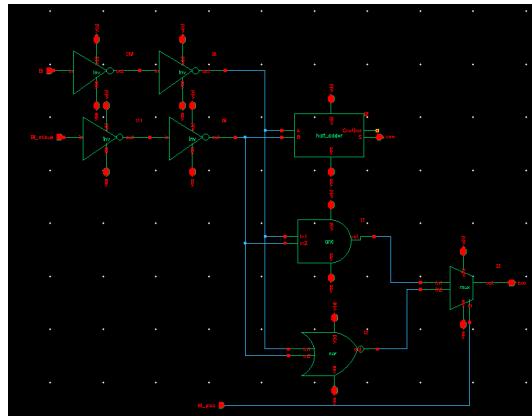


Figure 4: One-Bit Encoder Sub-Circuit Schematic.

This encoder was then used as a sub-circuit in hierachal design to create the full encoder, which allows B to be encoded completely through the one full encoder circuit.

Since the numbers shown in the encoding table are signed (with negative values), Booth's algorithm naturally implements two's complements signed multiplication, and is handled properly in the way that the integrated circuit is developed. While choosing unsigned multiplication simplifies the area and connections within the final design, the signed implementation was performed to mimic the structure of the algorithm as it is designed; the unsigned multiplication implementation requires changes in the decoding and overall design of the Booth algorithm to correct for signed versus unsigned representation. The nature of this comes from the intuition of how the encoding and decoding are derived, as previously mentioned for encoding which will be expanded on below for decoding.

Now that the encoder takes in B and processes the number to decide if A must be doubled, copied once, or negated (where combinations of negation and the one or two are allowed, as shown in Table 1, and where the negation bits are derived from Bi+1 and include the first, third, fifth, and seventh bit of B, respectively), the decoder can use this information to generate the partial products necessary to create the final result. The decoder takes in the one, two, and negative decisions that were determined from the encoder and outputs a partial product (PP) bit that must be added with the remaining partial products to generate the final result (which is 16 bits). The circuit implementation for this is shown in the image below:

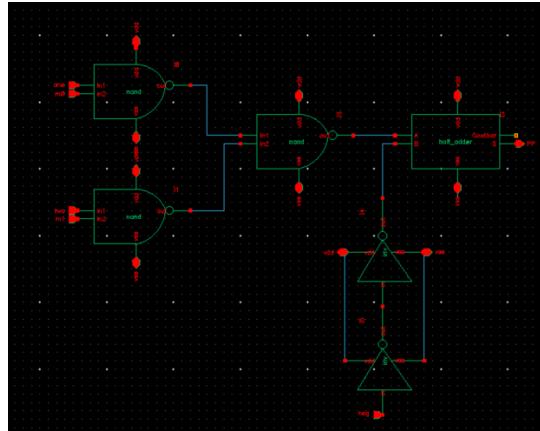


Figure 5: One-Bit Decoder Sub-Circuit Schematic.

This decoder was then copied nine times to create a full decoder circuit so that all eight bits of A can be processed at once (while the m0 bit in the first decoder subcircuit is grounded in the full decoder design). Note that this design handles fanout, but has one case of a fanout of five that is acceptable since it is worth the cost in order to save area (since another buffer being added for one extra fanout in this case costs area space, which is not worth the cost in this case for only one fanout that will not largely hurt the integrity of the final circuit).

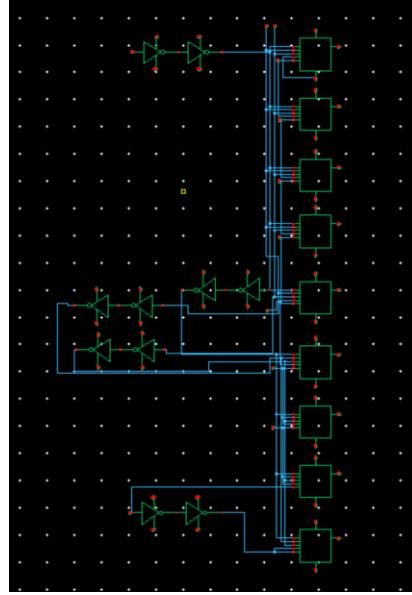


Figure 6: Full Decoder Schematic Implementation.

Now, the final eight-bit booth multiplier can be created. This takes the inputs of B, feeds them into the encoder, and then feeds the inputs of A into four copies of the full decoder, which each have inputs corresponding to one set of the one, two, and neg bits from the encoder (based on the overlapping). Essentially, each encoder subcircuit is fed into one full decoder in this implementation. Then, the addition is performed. For Booth's algorithm in eight bits, typically only 3 additions would be required to add the four eight-bit partial products that are generated by the full decoders. However, to handle signed two's complement additions within the adders for factors such as sign extensions, a fourth adder is needed to handle those negative bits discussed earlier (bits one, three, five, and seven of B). This results in the schematic below and was tested with the values in the table below to ensure accuracy.

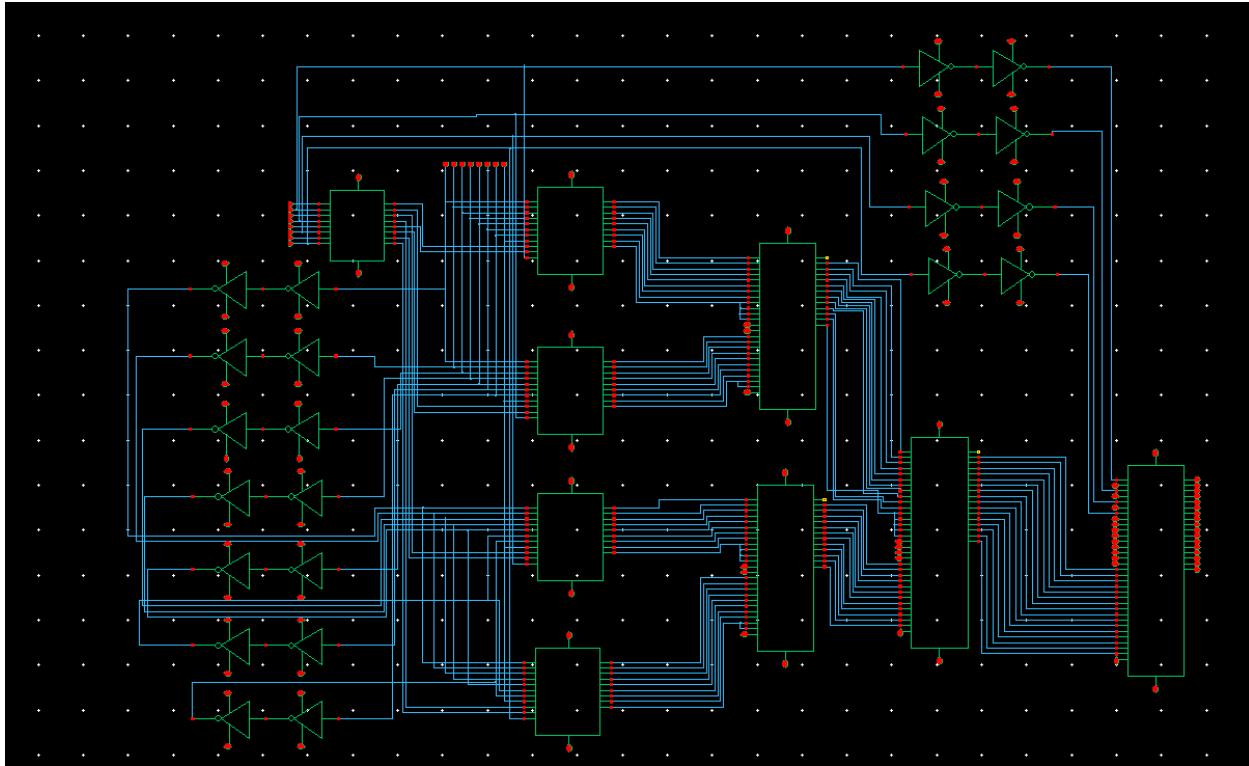


Figure 7: Eight-Bit Booth Multiplier Schematic.

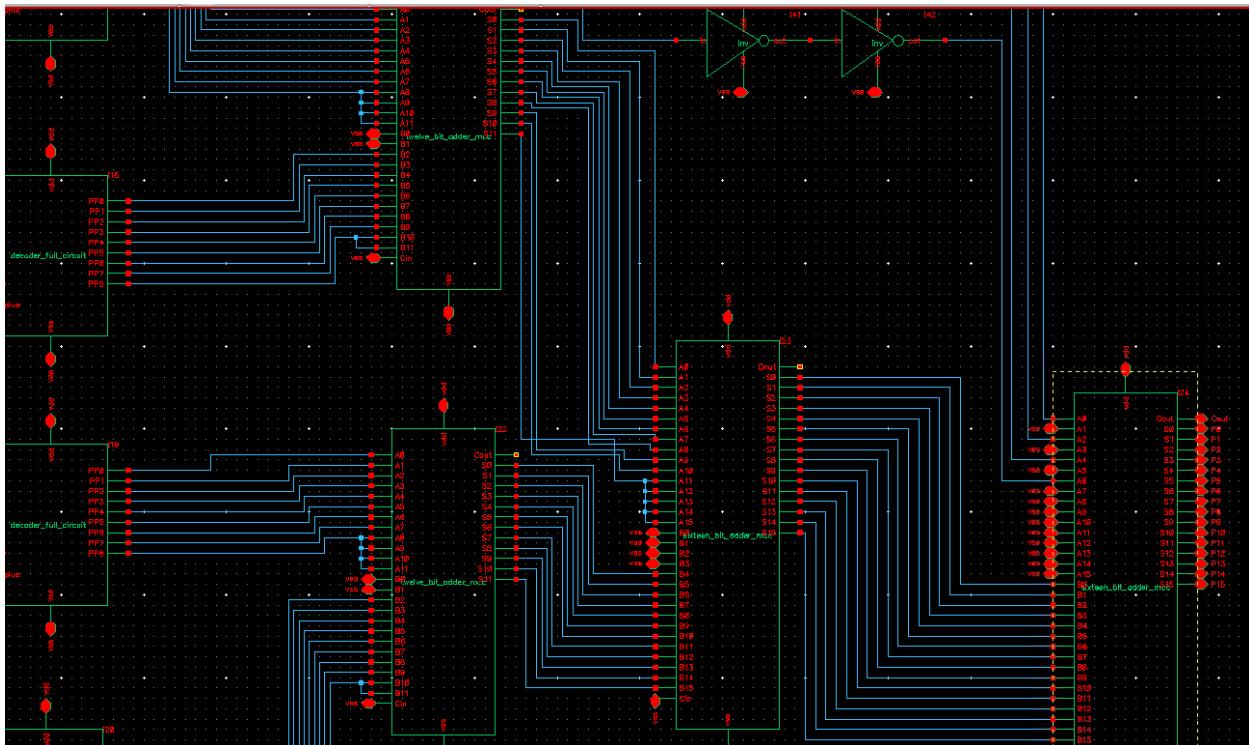


Figure 8: Closer Look at the Signed Addition Connections within the Multiplier Design.

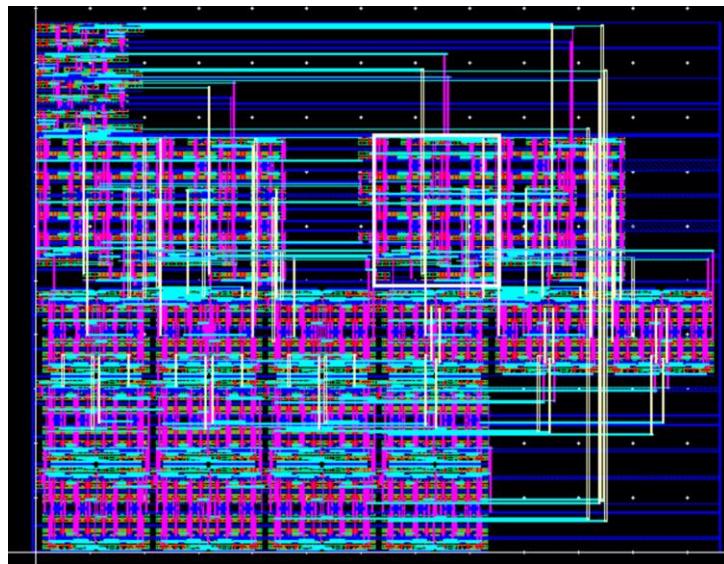
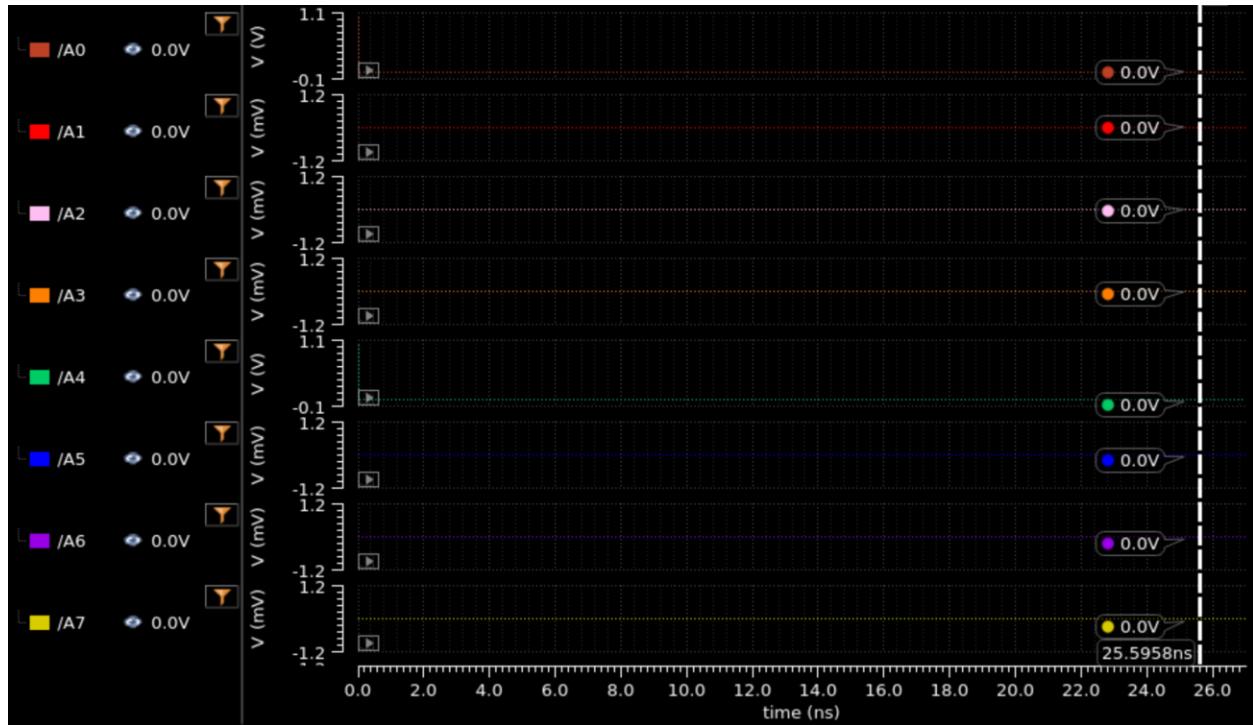


Figure 9: Eight-Bit Booth Multiplier Layout (about 63 by 48 microns).



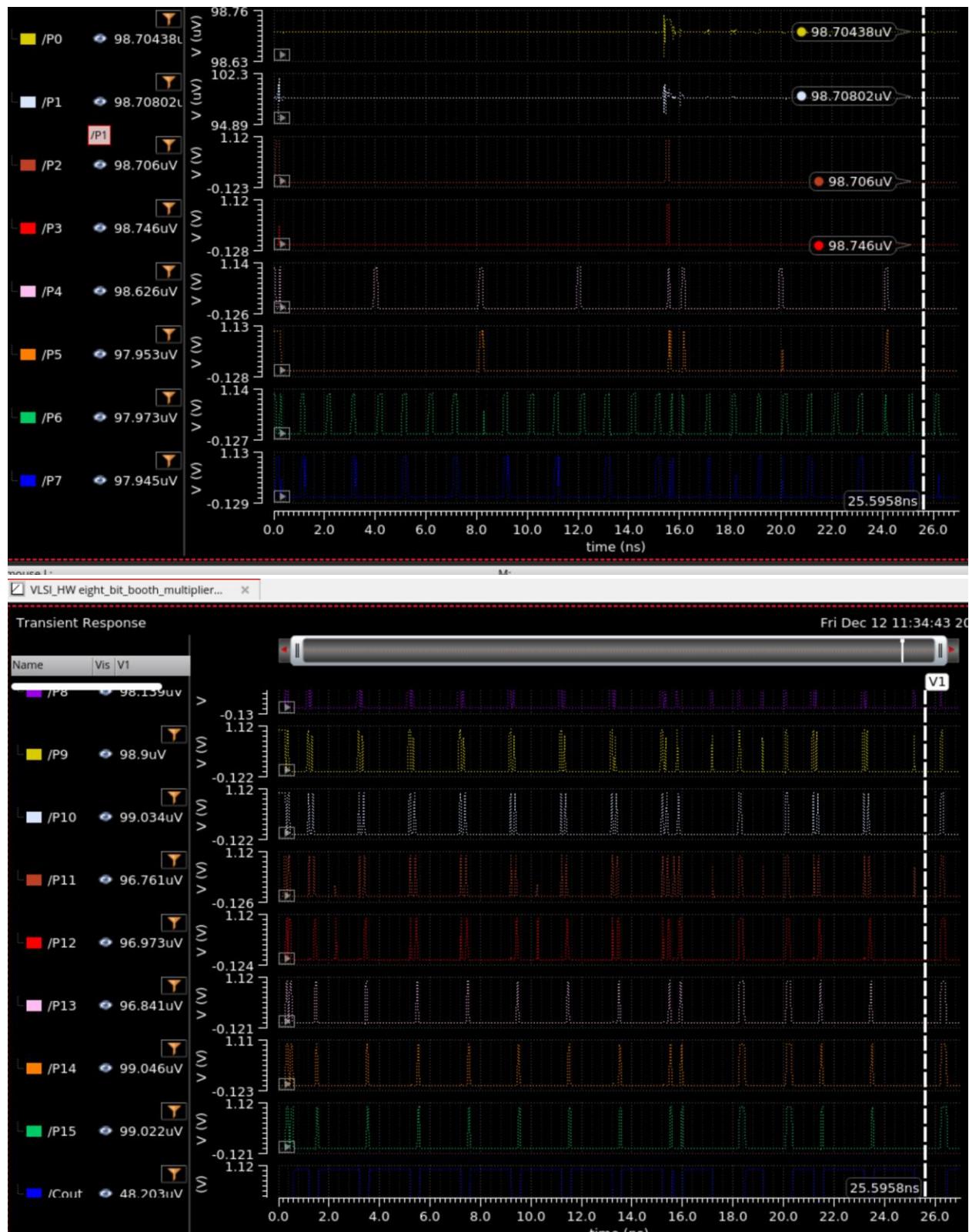
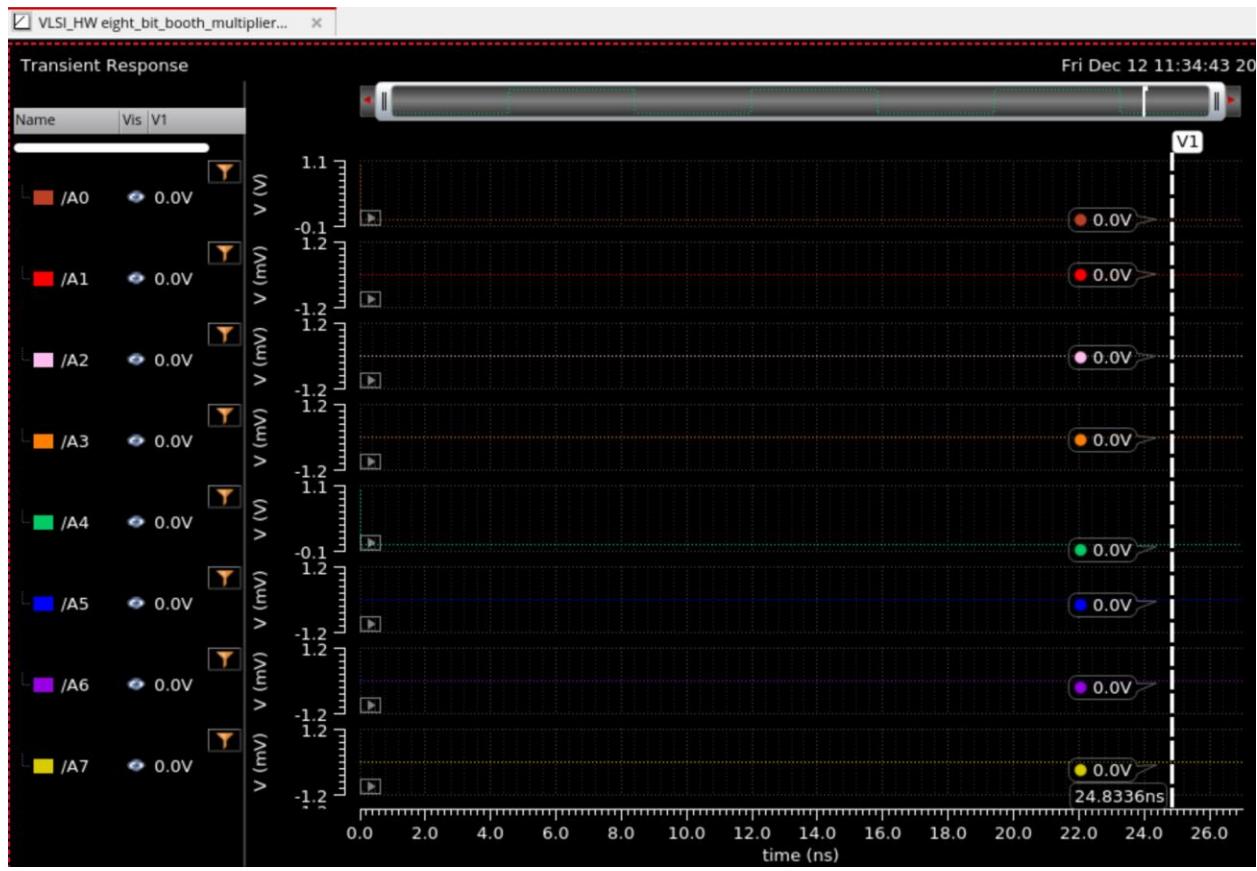


Figure 10: Edge Case 0x0 = 0.



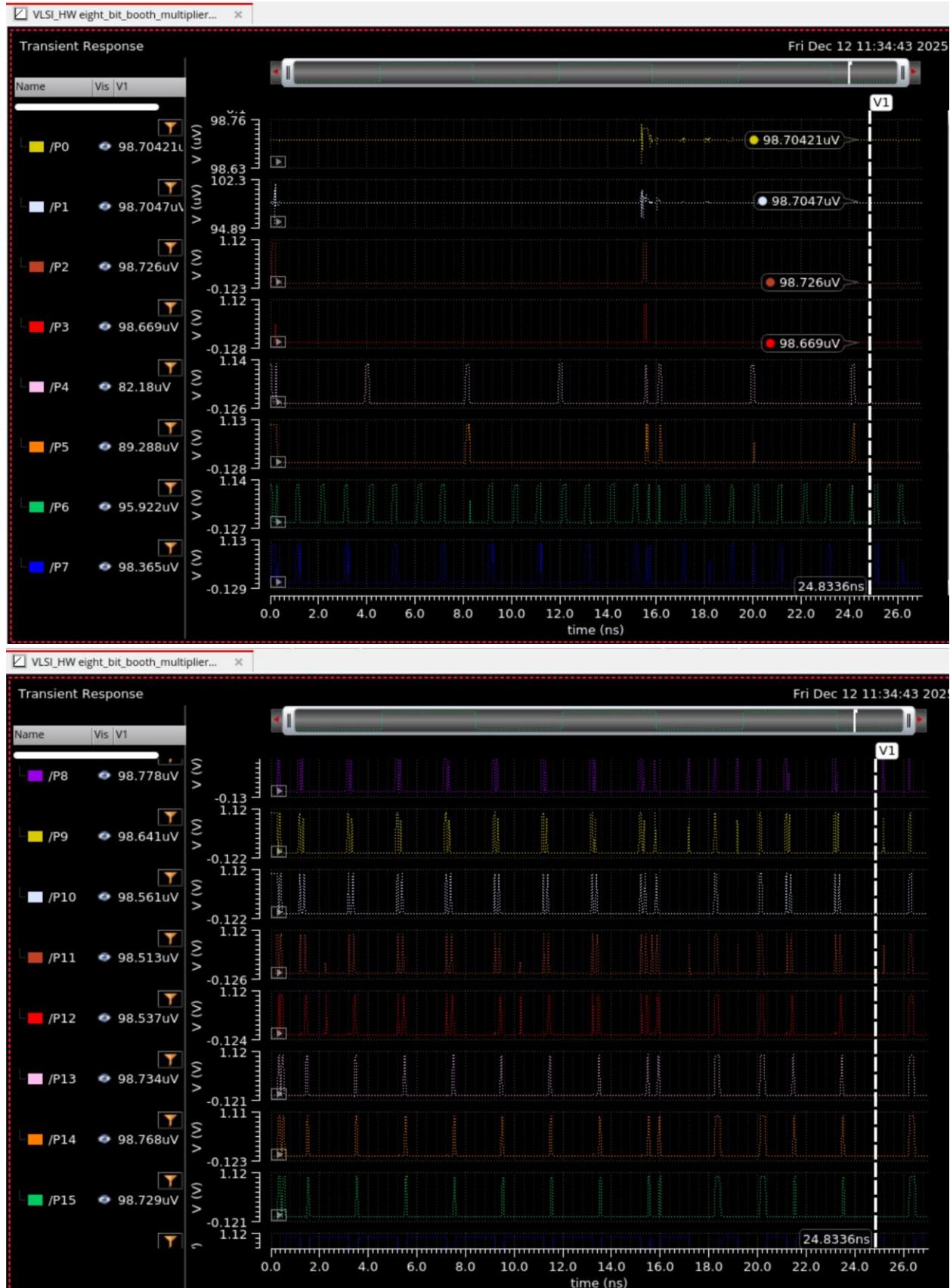


Figure 11: Edge Case 0x1=0.

Testing and Conclusion

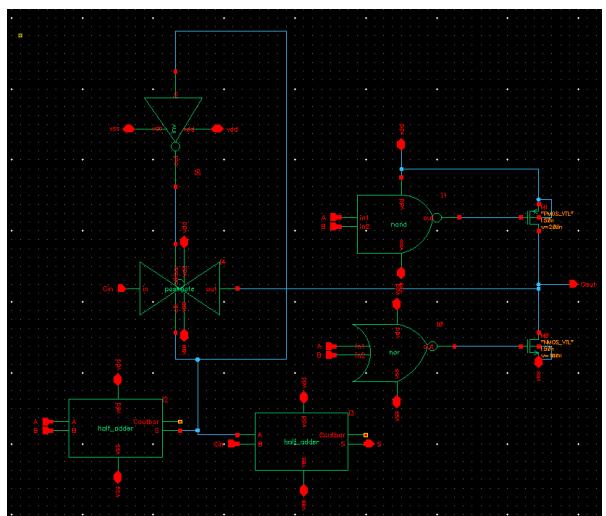
Now, this final IC design is ready to be prepared for fabrication. Once the design is fabricated and given to the user, it must be tested to ensure that design issues or issues within the fabrication process were not made. However, once the IC is fabricated, the internals of the device itself, which many transistors and layers of gates and hierachal design, cannot be tested, as only the I/O (input and output) pins are available. As a result, a function generator or DC power supply can be used on the inputs to add test values into the device (where Vdd is a logic 1 and ground is a logic 0). Then, a voltmeter or oscilloscope can be used on the output pins to measure the values that propagate on the output in order to determine if the chip is working as expected.

In conclusion, by employing various logical changes within the traditional multiplier algorithm used in previous homeworks, an efficient multiplier algorithm can be derived and implemented into an integrated circuit. While there may be tradeoffs to increase speed and efficiency of the multiplication algorithm, in this case, these tradeoffs are worth the significant increase in speed compared to previous algorithms. These design choices are important considerations that designers employ every day in order to create efficient chips and algorithms to utilize in electronic devices today. For future considerations, this Booth algorithm can be modified to pick if A or B should be modified based on how much of a reduction the modification makes. In addition, other adder implementations and versions of Booth's algorithm (such as the choices between radix-2 or radix-8 instead of radix-4) can be chosen as well as a multitude of other changes. While these are interesting future considerations, this design effectively blends a balance of effective considerations of speed, area, reliability, and power to create an efficient design for the purposes of this assignment.

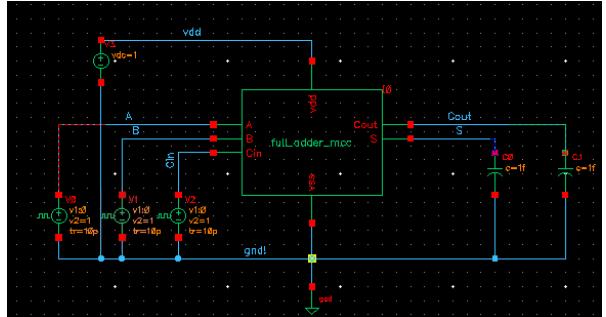
Table 2: 1-Bit Carry Lookahead Adder With Manchester Carry Chain Implementation

Required Snapshot Description	Snapshot
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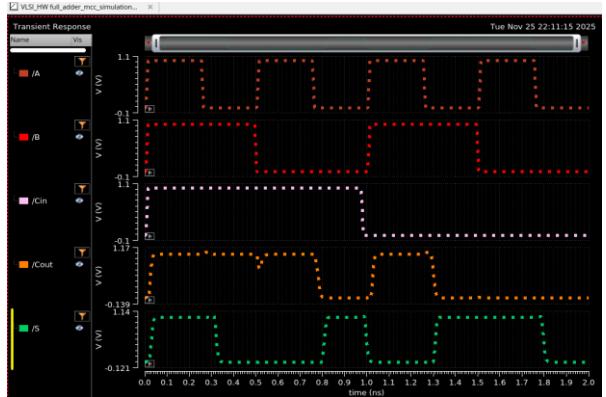
Schematic (Design)



Schematic Simulation Waveform Design



Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/full_adder_mcc_simulation/hspiceD/schema... x
File Edit View Help
cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 211 # elements = 52
# resistors = 0 # capacitors = 2 # inductors = 0
# parallel_lds = 0 # cccs = 0 # vccs = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 4
# curr_srcs = 0 # diodes = 0 # bnts = 0
# jfets = 0 # mosfets = 46 # U elements = 0
# diodes = 0 # pmosfets = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op point 0.00 1 13
transient 0.07 41 909 321 rev= 4
readin 0.02
ercheck 0.02
setup 0.00
output 0.00

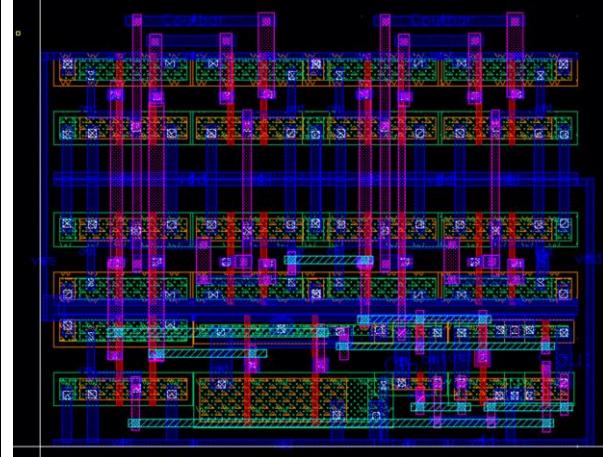
peak memory used 527.81 megabytes
total cpu time 0.11 seconds
total elapsed time 2.71 seconds
job started at 22:11:12 11/25/2025
job ended at 22:11:14 11/25/2025

>info: ***** hspice job concluded
job total runtime 2.71 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.55(s)
```

15 Trace:/Cin/Context:/home/zeruv/simulation/full_adder_mcc_simulation/hs L633 C21

Schematic Layout Design



DRC Transcript

Calibre Interactive - nmDRC v2024.3_25.13 : ./runset.calibre.drc *

```
File Settings Configurations Help TOTAL CPU | 1/1 >
Rules DRC RuleCheck Antenna.metal10 COMPLETED. Number of Results = 0 (0)
Inputs Cumulative ONE-LAYER BOOLEAN Time: CPU = 0 REAL = 0
Outputs Cumulative TWO-LAYER BOOLEAN Time: CPU = 0 REAL = 0
Run Control Cumulative SIZE Time: CPU = 0 REAL = 0
Search Cumulative REGION LOGICAL Time: CPU = 0 REAL = 0
Cumulative EDGED MEASURE Time: CPU = 0 REAL = 0
Cumulative ONE-LAYER DRC Time: CPU = 0 REAL = 0
Cumulative TWO-LAYER DRC Time: CPU = 0 REAL = 0
Cumulative THREE-LAYER DRC Time: CPU = 0 REAL = 0
Cumulative RAYER (RATIO) Time: CPU = 0 REAL = 0
Cumulative REGION (LOGICAL) Time: CPU = 0 REAL = 0
Cumulative MISCELLANEOUS Time: CPU = 0 REAL = 0
Cumulative CONNECT Time: CPU = 0 REAL = 0
Cumulative RDW Time: CPU = 0 REAL = 0
-- CALIBRE-DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
-- TOTAL RULECHECKS EXECUTED = 167
-- TOTAL RESULTS GENERATED = 0 (0)
-- DRC RESULTS DATABASE FILE = full_adder_mcc.drc.results (ASCII)
-- DRC RESULTS REPORT FILE = full_adder_mcc.drc.summary
-- DRC RESULTS LOGFILE = full_adder_mcc.drc.log
*** DRC run finished with exit code 0 ***
INFO: Starting command: $MGIC_HOME/bin/calibre -nowait -rve -drc full_adder_mcc.drc.results
RVE // Calibre v2024.3_25.13 - Thu Aug 1 18:57:13 PDT 2024
0 Errors, 1 Warning, 1 Info
Line | Type | Description
90 Warning Please increase descriptors limit for best performance (1024)
4268 Info Starting command: $MGIC_HOME/bin/calibre -nowait -rve -drc full_adder_mcc.drc.results
```

<h3>DRC Results</h3>	<p>Calibre - RVE v2024.3..25.13 : full_adder_mcc.drc.results</p> <p>File View Highlight Tools Window Setup Help</p> <p>Filter: Show All No Results Found</p> <p>Check / Cell Res</p> <ul style="list-style-type: none"> <input checked="" type="checkbox"/> Check Well 1 0 <input checked="" type="checkbox"/> Check Well 2 0 <input checked="" type="checkbox"/> Check Well 4 0 <input checked="" type="checkbox"/> Check Poly 1 0 <input checked="" type="checkbox"/> Check Poly 2 0 <input checked="" type="checkbox"/> Check Poly 3 0 <input checked="" type="checkbox"/> Check Poly 4 0 <input checked="" type="checkbox"/> Check Poly 5 0 <input checked="" type="checkbox"/> Check Poly 6 0 <input checked="" type="checkbox"/> Check Active 1 0 <input checked="" type="checkbox"/> Check Active 2 0 <input checked="" type="checkbox"/> Check Active 3 0 <input checked="" type="checkbox"/> Check Active 4 0 <input checked="" type="checkbox"/> Check Implant 1 0 <input checked="" type="checkbox"/> Check Implant 2 0 <input checked="" type="checkbox"/> Check Implant 3 0 <input checked="" type="checkbox"/> Check Implant 4 0 <input checked="" type="checkbox"/> Check Implant 5 0 <input checked="" type="checkbox"/> Check Contact 1 0 <input checked="" type="checkbox"/> Check Contact 2 0 <p>Rule File Pathname: <code>calibreRVE.rvl</code></p> <p>Well and Well must not overlap</p> <p>Calibre Run Completed Successfully -- Results are Valid</p> <p>Check Well 1</p>																														
<h3>LVS Transcript</h3>	<p>Calibre Interactive - nmLVS v2024.3..25.13 : ./runset.calibre.lvs *</p> <p>File Settings Configurations Help TOTAL CPU 2/2</p> <p>Rules Inputs H-Cells Outputs Options ERC Signatures Run Control Search Transcript Files</p> <p>Run LVS Start RVE</p> <p>0 Errors, 1 Warning, 2 Infos Filter</p> <pre> 1643 LVS completed. CORRECT. See report file: full_adder_mcc.lvs.report 1644 LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 67/69/69 MALLOC = 89/89/89 ELAPSED 1645 1646 -- LVS REPORT FILE = full_adder_mcc.lvs.report 1647 -- CALIBRE::LVS COMPARISON MODULE COMPLETED. TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP 1648 1649 -- CALIBRE::LVS/xRC COMPLETED - Fri Nov 28 20:30:27 2025 1650 -- XDB CROSS REFERENCE DATABASE = svdbfull_adder_mcc.xdb 1651 1652 -- SPICE NETLIST FILE = full adder mcc.sp 1653 -- CIRCUIT EXTRACTION REPORT FILE = full_adder_mcc.lvs.report.ext 1654 -- PERSISTENT HIERARCHICAL DATABASE(PHDB) = svdbfull_adder_mcc.phdb 1655 -- QUERY DATABASE = svdb: TOP CELL = full_adder_mcc 1656 -- GRAND TOTAL NON-HYPER/LVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP = 69 MALLOC 1657 1658 *** LVS run finished with exit code 0 *** 1659 1660 INFO: Starting command: \$MGC_HOME/bin/calibre -nowait -rve -lvs svdb full_adder_mcc 1661 1662 1663 PVE: // Calibre (v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024 1664 PVE: // Calibre Utility Library v0-10-13-2017-1 Fri Apr 12 08:04:27 PDT 2024 1665 PVE: // Litho Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024 1666 PVE: // 1667 PVE: // Copyright Siemens 1996-2024 1668 PVE: // All Rights Reserved. 1669 PVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION 1670 PVE: // WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION </pre>																														
<h3>LVS Comparison Results</h3>	<p>Calibre - RVE v2024.3..25.13 : svdb full_adder_mcc</p> <p>File View Highlight Tools Window Setup Help</p> <p>Navigator</p> <p>Results Extraction Results Comparison Results</p> <p>Reports Extraction Report LVS Report</p> <p>Rules Rules File</p> <p>View Info Finder Schematics</p> <p>Setup Options</p> <p>Comparison Results</p> <table border="1"> <thead> <tr> <th>Layout Cell / Type</th> <th>Source Cell</th> <th>Nets</th> <th>Instances</th> <th>Ports</th> </tr> </thead> <tbody> <tr> <td>full_adder_mcc</td> <td>full_adder_mcc</td> <td>171, 178</td> <td>151, 158</td> <td>71, 78</td> </tr> </tbody> </table> <p>Cell full_adder_mcc Summary (Clean)</p> <p>CELL COMPARISON RESULTS (TOP LEVEL)</p> <p>LAYOUT CELL NAME: full_adder_mcc SOURCE CELL NAME: full_adder_mcc</p> <p>INITIAL NUMBERS OF OBJECTS</p> <table border="1"> <thead> <tr> <th></th> <th>Layout</th> <th>Source</th> <th>Component Type</th> </tr> </thead> <tbody> <tr> <td>Ports:</td> <td>27</td> <td>27</td> <td></td> </tr> <tr> <td>Netels:</td> <td>23</td> <td>23</td> <td>NET (4 global)</td> </tr> <tr> <td>Instances:</td> <td>23</td> <td>23</td> <td>NET (4 global)</td> </tr> <tr> <td>Total Insts:</td> <td>46</td> <td>46</td> <td></td> </tr> </tbody> </table> <p>NUMBERS OF OBJECTS AFTER TRANSPARENCIES</p>	Layout Cell / Type	Source Cell	Nets	Instances	Ports	full_adder_mcc	full_adder_mcc	171, 178	151, 158	71, 78		Layout	Source	Component Type	Ports:	27	27		Netels:	23	23	NET (4 global)	Instances:	23	23	NET (4 global)	Total Insts:	46	46	
Layout Cell / Type	Source Cell	Nets	Instances	Ports																											
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Ports:	27	27																													
Netels:	23	23	NET (4 global)																												
Instances:	23	23	NET (4 global)																												
Total Insts:	46	46																													

PEX Transcript

Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *

File Settings Configurations Help Search

Rules
Inputs
Outputs
LVS
Run Control
Search
Transcript
Files

Run PEX
Start RVE

```

2250 ---- PDB NET SUMMARY ----
2251 pdb file name = svdb/FULL_ADDER_MCC.pdb
2252 root cell name = FULL_ADDER_MCC
2253 total nets = 27
2254 top-level nets = 17
2255 non-top-level nets = 0
2256 degenerate nets = 0
2257 merged nets = 0
2258 error nets = 0
2259
2260 =====
2261 CALIBRE XRC WARNING / ERROR Summary
2262 =====
2263 xRC Warnings = 3
2264 xRC Errors = 0
2265 =====
2266 --- CALIBRE xRC:FORMATTER COMPLETED - Fri Nov 28 21:01:44 2025
2267 --- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 1576/299 MALLOC = 261/261/2
2268 *** xRC run finished with exit code 0 ***
2269
2270
2271 0 Errors, 10 Warnings, 1 Info
2272 Line Type Description
2273 6 Info Verifying the source netlist is complete before starting th...
2274 7 Warning Please increase database limit for back annotation

```

PEX Netlist Output

Calibre Interactive - PEX v2024.3..25.13 : ./runset.bre.pex *

File Settings Configurations Help Search

Rules
Inputs
Outputs
LVS
Run Control
Search
Transcript
Files

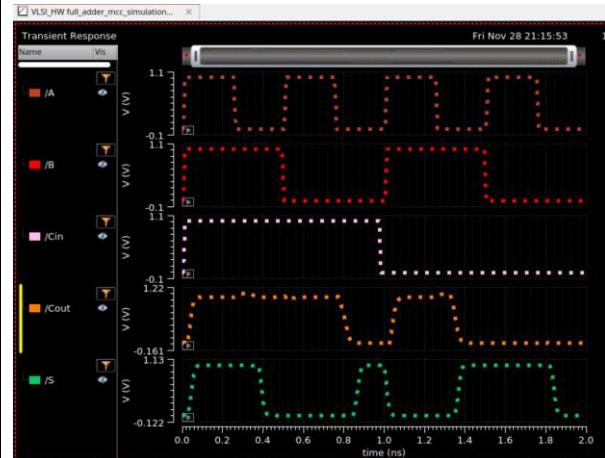
Run PEX
Start RVE

```

1 * File: full_adder_mcc.pex.netlist
2 * Created: Fri Nov 28 21:01:44 2025
3 * Program "Calibre xrc"
4 * Version "v2024.3_25.13"
5 *
6 .include "full_adder_mcc.pex.netlist.pex"
7 .subckt full_adder_mcc A B CIN COUT S VSS VDD
8 *
9 * VDD VDD
10 * VSS VSS
11 * S S
12 * COUT COUT
13 * CIN CIN
14 * B B
15 * A A
16 mx10/MM2 N_NET4_X10/MM2_d N_B_X10/MM2_g N_VSS_X10/MM2_s
N_VSS_X10/MM2_b NMOS_VTL
17 + L=5e-08 W=1e-07 AD=4.15e-14 AS=5.825e-14 PD=1.03e-06
PS=1.365e-06
18 mx10/MM3 N_NET4_X10/MM3_d N_A_X10/MM3_g N_VSS_X10/MM2_s
N_VSS_X10/MM2_b NMOS_VTL
19 + L=5e-08 W=1e-07 AD=3.35e-14 AS=5.825e-14 PD=8.7e-07
PS=1.365e-06
20 mx14/MM0 N_CIN_X14/MM0_d N_NET3_X14/MM0_g N_COUT_X14/
MM0_s N_VSS_X10/MM2_b
21 + NMOS_VTL L=5e-08 W=1e-07 AD=2.3e-14 AS=1.75e-14
PD=6.6e-07 PS=5.5e-07
22 mx16/MM1 N_NET6_X16/MM1_d N_NET3_X16/MM1_g N_VSS_X16/
MM1_s N_VSS_X10/MM2_b

```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```

/home/zeruv/simulation/full_adder_mcc_simulation/hspiceD/schema... x
cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 755 # elements = 1877
# resistors = 55 # capacitors = 1270 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vccs = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 4
# curr_srcs = 0 # diodes = 0 # bjt = 0
# jfets = 0 # p-nostots = 46 # Uelements = 0
# Telements = 0 # N elements = 0 # elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis      time   # points tot. iter conv.riter
op point     0.04          1       232
transient    0.17         41       767     280 rev=1
read        0.02
errchk      0.01
setup       0.01
output      0.00

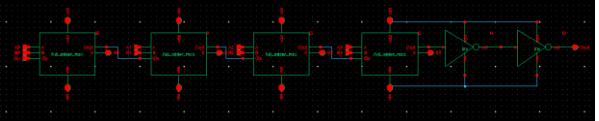
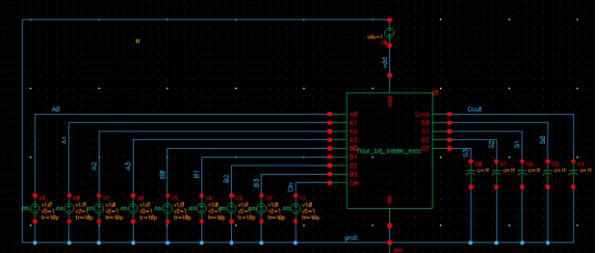
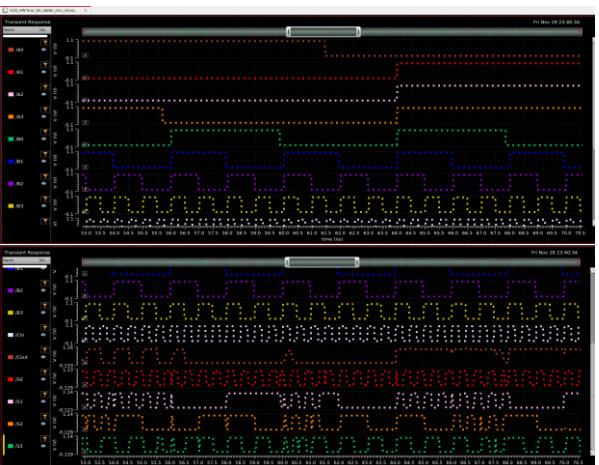
peak memory used      530.08 megabytes
total cpu time        0.25 seconds
total elapsed time    2.56 seconds
job started at        21:15:50 11/28/2025
job ended at          21:15:53 11/28/2025

>info: ***** hspice job concluded
      job total runtime 2.56 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.30(s)

```

Table 3: 4-Bit Carry Lookahead Adder With Manchester Carry Chain Implementation

Required Snapshot Description	Snapshot
Schematic (Design)	
Schematic Simulation Waveform Design	
Schematic Simulation Waveform Results	

Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/four_bit_adder_mcc_simulation/hspiceD/sc... x
File Edit View Help
cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 835 # elements = 199
# resistors = 0 # capacitors = 5 # inductors = 0
# mosfets = 0 # vols = 0 # volt_srcs = 0
# cccs = 0 # ccvs = 0 # curr_srcs = 10
# curr_srcs = 0 # diodes = 0 # btrs = 0
# jfets = 0 # mosfets = 184 # U elements = 0
# triodes = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # VA device = 0
# vector_srcs = 0 # N elements = 0

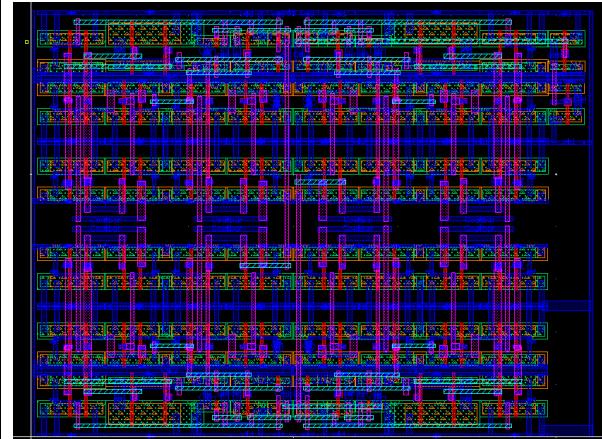
***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op point 0.01 1 13
transient 10.94 257 66306 23294 rev= 297
readin 0.01
erchk 0.03
setup 0.00
output 0.00

peak memory used 527.81 megabytes
total cpu time 11.00 seconds
total elapsed time 13.44 seconds
job started at 18:42:42 11/28/2025
job ended at 18:42:55 11/28/2025

>info: ***** hspice job concluded
      job total runtime 13.44 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.40(s)
```

Schematic Layout Design



DRC Transcript

```
Calibre Interactive - nmDRC v2024.3_25.13 : ./runset.calibre.drc *
File Settings Configurations Help
TOTAL CPU 1/1 < >
Rules 4257
4258 --- CALIBRE-DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
4259 --- TOTAL RULECHECKS EXECUTED = 167
4260 --- TOTAL RESULTS GENERATED = 0 (0)
4261 --- DRC RESULTS DATABASE FILE = four_bit_adder_mcc.drc.results (ASCII)
4262
4263 --- CALIBRE-DRC-H COMPLETED - Sat Nov 29 01:25:35 2025
4264 --- CPU TIME = 0 REAL TIME = 2
4265 --- PROCESSOR COUNT = 1
4266 --- SUMMARY REPORT FILE = four_bit_adder_mcc.drc.summary
4267
4268
4269 *** DRC run finished with exit code 0 ***
4270
4271 INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -drc four_bit_adder_mcc.drc.results
4272
4273 RVE: // Calibre v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
4274 RVE: // Calibre Utility Library v0-10-13-2017-1 Fri Apr 12 08:04:27 PDT 2024
4275 RVE: // Litho Libraries v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
4276 RVE: //
4277 RVE: // Copyright Siemens 1996-2024
4278 RVE: // All Rights Reserved.
4279 RVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
4280 RVE: // WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
4281 RVE: // OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
4282 RVE: //
4283 RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI,
4284 RVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
4285 RVE: // Linux is a registered trademark of Linus Torvalds.
4286 RVE: // Mentor Graphics software executing under x86-64 Linux
```

<h3>DRC Results</h3>	<p>LVS Transcript</p>
<h3>LVS Comparison Results</h3>	

PEX Transcript

```
Calibre Interactive - PEX v2024.3.25.13 : ./runset.calibre.pex *
File Settings Configurations Help
Rules Inputs Outputs LVS Run Control Search Transcript Files
ptb file name = svdb/FOUR_BIT_ADDER.MCC.pdb
root file name = FOUR_BIT_ADDER.MCC
total nets = 61
top-level nets = 61
non-top-level nets = 0
designed nets = 40
merged nets = 0
error nets = 0

=====
FOB NET SUMMARY
=====
root file name = svdb/FOUR_BIT_ADDER.MCC.pdb
root file name = FOUR_BIT_ADDER.MCC
total nets = 61
top-level nets = 61
non-top-level nets = 0
designed nets = 40
merged nets = 0
error nets = 0

=====
CALIBRE xRC WARNING / ERROR Summary
=====
xRC Warnings = 3
xRC Errors = 0
=====
=====
-- CALIBRE xRC:FORMATTER COMPLETED - Sun Nov 30 03:30:19 2025
-- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 1576/299 MALLOC = 267/267/267 ELAPSED TIME = 2
*** xRC run finished with exit code 0 ***
2347
0 Errors, 10 Warnings, 1 Info
Line Type Description
10 Info Verifying the source netlist is complete before starting the run
97 Warning Please increase descriptors limit for best performance (1024)
128 Warning PEX RESISTANCE LUMPED is obsolete. Please remove from your ruledeck.
256 Warning PEX RESISTANCE LUMPED is obsolete. Please remove from your ruledeck.
1843 Warning Please increase descriptors limit for best performance (1024)
```

PEX Netlist Output

```
Calibre Interactive - PEX v2024.3.25.13 : ./runset.calibre.pex *
File Settings Configurations Help
Rules Inputs Outputs LVS Run Control Search Transcript Files
four_bit_adder_micc.pex.netlist *
1 * file: four_bit_adder_micc.pex.netlist
* Created: Sun Nov 30 03:30:19 2025
* Program: Calibre PEX
* Version: "v2024.3.25.13"
* include "four_bit_adder_micc.pex.netlist"
* subckt four_bit_adder_micc VSS A1 A0 B1 B0 C1 S1 VDD S2 S3 B2 B3 A2 A3 COUT
*
* COUT COUT
* A3 A3
* A2 A2
* B3 B3
* B2 B2
* S3 S3
* S2 S2
* VDD VDD
* S0 S0
* S1 S1
* CIN CIN
* B0 B0
* B1 B1
* A0 A0
* A1 A1
* VSS VSS
mx55M1 N_COUT_XINMM1_2 N_NETS_XINMM1_2 N_VSS_XINMM1_2 N_VSS_XINMM1_1b
+ PMOS_VTL_L=5e-08 W=1e-07 AD=4.9e-14 AS=-3.7e-14 PD=4e-07 PS=7.7e-07
mx55M2 N_COUT_XINMM2_2 N_NETS_XINMM2_2 N_VDD_XINMM2_2 N_VDD_XINMM2_b
+ PMOS_VTL_L=5e-08 W=1e-07 AD=4.9e-14 AS=-3.7e-14 PD=4e-07 PS=7.7e-07
mx54M1 N_CIN_XINMM1_2 N_NETS_XINMM1_2 N_VDD_XINMM1_2 N_VDD_XINMM1_b
+ NMOS_VTL_L=5e-08 W=1e-07 AD=4.5e-14 AS=-1.8e-14 PD=6e-07 PS=7.7e-07
mx54M2 N_CIN_XINMM2_2 N_NETS_XINMM2_2 N_VDD_XINMM2_2 N_VDD_XINMM2_b
+ NMOS_VTL_L=5e-08 W=1e-07 AD=4.5e-14 AS=-1.8e-14 PD=6e-07 PS=7.7e-07
mx11/XINMM1_X11NET1_X11/XINMM1 d N_A1_X11/XINMM1 g N_B1_X11/XINMM1 s
+ N_VSS_X11/XINMM1 b NMOS_VTL_L=5e-08 W=1e-07 AD=4.15e-14 AS=4.825e-14
+ PS=5e-07
mx11/XINMM1_X11NET2_X11/XINMM1 d N_A1_X11/XINMM1 g N_VSS_X11/XINMM1 s
+ N_VSS_X11/XINMM1 b NMOS_VTL_L=5e-08 W=1e-07 AD=4.15e-14 AS=4.825e-14
+ PS=5e-07
mx11/XINMM1_X11NET3_X11/XINMM1 d N_A1_X11/XINMM1 g N_VSS_X11/XINMM1 s
+ N_VSS_X11/XINMM1 b NMOS_VTL_L=5e-08 W=1e-07 AD=4.15e-14 AS=4.825e-14
+ PS=5e-07
mx11/XINMM1_X11NET4_X11/XINMM1 d N_A1_X11/XINMM1 g N_VSS_X11/XINMM1 s
+ N_VSS_X11/XINMM1 b NMOS_VTL_L=5e-08 W=1e-07 AD=4.15e-14 AS=4.825e-14
+ PS=5e-07
mx11/XINMM1_X11NET5_X11/XINMM1 d N_A1_X11/XINMM1 g N_VSS_X11/XINMM1 s
+ N_VSS_X11/XINMM1 b NMOS_VTL_L=5e-08 W=1e-07 AD=4.15e-14 AS=4.825e-14
+ PS=5e-07
Run finished
```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```

/home/zeruv/simulation/four_bit_adder_mcc_simulation/hspiceD/schematic/psf/hspice.out
***** PrimeSim HSPICE Threads Information *****
System loadavg : 0.88 0.46 0.49 1/611 246471
File Edit View Help
cadence
***** Circuit Statistics *****
# nodes      = 3015 # elements      = 7599
# resistors = 2244 # capacitors   = 516 # inductors = 0
# metal_nds = 0 # cccvs        = 0 # vccs       = 0
# cccs       = 0 # ccvs         = 0 # volt_srcs  = 10
# curr_srcs = 0 # diodes        = 0 # bjts       = 0
# jfets      = 0 # mosfets       = 184 # U elements = 0
# T elements= 0 # T elements    = 0 # U elements = 0
# S elements= 0 # P elements    = 0 # VU device   = 0
# vector_srcs = 0 # N elements   = 0

***** Runtime Statistics (seconds) *****
analysis      time # points tot. iter conv.riter
op point     0.13      1      139
transient    43.14    257    54195    19411 rev= 991
readin       0.06
errchk       0.04
setup        0.05
output       0.00

peak memory used      550.23 megabytes
total cpu time        43.42 seconds
total elapsed time    45.36 seconds
job started at        01:44:02 11/29/2025
job ended at          01:44:48 11/29/2025

>info: ***** hspice job concluded
      job total runtime 45.36 seconds

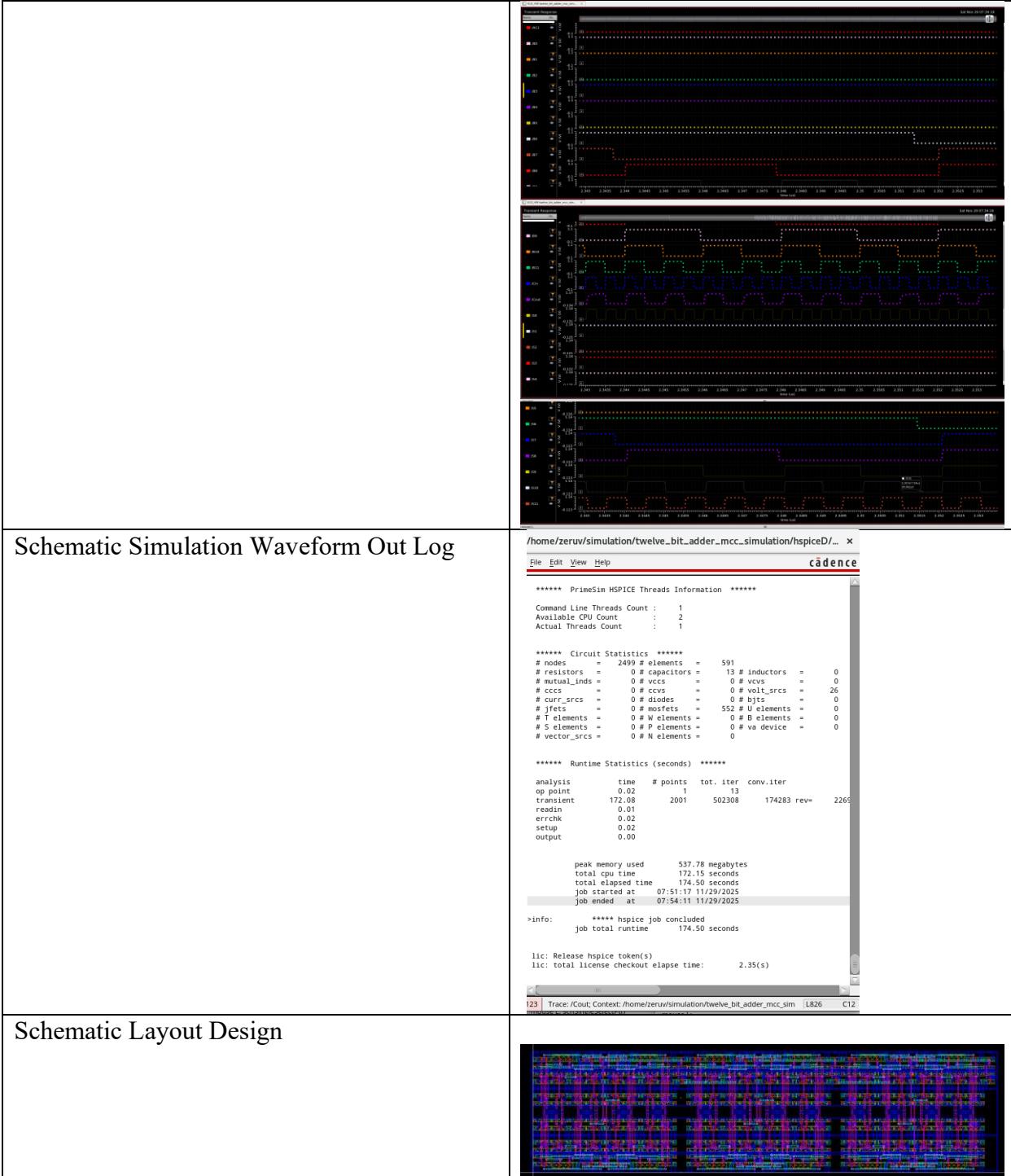
lic: Release hspice token(s)
lic: total license checkout elapse time: 1.94(s)

103 | Trace: /S3: Context:/home/zeruv/simulation/four_bit_adder_mcc_simulation/hspiceD/schematic/psf; Dataset: timeSweep L845 C1

```

Table 4: 12-Bit Carry Lookahead Adder With Manchester Carry Chain Implementation

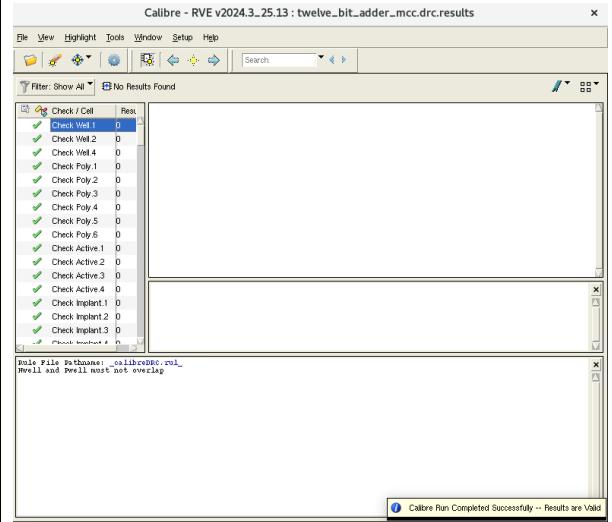
Required Snapshot Description	Snapshot
Schematic (Design)	
Schematic Simulation Waveform Design	
Schematic Simulation Waveform Results	



DRC Transcript

```
Calibre Interactive - nmDRC v2024.3..25.13 : ./runset.calibre.drc *
File Settings Configurations Help TOTAL CPU T 1/1 4/8
Rules DRC Rule-Check Antenna.metal0 COMPLETED: Number of Results = 0 (0)
Inputs Cumulative ONE-LAYER BOOLEAN Time: CPU = 0 REAL = 0
Outputs Cumulative TWO-LAYER BOOLEAN Time: CPU = 0 REAL = 0
Run Control Cumulative EDGE TOPOLOGICAL Time: CPU = 0 REAL = 0
Search Cumulative EDGE MEASUREMENT Time: CPU = 0 REAL = 0
Transcript Cumulative CELL CYCLICITY Time: CPU = 0 REAL = 0
Files Cumulative TWO-LAYER DRC Time: CPU = 0 REAL = 0
-- CALIBRE: DRC-CH EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
-- CALIBRE: DRC-CH REPORT FILE = twelve_bit_adder.mcc.drc.results
4296 -- DRC RESULTS GENERATED
-- DRC RESULTS DATABASE FILE = twelve_bit_adder.mcc.drc.results (ASCII)
-- CALIBRE: DRC-CH COMPLETED - Sat Nov 29 04:26:41 2024
-- TOTAL CPU TIME = 0 REAL TIME = 2
-- PREVIOUS RUN TIME = 18:57:13 PDT 2024
-- SUMMARY REPORT FILE = twelve_bit_adder_mcc.drc.summary
*** DRC run finished with exit code 0 ***
INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -drc twelve_bit_adder_mcc.drc.results
RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Lhs Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Copyright Siemens 1996-2024
RVE: // Compliant Siemens 1996-2024
0 Errors, 1 Warning, 1 Info Line Type Description
90 Warning Please increase descriptors limit for best performance (1024)
4272 Info Starting command: $MGC_HOME/bin/calibre -nowait -rve -drc twelve_bit_adder_mcc.drc.results
```

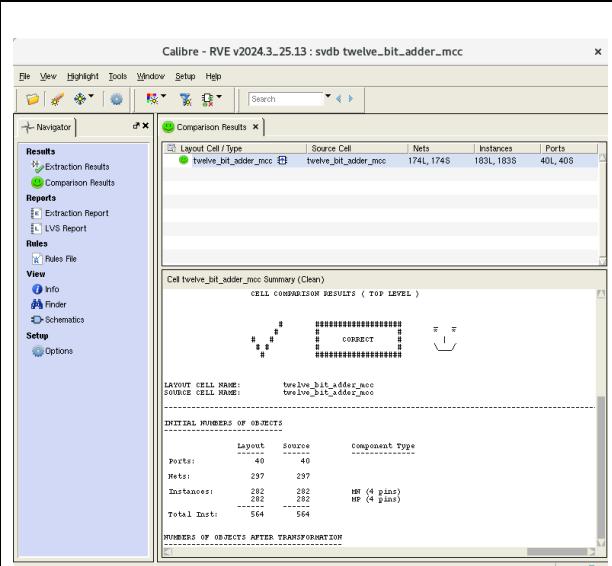
DRC Results



LVS Transcript

```
Calibre Interactive - nmLVS v2024.3..25.13 : ./runset.calibre.lvs *
File Settings Configuration Help TOTAL CPU T 2/2 4/8
Rules LVS completed: CORRECT. See report file: twelve_bit_adder_mcc.lvs.report
Inputs LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 67/71/71 MALLOC = 92/92/92 ELAPSED TIME = 3
H-Cells
Outputs
Signatures
Run Control
Search
Transcript
1781 -- LVS: LVS COMPARISON MODULE COMPLETED. [TOTAL CPU] TIME = 0 REAL TIME = 0 LVHEAP = 2/7/71 MALLOC = 92/92/92 ELAPSED TIME = 3
Files -- XDB CROSS REFERENCE DATABASE = svb/twelve_bit_adder_mcc.xdb
-- SPICE NETLIST FILE = twelve_bit_adder_mcc.sp
-- CIRCUIT DESCRIPTION REPORT FILE = twelve_bit_adder_mcc.lvs.report
-- PERSISTENT MEMORY REPORT FILE = svb/twelve_bit_adder_mcc.phb
-- QUERY DATABASE = svb/twelve_bit_adder_mcc.qdb
-- GRAND TOTAL NON-HYPHEN LVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP = 71 MALLOC = 100
*** LVS run finished with exit code 0 ***
INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -lvs svb/twelve_bit_adder
RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Lhs Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Copyright Siemens 1996-2024
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RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI, the
RVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
RVE: // Mentor Graphics software executing under x86-64 Linux
RVE: //
RVE: // Running on 1 CPU
RVE: // Memory: 16GB
RVE: // Graphical User-Interface startup... Complete.
RVE: // Calibration license acquired.
RVE: // Calibration license acquired.
RVE: // RVE authorized.
0 Errors, 1 Warning, 2 Infos Line Type Description
9 Info Verifying the source netlist is complete before starting the run
4272 Info Mmcx:source:decoupling:link for fast measurement (1024)
```

LVS Comparison Results



PEX Transcript

```

Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
-- NETWORK REDUCTION BEGIN:
-- READING FROM PDB...
-- BEGIN REDUCING NETS...
-- XRC: Using cell name defined in PEX NETLIST statement and "0" will be used in the netlist.
-- DONE REDUCING NETS...
-- WRITING TO PDB...
-- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 256/299/299 MALLOC = 280/280/280
-- PDB NET SUMMARY --
pds file name = svdb/TWELVE_BIT_ADDER_MCC.pdb
net cell name = TWELVE_BIT_ADDER_MCC
total nets = 297
top-level nets = 177
non-top-level nets = 0
degenerate nets = 120
merged nets = 0
error nets = 0

----- CALIBRE XRC WARNING / ERROR Summary -----
xRC Warnings = 3
xRC Errors = 0
----- CALIBRE PEX FORMATTER COMPLETED - Sun Nov 30 04:41:56 2025 -----
-- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 267/299 MALLOC = 292/292/292 ELAPSED TIME = 3
*** xRC run finished with exit code 0 ***
2436
0 Errors, 10 Warnings, 1 Info
Line Type Description
10 Info Verifying the source netlist is complete before starting the run
97 Warning Please increase descriptors limit for best performance (1024)
128 Warning PEX RESISTANCE LUMPED is obsolete. Please remove from your ruledeck.
256 Warning PEX RESISTANCE LUMPED is obsolete. Please remove from your ruledeck.
1927 Warning Please increase descriptors limit for best performance (1024)

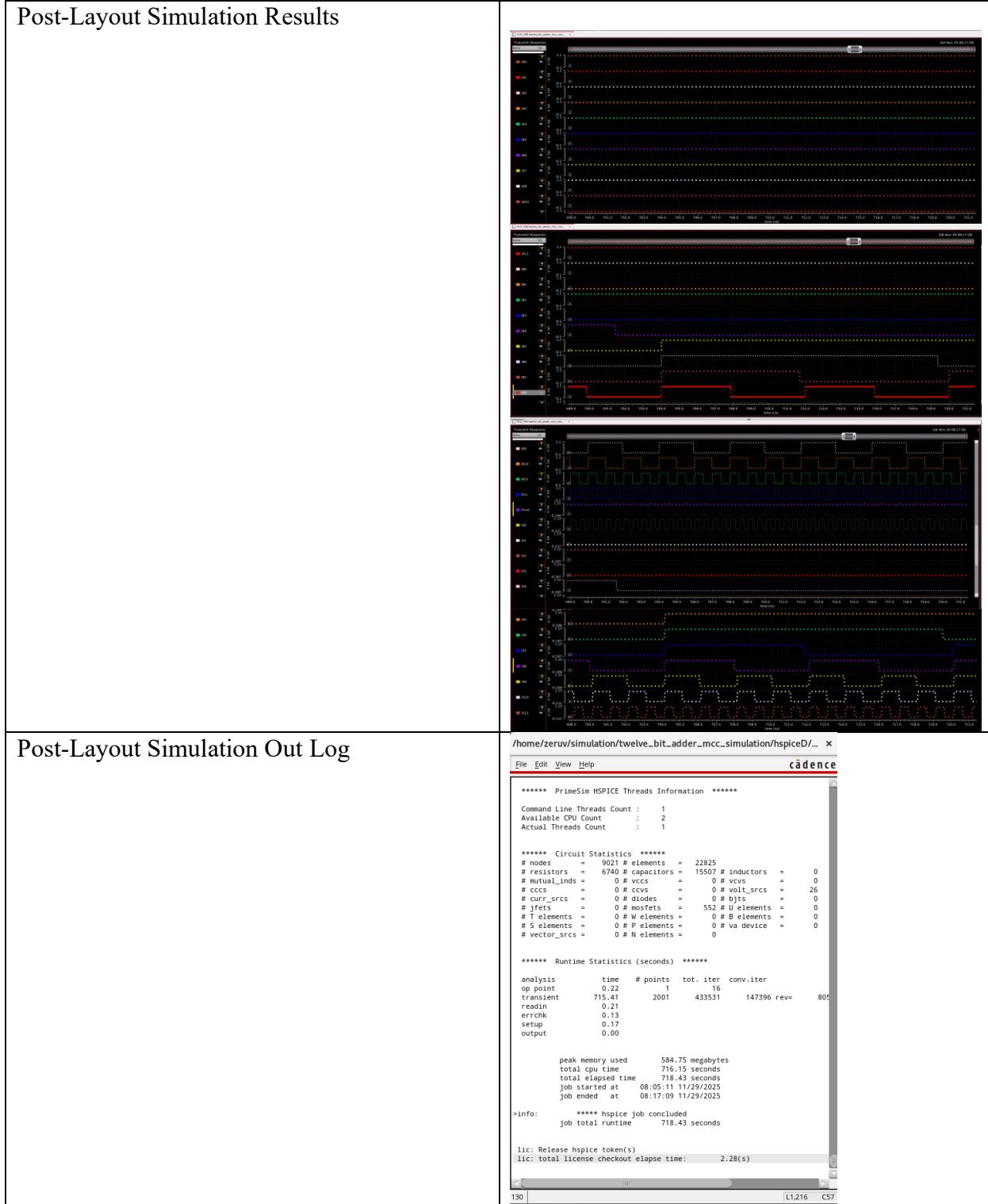
```

PEX Netlist Output

```

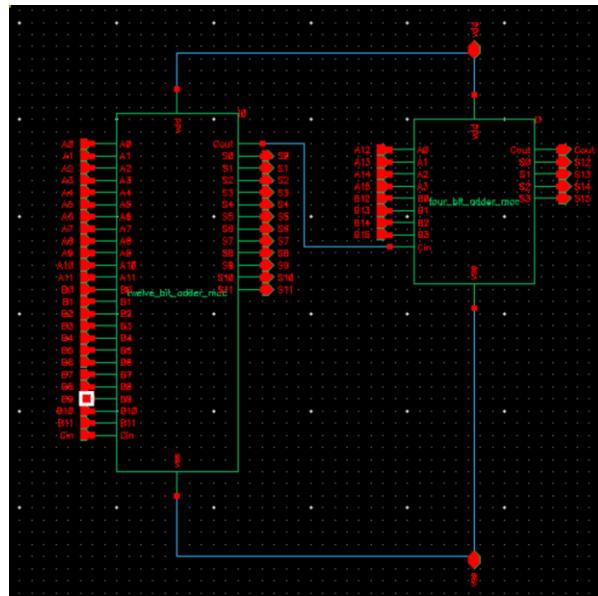
Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
twelve_bit_adder_mcc.pex.netlist *
1 * File twelve_bit_adder_mcc.pex.netlist
* Created: Sun Nov 30 04:41:55 2025
* Program "Calibre xRC"
* Version "v2024.3..25.13"
*
* include "twelve_bit_adder_mcc.pex.netlist.pex"
* include twelve_bit_adder.mcc.vss
* include twelve_bit_adder.mcc.vhd
* include twelve_bit_adder.mcc.vlog
* include twelve_bit_adder.mcc.vp
* include twelve_bit_adder.mcc.vt
* COUT COUT
* A11 A11
* A10 A10
* B11 B11
* B10 B10
* S11 S11
* S10 S10
* S8 S8
* S9 S9
* B9 B9
* B8 B8
* A9 A9
* A8 A8
* A7 A7
* A6 A6
* B7 B7
* B6 B6
* Z7 Z7
* S6 S6
* S4 S4
* S3 S3
* B5 B5
* B4 B4
* A4 A4
* A5 A5
* VDD VDD
* A3 A3
* A2 A2
* B3 B3
* B2 B2
* S3 S3
* S2 S2
* S1 S1
* CIN CIN
* B1 B1
* B0 B0

```

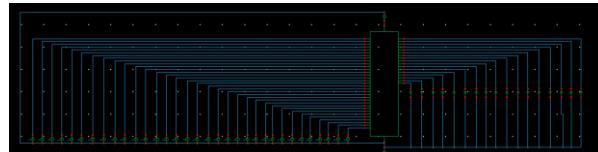
**Table 5: 16-Bit Carry Lookahead Adder With Manchester Carry Chain Implementation**

Required Snapshot Description	Snapshot
-------------------------------	----------

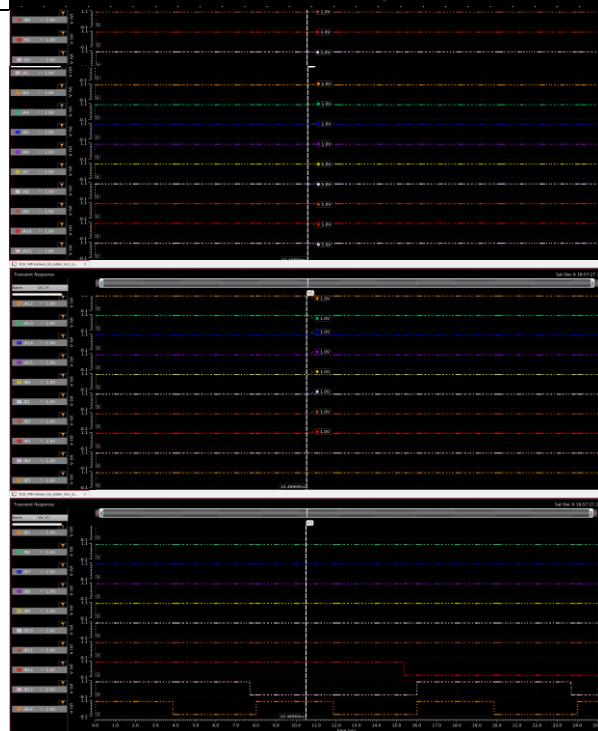
Schematic (Design)

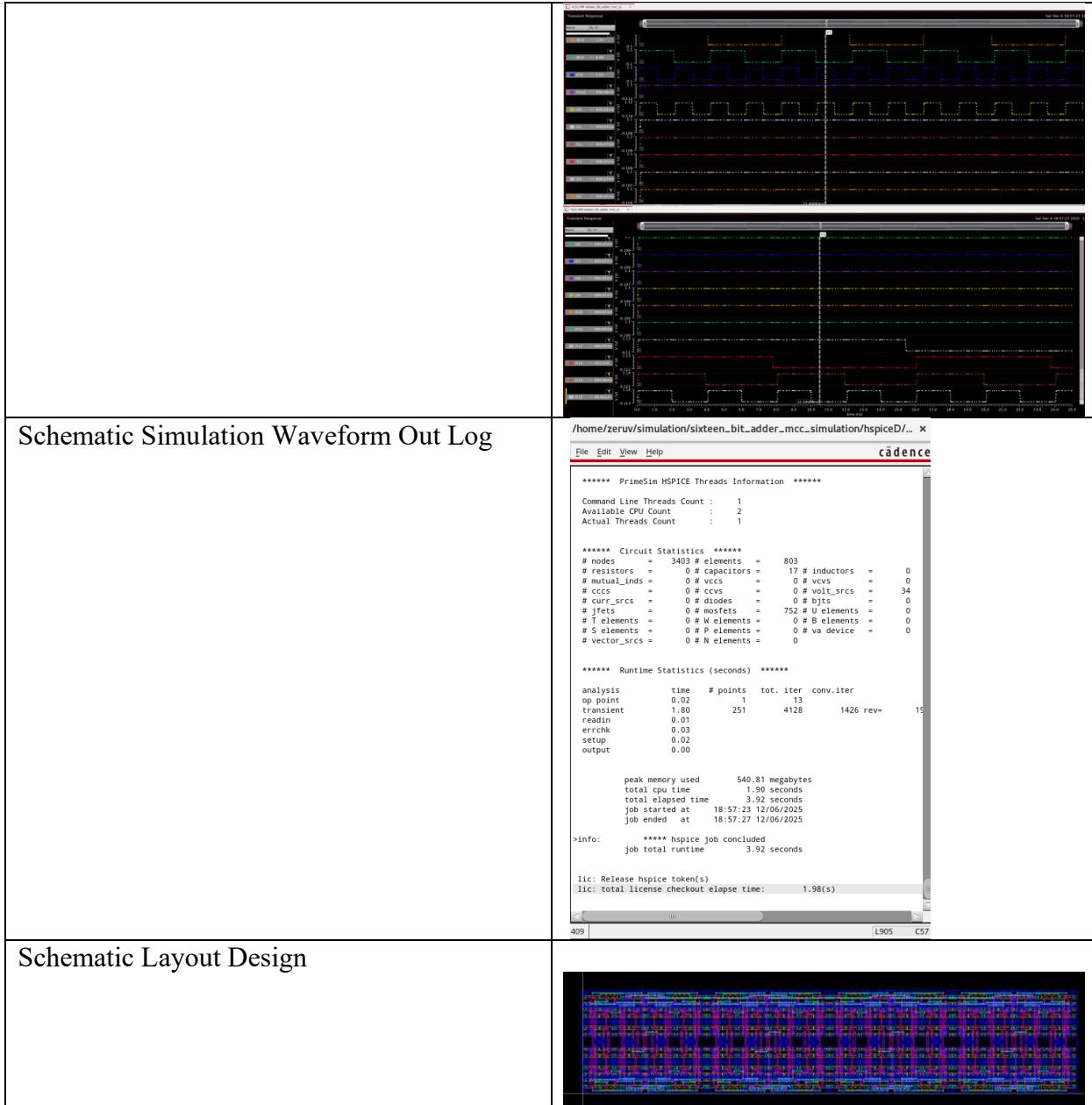


Schematic Simulation Waveform Design



Schematic Simulation Waveform Results





DRC Transcript

```
Calibre Interactive - nmDRC v2024.3..25.13 : ./runset.calibre.drc *
File Settings Configurations Help TOTAL CPU | 1/1
Rules Inputs Outputs Run Control Search Transcript Files
Cumulative EXECUTE TIME:CPU = 0 REAL = 0
Cumulative MISCCELLANEOUS Time: CPU = 0 REAL = 0
Cumulative CONNECT CPU = 0 REAL = 0
Cumulative RDB Time: CPU = 0 REAL = 0
-- CALIBRE:DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
-- TOTAL RULECHECKS EXECUTED = 167
-- DRC-H REPORT FILE = sixteen_bit_adder_mcc.drc.rpt
-- DRC RESULTS DATABASE FILE = sixteen_bit_adder_mcc.drc.results (ASCII)
-- DRC REPORT FILE = sixteen_bit_adder_mcc.drc.summary
-- DRC run finished with exit code 0 ***
INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -drc sixteen_bit_adder_mcc.drc.results
RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0-10-13-2017-1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Lhsa Libraries v2024..3..25..13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Copyright © Mentor Graphics Corporation 1996-2024
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RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI, the
RVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
RVE: //
RVE: // Mentor Graphics software executing under x86-64 Linux
RVE: //
RVE: // Running on 1 CPU
RVE: //
RVE: // Graphical User-Interface startup... Complete.
RVE: //
RVE: // Calibre4p0 license acquired.
RVE: // RVE authorized.

0 Errors, 1 Warning, 1 Info
Line Type Description
90 Warning Please increase descriptors limit for best performance (1024)
***
```

DRC Results

```
Calibre - RVE v2024.3..25.13 : sixteen_bit_adder_mcc.drc.results *
File View Highlight Tools Window Setup Help
File View Highlight Tools Window Setup Help
Filter: Show All No Results Found
Check / Cell Rest
✓ Check Well 1 0
✓ Check Well 2 0
✓ Check Well 4 0
✓ Check Poly 1 0
✓ Check Poly 2 0
✓ Check Poly 3 0
✓ Check Poly 4 0
✓ Check Poly 5 0
✓ Check Poly 6 0
✓ Check Active 1 0
✓ Check Active 2 0
✓ Check Active 3 0
✓ Check Active 4 0
✓ Check Implied 1 0
✓ Check Implied 2 0
✓ Check Implied 3 0
✓ Check Implied 4 0
Rule File Pathname: ..\calibre0RVE.rvl_
Well1 and Well1 must not overlap

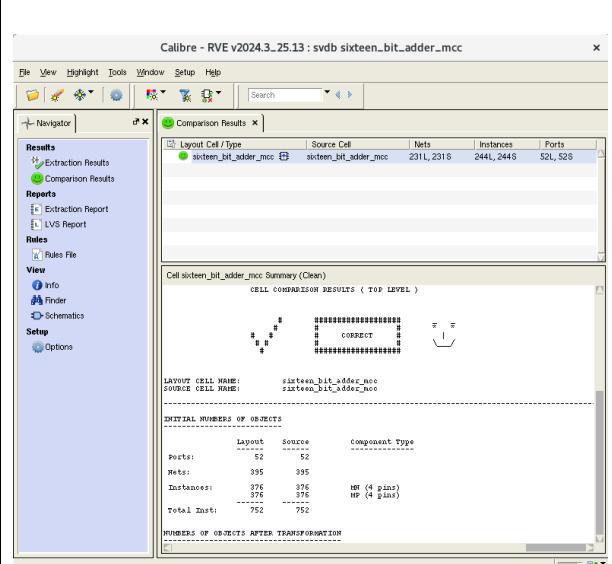
Calibre Run Completed Successfully -- Results are Valid
```

LVS Transcript

```
Calibre Interactive - nmLVS v2024.3..25.13 : ./runset.calibre.lvs *
File Settings Configurations Help TOTAL CPU | 2/2
Rules Inputs H-Cells Outputs Run Control Search Transcript Files
LVS completed. CORRECT. See report file: sixteen_bit_adder_mcc.lvs.report
LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 677/773 MALLOC = 93/93/93 ELAPSED TIME = 3
-- LVS REPORT FILE = sixteen_bit_adder_mcc.lvs.rpt
-- CALIBRE:LVS COMPARISON MODULE COMPLETED. TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 2/973 MALLOC = 95/95/95 ELAPSED TIME = 3
-- CALIBRE:LVSARC COMPUTED - Sun Nov 20 05:10:39 2025
-- XDR CROSS REFERENCE DATABASE = svb\sixteen_bit_adder_mcc.xdb
SPICE NETLIST FILE = sixteen_bit_adder_mcc.sp
CIRCUIT EXTRACTION REPORT FILE = sixteen_bit_adder_mcc.lvs.report.ext
PERSISTENT HIERARCHICAL DATABASE(PHDB) = svb\sixteen_bit_adder_mcc.phdb
OVERLAY REPORT FILE = svb\sixteen_bit_adder_mcc.overlay
GRAND TOTAL NON-HYPHEN COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP = 73 MALLOC = 102
*** LVS run finished with exit code 0 ***
INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -lvs svb\sixteen_bit_adder_mcc
RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0-10-13-2017-1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Lhsa Libraries v2024..3..25..13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Copyright © Mentor Graphics Corporation 1996-2024
RVE: // All Rights Reserved.
RVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
RVE: // WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
RVE: // OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI, the
RVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
RVE: //
RVE: // Mentor Graphics software executing under x86-64 Linux
RVE: //
RVE: // Starting command: $MGC_HOME/bin/calibre -nowait -rve -lvs svb\sixteen_bit_adder_mcc

0 Errors, 1 Warning, 2 Infos
Line Type Description
9 Info Verifying the source netlist is complete before starting the run
96 Warning Please increase descriptors limit for best performance (1024)
1820 Info Starting command: $MGC_HOME/bin/calibre -nowait -rve -lvs svb\sixteen_bit_adder_mcc
```

LVS Comparison Results



PEX Transcript

```
Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
--- NETWORK REDUCTION BEGIN:
--- READING FROM PDB...
--- BEGIN REDUCING NETS...
--- DONE REDUCING NETS...
--- WRITING TO PDB...
--- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 256/299/299 MALLOC = 276/276/276
--- PDB NET SUMMARY ---
pbd file name = svdbsIXTEEN_BIT_ADDER_MCC.pbd
root cell name = SIXTEEN_BIT_ADDER_MCC
total nets = 395
top-level nets = 235
non-top-level nets = 0
degenerate nets = 160
merged nets = 0
error nets = 0

--- CALIBRE XRC WARNING / ERROR Summary ---
xrc Warnings = 3
xrc Errors = 0
--- CALIBRE XRC:FORMATTER COMPLETED - Sun Nov 30 05:12:50 2025
--- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 16/76/299 MALLOC = 279/279/279 ELAPSED TIME = 3
*** xrc run finished with exit code 0 ***
2495
```

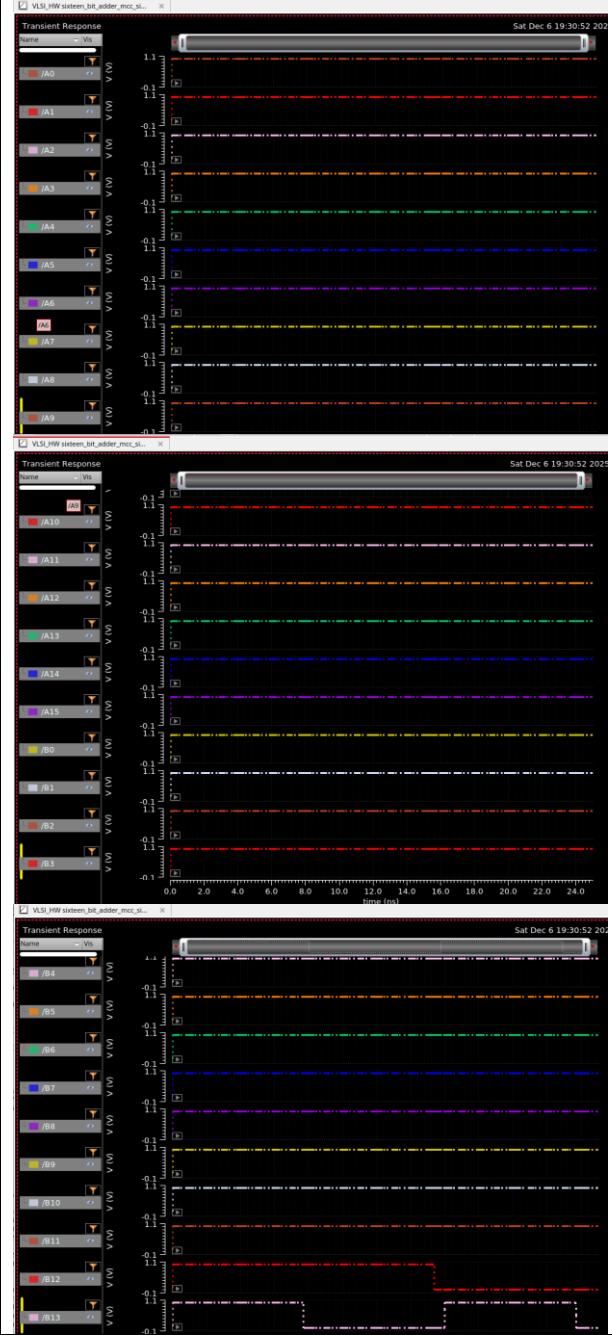
The screenshot shows the Calibre Interactive interface with the title "Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex". The "Transcript" tab is selected. The window displays the PEX transcript log, which includes network reduction statistics, a PDB net summary, and a CALIBRE XRC warning/error summary. The log concludes with a message indicating the xrc run finished with exit code 0.

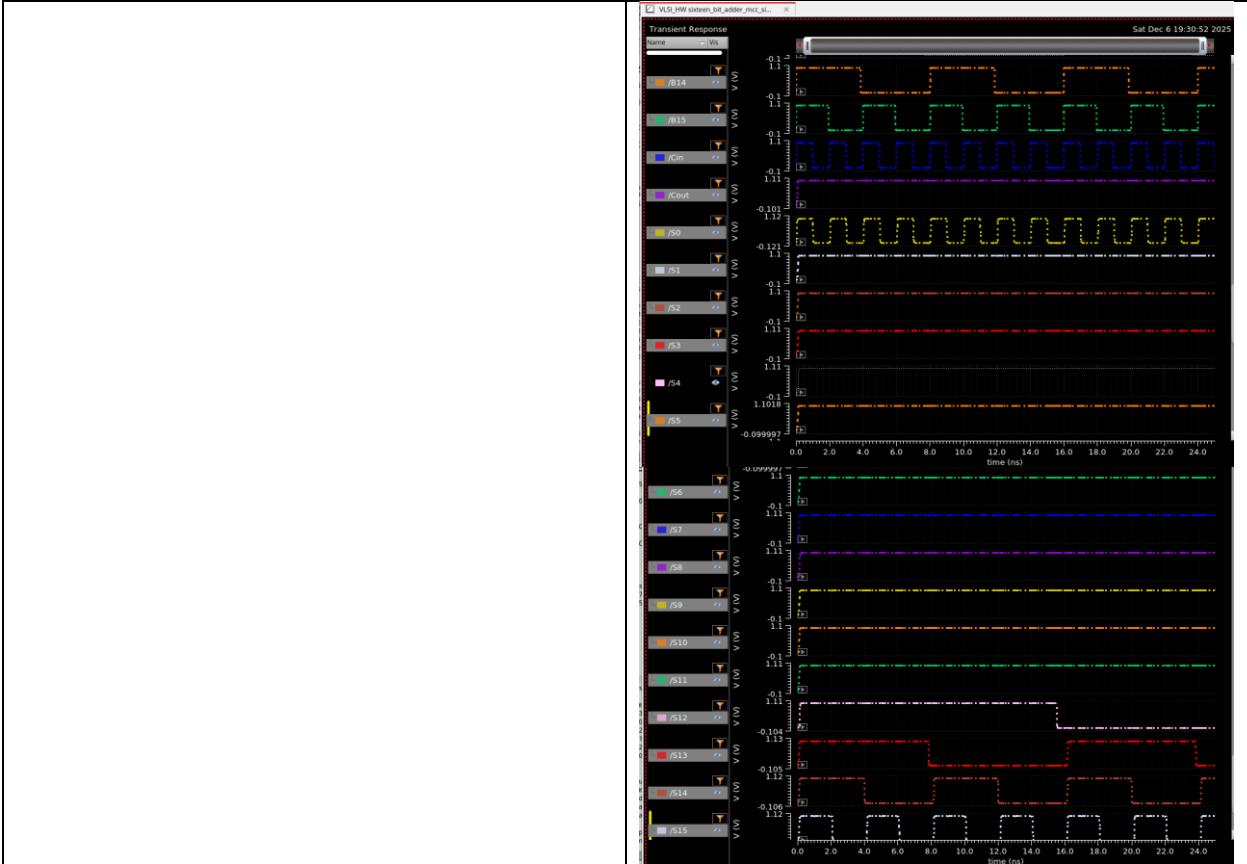
PEX Netlist Output

```
Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
sixteen_bit_adder_mcc.pex.netlist
1 * File: sixteen_bit_adder_mcc.pex.netlist
* Created: Sun Nov 30 05:12:49 2025
* Program: "Calibre xrc"
* Version: "v2024_3_25.13"
*
* include "sixteen_bit_adder_mcc.pex.netlist.pex"
* subcell "sixteen_bit_adder_mcc" VSS
* A0 A1 B0 B1 C0 S1 S0 S2 S3 B2 B3 A2 VDD
* + A12 A13 B12 B13 S7 S6 B6 B7 A7 A9 A8 B9 B8 B5 B10 S11 S12 B11 A11 A12
*
* COUT GOUT
* A14 A14
* A15 A15
* B13 B13
* B14 B14
* S15 S15
* A16 A16
* S12 S12
* S13 S13
* B15 B15
* B12 B12
* A13 A13
* A12 A12
* A10 A10
* A11 A11
* B10 B10
* B11 B11
* S11 S11
* S10 S10
* S8 S8
* S9 S9
* B8 B8
* A8 A8
* A9 A9
* A7 A7
* A6 A6
* S7 S7
* B6 B6
* S6 S6
* S2 S2
* S5 S5
* S4 S4
* B5 B5
* B4 B4
* A4 A4
* A5 A5
```

The screenshot shows the Calibre Interactive interface with the title "Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex". The "Files" tab is selected, displaying the netlist output for "sixteen_bit_adder_mcc.pex.netlist". The output lists various components and their connections, including subcells and specific pins like A0, A1, B0, B1, C0, S1, S2, S3, B2, B3, A2, VDD, A12, A13, B12, B13, S7, S6, B6, B7, A7, A9, A8, B9, B8, B5, B10, S11, S12, B11, A11, A12, COUT, GOUT, A14, A15, B13, B14, S15, A16, S12, S13, B15, B12, A13, A12, A10, A11, B10, B11, S11, S10, S8, S9, B8, A8, A9, A7, A6, S7, B6, S6, S2, S5, S4, B5, B4, A4, and A5.

Post-Layout Simulation Results







Post-Layout Simulation Out Log

```

/home/zeruv/simulation/sixteen_bit_adder_mcc_simulation/hspiceD... x
File Edit View Help                                         cadence
***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 12276 # elements = 31111
# resistors = 915 # capacitors = 21168 # inductors = 0
# mutual_linds = 0 # cccs = 0 # vccs = 0
# curr_srcs = 0 # diodes = 0 # bjt_srcs = 34
# curr_srcs = 0 # diodes = 0 # bjt_srcs = 0
# jfets = 0 # mosfets = 752 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # VA device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis      time   # points tot. iter conv. iter
op point     0.30      1       17
transient    8.02     251     3364    1123 rev=
readin       0.26
readch       0.15
setup        0.22
output       0.00

peak memory used      606.41 megabytes
total cpu time        8.97 seconds
total elapsed time    10.91 seconds
job started at        19:30:41 12/06/2025
job ended at          19:30:52 12/06/2025

>info: ***** hspice job concluded
job total runtime     10.91 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 1.94(s)

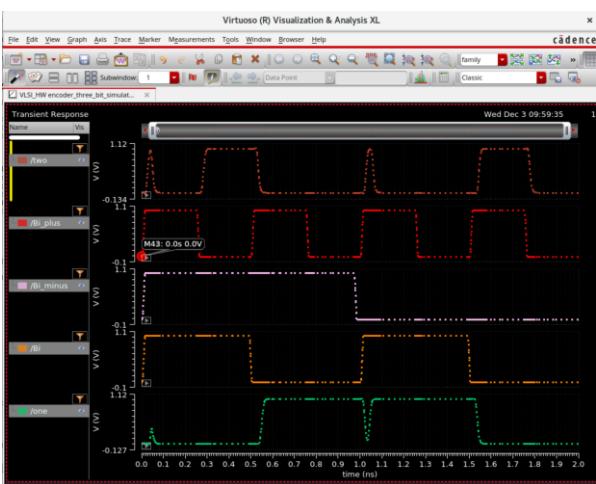
418 | Trace:/A8:Context:/home/zeruv/simulation/sixteen_bit_adder_mcc_simul L1,385 C1

```

Table 6: Encoder Sub-Circuit (3 Bit Encoder Using Radix-4 Booth Method)

Required Snapshot Description	Snapshot
Schematic (Design)	
Schematic Simulation Waveform Design	

Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```

***** primeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 221 # elements = 54
# resistors = 0 # capacitors = 2 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vccs = 0
# cccs = 0 # ccvs = 0 # volsrcs = 4
# curv_srcs = 0 # volsrcs = 0 # volsrcs = 0
# jfets = 0 # mosfets = 48 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op point 0.00 1 13 289 rev= 5
transient 0.06 41 797
readin 0.01
errchk 0.02
setup 0.00
output 0.00

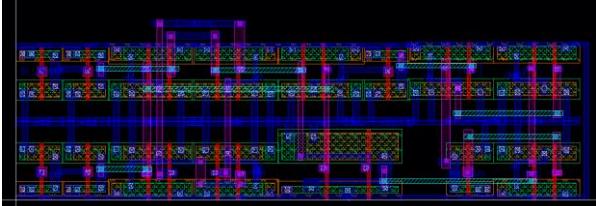
peak memory used 527.81 megabytes
total cpu time 0.10 seconds
total elapsed time 2.18 seconds
job started at 01:00:20 12/03/2025
job ended at 01:00:22 12/03/2025

>info: ***** hspice job concluded
job total runtime 2.18 seconds

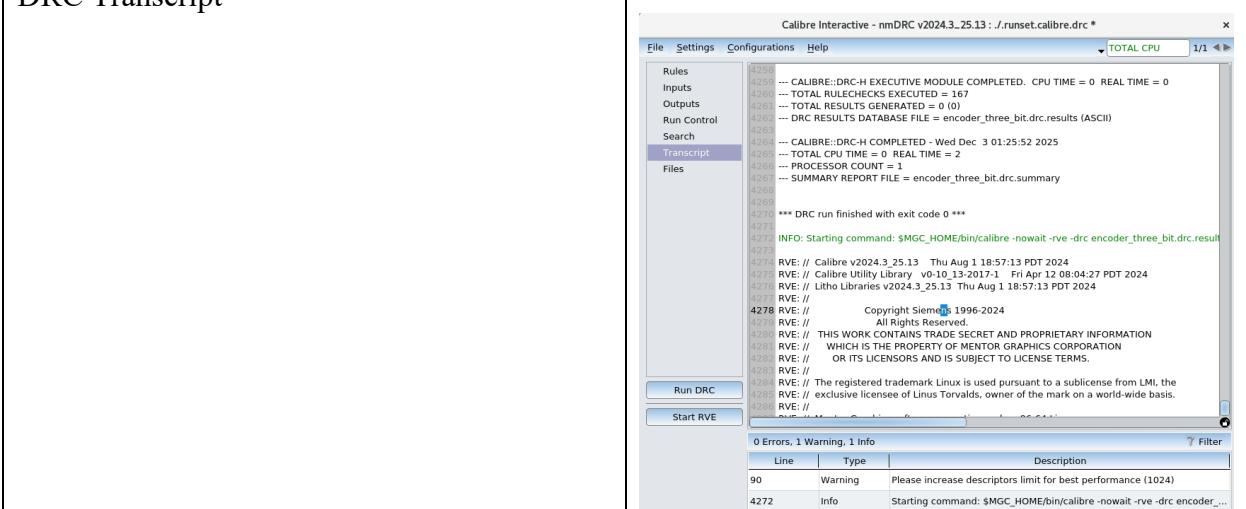
lic: Release hspice token(s)
lic: total license checkout elapse time: 2.05(s)

```

Schematic Layout Design



DRC Transcript



The screenshot shows the Calibre Interactive interface for nmDRC v2024.3_25.13. The menu bar includes File, Settings, Configurations, Help, TOTAL CPU, and 1/1. The main window displays a transcript of the DRC run. The transcript shows the following log entries:

```

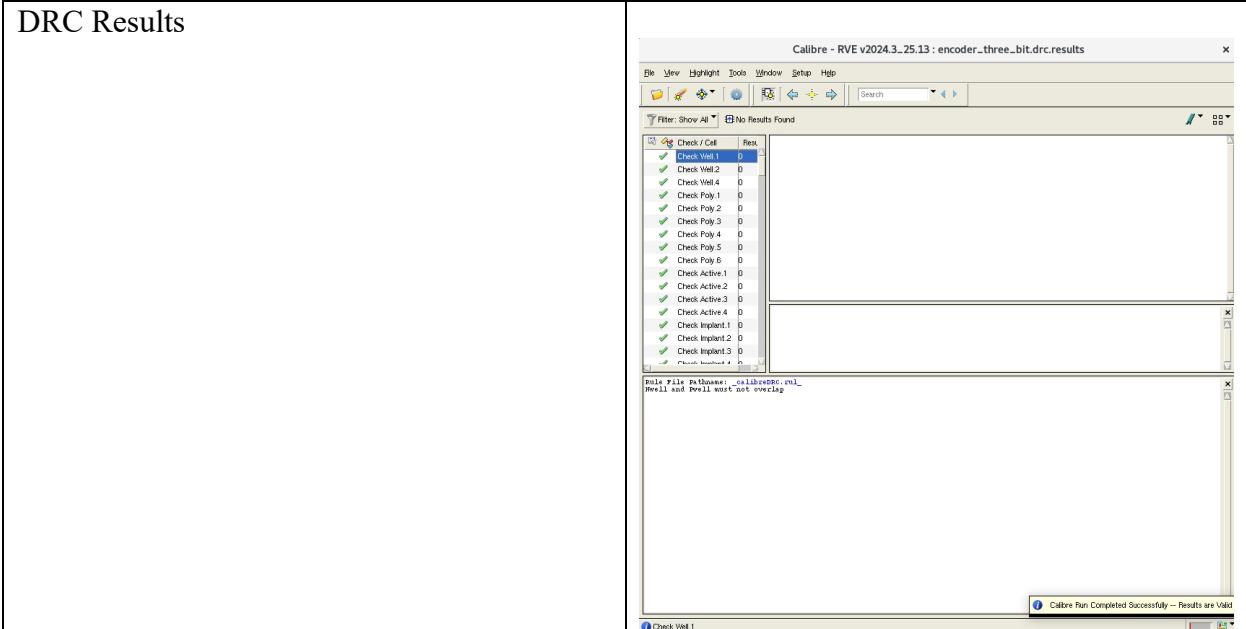
Rules          4258
Inputs         4259
Outputs        4260
Run Control   4261
Search         4262
Transcript    4263
Files          4264
4265 -- CALIBRE:DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
4266 -- TOTAL RULECHECKS EXECUTED = 167
4267 -- TOTAL RESULTS GENERATED = 0 (0)
4268 -- DRC RESULTS DATABASE FILE = encoder_three_bit.drc.results (ASCII)
4269
4270 -- CALIBRE:DRC-H COMPLETED - Wed Dec 3 01:25:52 2025
4271 -- TOTAL CPU TIME = 0 REAL TIME = 2
4272 -- PROCESSOR COUNT = 1
4273 -- SUMMARY REPORT FILE = encoder_three_bit.drc.summary
4274
4275 *** DRC run finished with exit code 0 ***
4276
4277 INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -drc encoder_three_bit.drc.result
4278 RVE: // Copyright Siemens 1996-2024
4279 RVE: // All rights reserved.
4280 RVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
4281 RVE: // WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
4282 RVE: // OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
4283 RVE: //
4284 RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI, the
4285 RVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
4286 RVE: //
4287
4288 Run DRC
4289 Start RVE

```

Below the transcript, there is a table titled "0 Errors, 1 Warning, 1 Info" with columns for Line, Type, and Description. The table contains two rows:

Line	Type	Description
90	Warning	Please increase descriptors limit for best performance (1024)
4272	Info	Starting command: \$MGC_HOME/bin/calibre -nowait -rve -drc encoder...

DRC Results



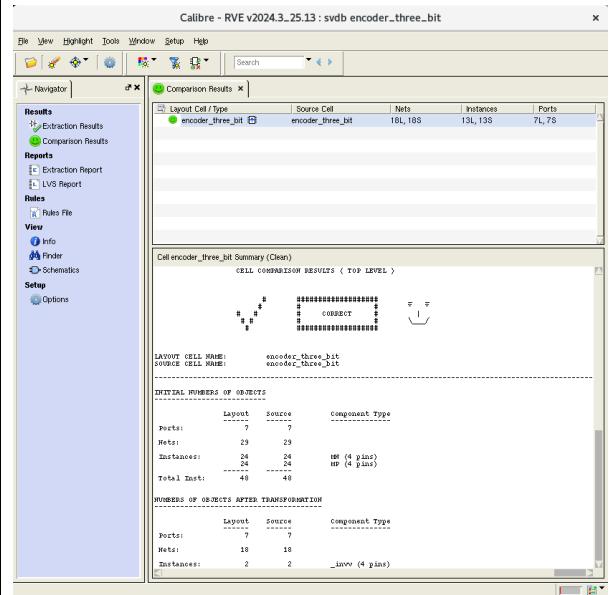
LVS Transcript

```

Calibre Interactive - nmLVS v2024.3..25.13 : ./runset.calibre.lvs *
File Settings Configurations Help TOTAL CPU 2/2 < >
Rules 1.6.3
Inputs 1.6.7
H-Cells 1.6.5
Outputs 1.6.4
LVS completed. CORRECT. See report file: encoder_three_bit.lvs.report
1.6.4
1.6.4 LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 67/69/69 MALLOC = 88/88/88 ELAPS
1.6.4
1.6.4 --- LVS REPORT FILE = encoder_three_bit.lvs.report
1.6.4 1643 --- CALIBRE:LVS/XRC COMPARISON MODULE COMPLETED. TOTAL CPU TIME = 0 REAL TIME = 0 LVH
1.6.4
1.6.4 --- CALIBRE:LVS/XRC COMPLETED - Wed Dec 3 01:26:48 2025
1.6.4 --- XDB CROSS REFERENCE DATABASE = svdb/encoder_three_bit.xdb
1.6.4
1.6.4 --- SPICE NETLIST FILE = encoder_three_bit.sp
1.6.4 --- CIRCUIT EXTRACTION REPORT FILE = encoder_three_bit.lvs.report.ext
1.6.4 --- PERSISTENT HIERARCHICAL DATABASE(PHDB) = svdb/encoder_three_bit.phdb
1.6.4 --- QUERY DATABASE = svdb TOP CELL = encoder_three_bit
1.6.4
1.6.4 --- GRAND TOTAL NON-HYPER/LVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP = 69 MAL
1.6.4
1.6.4 *** LVS run finished with exit code 0 ***
1.6.4
1.6.4 INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -lvs svdb encoder_three_bit
1.6.4
1.6.4 RVE: // Callibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
1.6.4 RVE: // Calibre Utility Library v0-10.13-2017-1 Fri Apr 12 08:04:27 PDT 2024
1.6.4 RVE: // Litho Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
1.6.4
1.6.4 RVE: // Copyright Siemens 1996-2024
1.6.4 RVE: // All Rights Reserved.
1.6.4 RVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
1.6.4 RVE: // WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
1.6.4 RVE: // OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
1.6.4 RVE: //
1.6.4 RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI, the
1.6.4 exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
1.6.4 RVE: //
1.6.4 RVE: // Mentor Graphics software executing under x86-64 Linux
1.6.4
1.6.4
0 Errors, 1 Warning, 2 Infos Filter
Line Type Description
9 Info Verifying the source netlist is complete before starting the run
one Warning Please increase deserializer limits for best performance (/var)

```

LVS Comparison Results



PEX Transcript

```
File Settings Configurations Help Search
-----  
Rules  
Inputs  
Outputs  
LVS  
Run Control  
Search  
Transcript  
Files  
  
2260  
2261 -----  
2262 PDB NET SUMMARY -----  
2263  
2264 pdb file name = svdb/ENCODER_THREE_BIT.pdb  
2265 root cell name = ENCODER_THREE_BIT  
2266 total nets = 29  
2267 top-level nets = 20  
2268 non-top-level nets = 0  
2269 degenerate nets = 9  
2270 merged nets = 0  
2271 error nets = 0  
2272  
2273 -----  
2274 CALIBRE XRC WARNING / ERROR Summary  
2275 -----  
2276 xRC Warnings = 3  
2277 xRC Errors = 0  
2278 -----  
2279  
2280  
2281  
2282 --- CALIBRE xRC::FORMATTER COMPLETED - Wed Dec 3 10:23:38 2025  
2283 --- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 15/76/299 MALLOC = 266/266/266 ELAPSE  
2284  
2285  
2286 *** xRC run finished with exit code 0 ***  
2287  
  
Run PEX  
Start RVE  
  
0 Errors, 10 Warnings, 1 Info Filter  


| Line | Type    | Description                                                        |
|------|---------|--------------------------------------------------------------------|
| 10   | Info    | Verifying the source netlist is complete before starting the run   |
| 97   | Warning | Please increase descriptors limit for best performance (1024)      |
| 128  | Warning | PEX RESISTANCE LUMPED is obsolete. Please remove from your rule... |
| 256  | Warning | PEX RESISTANCE LUMPED is obsolete. Please remove from your rule... |
| 1793 | Warning | Please increase descriptors limit for best performance (1024)      |
| 1822 | Warning | PEX RESISTANCE LUMPED is obsolete. Please remove from your rule... |


```

PEX Netlist Output

```
Calibre Interactive - PEX v2024.3_25.13 : ./runset.calibre.pex *
```

File Settings Configurations Help

Search

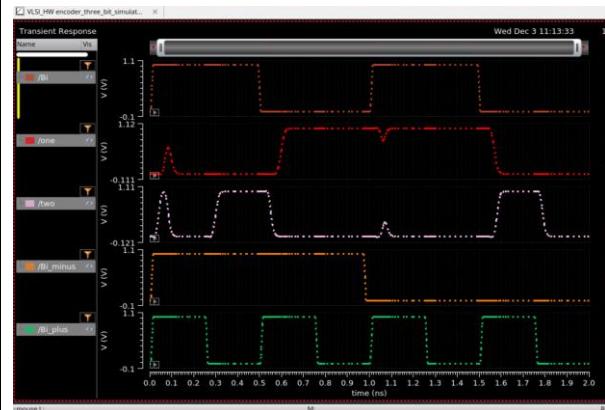
Calibre

Rules
Inputs
Outputs
LVS
Run Control
Search
Transcript
Files

encoder_three_bit_hex.netlist x

1 File: encoder_three_bit_hex.netlist
+ Created: Wed Dec 3 10:23:37 2025
+ Program "Calibre xcRC"
+ Version "v2024.3_25.13"
+
.include "encoder_three_bit.pex.netlist"
subckt encoder_three_bit BI_PLUS BI_MINUS VDD VSS ONE TWO
+
+
TWO TWO
+
ONE ONE
VSS VSS
VDD VDD
BI_MINUS BI_MINUS
BI BI
BI_PLUS BI_PLUS
m0/X10/MM2_X11/MM2_d_n NETL_X10/MM3_g_N_VSS_X10/MM3_s_N_VSS_X10/MM1_b
+ NMOS_VTL_L=5e-09 W=1e-07 AD=3.35e-14 AS=5.825e-14 PD=8.7e-05 PS=1.365e-06
m1/X12/MM2_N_NET2_X12/MM2_d_N NETL_X12/MM2_g_N_VSS_X12/MM2_s_N_VSS_X10/MM1_b
+ NMOS_VTL_L=5e-08 W=1e-07 AD=4.15e-14 AS=5.825e-14 PD=1.036e-06 PS=1.365e-06
m2/X12/MM2_X10/NET1_N_NET1_X12/MM2_g_N_VDD_X12/MM2_s_N_VDD_X10/MM2_b PMOS_VTL
+ L=5e-08 W=4e-07 AD=2.33e-13 AS=1.09e-13 PD=1.965e-06 PS=1.345e-06
m3/X11/MM1_N_NET2_X12/MM2_d_n NETL_X11/MM2_g_X12/NET1_N_VDD_X10/MM2_b PMOS_VTL
+ L=5e-08 W=4e-07 AD=1.66e-13 AS=2.33e-13 PD=1.636e-06 PS=1.965e-06
m4/X10/MM2_N_NET2_X11/MM2_d_n NETL_X10/MM2_g_N_VSS_X10/MM2_s_N_VSS_X10/MM1_b
+ NMOS_VTL_L=5e-08 W=1e-07 AD=2.45e-14 AS=5.7e-14 PD=9.07e-05 PS=5.7e-07
m5/X10/MM2_X10/NET1_N_NET1_X10/MM2_d_n BI_MINUS_X10/MM2_g_N_VDD_X10/MM2_b
+ PMOS_VTL_L=5e-08 W=1e-07 AD=4.9e-14 AS=3.7e-14 PD=8.9e-07 PS=7.7e-07
m6/X11/MM1_N_NET2_X11/MM2_d_n BI_MINUS_X11/MM1_g_N_VSS_X11/MM1_b
+ N_VSS_X11/MM1_b NMOS_VTL_L=5e-08 W=1e-07 AD=2.45e-14 AS=1.85e-14 PD=6.9e-07
PS=5.7e-07
m7/X11/MM2_N_NET2_X11/MM2_d_n BI_MINUS_X11/MM2_g_N_VDD_X11/MM2_b
+ PMOS_VTL_L=5e-08 W=1e-07 AD=4.9e-14 AS=3.7e-14 PD=8.9e-07 PS=7.7e-07
m8/X12/MM2_N_NET2_X12/MM2_d_n NETL_X12/MM2_g_N_VSS_X12/MM2_s_N_VSS_X10/MM1_b
+ NMOS_VTL_L=5e-08 W=1e-07 AD=2.45e-14 AS=1.85e-14 PD=9.07e-05 PS=5.7e-07
m9/X12/MM2_N_NET2_X12/MM2_d_n NETL_X12/MM2_g_N_VDD_X12/MM2_s_N_VDD_X10/MM2_b
+ PMOS_VTL_L=5e-08 W=1e-07 AD=4.9e-14 AS=3.7e-14 PD=8.9e-07 PS=7.7e-07
m10/X11/MM1_N_NET2_X11/MM2_d_n NETL_X11/MM1_g_N_VSS_X11/MM1_b
+ NMOS_VTL_L=5e-08 W=1e-07 AD=2.45e-14 AS=1.85e-14 PD=9.07e-05 PS=5.7e-07
m11/X12/MM2_N_NET2_X12/MM2_d_n NETL_X12/MM2_g_N_VDD_X12/MM2_s_N_VDD_X11/MM2_b
+ PMOS_VTL_L=5e-08 W=1e-07 AD=4.9e-14 AS=3.7e-14 PD=8.9e-07 PS=7.7e-07
Run PEX
Start RVE

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```
/home/zeruv/simulation/encoder_three_bit_simulation/hspiceD/sche... x
File Edit View Help                                         cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 764 # elements = 1836
# resistors = 560 # capacitors = 1217 # inductors = 0
# mosfets_lnds = 0 # vccs = 0 # vctrl = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 4
# curr_srcs = 0 # diodes = 0 # bjts = 0
# jfets = 0 # mosfets = 48 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # vector elements = 0 # device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis      time   # points tot. iter conv.ITER
op point     0.02           1       87
transient    0.10          41      620      226 rev=
readin       0.02
errchk       0.01
setup        0.01
output       0.00

peak memory used      529.82 megabytes
total cpu time        0.17 seconds
total elapsed time    2.48 seconds
job started at        11:13:31 12/03/2025
job ended at          11:13:33 12/03/2025

>info: ***** hspice job concluded
      job total runtime 2.48 seconds

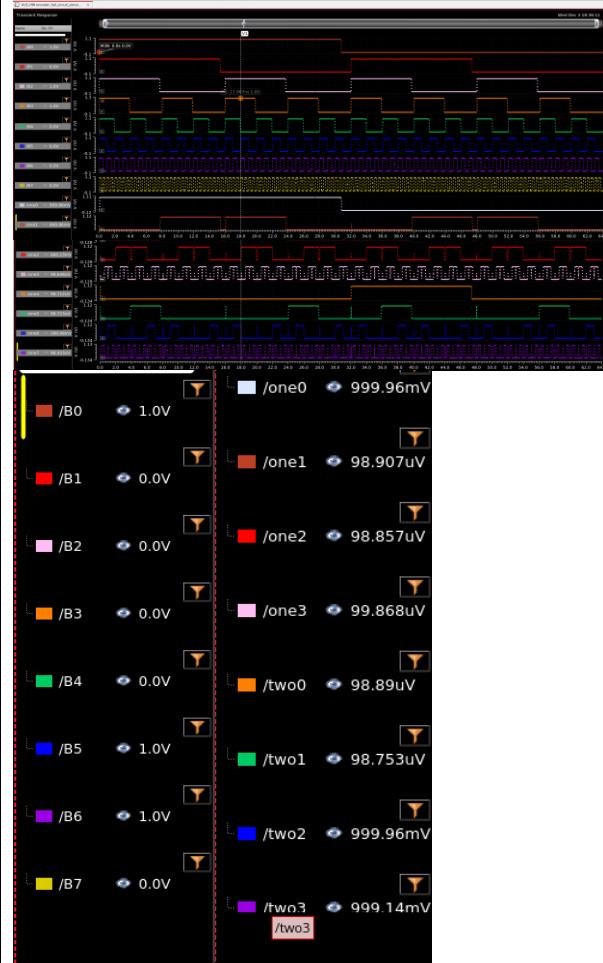
lic: Release hspice token(s)
lic: total license checkout elapse time: 2.32(s)

302 Trace:/B1 plus; Context: /home/zeruv/simulation/encoder_three_bit_simul L730 C18
```

Table 7: Full Encoder Circuit

Required Snapshot Description	Snapshot
Schematic (Design)	
Schematic Simulation Waveform Design	

Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 874 # elements = 209
# resistors = 0 # capacitors = 8 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vcv = 0
# ccs = 0 # vdd = 0 # vdd_srcs = 0
# curr_srcs = 0 # diodes = 0 # bjt_srcs = 0
# jfets = 0 # mosfets = 192 # U_elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op point 0.00 1 13
transient 3.61 1281 28423 10189 rev= 134
readin 0.01
errchk 0.03
setup 0.00
output 0.00

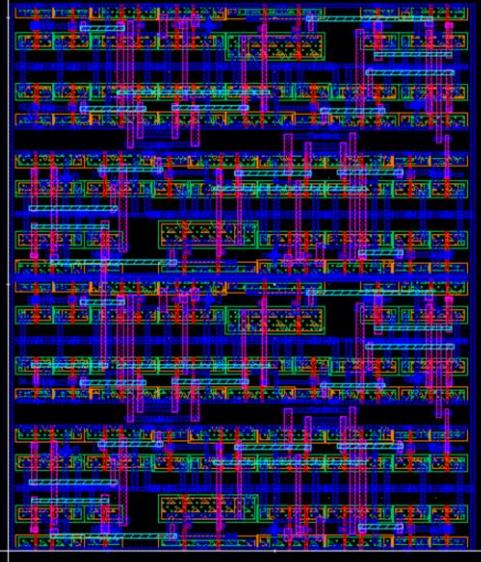
peak memory used 527.81 megabytes
total cpu time 3.66 seconds
total elapsed time 5.62 seconds
job started at 18:36:01 12/03/2025
job ended at 18:36:11 12/03/2025

>info: ***** hspice job concluded
      job total runtime 5.62 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 1.92(s)

```

Schematic Layout Design



DRC Transcript

```

Calibre Interactive - nmDRC v2024.3..25.13 : ./unset.calibre.drc
File Settings Configurations Help TOTAL CPU 1/1
Rules ----- CALIBRE-DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
Inputs ----- TOTAL RULE CHECKS EXECUTED = 167
Outputs ----- TOTAL REPORTS GENERATED = 0
Run Control ----- DRC RESULTS DATABASE FILE = encoder_full_circuit.drc.results (ASCII)
Search ----- CALIBRE-DRC-H COMPLETED - Thu Dec 4 02:37:11 2025
4266 ----- TOTAL CPU TIME = 0 REAL TIME = 2
Processor COUNT = 1
Files ----- PROCESSOR COUNT = 1
----- SUMMARY REPORT FILE = encoder_full_circuit.drc.summary

*** DRC run finished with exit code 0 ***
INFO: Starting command: SMIC_HOME/bin/calibre -nowait -rve -drc encoder_full_circuit.drc.results
RVE:// Calibre v2024.3.25.13 Thu Aug 1 18:57:13 PDT 2024
RVE:// Calibre Utility v2024.3.25.13 Thu Aug 1 18:57:13 PDT 2024
RVE:// Lulu Library v2024.3.25.13 Thu Aug 1 18:57:13 PDT 2024
RVE:// Copyright Siemens 1998-2024
RVE:// All rights Reserved.
RVE:// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
RVE:// WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
RVE:// OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
RVE://
RVE:// The registered trademark Linux is used pursuant to a sublicense from LMI, the
RVE:// exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
RVE://
RVE:// Mentor Graphics software executing under x86-64 Linux
RVE://
RVE:// Running on 1 CPU
RVE://
RVE://
0 Errors, 1 Warning, 1 Info
Line Type Description
90 Warning Please increase descriptors limit for best performance (1024)
*** File Pathname: ./calibre@enc_rve.rve
No Results Found

```

DRC Results

Calibre - RVE v2024.3..25.13 : encoder_full_circuit.drc.results	
File View Highlight Tools Window Setup Help	
Filter: Show All ▾ No Results Found	
Check / Cell	Res
✓ Check Well 1	0
✓ Check Well 2	0
✓ Check Well 4	0
✓ Check Poly 1	0
✓ Check Poly 2	0
✓ Check Poly 3	0
✓ Check Poly 4	0
✓ Check Poly 5	0
✓ Check Poly 6	0
✓ Check Active 1	0
✓ Check Active 2	0
✓ Check Active 3	0
✓ Check Active 4	0
✓ Check Implan 1	0
✓ Check Implan 2	0
✓ Check Implan 3	0
✓ Check Implan 4	0
✓ Check Contact 1	0
✓ Check Contact 2	0
✓ Check Contact 3	0
Rule File Pathname: ./calibre@enc_rve.rve	
Well1 and Poly1 must not overlap	
Calibre Run Completed Successfully -- Results are Valid	
Check Well 1	

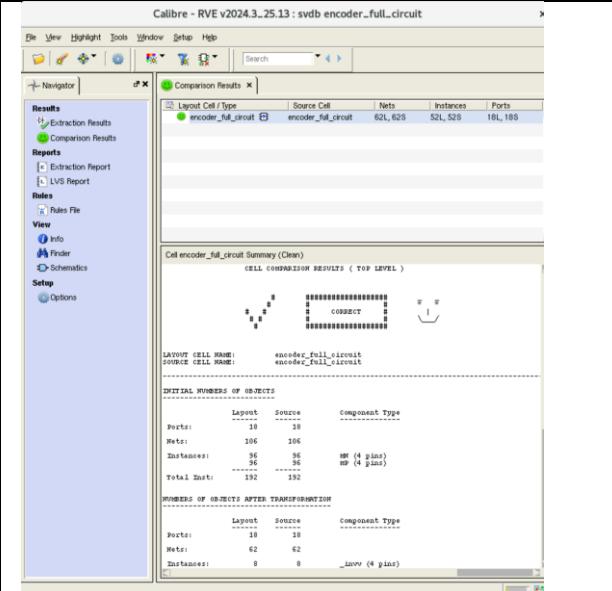
LVS Transcript

```

Calibre Interactive - nmLVS v2024.3..25.13 : ./runset.calibre.lvs *
File Settings Configurations Help TOTAL CPU 2/2
Rules Inputs Outputs LVS completed. CORRECT. See report file: encoder_full_circuit.lvs.report
H-Cells
EBC
Signatures Run Control Search
Transcript --- LVS REPORT FILE = encoder_full_circuit.lvs.report
Files --- CALIBRE-LVS/XRC COMPLETED - Thu Dec 4 02:54:11 2025
--- XDB CROSS REFERENCE DATABASE = svtbvencoder_full_circuit.xdb
--- SPICE NETLIST FILE = encoder_full_circuit.sp
--- CIRCUIT EXTRACTION REPORT FILE = encoder_full_circuit.xls.report
--- PDKS/HDL LIBRARIES = ./nmLVS/nmLVS/phdbs
--- QUERY DATABASE = svtbv TOP CELL = encoder_full_circuit
--- GRAND TOTAL NON-HYPERLVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP = 69 MALLOC = 95
*** LVS run finished with exit code 0 ***
INFO: Starting command: NMIC_HOME/bin/calibre -nosalt -rve -lvs svtbv encoder_full_circuit
RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library - v0.10.3-2017.3 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Copyright Siemens 1996-2024
RVE: // All Rights Reserved
RVE: // THIS WORK IS PROVIDED "AS IS" WITHOUT WARRANTY OR PROPRIETARY INFORMATION
RVE: // WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
RVE: // OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
RVE: // MENTOR
RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI, the
RVE: // owner of the trademark in the United States.
0 Errors, 1 Warning, 2 Infos
Line Type Description
4 Info Verifying the source netlist is complete before starting the run
n/a Information Please increase description limit for best performance (1000)

```

LVS Comparison Results



PEX Transcript

```

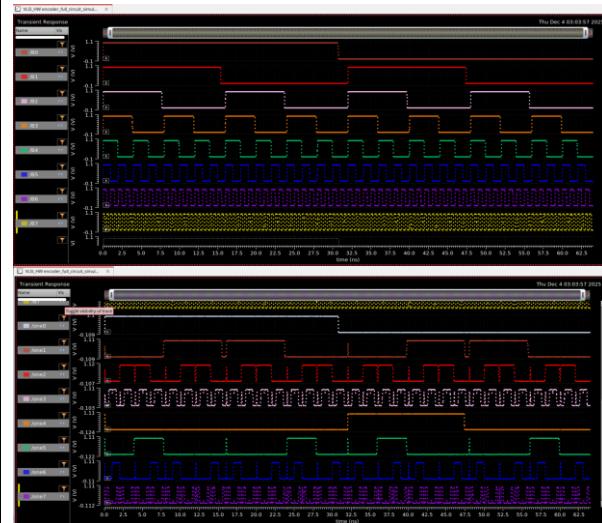
Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS
Run Control Search
Transcript --- NETWORK REDUCTION BEGIN:
--- READING FROM PDB...
--- WORKING ON PDB FILE name defined in PDB NETLIST statement and "D" will be used in the netlist.
--- BEGIN REDUCING NETS...
--- DONE REDUCING NETS...
--- WRITING TO PDB...
--- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 255/299/299 MALLOC = 261/261/261
--- PDB NET SUMMARY ---
pbd file name = svtbvENCODER_FULL_CIRCUIT.pbd
root cell name = ENCODER_FULL_CIRCUIT
total nets = 106
top-level nets = 36
non-top-level nets = 0
degenerate nets = 36
merged nets = 0
error nets = 0
-----CALIBRE-XRC WARNING / ERROR SUMMARY-----
xRC Warnings = 3
xRC Errors = 0
-----CALIBRE-XRC FORMATTER COMPLETED - Thu Dec 4 02:57:46 2025
--- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 157/6/299 MALLOC = 262/262/262 ELAPSED TIME = 2
*** xRC run finished with exit code 0 ***
2334
0 Errors, 10 Warnings, 1 Info
Line Type Description
10 Info Verifying the source netlist is complete before starting the run
n/a Information Please increase description limit for best performance (1000)

```

PEX Netlist Output

```
Calibre Interactive - PEX v2014.3.25.13 : /runset.calibre.prj *  
File Settings Configurations Help  
  
Rules Inputs Outputs LVS Run Control Search Transcript File  
  
encoder_full_circuit.pex.netlist x  
1 * File: encoder_full_circuit.pex.netlist  
  * Created: Thu Dec 4 02:57:46 2025  
  * Program: "Calibre xRC"  
  * Version: "v2014.3_25.13"  
  
  included 'encoder_full_circuit.pex.netlist.pex'  
  included 'encoder_full_circuit.b3.85.81.V55.B4.80.TW01.B03.TW03.B7.VD0.ONE0.ONE2.ONE3  
  + ONE1.TWO2.TW00.BB.92  
  
    B2  
    B6  
    TW00  
    TW01  
    TW02  
    ONE1  
    ONE3  
    ONE4  
    ONE5  
    ONE6  
    VDD  
    VDD  
    B7  
    TW03  
    TW02  
    TW01  
    B0  
    B4  
    V55  
    V55  
    B1  
    B5  
    B5  
    B1  
    B1  
    N03X02X0MM2_N.X03XNET2_X10X02XMM3_d.N.X03XNET1_X10X02XMM2_g  
+ N.V55_X03X02XMM3_i.N_V55_X03X10X0MM1_b_NMOS_VTL.L=5e-08_W=1e-07_AD=3.35e-14  
+ AS=5.42e-14_P0=7e-07_P1=3.65e-06  
+ N_V55_X03X02XMM3_s.v_V55_X03X10X0MM1_b_NMOS_VTL.L=5e-08_W=1e-07_AD=4.15e-14  
+ AS=5.42e-14_P0=7e-07_P1=3.65e-06  
+ N_V55_X03X02XMM3_d.v_V55_X03X10X0MM1_g_N.VDD_X10X02XMM2_s  
+ N_VDD_X10X02XMM2_d.PMOS_VTL.L=5e-08_W=4e-07_AD=2.33e-13_A5=1.09e-13  
+ N_VDD_X10X02XMM2_d.N_X03XNET3_X10X02XMM1_g_X10X02XMM1_s  
+ N_VDD_X10X02XMM2_d.PMOS_VTL.L=5e-08_W=4e-07_AD=1.66e-13_A5=2.33e-13  
+ PD=1.63e-06_P0=1.96e-06_P1=1.34e-06  
+ N_X03X10X0MM1_d.N_B6_X10X01X0MM1_g_N_V55_X03X10X0MM1_s  
+ N_V55_X03X10X0MM1_b_NMOS_VTL.L=5e-08_W=1e-07_AD=2.45e-14_A5=1.85e-14
```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```

/home/zeruv/simulation/encoder_full_circuit_simulation/hspiceD/sch... x

File Edit View Help                                         cädence

***** PrimeSim HSPICE Threads Information *****

Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 3064 # elements = 7505
# resistors = 2283 # capacitors = 5021 # inductors = 0
# minimal_conds = 0 # vccs = 0 # vccv = 0
# cccs = 0 # vdds = 0 # vddv = 0
# curc_srcs = 0 # diodes = 0 # bjts = 0
# jfets = 0 # mosfets = 192 # B elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis          time      # points    tot. iter conv.ite
op point         0.10           1        82
transient        15.84       1281     22440   8191 rev= 32
readin          0.06
errchk          0.04
setup            0.05
output           0.00

peak memory       549.39 megabytes
total cpu time   16.11 seconds
total elapsed time 18.21 seconds
job started at   03:03:39 12/04/2025
job ended at     03:03:57 12/04/2025

>info:        **** hspice job concluded
                job total runtime   18.21 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time:      2.10(s)

```

Table 8: Decoder Sub-Circuit (2-Bit Decoder for Generation of Bits of Each Partial Product)

Required Snapshot Description	Snapshot
Schematic (Design) f	
Schematic Simulation Waveform Design	
Schematic Simulation Waveform Results	

Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/decoder_subcircuit_simulation/hspiceD/sche... x
File Edit View Help
cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 133 # elements = 35
# resistors = 0 # capacitors = 1 # inductors = 0
# mosfets = 0 # vols = 0 # vccs = 6
# cccs = 0 # ccvs = 0 # volt_srcs = 0
# curr_srcs = 0 # diodes = 0 # bnts = 0
# jfets = 0 # mosfets = 28 # U_elements = 0
# elements = 0 # W_elements = 0 # B_elements = 0
# gnd_ports = 0 # pwr_ports = 0 # va_device = 0
# vector_srcs = 0 # N_elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.iterator
op point 0.00 1 13
transient 0.14 201 3557 1327 rev= 15
readin 0.00
errchk 0.00
setup 0.00
output 0.00

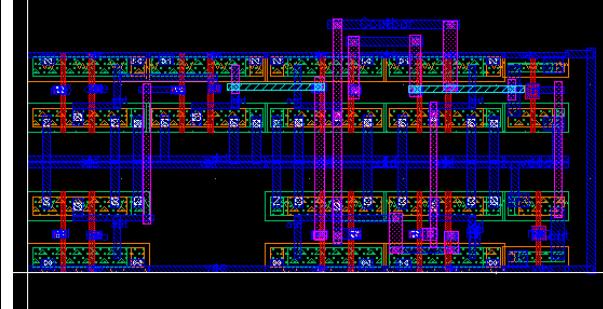
peak memory used 527.81 meabytes
total cpu time 0.15 seconds
total elapsed time 2.25 seconds
job started at 14:04:45 12/01/2025
job ended at 14:04:47 12/01/2025

>info: **** hspice job concluded
      job total runtime 2.25 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.09(s)

237 | Trace: /nep: Context: /home/zeruv/simulation/decoder_subcircuit_simulat | L629 C24
```

Schematic Layout Design



DRC Transcript

Calibre Interactive - nmDRC v2024.3_25.13 : /

```
File Settings Configurations Help
Rules 4250 -- CALIBRE:DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
Inputs 4251 -- TOTAL RULECHECKS EXECUTED = 167
Outputs 4252 -- TOTAL RESULTS GENERATED = 0 (0)
Run Control 4253 -- DRC RESULTS DATABASE FILE = decoder_subcircuit.drc.results (ASCII)
Search 4254 -- CALIBRE:DRC-H COMPLETED - Mon Dec 1 14:08:51 2025
Transcript 4255 -- TOTAL CPU TIME = 0 REAL TIME = 2
Files 4256 -- PROCESSOR COUNT = 1
        -- SUMMARY REPORT FILE = decoder_subcircuit.drc.summary
        -- *** DRC run finished with exit code 0 ***
4257 INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -drc decoder_subcircuit.drc.results
4258 RVE: // Calibre v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
4259 RVE: // Calibre Utility Library: vb-10_13-2017-1 Fri Apr 12 08:04:27 PDT 2024
4260 RVE: // Litho Libraries v2024_3_25.13 Thu Aug 1 18:57:13 PDT 2024
4261 RVE: // Copyright Siemens 1996-2024
4262 RVE: // All Rights Reserved.
4263 RVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
4264 RVE: // WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
4265 RVE: // OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
4266 RVE: //
4267 RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI, the
4268 RVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
4269 RVE: //
```

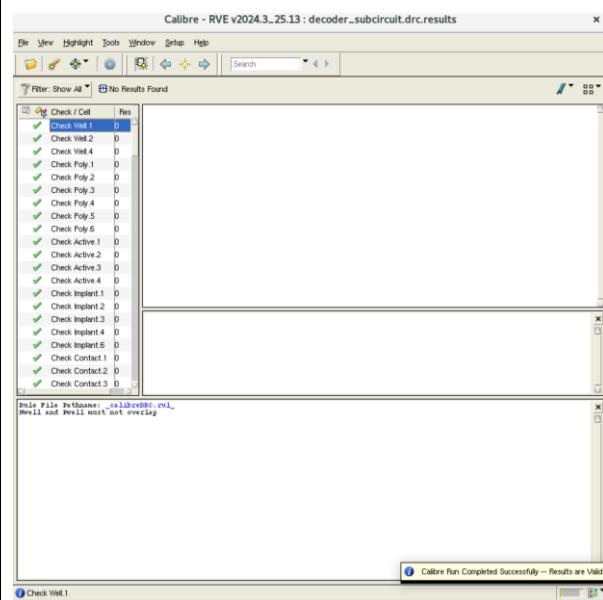
Run DRC

Show RVE

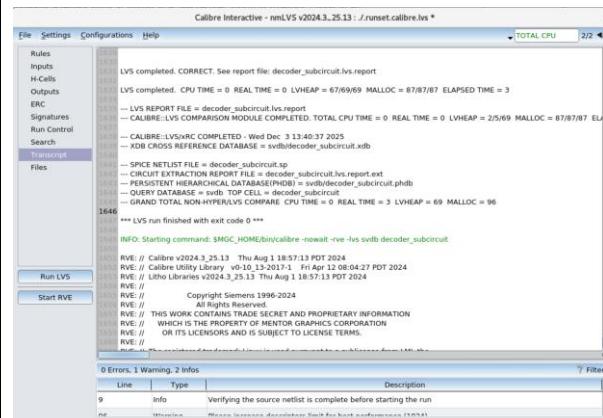
0 Errors, 1 Warning, 1 Info

Line	Type	Message
90	Warning	Please increase descriptors limit for best performance (1024)
4263	Info	Starting command: \$MGC_HOME/bin/calibre -nowait -rve -drc decoder_subcircuit.drc.results

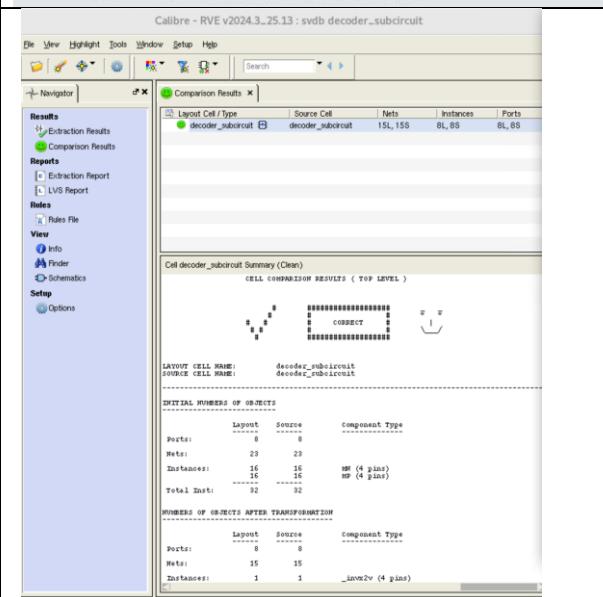
DRC Results



LVS Transcript



LVS Comparison Results



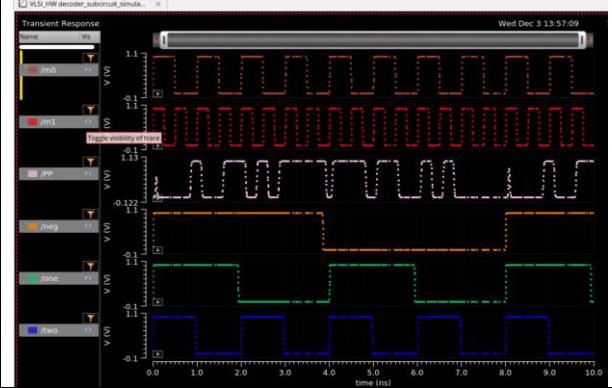
PEX Transcript

```
Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *
File Settings Configurations Help
Rules --- DOME REDUCING NETS...
Inputs --- WRITING TO PDN...
Outputs --- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 255/299 MALLOC = 263/263/263
LVS
Run Control
Search
Transcript
Files
PDB NET SUMMARY
pbdb file name = svrthDECODER.SUBCIRCUIT.pbdb
root cell name = DECODER_SUBCIRCUIT
total nets = 16
top-level nets = 16
non-top-level nets = 0
degenerated nets = 0
merged nets = 0
error nets = 0
CALIBRE xRC WARNING / ERROR Summary
xRC Warnings = 3
xRC Errors = 0
--- CALIBRE xRC: FORMATTER COMPLETED - Wed Dec 3 13:52:14 2025
--- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 157/299 MALLOC = 264/264/264 ELAPSED TIME = 2
2280
*** xRC run finished with exit code 0 ***
2280
0 Errors, 10 Warnings, 1 Info
Line Type Description
9 Info Verifying the source netlist is complete before starting the run
Run PEX Start RVE
```

PEX Netlist Output

```
Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *
File Settings Configurations Help
Rules 1 * File: decoder_subcircuit.pex.netlist
Inputs + Created: Wed Dec 3 13:52:14 2025
Outputs + Project: "Calibre"
LVS + Version: "v2024.3..25..13"
Run Control + include "decoder_subcircuit.pex.netlist.par"
Search + subcircuit decoder_subcircuit_1 H4_M0_TWG ONE_VSS VDD_PP NEG
Transcript + NEG NEG
Files + PP PP
+ VDD VDD
+ VSS VSS
+ ONE ONE
+ TWO TWO
+ MO MO
+ M1 M1
mxi1/MM3 X1/NET1 N HE_X1/MM3 g N VSS_X1/MM3 s N VGS_X1/MM3 b NMOS_VTL
+ L=5e-08 W=2e-07 Ad=5.15e-14 As=5.95e-14 Rd=9.15e-09 Ps=9.05e-07
mxi1/MM2 N NET2_X1/MM2 d N TWO_X1/MM2 g X1/NET1 N VSS_X1/MM3 b NMOS_VTL
+ L=5e-08 W=2e-07 Ad=5.15e-14 As=5.95e-14 Rd=9.15e-09 Ps=9.05e-07
mxi1/MM1 N NET3_X1/MM1 d N ONE_X1/MM1 g N VDD_X1/MM1 s N VOD_X1/MM1_b
+ PMOS_VTL L=5e-08 W=2e-07 Ad=5.15e-14 As=5.95e-14 Rd=9.15e-09 Ps=9.05e-07
mxi1/MM0 N NET2_X1/MM0 d N TWO_X1/MM0 g N VDD_X1/MM0 s N VOD_X1/MM0_b
+ PMOS_VTL L=5e-08 W=2e-07 Ad=5.15e-14 As=5.95e-14 Rd=9.15e-09 Ps=9.05e-07
mxi0/MM3 X0/NET1 N MO_X0/MM3 g N VSS_X0/MM3 s N VGS_X0/MM3 b NMOS_VTL
+ L=5e-08 W=2e-07 Ad=5.15e-14 As=5.95e-14 Rd=9.15e-09 Ps=9.05e-07
mxi0/MM2 N NET2_X0/MM2 d N ONE_X0/MM2 g X0/NET1 N VSS_X0/MM3 b NMOS_VTL
+ L=5e-08 W=2e-07 Ad=5.15e-14 As=5.95e-14 Rd=9.15e-09 Ps=9.05e-07
mxi0/MM1 N NET3_X0/MM1 d N NET2_X0/MM1 g N VDD_X0/MM1 s N VOD_X0/MM1_b
+ PMOS_VTL L=5e-08 W=2e-07 Ad=5.15e-14 As=5.95e-14 Rd=9.15e-09 Ps=9.05e-07
Run PEX Start RVE
```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```

/home/zeruv/simulation/decoder_subcircuit_simulation/hspiceD/sche... x
File Edit View Help cadence
***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 504 # elements = 1101
# resistors = 304 # capacitors = 697 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vccs = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 6
# curr_srcs = 0 # diodes = 0 # bjt = 0
# jfets = 0 # mosfets = 32 # u elements = 0
# p elements = 0 # n elements = 0 # n elements = 0
# s elements = 0 # p elements = 0 # v device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op point 0.01 1 38
transient 0.31 201 3027 1176 rev= 8
readout 0.01
errchk 0.01
setup 0.01
output 0.00

peak memory used 527.81 megabytes
total cpu time 0.35 seconds
total elapsed time 2.47 seconds
job started at 13:57:06 12/03/2025
job ended at 13:57:09 12/03/2025

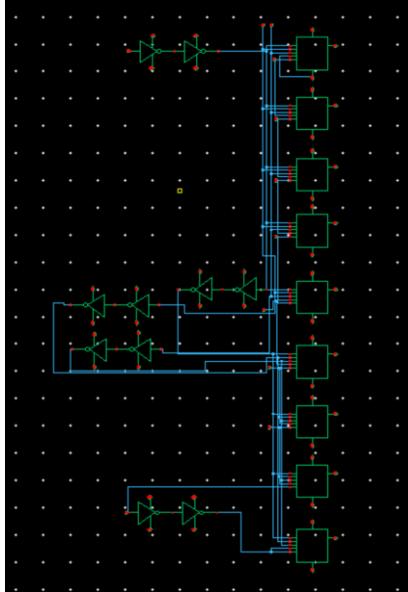
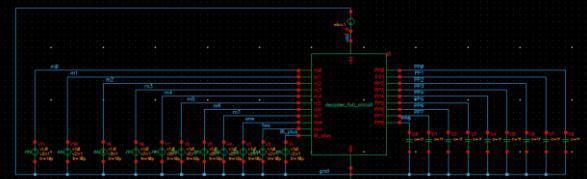
>info: ***** hspice job concluded
job total runtime 2.47 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.12(s)

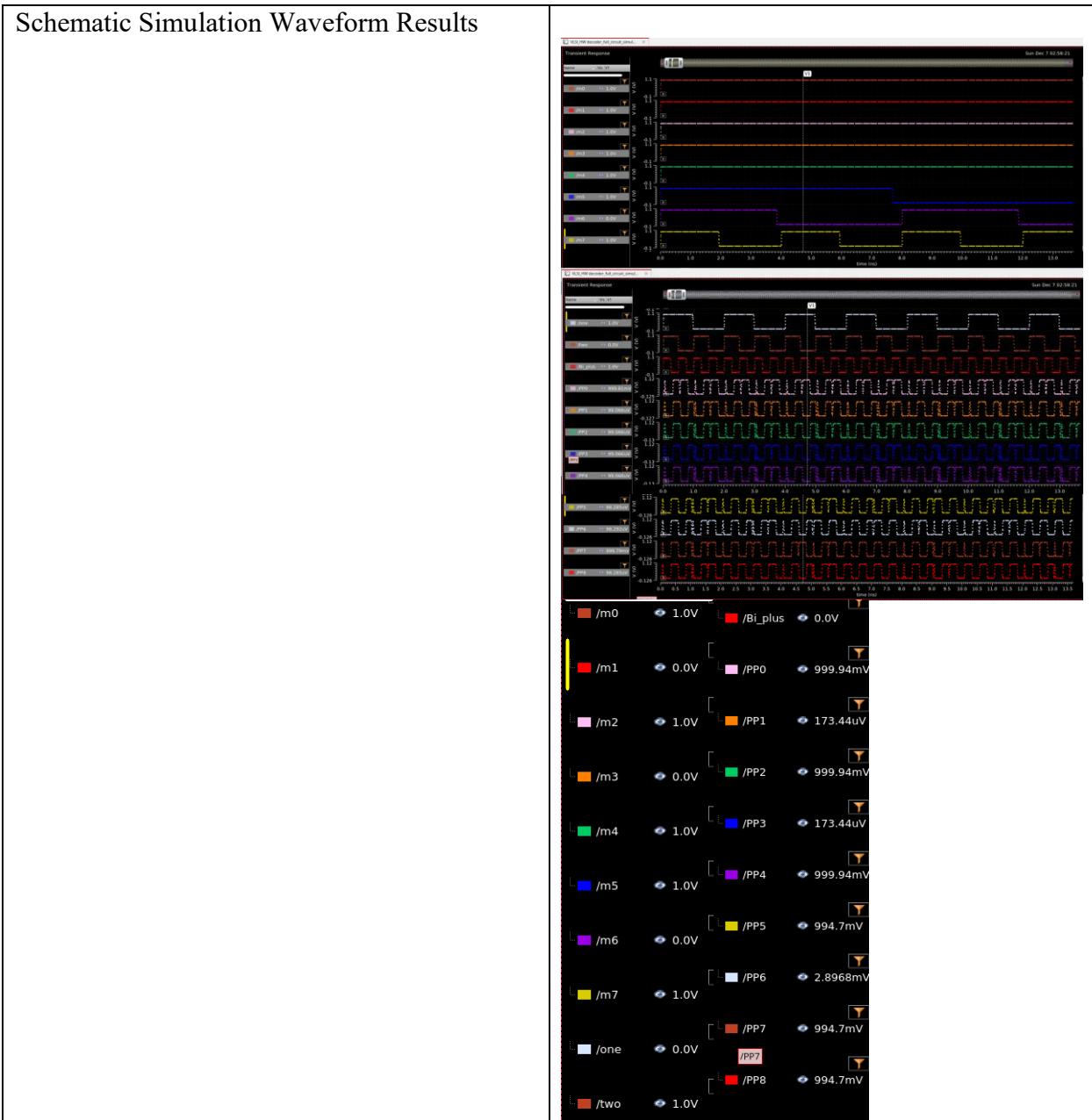
314 | Trace:/m1;Context:/home/zeruv/simulation/decoder_subcircuit_simulati | L720 C50

```

Table 9: Full Decoder Sub-Circuit (for Each Partial Product Generation)

Required Snapshot Description	Snapshot
Schematic (Design)	
Schematic Simulation Waveform Design	

Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/decoder_full_circuit_simulation/hspiceD/sch... ✘
File Edit View Help
cādence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 1399 # elements = 329
# resistors = 0 # capacitors = 9 # inductors = 0
# mosfets = 0 # cccs = 0 # vccs = 0
# cccs = 0 # cccs = 0 # volt_srcs = 12
# curr_srcs = 0 # diode = 0 # bjt = 0
# jfets = 0 # mosfets = 308 # U elements = 0
# triacs = 0 # wld_mosfets = 0 # B elements = 0
# S elements = 0 # elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

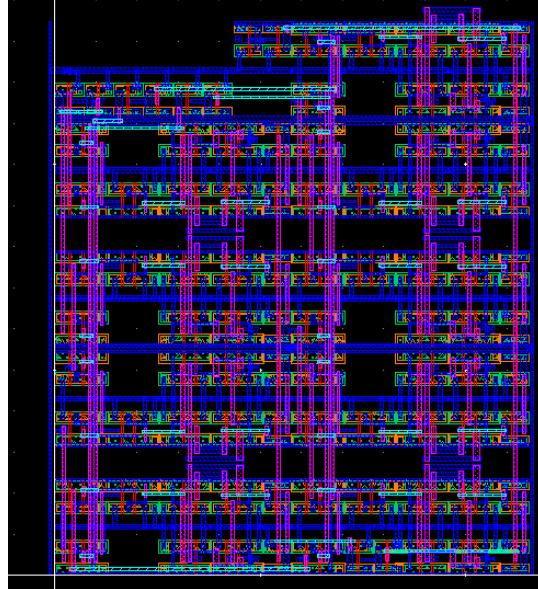
***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.ite
op point 0.01 1 13
transient 109.89 10241 318150 109001 rev= 1113
readin 0.01
errchk 0.03
setup 0.01
output 0.00

peak memory used 533.18 megabytes
total cpu time 109.97 seconds
total elapsed time 113.63 seconds
job started at 02:56:27 12/07/2025
job ended at 02:58:21 12/07/2025

>info: ***** hspice job concluded
>info: job total runtime 113.63 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 3.62(s)
```

Schematic Layout Design



DRC Transcript

```
Calibre Interactive - nmDRC v2024.3_25.13 : ./runset.calibre.drc ✘
File Settings Configurations Help
TOTAL CPU TIME 1/1

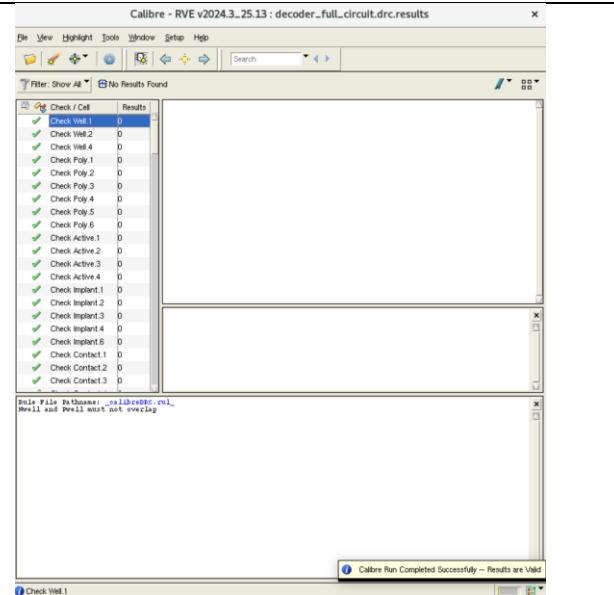
Policy
Inputs
Outputs
Run Control
Search
Transcript
4263
Files
-- CALIBRE-DRC EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
-- TOTAL RULECHECKS EXECUTED = 167
-- TOTAL CHECKS EXECUTED = 167
-- DRC RESULTS DATABASE FILE = decoder_full_circuit.drc.results (ASCII)
-- CALIBRE-DRC IS COMPLETED - Sun Dec 7 02:32:06 2025
-- TOTAL CPU TIME = 0 REAL TIME = 2
-- PROCESSOR COUNT = 1
-- SUMMARY REPORT FILE = decoder_full_circuit.drc.summary

*** DRC run finished with exit code 0 ***

INFO: Starting command: $MIG_HOME/bin/calibre -nowait -rve -drc decoder_full_circuit.drc.results
RVE: // Calibre v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0.12-2017-1 Fri Apr 12 04:27 PDT 2024
RVE: // Lulu Libraries v0.24.1-Sun Aug 1 18:57:13 PDT 2024
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RVE: // exclusive licensee of Linux Torvalds, owner of the mark on a world-wide basis.
RVE: //
RVE: // Mentor Graphics software executing under x86-64 Linux
RVE: //
RVE: // Running on 1 CPU
RVE: //
RVE: //
RVE: // Graphical User-Interface startup... Complete.
RVE: //

0 Errors, 1 Warning, 1 Info
Line Type Description
90 Warning Please increase descriptors limit for best performance (1024)
```

DRC Results



LVS Transcript

```
Calibre Interactive - nmLVS v2024.3..25.13 : ./unset.calibre.lvs +
File Settings Configurations Help TOTAL CPU: 2/2
Rules Inputs H-Cells Outputs ERC Signatures Run Control Search Transcript Files
LVS completed. CORRECT. See report file: decoder_full_circuit.lvs.report
LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 67/69/69 MALLOC = 90/90/90 ELAPSED TIME = 3
1694 -- CALIBRE-LVS COMPARISON MODULE COMPLETED TOTAL CPU: 2/2 REAL TIME = 0 REAL TIME = 0 LVHEAP = 2/5/69 MALLOC = 90/90/90 ELAPSED TIME = 3
-- CALIBRE-LVS/LVC COMPLETED - Sun Oct 7 11:49:20 2025
-- XDB CROSS REFERENCE DATABASE = svtb/decoder_full_circuit.xdb
-- SPICE NETLIST FILE = decoder_full_circuit.sp
-- CIRCUIT EXTRACTION REPORT FILE = decoder_full_circuit.lss.report_ext
-- PRESENTATION REPORT FILE = decoder_full_circuit.html
-- QUERY DATABASE = svtb/ TOP CELL = decoder_full_circuit
-- GRAND TOTAL NON-HYPERLVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP = 69 MALLOC = 98
*** LVS run finished with exit code 0 ***
INFO: Starting command: /MOC_HOME/bin/calibre -newest -rve -lvs svtb decoder_full_circuit
RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:33 PDT 2024
RVE: // Calibre Utility Library v0.10.13-2021.1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Utro Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
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RVE: // Mentor Graphics software executing under x86-64 Linux
0 Errors, 1 Warning, 2 Infos
Line Type Description
9 Info Verifying the source netlist is complete before starting the run
netlist
INFO: Starting command: /MOC_HOME/bin/calibre -newest -rve -lvs svtb decoder_full_circuit
```

LVS Comparison Results

The screenshot shows the Calibre interface with the title "Calibre - RVE v2024.3..25.13 : svtb decoder_full_circuit". The "Comparison Results" tab is active, showing a summary table for the "decoder_full_circuit" cell. Below the table, there are two detailed reports: "Cell decoder_full_circuit Summary (Clean)" and "Cell decoder_full_circuit Comparison Results (TOP LEVEL)". Both reports show initial and transformed object counts for Layout, Source, and Component types.

	Layout	Source	Component Type
Ports:	22	22	
Netz:	167	167	
Instances:	154	154	IN (4 pins)
Total Count:	388	388	

	Layout	Source	Component Type
Ports:	22	22	
Netz:	90	90	
Instances:	14	14	_inv2v (4 pins)

PEX Transcript

```
Calibre Interactive - PEX v2024.3.25.13 : ./runset.calibre.pex*
File Settings Configurations Help
Rules Inputs Outputs LVS Run Control Search Transcript Files
----- NETWORK REDUCTION BEGIN:
----- READING FROM PDB...
----- BEGIN REDUCING NETS...
----- DEDUPING OF NETS...
----- WRITING TO PDB...
----- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 256/299/299 MALLOC = 269/269/269
----- PDB NET SUMMARY -----
pbd file name = svrlb/DECODER_FULL_CIRCUIT.pdb
node cell name = DECODER_FULL_CIRCUIT
total nets = 167
top-level nets = 104
non-top-level nets = 0
degenerate nets = 63
merged nets = 0
error nets = 0

----- CALIBRE xRC WARNING / ERROR Summary -----
xRC Warnings = 3
xRC Errors = 0
----- CALIBRE xRC-FORMATTER COMPLETED - Sun Dec 7 11:51:20 2023
TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 1676/299 MALLOC = 270/270/270 ELAPSED TIME = 2
*** xRC run finished with exit code 0 ***
2348
```

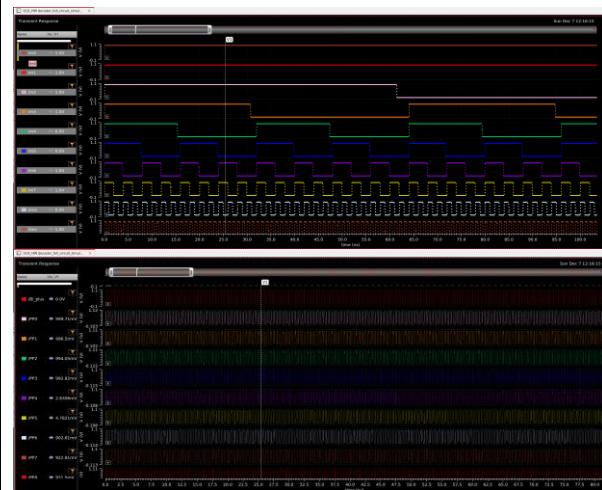
0 Errors, 10 Warnings, 1 Info

Line	Type	Description
9	Info	Verifying the source netlist is complete before starting the run

PEX Netlist Output

```
Calibre Interactive - PEX v2024.3.25.13 : ./runset.calibre.pex*
File Settings Configurations Help
decoder_full_circuit.pex.netlist
1 * file_decoder_full_circuit.pex.netlist
  * Created: Sun Dec 7 11:51:20 2023
  * Program: Calibre xRC
  * Version: "v2024.3_25_13"
  *
  include "decoder_full_circuit.pex.netlist.net"
  * subckt decoder_full_circuit M7 M5 M4 M6 ONE TWO M2 M0 M3 M1 VDD BI_PLUS PPS
  + PPS PPF VDD_VTL VSS_PP4 PP4_PP3 PP3_PP2 PP2_PP1 PPO
  *
  * PPG PPG
  * PP1 PP1
  * PP2 PP2
  * PP3 PP3
  * PP4 PP4
  * VSS VSS
  * VPP VPP
  * PP7 PP7
  * PP8 PP8
  * PP9 PP9
  * PP10 PP10
  * BI_PLUS BI_PLUS
  * VDD VDD
  * M1 M1
  * M2 M2
  * M3 M3
  * M4 M4
  * M5 M5
  * M6 M6
  * M7 M7
  *
  m010/MM1 N_NET65_X110/MM1_d N_NET74_X110/MM1_g N_VSS_X110/MM1_s
  + N_VDD_X110/MM1_b NMOS_VTL_L=5e-08 W=1e-07 AD=2.45e-14 AS=1.85e-14 PD=6.9e-07
  Ps=5.7e-07
  m010/MM2 N_NET65_X110/MM2_d N_NET74_X110/MM2_g N_VDD_X110/MM2_s
  + N_VSS_X110/MM2_b PMOS_VTL_L=5e-08 W=2e-07 AD=4.9e-14 AS=3.7e-14 PD=8.9e-07
  Ps=7.7e-07
  m010/MM1_N_NET74_X10/MM1_d N_M7_X10/MM1_g N_VSS_X10/MM1_s N_VSS_X10/MM1_s
  + N_VDD_X10/MM1_b NMOS_VTL_L=5e-08 W=1e-07 AD=2.45e-14 AS=1.85e-14 PD=6.9e-07
  Ps=5.7e-07
  m010/MM2_N_NET74_X10/MM2_d N_M7_X10/MM2_g N_VDD_X10/MM2_s N_VSS_X10/MM2_s
  + N_VSS_X10/MM2_b PMOS_VTL_L=5e-08 W=2e-07 AD=4.9e-14 AS=3.7e-14 PD=8.9e-07
  Ps=7.7e-07
Run Finished
```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```

/home/zeruv/simulation/decoder_full_circuit_simulation/hspiceD/sch... x
File Edit View Help                                         cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 4935 # elements = 12168
# resistors = 366 # capacitors = 818 # inductors = 0
# mosfet_ldns = 0 # vcap_ldns = 0 # vcvd = 0
# cccs = 0 # cvcs = 0 # volc_srcs = 12
# curr_srcs = 0 # diodes = 0 # bjts = 0
# jfets = 0 # mosfets = 308 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# O elements = 0 # N elements = 0 # VA device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.ITER
op point 0.16 1 72
transient 309.81 10241 280872 97045 rev= 524
readin 0.09
errchk 0.05
setup 0.37
output 0.00

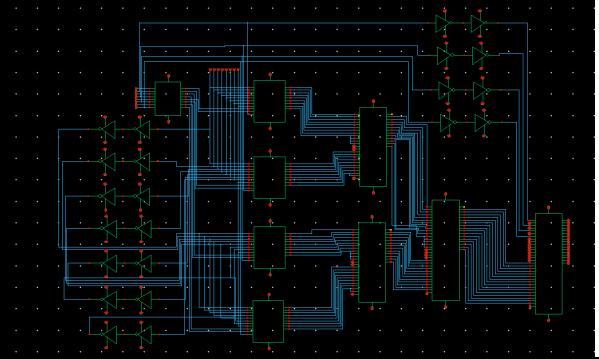
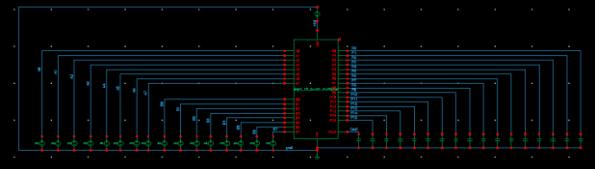
peak memory used 563.65 megabytes
total cpu time 310.22 seconds
total elapsed time 312.22 seconds
job started at 12:11:03 12/07/2025
job ended at 12:16:15 12/07/2025

>info: ***** hspice job concluded
lic: total license checkout elapse time: 1.99(s)
lic: Release hspice token(s)

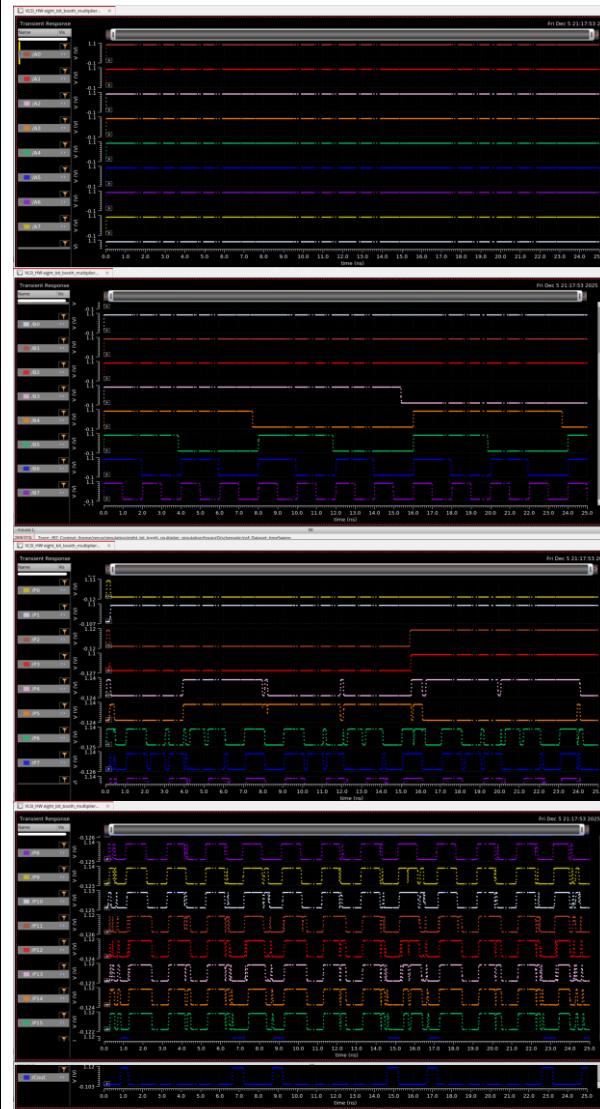
461 |                                         L1,016 C57

```

Table 10: 8-Bit Booth Multiplier

Required Snapshot Description	Snapshot
Schematic (Design)	
Schematic Simulation Waveform Design	

Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/eight_bit_booth_multiplier_simulation/hspice... x
File Edit View Help
cādence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 18412 # elements = 4134
# resistors = 0 # capacitors = 7 # inductors = 0
# mosfets = 0 # vccs = 0 # vctrs = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 17
# curr_srcs = 0 # diode = 0 # btrs = 0
# jfets = 0 # mosfets = 4100 # U elements = 0
# triacs = 0 # wsrcs = 0 # B elements = 0
# S elements = 0 # elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

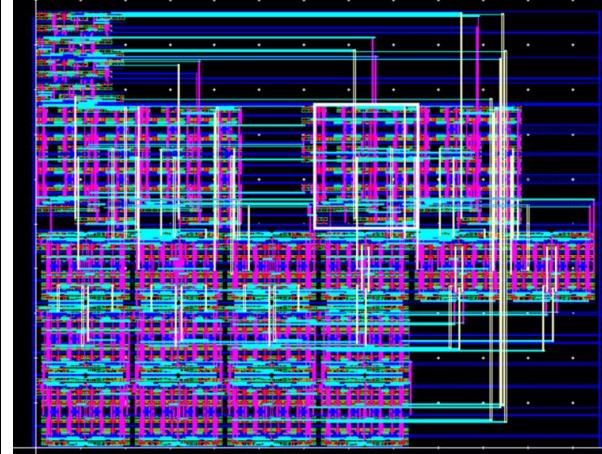
***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op point 0.11 1 13
transient 47.36 501 19991 6636 rev= 47
readin 0.01
errchk 0.07
setup 0.14
output 0.00

peak memory used 590.96 megabytes
total cpu time 47.70 seconds
total elapsed time 49.88 seconds
job started at 21:17:03 12/05/2025
job ended at 21:17:53 12/05/2025

>info: ***** hspice job concluded
job total runtime 49.88 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.18(s)
```

Schematic Layout Design



DRC Transcript

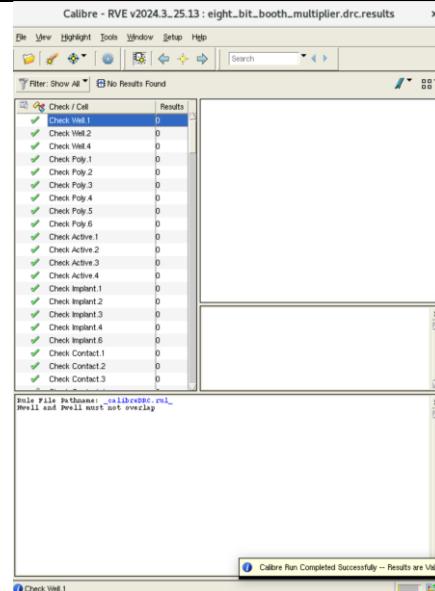
```
Calibre Interactive - nmDRC v2024.3, 25.13 : ./unset.calibre.drc *
File Settings Configurations Help
TOTAL CPU: 1/2 <=
Rules
Inputs
Outputs
Run Control
Search
Transcript
4287
Files
-- CALIBRE-DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
-- TOTAL RULE CHECKS EXECUTED = 167
-- TOTAL RULES VIOLATED = 0
-- DRC RESULTS DATABASE FILE = eight_bit_booth_multiplier.drc.results (ASCII)
-- CALIBRE-DRC-H COMPLETED - Mon Dec 6 22:30:59 2025
-- 2027/2025 TIME = 0 REAL TIME = 2
-- PROCESSOR COUNT = 1
-- SUMMARY REPORT FILE = eight_bit_booth_multiplier.drc.summary

*** DRC run finished with exit code 0 ***

INFO: Starting command: $MIG_HOME/bin/calibre -nowait -rve -drc eight_bit_booth_multiplier.drc.results
RVE: // Calibre v2024.3, 25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library - v0.10.13-2017.1 Fri Apr 12 08:42:27 PDT 2024
RVE: // LIO: Libraries - v0.10.13-2017.1 Fri Aug 1 18:57:13 PDT 2024
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RVE: // exclusive licensee of Linux Torvalds, owner of the mark on a world-wide basis.
RVE: // Mentor Graphics software executing under x86-64 Linux
RVE: //
RVE: // Running on 1 CPU
RVE: //
RVE: // Graphical User-Interface starts... Complete.
RVE: //

0 Errors, 1 Warning, 1 Info
Line Type Description
90 Warning Please increase descriptors limit for best performance (1024)
www.info Please increase descriptors limit for best performance (1024)
```

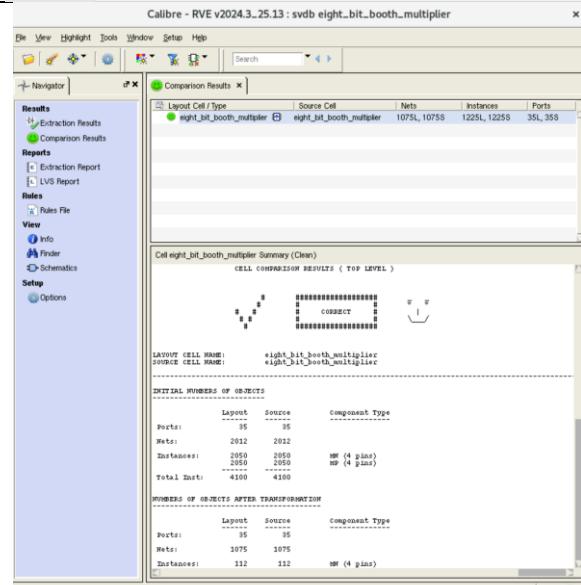
DRC Results



LVS Transcript

```
Calibre Interactive - nmLVS v2024.3.25.13 : ./runset.calibre.lvs *
File Settings Configurations Help TOTAL CPU 2/2
Rules Inputs H-Cells Outputs ERC Signatures Run Control Search Transcript Files
LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 68/91/91 MALLOC = 111/111/111 ELAPSED TIME = 2
2092 -- CALIBRE:LVS COMPARISON MODULE COMPLETED TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 2/27/91 MALLOC = 11
-- XDB CROSS REFERENCE DATABASE = svdb/eight_bit_booth_multiplier.xdb
-- SPICE NETLIST FILE = eight_bit_booth_multiplier.sp
-- CIRCUIT EXTRACTION REPORT FILE = eight_bit_booth_multiplier.lvs.report.ext
-- PERIODICITY CHECK REPORT FILE = svdb/eight_bit_booth_multiplier.phdb
-- QUERY DATABASE = svdb/TOP CELL = eight_bit_booth_multiplier
-- GRAND TOTAL NON-HYPERLVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP = 91 MALLOC = 119
*** LVS run finished with exit code 0 ***
INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -lvs svlb eight_bit_booth_multiplier
RVE: // Calibre v2024.3.25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0-10_13-2017-1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries v2024.3.25.13 Thu Aug 1 18:57:13 PDT 2024
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RVE: //
Run LVS Start RVE
0 Errors, 1 Warning, 2 Infos
Line Type Description
9 Info Verifying the source netlist is complete before starting the run
96 Warning Please increase descriptors limit for best performance (1024)
2105 Info Starting command: $MGC_HOME/bin/calibre -nowait -rve -lvs svlb eight_bit_booth_multiplier
```

LVS Comparison Results



PEX Transcript

```
Calibre Interactive - PEX-v2024.3_25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
----- PDB NET SUMMARY -----
pdbs file name = svb1EIGHT_BIT_BOOTH_MULTIPLIER.pdb
root cell name = EIGHT_BIT_BOOTH_MULTIPLIER
total nets = 2012
top-level nets = 1164
non-top-level nets = 0
degenerate nets = 848
merged nets = 0
error nets = 0

===== CALIBRE xRC WARNING / ERROR Summary =====
xRC Warnings = 3
xRC Errors = 0

===== CALIBRE xRC FORMATTER COMPLETED - Fri Dec 12 10:56:20 2023 =====
TOTAL CPU TIME = 0 REAL TIME = 1 LVHEAP = 16/78/301 MALLOC = 322/322/322 ELAPSED TIME = 4

*** xRC run finished with exit code 0 ***
2810
```

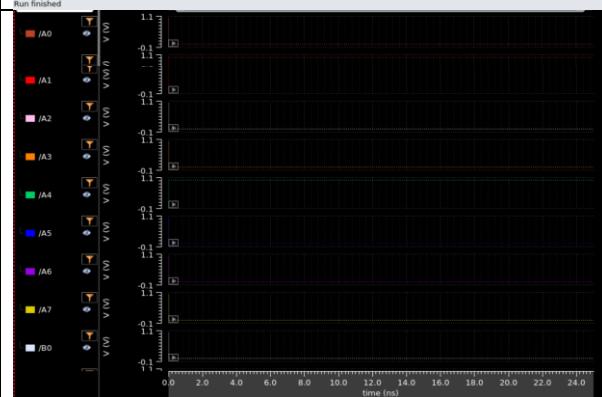
0 Errors, 10 Warnings, 1 Info

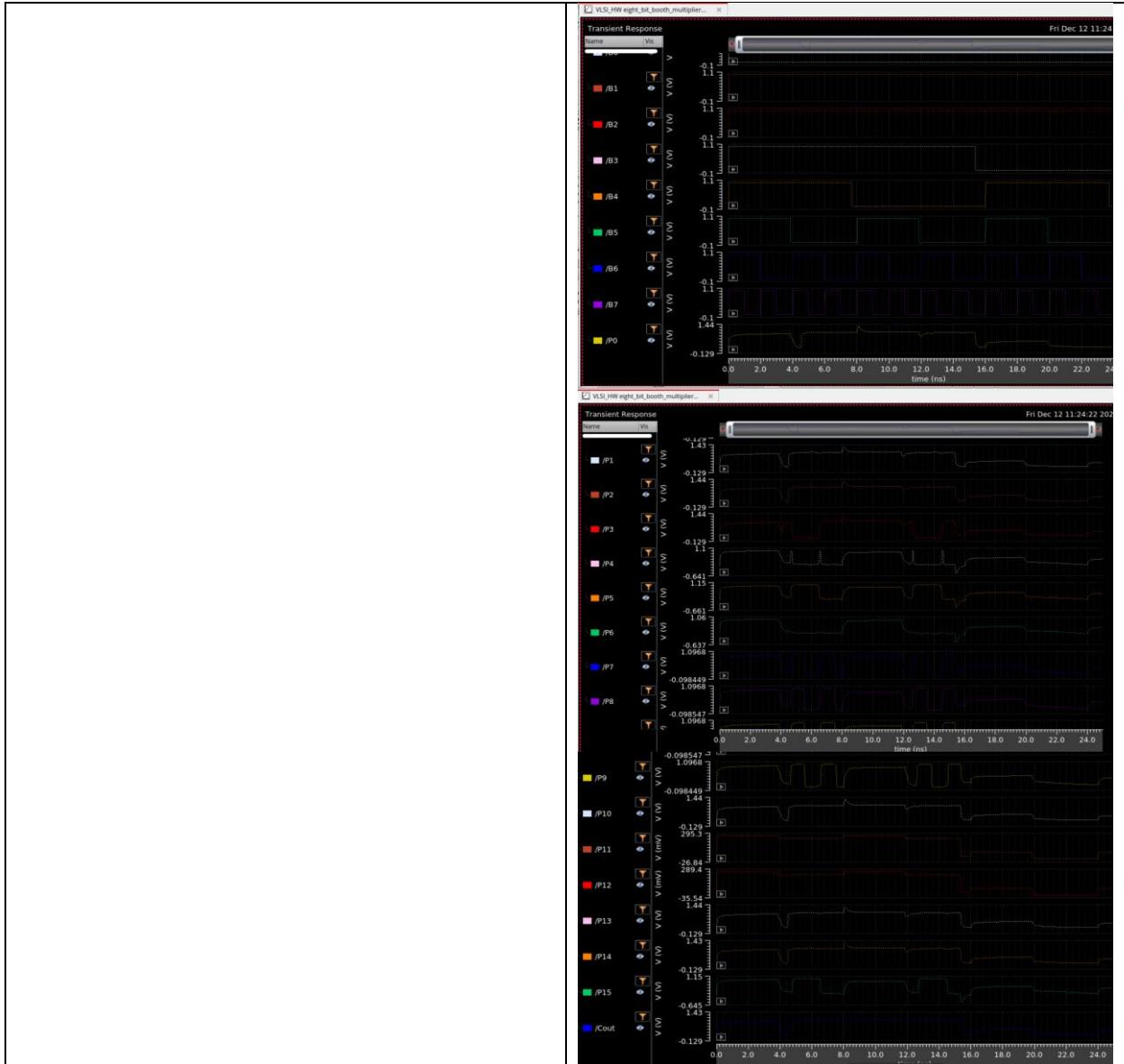
Line	Type	Description
9	Info	Verifying the source netlist is complete before starting the run
96	Warning	Please increase descriptors limit for best performance (1024)
127	Warning	PEX RESISTANCE LUMPED is obsolete. Please remove from your ruledeck.
255	Warning	PEX RESISTANCE LUMPED is obsolete. Please remove from your ruledeck.
2228	Warning	Please increase descriptors limit for best performance (1024)

PEX Netlist Output

```
Calibre Interactive - PEX-v2024.3_25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
----- eight_bit_booth_multiplier.netlist -----
1 * File: eight_bit_booth_multiplier.pex.netlist
* Created: Fri Dec 12 10:56:18 2023
* Program: "Calibre xRC"
* Version: "v2024_3_25.13"
*
* include "eight_bit_booth_multiplier.pex.netlist.pex"
* subckt eight_bit_booth_multiplier B3 B7 B5 B1 A1 A6 A3 A5 A4 A2 A0 VDD COUT
*   + VSS B4 B0 P15 P14 P12 P13 B6 B2 P10 P11 P9 P6 P7 P5 P4 P2 P3 P1 P0 A7
*
*   + A7
*   + P0
*   + P1
*   + P3
*   + P5
*   + P4
*   + P5
*   + P7
*   + P6
*   + P9
*   + P8
*   + P10
*   + B2
*   + B6
*   + P12
*   + P14
*   + P15
*   + B0
*   + B4
*   + VSS
*   + VDD
*   + COUT
*   + VDD
*   + A0
*   + A2
*   + A4
*   + A5
*   + A3
*   + A6
*   + A1
*   + B1
Run finished
```

Post-Layout Simulation Results





Post-Layout Simulation Out Log

```

/home/zeruv/simulation/eight_bit_booth_multiplier_simulation/hspic... x
File Edit View Help                                         cādence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count :      1
Available CPU Count :           2
Actual Threads Count :          1

***** Circuit Statistics *****
# nodes      = 65390 # elements = 177671
# resistors  = 48463 # capacitors = 125091 # inductors =      0
# meermal_lnds =      0 # vccs      =      0 # vccs      =      0
# cccs       =      0 # ccvs      =      0 # volt_srcs =      17
# curr_srcs  =      0 # diodes     =      0 # bjt_srcs =      0
# jfets       =      0 # mosfets    = 4106 # U elements =      0
# T elements =      0 # W elements =      0 # B elements =      0
# S elements =      0 # P elements =      0 # VA device =      0
# vector_srcs =      0 # N elements =      0

***** Runtime Statistics (seconds) *****
analysis      time   # points tot. iter conv. iter
op point     4.02        1      149
transient    88.69      501      5860      1950 rev= 5
readin       1.59
readch       0.97
setup        1.53
output       0.00

peak memory used      977.07 megabytes
total cpu time        96.98 seconds
total elapsed time    98.86 seconds
job started at        11:22:43 12/12/2025
job ended at          11:24:22 12/12/2025

>info:      ***** hspice job concluded
job total runtime     98.86 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time:      1.88(s)

967 | Trace: /A7, Context: /home/zeruv/simulation/eight_bit_booth_multiplier_si | L4,186 C17

```

Appendix

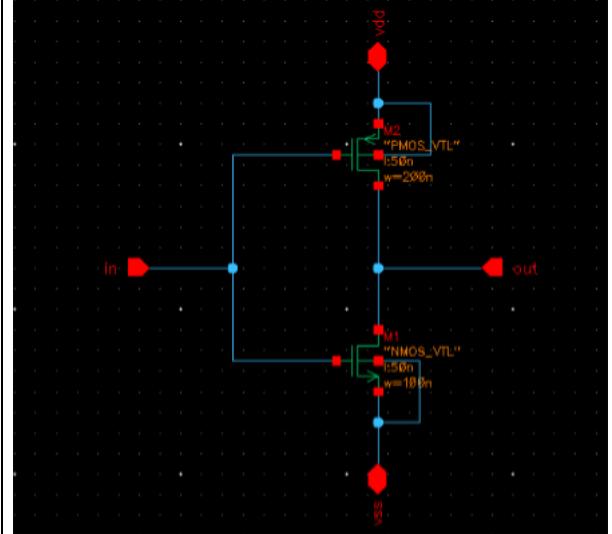
This section showcases circuit designs from previous assignments that have been used in the designs shown above. It acts as the library of components that this assignment uses that were used internally for the full booth multiplier design. These components are the following, and will be showcased in tables below:

- Inv (Inverter)
- NAND
- NOR
- And
- Passgate
- Mux
- Half Adder (which acts as an XOR gate when the Cout bit is ignored)

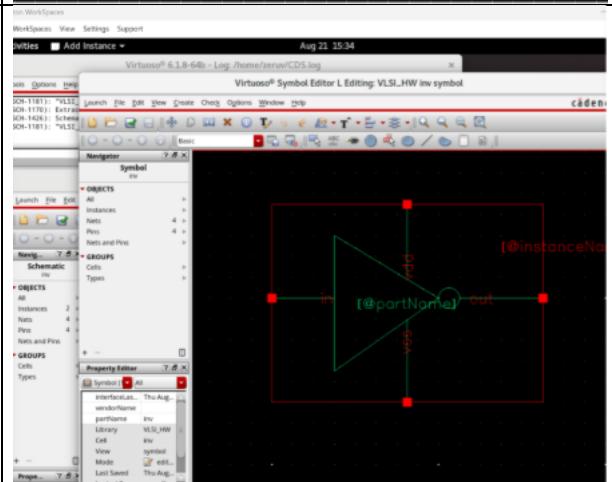
Inverter

Required Snapshot Description	Snapshot
-------------------------------	----------

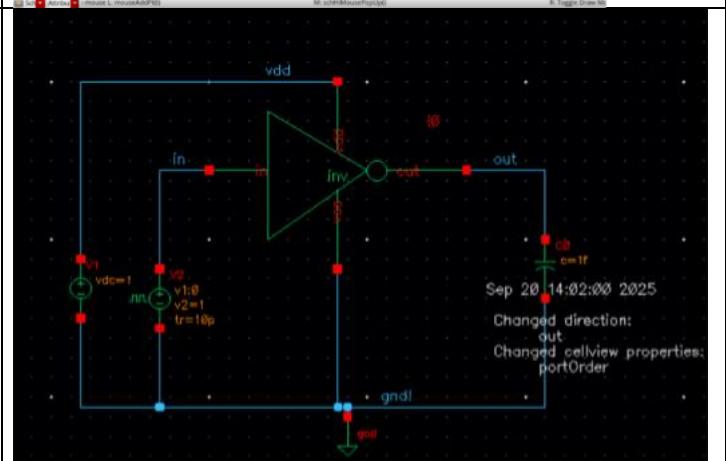
Schematic (Design)



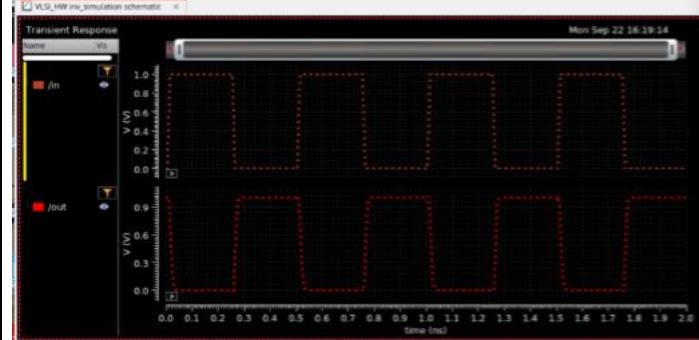
Schematic Symbol Design (Optional)



Schematic Simulation Waveform Design



Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```

***** Circuit Statistics *****
# nodes      =      12 # elements      =      5
# resistors   =      0 # capacitors    =      1 # inductors   =      0
# mutual_inds =      0 # vccs          =      0 # vcvs         =      0
# cccs        =      0 # ccvs          =      0 # volt_srcs   =      2
# curr_srcs   =      0 # diodes         =      0 # bjts          =      0
# jfets        =      0 # mosfets        =      2 # U elements  =      0
# T elements   =      0 # W elements     =      0 # B elements  =      0
# S elements   =      0 # P elements     =      0 # va device    =      0
# vector_srcs =      0 # N elements     =      0

***** Runtime Statistics (seconds) *****
analysis      time      # points      tot. iter      conv. iter
op point     0.00           1            4
transient    0.00          41           428       177 rev=  E
readin       0.00
errchk       0.01
setup        0.00
output       0.00

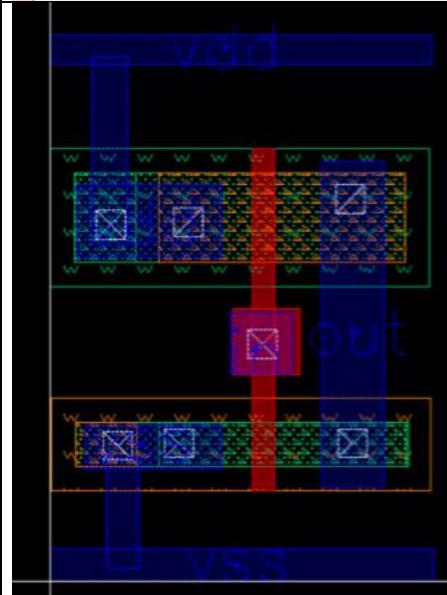
peak memory used      527.80 megabytes
total cpu time        0.02 seconds
total elapsed time    1.93 seconds
job started at        15:42:08 09/22/2025
job ended at          15:42:10 09/22/2025

>info:      ***** hspice job concluded
                job total runtime      1.93 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time:      1.91(s)

```

Schematic Layout Design



DRC Transcript

```
Calibre Interactive - nmDRC v2024.3_25.13 : ./runset.calibre.drc *
File Settings Configurations Help Search 1/3 < >
Rules 4057 Cumulative CONNECT Time: CPU = 0 REAL = 0
Inputs Cumulative RDB Time: CPU = 0 REAL = 0
Outputs
Run Control
Search
DRC-H
Files
--- CALIBRE-DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
--- TOTAL RULECHECKS EXECUTED = 167
--- TOTAL RESULTS GENERATED = 0 (0)
--- DRC RESULTS DATABASE FILE = inv.drc.results (ASCII)

--- CALIBRE-DRC-H COMPLETED - Fri Sep 5 21:02:58 2025
--- TOTAL CPU TIME = 0 REAL TIME = 2
--- PROCESSOR COUNT = 1
--- SUMMARY REPORT FILE = inv.drc.summary

*** DRC run finished with exit code 0 ***

INFO: Starting command: $MGIC_HOME/bin/calibre-newait -rve -drc inv.drc.results
RVE: // Calibre v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0-10_13-2017-1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: //
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RVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
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RVE: //
RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI; the
RVE: // executive licenses of Linux trademarks, names of the mark or a similar basis.

Run DRC
Show RVE
0 Errors, 1 Warning, 1 Info
DRC Run Completed Successfully -- Results are Valid Filter
Line Type Description
90 Warning Please increase descriptors limit for best performance (1024)
4073 Info Starting command: $MGIC_HOME/bin/calibre-newait -rve -drc in...
```

DRC Results

Calibre - RVE v2024.3_25.13 : inv.drc.results

File View Highlight Tools Window Setup Help

Filter Show All No Results Found

Check / Cell	Results
✓ Check Grid 17	0
✓ Check Grid 18	0
✓ Check Grid 19	0
✓ Check Grid 20	0
✓ Check Grid 21	0
✓ Check Grid 22	0
✓ Check Grid 23	0
✓ Check Grid 24	0
✓ Check Grid 25	0
✓ Check Grid 26	0
✓ Check Antenna poly	0
✓ Check Antenna metall	0
✓ Check Antenna metall2	0
✓ Check Antenna metall3	0
✓ Check Antenna metall4	0
✓ Check Antenna metall5	0
✓ Check Antenna metall6	0
✓ Check Antenna metall7	0
✓ Check Antenna metall8	0
✓ Check Antenna metall9	0
✓ Check Antenna metall0	0

RESULTS FROM PATTERN: CALIBRE-MIGRATION
Results and overall ruleset not overlapping

More Run Completed Successfully -- Results are Valid

Check Wk1

LVS Transcript

Calibre Interactive - nmLVS v2024.3_25.13 : ./runset.calibre.lvs *

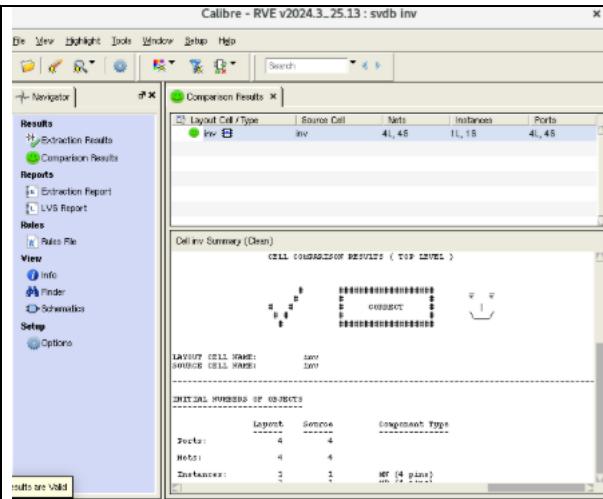
File Settings Configurations Help TOTAL CPU TIME: 20

Rules LVS completed. CORRECT. See report file: inv.lvs.report
Inputs LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 8657957 MALLOC = 90/90/90 ELAPSED TIME = 3
H-Cells
Outputs
ERC
Signatures
Run Control
Search
Transcript
1581 --- LVS REPORT FILE = inv.lvs.report
--- PLACEMENT LIBRARY: AIA:14M000A (PL00) = wabifine.phdb
--- QUERY DATABASE = SVS: TOP CELL = ITV
--- CHANNEL ID: 14A:14M000A(LVS) COMM: C00000 = 0.0000E+000.0000E+000.0000E+000
--- LVS run finished with exit code 0 ***

INFO: Starting command: \$MGIC_HOME/bin/calibre-newait -rve -lvs inv.lvs
RVE: // Calibre v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0-10_13-2017-1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: //
RVE: Copyright Siemens 1996-2024
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RVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
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0 Errors, 1 Warning, 2 Infos
Calibre Run Completed Successfully -- Results are Valid Filter

LVS Comparision Results



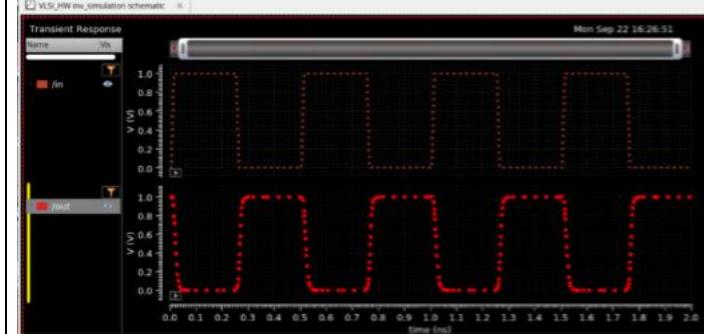
PEX Transcript

```
Calibre Interactive - PEX v2024.3_25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
----- PROCESSING PARASITIC MODELS -----
----- OUTPUT PARASITIC MODEL INSTANCE FILE NAME inv.pex.netlist.INV.pxi
----- NETWORK REDUCTION BEGIN: -----
----- READING FROM PDB...
----- BEGIN REDUCING NETS...
----- DONE REDUCING NETS...
----- WRITING TO PDB...
----- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 255/299/299 MALLOC = 0/0/0
----- PDB NET SUMMARY -----
----- File name = svdbINV.pdb
----- net cell name = INV
----- total nets = 4
----- top-level nets = 4
----- non top-level nets = 0
----- degenerate nets = 0
----- merged nets = 0
----- error nets = 0
----- CALIBRE xRC WARNING / ERROR Summary -----
----- xRC Warnings = 3
----- xRC Errors = 0
----- CALIBRE xRC: FORMATTER COMPLETED - Fri Sep 5 21:22:15 2025
----- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 15/76/299 MALLOC = 239/239/273 ELAPSED TIME = 00:00:00.000
----- WARNING: No ground net name defined in PEX NETLIST statement and "0" will be used in the netlist
*** xRC run finished with exit code 0 ***
2201
```

PEX Netlist Output

```
Calibre Interactive - PEX v2024.3_25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
inv.pex.netlist *
1. * File: inv.pex.netlist
2. * Created: Fri Sep 5 21:22:14 2025
3. * Program "Calibre xRC"
4. * Version "v2024.3_25.13"
5. *
6. include "inv.pex.netlist.pex"
7. subckt inv VDD VSS IN OUT
8. *
9. * OUT
10. * IN
11. * VSS
12. * VDD
13. VDD
MM1 N_OUT MM1_d N_IN_MM1_g N_VSS_MM1_s N_VSS_MM1_b NMOS_VTL L=5e-011 W=1e-07
+ AD=-3e-14 AS=-2.1e-14 PD=-8e-07 PS=6.2e-07
MM2 N_OUT MM2_d N_IN_MM2_g N_VDD_MM2_s N_VDD_MM2_b PMOS_VTL L=5e-08 W=2e-07
+ AD=5.95e-14 AS=4.25e-14 PD=9.95e-07 PS=8.25e-07
*
15. include "inv.pex.netlist.INV.pxi"
16. *
17. ends
18. *
```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```
/home/zeruv/simulation/inv_simulation/hspiceD/schematic/psf/hspic... x
File Edit View Help cādence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 30 # elements = 52
# resistors = 18 # capacitors = 30 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vccs = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 2
# curr_srcs = 0 # diodes = 0 # bjts = 0
# jfets = 0 # mosfets = 2 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op point 0.00 1 8
transient 0.00 41 363 152 rev= 1
readin 0.00
errchk 0.00
setup 0.00
output 0.00

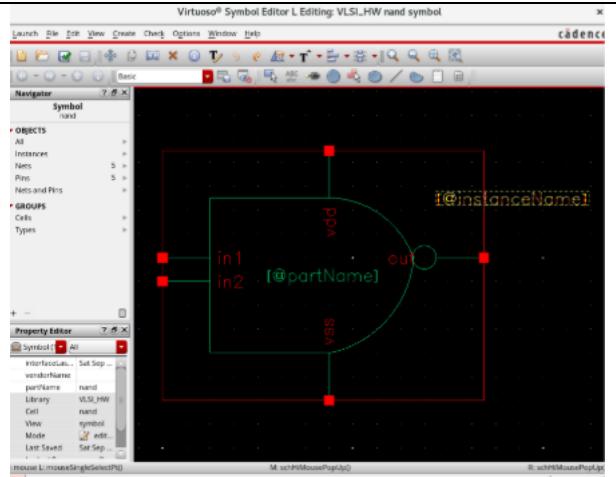
peak memory used 527.80 megabytes
total cpu time 0.02 seconds
total elapsed time 1.75 seconds
job started at 16:26:50 09/22/2025
job ended at 16:26:51 09/22/2025

>info: ***** hspice job concluded
in total runtime 1.75 seconds
```

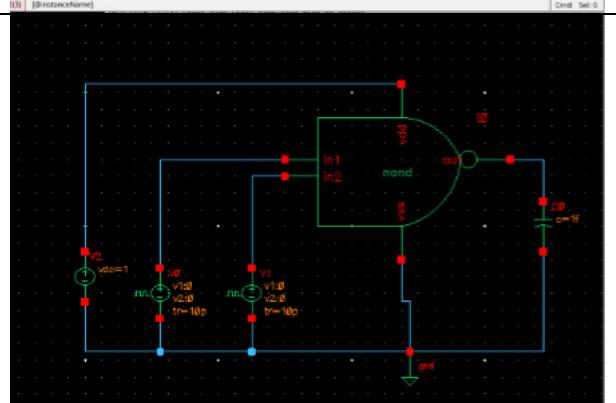
NAND

Required Snapshot Description	Snapshot
Schematic (Design)	

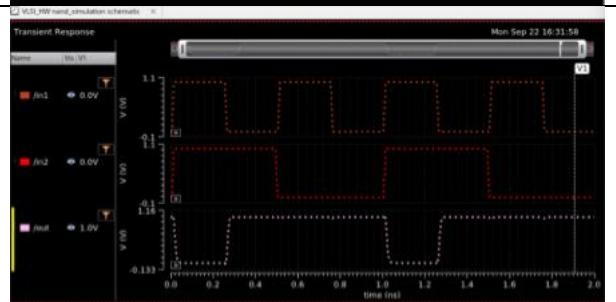
Schematic Symbol Design (Optional)



Schematic Simulation Waveform Design



Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/nand_simulation/hspiceD/schematic/psf/hspi_< x
File Edit View Help                                         Cadence

***** Circuit Statistics *****
# nodes      = 22 # elements      =     8
# resistors  = 0 # capacitors   = 1 # inductors  =     0
# mutual_inds = 0 # vccs        = 0 # vccs       =     0
# curr_smps  = 0 # vccs        = 0 # vccs       =     0
# curr_srcs  = 0 # diodes       = 0 # bjt_srcs    =     3
# jfets       = 0 # mosfets      = 4 # U-elements =     0
# T_elements = 0 # W-elements   = 0 # B-elements =     0
# S_ELEMENTS = 0 # P-elements   = 0 # VA-device   =     0
# vector_srcs = 0 # N-elements   = 0

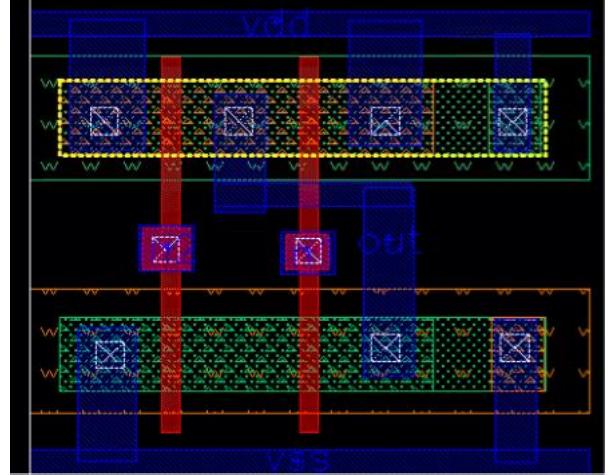
***** Runtime Statistics (seconds) *****
analysis      time  # points tot. iter conv.riter
op point     0.00      1          6
transient    0.01     41        457      182 revs
readin       0.00
errchk       0.00
setup        0.00
output       0.00

peak memory used      527.80 megabytes
total cpu time        0.02 seconds
total elapsed time    2.03 seconds
job started at        16:31:56 09/22/2025
job ended at          16:31:58 09/22/2025

>info:      ***** hspice job concluded
            job total runtime      2.03 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.01(s)
```

Schematic Layout Design



DRC Transcript

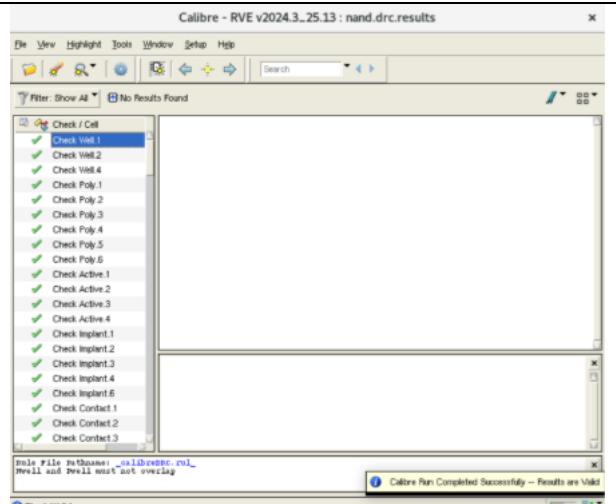
```
Calibre Interactive - nmDRC v2024.3.25.13 : ./runset.calibre.drc >
File Settings Configurations Help                                         TOTAL 15/15
Rules --- TOTAL RESULTS GENERATED = 0 (0)
Inputs --- DRC RESULTS DATABASE FILE = nand.drc.results (ASCII)
Outputs --- CALIBRE-DRC-H COMPLETED - Sat Sep 6 18:00:55 2025
Run Control --- TOTAL CPU TIME = 0 REAL TIME = 2
Search --- PROCESSOR COUNT = 1
Files --- SUMMARY REPORT FILE = nand.drc.summary

*** DRC run finished with exit code 0 ***

INFO: Starting command: $MOC_HOME/bin/calibre -nowait -v -drc nand.drc.results
RVE: // Calibre v2024.3.25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0.10.13-2017.1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries V2024.3.25.13 Thu Aug 1 18:57:13 PDT 2024
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RVE: //
RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI,
RVE: // the exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
RVE: //
RVE: // Mentor Graphics software executing under x86-64 Linux
RVE: //
RVE: // Running on 1 CPU
RVE: //
RVE: // Graphical User-Interface startup.... Complete.
RVE: //
RVE: // Calibregrbl license acquired.
RVE: // RVE authorized.

0 Errors, 1 Warning, 1 Info
Line | Type | Description
90  Warning | Please increase descriptors limit for best performance (1024)
ANT3  Info | Etching command: $MOC_HOME/bin/etches_nosplit_nrm_drc.nod.drc
```

DRC Results

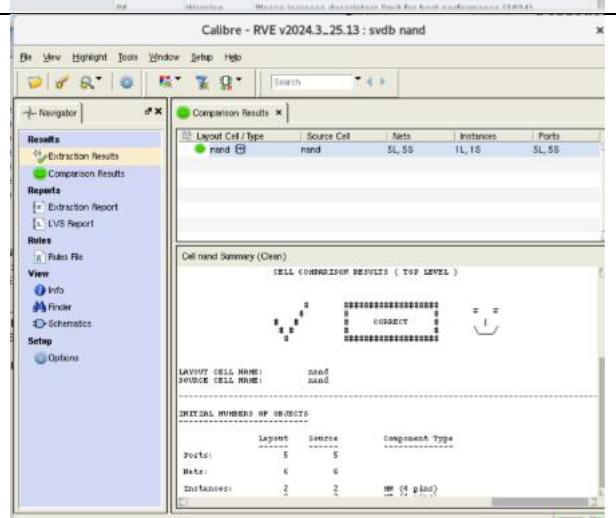


LVS Transcript

```

Calibre Interactive - nmLVS v2024.3_25.13 : ./runset.calibre.lvs *
File Settings Configurations Help TOTAL CPU TIME 2/2
Rules --- LVS REPORT FILE = nand.lvs.report
Inputs --- CALIBRE:LVS/XRC COMPLETED - Sat Sep 6 18:43:33 2025
H-Cells --- XDB CROSS REFERENCE DATABASE = svdb/nand.xdb
Outputs --- SPICE NETLIST FILE = nand.sp
ERC --- CIRCUIT EXTRACTION REPORT FILE = nand.lvs.report.ext
Signatures --- PERSISTENT HIERARCHICAL DATABASE(PHOB) = svdb/nand.phb
Run Control --- QUERY DATABASE = svdb/TOP CELL = nand
Search --- GRAND TOTAL NON-HYPER/LVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP = 67 MALLOC
Transcript *** LVS run finished with exit code 0 ***
Files
Run LVS
Show RVE
INFO: Starting command: $MGC_HOME/bin/calibre -newall -lvs svdb nand
RVE: // Calibre v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0-10_13-2017-1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
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RVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
RVE: //
RVE: // Mentor Graphics software executing under x86-64 Linux
0 Errors, 1 Warning, 2 Infos
Line Type Description
9 Info Verifying the source netlist is complete before starting the run
1st instance: MIGRATION: MIGRATION: detected back-to-back connections (100%)
```

LVS Comparision Results



PEX Transcript

```

Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript
----- PDB NET SUMMARY -----
2181 pdfb file name = svlib/NAND.pdfb
2182 root cell name = NAND
2183 total nets = 6
2184 top-level nets = 5
2185 non-top-level nets = 0
2186 degenerate nets = 1
2187 merged nets = 0
2188 error nets = 0
2189
2190
2191 ----- CALIBRE xRC WARNING / ERROR Summary -----
2192 xRC Warnings = 3
2193 xRC Errors = 0
2194
2195
2196 ----- CALIBRE xRC:FORMATTER COMPLETED - Sat Sep. 6 18:46:05 2025 -----
2197 --- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 15/76/299 MALLOC = 236/236/265 ELAPSED TIME = 00:00:00
2198
2199 *** xRC run finished with exit code 0 ***
2200
2201
2202 0 Errors, 10 Warnings, 1 Info
2203 Line Type Description
2204 8 info Verifying the source netlist is complete before starting the run
2205
2206

```

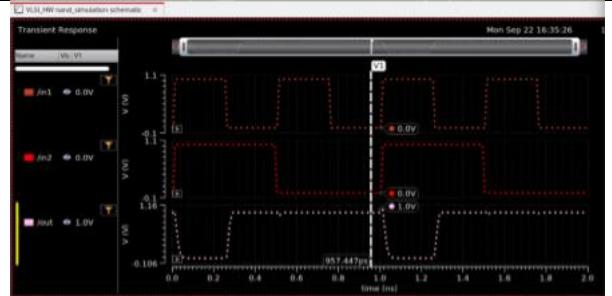
PEX Netlist Output

```

Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
----- nand.pex.netlist -----
1 * File: nand.pex.netlist
2 * Created: Sat Sep. 6 18:47:15 2025
3 * Version: v2024.3..25.13
4 *
5 * include "nand.pex.netlist.pex"
6 * subckt name IN2 IN1 OUT VDD VSS
7 *
8 * VSS VSS
9 * VDD VDD
10 * OUT OUT
11 * IN1 IN1
12 * IN2 IN2
13 *
14 MM1 NET1 I N2 MM3 g N VSS MM3 J N VSS_MM3_b NMOS_VTL L=5e-08 W=2e-07 AD=-6.4e-14
15 + AS=-5.45e-14 PD=1.04e-06 PS=-9.45e-07
16 MM2 N OUT_MM2 d N IN1 MM2 g NET1 N VSS_MM3_b NMOS_VTL L=5e-08 W=2e-07
17 + AD=-6.15e-14 AS=-6.4e-14 PD=1.015e-06 PS=1.04e-06
18 MM3 N OUT_MM1 d N IN2 MM1 g N VDD_MM1_1 N VDD_MM1_2 NMOS_VTL L=5e-08 W=2e-07
19 + AD=-6.4e-14 AS=-5.45e-14 PD=1.04e-06 PS=-9.45e-07
20 MM0 N OUT_MM0 d N IN1 MM0 g N VDD_MM0_1 N VDD_MM0_2 NMOS_VTL L=5e-08 W=2e-07
21 + AD=-6.4e-14 AS=-6.15e-14 PD=1.04e-06 PS=1.015e-06
22 *
23 include "nand.pex.netlist.NAND.pex"
24 *
25 ends
26
27

```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```

File Edit View Help           cadence

***** PrimeSim HSPICE Threads Information *****

Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes      = 61 # elements = 115
# resistors = 39 # capacitors = 69 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vcvs = 0
# cccs       = 0 # ccvs = 0 # volt_srcs = 3
# curr_srcs = 0 # diodes = 0 # bjts = 0
# jfets      = 0 # mosfets = 4 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis          time # points tot. iter conv.riter
op point         0.00          1     13
transient        0.01          41    400          163 rev-
readin          0.00
errchk          0.00
setup            0.00
output           0.00

peak memory used      527.80 megabytes
total cpu time        0.02 seconds
total elapsed time    1.83 seconds
job started at       16:35:24 09/22/2025
job ended at         16:35:26 09/22/2025

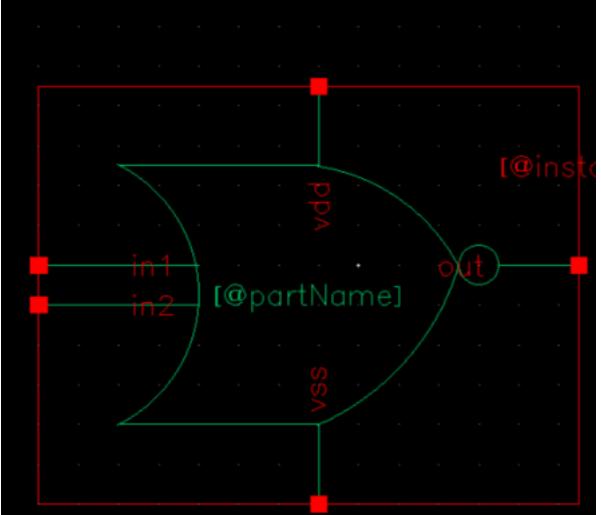
>info:      ***** hspice job concluded
             inh_total_runtime   1.81 seconds

```

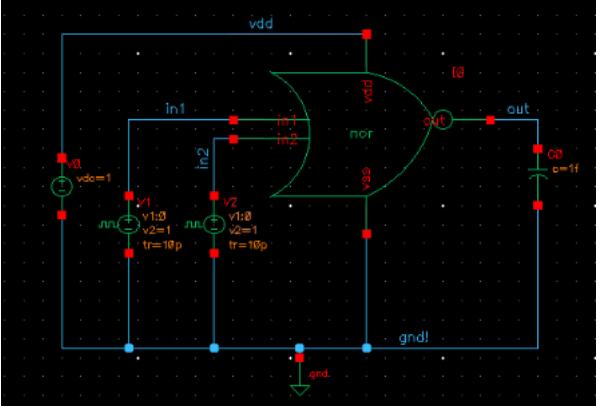
NOR

Required Snapshot Description	Snapshot
Schematic (Design)	

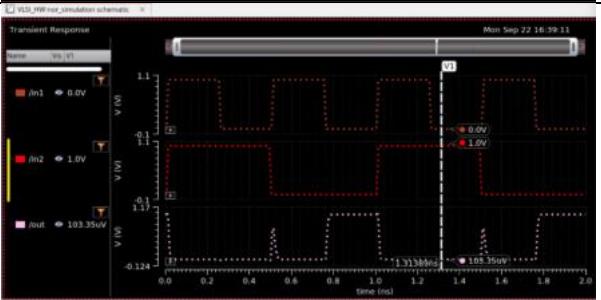
Schematic Symbol Design (Optional)



Schematic Simulation Waveform Design



Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/nor_simulation/hspiceD/schematic/psf/hspic... x
File Edit View Help
cadence

***** Circuit Statistics *****
# nodes      = 22 # elements =     8
# resistors =  0 # capacitors =   1 # inductors =     0
# mutual_conds = 0 # ccvs =    0 # vccs =     0
# cccs      = 0 # ccvs =    0 # volt_srcs =     3
# curr_srcs = 0 # diodes =   0 # bjt =     0
# jfets      = 0 # mosfets =   4 # U elements =     0
# T elements = 0 # N elements = 0 # B elements =     0
# S elements = 0 # P elements = 0 # va device =     0
# vector_srcs = 0 # N elements = 0

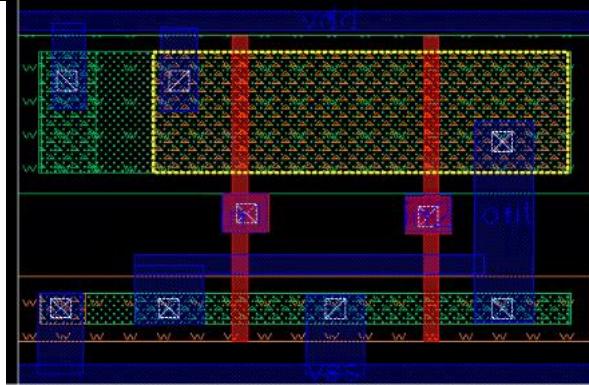
***** Runtime Statistics (seconds) *****
analysis      time # points tot. iter conv. iter
op point     0.00      1       4
transient    0.01     41      510      194 rev=
readin       0.00
errchk       0.00
setup        0.00
output       0.00

peak memory used      527.80 megabytes
total cpu time        0.02 seconds
total elapsed time    2.04 seconds
job started at        16:39:09 09/22/2025
job ended at          16:39:11 09/22/2025

>info: ***** hspice job concluded
job total runtime     2.04 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.02(s)
```

Schematic Layout Design



DRC Transcript

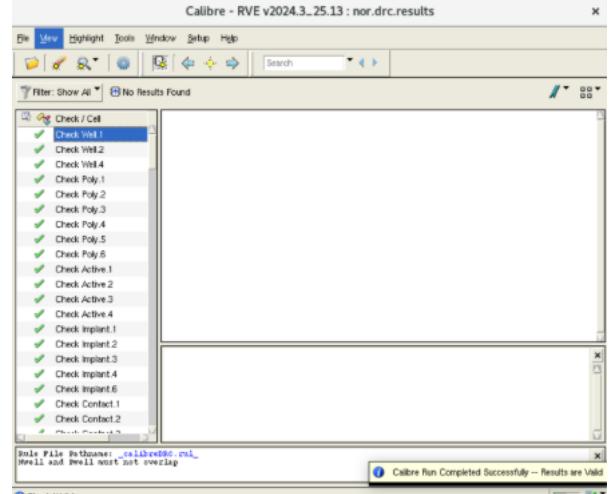
```
Activities Calibre Interactive - n... Sep 7 12:41
Calibre Interactive - nmDRC v2024.3_25.13 : ./runset.calibre.drc * x
File Settings Configurations Help TOTAL CPU TIME | 1/1 < >
Rules Inputs Outputs Run Control Search Transcript Files
Cumulative CONNECT Time: CPU = 0 REAL = 0
Cumulative RDB Time: CPU = 0 REAL = 0
-- CALIBRE-DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
-- TOTAL RULECHECKS EXECUTED = 367
-- TOTAL RESULTS GENERATED = 0 (0)
-- DRC RESULTS DATABASE FILE = nor.drc.results (ASCII)
-- CALIBRE-DRC-H COMPLETED - Sun Sep 7 12:40:03 2025
4066 -- CPU TIME = 0 REAL TIME = 2
-- PROCESSOR COUNT = 1
-- SUMMARY REPORT FILE = nor.drc.summary

*** DRC run finished with exit code 0 ***

INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -drc nor.drc.results
RVE: // Calibre v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0-10_13-2017-1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Lith Libraries v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
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RVE: // The registered trademark Linux is used pursuant to a sublicense from L
RVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide
RVE: //
RVE: // Mentor Graphics software executing under x86-64 Linux
RVE: //
RVE: // Running on 1 CPU
RVE: //
RVE: //

0 Errors, 1 Warning, 1 Info
Line Type Description
90 Warning Please increase descriptors limit for best performance...
```

DRC Results



LVS Transcript

```

Calibre Interactive - nmLVS v2024.3.25.13 : ./runset.calibre.lvs *
File Settings Configurations Help TOTAL CPU TIME 2/2

Rules:
Inputs
H-Cells
Outputs
ERC
Signatures
Run Control
Search
Transcript
Files

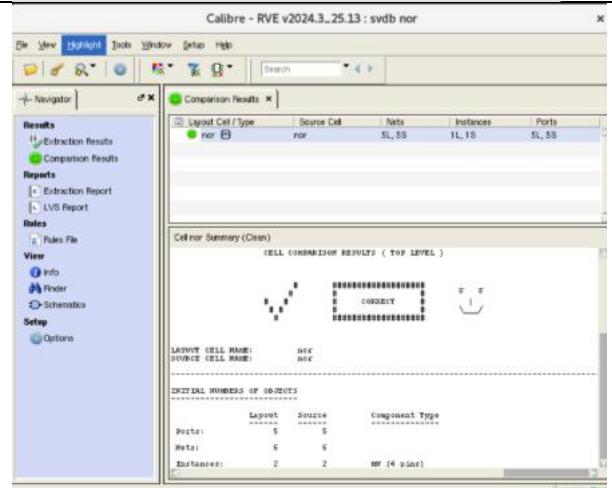
Run LVS
Start RVE

LVS completed. CORRECT. See report file: nor.lvs.report
LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 66/67/67 MALLOC = 87/8
-- LVS REPORT FILE = nor.lvs.report
1585 -- CALIBRE::LVS COMPARISON MODULE COMPLETED. TOTAL CPU TIME = 0 REAL TIME
-- CALIBRE::LVS/NRC COMPLETED - Sun Sep 7 12:49:51 2025
-- XDB CROSS REFERENCE DATABASE = svldb/nor.xdb
-- SPICE NETLIST FILE = nor.sp
-- CIRCUIT EXTRACTION REPORT FILE = nor.lvs.report.ext
-- PERSISTENT HIERARCHICAL DATABASE(PHDB) = svldb/nor.phdb
-- QUERY DATABASE = svldb: TOP CELL = nor
-- GRAND TOTAL NON-HYPER/LVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP
*** LVS run finished with exit code 0 ***
INFO: Starting command: $MGC_HOME/bin/calibre -nowait -lvs svldb nor
PVE: // Calibre v2024.3.25.13 Thu Aug 1 18:57:13 PDT 2024
PVE: // Calibre Utility Library v0.10.13-2017-1 Fri Apr 12 08:04:27 PDT 2024
PVE: // Litho Libraries v2024.3.25.13 Thu Aug 1 18:57:13 PDT 2024
PVE: //
PVE: // Copyright Siemens 1996-2024
PVE: // All Rights Reserved.
PVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
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PVE: // OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
PVE: //
PVE: // The registered trademark Linux is used pursuant to a sublicense from LMI, the
PVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
PVE: //
PVE: // Mentor Graphics software executing under x86-64 Linux
PVE: //

0 Errors, 1 Warning, 2 Infos
Line Type Description
9 Info Verifying the source netlist is complete before starting th...

```

LVS Comparision Results



PEX Transcript

Calibre Interactive - PEX v2024.3_25.13 : ./runset.calibre.pex *

File Settings Configurations Help Search

Rules
Inputs
Outputs
LVS
Run Control
Search
Transcript
Files

Run PEX
Start RVE

```

2164 -----
2165 ----- PDB NET SUMMARY -----
2166 -----
2167 pdb file name = svdb/NOR.pdb
2168 root cell name = NOR
2169 total nets = 6
2170 top-level nets = 5
2171 non-top-level nets = 0
2172 degenerate nets = 1
2173 merged nets = 0
2174 error nets = 0
2175
2176 -----
2177 ----- CALIBRE xRC WARNING / ERROR Summary -----
2178 -----
2179 xRC Warnings = 3
2180 xRC Errors = 0
2181 -----
2182 -----
2183 ----- CALIBRE xRC::FORMATTER COMPLETED - Sun Sep 7 12:57:03 2025
2184 ----- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 15/76/299 MALLOC = 236/2
2185 -----
2186 *** xRC run finished with exit code 0 ***

```

Line	Type	Description
10	Info	Verifying the source netlist is complete before starti...
07	Information	Please increase deobfuscate_level for better performance.

PEX Netlist Output

Calibre Interactive - PEX v2024.3_25.13 : ./runset.calibre.pex *

File Settings Configurations Help Search

Rules
Inputs
Outputs
LVS
Run Control
Search
Transcript
Files

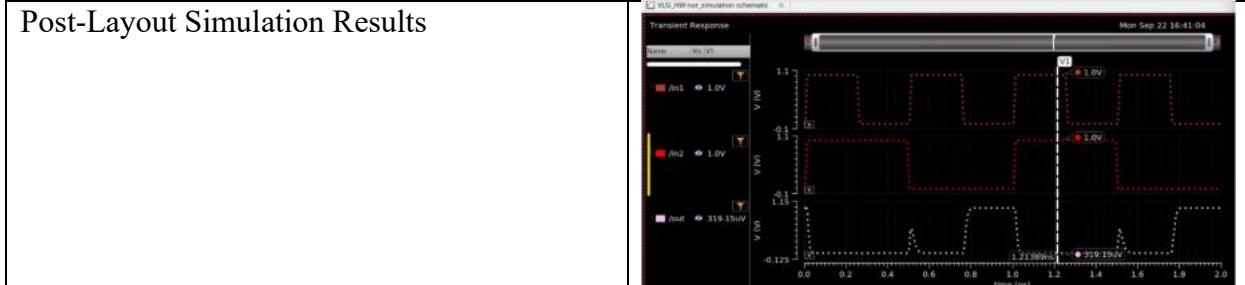
Run PEX
Start RVE

```

1 * File: nor.pex.netlist
* Created: Sun Sep 7 12:57:02 2025
* Program "Calibre xRC"
* Version "v2024.3_25.13"
*
.include "nor.pex.netlist.pex"
.subckt nor VDD IN1 VSS IN2 OUT
*
* OUT OUT
* IN2 IN2
* VSS VSS
* IN1 IN1
* VDD VDD
MM3_N_OUT_MM3_d_N_IN1_MM3_g_N_VSS_MM3_s_N_VSS_MM3_b NMOS_VTL
L=5e-08 W=1e-07
+ AD=3.2e-14 AS=5.825e-14 PD=8.4e-07 PS=1.365e-06
MM2_N_OUT_MM2_d_N_IN2_MM2_g_N_VSS_MM3_s_N_VSS_MM3_b NMOS_VTL
L=5e-08 W=1e-07
+ AD=4.3e-14 AS=5.825e-14 PD=1.06e-06 PS=1.365e-06
MM0_NET1_N_IN1_MM0_g_N_VDD_MM0_s_N_VDD_MM0_b PMOS_VTL L=5e-08
W=4e-07
+ AD=2.33e-13 AS=1.05e-13 PD=1.965e-06 PS=1.325e-06
MM1_N_OUT_MM1_d_N_IN2_MM1_g_NET1_N_VDD_MM0_b PMOS_VTL L=5e-08
W=4e-07 AD=1.7e-13
+ AS=2.33e-13 PD=1.65e-06 PS=1.965e-06
*
.include "nor.pex.netlist.NOR.pxi"
*
.ends
*

```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```

/home/zeruv/simulation/nor_simulation/hspiceD/schematic/pnf/hspic... >
File Edit View Help
cadence

***** Circuit Statistics *****
# nodes      = 59 # elements      = 109
# resistors  = 37 # capacitors   = 65 # inductors  = 0
# mutual_conds = 0 # cccvs       = 0 # vcvss      = 0
# cccs        = 0 # ccvs        = 0 # volt_srcs   = 3
# curr_srcs   = 0 # diodes       = 0 # bjts        = 0
# jfets        = 0 # mosfets      = 4 # U elements = 0
# T elements  = 0 # W elements   = 0 # B elements = 0
# S elements  = 0 # P elements   = 0 # va device   = 0
# vector_srcs = 0 # N elements   = 0

***** Runtime Statistics (seconds) *****
analysis      time    # points tot. iter conv.converter
op point     0.00          1       12
transient    0.01         41      402      163 rev=1
readin       0.00
errchk       0.00
setup        0.00
output       0.00

peak memory used      527.80 megabytes
total cpu time        0.02 seconds
total elapsed time    1.68 seconds
job started at        16:41:02 09/22/2025
job ended at          16:41:03 09/22/2025

>info:      ***** hspice job concluded
                job total runtime    1.68 seconds

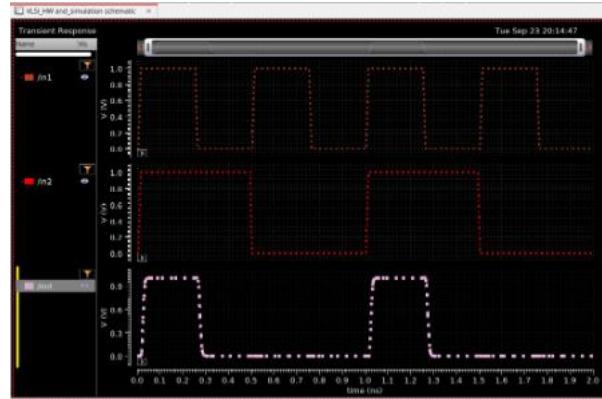
lic: Release hspice token(s)
lic: total license checkout elapse time: 1.66(s)

```

And Gate

Required Snapshot Description	Snapshot
Schematic (Design)	
Schematic Simulation Waveform Design	

Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/and_simulation/hspiceD/schematicC/pst/hspic... x
File Edit View Help
cadence
***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 31 # elements = 10
# resistors = 0 # capacitors = 1 # inductors = 0
# control_lnds = 0 # vccs = 0 # vccs = 0
# cccs = 0 # ccvs = 0 # ccvs = 3
# curr_srcs = 0 # diodes = 0 # volt_srcs = 0
# jfets = 0 # mosfets = 6 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # VA device = 0
# vector_srcs = 0 # N elements = 0

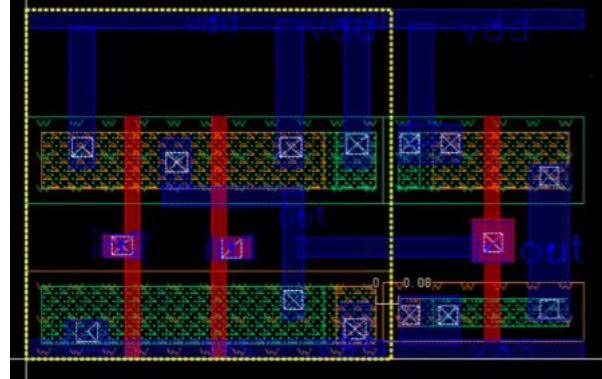
***** Runtime Statistics (seconds) *****
analysis          time # points tot. iter conv.riter
op point        0.00      1       6
transient        0.01     41      513      198 rev= 3
readin          0.00
errchk          0.00
setup           0.00
output          0.00

peak memory used      527.80 megabytes
total cpu time        0.02 seconds
total elapsed time    2.00 seconds
job started at 18:12:41 09/20/2025
job ended at 18:12:43 09/20/2025

>info:      ***** hspice job concluded
>info:      job total runtime 2.00 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 1.98(s)
```

Schematic Layout Design



DRC Transcript

```
Calibre Interactive - nmDRC v2024.3..25.13 : ./runset.calibre.drc *
File Settings Configurations Help TOTAL CPU TIME 1/1
Rules Inputs Outputs Run Control Search Transcript Files
-- CALIBRE:DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
-- TOTAL RULECHECKS EXECUTED = 167
-- TOTAL RESULTS GENERATED = 0 (0)
-- DRC RESULTS DATABASE FILE = and.drc.results (ASCII)

-- CALIBRE:DRC-H COMPLETED - Sat Sep 20 16:30:15 2025
-- TOTAL CPU TIME = 0 REAL TIME = 2
-- PROCESSOR COUNT = 1
-- SUMMARY REPORT FILE = and.drc.summary

*** DRC run finished with exit code 0 ***

INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -drc and.drc.results

RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0_10_13-2017_1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: //
RVE: // Copyright Siemens 1996-2024
RVE: // All Rights Reserved.
RVE: // THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION

Run DRC Start RVE 0 Errors, 1 Warning, 1 Info ? Filter
Line Type Description
```

DRC Results

Calibre - RVE v2024.3..25.13 : and.drc.results

File View Highlight Tools Window Setup Help

Filter: Show All | No results found

Check / Cell	Res
✓ Check Vdd.1	0
✓ Check Vdd.2	0
✓ Check Vdd.4	0
✓ Check Poly.1	0
✓ Check Poly.2	0
✓ Check Poly.3	0
✓ Check Poly.4	0
✓ Check Poly.5	0
✓ Check Poly.6	0
✓ Check Active.1	0
✓ Check Active.2	0
✓ Check Active.3	0
✓ Check Active.4	0
✓ Check Inspect.1	0
✓ Check Inspect.2	0
✓ Check Inspect.3	0
✓ Check Inspect.4	0
✓ Check Inspect.5	0
✓ Check Contact.1	0
✓ Check Contact.2	0
✓ Check Contact.3	0

Results File Pathname: calibre303.rvl
Rvll and Rvll must not overlap

Calibre Run Completed Successfully -- Results are Valid

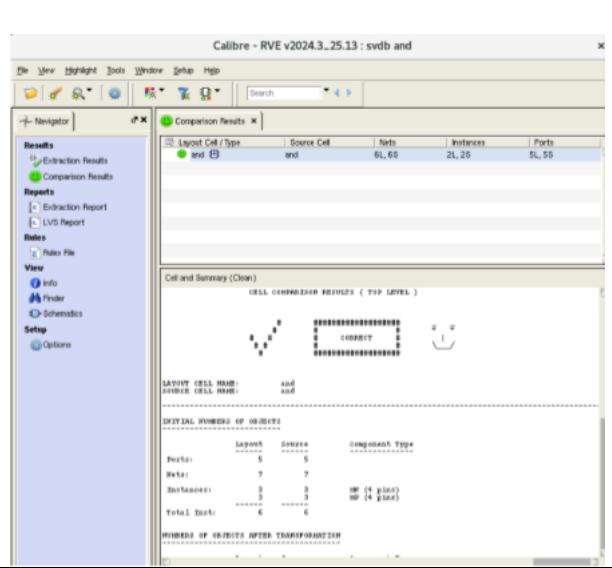
LVS Transcript

```
Calibre Interactive - nmLVS v2024.3..25.13 : ./runset.calibre.lvs *
File Settings Configurations Help TOTAL CPU TIME 2/2
Rules Inputs H-Cells Outputs Run Control Search Transcript Files
LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 67/69/69 MALLOC = 88/88/88
-- LVS REPORT FILE = and.lvs.report
1587 -- CALIBRE:LVS COMPARISON MODULE COMPLETED. TOTAL CPU TIME = 0 REAL TIME
-- CALIBRE:LVS/XRC COMPLETED - Sat Sep 20 16:32:45 2025
-- XDB CROSS REFERENCE DATABASE = svdb/and.xdb
-- SPICE NETLIST FILE = and.sp
-- CIRCUIT EXTRACTION REPORT FILE = and.lvs.report.ext
-- PERSISTENT HIERARCHICAL DATABASE(PHOB) = svdb/and.phdb
-- QUERY DATABASE = svdb TOP CELL = and
-- GRAND TOTAL NON-HYPER/LVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHEAP =
*** LVS run finished with exit code 0 ***

INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -lvs svdb and

RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0_10_13-2017_1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: //
```

LVS Comparision Results



PEX Transcript

```
Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
Run PEX Start RVE
=====
PDB NET SUMMARY
=====
pdb file name = svdb/AND.pdb
root cell name = AND
total nets = 7
top-level nets = 6
non-top-level nets = 0
degenerate nets = 1
merged nets = 0
error nets = 0
WARNING: No ground net name defined in PEX NETLIST statement and "0" will be used

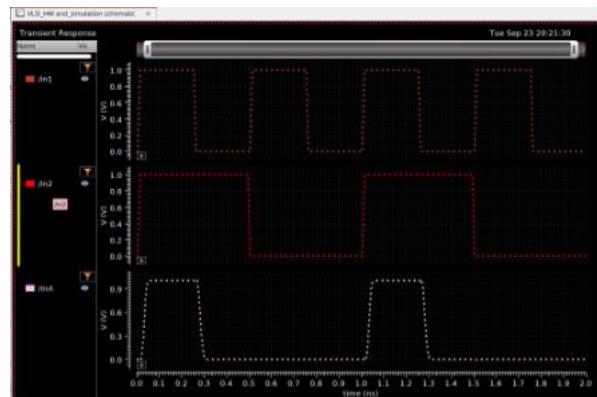
=====
CALIBRE xRC WARNING / ERROR Summary
=====
xRC Warnings = 3
xRC Errors = 0
=====

-- CALIBRE xRC::FORMATTER COMPLETED - Sat Sep 20 16:34:19 2025
-- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 15/76/299 MALLOC = 233/233/262
*** xRC run finished with exit code 0 ***
2217
```

PEX Netlist Output

```
Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
Run PEX Start RVE
and.pex.netlist *
1 * File: and.pex.netlist
1 * Created: Sat Sep 20 16:34:18 2025
1 * Program: "Calibre xRC"
1 * Version: "v2024.3..25.13"
1 *
1 .include "and.pex.netlist.pex"
1 subckt and IN2 IN1 VDD VSS OUT
1 *
1 * OUT OUT
1 * VSS VSS
1 * VDD VDD
1 * IN1 IN1
1 * IN2 IN2
mX10/MM3 X10/NET1 N_IN2_X10/MMM2 g N_VSS_X10/MMM3_3 N_VSS_X10/MMM3_b NMOS_VTL
+ L=5e-08 W=2e-07 AD=5.15e-14 AS=5.95e-14 PD=9.15e-07 PS=9.95e-07
mX10/MM2 N_IN1_X10/MM2_d N_IN1_X10/MM2_g X10/NET1_N_VSS_X10/MM3_b NMOS_VTL
+ L=5e-08 W=2e-07 AD=5.15e-14 AS=5.95e-14 PD=9.15e-07 PS=9.95e-07
mX11/MM1 N_IN1_X11/MM1_d N_IN1_X11/MM1_g N_VSS_X10/MMM1_3 N_VSS_X10/MMM1_b NMOS_VTL
+ L=5e-08 W=2e-07 AD=2.45e-14 AS=1.85e-14 PD=9.9e-07 PS=5.7e-07
mX10/MM1 N_IN1_X10/MM1_d N_IN2_X10/MM1_g N_VDD_X10/MMM1_s N_VDD_X10/MMM1_b
+ PMOS_VTL L=5e-08 W=2e-07 AD=5.15e-14 AS=5.95e-14 PD=9.15e-07 PS=9.95e-07
mX10/MM0 N_IN1_X10/MM1_d N_IN1_X10/MM0_g N_VDD_X10/MMM0_s N_VDD_X10/MMM0_b
+ PMOS_VTL L=5e-08 W=2e-07 AD=5.15e-14 AS=6.9e-14 PD=9.15e-07 PS=1.09e-06
mX11/MM2 N_OUT_X11/MM2_d N_NET1_X11/MM2_g N_VDD_X11/MMM2_3 N_VDD_X10/MMM1_b
+ PMOS_VTL L=5e-08 W=2e-07 AD=4.9e-14 AS=3.7e-14 PD=8.9e-07 PS=7.7e-07
*
1 .include "and.pex.netlist.AND.pxi"
1 *
1 .ends
1 *
1 *
```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```
/home/zeruv/simulation/and_simulation/hspiceD/schematic/psf/hspic... x
File Edit View Help
cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 91 # elements = 173
# resistors = 62 # capacitors = 102 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vcc = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 3
# curr_srcs = 0 # diodes = 0 # bjt = 0
# curr_vsrcs = 0 # mosfets = 6 # U elements = 0
# jfets = 0 # npn = 0 # pnp = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # VA device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op_start 0.00 1 13
transient 0.01 41 421 169 rev
readin 0.01
errchk 0.00
setup 0.00
output 0.00

peak memory used 527.80 megabytes
total cpu time 0.02 seconds
total elapsed time 2.07 seconds
job started at 01:37:37 09/21/2005
job ended at 01:37:39 09/21/2005

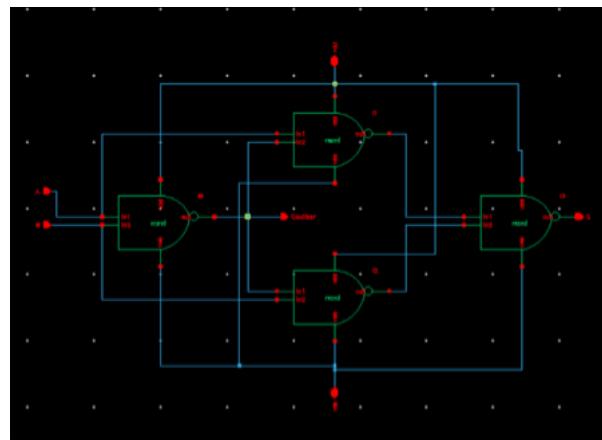
>info: ***** hspice job concluded
job total runtime 2.07 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.05(s)
```

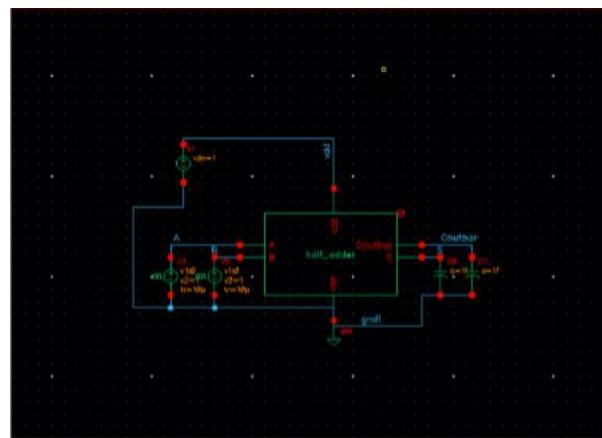
XOR/Half-Adder (The Counter Requires an XOR Gate, and a half-adder has the same function/truth table as an xor gate, which works for this purpose).

Required Snapshot Description	Snapshot
-------------------------------	----------

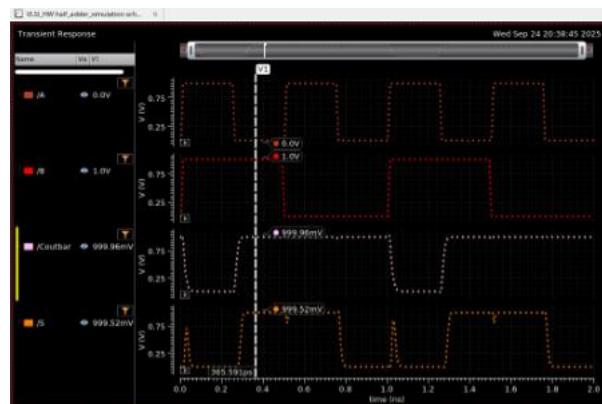
Schematic (Design)



Schematic Simulation Waveform Design



Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/half_adder_simulation/hspiceD/schematic/p_<-->.out
File Edit View Help
cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 76 # elements = 21
# resistors = 0 # capacitors = 2 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vccv = 0
# ccos = 0 # curvs = 0 # curr_srcs = 3
# curr_srcs = 0 # diodes = 0 # brys = 0
# fetes = 0 # mosfets = 16 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # VA device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tet. iter conv.mtr
op point 0.00 1 13
transient 0.02 41 671 246 rev
readin 0.00
errchk 0.00
setup 0.00
output 0.00

peak memory used 527.80 megabytes
total cpu time 0.03 seconds
total elapsed time 2.17 seconds
job started at 19:34:08 09/17/2025
job ended at 19:34:08 09/17/2025

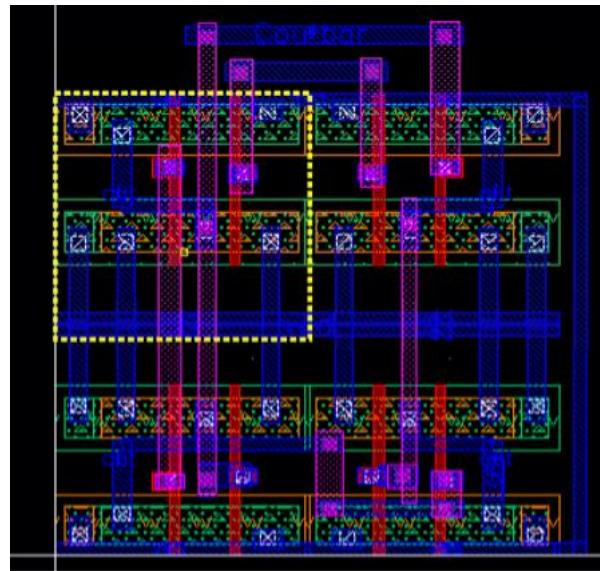
>info: ***** hspice job concluded
job total runtime 2.17 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.13(s)

/home/zeruv/simulation/half_adder_simulation/hspiceD/schematic/psf/hspice.out
File Edit View Help
cadence

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this software is strictly prohibited.
Input File: input.ckt
Command line options: /usr/local/isde/synopsis/hspice/linux64/hspice input.ckt
Start time: Wed Sep 17 19:34:06 2025
lic: FLEXIM: SDK 12.11.6
lic: USER: zero
lic: HOSTID: 37bae5fc
lic: Using FLEXIM license file:
lic: 732681license.isde.vanderbilt.edu
lic: Checkout 1 hspice
lic: License/Maintenance for hspice will expire on 24-oct-2025/2023.03
lic: (%in_use/50total) FLOATING license(s) on SERVER 732681license.isde.vanderbilt.edu
lic:
***** PrimeSim HSPICE -- U-2023.03-SPI-2 linux64 (Jul 31 2023 838398) *****
***** generated for: hspiced
***** circuit name directory
circuit number to circuit name directory
number circuitname definition multiplier
1 x00 half_adder 1.00
2 x10 x13 nand 1.00
3 x10 x12 nand 1.00
4 x10 x11 nand 1.00
5 x10 x10 nand 1.00
*****
** generated for: hspiced
***** psf model parameters tnom= 25.000 temp= 25.000 *****
Model file: /usr/local/isde/PSF/freePSF5/ncsu_basel1/models/hspice/tran_models/models_nmn/AMOS_VTL.inc
Model LINE: 3
Model Name: amos_vtl
OSIM Model (Level 54)
Model Type: SPICE
BINWRT = 1
PARAMCHK = 1
CAPMOD = 2
DTMOD = 1
***** Trace: /A/Clock: Home/zeruv/simulation/half_adder_simulation/hspiceD/schematic/pd:Dataset:timesweep 1625 249
```

Schematic Layout Design



DRC Transcript

Calibre Interactive - nmDRC v2024.3..25.13 : ./runset.calibre.drc *

File Settings Configurations Help Search

Rules Inputs Outputs Run Control Search Transcript Files

Run DRC Start RVE

```
-- CALIBRE-DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
-- TOTAL RULECHECKS EXECUTED = 167
-- TOTAL RESULTS GENERATED = 0 (0)
-- DRC RESULTS DATABASE FILE = half_adder.drc.results (ASCII)

-- CALIBRE-DRC-H COMPLETED - Wed Sep 17 12:04:44 2025
-- TOTAL CPU TIME = 0 REAL TIME = 2
-- PROCESSOR COUNT = 1
-- SUMMARY REPORT FILE = half_adder.drc.summary

*** DRC run finished with exit code 0 ***

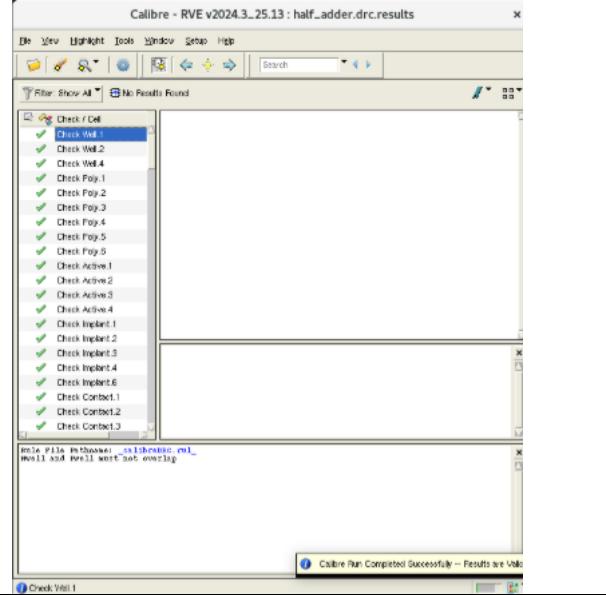
INFO: Starting command: $MGC_HOME/bin/calibre -nowait -rve -drc half_adder.drc.res

RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0.10.13 2017.1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
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RVE: // The registered trademark Linux is used pursuant to a sublicense from LMI,
RVE: // the exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.
RVE: //
RVE: // Mentor Graphics software executing under x86-64 Linux
```

0 Errors, 1 Warning, 1 Info

Line	Type	Description
90	Warning	Please increase descriptors limit for best performance (1024)
4084	Info	Starting command: \$MGC_HOME/bin/calibre -nowait -rve -drc...

DRC Results



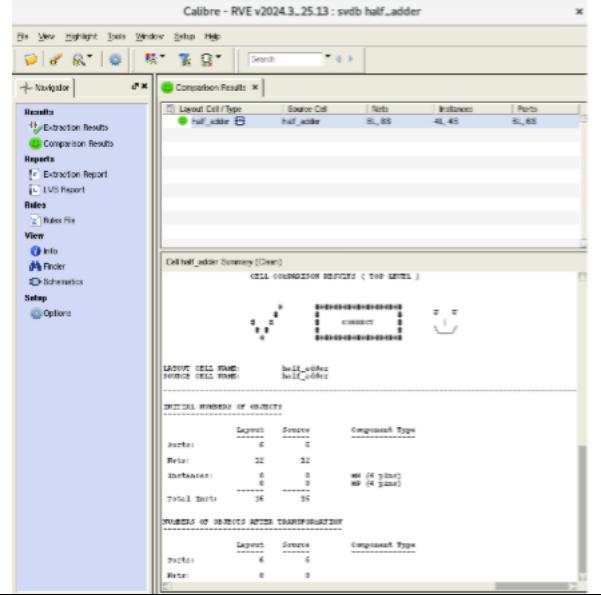
LVS Transcript

```

Calibre Interactive - nmLVS v2024.3_25.13 : ./runset.calibre.lvs *
File Settings Configurations Help TOTAL CPU TIME 2/2
Rules Inputs H-Cells Outputs ERC Signatures Run Control Search Transcript Files
LVS completed. CORRECT. See report file: half_adder.lvs.report
LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 66/69/69 MALLOC = 86
-- LVS REPORT FILE = half_adder.lvs.report
1613 -- CALIBRE:LVS COMPARISON MODULE COMPLETED. [TOTAL_CPU_TIME] = 0 REAL
-- CALIBRE:LVSxRC COMPLETED - Wed Sep 17 12:24:17 2023
-- XDB CROSS REFERENCE DATABASE = svdb/half_adder.xdb
-- SPICE NETLIST FILE = half_adder.sp
-- CIRCUIT EXTRACTION REPORT FILE = half_adder.lvs.report.ext
-- PERSISTENT HIERARCHICAL DATABASE(PHDB) = svdb/half_adder.phdb
-- QUERY DATABASE = svdb TOP CELL = half_adder
-- GRAND TOTAL NON-HYPER/LVS COMPARE CPU TIME = 0 REAL TIME = 3 LVHE
*** LVS run finished with exit code 0 ***
INFO: Starting command: $MOC_HOME/bin/calibre -nowait -rve -lvs svdb half_adder
RVE: // Calibre v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v0-10_13-2017-1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Litho Libraries v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
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RVE: // Mentor Graphics software runs under the GPL license.

```

LVS Comparision Results



PEX Transcript

```
Calibre Interactive - PEX v2024.3_25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
Run PEX Start RVE
----- PDB NET SUMMARY -----
pbd file name = svdb/HALF_ADDER.pbd
root cell name = HALF_ADDER
total nets = 12
top-level nets = 8
non-top-level nets = 0
degenerate nets = 4
merged nets = 0
error nets = 0

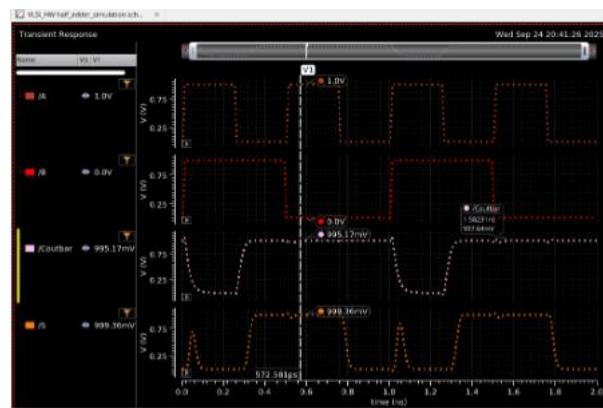
===== CALIBRE xRC WARNING / ERROR Summary =====
xRC Warnings = 3
xRC Errors = 0
=====

-- CALIBRE XRC-FORMATTER COMPLETED - Wed Sep 17 12:28:46 2025
-- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 15/76/299 MALLOC = 260/260
*** XRC run finished with exit code 0 ***
```

PEX Netlist Output

```
Calibre Interactive - PEX v2024.3_25.13 : ./runset.calibre.pex *
File Settings Configurations Help Search
Rules Inputs Outputs LVS Run Control Search Transcript Files
half_adder.pex.netlist *
1 File: half_adder.pex.netlist
* Created: Wed Sep 17 12:28:45 2025
* Program "Calibre xRC"
* Version "v2024.3_25.13"
*
include "half_adder.pex.netlist.pex"
subckt half_adder A COUTBAR B VDD VSS S
*
* S S
* VSS VSS
* VDD VDD
* B B
* COUTBAR COUTBAR
* A A
m/X1_MM3_X11_NET1_N_COUTBAR_X11_MM3_g N_VSS_X11_MM3_s N_V55_X11_MM3_b
NMOS_VTL
+ L=5e-08 W=2e-07 AD=5.15e-14 AS=5.95e-14 PD=9.15e-07 PS=9.95e-07
m/X1_MM2_N_NET1_X11_MM2_d N_A_X11_MM2_g X11_NET1_N_V55_X11_MM3_b
NMOS_VTL
+ L=5e-09 W=2e-07 AD=6.9e-14 AS=5.15e-14 PD=1.09e-06 PS=9.15e-07
m/X1_MM1_N_NET1_X11_MM1_d N_COUTBAR_X11_MM1_g N_VDD_X11_MM1_b
NMOS_VTL
+ PMOS_VTL L=5e-08 W=2e-07 AD=5.15e-14 AS=5.95e-14 PD=9.15e-07
PS=9.95e-07
m/X1_MM0_N_NET1_X11_MM0_d N_A_X11_MM0_g N_VDD_X11_MM0_s
N_VDD_X11_MM0_b PMOS_VTL
+ L=5e-08 W=2e-07 AD=5.15e-14 AS=6.9e-14 PD=9.15e-07 PS=1.09e-06
m/X0_MM3_X10_NET1_N_B_X10_MM3_g N_V55_X10_MM3_s N_V55_X10_MM3_b
NMOS_VTL L=5e-08
+ W=2e-07 AD=5.15e-14 AS=5.95e-14 PD=9.15e-07 PS=9.95e-07
m/X0_MM2_N_COUTBAR_X10_MM2_d N_A_X10_MM2_g X10_NET1_N_V55_X10_MM3_b
NMOS_VTL
... (remaining netlist lines)
```

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```

home/zeruv/simulation/half_adder_simulation/hspiceD/schematic/p... x
File Edit View Help cādence
***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 264 # elements = 592
# resistors = 192 # capacitors = 381 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vcss = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 3
# curr_srcs = 0 # diodes = 0 # bjt = 0
# pmos = 0 # nmos = 163 # elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # VA device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis      time   # points tot. iter conv.riter
op point    0.00      1       1    23
transient    0.04     41      561    211 rev=1
readin       0.01
scrch        0.01
setup        0.00
output       0.00

peak memory used      527.80 megabytes
total cpu time        0.06 seconds
total elapsed time    2.17 seconds
job started at        19:53:17 09/17/2025
job ended at          19:53:19 09/17/2025

info: ***** hspice job concluded
info: job total runtime 2.17 seconds

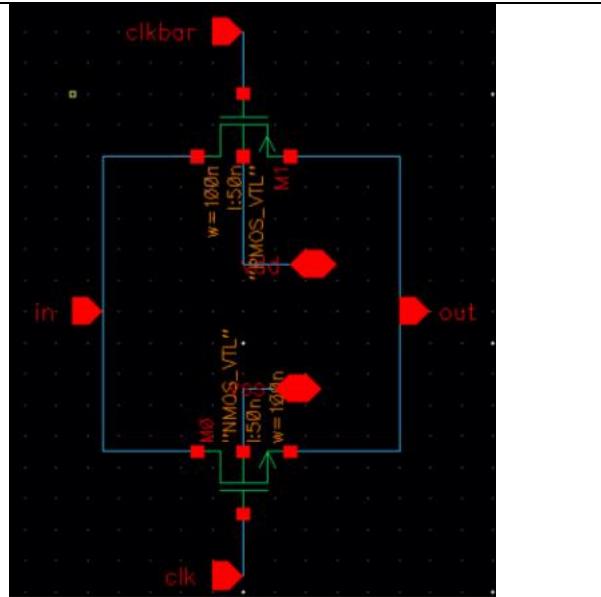
lic: Release hspice token(s)
lic: total license checkout elapse time: 2.11(s)

```

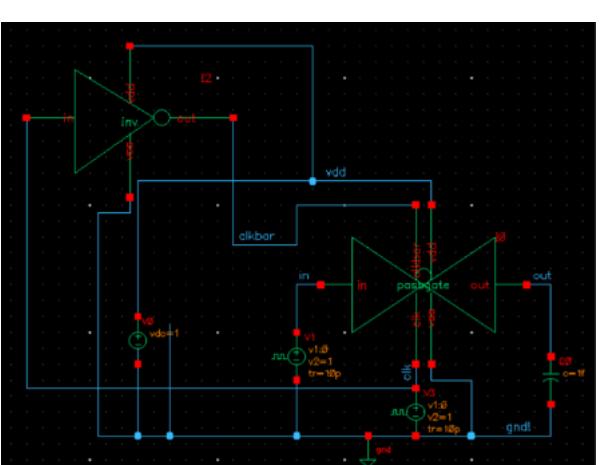
Passgate

Required Snapshot Description	Snapshot
-------------------------------	----------

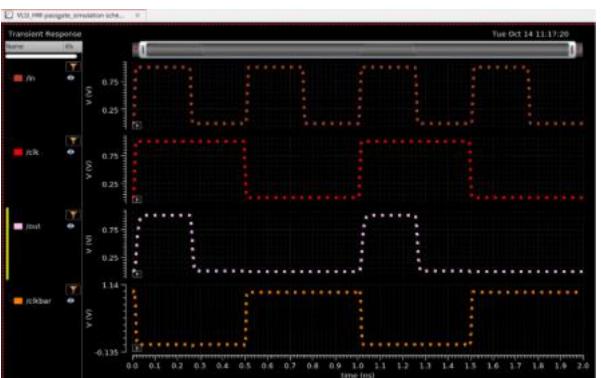
Schematic (Design)



Schematic Simulation Waveform Design



Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/passgate_simulation/hspiceD/schematic/psff... x
File Edit View Help
cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 22 # elements = 8
# resistors = 0 # capacitors = 1 # inductors = 0
# mosfet_ldns = 0 # cccs = 0 # vccs = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 3
# curr_srcs = 0 # diodes = 0 # bnts = 0
# jfets = 0 # mosfets = 4 # U elements = 0
# t_element = 0 # M elements = 0 # B elements = 0
# elements = 0 # N elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

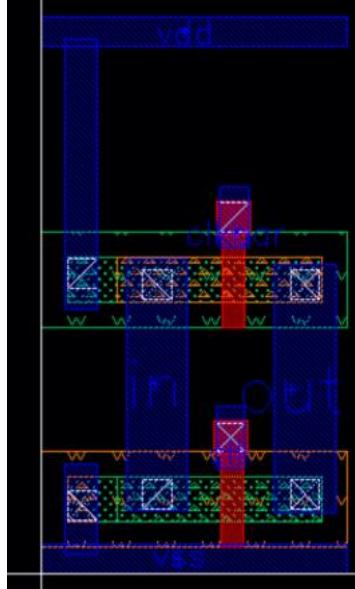
***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op point 0.00 1 5
transient 0.00 41 442 178 rev+ 2
readin 0.00
ercheck 0.00
setup 0.00
output 0.00

peak memory used 527.80 megabytes
total cpu time 0.02 seconds
total elapsed time 2.12 seconds
job started at 11:17:17 10/14/2025
job ended at 11:17:20 10/14/2025

>info: ***** hspice job concluded
>info: job total runtime 2.12 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.11(s)
```

Schematic Layout Design



DRC Transcript

Calibre Interactive - nmDRC v2024.3..25.13 : ./sunset.calibre.drc *

File Settings Configurations Help

Rules
--- TOTAL RULECHECKS EXECUTED = 167
--- TOTAL RESULTS GENERATED = 0 (0)
--- DRC RESULTS DATABASE FILE = passgate.drc.results (ASCII)

Inputs
4066 --- CALIBRE - DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0

Outputs
--- TOTAL CPU TIME = 0 REAL TIME = 2

Run Control
--- PROCESSOR COUNT = 1

Search
--- SUMMARY REPORT FILE = passgate.drc.summary

Transcript
4066 *** DRC run finished with exit code 0 ***

Files

INFO: Starting command: \$MGC_HOME/bin/calibre -nowait -rve -drc passgate.drc.results

RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024

RVE: // Calibre Utility Library v0.10.13-2017-1 Fri Apr 12 08:04:27 PDT 2024

RVE: // Litho Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024

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RVE: // exclusive licensee of Linus Torvalds, owner of the mark on a world-wide basis.

RVE: //

RVE: // Mentor Graphics software executing under x86-64 Linux

Run DRC

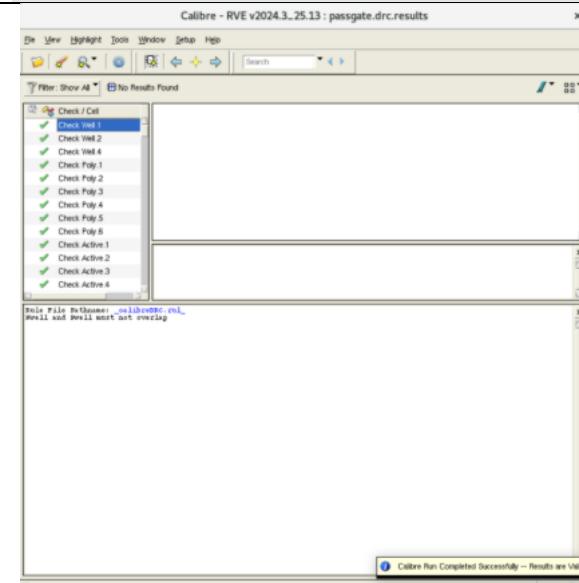
Show RVE

0 Errors, 1 Warning, 1 Info

Line	Type	Description
90	Warning	Please increase descriptors limit for best performance (1024)
4073	Info	Starting command: \$MGC_HOME/bin/calibre -nowait -rve -drc passgate.drc.re...

Calibre Run Completed Successfully - Results are Valid

DRC Results



LVS Transcript

Calibre Interactive - nmLVS v2024.3..25.13 : ./sunset.calibre.lvs *

File Settings Configurations Help

Rules
LVS completed. CORRECT. See report file: passgate.lvs.report

Inputs
LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 66/67/67 MALLOC = 85/85/85 ELAPSED TIME = 3

II-Cells
--- LVS REPORT FILE = passgate.lvs.report

Outputs
--- CALIBRE - LVS COMPARISON MODULE COMPLETED. TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 2/3/67 MALLOC = 85/85

ERC
--- XDB CROSS REFERENCE DATABASE = ./xdb/passgate.xdb

Signtures

Run Control

Search

Transcript

Files

INFO: Starting command: \$MGC_HOME/bin/calibre -nowait -rve -lvs svdb passgate

RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024

RVE: // Calibre Utility Library v0.10.13-2017-1 Fri Apr 12 08:04:27 PDT 2024

RVE: // Litho Libraries v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024

RVE: //

RVE: // Copyright Siemen 1996-2024

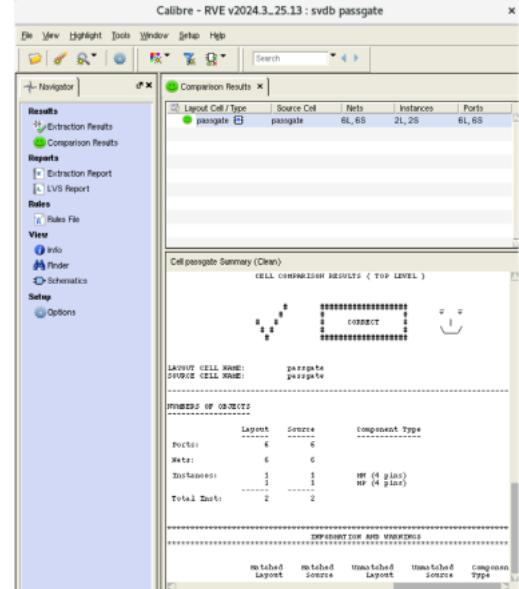
RVE: // All Rights Reserved.

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0 Errors, 1 Warnings, 0 Infos

LVS Comparision Results



PEX Transcript

Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *

```

File Settings Configurations Help
Rules Inputs Outputs LVS Run Control Search Transcript Files
----- PEX NET SUMMARY -----
pbdb file name = svdb/PASSGATE.pbdb
root cell name = PASSGATE
total nets = 6
top-level nets = 6
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0
----- CALIBRE XRC WARNING / ERROR Summary -----
xRC Warnings = 3
xRC Errors = 0
----- CALIBRE XRC FORMATTER COMPLETED - Tue Oct 14 11:08:23 2025 -----
TOTAL CPU TIME = 0 REAL TIME = 0 LVNHEAP = 1576/299 MALLOC = 235/235/264 ELAPSED TIME = 2
*** xRC run finished with exit code 0 ***

```

Run PEX 2205 Start RVE

PEX Netlist Output

Calibre Interactive - PEX v2024.3..25.13 : ./runset.calibre.pex *

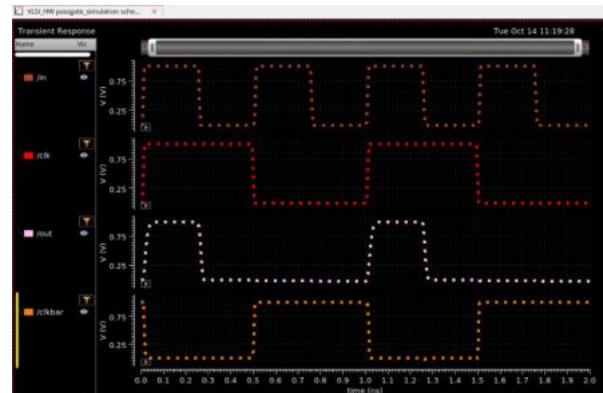
```

File Settings Configurations Help
passgate.pex.netlist *
----- #File: passgate.pex.netlist -----
* Created: Tue Oct 14 11:08:23 2025
* Program: "Calibre xrc"
* Version: "v2024.3..25_13"
* include "passgate.pex.netlist.pex"
* subckt passgate VSS VDD IN CLK CLKBAR OUT
* 
* - OUT - OUT
* - CLKBAR - CLKBAR
* CLK
* IN
* VDD
* VSS
* VSS VDD
* MMIO_N_MMIO_d_N_CLK_MMIO_d_N_OUT_MMIO_d_N_VSS_MMIO_b_MMIO_VTL L=5e-08 W=1e-07
* AD=2.35e-14 AS=1.7e-14 PT=4.8e-07 PS=5.5e-07
* MMIO_N_MMIO_d_N_CLKBAR_MMIO_d_N_OUT_MMIO_d_N_VDD_MMIO_b_MMIO_VTL L=1e-08 W=1e-07
* AD=2.35e-14 AS=1.7e-14 PT=4.8e-07 PS=5.4e-07
*
* include "passgate.pex.netlist.PASSGATE.pex"
*
ends
*

```

Run PEX Start RVE

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```
/home/zeruv/simulation/passgate_simulation/hspiceD/schematic/psf/... x
File Edit View Help cādence
***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# resistors = 18 # capacitors = 43 # inductors = 0
# mutual_inds = 0 # ccvs = 0 # vccs = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 3
# curr_srcs = 0 # diodes = 0 # bjts = 0
# jfets = 0 # mosfets = 4 # U elements = 0
# zl_elements = 0 # elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # VA device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis      time # points tot. iter conv.riter
op point     0.00      1       8
transient    0.00     41     368      151 rev=1
reset        0.01
errchk       0.00
setup        0.00
output       0.00

peak memory used      527.80 megabytes
total cpu time        0.02 seconds
total elapsed time    2.00 seconds
job started at        11:19:25 10/14/2025
job ended   at        11:19:27 10/14/2025

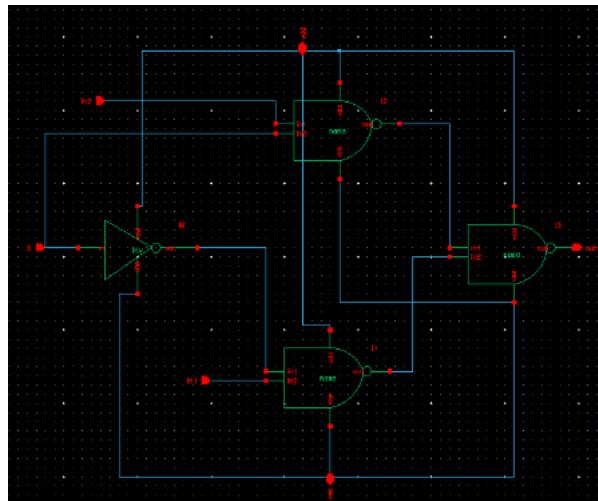
>info: ***** hspice job concluded
>info: job total runtime 2.00 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 1.98(s)
```

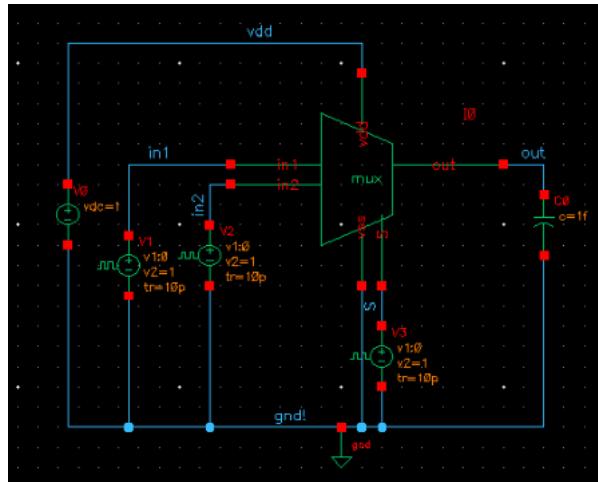
Mux

Required Snapshot Description	Snapshot
-------------------------------	----------

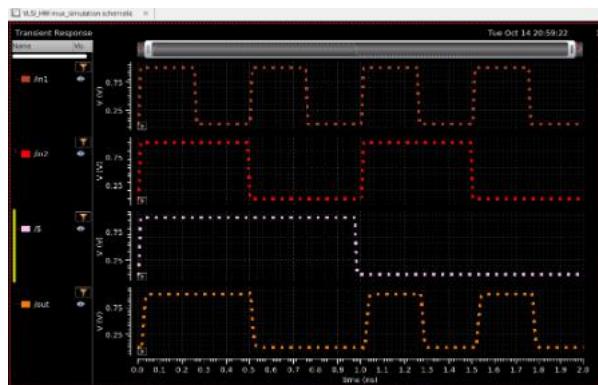
Schematic (Design)



Schematic Simulation Waveform Design



Schematic Simulation Waveform Results



Schematic Simulation Waveform Out Log

```
/home/zeruv/simulation/mux_simulation/hspiceD/schematic/psf/hspi... x
File Edit View Help
cadence

***** PrimeSim HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count : 2
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 68 # elements = 19
# resistors = 0 # capacitors = 1 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vccs = 0
# cccs = 0 # cvcs = 0 # volt_srcs = 4
# curr_srcs = 0 # diodes = 0 # bjt = 0
# fets = 0 # mosfets = 14 # elements = 0
# T elements = 0 # M elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # VA device = 0
# vector_srcs = 0 # N elements = 0

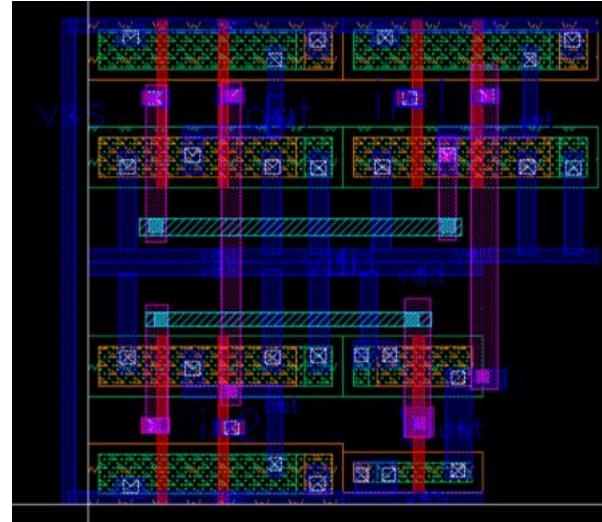
***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv.riter
op point 0.00 1 13
transient 0.02 41 607 234 revs
readin 0.01
errchk 0.01
setup 0.00
output 0.00

peak memory used 527.80 megabytes
total cpu time 0.09 seconds
total elapsed time 2.10 seconds
job started at 20:51:49 10/14/2025
job ended at 20:51:51 10/14/2025

>info: ***** hspice job concluded
job total runtime 2.10 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 2.03(s)
```

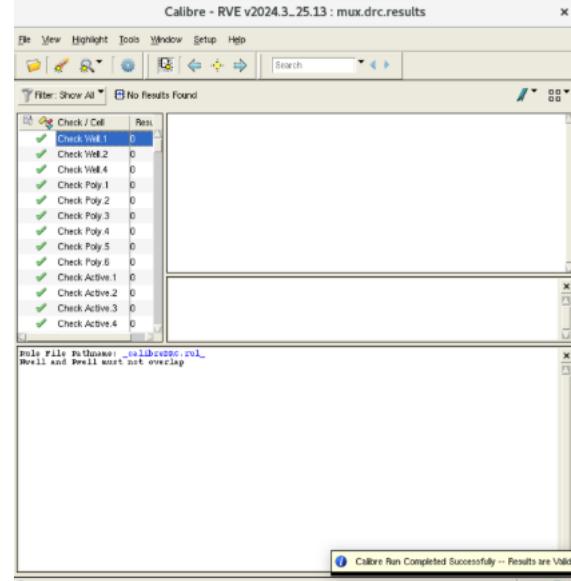
Schematic Layout Design



DRC Transcript

```
Calibre interactive - nmDRC v2024.3_25.13 : ./runset.calibre.drc *
File Settings Configurations Help
TOTAL CPU 1/2
Rules
Inputs
Outputs
Run Control
Search
Transcript
Files
Cumulative RDB Time: CPU = 0 REAL = 0
CALIBRE: DRC-H EXECUTIVE MODULE COMPLETED.. CPU TIME = 0 REAL TIME = 0
TOTAL RESULTS GENERATED = 0 (0)
DRC RESULTS DATABASE FILE = mux.drc.results (ASCII)
CALIBRE: DRC-H COMPLETED - Wed Oct 18 06:13:10 2024
TOTAL CPU TIME = 0 REAL TIME = 2
PROCESSOR COUNT = 1
SUMMARY REPORT FILE = mux.drc.summary
*** DRC run finished with exit code 0 ***
INFO: Starting command: NMIC_HOME/calibre/nmDRC -r -db mux.drc.results
RVE: / Calibre v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: / Calibre Utility Library v0-10_13-2017-1 Fri Apr 12 08:04:27 PDT 2024
RVE: / Litho Library v2024.3_25.13 Thu Aug 1 18:57:13 PDT 2024
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```

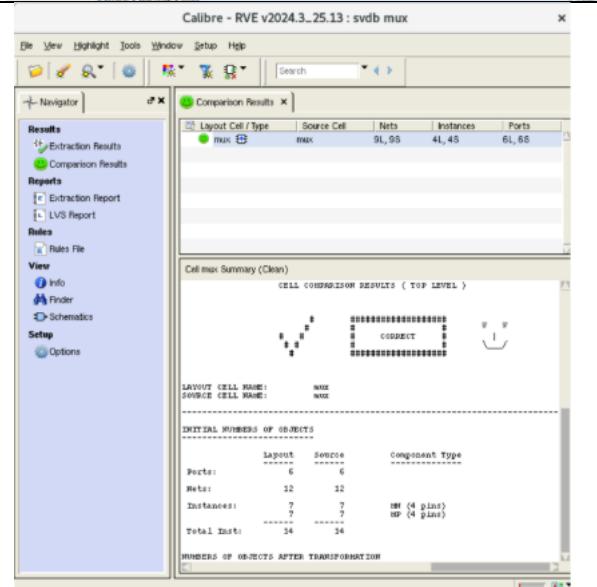
DRC Results



LVS Transcript

```
Calibre Interactive - nmLVS v2024.3..25.13 : ./runset.calibre.lvs *
File Settings Configurations Help TOTAL CPU 2/2
Rules Inputs LVS completed. CORRECT. See report file: mux.lvs.report.
H-Cells Outputs -- LVS REPORT FILE = mux.lvs.report
Outputs -- LVS REPORT FILE = mux.lvs.report
-- CALIBRE-LVS COMPARISON MODULE COMPLETED. TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 2/569 MALLOC = 86/898 ELAPSED TIME = 3
-- XDB CROSS REFERENCE DATABASE = svbmxmx.xdb
-- SPICE NETLIST FILE = mux.sp
-- CIRCUIT TRANSACTION REPORT FILE = mux.lvs.report.est
-- PERIODIC REPORT FILE = mux.lvs.report.phd
-- QUERY DATABASE = svbmxmx.TOP CELL = mux
-- GRAND TOTAL NON-HYBRID/LVS COMMANDS CPU TIME = 0 REAL TIME = 3 LVHEAP = 69 MALLOC = 97
*** LVS run finished with exit code 0 ***
INFO: Starting command: SMIC_HOME/calibre/runset -rue -lvs svbmx
RVE: // Calibre v2024.3..25.13 Thu Aug 1 18:57:13 PDT 2024
RVE: // Calibre Utility Library v6-10_13-2017.1 Fri Apr 12 08:04:27 PDT 2024
RVE: // Lttm Libraries v2024.3..25.13 Thu Aug 1 18:57:19 PDT 2024
RVE: //
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RVE: //
```

LVS Comparision Results



PEX Transcript

The screenshot shows the Calibre Interactive interface with the following details:

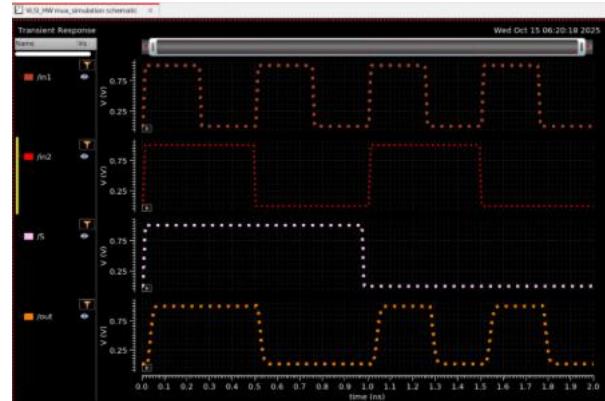
- File**, **Settings**, **Configurations**, **Help** menu items.
- Search** bar.
- Run Control** tab selected.
- Rules**, **Inputs**, **Outputs**, **LVS**, **Search**, **Calibration** buttons.
- Files** dropdown menu.
- POB NET SUMMARY** table:

pdfl file name =	svrlMLX.pdb
root Cell name =	RUX
total nets =	12
top-level nets =	9
loop-level nets =	0
designed nets =	3
merged nets =	0
error nets =	0
- CALIBRE xRC WARNING / ERROR Summary** table:

xrc Warnings =	3
xrc Errors =	0
- CALIBRE xRC: FORMATTER COMPLETED - Wed Oct 15 06:16:16 2025**
- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 15/76/299 MALLOC = 264/264/264 ELAPSED TIME = 2**
- 2248*** xRC run finished with exit code 0 *****
- 8 Errors, 10 Warnings, 1 Info** status message.

PEX Netlist Output

Post-Layout Simulation Results



Post-Layout Simulation Out Log

```

home/zeruv/simulation/mux_simulation/hspiceD/schematic/psf/hspiceD.sch : cadence
***** PrimeSim HSPICE Threads Information *****
File Edit View Help
***** Circuit Statistics *****
# nodes = 213 # elements = 480
# resistors = 150 # capacitors = 312 # inductors = 0
Available CPU Count : 2
Actual Threads Count : 1
# mutual_inds = 0 # vccs = 0 # vccs = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 4
# curr_srcs = 0 # diodes = 0 # bjt = 0
# jfets = 0 # mosfets = 14 # U elements = 0
# T elements = 0 # M elements = 0 # B elements = 0
# 3 elements = 0 # N elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis      time    # points tot. iter conv.riter
op point     0.00        1       26
transient    0.03        41      515      200 revs
readin       0.01
errchk       0.00
setup        0.00
output       0.00

peak memory used      527.80 megabytes
total cpu time        0.05 seconds
total elapsed time    2.02 seconds
job started at        06:20:18 10/15/2025
job ended at          06:20:18 10/15/2025

info:      **** hspice job concluded
job total runtime      2.02 seconds

lic: Release hspice token(s)
lic: total license checkout elapse time: 1.97(s)

```

References

- Kyung-Ju Cho, Kwang-Chul Lee, Jin-Gyun Chung and K. K. Parhi, "Design of low-error fixed-width modified booth multiplier," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 5, pp. 522-531, May 2004,
doi: 10.1109/TVLSI.2004.825853.