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ECE 4435: Lab Report 11

How it works:

The memory and writeback stages interact with main memory and the register file respectively. The writeback stage is simple and just stores the data for a cycle before passing it to the register file. The memory stage uses a 2-bit control vector to determine whether to do nothing, write to memory, pass the data to writeback stage, or read from memory and pass that to the writeback stage. I also pass out a stall signal to all previous stages based on the mdelay signal coming back from memory.

How I tested it:

I tested these stages by hooking them up to my existing combination of decode and execute stages and ran one of each opcode type through the architecture to ensure that the results were as expected. I took care not to induce any hazards when sending the commands because I still need to implement anti-hazard measures. I ran both JMP and JAL through because they have different effects on the register file. The same was applied to LIL and LIH.