EE 316 Lab 6 Cover Sheet

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Section: 16050

Design Problem: 10.6 and 17.F

Part 1:

1. Block Diagram and VHDL code
2. Snapshot of output waveform with given inputs

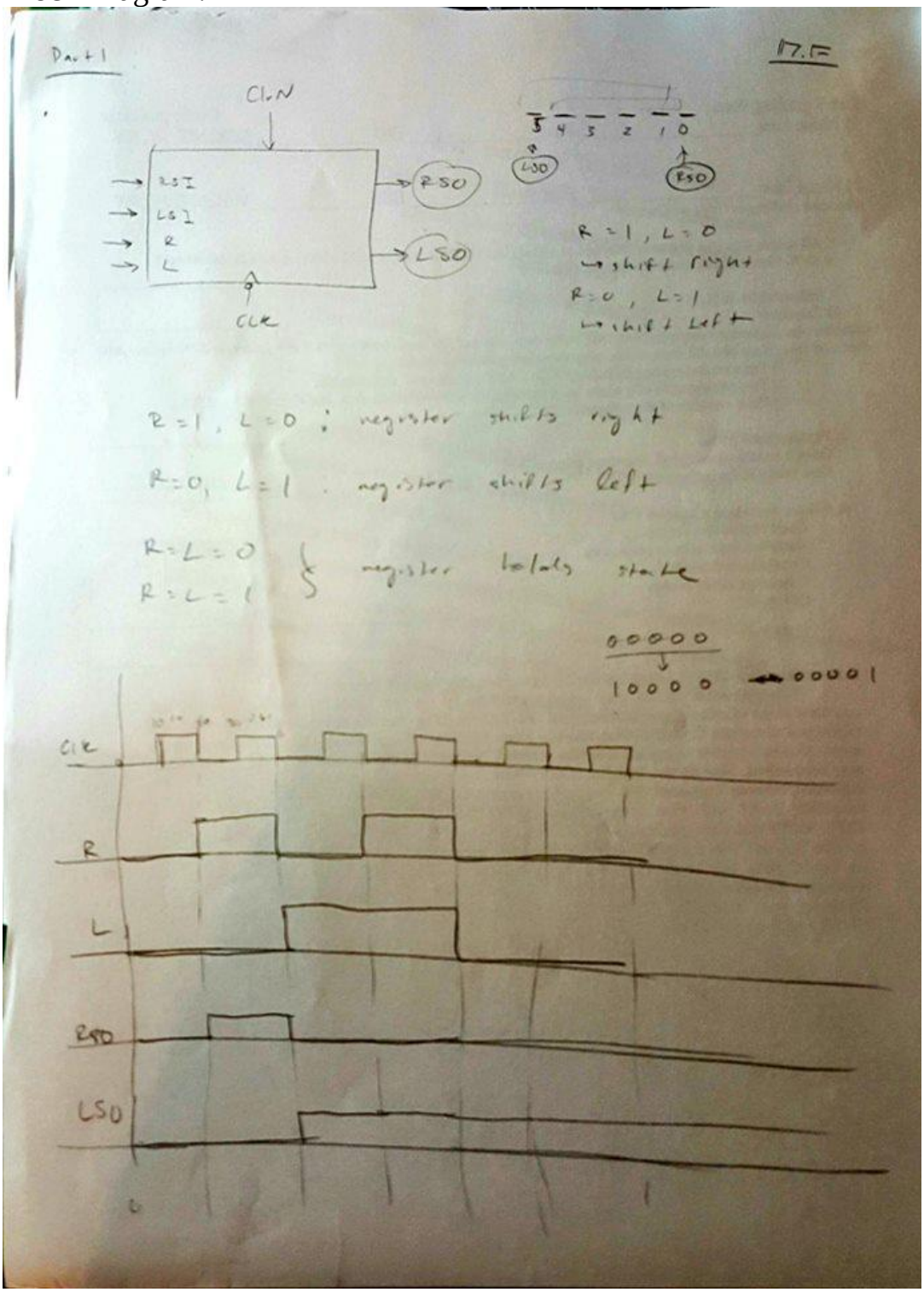
Part 2:

3. VHDL code
4. Snapshot of output waveform with the same test inputs used in Lab 5

Signatures of the TA:

1. Block Diagram and VHDL code

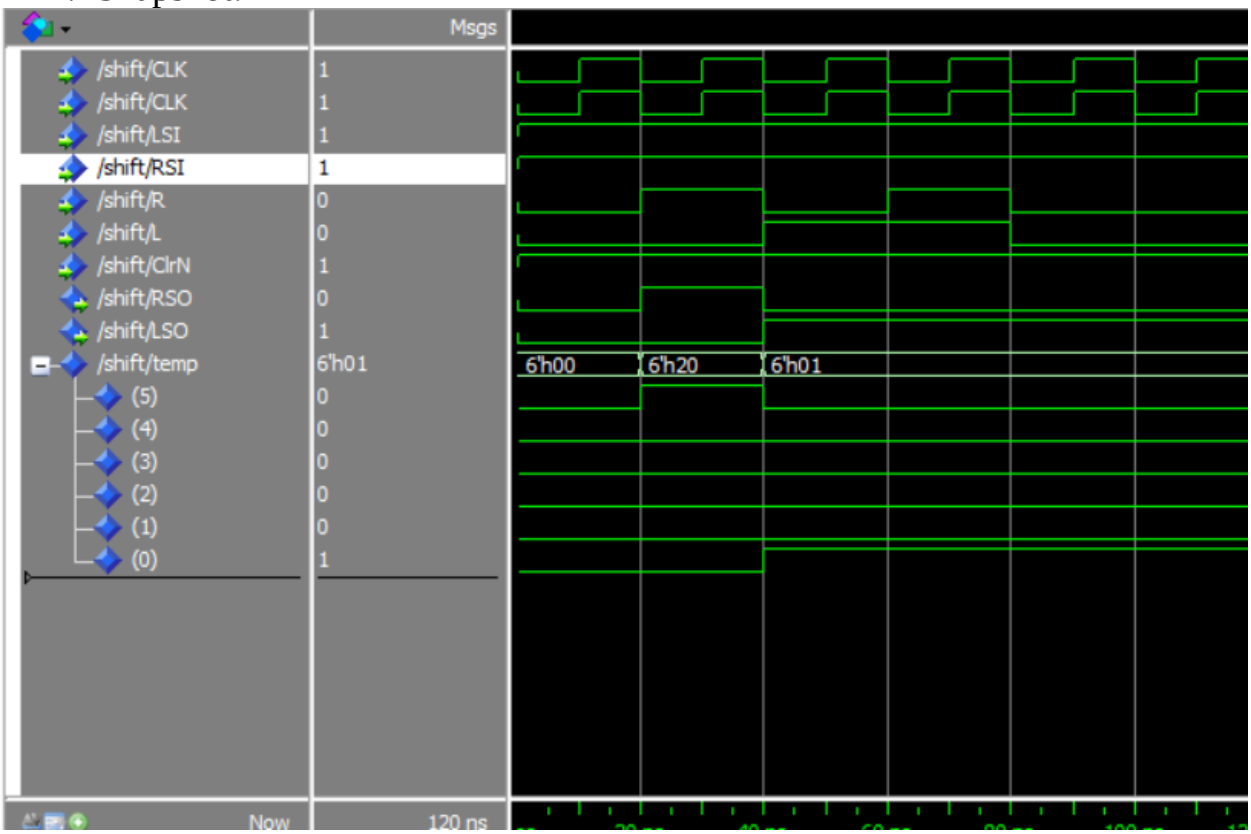
Block Diagram:



VHDL:

```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;

Entity shift is
    Port(CLK, LSI, RSI, R, L, ClrN: in std_logic;
        RSO, LSO: out std_logic);
End shift;

Architecture shiftarch of shift is
    signal temp: std_logic_vector(5 downto 0) := (Others => '0');
--    if(ClrN = '0') then
--        temp <= 0;
--    end if;
    begin
        process(CLK, ClrN)
            begin
                if(ClrN = '0') then
                    temp <= (others => '0');
                elsif(CLK'event and CLK = '1') then
                    if(R = '1' and L = '0') then
                        temp <= RSI & temp(5 downto 1);
                    elsif(R = '0' and L = '1') then
                            temp <= temp(4 downto 0) & LSI;
                    end if;
                end if;
        end process;
     RSO <= temp(5);
     LSO <= temp(0);
 end shiftarch;
```

2. Snapshot:


Msgs
/shift/CLK
/shift/CLK
/shift/LSI
/shift/RSI
/shift/R
/shift/L
/shift/ClrN
/shift/RSO
/shift/LSO
/shift/temp
(5)
(4)
(3)
(2)
(1)
(0)
1
1
1
1
0
0
1
0
1
6'h01
0
0
0
0
0
1
6'h00
6'h20
6'h01
Now
120 ns

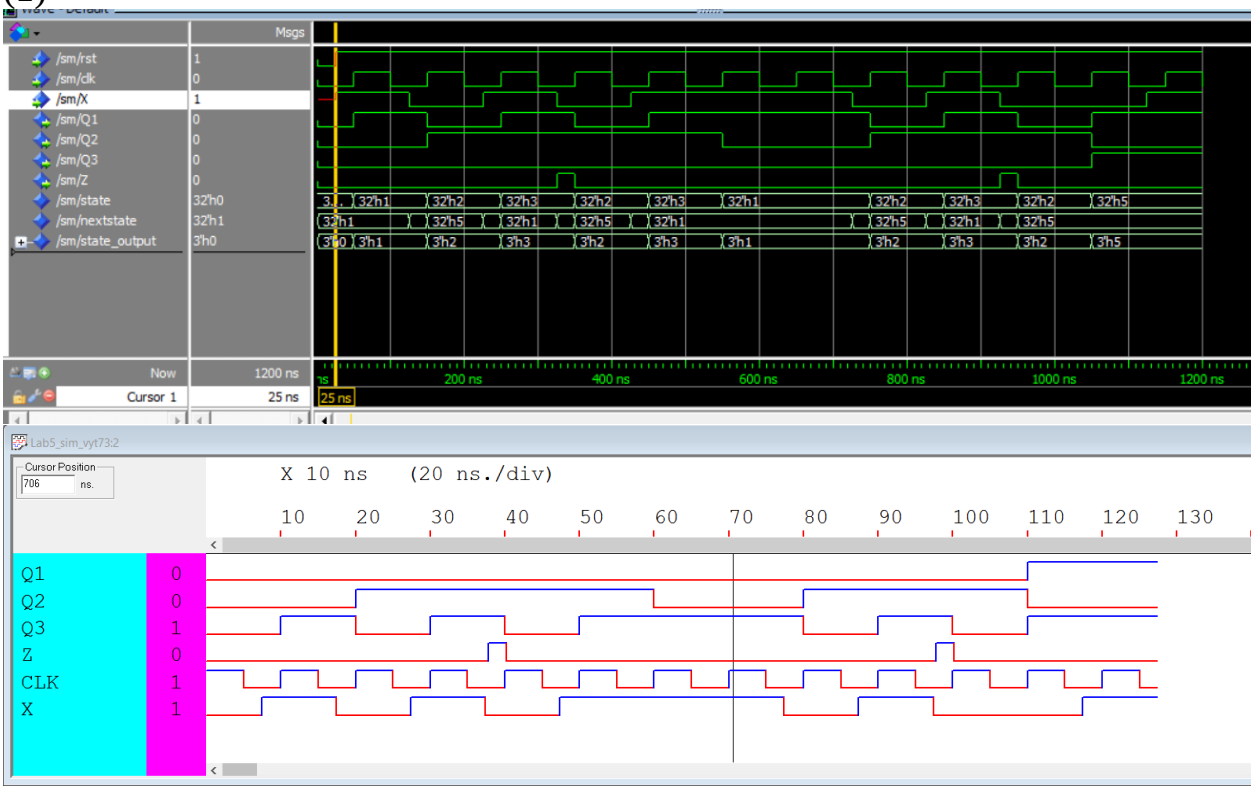
3. VHDL Code:

```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;

entity SM is
	Port(rst, clk, X: in std_logic;
		Q1, Q2, Q3, Z: out std_logic);
end SM;

architecture archsm of sm is
	signal state, nextstate: integer range 0 to 5 := 0;
	signal state_output: std_logic_vector(2 downto 0);

begin
	state_output <= conv_std_logic_vectOr(state, 3);
		Q3 <= state_output(2);
		Q2 <= state_output(1);
		Q1 <= state_output(0);

	process(state, X)
	begin
		case State is
			when 0 =>
				if X = '0' then Z<= '0'; nextstate <= 4;
				else Z <= '0'; nextstate <= 1; end if;
			when 1 =>
				if X = '0' then Z<= '0'; nextstate <= 2;
				else Z <= '0'; nextstate <= 1; end if;
			when 2 =>
				if X = '0' then Z<= '0'; nextstate <= 5;
				else Z <= '0'; nextstate <= 3; end if;
			when 3 =>
				if X = '0' then Z<= '1'; nextstate <= 2;
				else Z <= '0'; nextstate <= 1; end if;
			when 4 =>
				if X = '0' then Z<= '0'; nextstate <= 5;
				else Z <= '0'; nextstate <= 1; end if;
			when 5 =>
				if X = '0' then Z<= '0'; nextstate <= 5;
				else Z <= '0'; nextstate <= 5; end if;
		end case;
	end process;

	process(clk, rst)
	begin
		if (rst = '0') then
			state <= 0;
		elsif clk'event and clk = '1' then  --rising edge
			state <= nextstate;
		end if;
	end process;

end archsm;
```

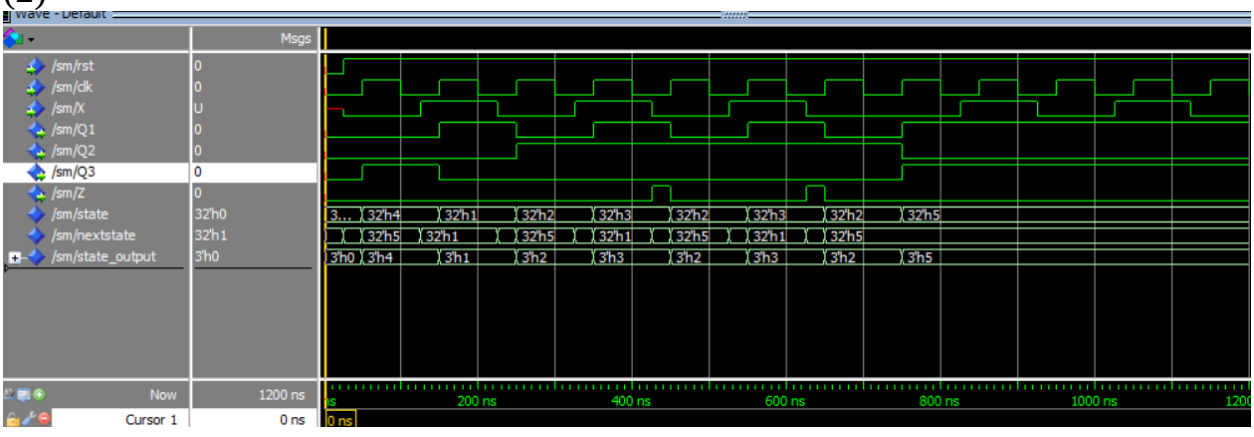
4. Snapshots:

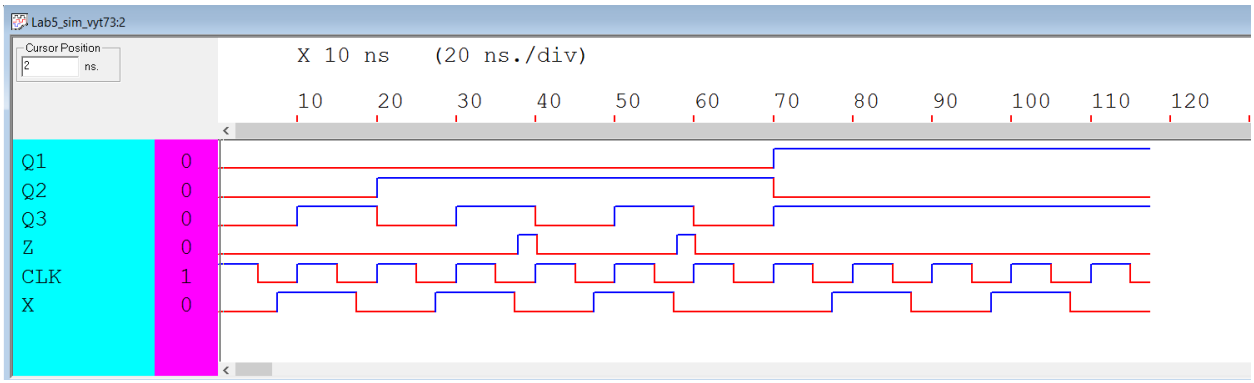
(1) X = 1 0 1 0 1 1 1 0 1 0 0 1
Z = 0 0 0 1 0 0 0 0 0 1 0 0
(2) X = 0 1 0 1 0 1 0 0 1 0 1 0
Z = 0 0 0 0 1 0 1 0 0 0 0 0

(1)



(2)




Lab5_sim_vyt73:2
Cursor Position
2
ns.
X 10 ns (20 ns./div)
10 20 30 40 50 60 70 80 90 100 110 120
Q1 0
Q2 0
Q3 0
Z 0
CLK 1
X 0