EE 316 Lab 5.1 Cover Sheet

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Section: 16050

Design Problem: 10.6

Attachment checklist:

1. Coversheet for Lab 5.1
2. Preparatory Questions & Answers
3. State graph and table, K-maps, and equations (by hand)
4. Printout of state table and verification window (*Print All* command in LogicAid)

5-1. A state assignment (by hand)

5-2. Printout of two different state assignments (5-1 and another) in LogicAid

6. Transition table determined from the SimUaid simulation (by hand)
7. Output sequences for Z under two different input sequences
8. Printout of waveforms in landscape mode (scaled to 20ns/div)
9. Printout of SimUAid circuit (with minimum no. of gates)

(Before submission, you should save/remember all your Lab 5.1 work for Lab 6.2)

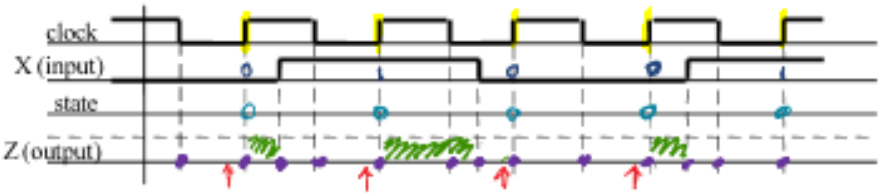
Signatures of the TA:

2. Preparatory Questions & Answers

Preparatory Questions of Lab 5

a. The graph given below represents a timing diagram for a Mealy sequential circuit. Assume that the flip-flops in the circuit are D flip-flops which change state on the **rising edge** of the clock pulse.

- Circle the points on the state axis at which the flip-flops could change state.
- Circle the points on the Z axis at which Z could change.
- A "false" output can occur after the flip-flops have changed state but before the input X has changed to the next value. Shade the spaces on the Z part of the diagram during which false outputs could occur.



When using the simulator, a switch will be used to generate the clock pulse. In the laboratory, a push-button will be used. When the button is depressed, the clock goes to 1, and when it is released, the clock goes to 0. Answer the following questions, keeping in mind that the flip-flops we are using trigger on the **rising edge** of the clock pulse:

b. Will the flip-flops change state when the clock switch is changed from 0 to 1, or from 1 to 0? 0 to 1

c. Will the output of the above Mealy circuit always be correct after the clock switch goes from 0 to 1?
No Explain: the state can change before the input, resulting in a false output

d. Will the Mealy circuit output always be correct after the input has been changed and before the clock switch is changed from 0 to 1? yes

e. Should you read the output for the first time before or after the first rising edge of the clock pulse? before

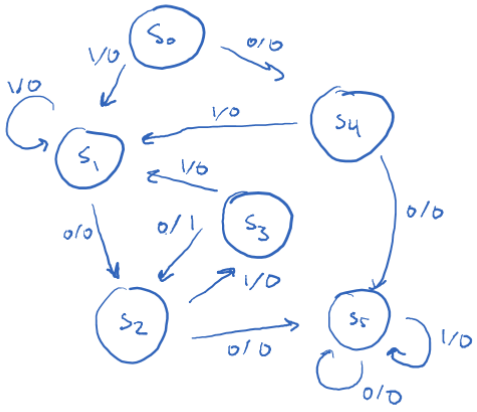
f. On the above timing diagram, draw arrows to indicate the times to read the Z output.

g. For a Mealy circuit, which of the two sequences given below will give the correct output:

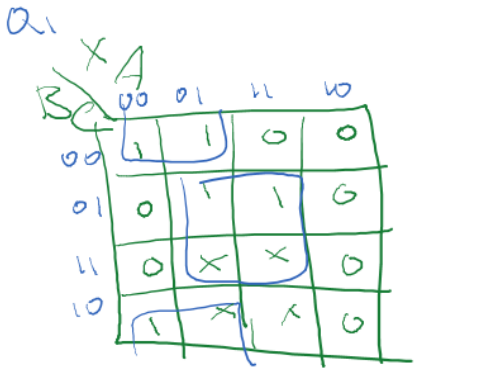
A: 1. Set the input value
2. Clock the circuit
3. Read the output

B: 1. Set the input value
2. Read the output
3. Clock the circuit

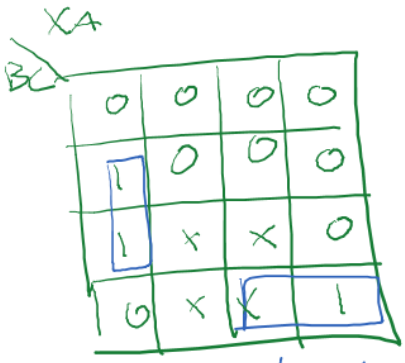
3. State graph and table, K-maps, and equations (by hand)



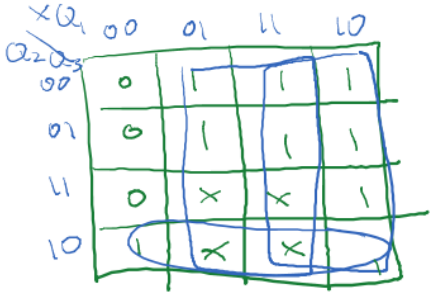
Present	Next State x=0	Next State x=1	Output x=0	Output x=1
S_0	S_4	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_5	S_3	0	0
S_3	S_2	S_1	1	0
S_4	S_5	S_1	0	0
S_5	S_5	S_5	0	0



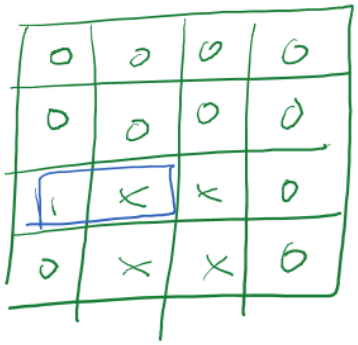
$Q_1 = X'Q_3' + Q_1Q_3$



$Q_2 = X'Q_1'Q_3' + XQ_2Q_3'$



$Q_3 = X + Q_1 + Q_2Q_3'$



$Z = X'Q_2Q_3$

4. Printout of state table and verification window (*Print All* command in LogicAid)

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LogicAid, 2nd Ed.        Name: Vivian                    Modified: 04/06/16 18:30:55

*** State_Table: State_Table2                                              Page 1

PS   NS       OUTPUTs*  INPUT-VARs

     0  1     0 1       X1
_____________________________________
s0   s4 s1    0 0
s1   s2 s1    0 0
s2   s5 s3    0 0
s3   s2 s1    1 0
s4   s5 s1    0 0
s5   s5 s5    0 0


_____________________________________
*  Z1


*** Output: State_Table2_C
     Test State Table Title:
     Solution State Table Title:  C:\Users\Vivian\Documents\UT\Spring 2016\EE
316\Labs\Lab5\LogicCheckers\16-6.aid

     ***** Correct State Table *****
```

5-1. A state assignment (by hand)

Present	Next State x=0	Next State x=1	Output x=0	Output x=1
S_0 000	S_4 100	S_1 001	0	0
S_1 001	S_2 010	S_1 001	0	0
S_2 010	S_5 101	S_3 011	0	0
S_3 011	S_2 010	S_1 001	1	0
S_4 100	S_5 101	S_1 001	0	0
S_5 101	S_5 101	S_5 101	0	0

5-2. Printout of two different state assignments (5-1 and another) in LogicAid

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LogicAid, 2nd Ed.        Name: Vivian                        Modified: 04/06/16 19:56:37

*** State_Table: State_Table10                                                  Page 1

ASSIGN   PS   NS       OUTPUTs*  INPUT-VARs

              0  1     0 1       X1
_____________________________________________
000      s0   s4 s1    0 0
001      s1   s2 s1    0 0
010      s2   s5 s3    0 0
011      s3   s2 s1    1 0
100      s4   s5 s1    0 0
101      s5   s5 s5    0 0

_____________________________________________
*  Z1


*** Output: State_Table10_O

     Simplification Routine:  PI Chart

D(Q1)  =  X1'Q3' + Q1 Q3

     Input Cost = 6           Gate Cost  = 3

D(Q2)  =  X1'Q1'Q3 + X1 Q2 Q3'

     Input Cost = 8           Gate Cost  = 3

D(Q3)  =  X1 + Q2 Q3' + Q1

     Input Cost = 5           Gate Cost  = 2

Z1  =  X1'Q2 Q3

     Input Cost = 3           Gate Cost  = 1


      ***Total Input Cost = 22***
      ***Total Gate  Cost = 9***


*** Output: State_Table10_C
     Test State Table Title:
     Solution State Table Title:  C:\Users\Vivian\Documents\UT\Spring 2016\EE
316\Labs\Lab5\LogicCheckers\16-6.aid

     ***** Correct State Table *****
```

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LogicAid, 2nd Ed.        Name: Vivian                    Modified: 04/06/16 19:48:48

*** State_Table: State_Table2                                          Page 1

ASSIGN    PS    NS       OUTPUTs*  INPUT-VARs

              0  1       0 1       X1
_____________________________________________
000       s0    s4 s1    0 0
001       s1    s2 s1    0 0
100       s2    s5 s3    0 0
010       s3    s2 s1    1 0
011       s4    s5 s1    0 0
101       s5    s5 s5    0 0


_____________________________________________
*  Z1

*** Output: State_Table2_O

     Simplification Routine:  PI Chart

D(Q1)  =  X1'Q3 + X1'Q1 + X1'Q2 + Q1 Q3

     Input Cost = 12          Gate Cost  = 5

D(Q2)  =  X1'Q1'Q2'Q3' + X1 Q1 Q3'

     Input Cost = 9           Gate Cost  = 3

D(Q3)  =  Q2 Q3 + X1 Q1' + X1'Q2'Q3' + Q1 Q3

     Input Cost = 13          Gate Cost  = 5

Z1  =  X1'Q2 Q3'

     Input Cost = 3           Gate Cost  = 1

      ***Total Input Cost = 37***
      ***Total Gate  Cost = 14***


*** Output: State_Table2_C
     Test State Table Title:
     Solution State Table Title:  C:\Users\Vivian\Documents\UT\Spring 2016\EE
316\Labs\Lab5\LogicCheckers\16-6.aid

     ***** Correct State Table *****
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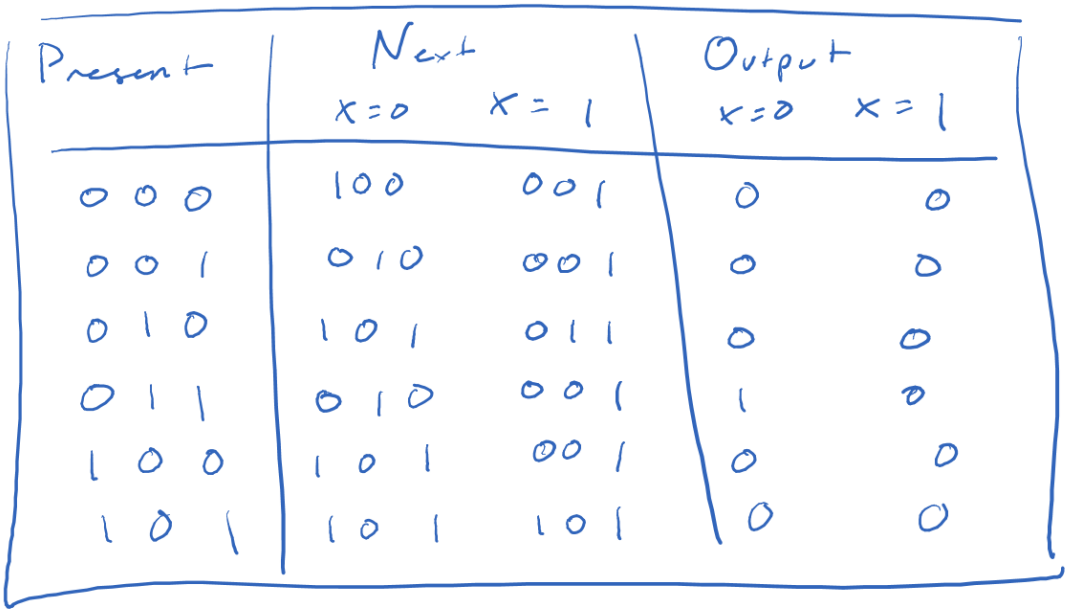
6. Transition table determined from the SimUaid simulation (by hand)



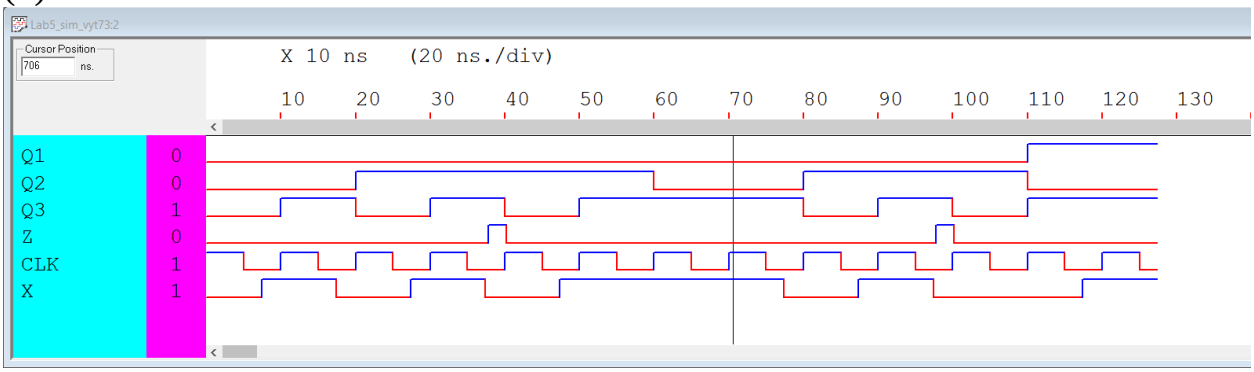
7. Output sequences for Z under two different input sequences

(1) X = 1 0 1 0 1 1 1 0 1 0 0 1
Z = 0 0 0 1 0 0 0 0 0 1 0 0

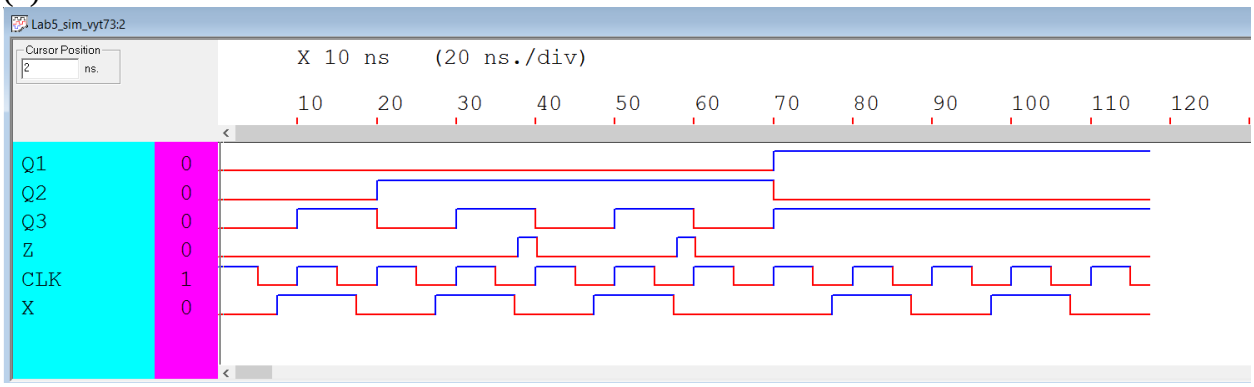
(2) X = 0 1 0 1 0 1 0 0 1 0 1 0
Z = 0 0 0 0 1 0 1 0 0 0 0 0

8. Printout of waveforms in landscape mode (scaled to 20ns/div)

(1)



(2)



9. Printout of SimUAid circuit (with minimum no. of gates)
(Before submission, you should save/remember all your Lab 5.1 work for Lab 6.2)