ST7735S

132RGB x 162dot 262K Color with Frame Memory Single-Chip TFT Controller/Driver

Datasheet

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LIST OF CONTENT

1 GENERAL DESCRIPTION 10
2 FEATURES 10
3 PAD ARRANGEMENT 12
3.1 Output Bump Dimension 12
3.2 Input Bump Dimension 13
3.3 Alignment Mark Dimension 14
3.4 Chip Information 15
4 PAD CENTER COORDINATES 16
5 BLOCK DIAGRAM 22
6 PIN DESCRIPTION 23
6.1 Power Supply Pin 23
6.2 Interface Logic Pin 23
6.3 Mode Selection Pin 25
6.4 Driver Output pins 26
6.5 Test Pins 27
7 DRIVER ELECTRICAL CHARACTERISTICS 28
7.1 Absolute Operation Range 28
7.2 DC Characteristic 29
7.3 Power Consumption 30
8 Timing chart 31
8.1 Parallel Interface Characteristics: 18, 16, 9 or 8-bit Bus (8080 Series MCU Interface) 31
8.2 Parallel Interface Characteristics: 18, 16, 9 or 8-bit Bus (6800 Series MCU Interface) 33
8.3 Serial Interface Characteristics (3-line Serial) 35
8.4 Serial Interface Characteristics (4-line Serial) 36
9 Function Description 37
9.1 Interface Type Selection 37
9.2 8080-series MCU Parallel Interface (P68 = '0') 38
9.2.1 Write Cycle Sequence 39
9.2.2 Read Cycle Sequence 40
9.3 6800-series MCU Parallel Interface (P68 = '1') 41
9.3.1 Write Cycle Sequence 42
9.3.2 Read Cycle Sequence 43
9.4 Serial Interface 44
9.4.1 Command Write Mode 44
9.4.2 Read Functions 46

9.4.3 3-line Serial Protocol 46
9.4.4 4-line Serial Protocol 47
9.5 Data Transfer Break and Recovery....48
9.6 Data Transfer Pause....50
9.6.1 Serial Interface Pause 50
9.6.2 Parallel Interface Pause 50
9.7 Data Transfer Modes 51
9.7.1 Method 1....51
9.7.2 Method 2....51
9.8 Data Color Coding 52
9.8.1 8-bit Parallel Interface (IM2, IM1, IM0= “100”)....52
9.8.2 8-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH= “03h”....52
9.8.3 8-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH= “05h”....53
9.8.4 8-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH= “06h”....54
9.8.5 16-Bit Parallel Interface (IM2,IM1, IM0= “101”)....55
9.8.6 16-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH= “03h”....55
9.8.7 16-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH= “05h”....56
9.8.8 16-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH= “06h”....57
9.8.9 9-Bit Parallel Interface (IM2, IM1, IM0=“110”) 58
9.8.10 Write 9-bit Data for RGB 6-6-6-bit Input (262k-color)....58
9.8.11 18-Bit Parallel Interface (IM2, IM1, IM0=“111”)....59
9.8.12 18-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH=“03h”....59
9.8.13 18-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH=“05h”....60
9.8.14 18-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH=“06h”....61
9.8.15 3-line Serial Interface....62
9.8.16 Write Data for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH=“03h” 62
9.8.17 Write Data for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH=“05h” 63
9.8.18 Write Data for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH=“06h” 64
9.8.19 4-line Serial Interface....65
9.8.20 Write Data for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH=“03h” 65
9.8.21 Write Data for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH=“05h” 66
9.8.22 Write Data for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH=“06h” 66
9.9 Display Data RAM....67
9.9.1 Configuration (GM[1:0] = “00”)....67
9.9.2 Memory to Display Address Mapping....68
9.9.3 When using 128RGB x 160 resolution (GM[1:0] = “11”, SMX=SMY=SRGB= ‘0’) 68
9.9.4 When using 132RGB x 132resolution (GM[1:0] = “01”, SMX=SMY=SRGB= ‘0’) 69
9.9.5 When using 132RGB x 162 resolution (GM[1:0] = “00”, SMX=SMY=SRGB= ‘0’) 70

9.9.6 Normal Display On or Partial Mode On 71
9.9.7 When using 128RGB x 160 resolution (GM[1:0] = “11”) 71
9.9.8 When using 128RGB x 160 resolution (GM[1:0] = “01”) 72
9.9.9 When using 132RGB x 162 resolution (GM[1:0] = “00”) 73
9.10 Address Counter 74
9.11 Memory Data Write/ Read Direction 75
9.11.1 When 128RGBx160 (GM= “11”) 75
9.11.2 When 132RGBx132 (GM= “01”) 75
9.11.3 When 132RGBx162 (GM= “00”) 76
9.11.4 Frame Data Write Direction According to the MADCTL Parameters (MV, MX and MY) 77
9.11.5 Scroll Address Circuit 78
9.11.6 Vertical Scroll Mode 78
9.11.7 Vertical Scroll Example 79
9.11.8 Case 1: TFA + VSA + BFA<162 79
9.11.9 Case 2: TFA + VSA + BFA=162 (Rolling Scrolling) 80
9.12 Tearing Effect Output Line 81
9.12.1 Tearing Effect Line Modes 81
9.12.2 Tearing Effect Line Timings 82
9.12.3 Example 1: MPU Write is faster than panel read 83
9.12.4 Example 2: MPU Write is slower than panel read 84
9.13 Power ON/OFF Sequence 85
9.13.1 Uncontrolled Power Off 86
9.14 Power Level Definition 87
9.14.1 Power Level 87
9.14.2 Power Flow Chart 88
9.15 Reset Table 89
9.15.1 Reset Table(Default Value, GM[1:0]=“11”, 128RGB x 160) 89
9.15.2 Reset Table (GM[1:0]= “01”, 132RGB x 132) 90
9.15.3 Reset Table (GM[1:0]= “00”, 132RGB x 162) 91
9.16 Module Input/Output Pins 92
9.16.1 Output or Bi-directional (I/O) Pins 92
9.17 Reset Timing 93
9.18 Color Depth Conversion Look Up Tables 94
9.18.1 65536 Color to 262,144 Color 94
9.18.2 4096 Color to 262,144 Color 98
9.19 Sleep Out-Command and Self-Diagnostic Functions of the Display Module 100
9.19.1 Register Loading Detection 100
9.19.2 Functionality Detection 101

9.19.3 Chip Attachment Detection (Optional) 102
9.19.4 Display Glass Break Detection (Optional) 103
10 COMMAND 104
10.1 System Function Command List and Description 104
10.1.1 NOP (00h) 107
10.1.2 SWRESET (01h): Software Reset 108
10.1.3 RDDID (04h): Read Display ID 109
10.1.4 RDDST (09h): Read Display Status 110
10.1.5 RDDPM (0Ah): Read Display Power Mode 112
10.1.6 RDDMADCTL (0Bh): Read Display MADCTL 113
10.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format 114
10.1.8 RDDIM (0Dh): Read Display Image Mode 115
10.1.9 RDDSM (0Eh): Read Display Signal Mode 116
10.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result 118
10.1.11 SLPIN (10h): Sleep In 119
10.1.12 SLPOUT (11h): Sleep Out 120
10.1.13 PTLON (12h): Partial Display Mode On 121
10.1.14 NORON (13h): Normal Display Mode On 122
10.1.15 INVOFF (20h): Display Inversion Off 123
10.1.16 INVON (21h): Display Inversion On 124
10.1.17 GAMSET (26h): Gamma Set 125
10.1.18 DISPOFF (28h): Display Off 126
10.1.19 DISPON (29h): Display On 127
10.1.20 CASET (2Ah): Column Address Set 128
10.1.21 RASET (2Bh): Row Address Set 130
10.1.22 RAMWR (2Ch): Memory Write 132
10.1.23 RGBSET (2Dh): Color Setting for 4K, 65K and 262K 133
10.1.24 RAMRD (2Eh): Memory Read 134
10.1.25 PTLAR (30h): Partial Area 135
10.1.26 SCRLAR (33h): Scroll Area Set 137
10.1.27 TEOFF (34h): Tearing Effect Line OFF 139
10.1.28 TEON (35h): Tearing Effect Line ON 140
10.1.29 MADCTL (36h): Memory Data Access Control 142
10.1.30 VSCSAD: Vertical Scroll Start Address of RAM (37h) 145
10.1.31 IDMOFF (38h): Idle Mode Off 147
10.1.32 IDMON (39h): Idle Mode On 148
10.1.33 COLMOD (3Ah): Interface Pixel Format 150
10.1.34 RDID1 (DAh): Read ID1 Value 151

10.1.35 RDID2 (DBh): Read ID2 Value....152
10.1.36 RDID3 (DCh): Read ID3 Value....154
10.2 Panel Function Command List and Description....155
10.2.1 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)....159
10.2.2 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)....160
10.2.3 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)....161
10.2.4 INVCTR (B4h): Display Inversion Control....162
10.2.5 PWCTR1 (C0h): Power Control 1....163
10.2.6 PWCTR2 (C1h): Power Control 2....165
10.2.7 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)....167
10.2.8 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)....169
10.2.9 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)....171
10.2.10 VMCTR1 (C5h): VCOM Control 1....173
10.2.11 VMOFCTR (C7h): VCOM Offset Control....175
10.2.12 WRID2 (D1h): Write ID2 Value....177
10.2.13 WRID3 (D2h): Write ID3 Value....178
10.2.14 NVFCTR1 (D9h): NVM Control Status....179
10.2.15 NVFCTR2 (DEh): NVM Read Command....180
10.2.16 NVFCTR3 (DFh): NVM Write Command....181
10.2.17 GMCTRP1 (E0h): Gamma (‘+’polarity) Correction Characteristics Setting....182
10.2.18 GMCTRN1 (E1h): Gamma ‘-’polarity Correction Characteristics Setting....184
10.2.19 GCV(FCh): Gate Pump Clock Frequency Variable....186
11 Power Sturcture....187
11.1 Driver IC Operating Voltage Specification....187
11.2 Power Booster Circuit....188
12 Gamma Structure....189
12.1 Structure of Grayscale Amplifier....189
12.2 Gamma Voltage Formula (Positive/ Negative Polarity)....190
13 Example Connection with Panel Direction and Different Resolution 192
13.1 Application of Connection with Panel Direction....192
13.2 Application of Connection with Different Resolution....194
13.3 Microprocessor Interface Applications....197
13.3.1 8080-Series MCU Interface for 8-bit Data Bus (P68=0, IM2, IM1, IM0=”100”)....197
13.3.2 8080-Series MCU Interface for 16-bit Data Bus (P68=0, IM2, IM1, IM0=”101”)....197
13.3.3 8080-Series MCU Interface for 9-bit Data Bus (P68=0, IM2, IM1, IM0=”110”)....197
13.3.4 8080-Series MCU Interface for 18-bit Data Bus (P68=0, IM2, IM1, IM0=”111”)....198
13.3.5 6800-Series MCU Interface for 8-bit Data Bus (P68=1, IM2, IM1, IM0=”100”)....198

13.3.6 6800-Series MCU Interface for 16-bit Data Bus (P68=1, IM2, IM1, IM0=”101”).....198
13.3.7 6800-Series MCU Interface for 9-bit Data Bus (P68=1, IM2, IM1, IM0=”110”).....199
13.3.8 6800-Series MCU Interface for 18-bit Data Bus (P68=1, IM2, IM1, IM0=”111”).....199
13.3..9 3-Line Serial MCU Interface (IM2, IM1, IM0=”000”, SPI4W=0) 199
13.3.10 4-Line Serial MCU Interface (IM2, IM1, IM0=”000”, SPI4W=1) 200
14 Revision History 201

LIST OF FIGURES

Figure 1 Parallel interface timing characteristics (8080 series MCU interface)....31
Figure 2 Rising and falling timing for input and output signal....32
Figure 3 Chip selection (CSX) timing....32
Figure 4 Write-to-read and read-to-write timing....32
Figure 5 Parallel Interface Timing Characteristics (6800-Series MCU Interface)....33
Figure 6 3-line serial interface timing....35
Figure 7 4-line serial interface timing....36
Figure 8 8080-series WRX protocol....39
Figure 9 8080-series parallel bus protocol, write to register or display RAM....39
Figure 10 8080-series RDX protocol....40
Figure 11 8080-series parallel bus protocol, read data from register or display RAM....40
Figure 12 6800-Series Write Protocol....42
Figure 13 6800-series parallel bus protocol, write to register or display RAM....42
Figure 14 6800-series read protocol....43
Figure 15 6800-series parallel bus protocol, read data form register or display RAM....43
Figure 16 Serial interface data stream format....45
Figure 17 3-line serial interface write protocol (write to register with control bit in transmission)....45
Figure 18 4-line serial interface write protocol (write to register with control bit in transmission)....45
Figure 19 3-line serial interface read protocol....46
Figure 20 4-line serial interface read protocol....47
Figure 21 Serial bus protocol, write mode–interrupted by RESX....48
Figure 22 Serial bus protocol, write mode–interrupted by CSX....48
Figure 23 Write interrupts recovery (serial interface)....49
Figure 24 Write interrupts recovery (both serial and parallel Interface)....49
Figure 25 Serial interface pause protocol (pause by CSX)....50
Figure 26 Parallel bus pause protocol (paused by CSX)....50
Figure 27 Display data RAM organization....67
Figure 28 Data streaming order....75

LIST OF TABLES

Table 1 Absolute Operation Range 28
Table 2 DC Characteristic 29
Table 3 Power Consumption 30
Table 4 8080 Parallel Interface Characteristics....32
Table 5 6800 Parallel Interface Characteristics....34
Table 6 3-line Serial Interface Characteristics....35
Table 7 4-line Serial Interface Characteristics....36
Table 8 Interface Type Selection 37
Table 9 Pin Connection According to Various MCU Interface 37
Table 10 The Function of 8080-series Parallel Interface 38
Table 11 The Function of 6800-series Parallel Interface 41
Table 12 Selection of Serial Interface 44
Table 13 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C) 82
Table 14 Reset Timing 93
Table 15 System Function Command List (1) 104
Table 16 System Function Command List (2) 105
Table 17 System Function command List (3) 106
Table 18 Panel Function Command List (1) 155
Table 19 Panel Function Command List (2) 156
Table 20 Panel Function Command List (3) 157
Table 21 Panel Function Command List (4) 158

1 GENERAL DESCRIPTION

The ST7735S is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 396 source line and 162 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts Serial Peripheral Interface (SPI), 8-bit/9-bit/16-bit/18-bit parallel interface. Display data can be stored in the on-chip display data RAM of 132 x 162 x 18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuits necessary to drive liquid crystal, it is possible to make a display system with fewer components.

2 FEATURES

Single Chip TFT-LCD Controller/Driver with RAM
On-chip Display Data RAM (i.e. Frame Memory)

132 (H) x RGB x 162 (V) Bits

LCD Driver Output Circuits:

Source Outputs: 132 RGB Channels

Gate Outputs: 162 Channels

Common Electrode Output

Display Colors (Color Mode)

Full Color: 262K, RGB=(666) Max., Idle Mode OFF

Color Reduce: 8-color, RGB=(111), Idle Mode ON

Programmable Pixel Color Format (Color Depth) for Various Display Data input Format

12-bit/pixel: RGB=(444) Using the 384k-bit Frame Memory and LUT

16-bit/pixel: RGB=(565) Using the 384k-bit Frame Memory and LUT

18-bit/pixel: RGB=(666) Using the 384k-bit Frame Memory and LUT

Various Interfaces

Parallel 8080-series MCU Interface

(8-bit, 9-bit, 16-bit & 18-bit)

Parallel 6800-series MCU Interface

(8-bit, 9-bit, 16-bit & 18-bit)

3-line Serial Interface

4-line Serial Interface

Display Features

Support Both Normal-black & Normal-white LC

Software Programmable Color Depth Mode

Partial Window Moving & Data Scrolling

Built-in Circuits

DC/DC Converter

Adjustable VCOM Generation

Non-volatile (NV) Memory to Store Initial Register Setting

Oscillator for Display Clock Generation

Factory default value (module ID, module version, etc) are stored in NV memory.

Timing Controller

Built-in NV Memory for LCD Initial Register Setting

7-bits for ID2

8-bits for ID3

7-bits for VCOM Offset Adjustment

Wide Supply Voltage Range

I/O Voltage (VDDI to DGND): 1.65V~3.7V (VDDI ≤ VDD)

Analog Voltage (VDD to AGND): 2.5V~4.8V

On-Chip Power System

Source Voltage (GVDD to AGND): 3.15V to 5V

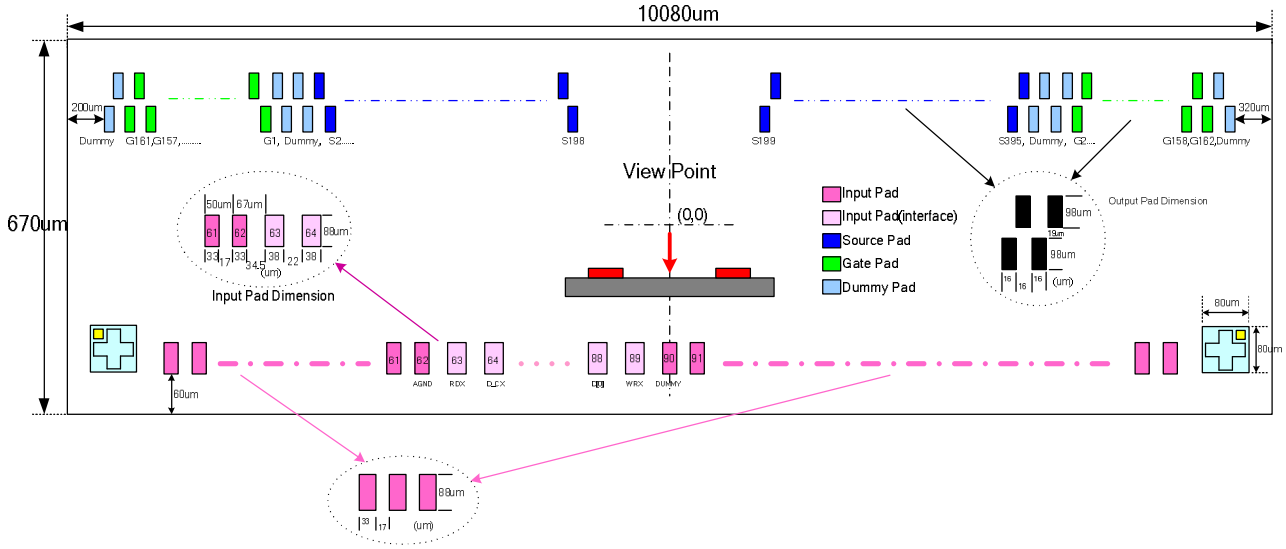
VCOM level (VCOM to AGND): -0.425V to -2.0V

Gate Driver HIGH Level (VGH to AGND): +10.0V to +15V

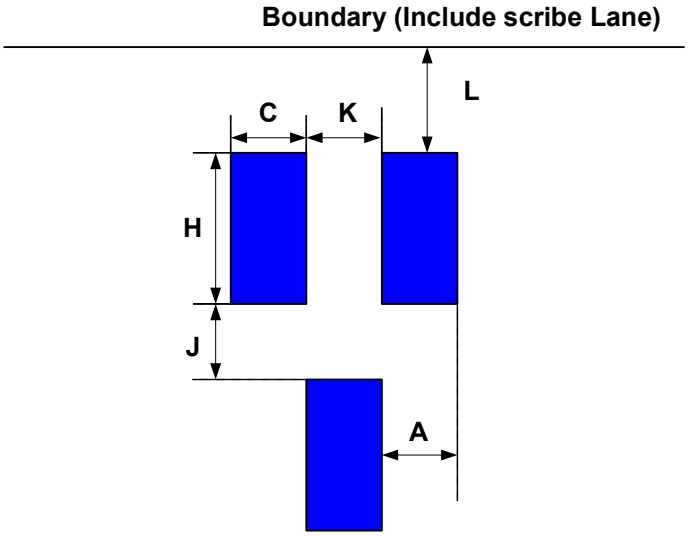
Gate Driver LOW Level (VGL to AGND): -13V to -7.5V

Operating Temperature: -30°C to +85°C

3 PAD ARRANGEMENT

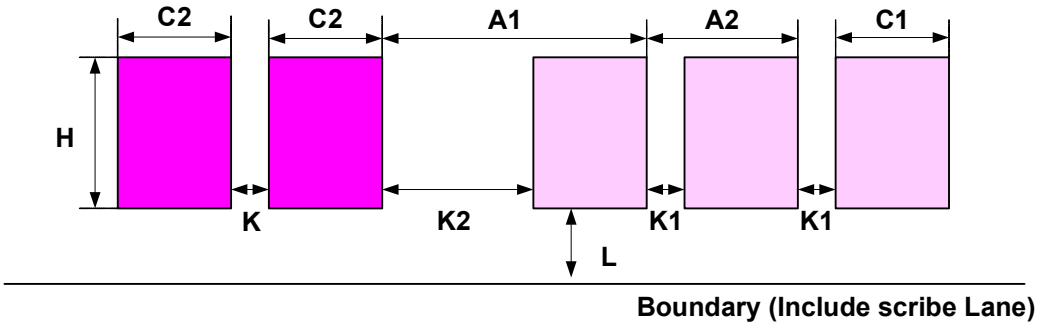


3.1 Output Bump Dimension



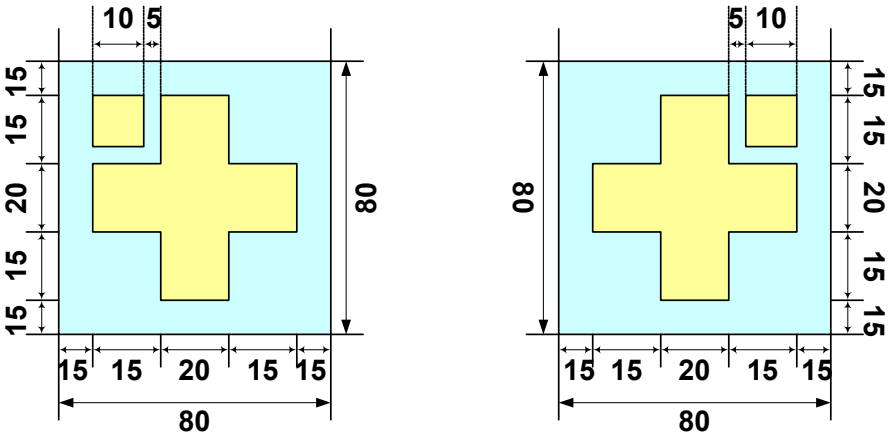
Item	Symbol	Size
Bump Pitch	A	16 um
Bump Width	C	16 um
Bump Height	H	98 um
Bump Gap1 (Vertical)	J	19 um
Bump Gap2 (Horizontal)	K	16 um
Bump Area	C x H	1568 um2
Chip Boundary (Include Scribe Lane)	L	59 um

3.2 Input Bump Dimension



Item	Symbol	Size
Bump Pitch 1	A1	72.5 um
Bump Pitch 2	A2	60 um
Bump Width 1	C1	38 um
Bump Width 2	C2	33 um
Bump Height	H	88 um
Bump Gap	K	17 um
Bump Gap1	K1	22 um
Bump Gap2	K2	34.5 um
Bump Area 1	C1 X H	3344 um2
Bump Area 2	C2 X H	2904 um2
Chip Boundary(Include Scribe Lane)	L	60 um

3.3 Alignment Mark Dimension



3.4 Chip Information

Chip Size (um x um): 10080 x 670

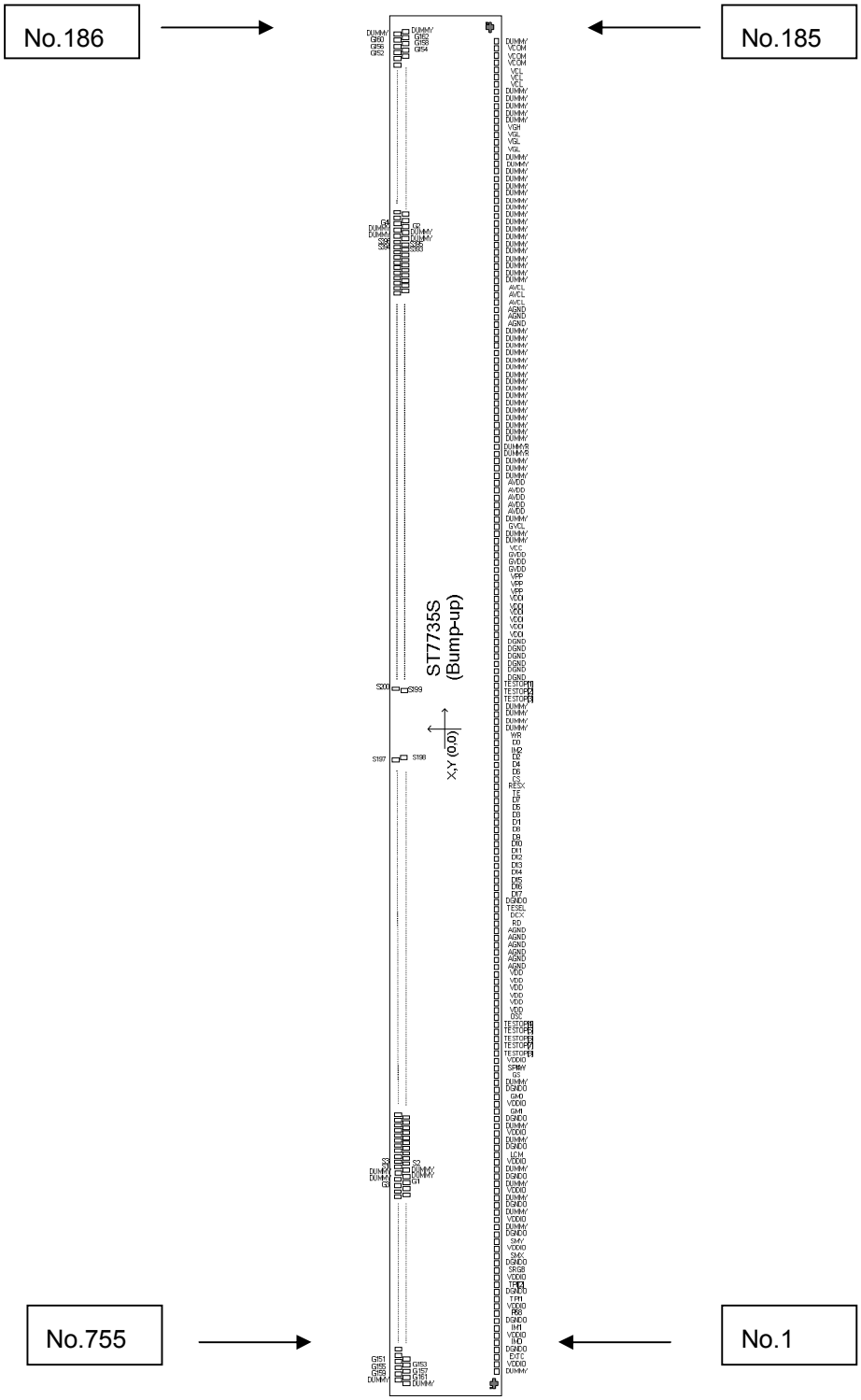
PAD Coordinate: Pad Center

Coordinate Origin: Chip Center

Chip Thickness (um): 250 or 300(TYP)

Bump Height (um): 9 or 12(TYP)

Bump Hardness (HV): 75(TYP)



4 PAD CENTER COORDINATES

No.	PAD Name	X	Y
1	Dummy	-4750	-231
2	VDDIO	-4700	-231
3	EXTC	-4650	-231
4	DGNDO	-4600	-231
5	IM0	-4550	-231
6	VDDIO	-4500	-231
7	IM1	-4450	-231
8	DGNDO	-4400	-231
9	P68	-4350	-231
10	VDDIO	-4300	-231
11	TEST1P	-4250	-231
12	DGNDO	-4200	-231
13	TEST2P	-4150	-231
14	VDDIO	-4100	-231
15	SRGB	-4050	-231
16	DGNDO	-4000	-231
17	SMX	-3950	-231
18	VDDIO	-3900	-231
19	SMY	-3850	-231
20	DGNDO	-3800	-231
21	Dummy	-3750	-231
22	VDDIO	-3700	-231
23	Dummy	-3650	-231
24	DGNDO	-3600	-231
25	Dummy	-3550	-231
26	VDDIO	-3500	-231
27	Dummy	-3450	-231
28	DGNDO	-3400	-231
29	Dummy	-3350	-231
30	VDDIO	-3300	-231
31	LCM	-3250	-231
32	DGNDO	-3200	-231
33	DUMMY	-3150	-231
34	VDDIO	-3100	-231
35	Dummy	-3050	-231
36	DGNDO	-3000	-231
37	GM1	-2950	-231
38	VDDIO	-2900	-231
39	GM0	-2850	-231
40	DGNDO	-2800	-231
41	Dummy	-2750	-231
42	GS	-2700	-231
43	SPI4W	-2650	-231
44	VDDIO	-2600	-231
45	TESTOP[8]	-2550	-231
46	TESTOP[7]	-2500	-231
47	TESTOP[6]	-2450	-231
48	TESTOP[5]	-2400	-231
49	TESTOP[4]	-2350	-231
50	OSCP	-2300	-231
51	VDD	-2250	-231
52	VDD	-2200	-231
53	VDD	-2150	-231
54	VDD	-2100	-231
55	VDD	-2050	-231
56	VDD	-2000	-231
57	AGND	-1950	-231
58	AGND	-1900	-231
59	AGND	-1850	-231
60	AGND	-1800	-231
61	AGND	-1750	-231
62	AGND	-1700	-231
63	RDX	-1630	-231
64	D_CX	-1570	-231
65	TESEL	-1510	-231
66	DGNDO	-1450	-231
67	D17	-1390	-231
68	D16	-1330	-231
69	D15	-1270	-231
70	D14	-1210	-231
71	D13	-1150	-231
72	D12	-1090	-231
73	D11	-1030	-231
74	D10	-970	-231
75	D9	-910	-231
76	D8	-850	-231
77	D1	-790	-231
78	D3	-730	-231
79	D5	-670	-231
80	D7	-610	-231
81	TE	-550	-231
82	RESX	-490	-231
83	CSX	-430	-231
84	D6	-370	-231
85	D4	-310	-231
86	D2	-250	-231
87	IM2	-190	-231
88	D0	-130	-231
89	WRX	-70	-231
90	Dummy	0	-231
91	Dummy	50	-231
92	Dummy	100	-231
93	Dummy	150	-231
94	TESTOP[3]	200	-231
95	TESTOP[2]	250	-231
96	TESTOP[1]	300	-231
97	DGND	350	-231
98	DGND	400	-231
99	DGND	450	-231
100	DGND	500	-231
101	DGND	550	-231
102	DGND	600	-231
103	VDDI	650	-231
104	VDDI	700	-231
105	VDDI	750	-231
106	VDDI	800	-231
107	VDDI	850	-231
108	VDDI	900	-231
109	VPP	950	-231
110	VPP	1000	-231
111	VPP	1050	-231
112	GVDD	1100	-231
113	GVDD	1150	-231
114	GVDD	1200	-231
115	VCC	1250	-231
116	Dummy	1300	-231
117	Dummy	1350	-231
118	GVCL	1400	-231
119	Dummy	1450	-231
120	AVDD	1500	-231
121	AVDD	1550	-231
122	AVDD	1600	-231
123	AVDD	1650	-231
124	AVDD	1700	-231
125	Dummy	1750	-231
126	Dummy	1800	-231
127	Dummy	1850	-231
128	DummyR	1900	-231
129	DummyR	1950	-231
130	Dummy	2000	-231
131	Dummy	2050	-231
132	Dummy	2100	-231
133	Dummy	2150	-231
134	Dummy	2200	-231
135	Dummy	2250	-231
136	Dummy	2300	-231
137	Dummy	2350	-231
138	Dummy	2400	-231
139	Dummy	2450	-231
140	Dummy	2500	-231
141	Dummy	2550	-231
142	Dummy	2600	-231
143	Dummy	2650	-231
144	Dummy	2700	-231
145	Dummy	2750	-231
146	AGND	2800	-231
147	AGND	2850	-231
148	AGND	2900	-231
149	AVCL	2950	-231
150	AVCL	3000	-231

No.	PAD Name	X	Y
151	AVCL	3050	-231
152	Dummy	3100	-231
153	Dummy	3150	-231
154	Dummy	3200	-231
155	Dummy	3250	-231
156	Dummy	3300	-231
157	Dummy	3350	-231
158	Dummy	3400	-231
159	Dummy	3450	-231
160	Dummy	3500	-231
161	Dummy	3550	-231
162	Dummy	3600	-231
163	Dummy	3650	-231
164	Dummy	3700	-231
165	Dummy	3750	-231
166	Dummy	3800	-231
167	Dummy	3850	-231
168	Dummy	3900	-231
169	Dummy	3950	-231
170	VGL	4000	-231
171	VGL	4050	-231
172	VGL	4100	-231
173	VGH	4150	-231
174	Dummy	4200	-231
175	Dummy	4250	-231
176	Dummy	4300	-231
177	Dummy	4350	-231
178	Dummy	4400	-231
179	VCL	4450	-231
180	VCL	4500	-231
181	VCL	4550	-231
182	VCOM	4600	-231
183	VCOM	4650	-231
184	VCOM	4700	-231
185	Dummy	4750	-231
186	Dummy	4772	110
187	Dummy	4756	227
188	G162	4740	110
189	G160	4724	227
190	G158	4708	110
191	G156	4692	227
192	G154	4676	110
193	G152	4660	227
194	G150	4644	110
195	G148	4628	227
196	G146	4612	110
197	G144	4596	227
198	G142	4580	110
199	G140	4564	227
200	G138	4548	110

No.	PAD Name	X	Y
201	G136	4532	227
202	G134	4516	110
203	G132	4500	227
204	G130	4484	110
205	G128	4468	227
206	G126	4452	110
207	G124	4436	227
208	G122	4420	110
209	G120	4404	227
210	G118	4388	110
211	G116	4372	227
212	G114	4356	110
213	G112	4340	227
214	G110	4324	110
215	G108	4308	227
216	G106	4292	110
217	G104	4276	227
218	G102	4260	110
219	G100	4244	227
220	G98	4228	110
221	G96	4212	227
222	G94	4196	110
223	G92	4180	227
224	G90	4164	110
225	G88	4148	227
226	G86	4132	110
227	G84	4116	227
228	G82	4100	110
229	G80	4084	227
230	G78	4068	110
231	G76	4052	227
232	G74	4036	110
233	G72	4020	227
234	G70	4004	110
235	G68	3988	227
236	G66	3972	110
237	G64	3956	227
238	G62	3940	110
239	G60	3924	227
240	G58	3908	110
241	G56	3892	227
242	G54	3876	110
243	G52	3860	227
244	G50	3844	110
245	G48	3828	227
246	G46	3812	110
247	G44	3796	227
248	G42	3780	110
249	G40	3764	227
250	G38	3748	110

No.	PAD Name	X	Y
251	G36	3732	227
252	G34	3716	110
253	G32	3700	227
254	G30	3684	110
255	G28	3668	227
256	G26	3652	110
257	G24	3636	227
258	G22	3620	110
259	G20	3604	227
260	G18	3588	110
261	G16	3572	227
262	G14	3556	110
263	G12	3540	227
264	G10	3524	110
265	G8	3508	227
266	G6	3492	110
267	G4	3476	227
268	G2	3460	110
269	Dummy	3444	227
270	Dummy	3428	110
271	Dummy	3412	227
272	Dummy	3396	110
273	S396	3380	227
274	S395	3364	110
275	S394	3348	227
276	S393	3332	110
277	S392	3316	227
278	S391	3300	110
279	S390	3284	227
280	S389	3268	110
281	S388	3252	227
282	S387	3236	110
283	S386	3220	227
284	S385	3204	110
285	S384	3188	227
286	S383	3172	110
287	S382	3156	227
288	S381	3140	110
289	S380	3124	227
290	S379	3108	110
291	S378	3092	227
292	S377	3076	110
293	S376	3060	227
294	S375	3044	110
295	S374	3028	227
296	S373	3012	110
297	S372	2996	227
298	S371	2980	110
299	S370	2964	227
300	S369	2948	110

No.	PAD Name	X	Y
301	S368	2932	227
302	S367	2916	110
303	S366	2900	227
304	S365	2884	110
305	S364	2868	227
306	S363	2852	110
307	S362	2836	227
308	S361	2820	110
309	S360	2804	227
310	S359	2788	110
311	S358	2772	227
312	S357	2756	110
313	S356	2740	227
314	S355	2724	110
315	S354	2708	227
316	S353	2692	110
317	S352	2676	227
318	S351	2660	110
319	S350	2644	227
320	S349	2628	110
321	S348	2612	227
322	S347	2596	110
323	S346	2580	227
324	S345	2564	110
325	S344	2548	227
326	S343	2532	110
327	S342	2516	227
328	S341	2500	110
329	S340	2484	227
330	S339	2468	110
331	S338	2452	227
332	S337	2436	110
333	S336	2420	227
334	S335	2404	110
335	S334	2388	227
336	S333	2372	110
337	S332	2356	227
338	S331	2340	110
339	S330	2324	227
340	S329	2308	110
341	S328	2292	227
342	S327	2276	110
343	S326	2260	227
344	S325	2244	110
345	S324	2228	227
346	S323	2212	110
347	S322	2196	227
348	S321	2180	110
349	S320	2164	227
350	S319	2148	110

No.	PAD Name	X	Y
351	S318	2132	227
352	S317	2116	110
353	S316	2100	227
354	S315	2084	110
355	S314	2068	227
356	S313	2052	110
357	S312	2036	227
358	S311	2020	110
359	S310	2004	227
360	S309	1988	110
361	S308	1972	227
362	S307	1956	110
363	S306	1940	227
364	S305	1924	110
365	S304	1908	227
366	S303	1892	110
367	S302	1876	227
368	S301	1860	110
369	S300	1844	227
370	S299	1828	110
371	S298	1812	227
372	S297	1796	110
373	S296	1780	227
374	S295	1764	110
375	S294	1748	227
376	S293	1732	110
377	S292	1716	227
378	S291	1700	110
379	S290	1684	227
380	S289	1668	110
381	S288	1652	227
382	S287	1636	110
383	S286	1620	227
384	S285	1604	110
385	S284	1588	227
386	S283	1572	110
387	S282	1556	227
388	S281	1540	110
389	S280	1524	227
390	S279	1508	110
391	S278	1492	227
392	S277	1476	110
393	S276	1460	227
394	S275	1444	110
395	S274	1428	227
396	S273	1412	110
397	S272	1396	227
398	S271	1380	110
399	S270	1364	227
400	S269	1348	110

No.	PAD Name	X	Y
401	S268	1332	227
402	S267	1316	110
403	S266	1300	227
404	S265	1284	110
405	S264	1268	227
406	S263	1252	110
407	S262	1236	227
408	S261	1220	110
409	S260	1204	227
410	S259	1188	110
411	S258	1172	227
412	S257	1156	110
413	S256	1140	227
414	S255	1124	110
415	S254	1108	227
416	S253	1092	110
417	S252	1076	227
418	S251	1060	110
419	S250	1044	227
420	S249	1028	110
421	S248	1012	227
422	S247	996	110
423	S246	980	227
424	S245	964	110
425	S244	948	227
426	S243	932	110
427	S242	916	227
428	S241	900	110
429	S240	884	227
430	S239	868	110
431	S238	852	227
432	S237	836	110
433	S236	820	227
434	S235	804	110
435	S234	788	227
436	S233	772	110
437	S232	756	227
438	S231	740	110
439	S230	724	227
440	S229	708	110
441	S228	692	227
442	S227	676	110
443	S226	660	227
444	S225	644	110
445	S224	628	227
446	S223	612	110
447	S222	596	227
448	S221	580	110
449	S220	564	227
450	S219	548	110

No.	PAD Name	X	Y
451	S218	532	227
452	S217	516	110
453	S216	500	227
454	S215	484	110
455	S214	468	227
456	S213	452	110
457	S212	436	227
458	S211	420	110
459	S210	404	227
460	S209	388	110
461	S208	372	227
462	S207	356	110
463	S206	340	227
464	S205	324	110
465	S204	308	227
466	S203	292	110
467	S202	276	227
468	S201	260	110
469	S200	244	227
470	S199	228	110
471	S198	-228	110
472	S197	-244	227
473	S196	-260	110
474	S195	-276	227
475	S194	-292	110
476	S193	-308	227
477	S192	-324	110
478	S191	-340	227
479	S190	-356	110
480	S189	-372	227
481	S188	-388	110
482	S187	-404	227
483	S186	-420	110
484	S185	-436	227
485	S184	-452	110
486	S183	-468	227
487	S182	-484	110
488	S181	-500	227
489	S180	-516	110
490	S179	-532	227
491	S178	-548	110
492	S177	-564	227
493	S176	-580	110
494	S175	-596	227
495	S174	-612	110
496	S173	-628	227
497	S172	-644	110
498	S171	-660	227
499	S170	-676	110
500	S169	-692	227

No.	PAD Name	X	Y
501	S168	-708	110
502	S167	-724	227
503	S166	-740	110
504	S165	-756	227
505	S164	-772	110
506	S163	-788	227
507	S162	-804	110
508	S161	-820	227
509	S160	-836	110
510	S159	-852	227
511	S158	-868	110
512	S157	-884	227
513	S156	-900	110
514	S155	-916	227
515	S154	-932	110
516	S153	-948	227
517	S152	-964	110
518	S151	-980	227
519	S150	-996	110
520	S149	-1012	227
521	S148	-1028	110
522	S147	-1044	227
523	S146	-1060	110
524	S145	-1076	227
525	S144	-1092	110
526	S143	-1108	227
527	S142	-1124	110
528	S141	-1140	227
529	S140	-1156	110
530	S139	-1172	227
531	S138	-1188	110
532	S137	-1204	227
533	S136	-1220	110
534	S135	-1236	227
535	S134	-1252	110
536	S133	-1268	227
537	S132	-1284	110
538	S131	-1300	227
539	S130	-1316	110
540	S129	-1332	227
541	S128	-1348	110
542	S127	-1364	227
543	S126	-1380	110
544	S125	-1396	227
545	S124	-1412	110
546	S123	-1428	227
547	S122	-1444	110
548	S121	-1460	227
549	S120	-1476	110
550	S119	-1492	227

No.	PAD Name	X	Y
551	S118	-1508	110
552	S117	-1524	227
553	S116	-1540	110
554	S115	-1556	227
555	S114	-1572	110
556	S113	-1588	227
557	S112	-1604	110
558	S111	-1620	227
559	S110	-1636	110
560	S109	-1652	227
561	S108	-1668	110
562	S107	-1684	227
563	S106	-1700	110
564	S105	-1716	227
565	S104	-1732	110
566	S103	-1748	227
567	S102	-1764	110
568	S101	-1780	227
569	S100	-1796	110
570	S99	-1812	227
571	S98	-1828	110
572	S97	-1844	227
573	S96	-1860	110
574	S95	-1876	227
575	S94	-1892	110
576	S93	-1908	227
577	S92	-1924	110
578	S91	-1940	227
579	S90	-1956	110
580	S89	-1972	227
581	S88	-1988	110
582	S87	-2004	227
583	S86	-2020	110
584	S85	-2036	227
585	S84	-2052	110
586	S83	-2068	227
587	S82	-2084	110
588	S81	-2100	227
589	S80	-2116	110
590	S79	-2132	227
591	S78	-2148	110
592	S77	-2164	227
593	S76	-2180	110
594	S75	-2196	227
595	S74	-2212	110
596	S73	-2228	227
597	S72	-2244	110
598	S71	-2260	227
599	S70	-2276	110
600	S69	-2292	227

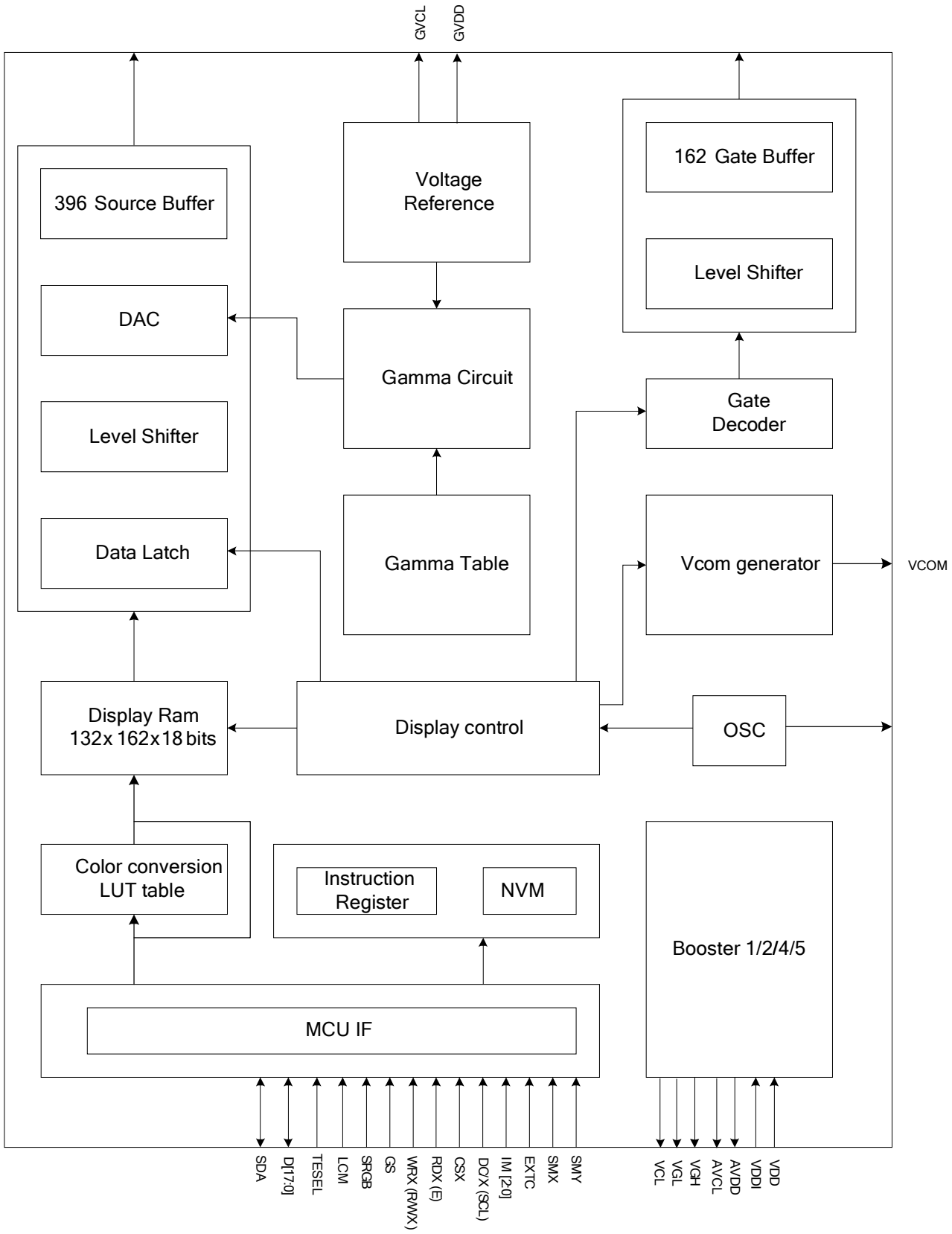
No.	PAD Name	X	Y
601	S68	-2308	110
602	S67	-2324	227
603	S66	-2340	110
604	S65	-2356	227
605	S64	-2372	110
606	S63	-2388	227
607	S62	-2404	110
608	S61	-2420	227
609	S60	-2436	110
610	S59	-2452	227
611	S58	-2468	110
612	S57	-2484	227
613	S56	-2500	110
614	S55	-2516	227
615	S54	-2532	110
616	S53	-2548	227
617	S52	-2564	110
618	S51	-2580	227
619	S50	-2596	110
620	S49	-2612	227
621	S48	-2628	110
622	S47	-2644	227
623	S46	-2660	110
624	S45	-2676	227
625	S44	-2692	110
626	S43	-2708	227
627	S42	-2724	110
628	S41	-2740	227
629	S40	-2756	110
630	S39	-2772	227
631	S38	-2788	110
632	S37	-2804	227
633	S36	-2820	110
634	S35	-2836	227
635	S34	-2852	110
636	S33	-2868	227
637	S32	-2884	110
638	S31	-2900	227
639	S30	-2916	110
640	S29	-2932	227
641	S28	-2948	110
642	S27	-2964	227
643	S26	-2980	110
644	S25	-2996	227
645	S24	-3012	110
646	S23	-3028	227
647	S22	-3044	110
648	S21	-3060	227
649	S20	-3076	110
650	S19	-3092	227

No.	PAD Name	X	Y
651	S18	-3108	110
652	S17	-3124	227
653	S16	-3140	110
654	S15	-3156	227
655	S14	-3172	110
656	S13	-3188	227
657	S12	-3204	110
658	S11	-3220	227
659	S10	-3236	110
660	S9	-3252	227
661	S8	-3268	110
662	S7	-3284	227
663	S6	-3300	110
664	S5	-3316	227
665	S4	-3332	110
666	S3	-3348	227
667	S2	-3364	110
668	S1	-3380	227
669	Dummy	-3396	110
670	Dummy	-3412	227
671	Dummy	-3428	110
672	Dummy	-3444	227
673	G1	-3460	110
674	G3	-3476	227
675	G5	-3492	110
676	G7	-3508	227
677	G9	-3524	110
678	G11	-3540	227
679	G13	-3556	110
680	G15	-3572	227
681	G17	-3588	110
682	G19	-3604	227
683	G21	-3620	110
684	G23	-3636	227
685	G25	-3652	110
686	G27	-3668	227
687	G29	-3684	110
688	G31	-3700	227
689	G33	-3716	110
690	G35	-3732	227
691	G37	-3748	110
692	G39	-3764	227
693	G41	-3780	110
694	G43	-3796	227
695	G45	-3812	110
696	G47	-3828	227
697	G49	-3844	110
698	G51	-3860	227
699	G53	-3876	110
700	G55	-3892	227

No.	PAD Name	X	Y
701	G57	-3908	110
702	G59	-3924	227
703	G61	-3940	110
704	G63	-3956	227
705	G65	-3972	110
706	G67	-3988	227
707	G69	-4004	110
708	G71	-4020	227
709	G73	-4036	110
710	G75	-4052	227
711	G77	-4068	110
712	G79	-4084	227
713	G81	-4100	110
714	G83	-4116	227
715	G85	-4132	110
716	G87	-4148	227
717	G89	-4164	110
718	G91	-4180	227
719	G93	-4196	110
720	G95	-4212	227
721	G97	-4228	110
722	G99	-4244	227
723	G101	-4260	110
724	G103	-4276	227
725	G105	-4292	110
726	G107	-4308	227
727	G109	-4324	110
728	G111	-4340	227
729	G113	-4356	110
730	G115	-4372	227
731	G117	-4388	110
732	G119	-4404	227
733	G121	-4420	110
734	G123	-4436	227
735	G125	-4452	110
736	G127	-4468	227
737	G129	-4484	110
738	G131	-4500	227
739	G133	-4516	110
740	G135	-4532	227
741	G137	-4548	110
742	G139	-4564	227
743	G141	-4580	110
744	G143	-4596	227
745	G145	-4612	110
746	G147	-4628	227
747	G149	-4644	110
748	G151	-4660	227
749	G153	-4676	110
750	G155	-4692	227

No.	PAD Name	X	Y
751	G157	-4708	110
752	G159	-4724	227
753	G161	-4740	110
754	Dummy	-4756	227
755	Dummy	-4772	110
	ALIGNMENT_R	4841	-220
	ALIGNMENT_L	-4841	-220

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power Supply Pin

Name	I/O	Description	Connect Pin
VDD	I	Power Supply for Analog, Digital System and Booster Circuit.	VDD
VDDI	I	Power Supply for I/O system.	VDDI
AGND	I	System Ground for Analog System and Booster Circuit.	GND
DGND	I	System Ground for I/O System and Digital System.	GND

6.2 Interface Logic Pin

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect pin</th></tr>
<tr><td>P68</td><td>I</td><td>-8080/6800 MCU Interface Mode Select.
-P68='1', Select 6800 MCU Parallel Interface.
-P68='0', Select 8080 MCU Parallel Interface.
-If not used, Please Fix this Pin at DGND Level.</td><td>DGND/VDDI</td></tr>
<tr><td>IM2</td><td>I</td><td>MCU Parallel Interface Bus and Serial Interface select
IM2='1', Parallel Interface
IM2='0', Serial Interface</td><td>DGND/VDDI</td></tr>
<tr><td>IM1,IM0</td><td>I</td><td>- MCU Parallel Interface Type Selection
-If Not Used, Please Fix this Pin at VDDI or DGND Level.
<table>
<tr><th>IM1</th><th>IM0</th><th>Parallel Interface</th></tr>
<tr><td>0</td><td>0</td><td>MCU 8-bit Parallel</td></tr>
<tr><td>0</td><td>1</td><td>MCU 16-bit Parallel</td></tr>
<tr><td>1</td><td>0</td><td>MCU 9-bit Parallel</td></tr>
<tr><td>1</td><td>1</td><td>MCU 18-bit Parallel</td></tr>
</table></td><td>DGND/VDDI</td></tr>
<tr><td>SPI4W</td><td>I</td><td>- SPI4W='0', 3-line SPI Enable.
- SPI4W='1', 4-line SPI Enable.
-If Not Used, Please fix this Pin at DGND Level.</td><td>DGND/VDDI</td></tr>
<tr><td>RESX</td><td>I</td><td>-This signal will reset the device and it must be applied to properly initialize the chip.
-Signal is active low.</td><td>MCU</td></tr>
<tr><td>CSX</td><td>I</td><td>-Chip Selection Pin
-Low Enable.</td><td>MCU</td></tr>
</table>

D/CX (SCL)	I	-Display data/command Selection Pin in MCU Interface. -D/CX='1': Display Data or Parameter. -D/CX='0': Command Data. -In Serial Interface, this is used as SCL. -If not used, please fix this pin at VDDI or DGND level.	MCU
RDX	I	-Read Enable in 8080 MCU Parallel Interface. -If not used, please fix this pin at VDDI or DGND level.	MCU
WRX (D/CX)	I	-Write Enable in MCU Parallel Interface. -In 4-line SPI, this pin is used as D/CX (data/ command selection). -If not used, please fix this pin at VDDI or DGND level.	MCU
D[17:0]	I/O	-D[17:0] are used as MCU parallel interface data bus. -D0 is the serial input/output signal in serial interface mode. -In serial interface, D[17:1] are not used and should be fixed at VDDI or DGND level.	MCU
TE	O	-Tearing effect output pin to synchronies MCU to frame rate, activated by S/W command. -If not used, please open this pin.	MCU
OSC	O	-Monitoring pin of internal oscillator clock and is turned ON/OFF by S/W command. -When this pin is inactive (function OFF), this pin is DGND level. -If not used, please open this pin.	-

Note1. When in parallel mode, no use data pin must be connected to "1" or "0".

Note2. When CSX="1", there is no influence to the parallel and serial interface.

6.3 Mode Selection Pin

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td>EXTC</td><td>I</td><td>- During normal operation, please connect to VDDI..
<table>
<tr><th>EXTC</th><th>Enable/disable Modification of Extend Command</th></tr>
<tr><td>0</td><td>Panel Function Commands Disable.</td></tr>
<tr><td>1</td><td>Panel Function Commands Enable.</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>GM1,
GM0</td><td>I</td><td>-Panel Resolution Selection Pins.
<table>
<tr><th>GM1</th><th>GM0</th><th>Selection of panel resolution</th></tr>
<tr><td>0</td><td>0</td><td>132RGB x 162 (S1~S396 & G1~G162 output)</td></tr>
<tr><td>0</td><td>1</td><td>132RGB x 132 (S1~S396 & G1~G132 Output)</td></tr>
<tr><td>1</td><td>1</td><td>128RGB x 160 (S7~S390 & G2~G161 output)</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>SRGB</td><td>I</td><td>-RGB Direction Select H/W Pin for Color Filter Setting.
<table>
<tr><th>SRGB</th><th>RGB Arrangement</th></tr>
<tr><td>0</td><td>S1, S2, S3 Filter Order = ’R’, ’G’, ’B’</td></tr>
<tr><td>1</td><td>S1, S2, S3 Filter Order = ‘B’, ‘G’, ‘R’</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>SMX</td><td>I</td><td>-Module Source Output Direction H/W Selection Pin.
<table>
<tr><th>SMX</th><th colspan="3">Scanning direction of source output</th></tr>
<tr><td></td><td>GM= ‘00’</td><td>GM= ‘01’</td><td>GM= ‘11’</td></tr>
<tr><td>0</td><td>S1 -> S396</td><td>S1 -> S396</td><td>S7 -> S390</td></tr>
<tr><td>1</td><td>S396 -> S1</td><td>S396 -> S1</td><td>S390 -> S7</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>SMY</td><td>I</td><td>-Module Gate Output Direction H/W Selection Pin.
<table>
<tr><th>SMY</th><th colspan="3">Scanning direction of gate output</th></tr>
<tr><td></td><td>GM= ‘00’</td><td>GM= ‘01’</td><td>GM= ‘11’</td></tr>
<tr><td>0</td><td>G1 -> G162</td><td>G1 -> G132</td><td>G2 -> G161</td></tr>
<tr><td>1</td><td>G162 -> G1</td><td>G132 -> G1</td><td>G161 -> G2</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>LCM</td><td>I</td><td>-Liquid Crystal (LC) Type Selection Pins.
<table>
<tr><th>LCM</th><th>Selection of LC Type</th></tr>
<tr><td>0</td><td>Normally White LC Type</td></tr>
<tr><td>1</td><td>Normally Black LC Type</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>GS</td><td>I</td><td>-Gamma Curve Selection Pin.
<table>
<tr><th>GS</th><th>Selection of Gamma Curve</th></tr>
<tr><td>0</td><td>GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8</td></tr>
<tr><td>1</td><td>GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0</td></tr>
</table></td><td>VDDI/DGND</td></tr>
</table>

<table>
<tr><td>VPP</td><td>I</td><td>When writing NVM, it needs external power supply voltage (7.5V).</td><td></td></tr>
<tr><td>TESEL</td><td>I</td><td>Input pin to select horizontal line number in TE signal.
This pin is internally pull low.
<table><tr><th>TESEL</th><th>Selection of gamma curve</th></tr><tr><td>0</td><td>TE output 162 lines</td></tr><tr><td>1</td><td>TE output 160 lines</td></tr></table></td><td>DGND</td></tr>
</table>

6.4 Driver Output pins

Name	I/O	Description	Connect Pin
S1 to S396	O	- Source Driver Output Pins.	-
G1 to G162	O	- Gate Driver Output Pins.	-
AVDD	O	- Power Pin for Analog Circuits.	-
AVCL	O	- A power Supply Pin for Generating GVCL.	-
VGH	O	- Power Output Pin for Gate Driver	-
VGL	O	- Power Output (Negative) Pin for Gate Driver	-
GVDD	O	- A power Output of Grayscale Voltage Generator. - When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V) to this pin.	-
GVCL	O	- A power Output (Negative) of Grayscale Voltage Generator. - When internal GVCL generator is not used, connect an external power supply (AVCL+0.5V) to this pin.	-
VCOM	O	- A Power Supply for the TFT-LCD Common Electrode.	Common Electrode
VCC	O	- Monitoring Pin of Internal Digital Reference Voltage. - Please Open These Pins.	
VCL	O	- A power output of VCOM voltage (Negative) generator.	
VDDIO	O	- VDDI Voltage Output Level for Monitoring.	-
DGNDO	O	- DGND Voltage Output Level for Monitoring.	-

6.5 Test Pins

Name	I/O	Description	Connect Pin
TEST2P TEST1P	I	-These test pins for driver vender test used. -Please connect these pins to DGND.	DGND
TESTOP[8] TESTOP[7] TESTOP[6] TESTOP[5] TESTOP[4] TESTOP[3] TESTOP[2] TESTOP[1]	O	-These test pins for driver vender test used. -Please open these pins.	Open
DummyR	-	-These pins are dummy (have no function inside). -Pad128 DummyR internal short to pad 129 DummyR.	Open
Dummy	-	-These pins are dummy (have no function inside). -Can allow signal traces pass through these pads on TFT glass. -Please open these pins.	Open

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

Item	Symbol	Rating	Unit
Supply Voltage	VDD	- 0.3 ~ +4.8	V
Supply Voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Supply Voltage (Digital)	VCC	-0.3 ~ +1.95	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Input Voltage Range	VO	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC Characteristic

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			Min	Typ	Max		
Power & Operation Voltage							
System Voltage	VDD	Operating Voltage	2.5	2.75	4.8	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.7	V	
Gate Driver High Voltage	VGH		11		16	V	Note 4
Gate Driver Low Voltage	VGL		-13		-7.5	V	
Gate Driver Supply Voltage		| VGH-VGL |	18.5		29	V	Note 4
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM Amplitude	VCOM		-2		-0.425	V	
Source driver							
Source Output Range	Vsout		0.1		GVDD	V	
Gamma Reference Voltage	GVDD		3.15		4.7	V	
Source Output Settling Time	Tr	Below with 99% precision			20	us	Note 2
Output Offset Voltage	Voffset				35	mV	Note 3

Table 2 DC Characteristic

Notes:

1. TA= -30 to 85℃.

2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.

3. The Max. value is between measured point of source output and gamma setting value.

4. VGH setting condition is AVDD=4.7V, the Max and Min VGH voltage depend on AVDD setting, VGH-VGL can not large than 30V.

7.3 Power Consumption

Ta=25℃, Frame rate = 60Hz, Bare die, the registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal Mode	Note 1	0.01	0.9	0.02	2
	Note 2	0.01	0.9	0.02	2
Partial + Idle Mode (40 lines)	Note 1	0.01	0.8	0.02	2
	Note 2	0.01	0.8	0.02	2
Sleep-In Mode	N/A	0.005	0.015	0.01	0.03

Table 3 Power Consumption

Notes:

1. All pixels black.

2. All pixels white.

3. The Current Consumption is DC characteristics of ST7735S.

4. Typical: VDDI=1.8V, VDD=2.75V; Maximum: VDDI=1.65 to 3.7V, VDD=2.5 to 4.8V

8 Timing chart

8.1 Parallel Interface Characteristics: 18, 16, 9 or 8-bit Bus (8080 Series MCU Interface)

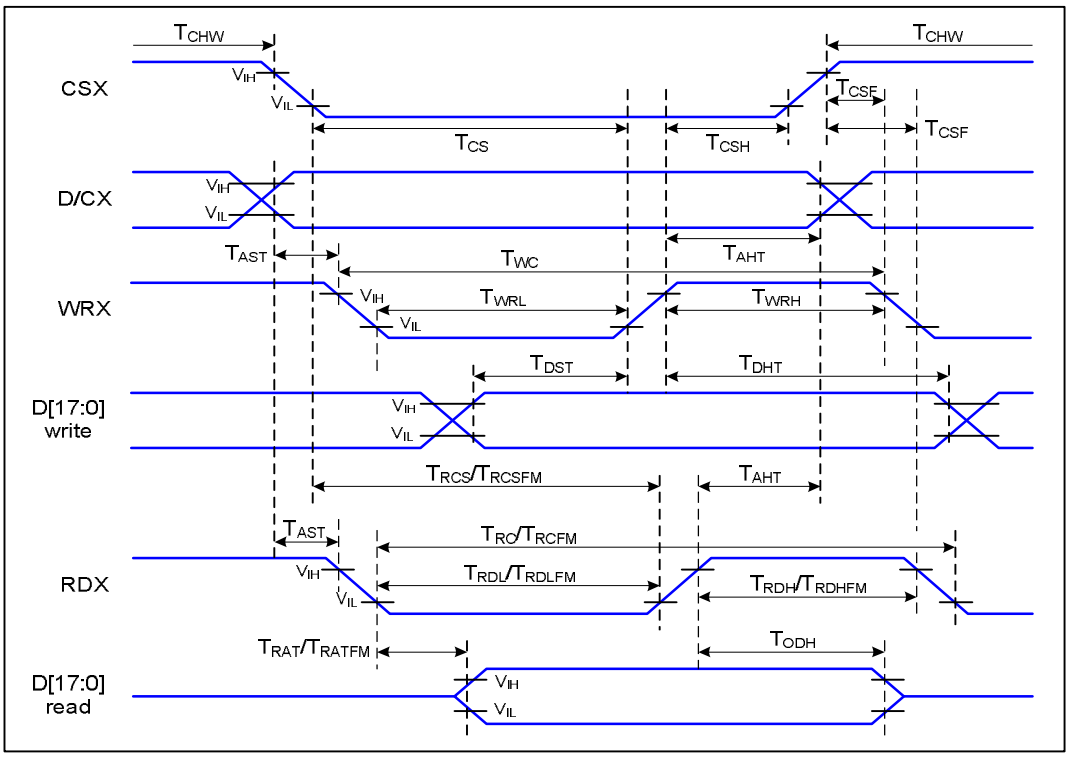


Figure 1 Parallel Interface Timing Characteristics (8080 Ceries MCU Interface)

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.5~4.8V

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	TAST	Address Setup Ttime	0		ns	-
	TAHT	Address Hold Time (Write/Read)	10		ns	
CSX	TCHW	Chip Select “H” Pulse Width	0		ns	-
	TCS	Chip Select Setup Time (Write)	15		ns	
	TRCS	Chip Select Setup Time (Read ID)	45		ns	
	TRCSFM	Chip Select Setup time (Read FM)	355		ns	
	TCSF	Chip Select Wait Time (Write/Read)	10		ns	
	TCSH	Chip Select Hold Time	10		ns	
WRX	TWC	Write Cycle	66		ns	
	TWRH	Control Pulse “H” Duration	15		ns	
	TWRL	Control Pulse “L” Duration	15		ns	
RDX (ID)	TRC	Read Cycle (ID)	160		ns	When Read ID Data
	TRDH	Control Pulse “H” Duration (ID)	90		ns	
	TRDL	Control Pulse “L” Duration (ID)	45		ns	

RDX (FM)	TRCFM	Read Cycle (FM)	450		ns	When Read from Frame Memory
	TRDHFM	Control Pulse “H” Duration (FM)	90		ns	
	TRDLFM	Control Pulse “L” Duration (FM)	355		ns	
D[17:0]	TDST	Data Setup Time	10		ns	For CL=30pF
	TDHT	Data Hold Time	10		ns	
	TRAT	Read Access Time (ID)		40	ns	
	TRATFM	Read Access Time (FM)		340	ns	
	TODH	Output Disable Time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

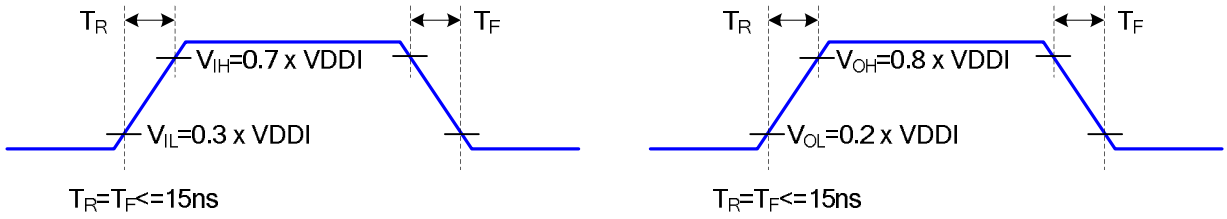


Figure 2 Rising And Falling Timing for Input And Output Signal

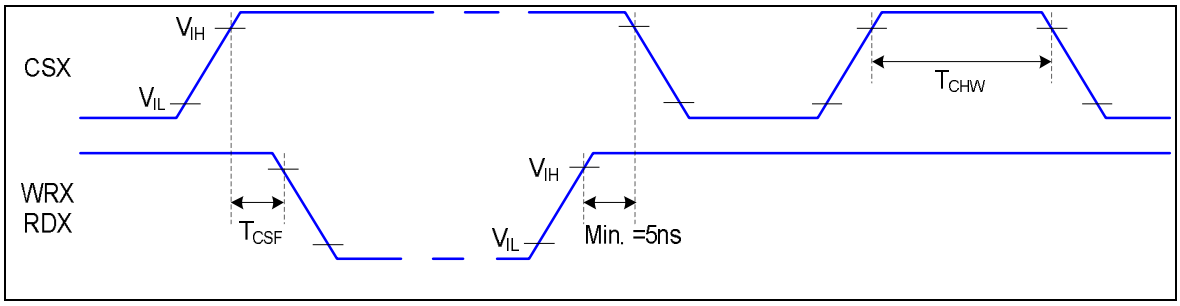


Figure 3 Chip Selection (CSX) Timing

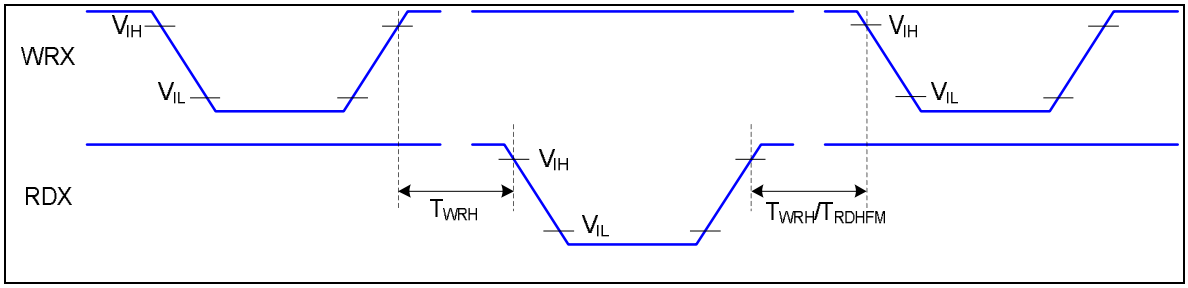


Figure 4 Write-to-Read And Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.2 Parallel Interface Characteristics: 18, 16, 9 or 8-bit Bus (6800 Series MCU Interface)

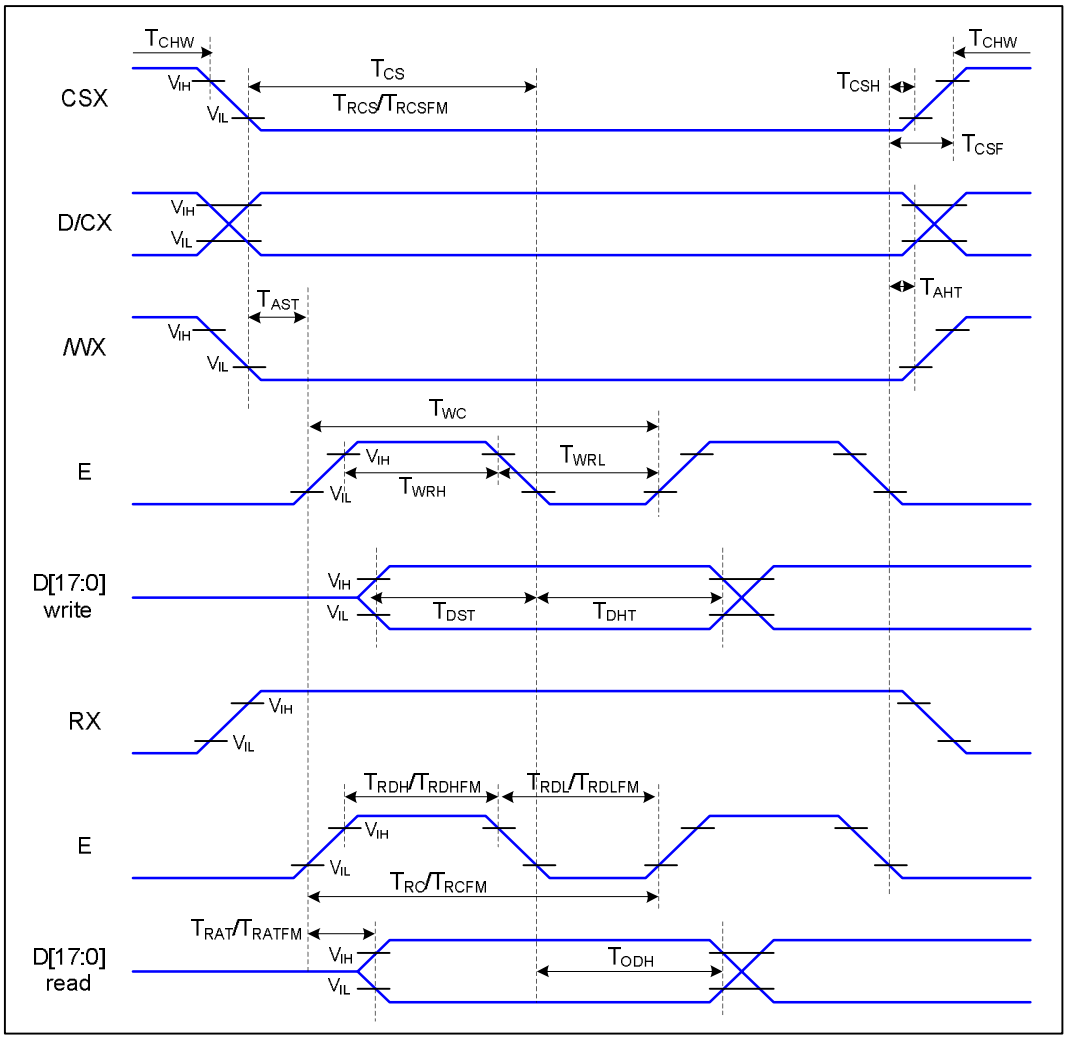


Figure 5 Parallel Interface Timing Characteristics (6800-Series MCU Interface)

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.5~4.8V

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address Setup Time	0		ns	-
	T_{AHT}	Address Hold Time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip Select “H” Pulse Width	0		ns	-
	T_{CS}	Chip Select Setup Time (Write)	15		ns	
	T_{RCS}	Chip Select Setup Time (Read ID)	45		ns	
	T_{RCSFM}	Chip Select Setup Time (Read FM)	355		ns	
	T_{CSF}	Chip Select wait Time (Write/Read)	10		ns	
	T_{CSH}	Chip Select Hold Time	10		ns	
WRX	T_{WC}	Write Cycle	66		ns	
	T_{WRH}	Control Pulse “H” Duration	15		ns	
	T_{WRL}	Control Pulse “L” Duration	15		ns	

RDX (ID)	T_{RC}	Read Cycle (ID)	160		ns	When Read ID Data
	T_{RDH}	Control Pulse “H” Duration (ID)	90		ns	
	T_{RDL}	Control Pulse “L” Duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read Cycle (FM)	450		ns	When Read From Frame Memory
	T_{RDHFM}	Control Pulse “H” Duration (FM)	90		ns	
	T_{RDLFM}	Control Pulse “L” Duration (FM)	355		ns	
D[17:0]	T_{DST}	Data Setup Time	10		ns	
	T_{DHT}	Data Hold Time	10		ns	
	T_{ODH}	Output Disable Time	20	80	ns	

Table 5 6800 Parallel Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

8.3 Serial Interface Characteristics (3-line Serial)

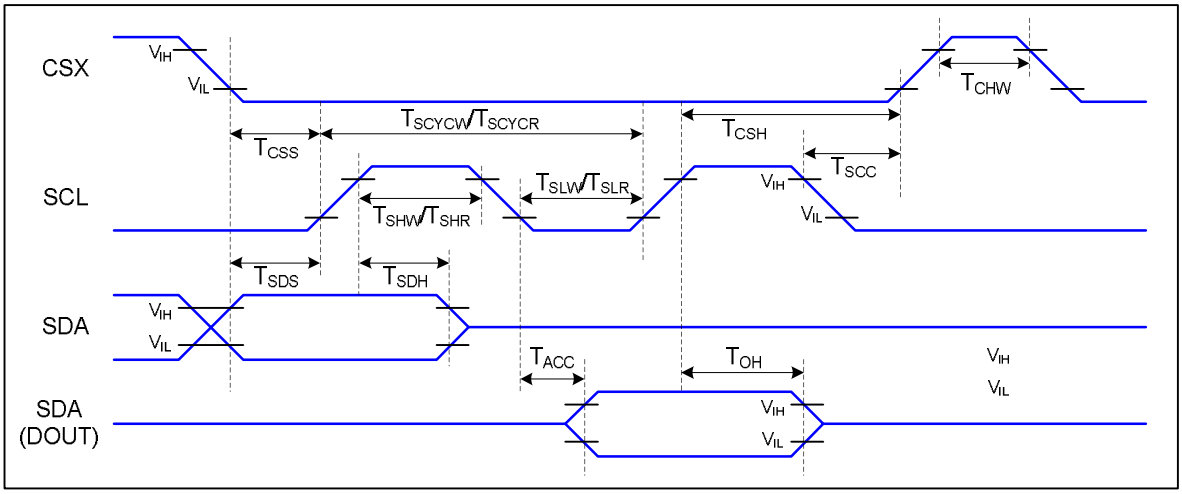


Figure 6 3-line Serial Interface Timing

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.5~4.8V

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	TCSS	Chip Select Setup Time (Write)	15		ns	
	TCSH	Chip Select Hold Time (Write)	15		ns	
	TCSS	Chip Select Setup Time (Read)	60		ns	
	TSCC	Chip Select Hold Time (Read)	65		ns	
	TCHW	Chip Select “H” pulse width	40		ns	
SCL	TSCYCW	Serial Clock Cycle (Write)	66		ns	
	TSHW	SCL “H” Pulse Width (Write)	15		ns	
	TSLW	SCL “L” Pulse Width (Write)	15		ns	
	TSCYCR	Serial Clock Cycle (Read)	150		ns	
	TSHR	SCL “H” Pulse Width (Read)	60		ns	
	TSLR	SCL “L” Pulse Width (Read)	60		ns	
SDA (DIN) (DOUT)	TSDS	Data Setup Time	10		ns	For Maximum CL=30pF For Minimum CL=8pF
	TSDH	Data Hold Time	10		ns	
	TACC	Access Time	10	50	ns	
	TOH	Output Disable Time	15	50	ns	

Table 6 3-line Serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.4 Serial Interface Characteristics (4-line Serial)

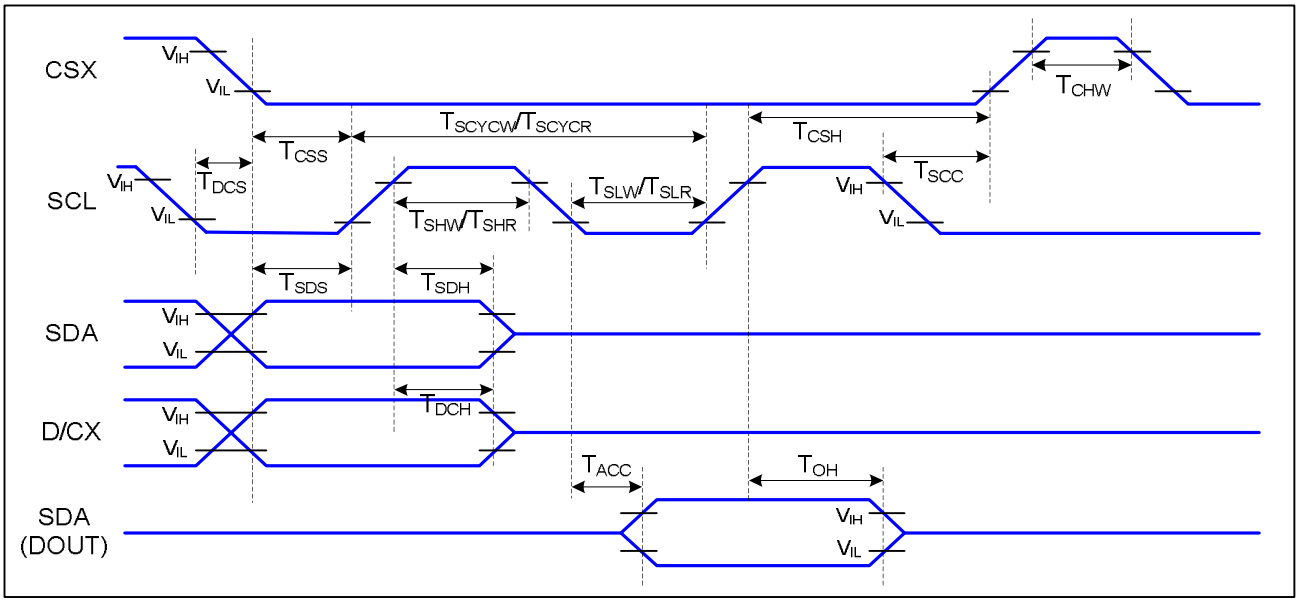


Figure 7 4-line Serial Interface Timing

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.5~4.8V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip Select Setup Time (Write)	45		ns	
	TCSH	Chip Select Hold Time (Write)	45		ns	
	TCSS	Chip Select Setup Time (Read)	60		ns	
	TSCC	Chip Select Hold Time (Read)	65		ns	
	TCHW	Chip Select “H” Pulse Width	40		ns	
SCL	TSCYCW	Serial Clock Cycle (Write)	66		ns	-Write Command & Data Ram
	TSHW	SCL “H” Pulse Width (Write)	15		ns	
	TSLW	SCL “L” Pulse Width (Write)	15		ns	
	TSCYCR	Serial Clock Cycle (Read)	150		ns	-Read Command & Data Ram
	TSHR	SCL “H” Pulse Width (Read)	60		ns	
	TSLR	SCL “L” Pulse Width (Read)	60		ns	
D/CX	TDCS	D/CX Setup Time	10		ns	
	TDCH	D/CX Hold Time	10		ns	
SDA (DIN) (DOUT)	TSDS	Data Setup Time	10		ns	For Maximum CL=30pF For Minimum CL=8pF
	TSDH	Data Hold Time	10		ns	
	TACC	Access Time	10	50	ns	
	TOH	Output Disable Time	15	50	ns	

Table 7 4-line Serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

9 Function Description

9.1 Interface Type Selection

The selection of given interfaces are done by setting IM2, IM1, and IM0 pins as shown in following table.

P68	IM2	IM1	IM0	Interface	Read Back Selection
-	0	-	-	3-line Serial Interface	Via the Read Instruction
0	1	0	0	8080 MCU 8-bit Parallel	RDX Strobe (8-bit Read Data and 8-bit Read Parameter)
0	1	0	1	8080 MCU 16-bit Parallel	RDX Strobe (16-bit Read Data and 8-bit Read Parameter)
0	1	1	0	8080 MCU 9-bit Parallel	RDX Strobe (9-bit Read Data and 8-bit Read Parameter)
0	1	1	1	8080 MCU 18-bit Parallel	RDX Strobe (18-bit Read Data and 8-bit Read Parameter)
-	0	-	-	3-line Serial Interface	Via the Read Instruction
1	1	0	0	6800 MCU 8-bit Parallel	E Strobe (8-bit Read Data and 8-bit Read Parameter)
1	1	0	1	6800 MCU 16-bit Parallel	E Strobe (16-bit Read Data and 8-bit Read Parameter)
1	1	1	0	6800 MCU 9-bit Parallel	E Strobe (9-bit Read Data and 8-bit Read Parameter)
1	1	1	1	6800 MCU 18-bit Parallel	E Strobe (18-bit Read Data and 8-bit Read Parameter)

Table 8 Interface Type Selection

P68	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
-	0	-	-	3-line Serial Interface	Note1	Note1	SCL	D[17:1]: Unused, D0: SDA
0	1	0	0	8080 8-bit Parallel	RDX	WRX	D/CX	D[17:8]: Unused, D7-D0: 8-bit Data
0	1	0	1	8080 16-bit Parallel	RDX	WRX	D/CX	D[17:16]: Unused, D15-D0: 16-bit Data
0	1	1	0	8080 9-bit Parallel	RDX	WRX	D/CX	D[17:9]: Unused, D8-D0: 9-bit Data
0	1	1	1	8080 18-bit Parallel	RDX	WRX	D/CX	D17-D0: 18-bit Data
-	0	-	-	3-line Serial Interface	Note1	D/CX	SCL	D[17:1]: Unused, D0: SDA
1	1	0	0	6800 8-bit Parallel	E	WRX	RS	D[17:8]: Unused, D7-D0: 8-bit Data
1	1	0	1	6800 16-bit Parallel	E	WRX	RS	D[17:16]: Unused, D15-D0: 16-bit Data
1	1	1	0	6800 9-bit Parallel	E	WRX	RS	D[17:9]: Unused, D8-D0: 9-bit Data
1	1	1	1	6800 18-bit Parallel	E	WRX	RS	D17-D0: 18-bit Data

Table 9 Pin Connection According to Various MCU Interface

Note: Unused pins can be open, or connected to DGND or VDDI.

9.2 8080-series MCU Parallel Interface (P68 = '0')

The MCU can use one of following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-line with 16-data parallel interface or 21-lines with 18-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits is either display data or command parameter. When D/C='0', D[17:0] bits is command. The interface functions of 8080-series parallel interface are given in following table..

IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read Back Selection
1	0	0	8-bit Parallel	0	1	↑	Write 8-bit Command (D7 to D0)
				1	1	↑	Write 8-bit Display Data or 8-bit Parameter (D7 to D0)
				1	↑	1	Read 8-bit Display Data (D7 to D0)
				1	↑	1	Read 8-bit Parameter or Status (D7 to D0)
1	0	1	16-bit Parallel	0	1	↑	Write 8-bit Command (D7 to D0)
				1	1	↑	Write 16-bit Display Data or 8-bit Parameter (D15 to D0)
				1	↑	1	Read 16-bit Display Data (D15 to D0)
				1	↑	1	Read 8-bit Parameter or Status (D7 to D0)
1	1	0	9-bit Parallel	0	1	↑	Write 8-bit Command (D7 to D0)
				1	1	↑	Write 9-bit Display Data or 8-bit Parameter (D8 to D0)
				1	↑	1	Read 9-bit Display Data (D8 to D0)
				1	↑	1	Read 8-bit Parameter or Status (D7 to D0)
1	1	1	18-bit Parallel	0	1	↑	Write 8-bit Command (D7 to D0)
				1	1	↑	Write 18-bit Display Data or 8-bit Parameter (D17 to D0)
				1	↑	1	Read 18-bit Display Data (D17 to D0)
				1	↑	1	Read 8-bit Parameter or Status (D7 to D0)

Table 10 The Function of 8080-series Parallel Interface

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

9.2.1 Write Cycle Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data ('1').

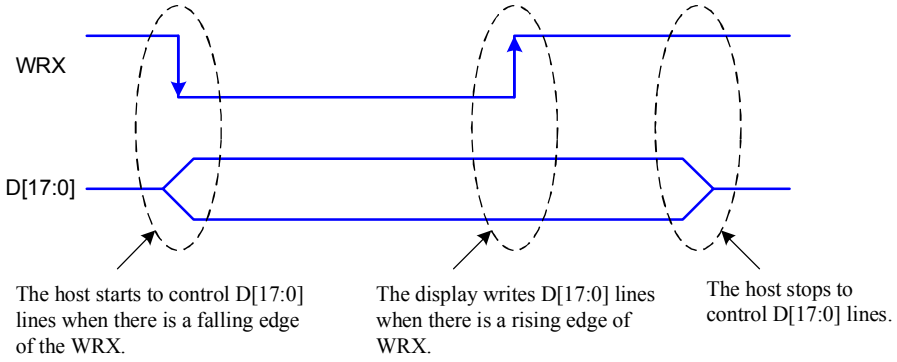


Figure 8 8080-series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

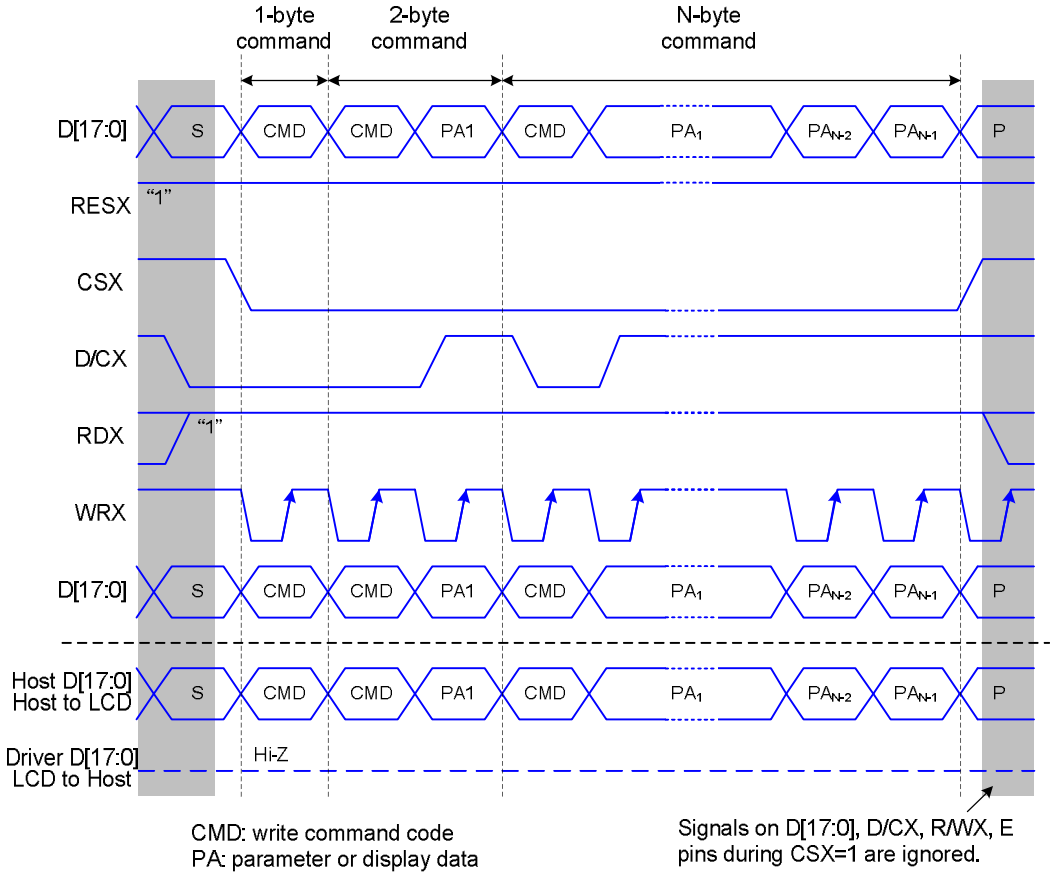


Figure 9 8080-series Parallel Bus Protocol, Write to Register or Display RAM

9.2.2 Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

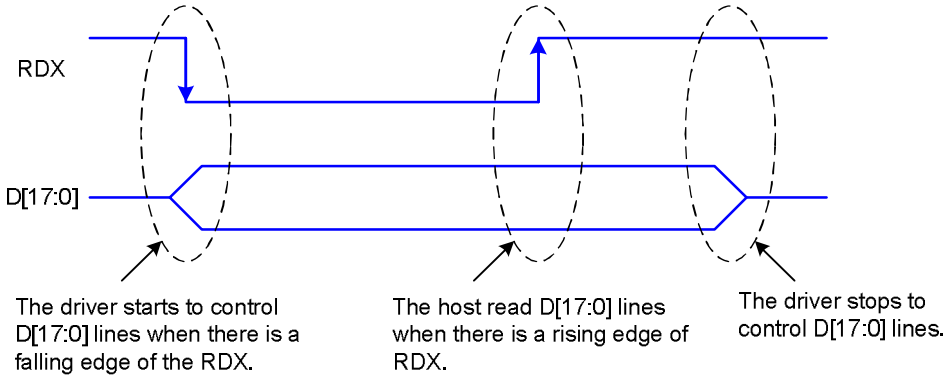


Figure 10 8080-series RDX Protocol

Note: RDX is an unsynchronized signal (It can be stopped).

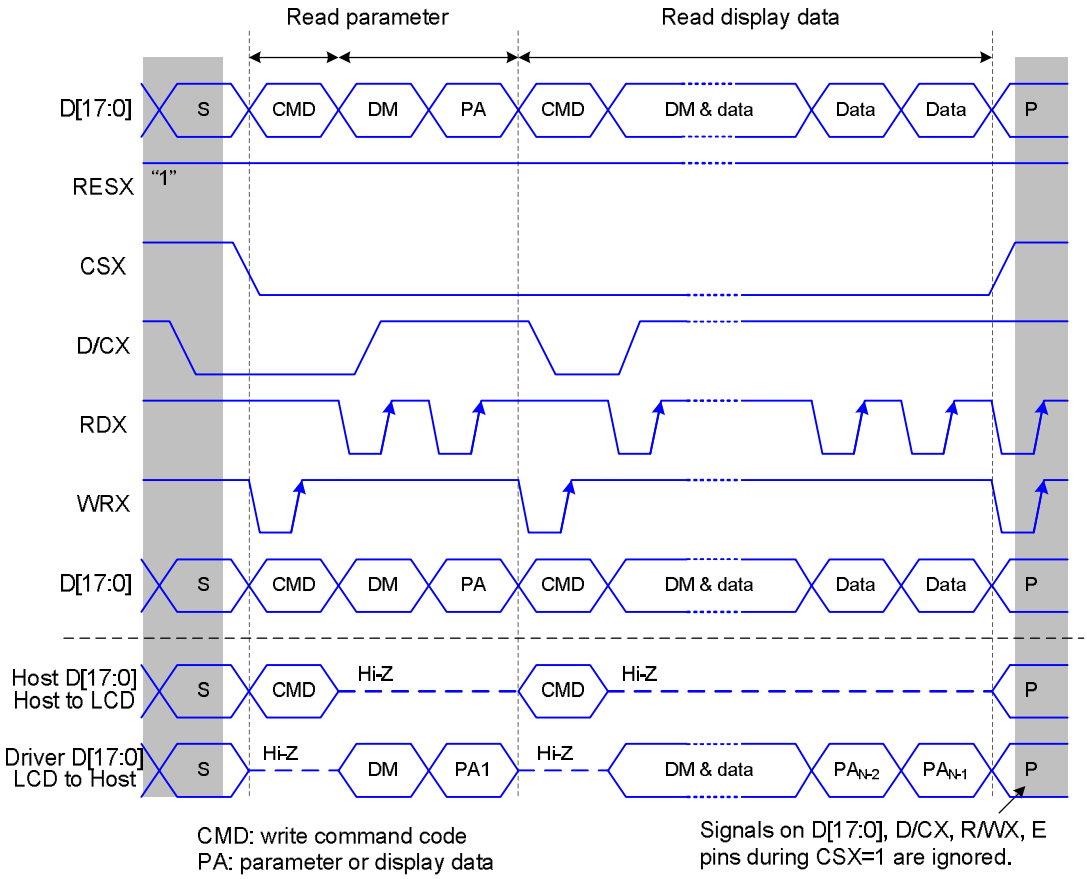


Figure 11 8080-series Parallel Bus Protocol, Read Data from Register or Display RAM

9.3 6800-series MCU Parallel Interface (P68 = '1')

The MCU uses one of following interface: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-lines with 16-data parallel interface, or 21-lines with 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data bus.

The LCD driver reads the data at the falling edge of E signal when R/WX= '1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C= '0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0.The interface functions of 6800-series parallel interface are given in Table11.

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	1	0	0	8-bit Parallel	0	0	↓	Write 8-bit Command (D7 to D0)
					1	0	↓	Write 8-bit Display Data or 8-bit Parameter (D7 to D0)
					1	1	↓	Read 8-bit Display Data (D7 to D0)
					1	1	↓	Read 8-bit Parameter or Status (D7 to D0)
1	1	0	1	16-bit Parallel	0	0	↓	Write 8-bit Command (D7 to D0)
					1	0	↓	Write 16-bit Display Data or 8-bit Parameter (D15 to D0)
					1	1	↓	Read 16-bit Display Data (D15 to D0)
					1	1	↓	Read 8-bit Parameter or Status (D7 to D0)
1	1	1	0	9-bit Parallel	0	0	↓	Write 8-bit Command (D7 to D0)
					1	0	↓	Write 9-bit Display Data or 8-bit Parameter (D8 to D0)
					1	1	↓	Read 9-bit Display Data (D8 to D0)
					1	1	↓	Read 8-bit Parameter or Status (D7 to D0)
1	1	1	1	18-bit Parallel	0	0	↓	Write 8-bit Command (D7 to D0)
					1	0	↓	Write 18-bit Display Data or 8-bit Parameter (D17 to D0)
					1	1	↓	Read 18-bit Display Data (D17 to D0)
					1	1	↓	Read 8-bit Parameter or Status (D7 to D0)

Table 11 The Function of 6800-series Parallel Interface

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

9.3.1 Write Cycle Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control signals (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

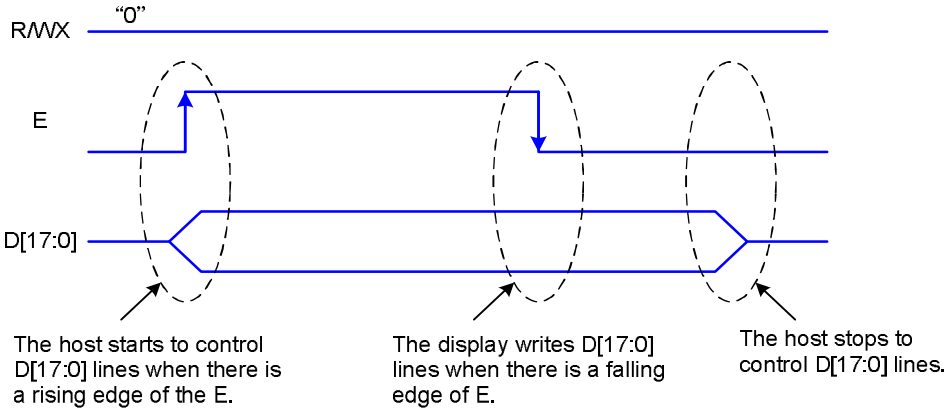


Figure 12 6800-series Write Protocol

Note: E is an unsynchronized signal (It can be stopped)

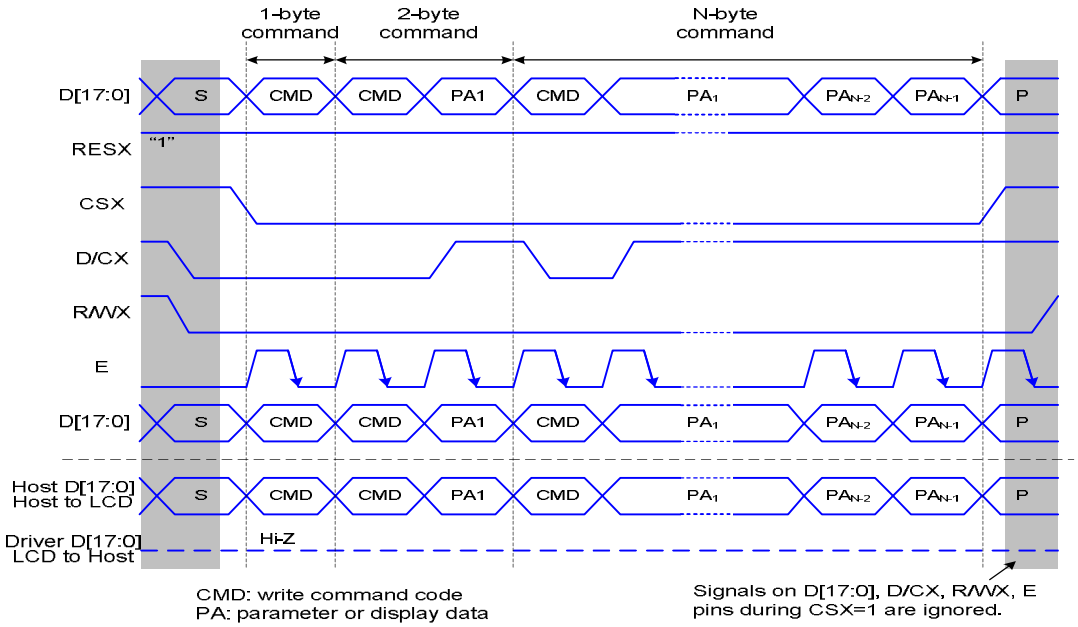


Figure 13 6800-series Parallel Bus Protocol, Write to Register or Display RAM

9.3.2 Read Cycle Sequence

The read cycle (E low-high-low sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a rising edge of E and the host reads data when there is a falling edge of E.

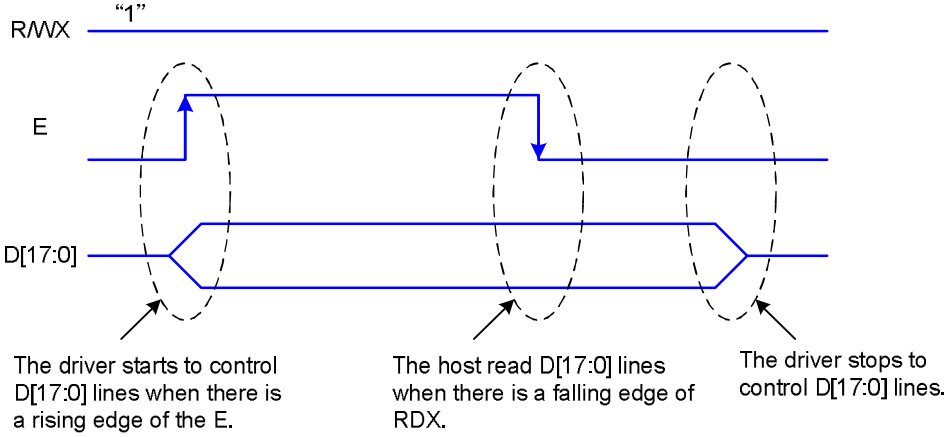


Figure 14 6800-series Read Protocol

Note: E is an unsynchronized signal (It can be stopped)

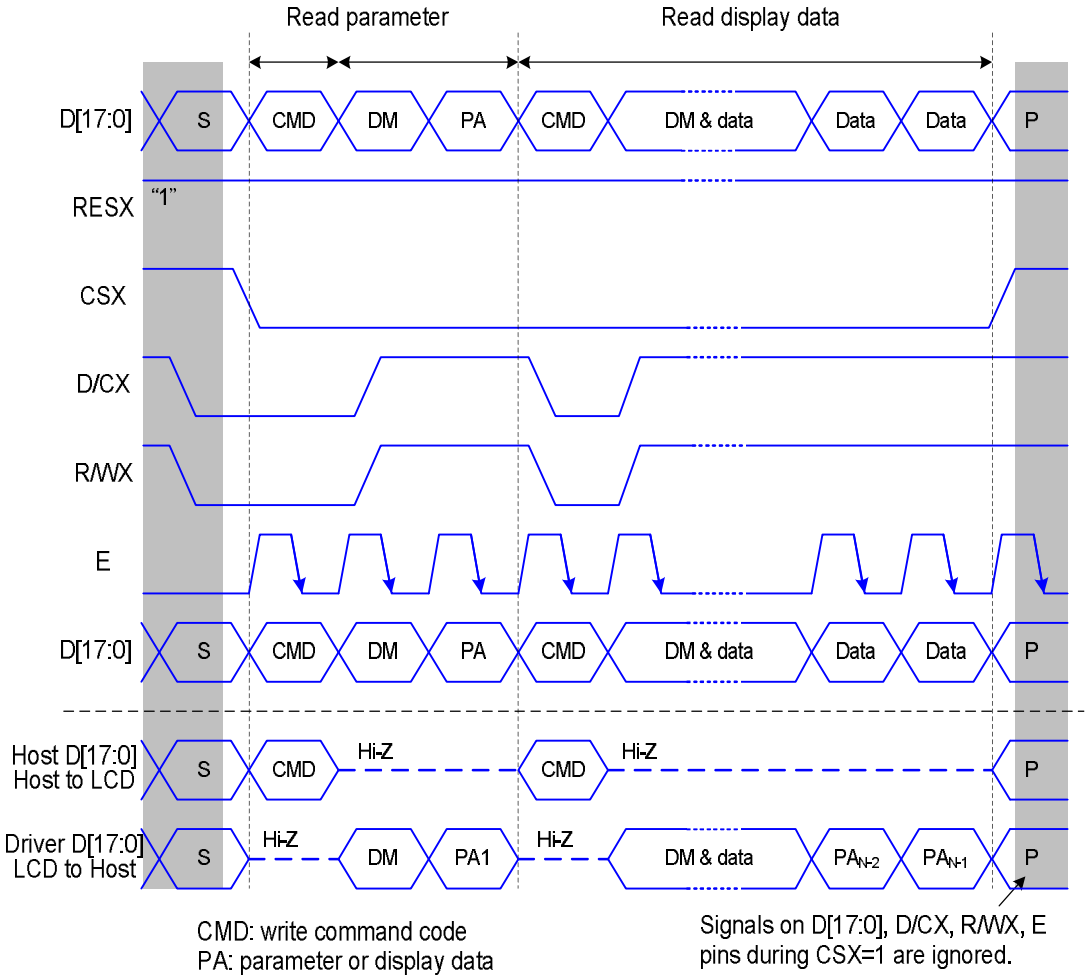


Figure 15 6800-series Parallel Bus Protocol, Read Data form Register or Display RAM

9.4 Serial Interface

The selection of this interface is done by IM2. See the Table 12.

IM2	4WSPI	Interface	Read Back Selection
0	0	3-line Serial Interface	Via the Read Instruction (8-bit, 24-bit and 32-bit Read Parameter)
0	1	4-line Serial Interface	Via the Read Instruction (8-bit, 24-bit and 32-bit Read Parameter)

Table 12 Selection of Serial Interface

The serial interface is either 3-lines/9-bits or 4-lines/8-bts bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

9.4.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

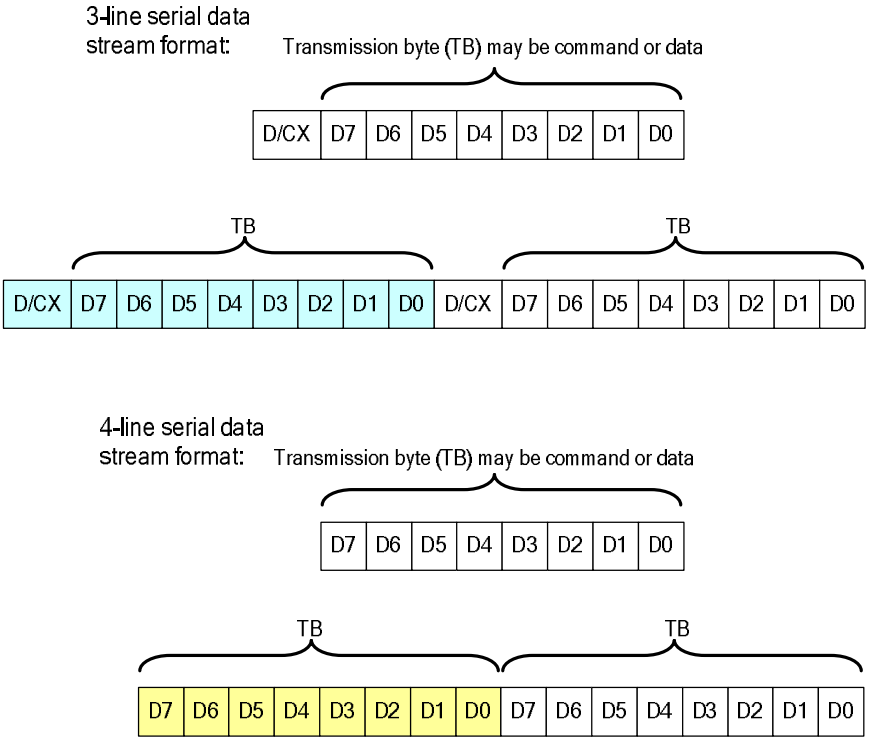


Figure 16 Serial Interface Data Stream Format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see Figure 17). SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter/RAM data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-lines serial interface) or 8th rising edge of SCL (4-lines serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-lines serial interface) or D7 (4-lines serial interface) of the next byte at the next rising edge of SCL..

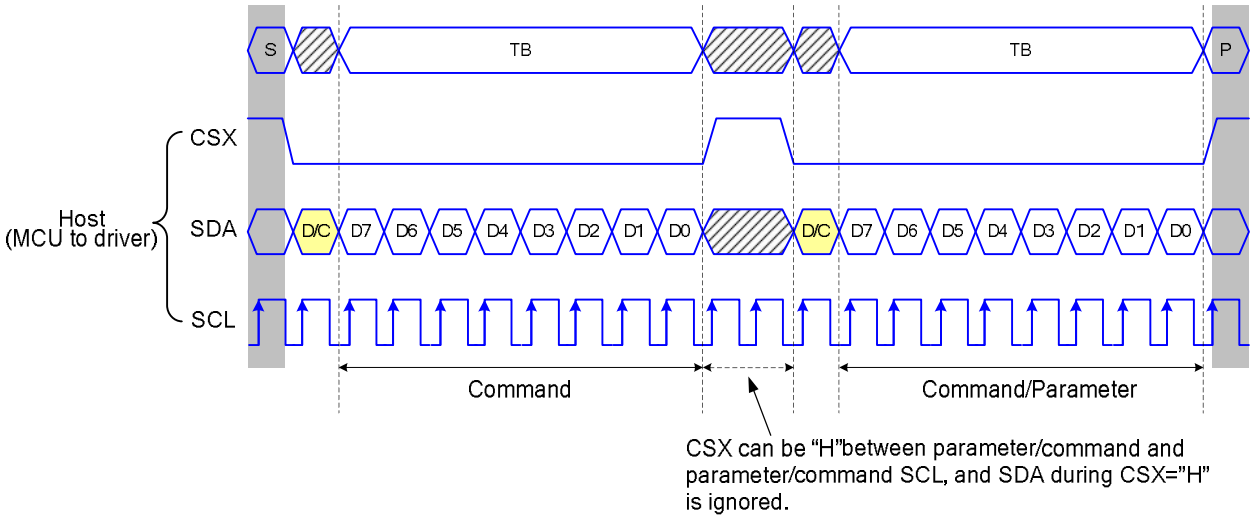


Figure 17 3-line Serial Interface Write Protocol (Write to Register with Control Bit in Transmission)

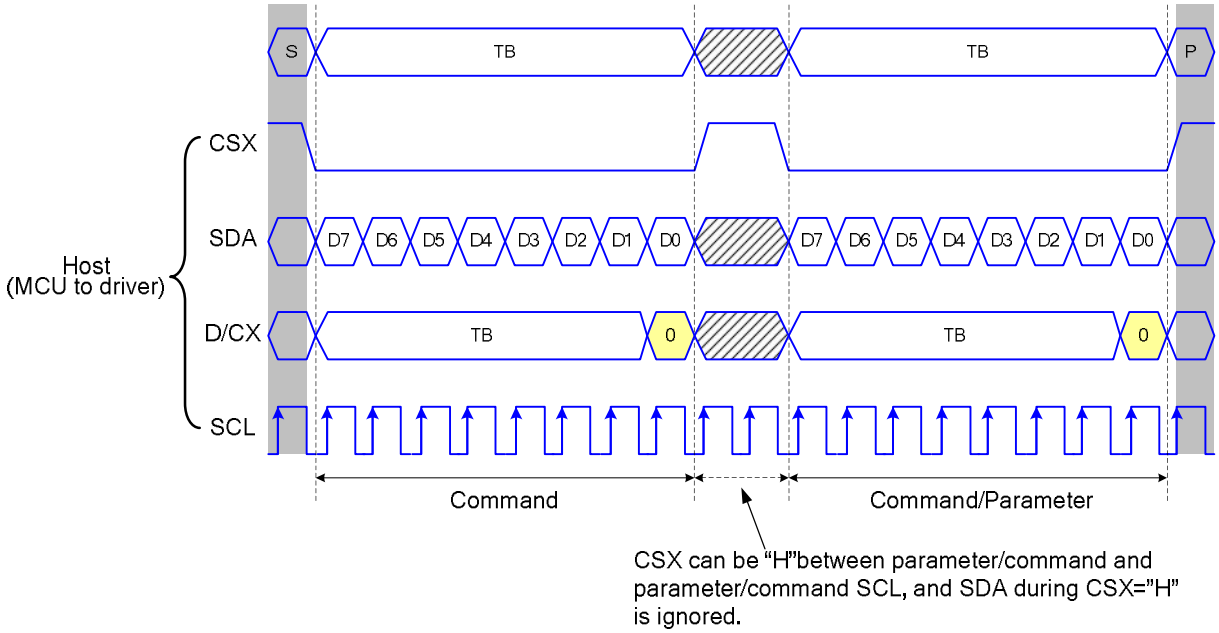


Figure 18 4-line Serial Interface Write Protocol (Write to Register with Control Bit in Transmission)

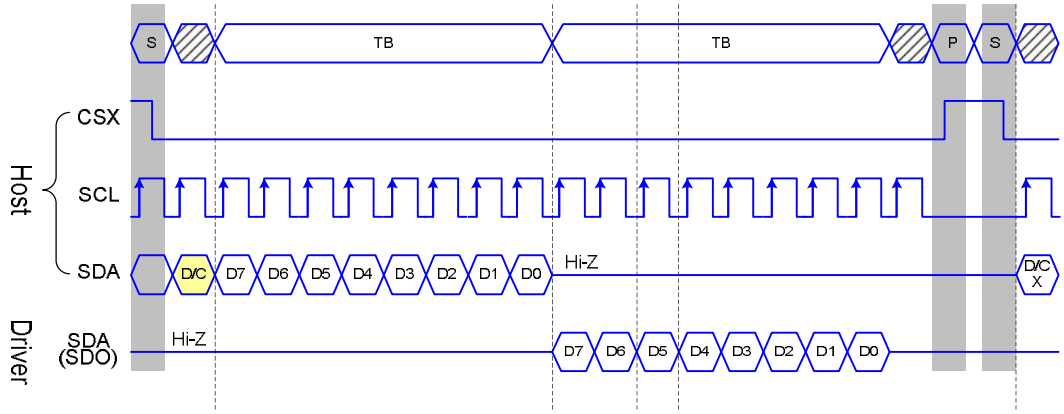
9.4.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

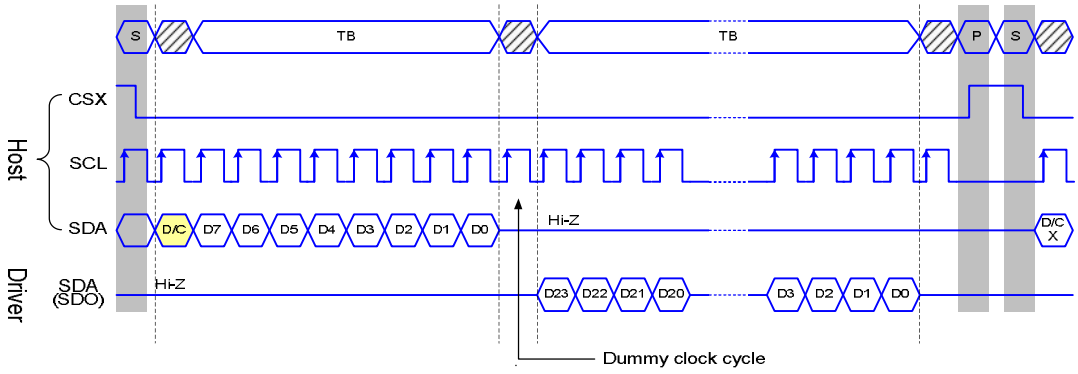
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

9.4.3 3-line Serial Protocol

3-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh Command: 8-bit Read):



3-line Serial Protocol (for RDDID Command: 24-bit Read)



3-line Serial Protocol (for RDDST Command: 32-bit Read)

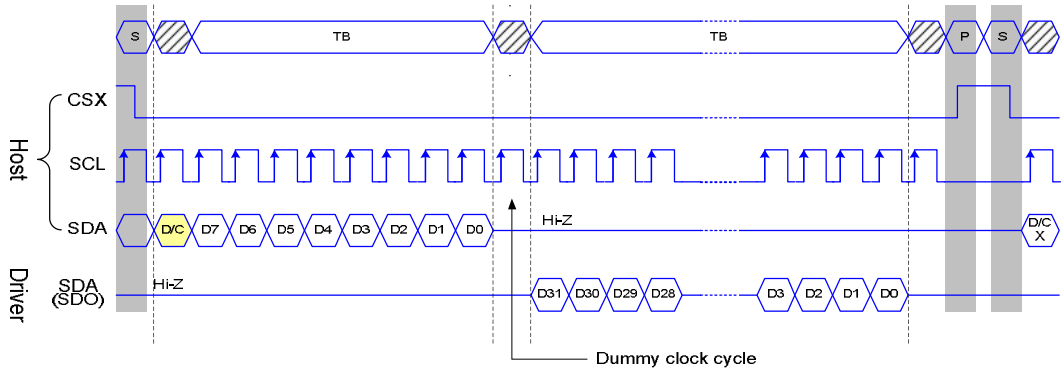
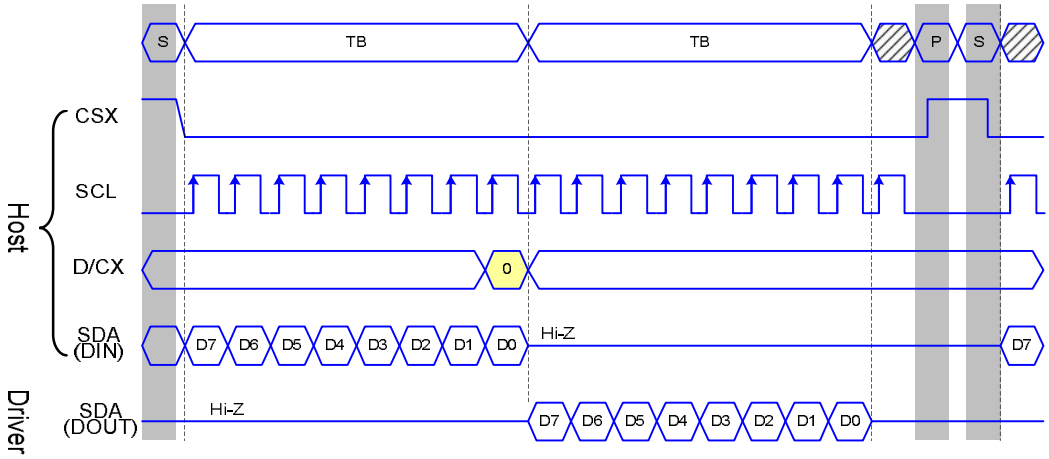


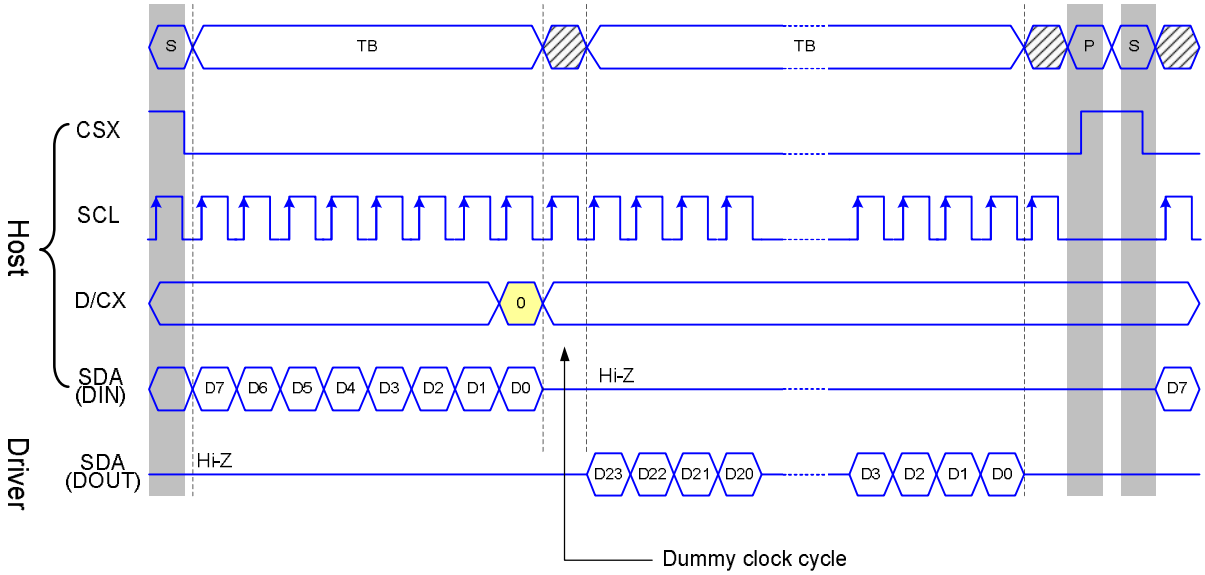
Figure 19 3-line Serial Interface Read Protocol

9.4.4 4-line Serial Protocol

4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh Command: 8-bit Read):



4-line Serial Protocol (for RDDID Command: 24-bit Read)



4-line Serial Protocol (for RDDST Command: 32-bit Read)

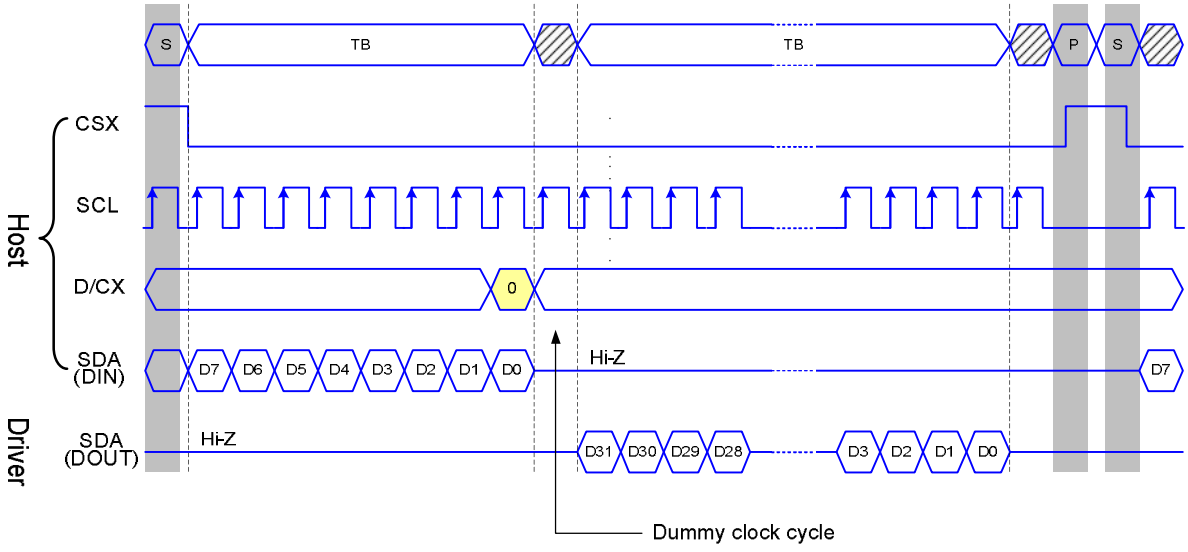


Figure 20 4-line Serial Interface Read Protocol

9.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state. See the following example

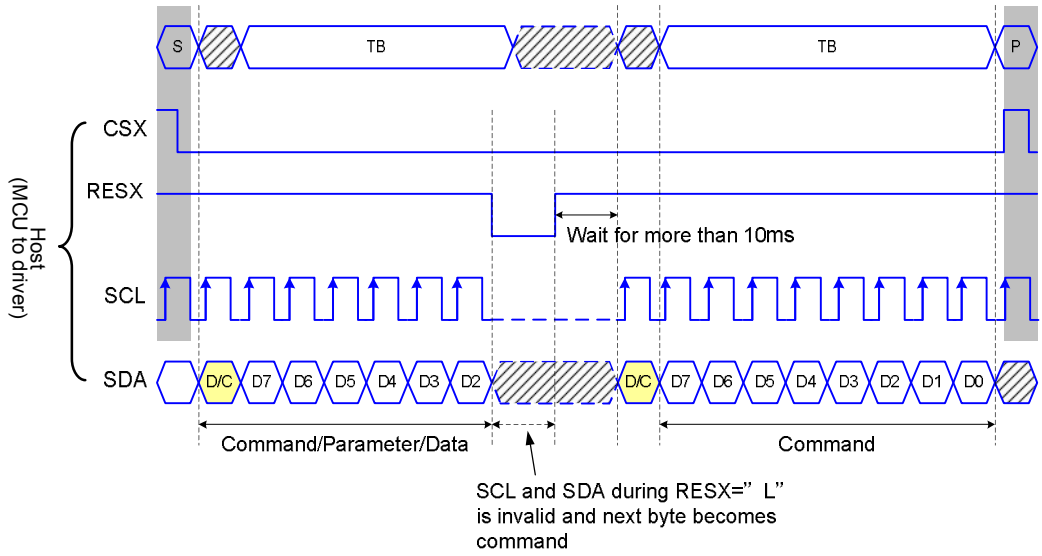


Figure 21 Serial Bus Protocol, Write Mode – Interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

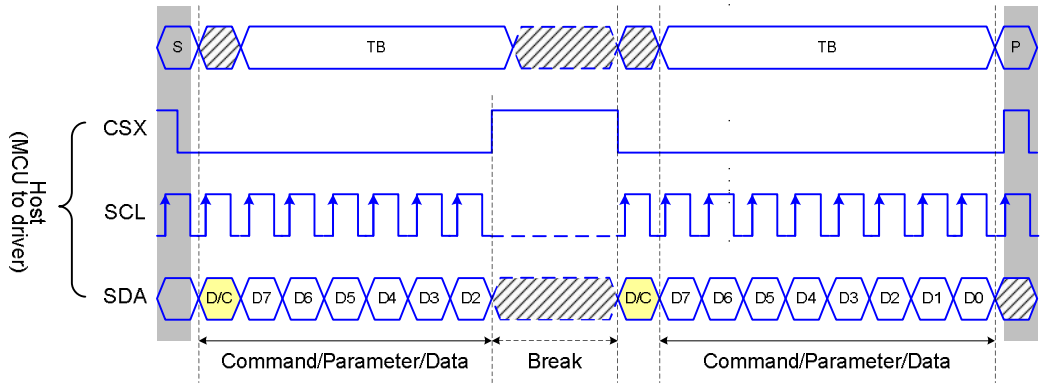


Figure 22 Serial Bus Protocol, Write Mode – Interrupted by CSX

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

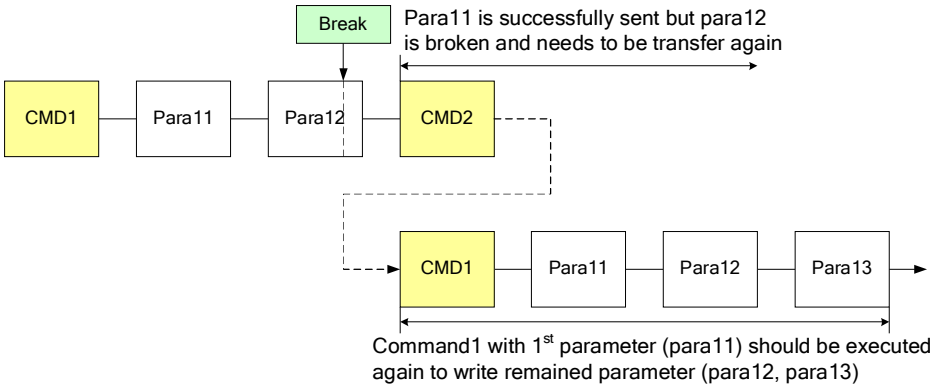


Figure 23 Write Interrupts Recovery (Serial Interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

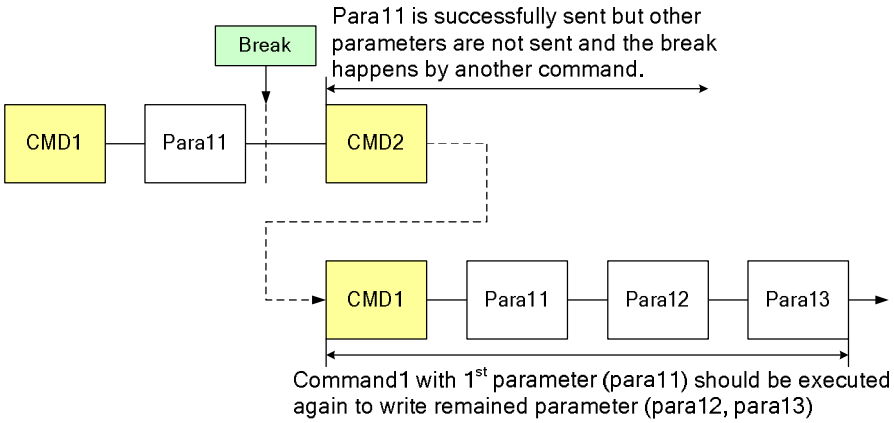


Figure 24 Write Interrupts Recovery (Both Serial and Parallel Interface)

9.6 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

9.6.1 Serial Interface Pause

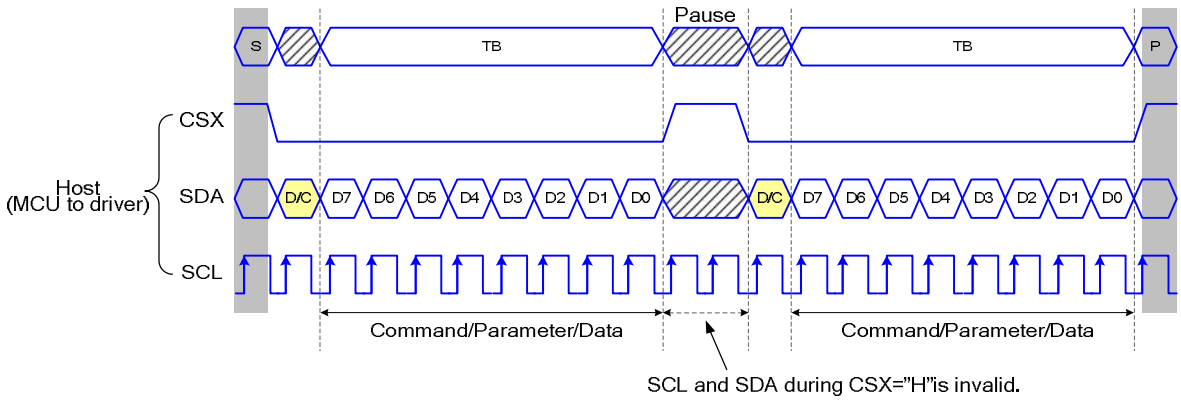


Figure 25 Serial Interface Pause Protocol (Pause by CSX)

9.6.2 Parallel Interface Pause

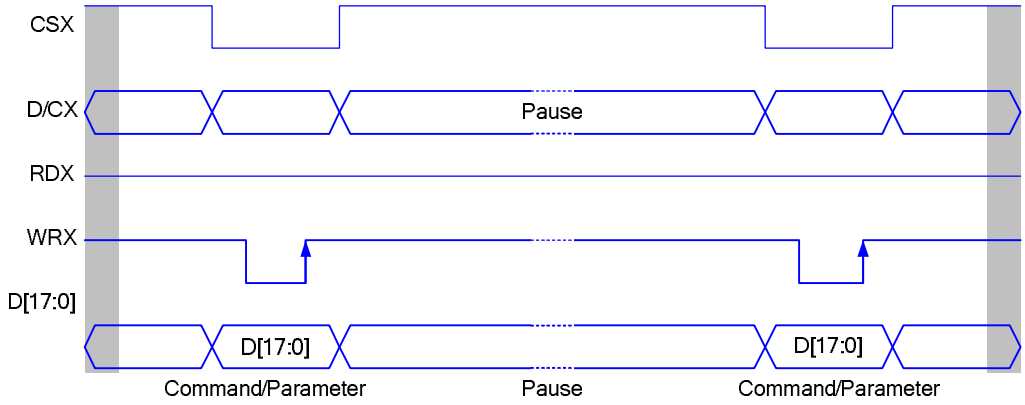


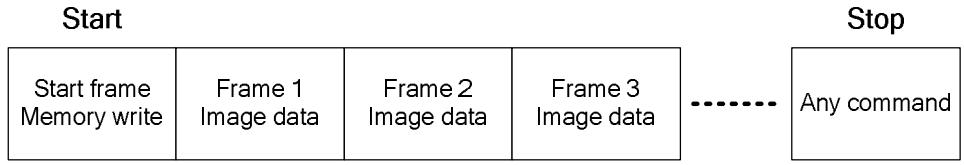
Figure 26 Parallel Bus Pause Protocol (Paused by CSX)

9.7 Data Transfer Modes

The module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

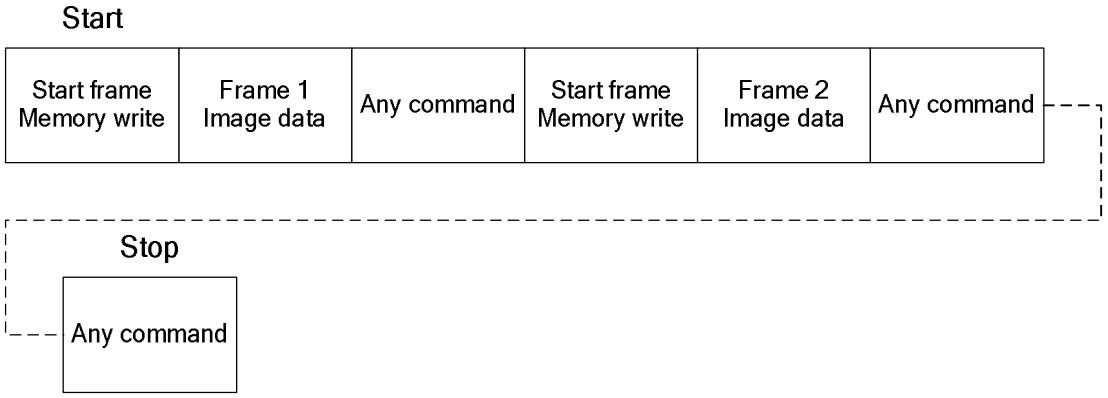
9.7.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



9.7.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

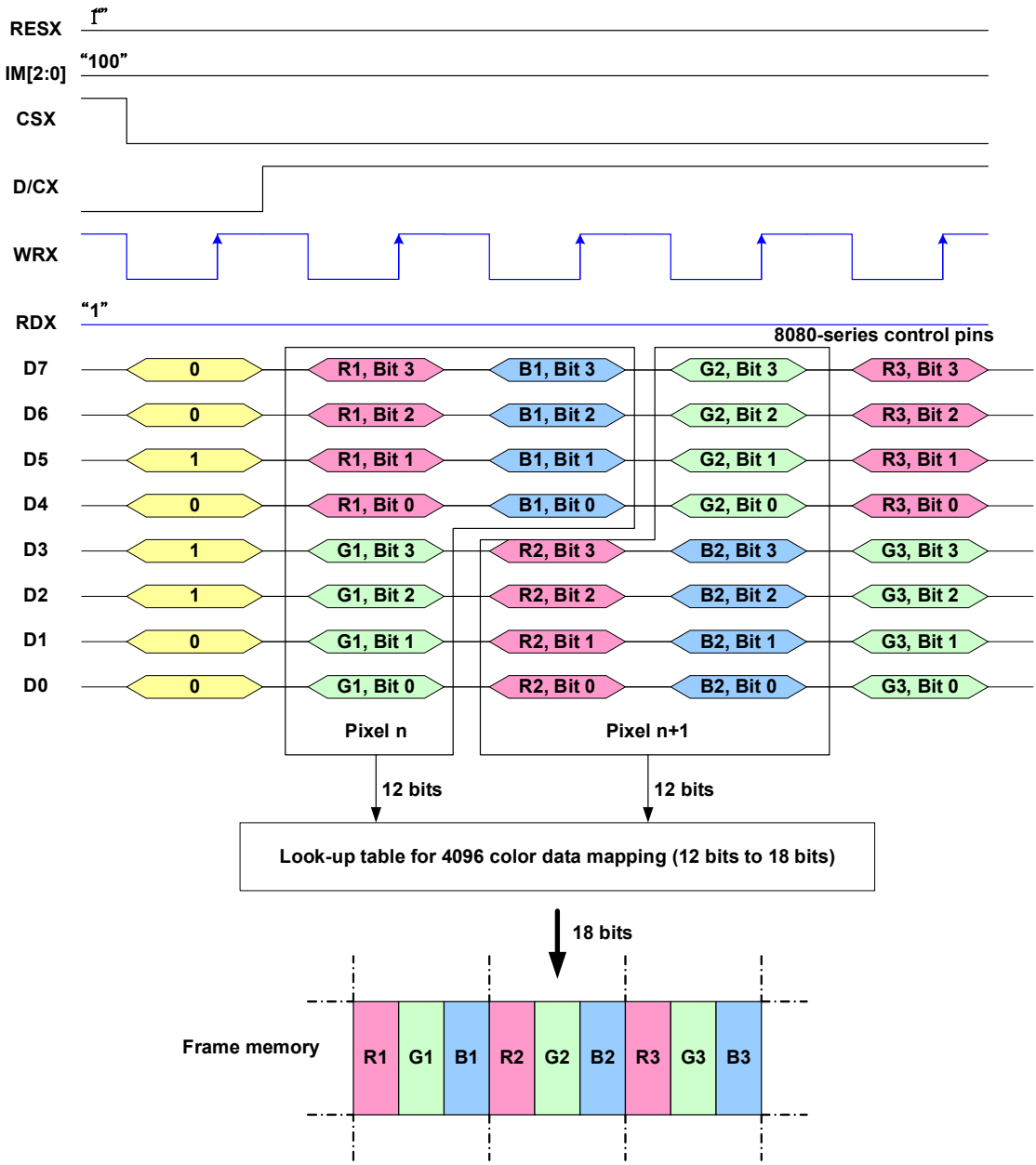
9.8 Data Color Coding

9.8.1 8-bit Parallel Interface (IM2, IM1, IM0= “100”)

Different display data formats are available for three Colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bit Input.
- 65k Colors, RGB 5,6,5-bit Input.
- 262k Colors, RGB 6,6,6-bit Input.

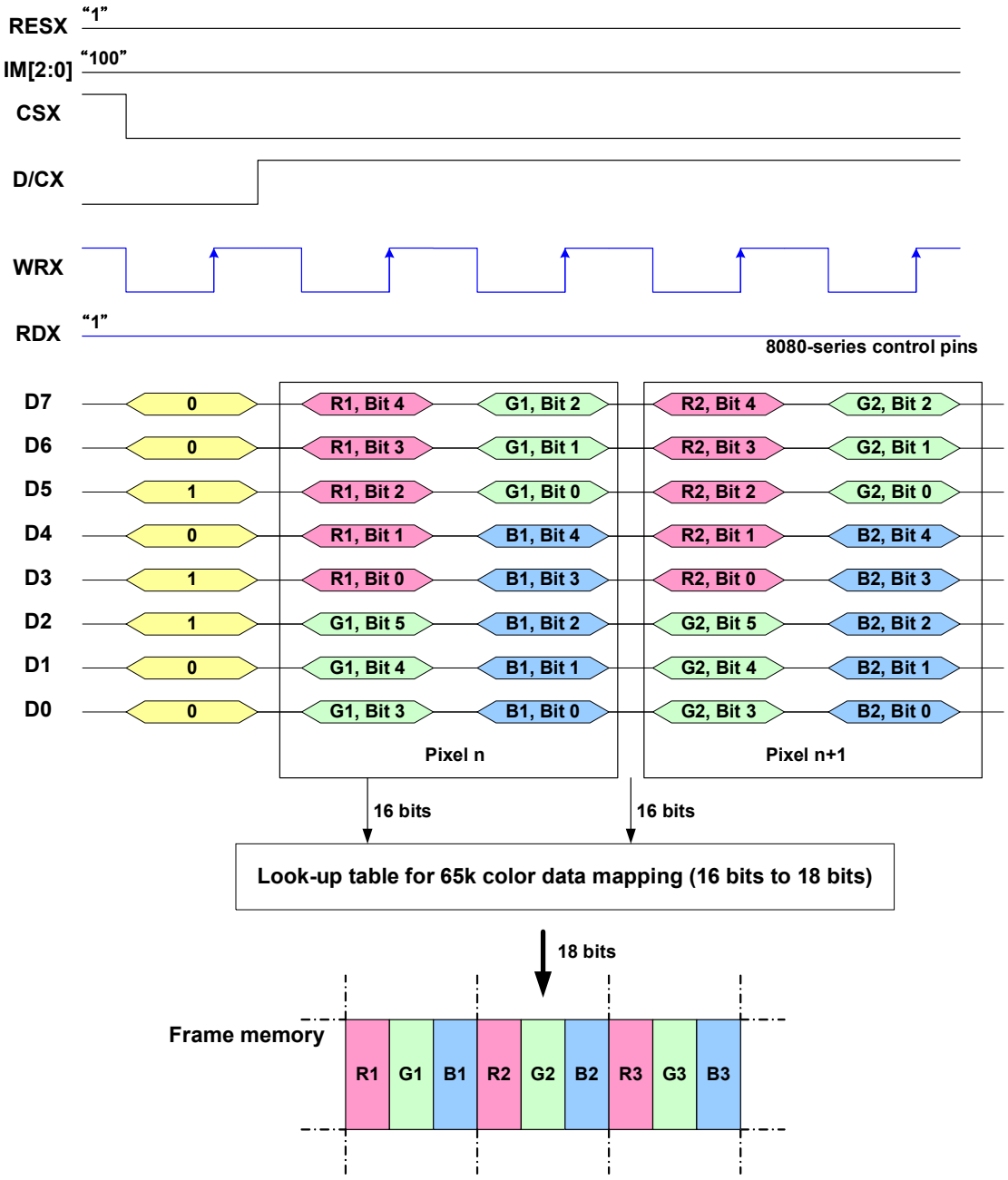
9.8.2 8-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH= “03h”



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 3-time transfer is used to transmit 1 pixel data with the 12-bit color depth information.
Note 3: '-' = Don't care - Can be set to '0' or '1'

9.8.3 8-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH= “05h”

There is 1 pixel (3 sub-pixels) per 2-byte



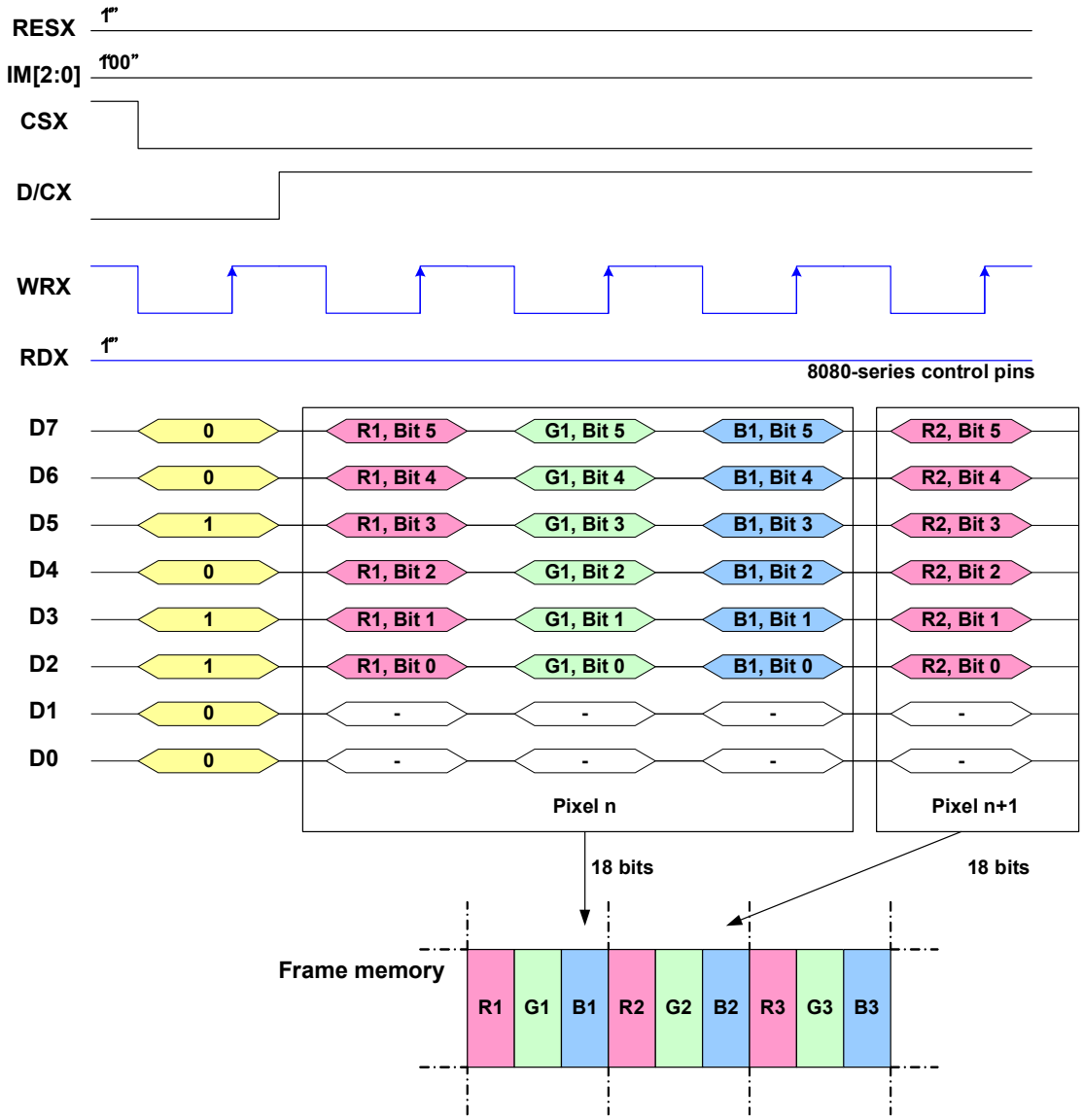
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.4 8-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH= “06h”

There is 1 pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don't care - Can be set to '0' or '1'

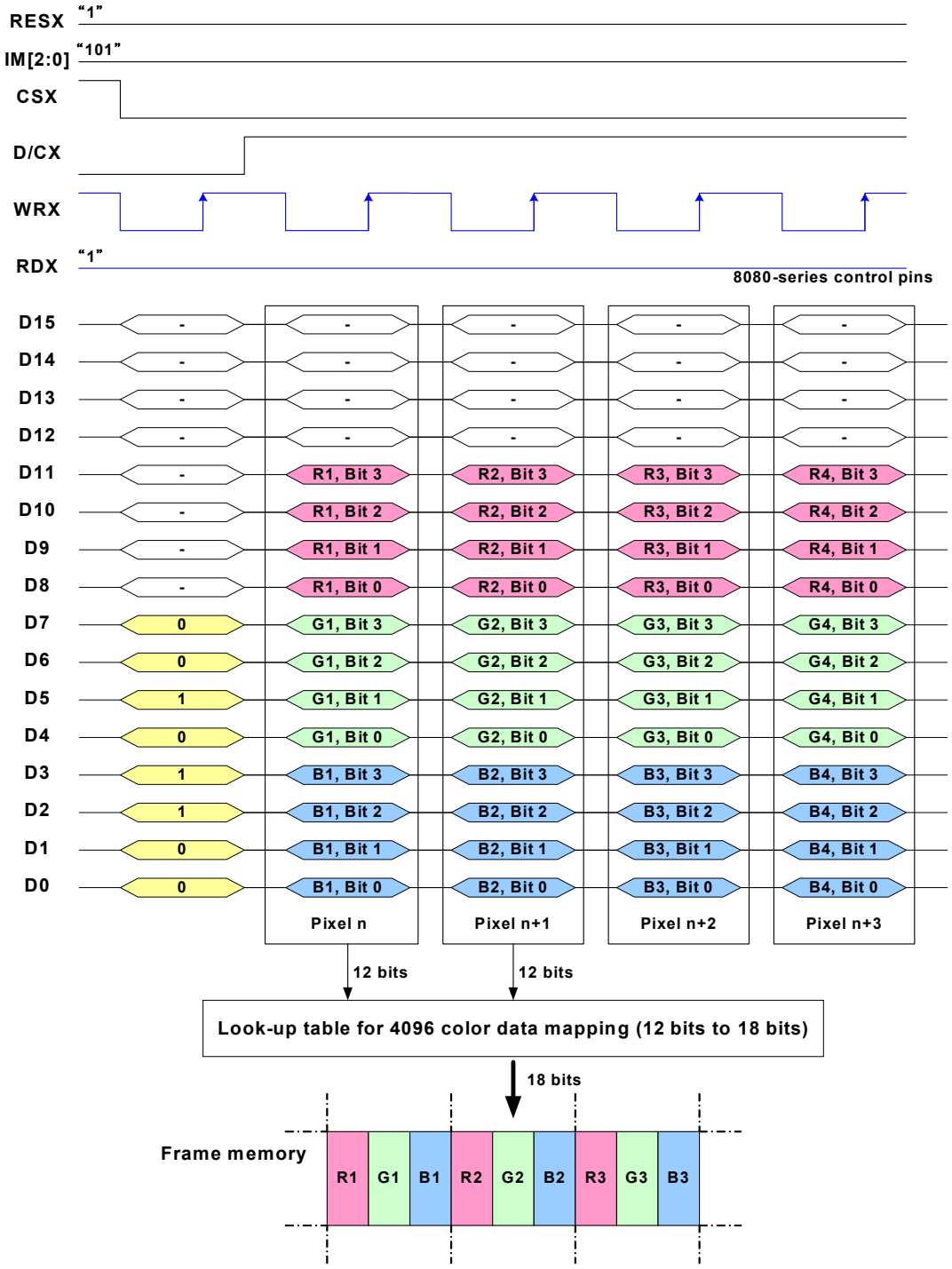
9.8.5 16-Bit Parallel Interface (IM2,IM1, IM0= “101”)

Different display data formats are available for three colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bit Input
- 65k Colors, RGB 5,6,6-bit Input
- 262k Colors, RGB 6,6,6-bit Input

9.8.6 16-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH= “03h”

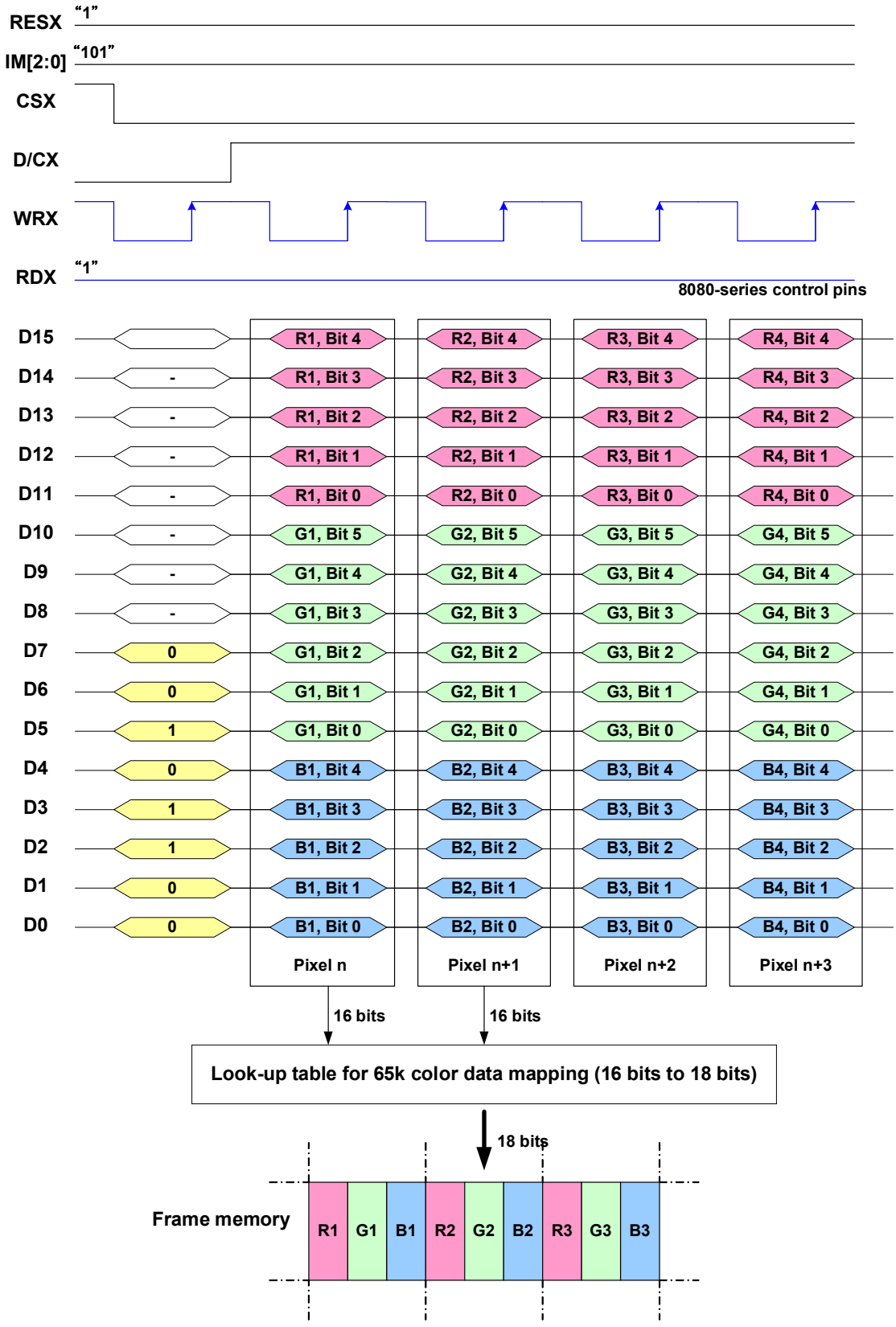
There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

9.8.7 16-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH= “05h”

There is 1 pixel (3 sub-pixels) per 1 byte



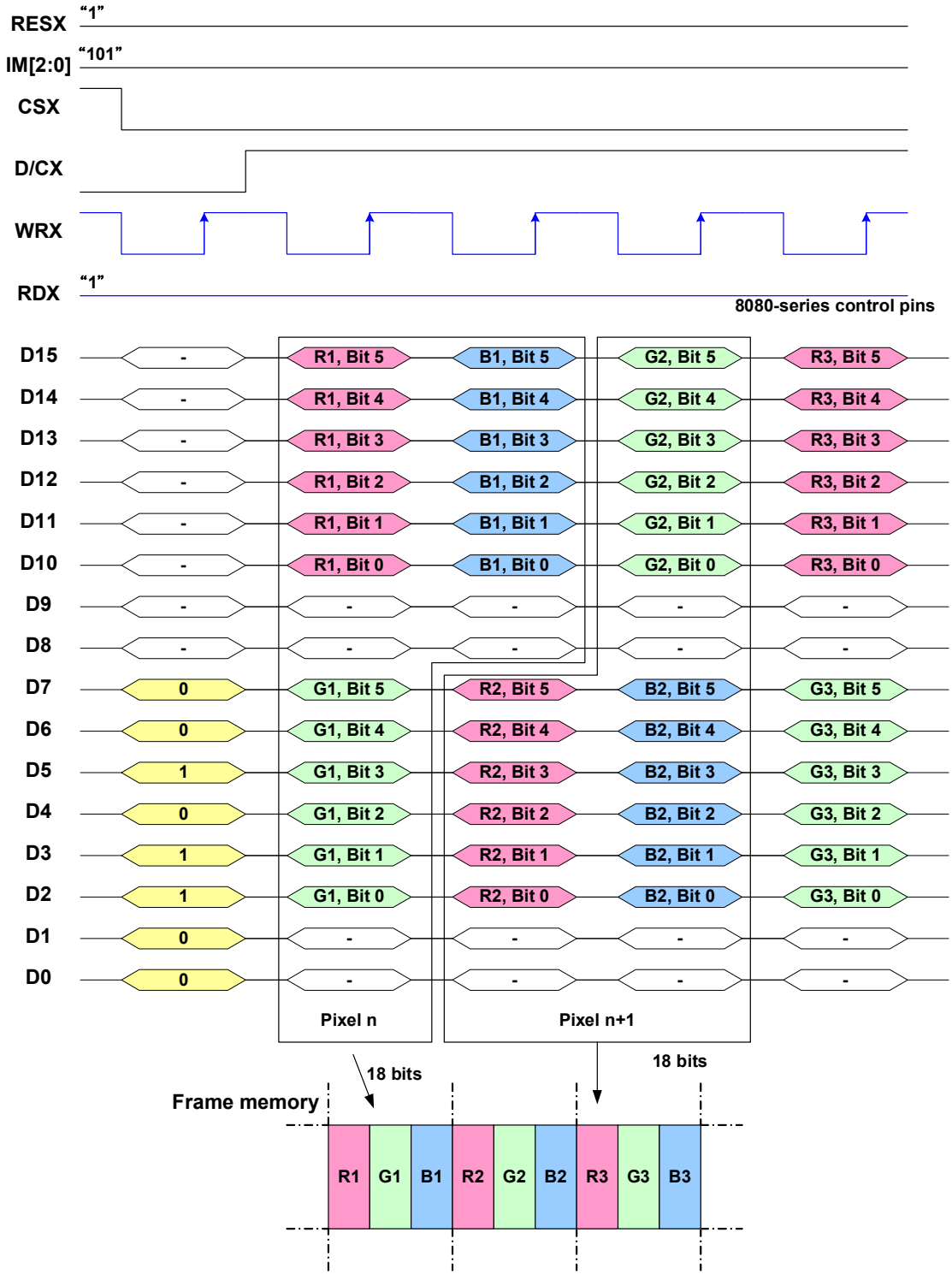
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.8 16-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH= “06h”

There are 2 pixels (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don't care - Can be set to '0' or '1'

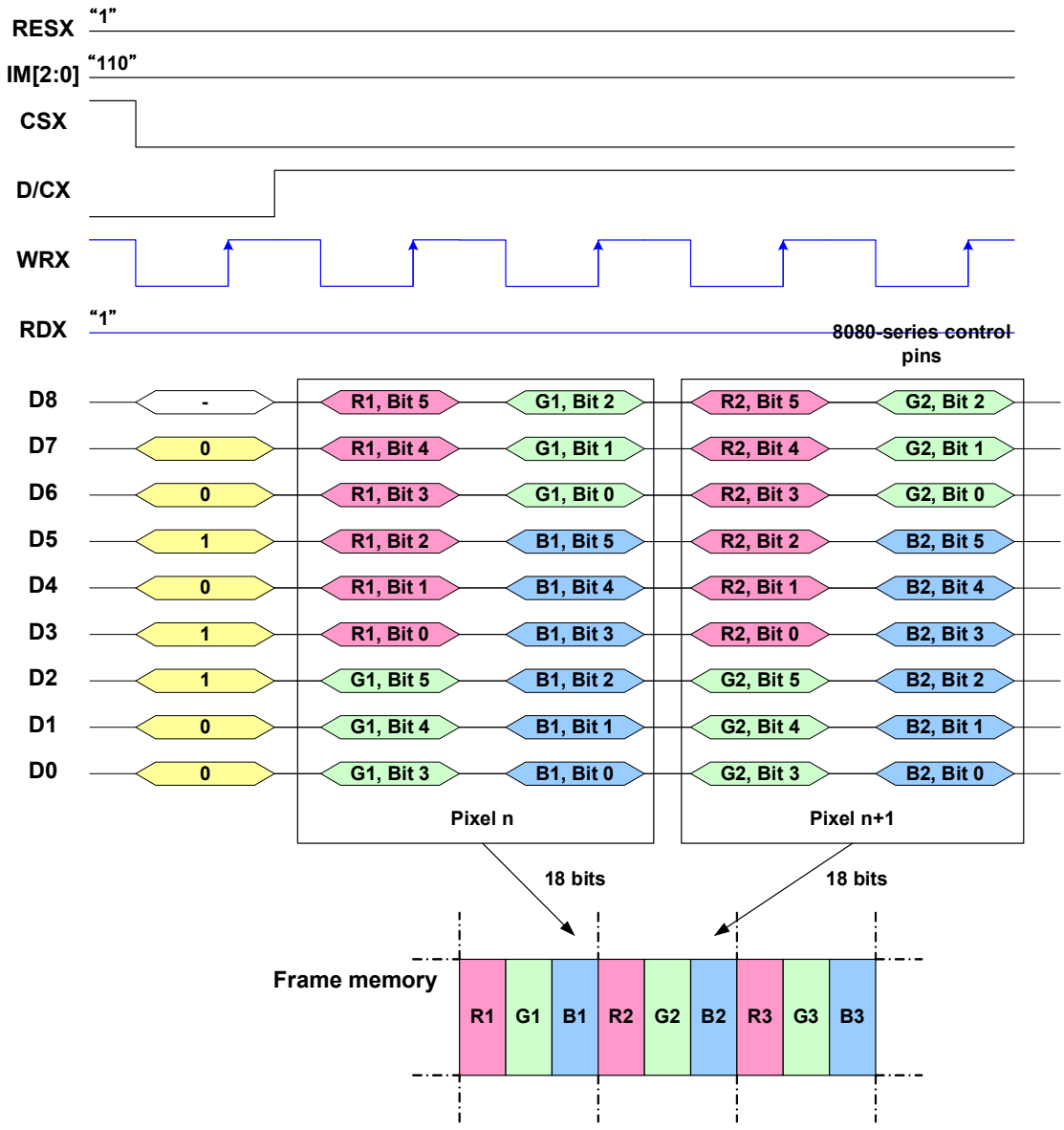
9.8.9 9-Bit Parallel Interface (IM2, IM1, IM0="110")

Different display data formats are available for three colors depth supported by listed below.

-262k colors, RGB 6,6,6-bit input

9.8.10 Write 9-bit Data for RGB 6-6-6-bit Input (262k-color)

There is 1 pixel (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

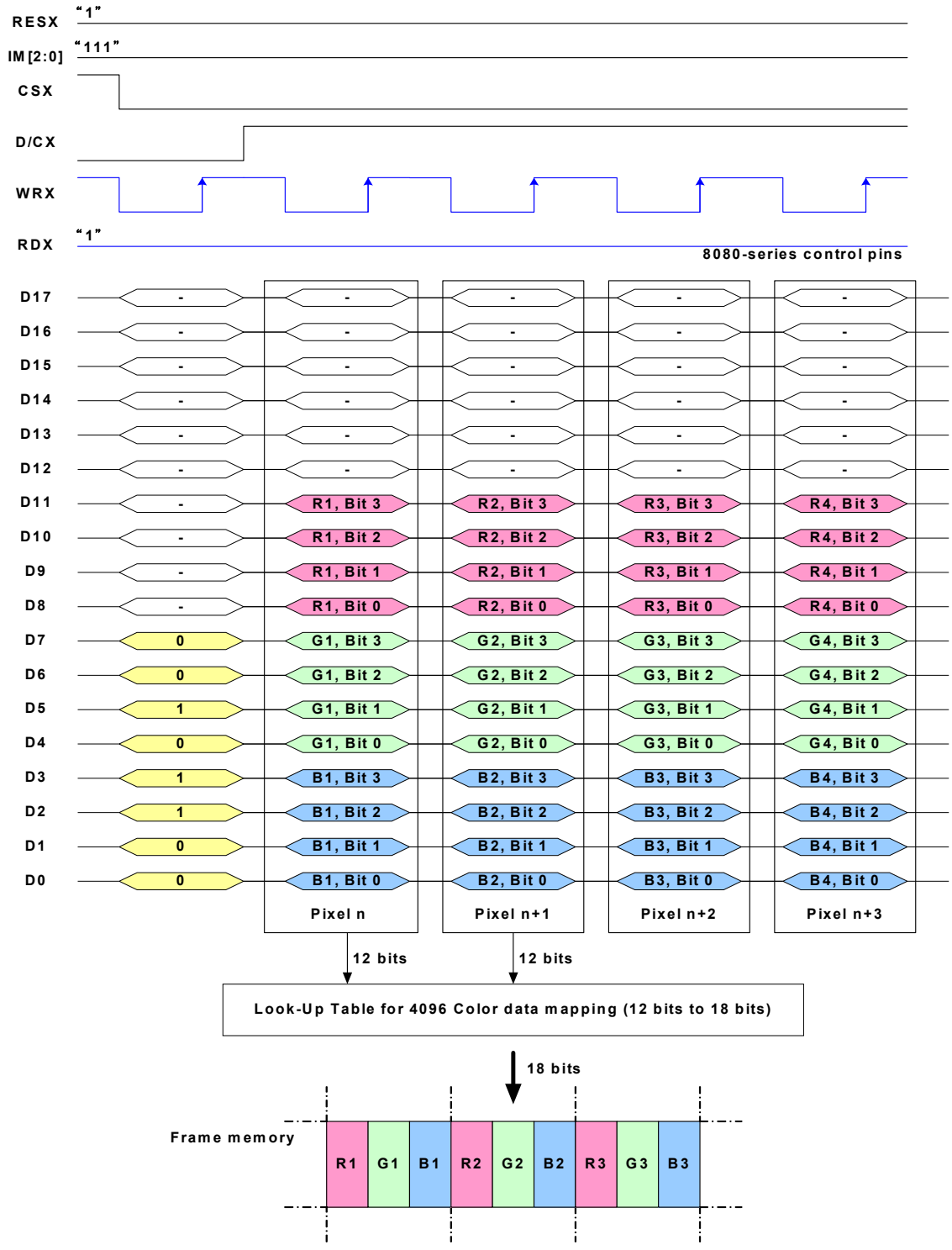
9.8.11 18-Bit Parallel Interface (IM2, IM1, IM0="111")

Different display data formats are available for three colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bit Input
- 65k Colors, RGB 5,6,5-bit Input
- 262k Colors, RGB 6,6,6-bit Input.

9.8.12 18-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH="03h"

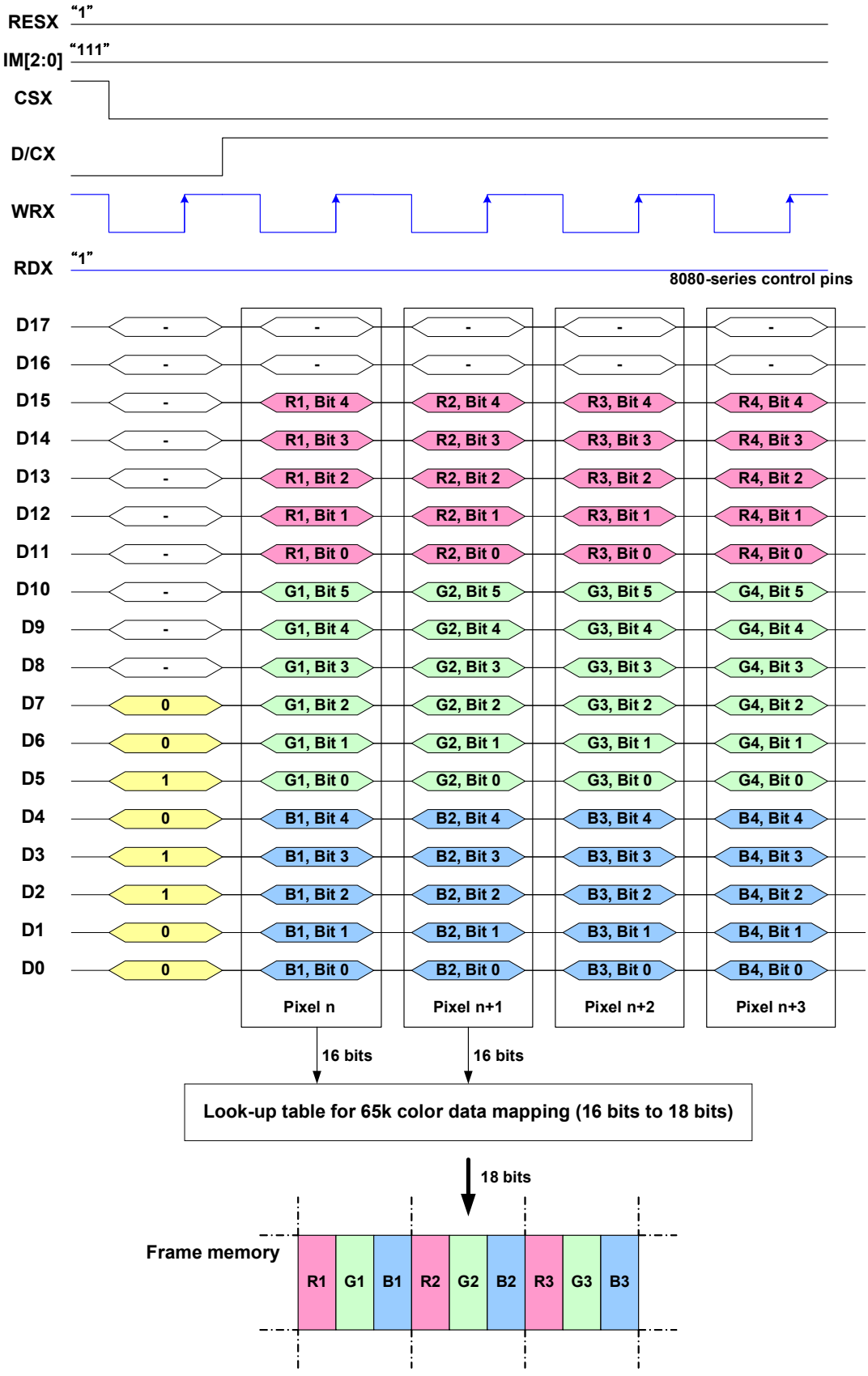
There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.

9.8.13 18-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH="05h"

There is 1 pixel (3 sub-pixels) per 1 byte

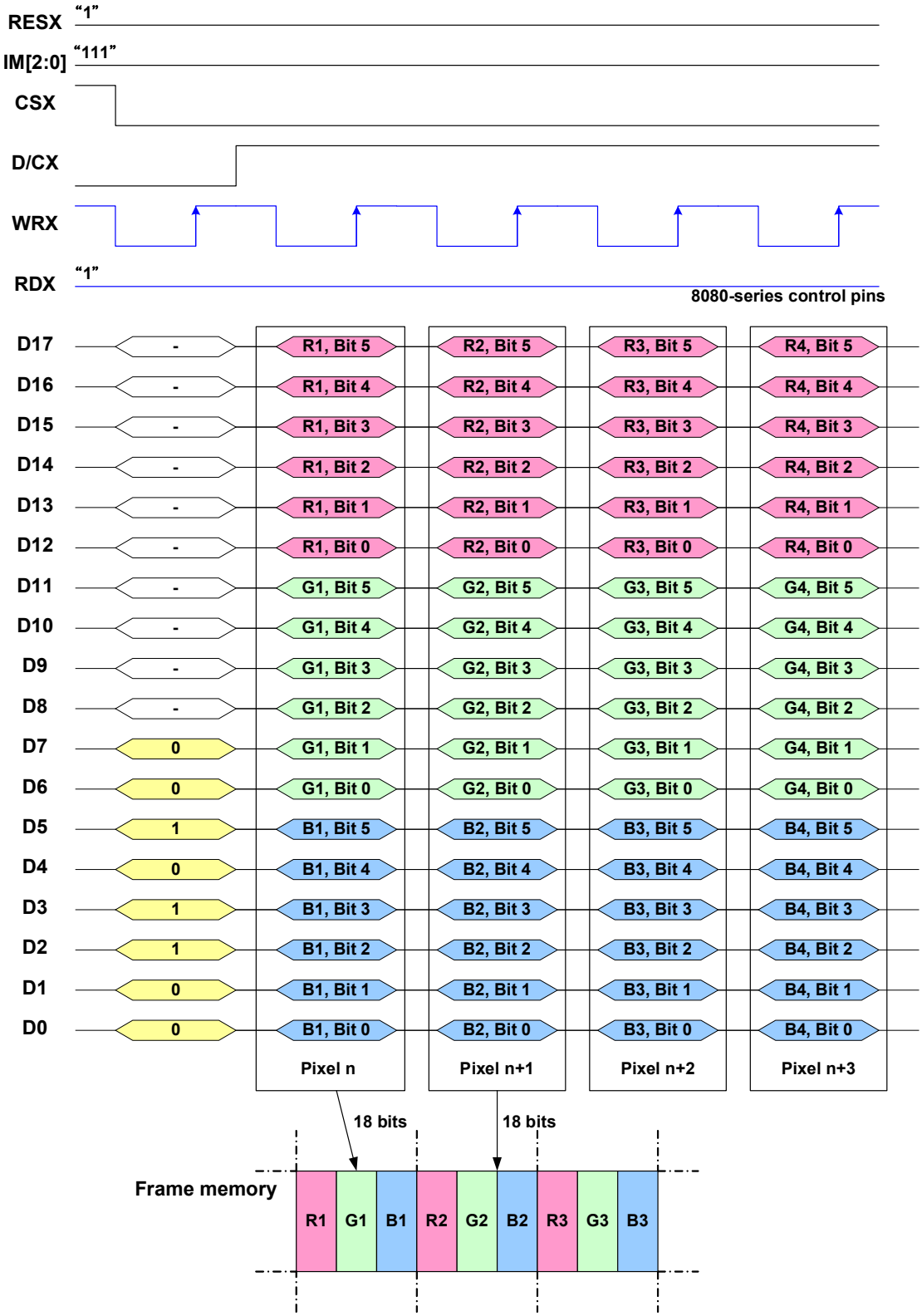


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

9.8.14 18-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH="06h"

There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

9.8.15 3-line Serial Interface

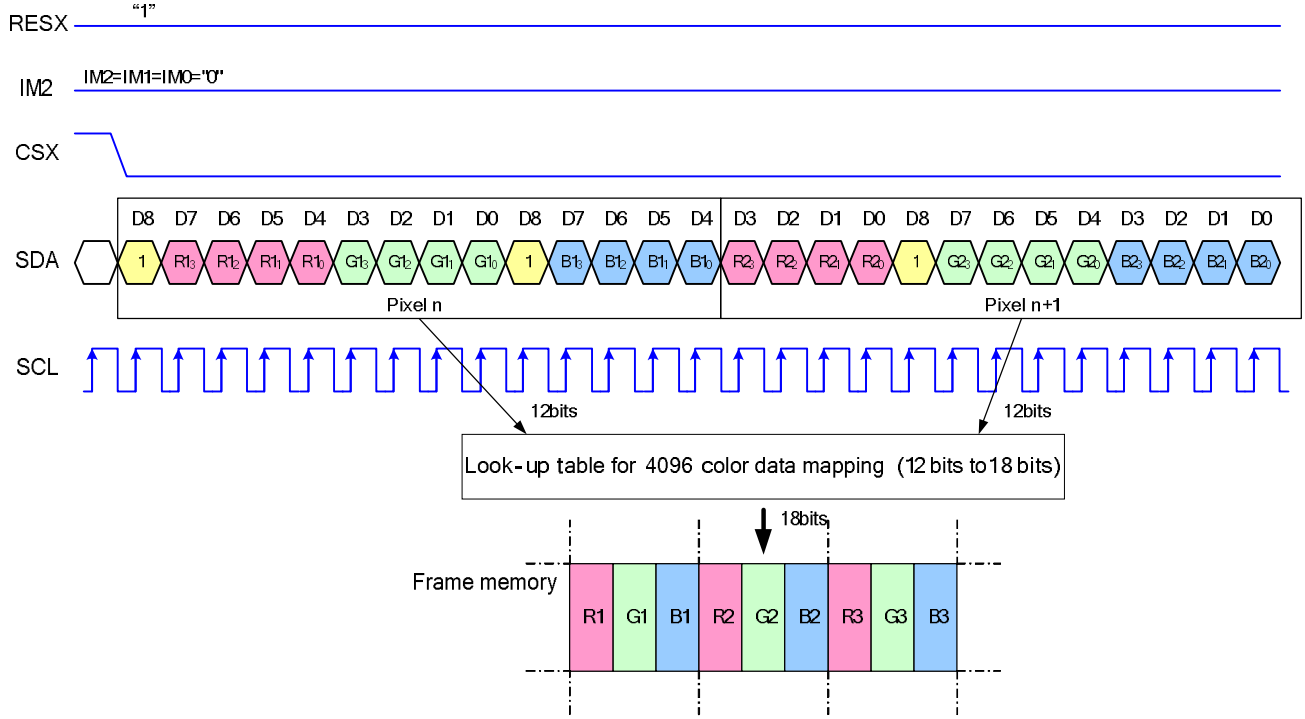
Different display data formats are available for three colors depth supported by the LCM listed below.

4k Colors, RGB 4-4-4-bit Input

65k Colors, RGB 5-6-5-bit Input

262k Colors, RGB 6-6-6-bit Input

9.8.16 Write Data for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH="03h"

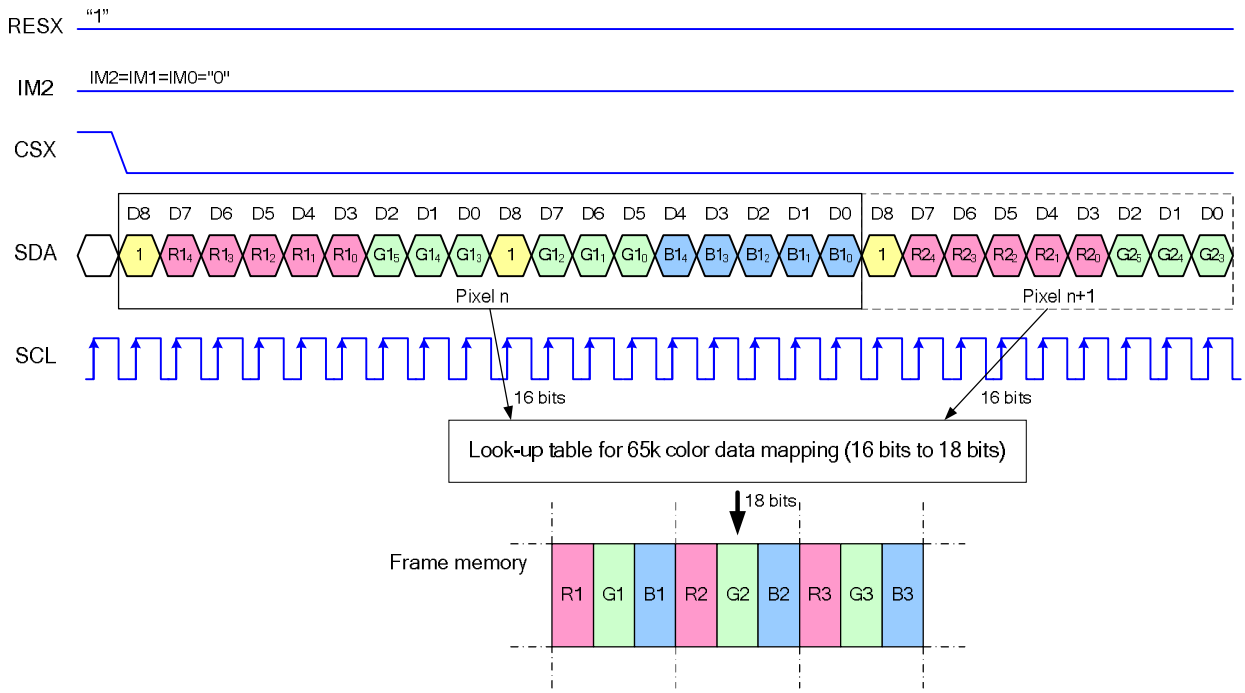


Note 1: Pixel data with the 12-bit color depth information

Note 2: The most significant bits are: Rx3, Gx3 and Bx3

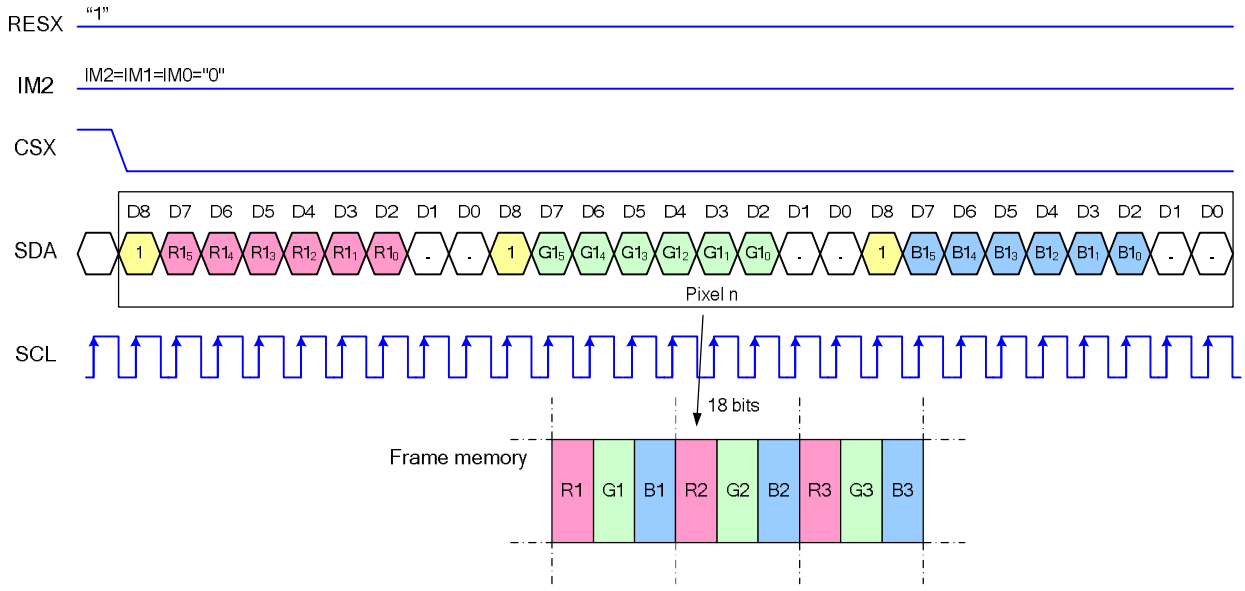
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8.17 Write Data for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH="05h"



Note 1: Pixel data with the 16-bit color depth information
Note 2: The most significant bits are: Rx4, Gx5 and Bx4
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8.18 Write Data for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH="06h"



Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8.19 4-line Serial Interface

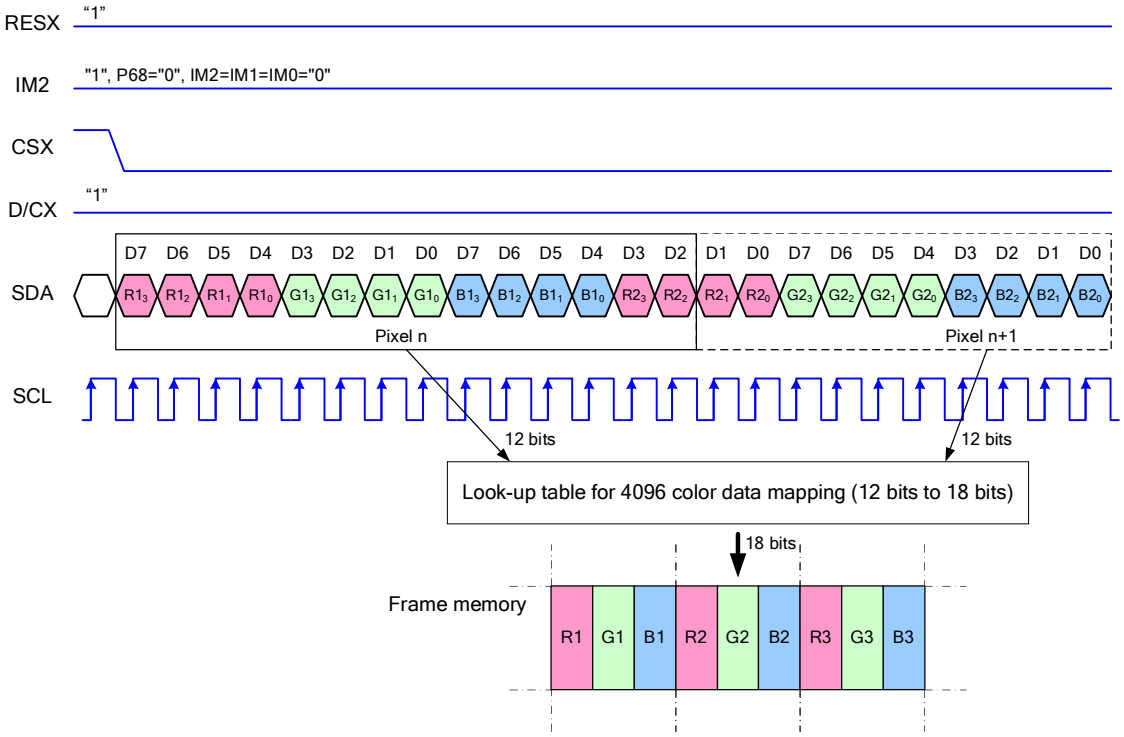
Different display data formats are available for three colors depth supported by the LCM listed below.

4k Colors, RGB 4-4-4-bit Input

65k Colors, RGB 5-6-5-bit Input

262k Colors, RGB 6-6-6-bit Input

9.8.20 Write Data for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH="03h"

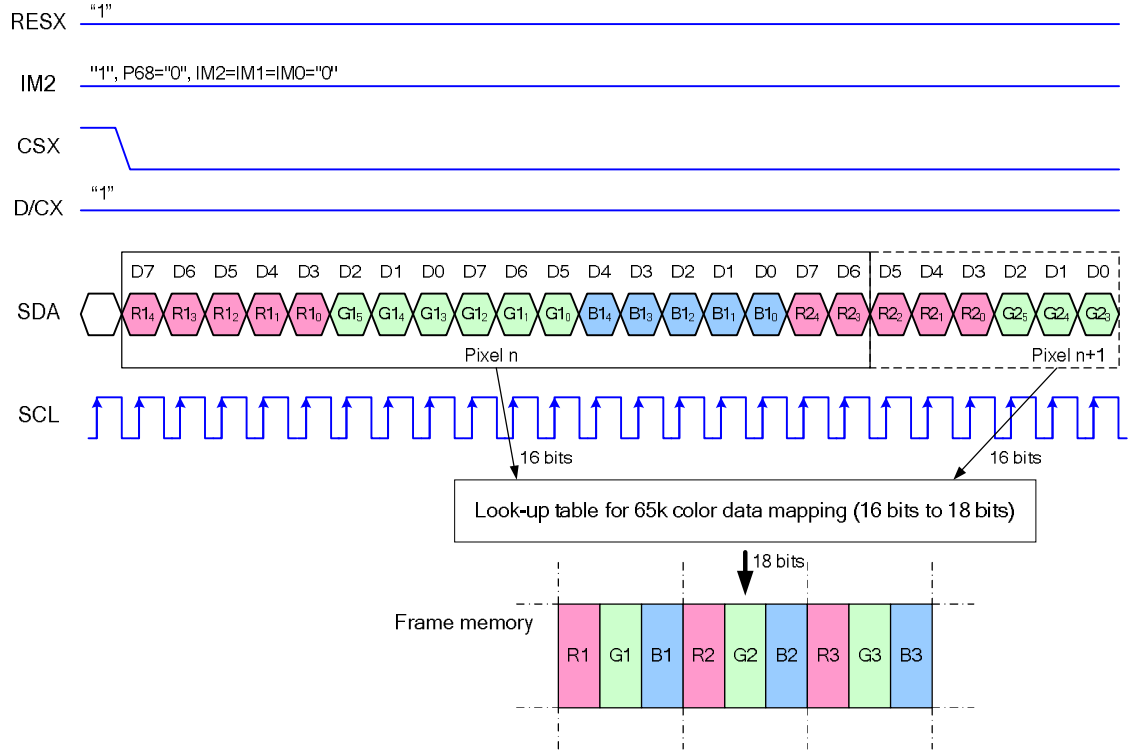


Note 1. pixel data with the 12-bit color depth information

Note 2. The most significant bits are: Rx3, Gx3 and Bx3

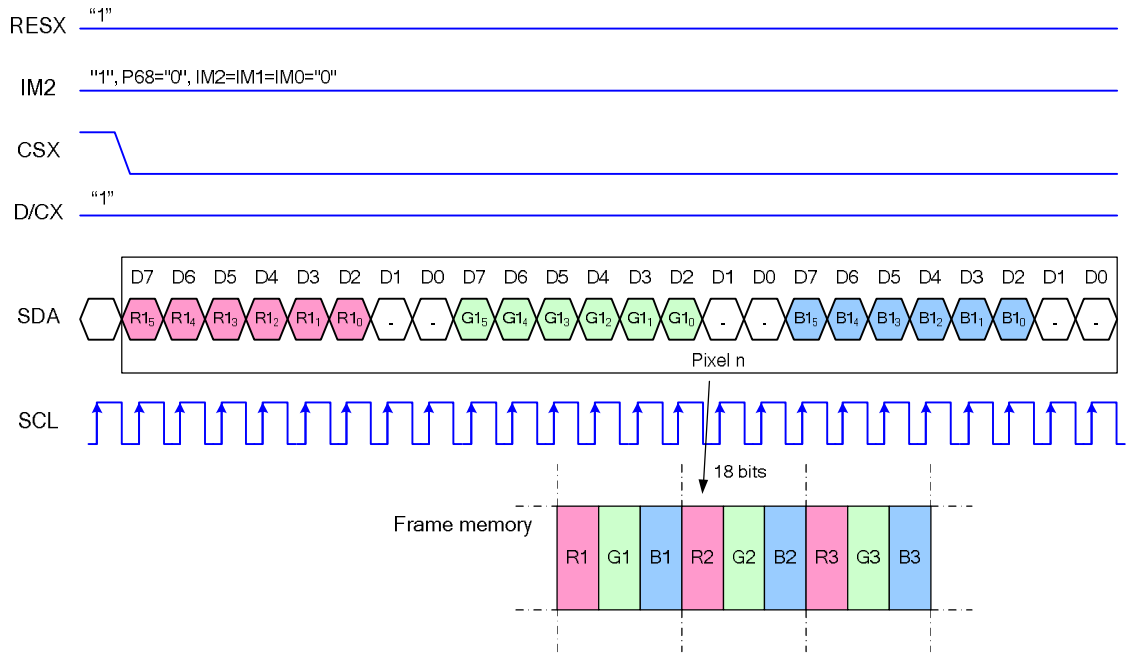
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.21 Write Data for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH="05h"



Note 1. pixel data with the 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.22 Write Data for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH="06h"



Note 1. pixel data with the 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.9 Display Data RAM

9.9.1 Configuration (GM[1:0] = “00”)

The display module has an integrated 132x162x18-bit graphic type static RAM. This 384,912-bit memory allows storing on-chip a 132xRGBx162 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

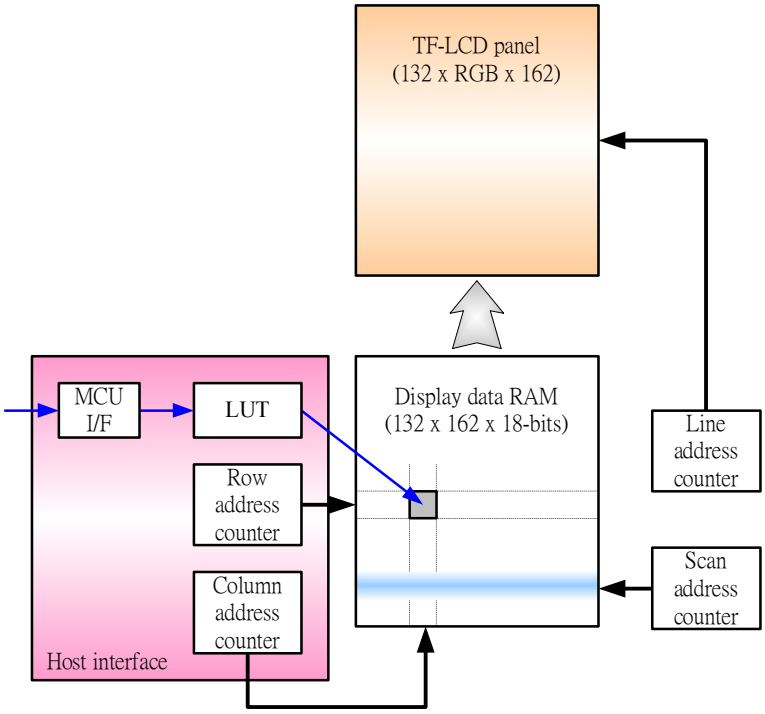
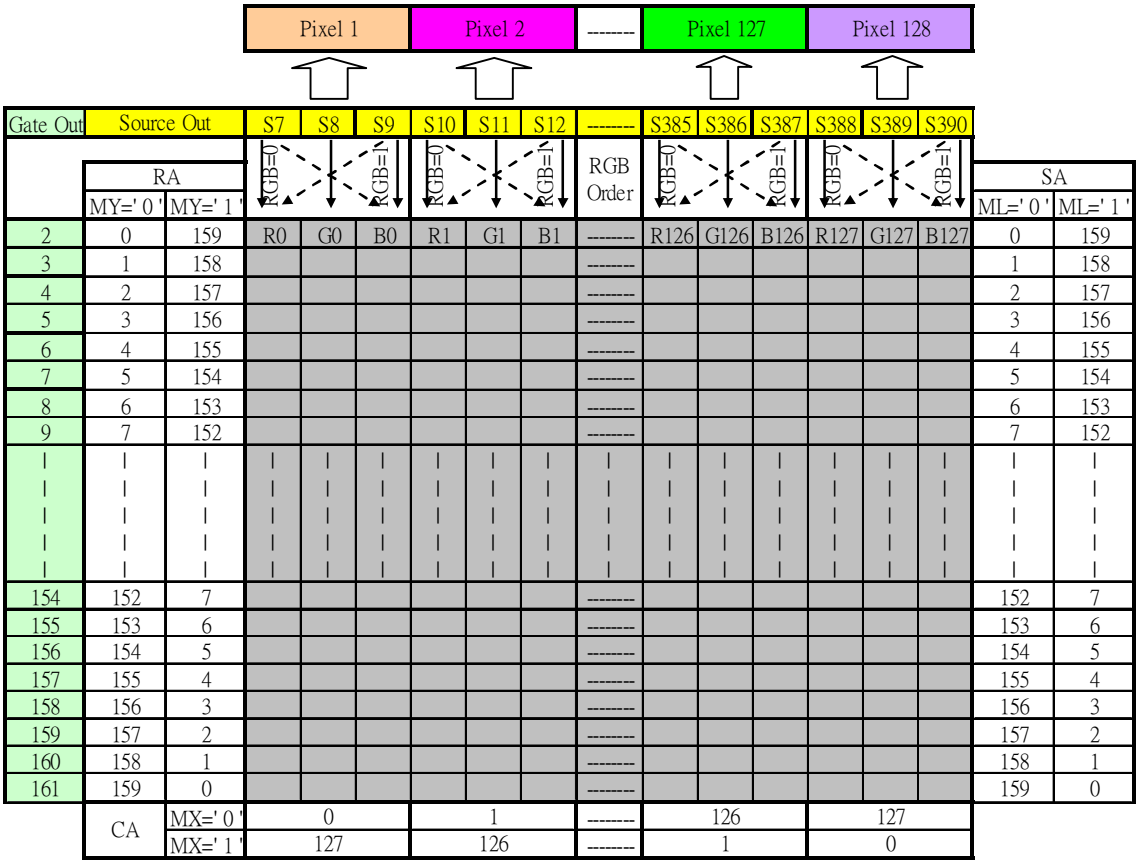


Figure 27 Display Data RAM Organization

9.9.2 Memory to Display Address Mapping

9.9.3 When using 128RGB x 160 resolution (GM[1:0] = “11”, SMX=SMY=SRGB= ‘0’)



			Pixel 1			Pixel 2			-------	Pixel 127			Pixel 128				
Gate Out	Source Out		S7	S8	S9	S10	S11	S12	-------	S385	S386	S387	S388	S389	S390		
	RA		RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1	SA	
	MY=' 0 '	MY=' 1 '														ML=' 0 '	ML=' 1 '
2	0	159	R0	G0	B0	R1	G1	B1	-------	R126	G126	B126	R127	G127	B127	0	159
3	1	158							-------							1	158
4	2	157							-------							2	157
5	3	156							-------							3	156
6	4	155							-------							4	155
7	5	154							-------							5	154
8	6	153							-------							6	153
9	7	152							-------							7	152
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
154	152	7							-------							152	7
155	153	6							-------							153	6
156	154	5							-------							154	5
157	155	4							-------							155	4
158	156	3							-------							156	3
159	157	2							-------							157	2
160	158	1							-------							158	1
161	159	0							-------							159	0
	CA	MX=' 0 '	0			1			-------	126			127				
		MX=' 1 '	127			126			-------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

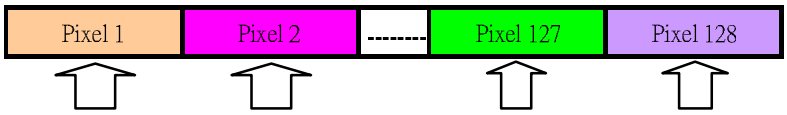
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

9.9.4 When using 132RGB x 132resolution (GM[1:0] = “01”, SMX=SMY=SRGB= ‘0’)



Gate Out	Source Out	S7	S8	S9	S10	S11	S12	--------	S385	S386	S387	S388	S389	S390		
	RA	RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1	SA	
	MY=' 0 '	MY=' 1 '													ML=' 0 '	ML=' 1 '
1	0	131	R0	G0	B0	R1	G1	B1	--------	R126	G126	B126	R127	G127	B127	0	131
2	1	130							--------							1	130
3	2	129							--------							2	129
4	3	128							--------							3	128
5	4	127							--------							4	127
6	5	126							--------							5	126
7	6	125							--------							6	125
8	7	124							--------							7	124
125	124	7							--------							124	7
126	125	6							--------							125	6
127	126	5							--------							126	5
128	127	4							--------							127	4
129	128	3							--------							128	3
130	129	2							--------							129	2
131	130	1							--------							130	1
132	131	0							--------							131	0
	CA	MX=' 0 '	0			1			--------	130			131				
		MX=' 1 '	131			130			--------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

9.9.5 When using 132RGB x 162 resolution (GM[1:0] = “00”, SMX=SMY=SRGB= ‘0’)

Gate Out	Source Out		S1	S2	S3	S4	S5	S6	-------	S391	S392	S393	S394	S395	S396		
	RA		RGB=0 ▲		RGB=1 ▼	RGB=0 ▲		RGB=1 ▼	RGB Order	RGB=0 ▲		RGB=1 ▼	RGB=0 ▲		RGB=1 ▼	SA	
	MY=' 0 '	MY=' 1 '														ML=' 0 '	ML=' 1 '
1	0	161	R0	G0	B0	R1	G1	B1	-------	R131	G131	B131	R132	G132	B132	0	161
2	1	160							-------							1	160
3	2	159							-------							2	159
4	3	158							-------							3	158
5	4	157							-------							4	157
6	5	156							-------							5	156
7	6	155							-------							6	155
8	7	154							-------							7	154
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
155	154	7							-------							154	7
156	155	6							-------							155	6
157	156	5							-------							156	5
158	157	4							-------							157	4
159	158	3							-------							158	3
160	159	2							-------							159	2
161	160	1							-------							160	1
162	161	0							-------							161	0
	CA	MX=' 0 '	0			1			-------	130			131				
		MX=' 1 '	131			130			-------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

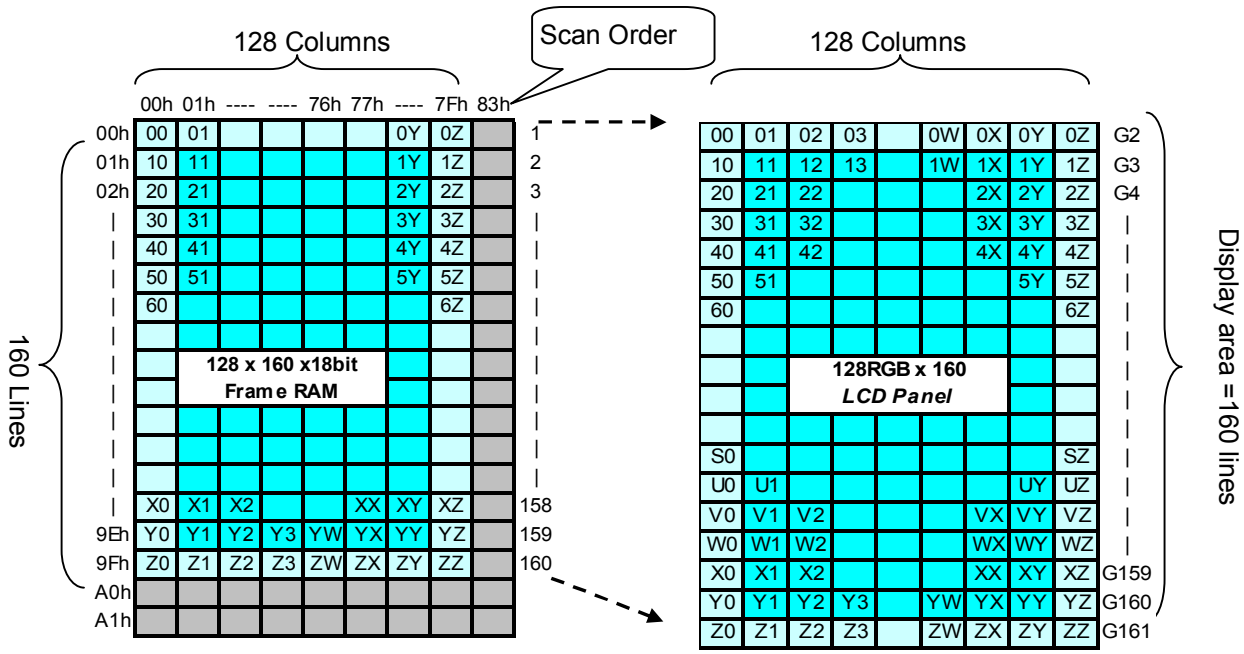
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

9.9.6 Normal Display On or Partial Mode On

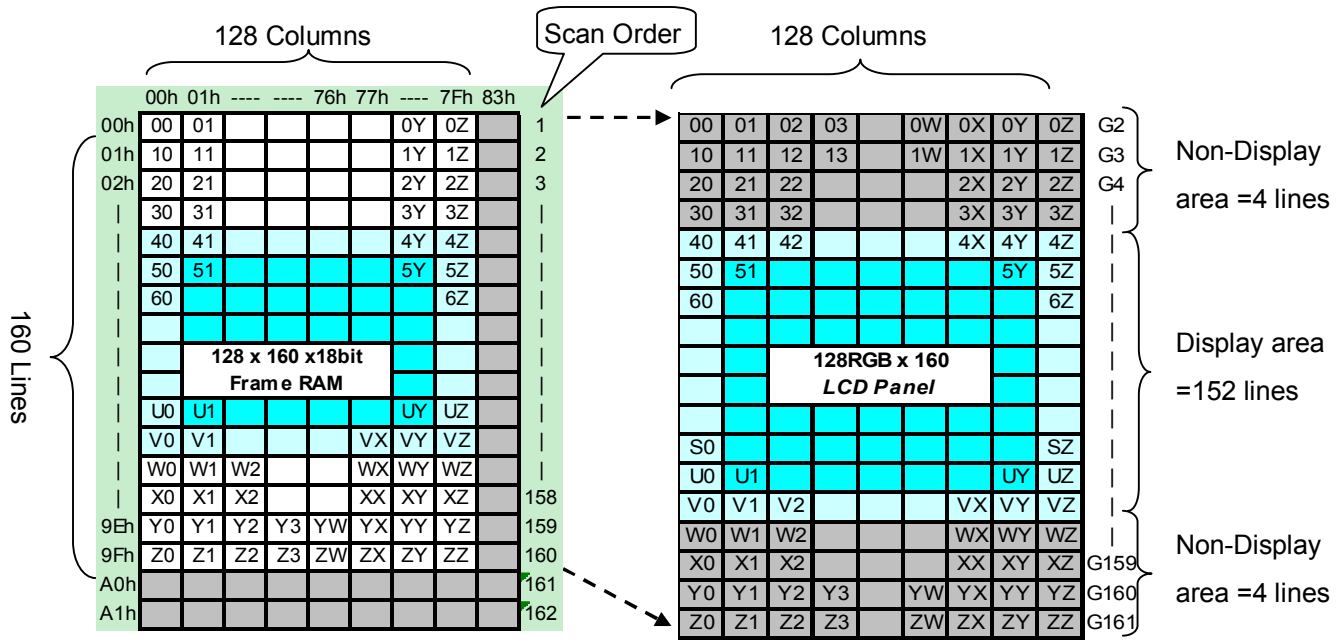
9.9.7 When using 128RGB x 160 resolution (GM[1:0] = "11")

In this mode, the content of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



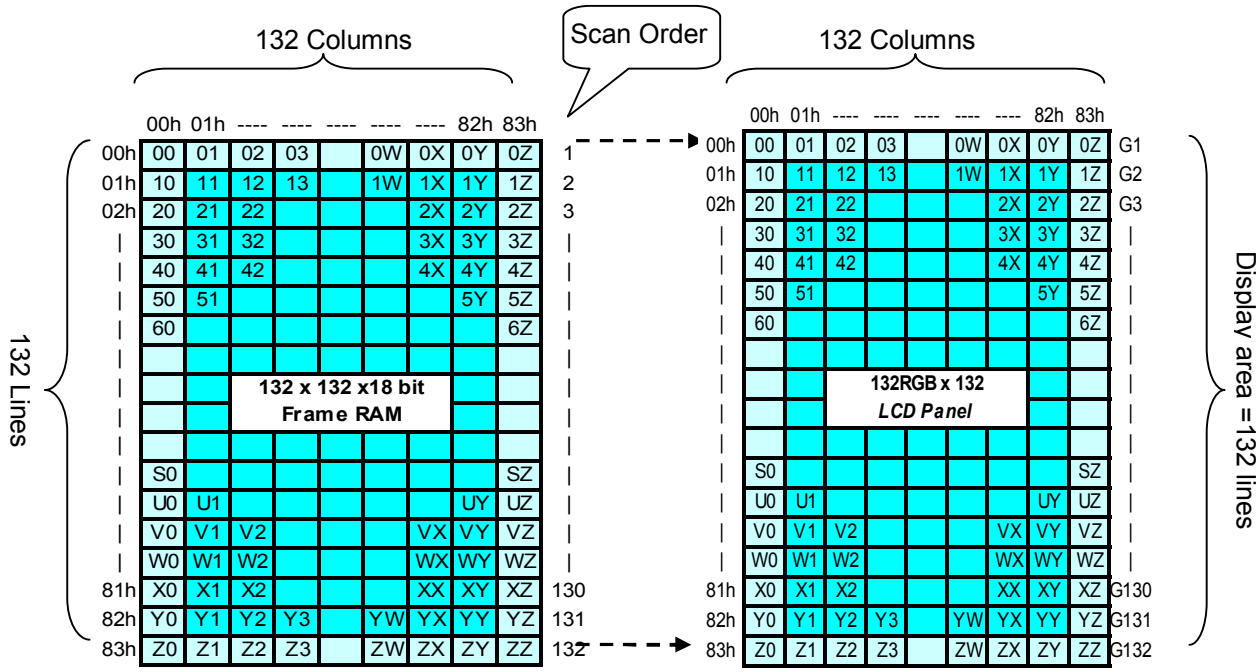
2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Bh, MX=MV=ML='0' ,SMX=SMY='0')



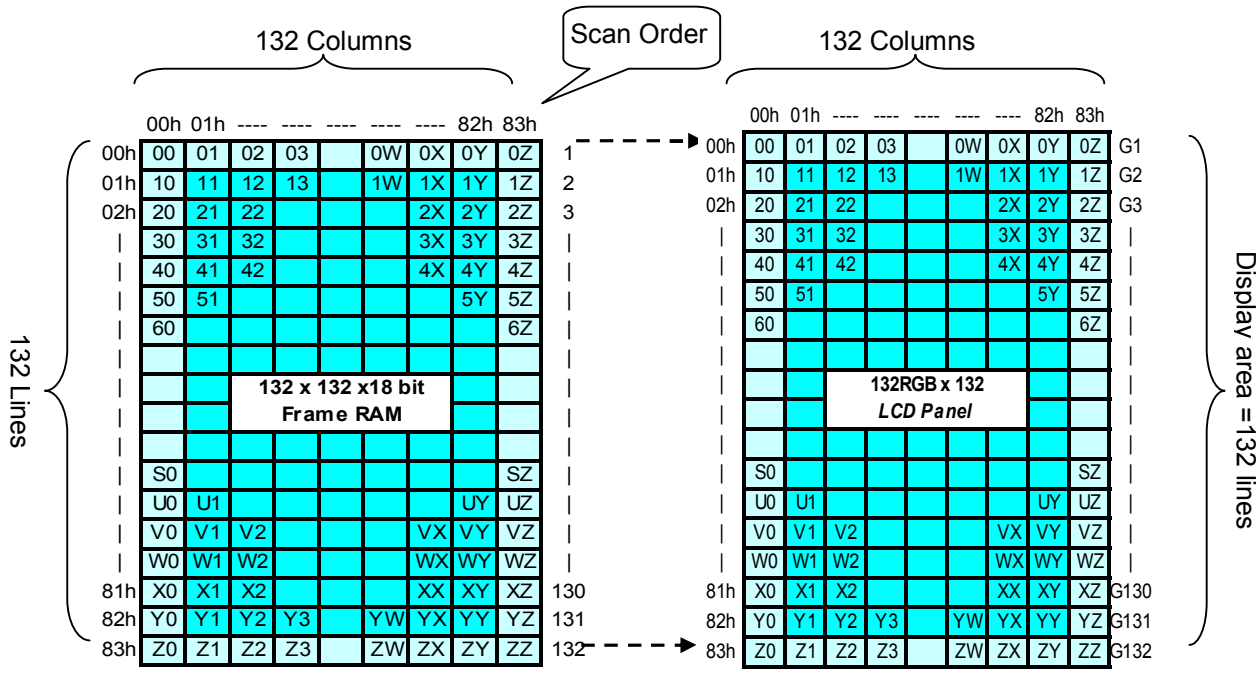
9.9.8 When using 128RGB x 160 resolution (GM[1:0] = “01”)

In this mode, the content of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to 83h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML=’0’, SMX=SMY=’0’)



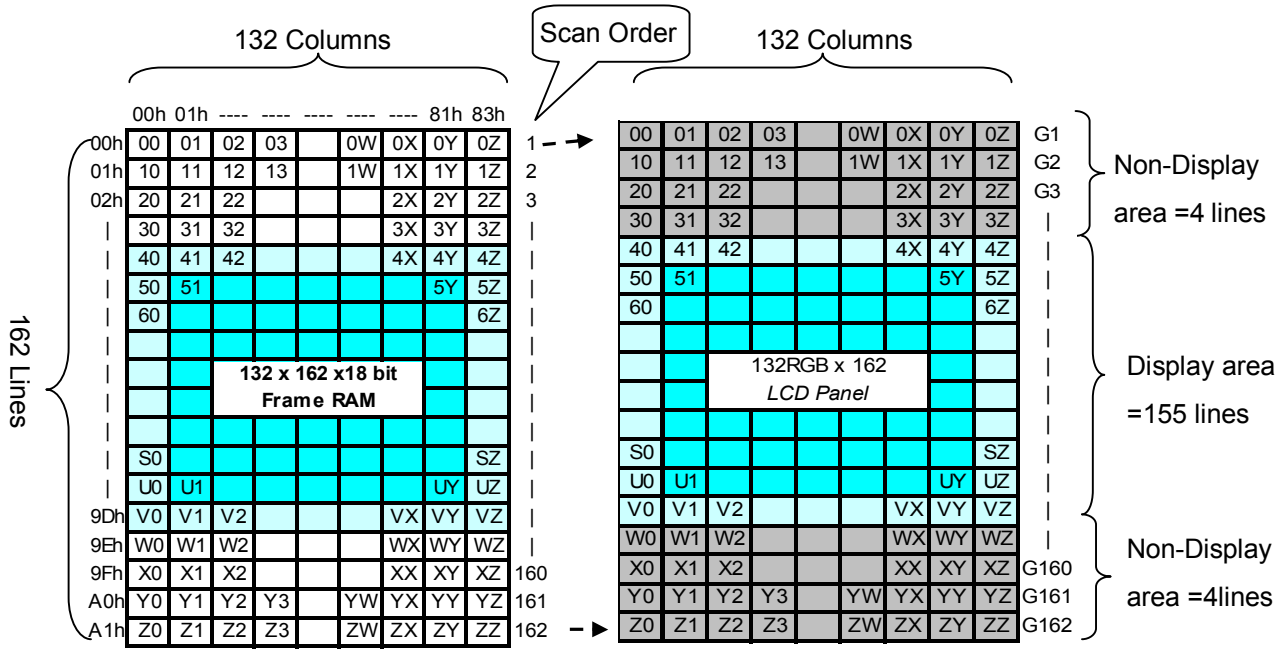
2). Example for Partial Display On (PSL[7:0]=00h,PEL[7:0]=83h, MX=MV=ML=’0’ ,SMX=SMY=’0’)



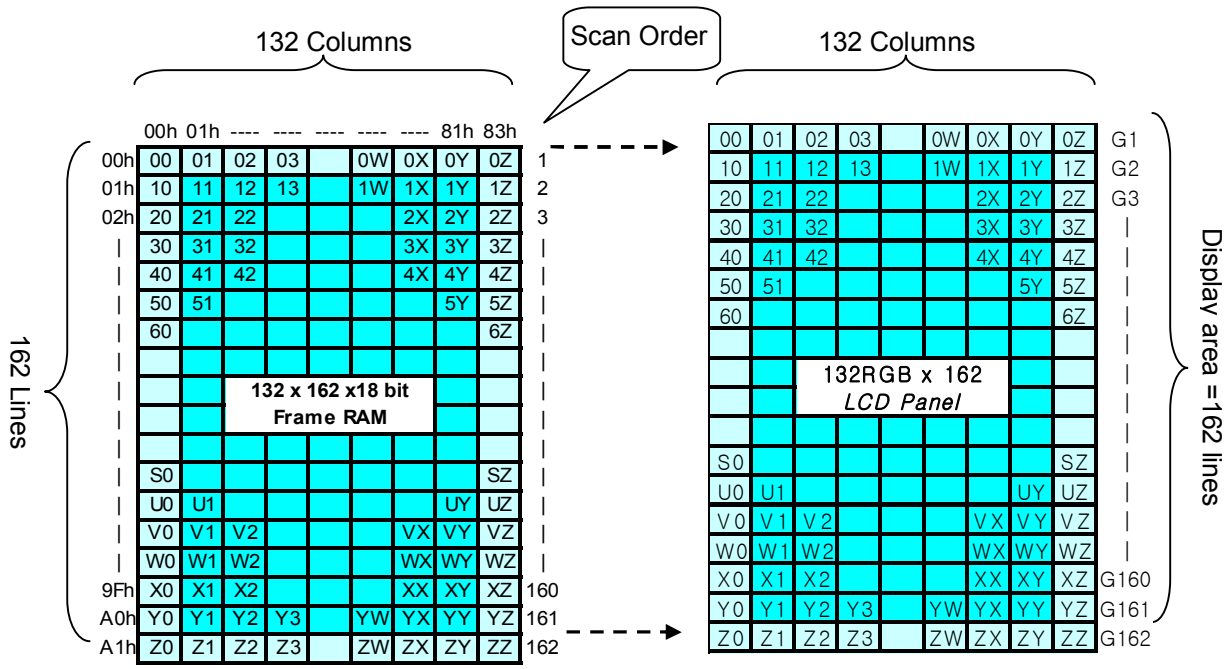
9.9.9 When using 132RGB x 162 resolution (GM[1:0] = "00")

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0)

1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Dh, MX=MV=ML='0' ,SMX=SMY='0')



9.10 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.
Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=127 (83h), YE=161 (A1h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET and MADCTL” (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.10 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section 9.11 below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

9.11 Memory Data Write/ Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.

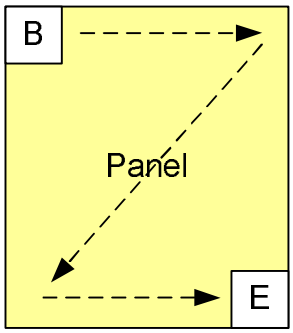


Figure 28 Data Streaming order

9.11.1 When 128RGBx160 (GM= “11”)

MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (159-Physical Row Pointer)
0	1	0	Direct to (127-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (127-Physical Column Pointer)	Direct to (159-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (127-Physical Column Pointer)
1	1	1	Direct to (159-Physical Row Pointer)	Direct to (127-Physical Column Pointer)

9.11.2 When 132RGBx132 (GM= “01”)

MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (131-Physical Row Pointer)
0	1	0	Direct to (131-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (131-Physical Column Pointer)	Direct to (131-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (131-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (131-Physical Column Pointer)
1	1	1	Direct to (131-Physical Row Pointer)	Direct to (131-Physical Column Pointer)

9.11.3 When 132RGBx162 (GM= “00”)

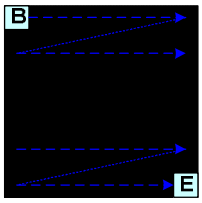
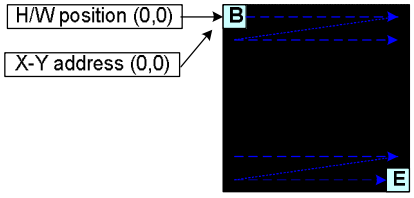
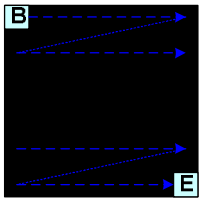
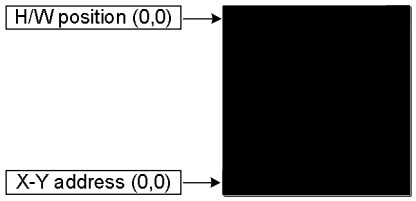
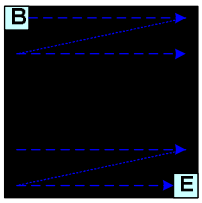
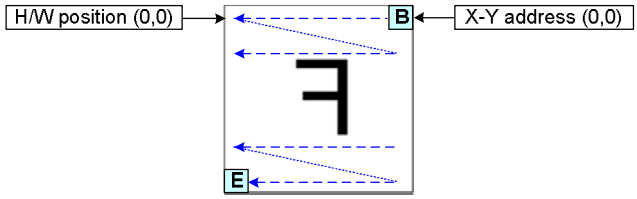
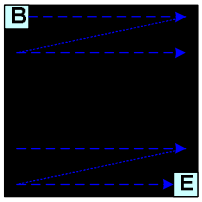
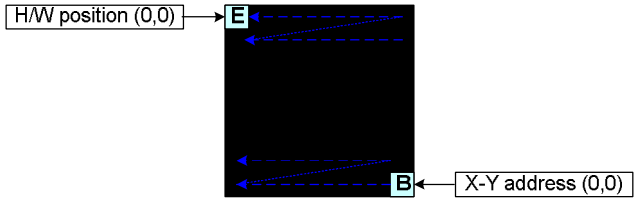
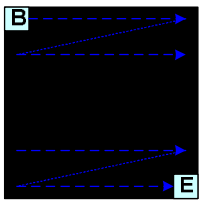
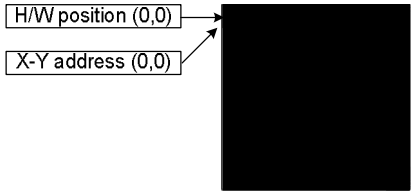
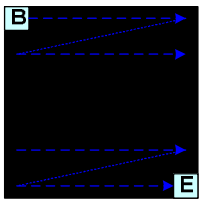
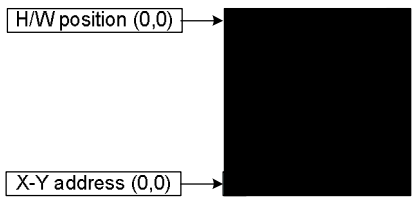
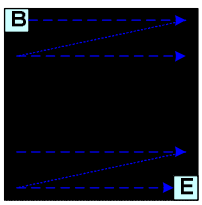
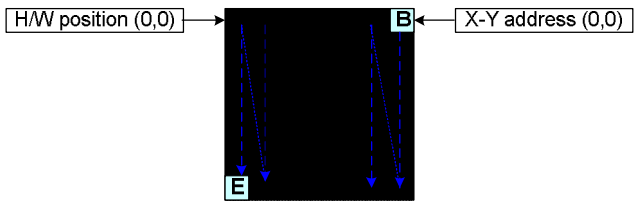
MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (161-Physical Row Pointer)
0	1	0	Direct to (131-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (131-Physical Column Pointer)	Direct to (161-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (161-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (131-Physical Column Pointer)
1	1	1	Direct to (161-Physical Row Pointer)	Direct to (131-Physical Column Pointer)

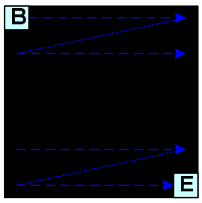
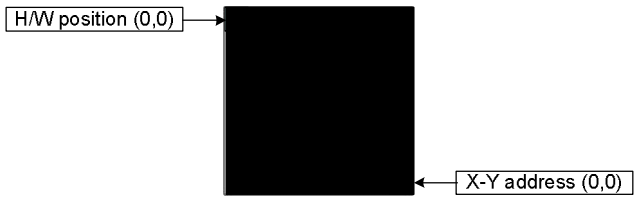
Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1page counter value on the Frame Memory.

9.11.4 Frame Data Write Direction According to the MADCTL Parameters (MV, MX and MY)

Display Data Direction	MADCTL Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		

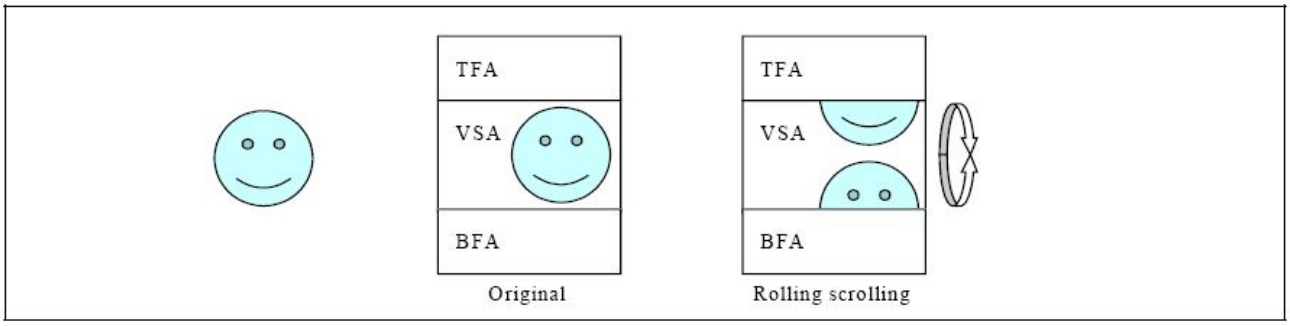
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

9.11.5 Scroll Address Circuit

The circuit associates lines on DDRAM with Gate output. ST7735S processes signals for the liquid crystal display on 1-line basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in line.

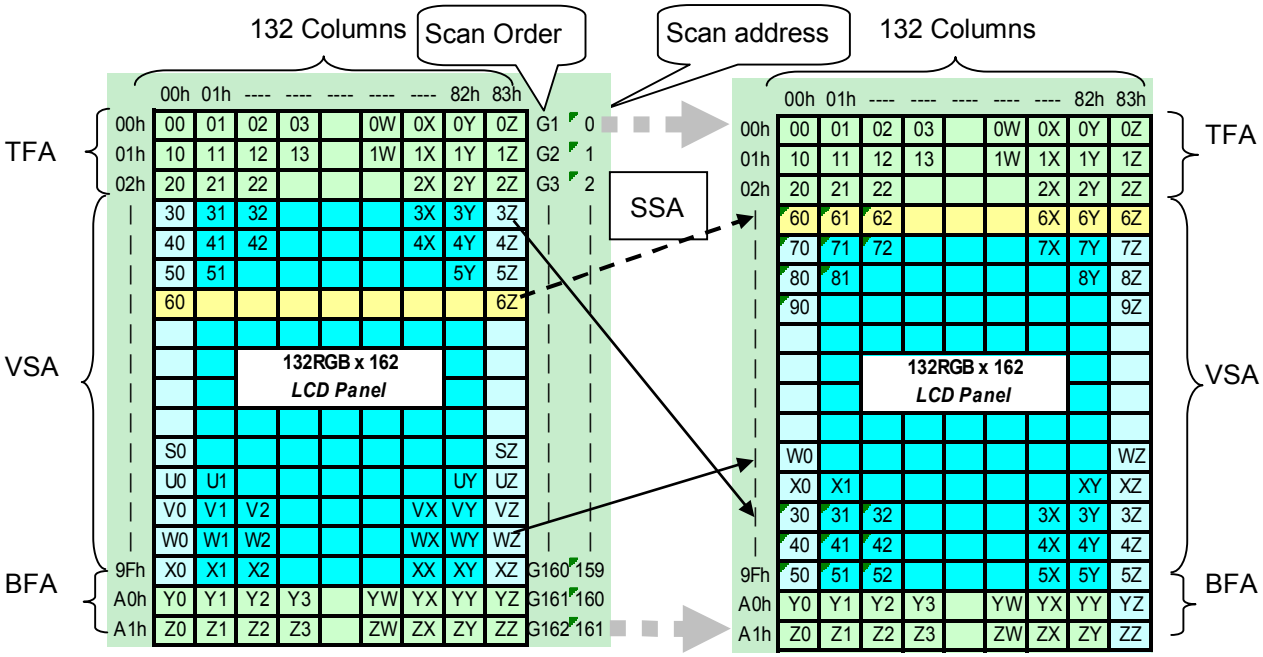
9.11.6 Vertical Scroll Mode

There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h)

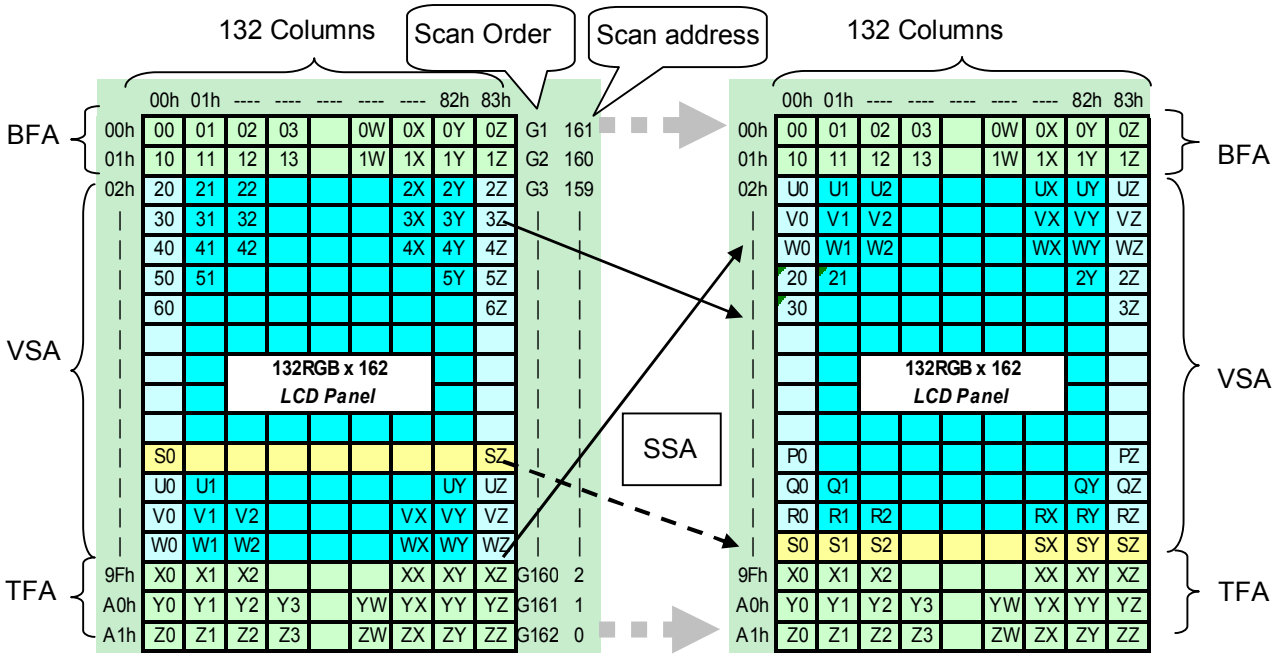


When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =162. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example 1) Panel size=132(RGB) x 162, TFA =3, VSA=157, BFA=2, SSA=6, MADCTR (ML) =0: Rolling Scroll



Example 2) Panel size=132(RGB) x 162, TFA =3, VSA=157, BFA=2, SSA=6, MADCTR (ML) =1: Rolling Scroll.



9.11.7 Vertical Scroll Example

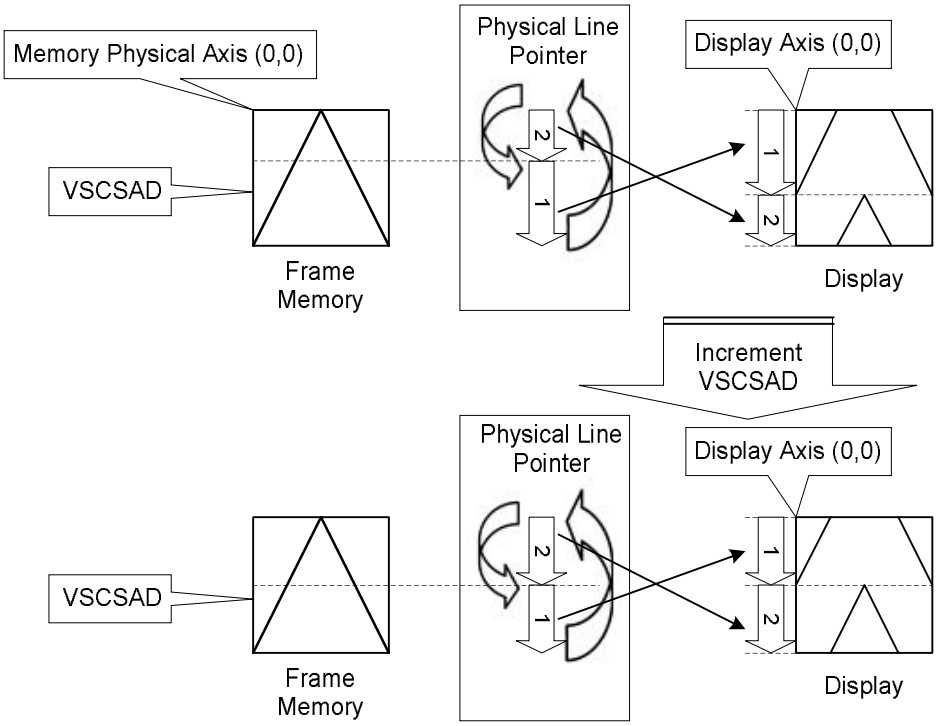
There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

9.11.8 Case 1: TFA + VSA + BFA<162

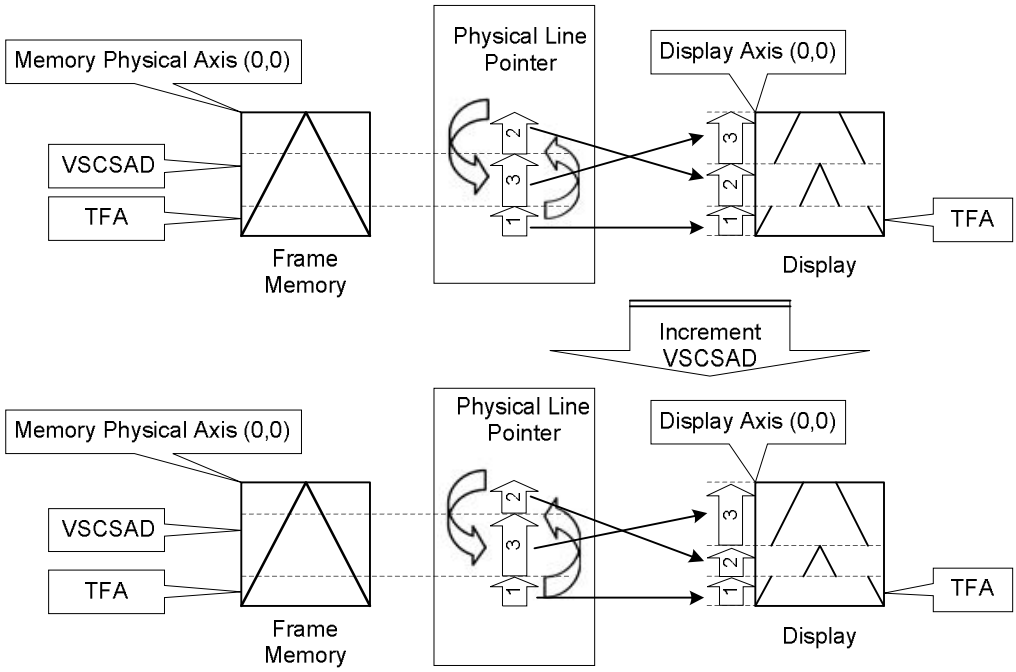
N/A. Do not set TFA + VSA + BFA<162. In that case, unexpected picture will be shown.

9.11.9 Case 2: TFA + VSA + BFA=162 (Rolling Scrolling)

Example 2-a) When MADCTR parameter ML="0", TFA=0, VSA=162, BFA=0 and VSCSAD=40



Example 2-b) When MADCTR parameter ML="1", TFA=10, VSA=152, BFA=0 and VSCSAD=30

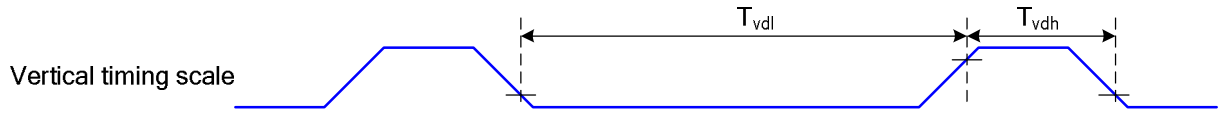


9.12 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

9.12.1 Tearing Effect Line Modes

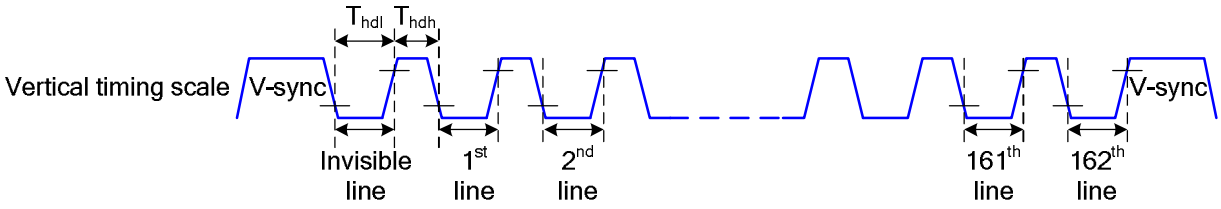
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

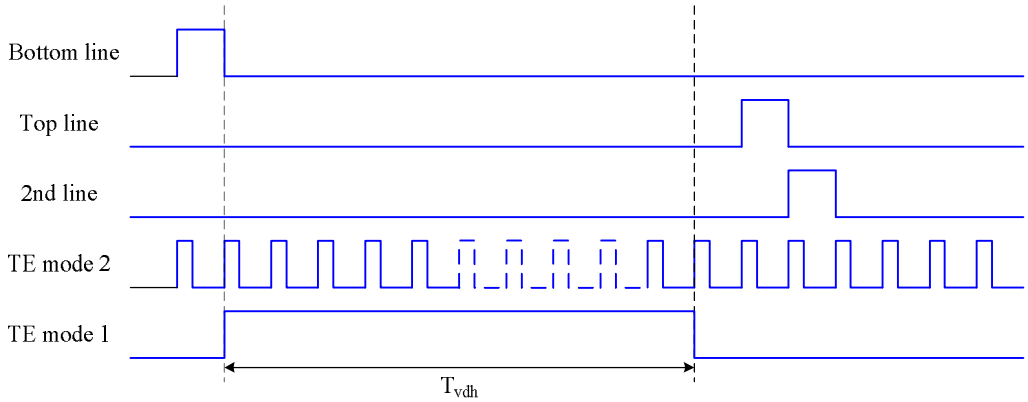
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

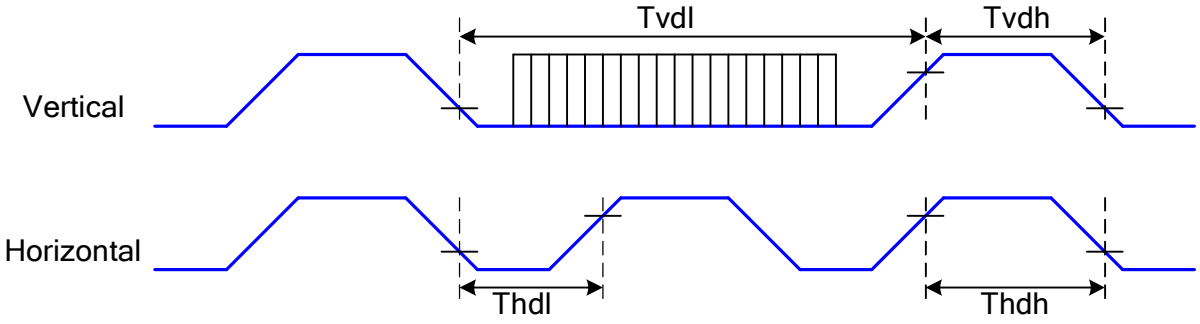
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

9.12.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:

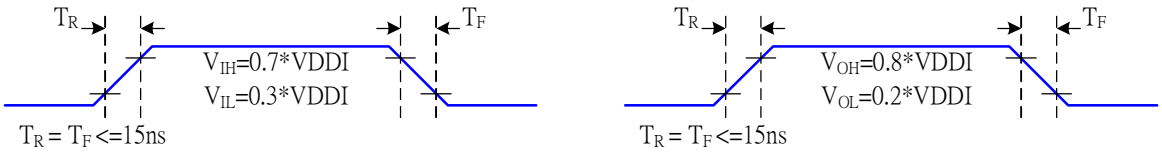


Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	33	-	µs	
thdh	Horizontal Timing Low Duration	25	500	µs	

Table 13 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

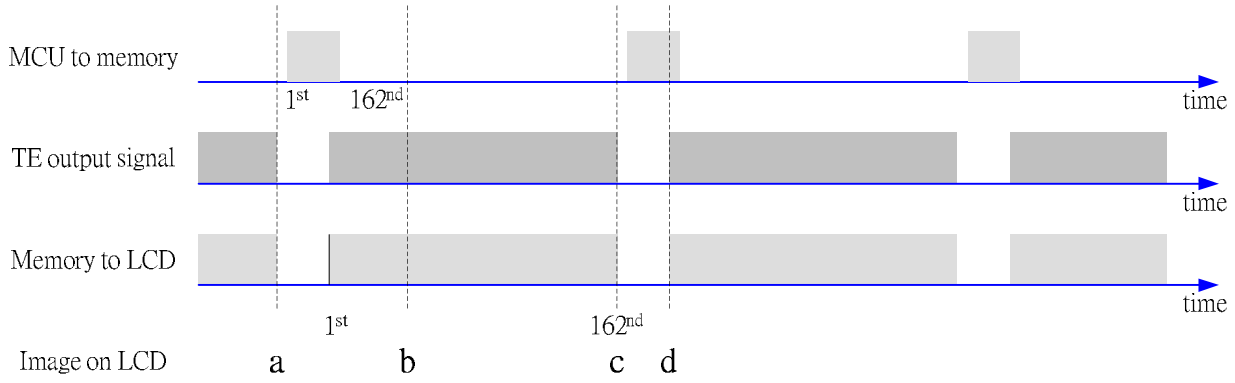
Note: The timings in Table 9.10.1 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

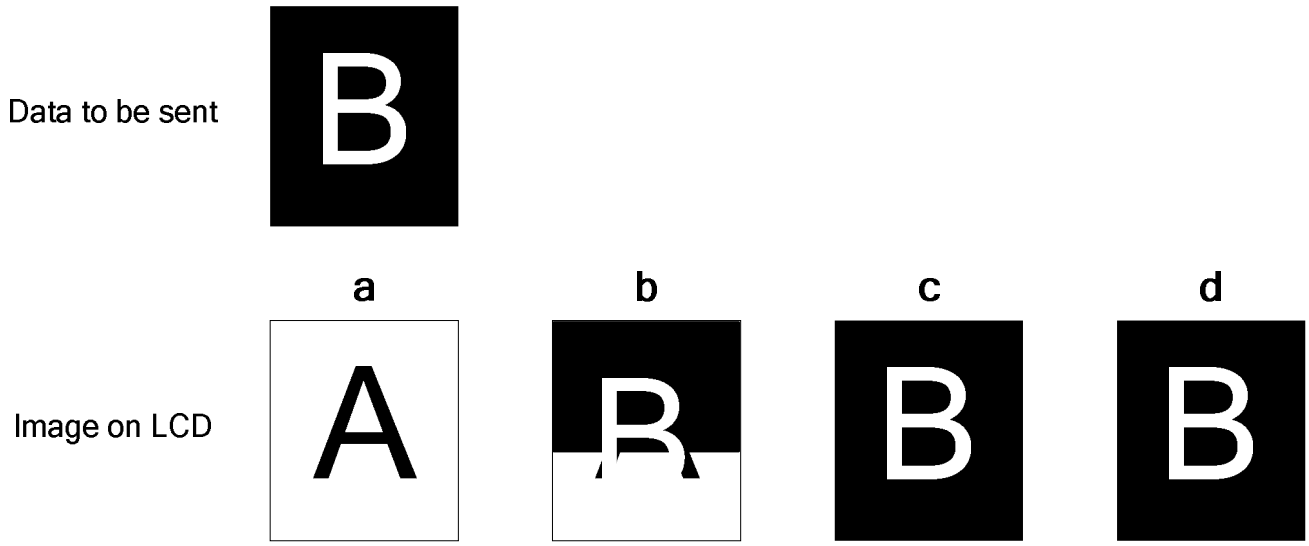


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

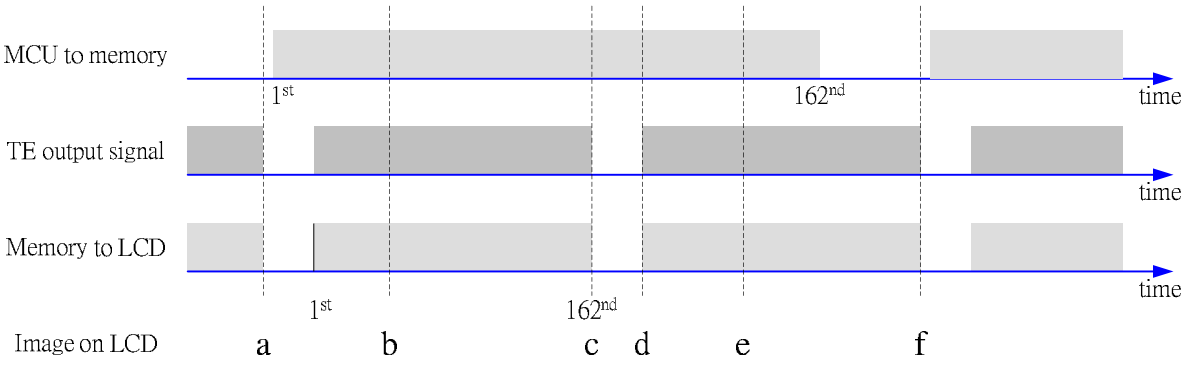
9.12.3 Example 1: MPU Write is faster than panel read



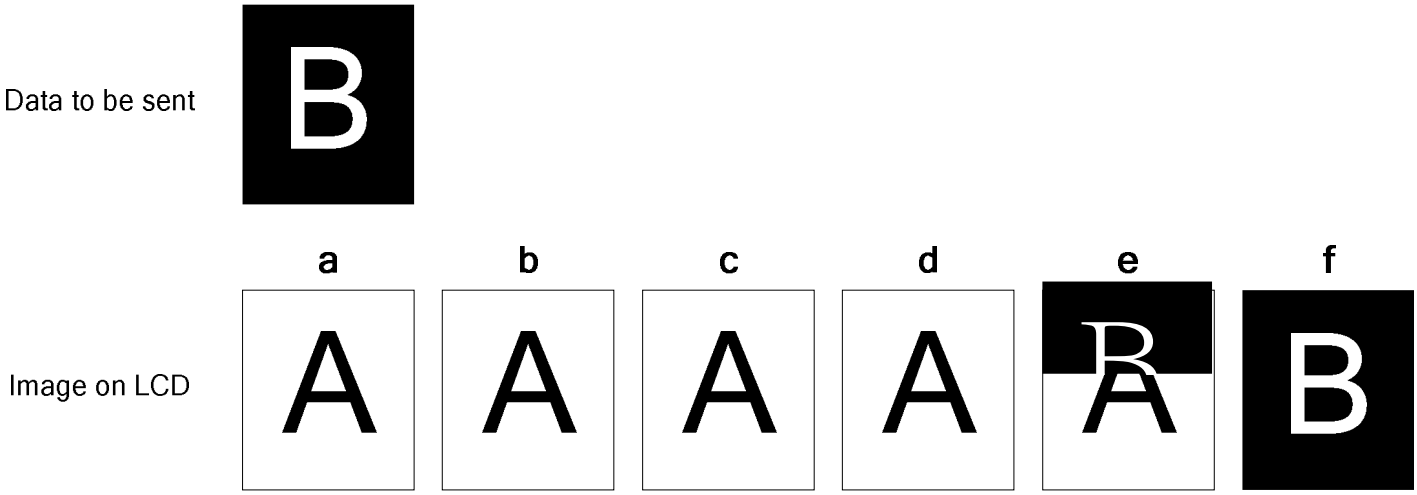
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



9.12.4 Example 2: MPU Write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



9.13 Power ON/OFF Sequence

VDDI and VDD can be applied in any order

VDD and VDDI can be powered down in any order

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

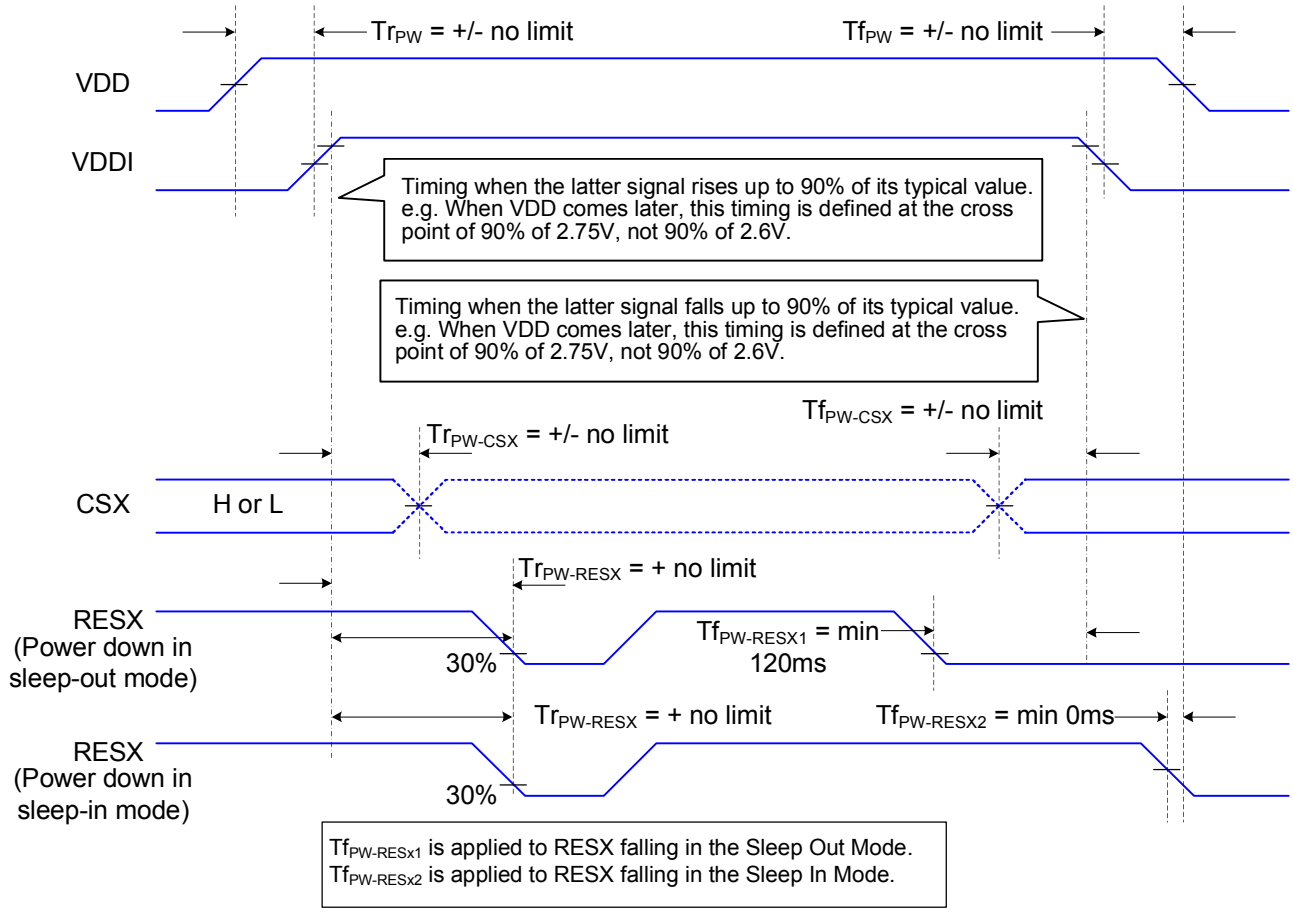
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



9.13.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

9.14 Power Level Definition

9.14.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.
In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display area is used but with 8 colors.

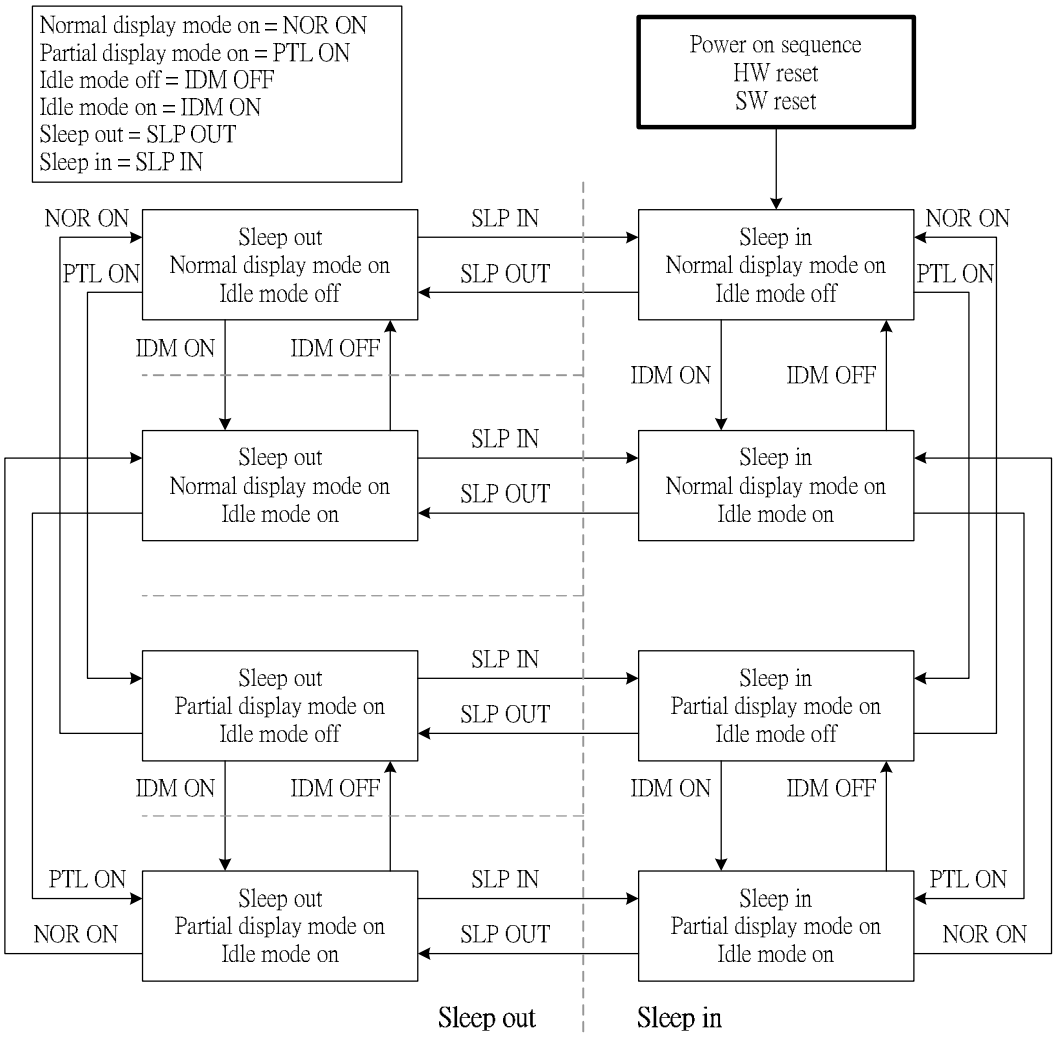
4. Partial Mode On, Idle Mode On, Sleep Out.
In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode
In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode
In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

9.14.2 Power Flow Chart



9.15 Reset Table

9.15.1 Reset Table(Default Value, GM[1:0]="11", 128RGB x 160)

Item	After Power On	After H/W Reset	After S/W Reset
Frame Memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display Mode (Normal/Partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	007Fh	007Fh	007Fh (127d) (when MV=0) 009Fh (159d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	009Fh	009Fh	009Fh (159d) (when MV=0) 007Fh (127d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	Random values	Random values	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	009Fh	009Fh	009Fh
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

9.15.2 Reset Table (GM[1:0]= “01”, 132RGB x 132)

Item	After Power On	After H/W Reset	After S/W Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display Mode (Normal/Partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0083h	0083h	0083h (131d) (when MV=0) 0083h (131d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	0083h	0083h	0083h (131d) (when MV=0) 0083h (131d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	See Section 9.17	See Section 9.17	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	0083h	0083h	0083h
Tearing: On/Off	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	0084h	0084h	0084h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

9.15.3 Reset Table (GM[1:0]= “00”, 132RGB x 162)

Item	After Power On	After H/W Reset	After S/W Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0083h	0083h	0083h (131d) (when MV=0) 00A1h (161d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00A1h	00A1h	00A1h (161d) (when MV=0) 0083h (131d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	Random values	Random values	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00A2h	00A2h	00A2h
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	0084h	0084h	0084h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

9.16 Module Input/Output Pins

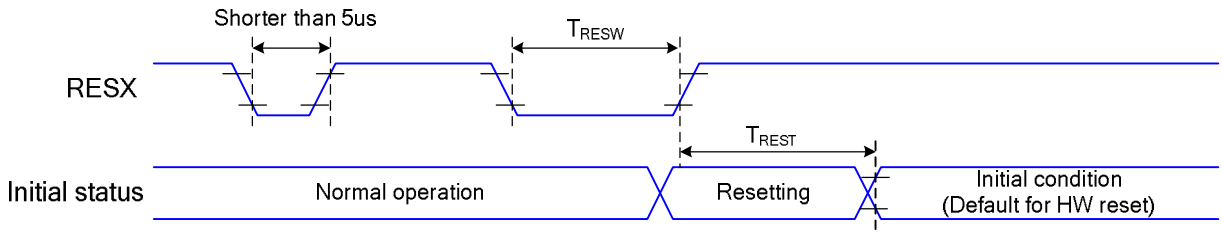
9.16.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D7 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 9.14	Input valid	Input valid	Input valid	See 9.14
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D7 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

9.17 Reset Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	tRESW	Reset Pulse Duration	10	-	us
	tREST	Reset Cancel	-	5	ms
				120	ms

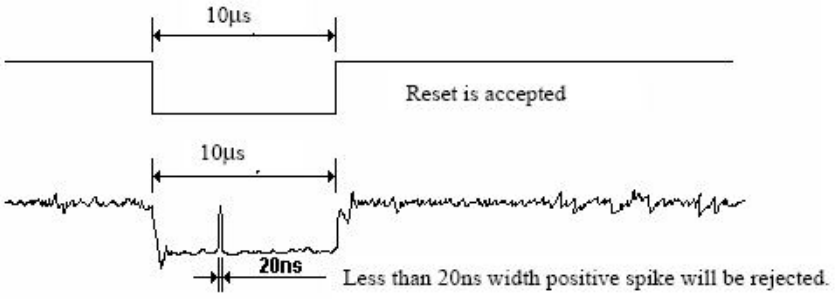
Table 14 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9.18 Color Depth Conversion Look Up Tables

9.18.1 65536 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
RED	R005 R004 R003 R002 R001 R000	1	00000
	R015 R014 R013 R012 R011 R010	2	00001
	R025 R024 R023 R022 R021 R020	3	00010
	R035 R034 R033 R032 R031 R030	4	00011
	R045 R044 R043 R042 R041 R040	5	00100
	R055 R054 R053 R052 R051 R050	6	00101
	R065 R064 R063 R062 R061 R060	7	00110
	R075 R074 R073 R072 R071 R070	8	00111
	R085 R084 R083 R082 R081 R080	9	01000
	R095 R094 R093 R092 R091 R090	10	01001
	R105 R104 R103 R102 R101 R100	11	01010
	R115 R114 R113 R112 R111 R110	12	01011
	R125 R124 R123 R122 R121 R120	13	01100
	R135 R134 R133 R132 R131 R130	14	01101
	R145 R144 R143 R142 R141 R140	15	01110
	R155 R154 R153 R152 R151 R150	16	01111
	R165 R164 R163 R162 R161 R160	17	10000
	R175 R174 R173 R172 R171 R170	18	10001
	R185 R184 R183 R182 R181 R180	19	10010
	R195 R194 R193 R192 R191 R190	20	10011
	R205 R204 R203 R202 R201 R200	21	10100
	R215 R214 R213 R212 R211 R210	22	10101
	R225 R224 R223 R222 R221 R220	23	10110
	R235 R234 R233 R232 R231 R230	24	10111
	R245 R244 R243 R242 R241 R240	25	11000
	R255 R254 R253 R252 R251 R250	26	11001
	R265 R264 R263 R262 R261 R260	27	11010
	R275 R274 R273 R272 R271 R270	28	11011
	R285 R284 R283 R282 R281 R280	29	11100
	R295 R294 R293 R292 R291 R290	30	11101
	R305 R304 R303 R302 R301 R300	31	11110
	R315 R314 R313 R312 R311 R310	32	11111

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
GREEN	G005 G004 G003 G002 G001 G000	33	000000
	G015 G014 G013 G012 G011 G010	34	000001
	G025 G024 G023 G022 G021 G020	35	000010
	G035 G034 G033 G032 G031 G030	36	000011
	G045 G044 G043 G042 G041 G040	37	000100
	G055 G054 G053 G052 G051 G050	38	000101
	G065 G064 G063 G062 G061 G060	39	000110
	G075 G074 G073 G072 G071 G070	40	000111
	G085 G084 G083 G082 G081 G080	41	001000
	G095 G094 G093 G092 G091 G090	42	001001
	G105 G104 G103 G102 G101 G100	43	001010
	G115 G114 G113 G112 G111 G110	44	001011
	G125 G124 G123 G122 G121 G120	45	001100
	G135 G134 G133 G132 G131 G130	46	001101
	G145 G144 G143 G142 G141 G140	47	001110
	G155 G154 G153 G152 G151 G150	48	001111
	G165 G164 G163 G162 G161 G160	49	010000
	G175 G174 G173 G172 G171 G170	50	010001
	G185 G184 G183 G182 G181 G180	51	010010
	G195 G194 G193 G192 G191 G190	52	010011
	G205 G204 G203 G202 G201 G200	53	010100
	G215 G214 G213 G212 G211 G210	54	010101
	G225 G224 G223 G222 G221 G220	55	010110
	G235 G234 G233 G232 G231 G230	56	010111
	G245 G244 G243 G242 G241 G240	57	011000
	G255 G254 G253 G252 G251 G250	58	011001
	G265 G264 G263 G262 G261 G260	59	011010
	G275 G 274 G273 G272 G271 G270	60	011011
	G285 G 284 G283 G282 G281 G280	61	011100
	G295 G 294 G293 G292 G291 G290	62	011101
	G305 G 304 G303 G302 G301 G300	63	011110
	G315 G 314 G313 G312 G311 G310	64	011111
	G325 G324 G323 G322 G321 G320	65	100000
	G335 G334 G333 G332 G331 G330	66	100001
	G345 G344 G343 G342 G341 G340	67	100010
	G355 G354 G353 G352 G351 G350	68	100011

	G365 G364 G363 G362 G361 G360	69	100100
	G375 G374 G373 G372 G371 G370	70	100101
	G385 G384 G383 G382 G381 G380	71	100110
	G395 G394 G393 G392 G391 G390	72	100111
	G405 G404 G403 G402 G401 G400	73	101000
	G415 G414 G413 G412 G411 G410	74	101001
	G425 G424 G423 G422 G421 G420	75	101010
	G435 G434 G433 G432 G431 G430	76	101011
	G445 G444 G443 G442 G441 G440	77	101100
	G455 G454 G453 G452 G451 G450	78	101101
	G465 G464 G463 G462 G461 G460	79	101110
	G475 G474 G473 G472 G471 G470	80	101111
	G485 G484 G483 G482 G481 G480	81	110000
	G495 G494 G493 G492 G491 G490	82	110001
	G505 G504 G503 G502 G501 G500	83	110010
	G515 G514 G513 G512 G511 G510	84	110011
	G525 G524 G523 G522 G521 G520	85	110100
	G535 G534 G533 G532 G531 G530	86	110101
	G545 G544 G543 G542 G541 G540	87	110110
	G555 G554 G553 G552 G551 G550	88	110111
	G565 G564 G563 G562 G561 G560	89	111000
	G575 G574 G573 G572 G571 G570	90	111001
	G585 G584 G583 G582 G581 G580	91	111010
	G595 G594 G593 G592 G591 G590	92	111011
	G605 G604 G603 G602 G601 G600	93	111100
	G615 G614 G613 G612 G611 G610	94	111101
	G625 G624 G623 G622 G621 G620	95	111110
	G635 G634 G633 G632 G631 G630	96	111111

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
BLUE	B005 B004 B003 B002 B001 B000	97	00000
	B015 B014 B013 B012 B011 B010	98	00001
	B025 B024 B023 B022 B021 B020	99	00010
	B035 B034 B033 B032 B031 B030	100	00011
	B045 B044 B043 B042 B041 B040	101	00100
	B055 B054 B053 B052 B051 B050	102	00101
	B065 B064 B063 B062 B061 B060	103	00110

	B075 B074 B073 B072 B071 B070	104	00111
	B085 B084 B083 B082 B081 B080	105	01000
	B095 B094 B093 B092 B091 B090	106	01001
	B105 B104 B103 B102 B101 B100	107	01010
	B115 B114 B113 B112 B111 B110	108	01011
	B125 B124 B123 B122 B121 B120	109	01100
	B135 B134 B133 B132 B131 B130	110	01101
	B145 B144 B143 B142 B141 B140	111	01110
	B155 B154 B153 B152 B151 B150	112	01111
	B165 B164 B163 B162 B161 B160	113	10000
	B175 B174 B173 B172 B171 B170	114	10001
	B185 B184 B183 B182 B181 B180	115	10010
	B195 B194 B193 B192 B191 B190	116	10011
	B205 B204 B203 B202 B201 B200	117	10100
	B215 B214 B213 B212 B211 B210	118	10101
	B225 B224 B223 B222 B221 B220	119	10110
	B235 B234 B233 B232 B231 B230	120	10111
	B245 B244 B243 B242 B241 B240	121	11000
	B255 B254 B253 B252 B251 B250	122	11001
	B265 B264 B263 B262 B261 B260	123	11010
	B275 B274 B273 B272 B271 B270	124	11011
	B285 B284 B283 B282 B281 B280	125	11100
	B295 B294 B293 B292 B291 B290	126	11101
	B305 B304 B303 B302 B301 B300	127	11110
	B315 B314 B313 B312 B311 B310	128	11111

9.18.2 4096 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 4k Color (4-bits)
RED	R005 R004 R003 R002 R001 R000	1	0000
	R015 R014 R013 R012 R011 R010	2	0001
	R025 R024 R023 R022 R021 R020	3	0010
	R035 R034 R033 R032 R031 R030	4	0011
	R045 R044 R043 R042 R041 R040	5	0100
	R055 R054 R053 R052 R051 R050	6	0101
	R065 R064 R063 R062 R061 R060	7	0110
	R075 R074 R073 R072 R071 R070	8	0111
	R085 R084 R083 R082 R081 R080	9	1000
	R095 R094 R093 R092 R091 R090	10	1001
	R105 R104 R103 R102 R101 R100	11	1010
	R115 R114 R113 R112 R111 R110	12	1011
	R125 R124 R123 R122 R121 R120	13	1100
	R135 R134 R133 R132 R131 R130	14	1101
	R145 R144 R143 R142 R141 R140	15	1110
	R155 R154 R153 R152 R151 R150	16	1111
	R165 R164 R163 R162 R161 R160	17	Not used
	|	|	
	R315 R314 R313 R312 R311 R310	32	
GREEN	G005 G004 G003 G002 G001 G000	33	0000
	G015 G014 G013 G012 G011 G010	34	0001
	G025 G024 G023 G022 G021 G020	35	0010
	G035 G034 G033 G032 G031 G030	36	0011
	G045 G044 G043 G042 G041 G040	37	0100
	G055 G054 G053 G052 G051 G050	38	0101
	G065 G064 G063 G062 G061 G060	39	0110
	G075 G074 G073 G072 G071 G070	40	0111
	G085 G084 G083 G082 G081 G080	41	1000
	G095 G094 G093 G092 G091 G090	42	1001
	G105 G104 G103 G102 G101 G100	43	1010
	G115 G114 G113 G112 G111 G110	44	1011
	G125 G124 G123 G122 G121 G120	45	1100
	G135 G134 G133 G132 G131 G130	46	1101
	G145 G144 G143 G142 G141 G140	47	1110
	G155 G154 G153 G152 G151 G150	48	1111

	G165 G164 G163 G162 G161 G160	49	Not used
	|	|	
	G635 G634 G633 G632 G631 G630	96	
BLUE	B005 B004 B003 B002 B001 B000	97	0000
	B015 B014 B013 B012 B011 B010	98	0001
	B025 B024 B023 B022 B021 B020	99	0010
	B035 B034 B033 B032 B031 B030	100	0011
	B045 B044 B043 B042 B041 B040	101	0100
	B055 B054 B053 B052 B051 B050	102	0101
	B065 B064 B063 B062 B061 B060	103	0110
	B075 B074 B073 B072 B071 B070	104	0111
	B085 B084 B083 B082 B081 B080	105	1000
	B095 B094 B093 B092 B091 B090	106	1001
	B105 B104 B103 B102 B101 B100	107	1010
	B115 B114 B113 B112 B111 B110	108	1011
	B125 B124 B123 B122 B121 B120	109	1100
	B135 B134 B133 B132 B131 B130	110	1101
	B145 B144 B143 B142 B141 B140	111	1110
	B155 B154 B153 B152 B151 B150	112	1111
	B165 B164 B163 B162 B161 B160	113	Not used
	|	|	
	B315 B314 B313 B312 B311 B310	128	

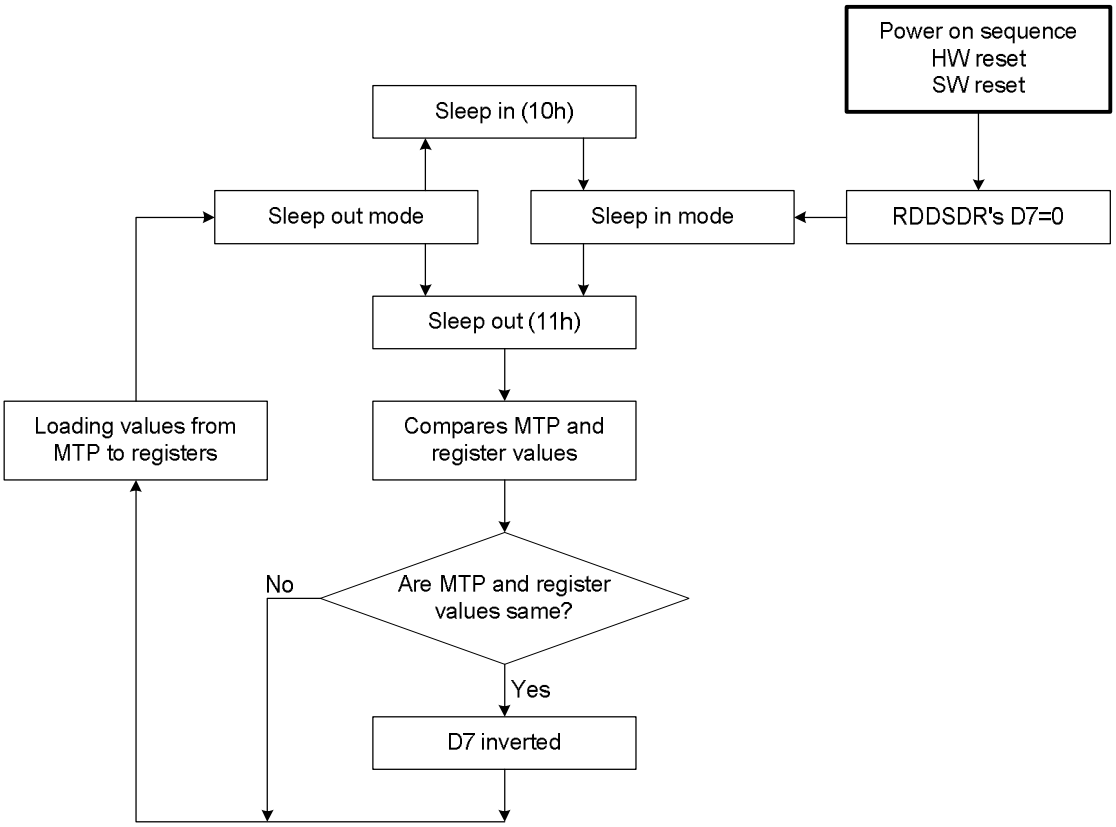
9.19 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

9.19.1 Register Loading Detection

Sleep Out-command (See section 0 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from MTP (or similar device) to registers of the display controller is working properly.

There are compared factory values of the MTP and register values of the display controller by the display controller. If those both values (MTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 0 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:

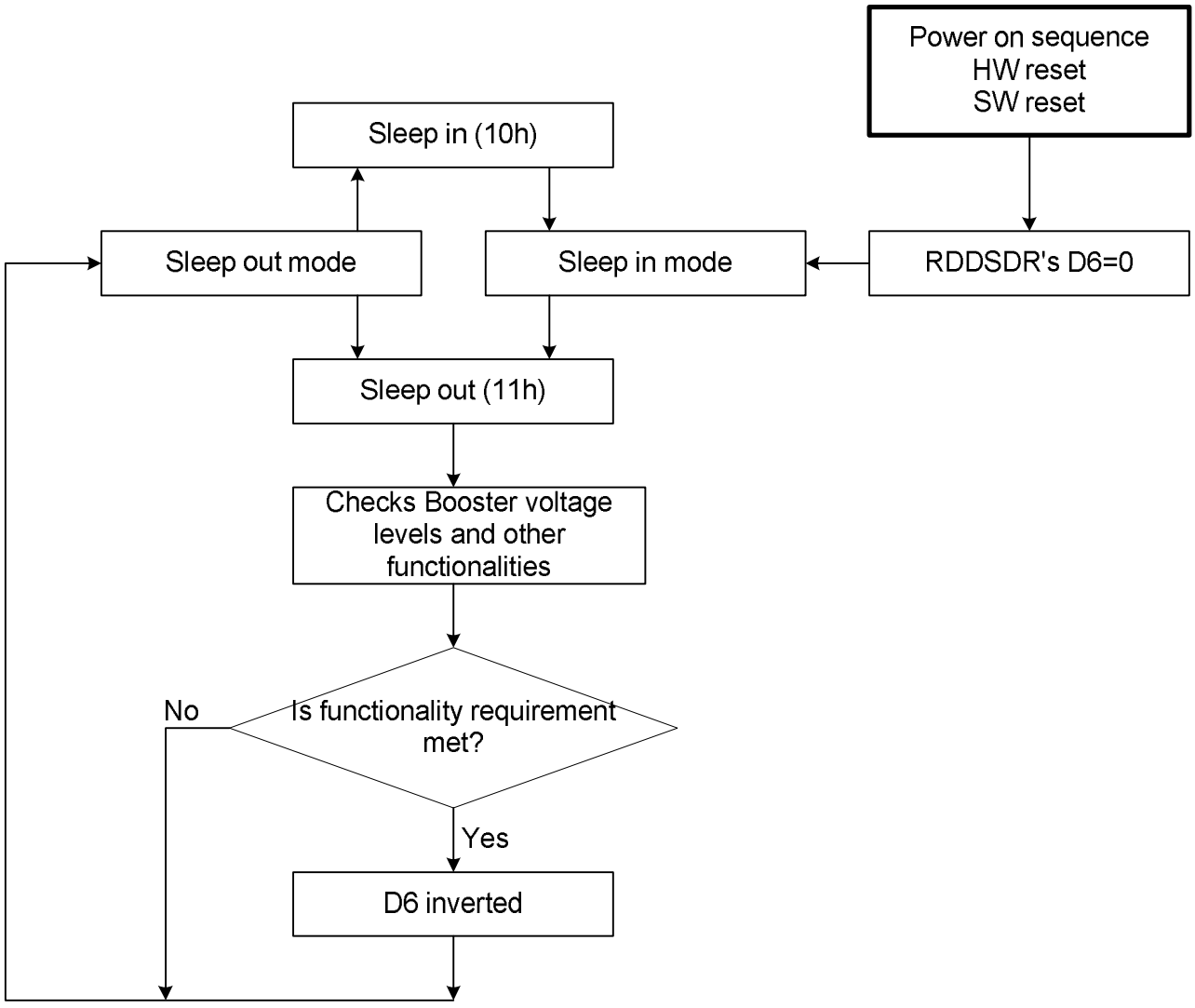


Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

9.19.2 Functionality Detection

Sleep Out-command (See section 0 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 0 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).The flow chart for this internal function is following:



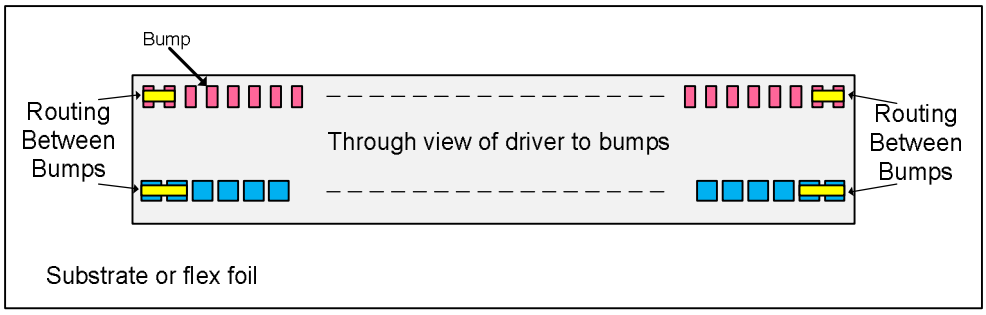
Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

9.19.3 Chip Attachment Detection (Optional)

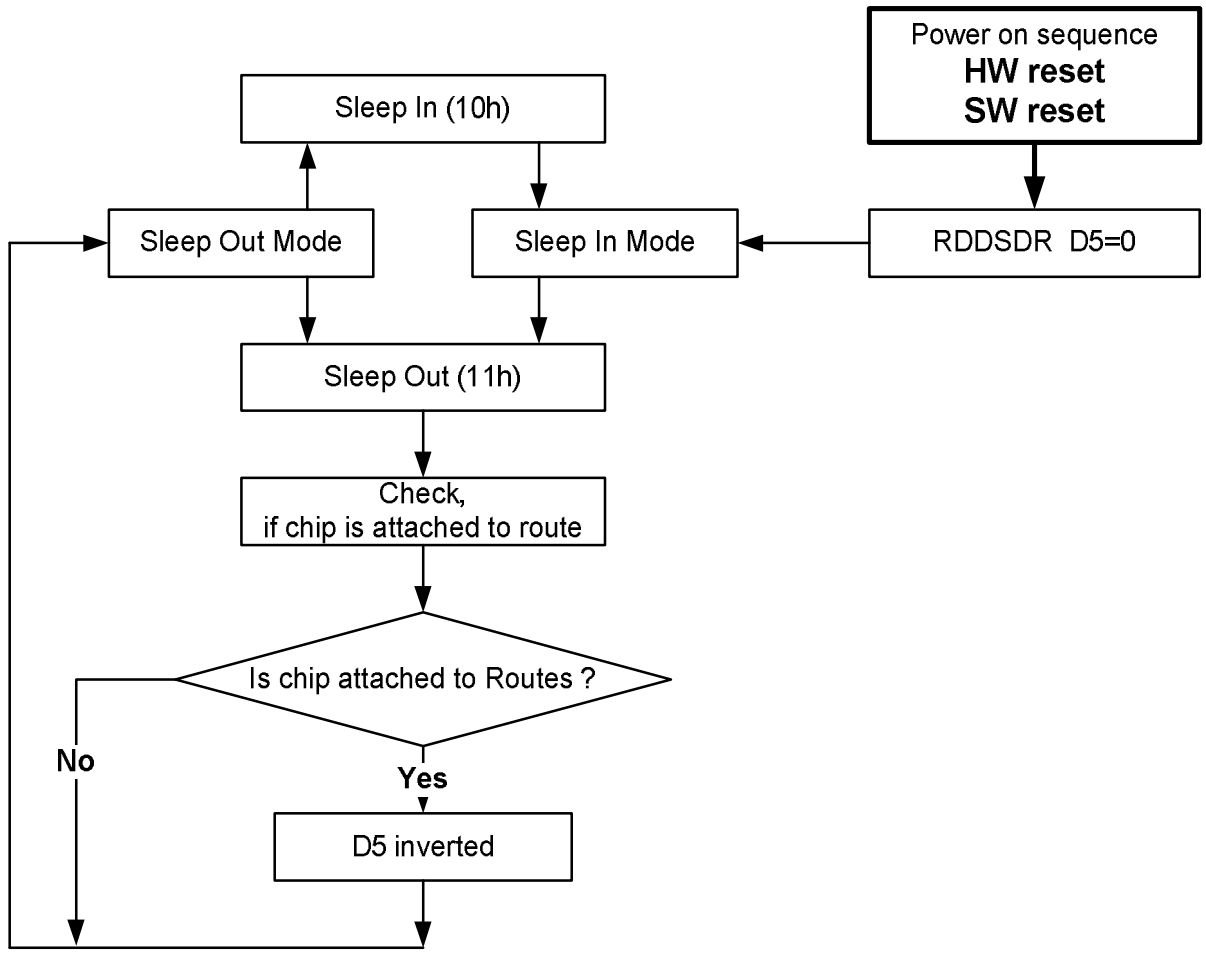
Sleep Out-command (See section 0 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit, which is defined in command 0 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= increased by 1).

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



The flow chart for this internal function is following:

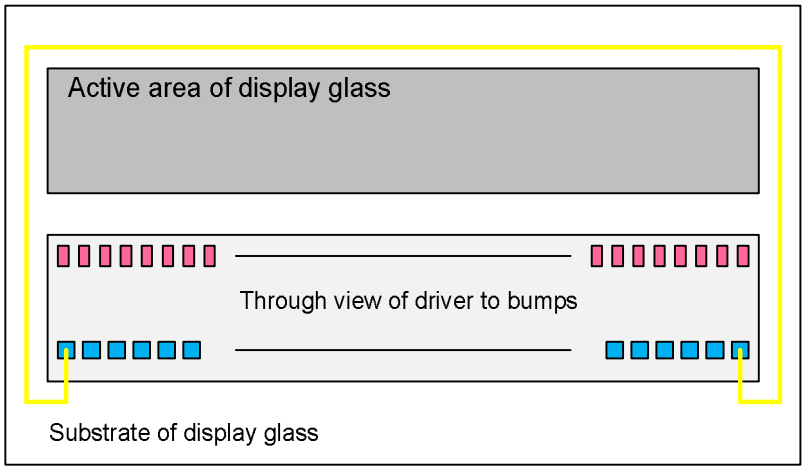


9.19.4 Display Glass Break Detection (Optional)

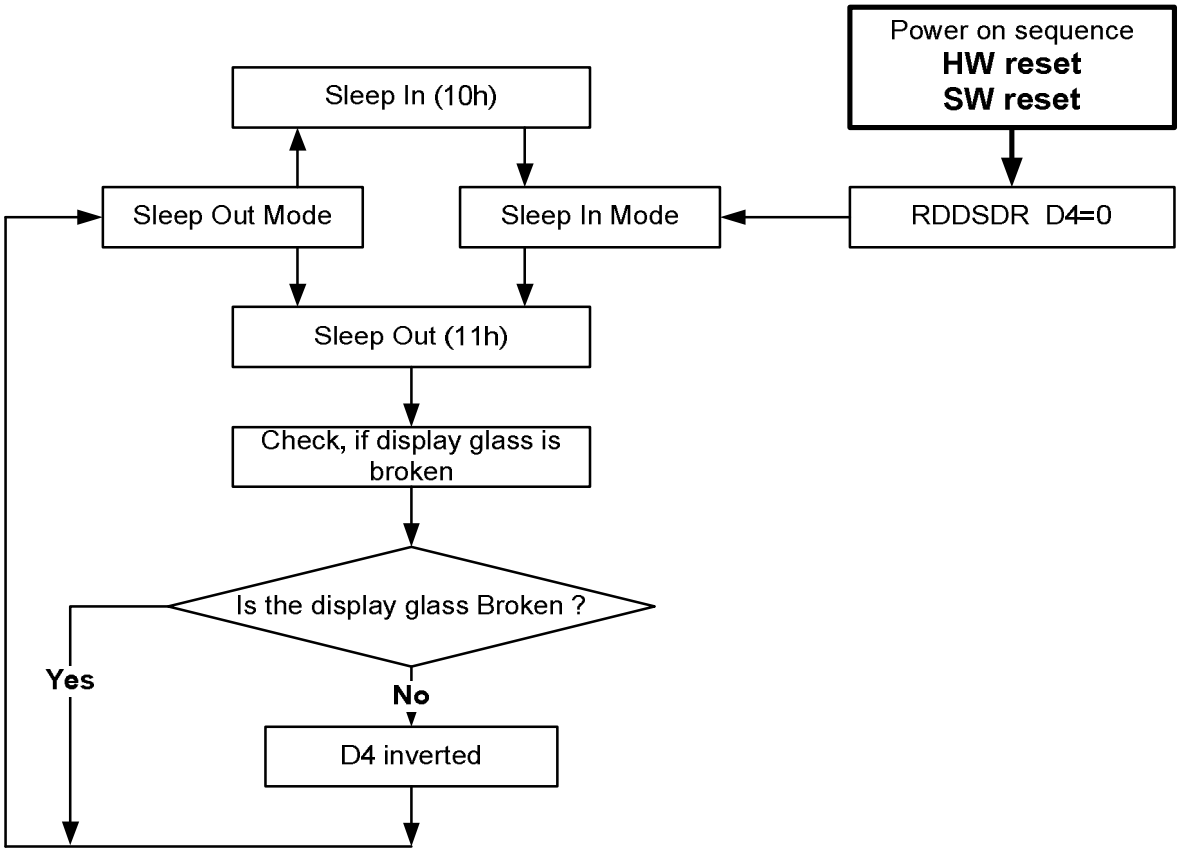
Sleep Out-command (See section 0 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display glass of the display module is broken or not.

There is inverted (= increased by 1) a bit, which is defined in command 0 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D4), if the display glass is not broken. If this display glass is broken, this bit (D4) is not inverted (= increased by 1).

The following figure is a reference, how this glass break detection can be implemented e.g. there is connected together 2 bumps via route of ITO. This route of ITO is the nearest route of the edge of the display glass.



The flow chart for this internal function is following:



10 COMMAND

10.1 System Function Command List and Description

Table 15 System Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	0	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software Reset
RDDID	0	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 Read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 Read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 Read
RDDST	0	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
		1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
		1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	-	-		-
RDD MADCTL	0	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTL
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	MY	MX	MV	ML	RGB	MH	-	-		-
RDD COLMOD	0	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0		-
RDDIM	0	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	VSSON	D6	INVON	-	-	GCS2	GCS1	GCS0		-
RDDSM	0	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	TEON	TEM	-	-	-	-	-	-		-
RDDSDR	0	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Display Self-diagnostic result
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	RELD	FUND	ATTD	BRD	-	-	-	-		-

"-": Don't care

Table 16 System Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
SLPIN	0	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep In & Booster Off
SLPOUT	0	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep Out & Booster On
PTLON	0	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial Mode On
NORON	0	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial Off (Normal)
INVOFF	0	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display Inversion Off (Normal)
INVON	0	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display Inversion On
GAMSET	0	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma Curve Select
		1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0		-
DISPOFF	0	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display Off
DISPON	0	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display On
CASET	0	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column Address Set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X Address Start: 0≦XS≦X
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X Address End: S≦ XE≦ X
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	0	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row Address Set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y Address Start: 0≦YS≦Y
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y Address End:S≦YE≦Y
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory Write
		1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		Write Data
RGBSET	0	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)	LUT for 4k,65k,262k Color display
		1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000		Red Tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0		Red Tone “a”
		1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000		Green Tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0		Green Tone “b”
		1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000		Blue Tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0		Blue Tone “c”
RAMRD	0	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory Read
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		Read Data

“-“: Don’t care

Table 17 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PTLAR	10.1.25	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial Start/End Address Set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial Start Address (0,1,2, ..P)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial End Address (0,1,2, .., P)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
SCRLAR	10.1.26	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set
		1	↑	1	-	-	-	-	-	-	-	-	-		Top fixed area (0,1, 2, .., 161)
		1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
		1	↑	1	-	-	-	-	-	-	-	-	-		Vertical scroll area (0,1, 2, .., 161)
		1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
		1	↑	1	-	-	-	-	-	-	-	-	-		Bottom fixed area (0,1, 2, .., 161)
		1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	10.1.27	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	10.1.28	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing Effect Mode Set & on
		1	↑	1	-	-	-	-	-	-	-	-	TEM		Mode1: TEM="0" Mode2: TEM="1"
MADCTL	10.1.29	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory Data Access Control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-		-
VSCSAD	10.1.30	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll Start Address of RAM
		1	1	1	-	-	-	-	-	-	-	-			SSA=0,1,2,…,161
		1	1	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0		
IDMOFF	10.1.31	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle Mode Off
IDMON	10.1.32	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle Mode On
COLMOD	10.1.33	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface Pixel Format
		1	↑	1	-	-	-	-	-	-	IFPF2	IFPF1	IFPF0		Interface Format
RDID1	10.1.34	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read Parameter
RDID2	10.1.35	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read Parameter
RDID3	10.1.36	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read Parameter

"-": Don't care

Note 1: After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2: Undefined commands are treated as NOP (00 h) command.

Note 3: B0 to D9 and DA to F are for factory use of driver supplier.

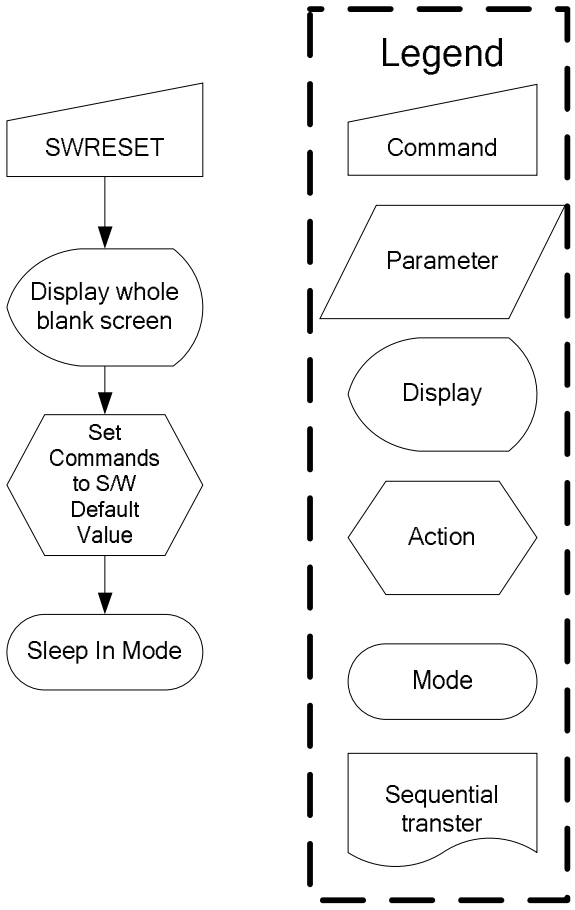
Note 4: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh).

10.1.1 NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-
Description	This command is empty command.												

"-" Don't care

10.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-
Description	"-" Don't care -If Software Reset is applied during Sleep In mode, it will be necessary to wait 120msec before sending next command. -The display module loads all default values to the registers during 120msec. -If Software Reset is applied during Sleep Out or Display On Mode, it will be necessary to wait 120msec before sending next command.												
Flow Chart													

10.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
3rd Parameter	1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
4th Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

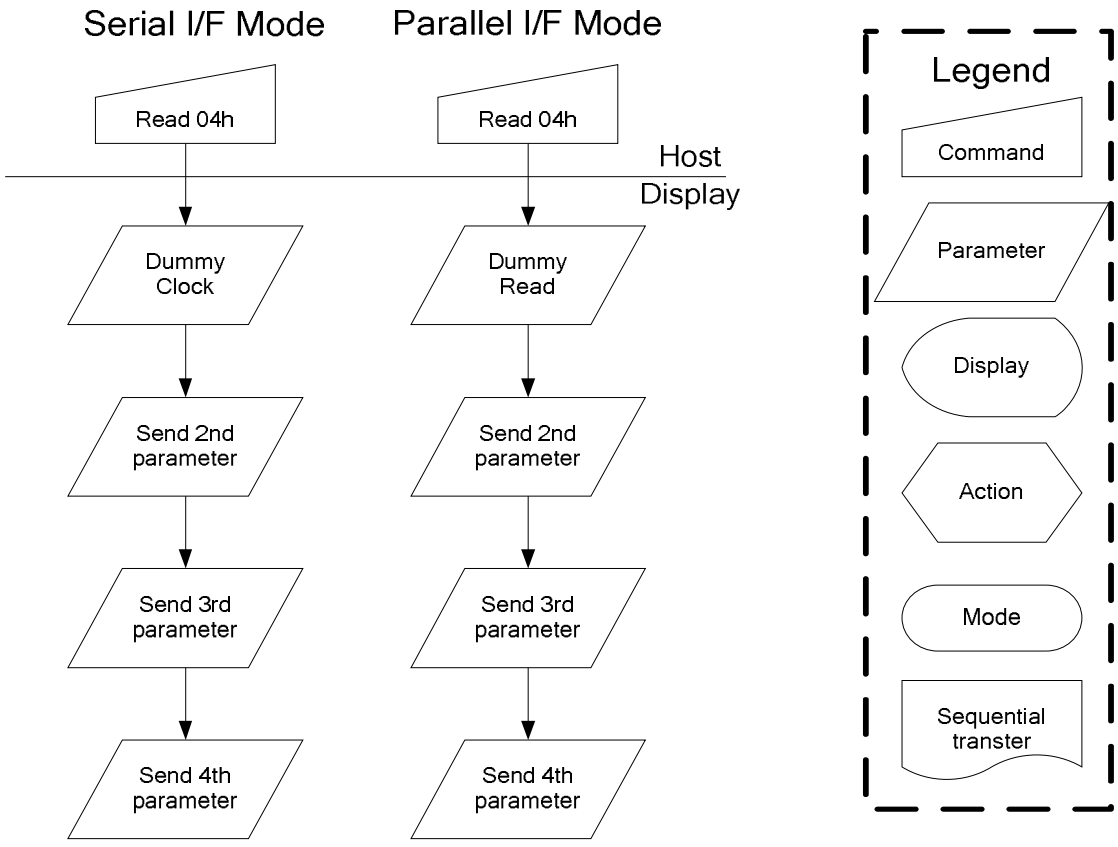
Description

-This read byte returns 24-bit display identification information.
-The 1st parameter is dummy data
-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.
-The 3rd parameter (ID26 to ID20): LCD module/driver version ID
-The 4th parameter (ID37 to UD30): LCD module/driver ID.
-Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.
"-" Don't care

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	0x7C	NV Value	NV Value
S/W Reset	0x7C	NV Value	NV Value
H/W Reset	0x7C	NV Value	NV Value

Flow Chart



10.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	
3rd Parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4th Parameter	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5th Parameter	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='1')
MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0'
ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
MH	Horizontal Order	'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')
ST24	For Future Use	'0'
ST23	For Future Use	'0'
IFPF2 IFPF1 IFPF0	Interface Color Pixel Format Definition	"011" = 12-bit / pixel, "101" = 16-bit / pixel, "110" = 18-bit / pixel, others are no define
IDMON	Idle Mode On/Off	'1' = On, "0" = Off
PTLON	Partial Mode	'1' = On, "0" = Off
SLPOUT	Sleep In/Out	'1' = Out, "0" = In
NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
ST15	Vertical Scrolling	'1' = Scroll on,"0" = Scroll off
ST14	Horizontal Scroll	'0'
INVON	Inversion Status	'1' = On, "0" = Off
ST12	All Pixels On (Not	'0'
ST11	All Pixels Off (Not	'0'
DISON	Display On/Off	'1' = On, "0" = Off
TEON	Tearing effect line	'1' = On, "0" = Off
GCSEL2 GCSEL1 GCSEL0	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3

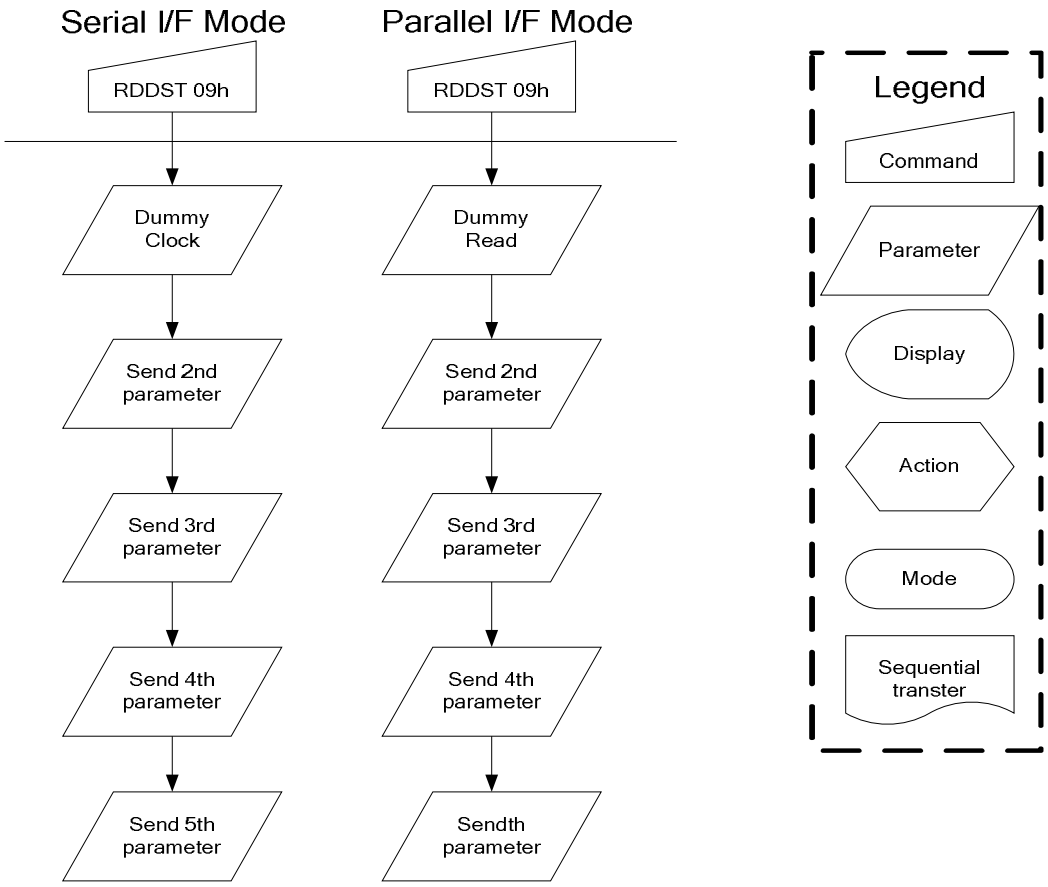
TEM	Tearing effect line	‘0’ = mode1, ‘1’ = mode2
ST4	For Future Use	‘0’
ST3	For Future Use	‘0’
ST2	For Future Use	‘0’
ST1	For Future Use	‘0’
ST0	For Future Use	‘0’

“-“ Don’t care

Default

Status	Default Value (ST31 to ST0)			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx0xx00	0xxx-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

Flow Chart



10.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑		BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	

Description

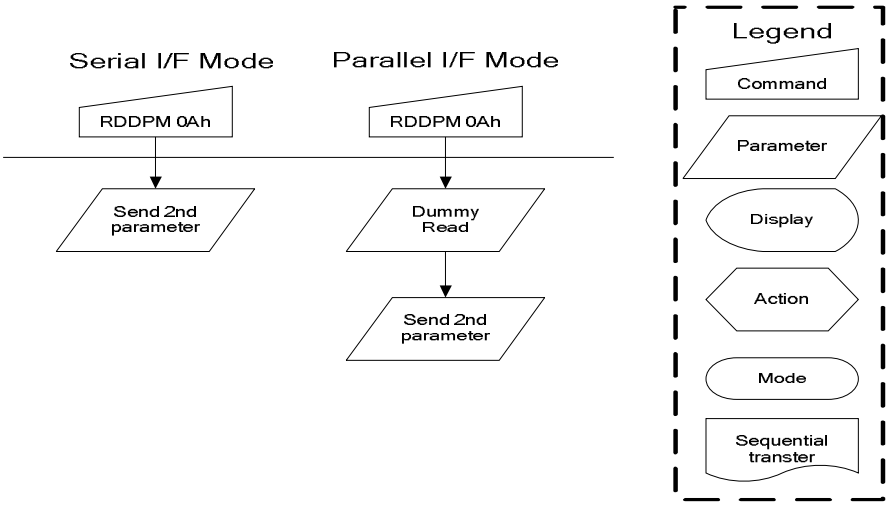
This command indicates the current status of the display as described in the table below:
"-" Don't care

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off
SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In
NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
DISON	Display On/Off	'1' = Display On, '0' = Display Off
D1	Not Used	'0'
D0	Not Used	'0'

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_1000(08h)
S/W Reset	0000_1000(08h)
H/W Reset	0000_1000(08h)

Flow Chart



10.1.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑		MY	MX	MV	ML	RGB	MH	D1	D0	

Description

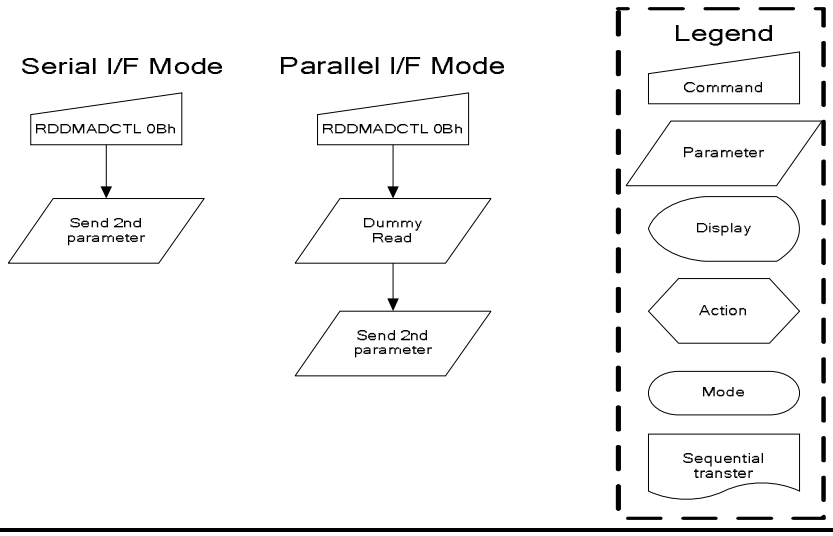
This command indicates the current status of the display as described in the table below:
"-" Don't care

Bit	Description	Value
MX	Column Address Order	'1' = Right to Left (When MADCTL B6='1') '0' = Left to Right (When MADCTL B6='0')
MY	Row Address Order	'1' = Bottom to Top (When MADCTL B7='1') '0' = Top to Bottom (When MADCTL B7='0')
MV	Row/Column Order (MV)	'1' = Row/column exchange (MV=1) '0' = Normal (MV=0)
ML	Vertical Refresh Order	'1' =LCD Refresh Bottom to Top '0' =LCD Refresh Top to Bottom
RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
MH	Horizontal Refresh Order	LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left
D1	Not Used	'0'
D0	Not Used	'0'

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change
H/W Reset	0000_0000 (00h)

Flow Chart



10.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0	

Description

This command indicates the current status of the display as described in the table below:

IFPF[2:0]	MCU Interface Color Format
011	12-bit/pixel
101	16-bit/pixel
110	18-bit/pixel
111	No used

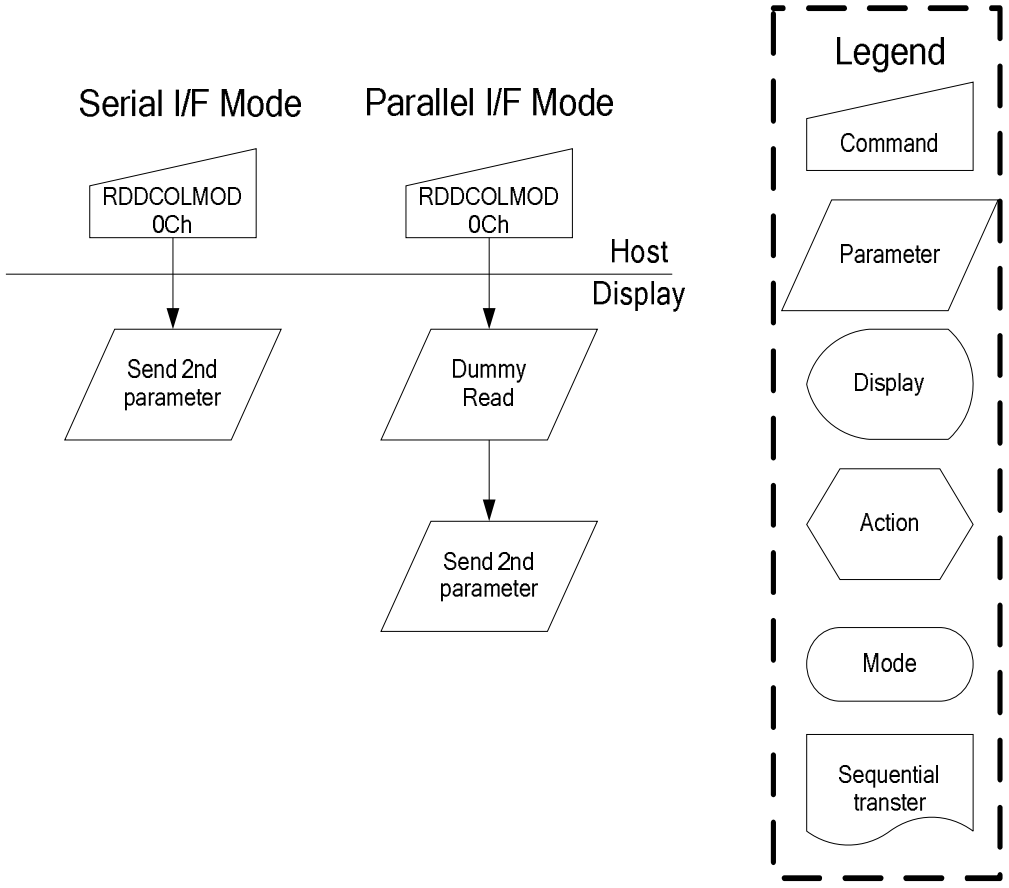
Others are no define and invalid

"-" Don't care

Default

Status	Default Value
	IFPF[2:0]
Power On Sequence	0110 (18 bits/pixel)
S/W Reset	No Change
H/W Reset	0110 (18 bits/pixel)

Flow Chart



10.1.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (0Dh): Read Display Image Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	

Description

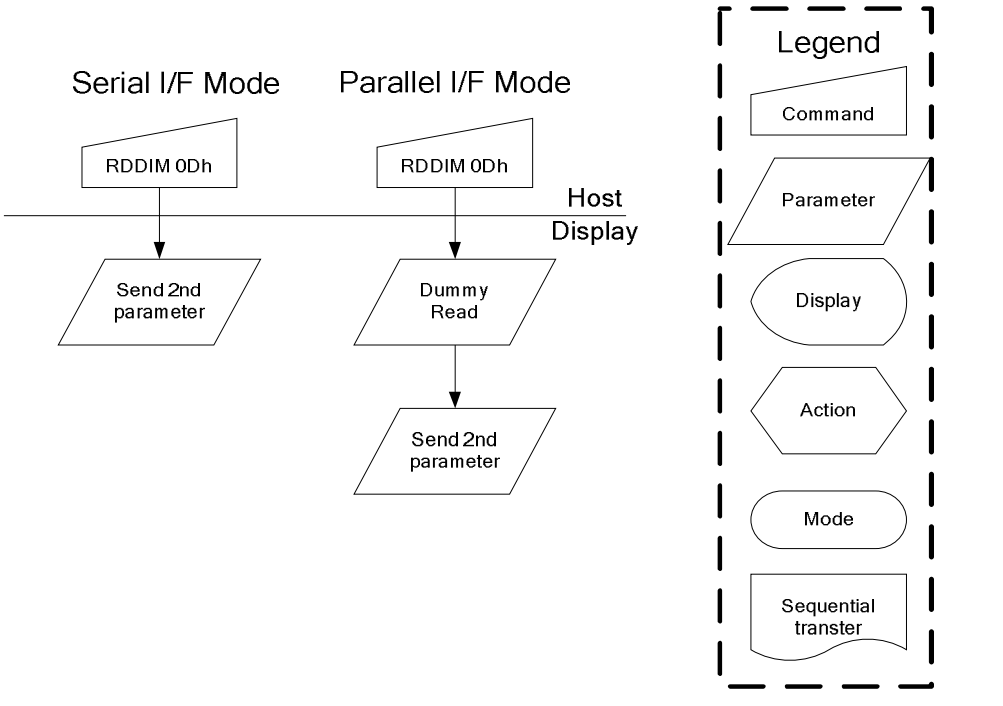
This command indicates the current status of the display as described in the table below:
"-" Don't care

Bit	Description	Value
VSSON	Reversed	"0"
D6	Reversed	"0"
INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	All Pixels On	"0" (Not used)
D3	All Pixels Off	"0" (Not used)
GCS2 GCS1 GCS0	Gamma Curve Selection	"000" = GC0, "001" = GC1, "010" = GC2, "011" = GC3, "100" to "111" = Not defined

Default

Status	Default Value(D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



10.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (0Eh): Read Display Signal Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	TEON	TEM	D5	D4	D3	D2	D1	D0	

Description

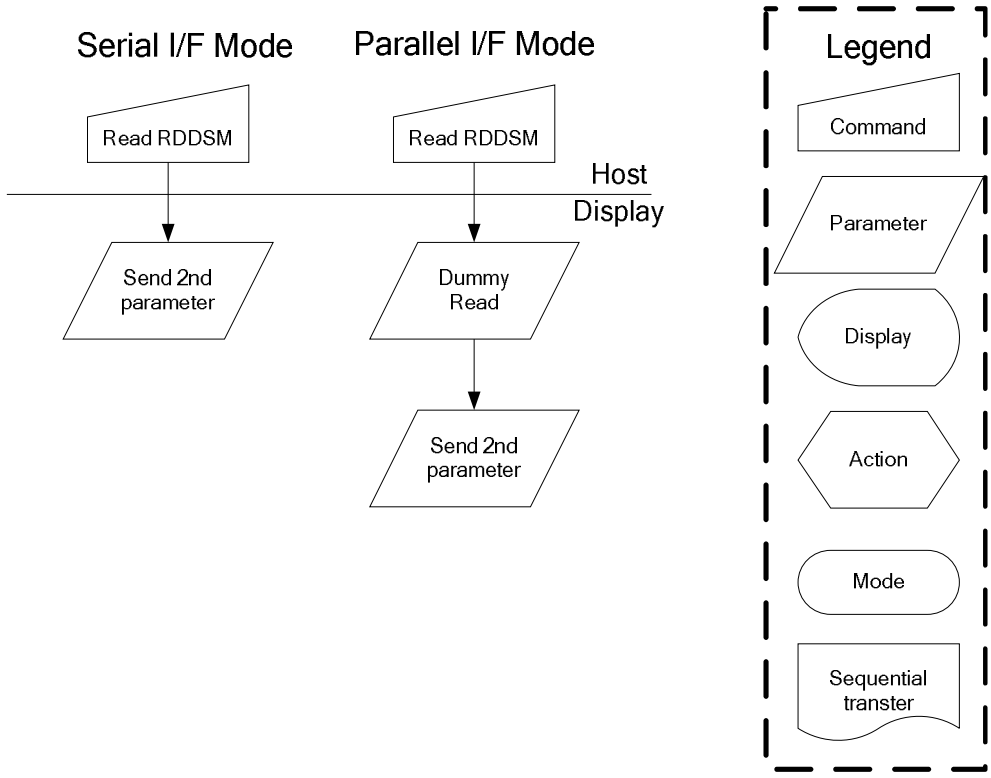
This command indicates the current status of the display as described in the table below:
"-" Don't care

Bit	Description	Value
TEON	Tearing Effect Line On/Off	"1" = On, "0" = Off
TEM	Tearing effect line mode	"1" = Mode2, "0" = Mode1
D5	Not Used	"1" = On, "0" = Off
D4	Not Used	"1" = On, "0" = Off
D3	Not Used	"1" = On, "0" = Off
D2	Not Used	"1" = On, "0" = Off
D1	Not Used	"1" = On, "0" = Off
D0	Not Used	"1" = On, "0" = Off

Default

Status	Default Value(D7~D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read RDDSM
Read RDDSM
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

10.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (0Fh): Read Display Self-Diagnostic Result												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0	

Description

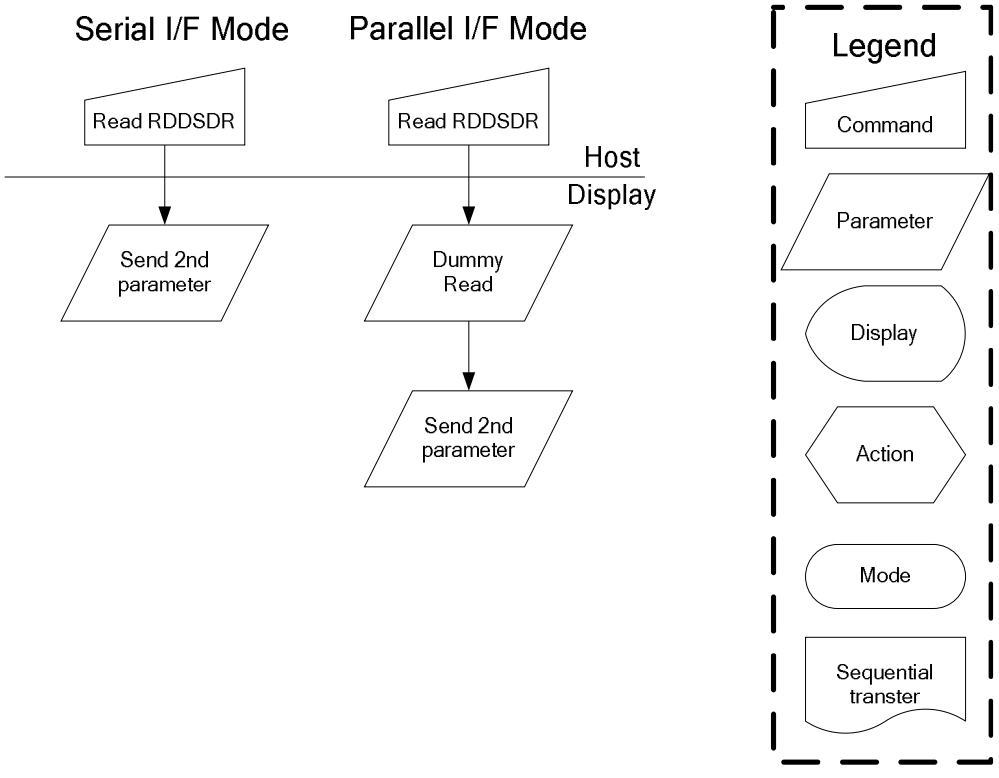
This command indicates the current status of the display as described in the table below:
"-" Don't care

Bit	Description	Value
RELD	Register Loading Detection	See Section 9.19.1
FUND	Functionality Detection	See Section 9.19.2
ATTD	Chip Attachment Detection	See Section 9.19.3
BRD	Display Glass Break Detection	See Section 9.19.4
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Default

Status	Default Value(D7~D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart

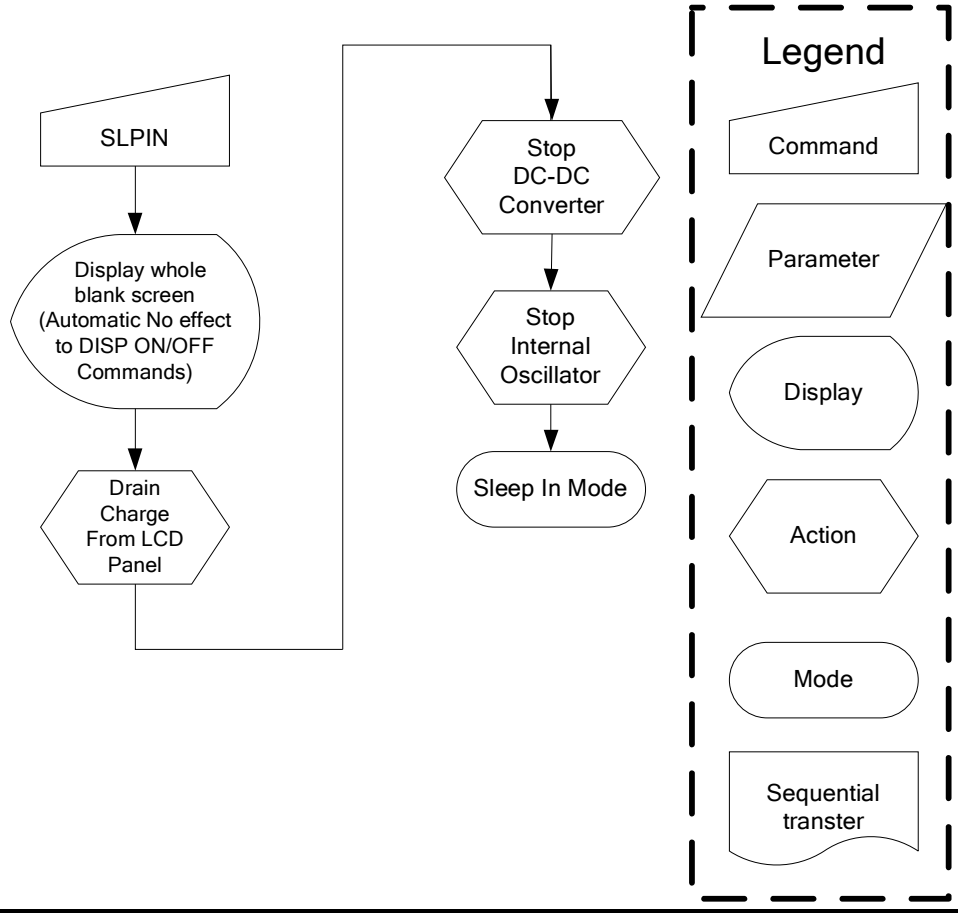


10.1.11 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
Parameter	No Parameter												-
Description	-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.												
Restriction	-This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). -When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits.												
Default													

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep in Mode

Flow Chart

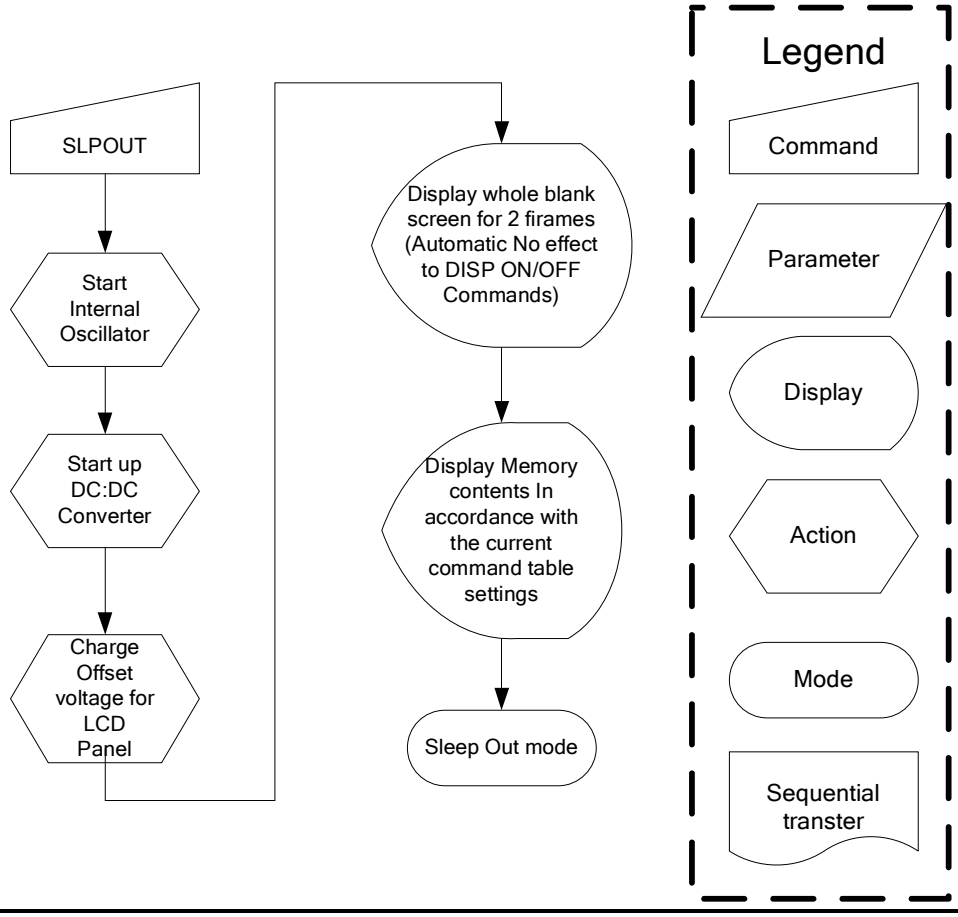


10.1.12 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
Parameter	No Parameter												-
Description	-This command turns off sleep mode. -In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.												
Restriction	-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h). -When IC is in Sleep In mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits. -When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command due to the download of default value of registers and the execution of self-diagnostic function.												
Default													

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep in Mode

Flow Chart



10.1.13 PTLON (12h): Partial Display Mode On

12H	PTLON (12h): Partial Display Mode On												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
Parameter	No Parameter												-
Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h) -To leave Partial mode, the Normal Display Mode On command (13h) should be written. "-" Don't care												
Default	Status: Power On Sequence — Default Value: Normal Mode On Status: S/W Reset — Default Value: Normal Mode On Status: H/W Reset — Default Value: Normal Mode On												
Flow Chart	See Partial Area (30h)												

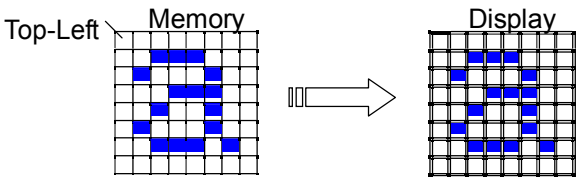
10.1.14 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
Parameter	No Parameter												-
Description	-This command returns the display to normal mode. -Normal display mode on means Partial mode off. -Exit from NORON by the Partial mode On command (12h) "-" Don't care												
Default													

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

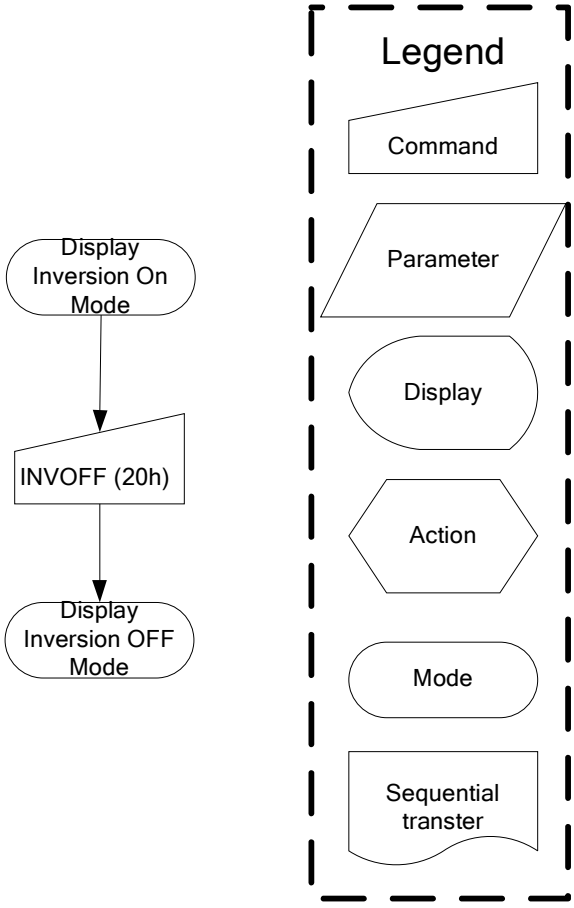
Flow Chart	See Partial Area Definition Descriptions for details of when to use this command

10.1.15 INVOFF (20h): Display Inversion Off

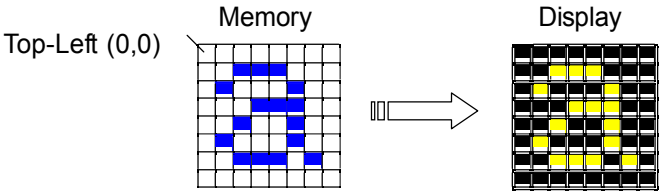
20H	IVNOFF (Normal Display Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
Parameter	No Parameter												-
Description	-This command is used to recover from display inversion mode. "-" Don't care (Example) 												

Default	Status	Default Value
	Power On Sequence	Display Inversion off
	S/W Reset	Display Inversion off
	H/W Reset	Display Inversion off

Flow Chart

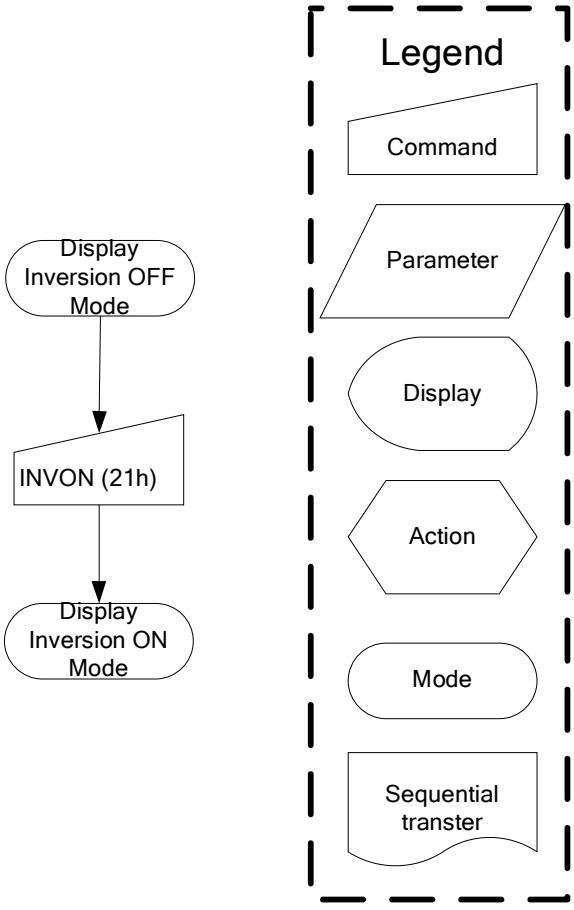


10.1.16 INVON (21h): Display Inversion On

21H	IVNOFF (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
Parameter	No Parameter												-
Description	-This command is used to enter into display inversion mode -To exit from Display Inversion On, the Display Inversion Off command (20h) should be written. "-" Don't care (Example) Top-Left (0,0) Memory → Display 												

Default	Status	Default Value
	Power On Sequence	Display Inversion off
	S/W Reset	Display Inversion off
	H/W Reset	Display Inversion off

Flow Chart



10.1.17 GAMSET (26h): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)
Parameter	1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0	

Description

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

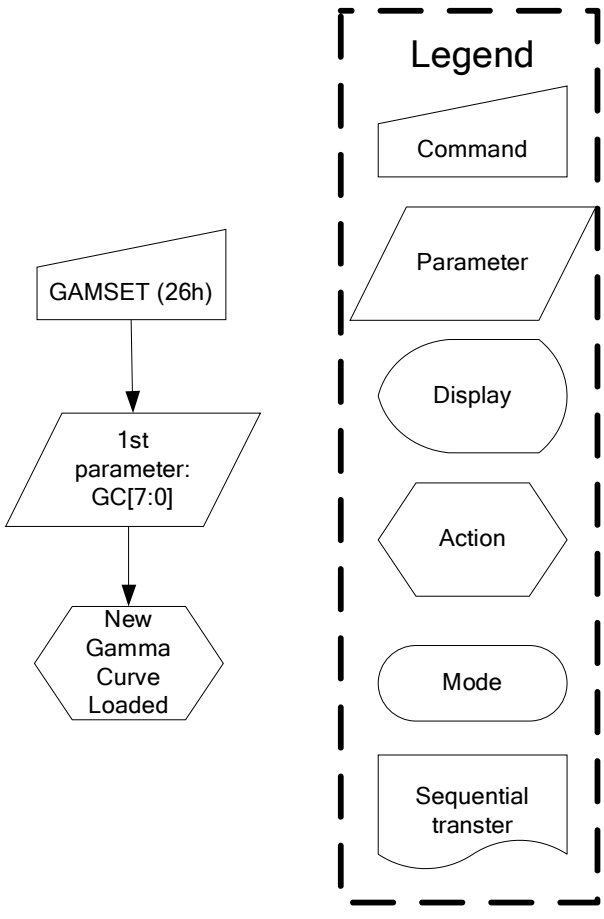
GC [7:0]	Parameter	Curve Selected	
		GS=1	GS=0
01h	GC0	Gamma Curve 1 (G2.2)	Gamma Curve 1 (G1.0)
02h	GC1	Gamma Curve 2 (G1.8)	Gamma Curve 2 (G2.5)
04h	GC2	Gamma Curve 3 (G2.5)	Gamma Curve 3 (G2.2)
08h	GC3	Gamma Curve 4 (G1.0)	Gamma Curve 4 (G1.8)

Note: All other values are undefined.

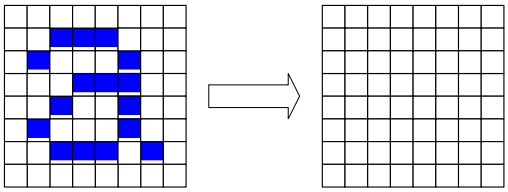
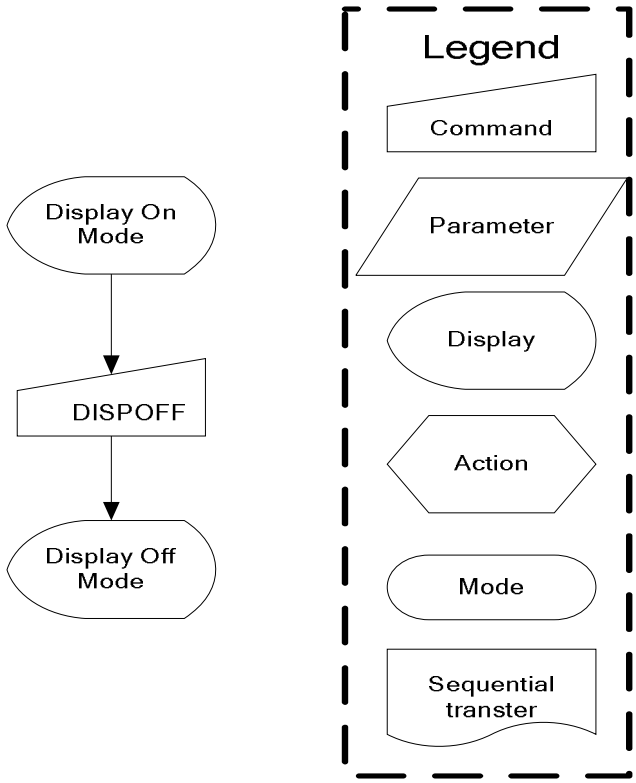
Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

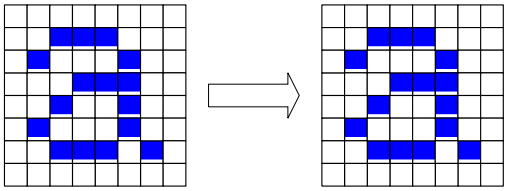
Flow Chart



10.1.18 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
Parameter	No Parameter												-
Description	- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29h) **(Example)** **Memory** **Display** 												
Default	Status: Power On Sequence / S/W Reset / H/W Reset Default Value: Display off / Display off / Display off												
Flow Chart													

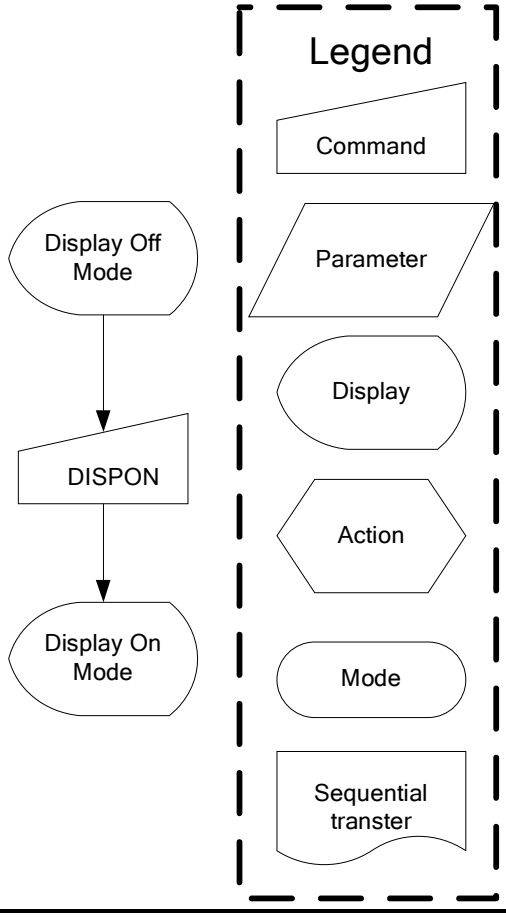
10.1.19 DISPON (29h): Display On

29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
Parameter	No Parameter												-
Description	- This command is used to recover from DISPLAY OFF mode. - Output from the Frame Memory is enabled. - This command makes no change of contents of frame memory. - This command does not change any other status. (Example) Memory → Display 												

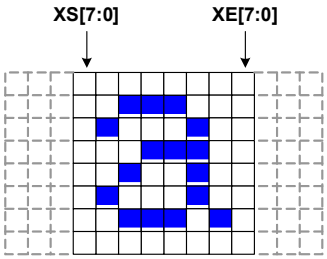
Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



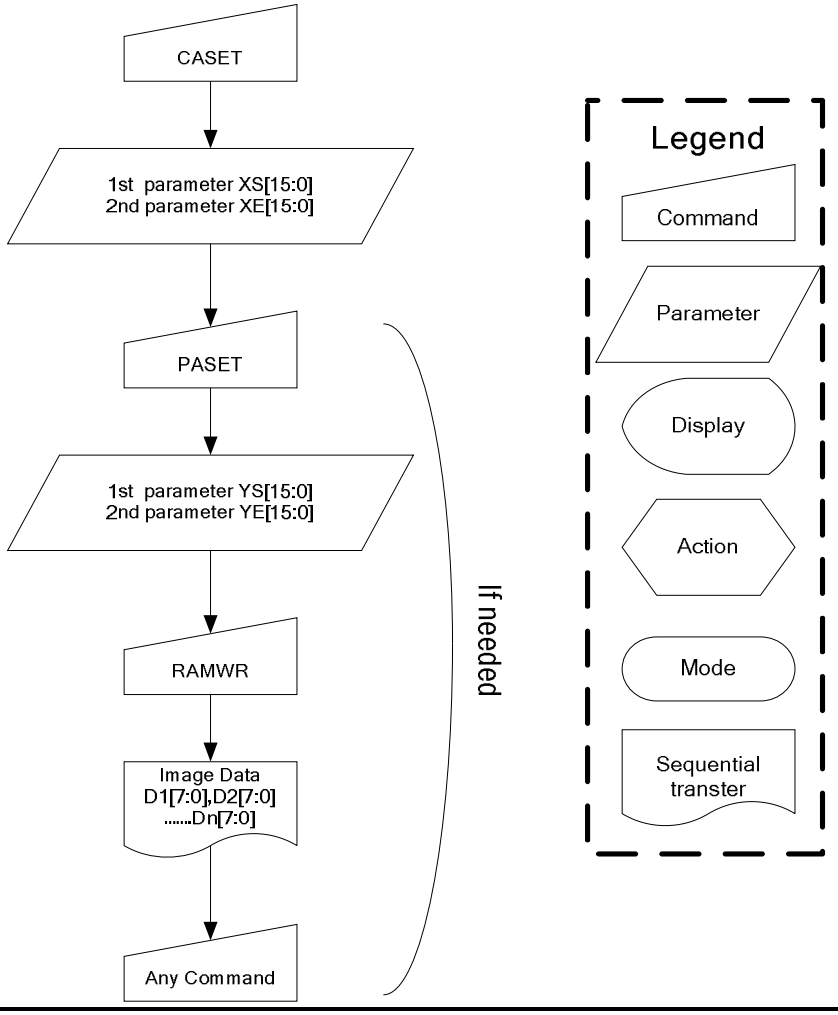
10.1.20 CASET (2Ah): Column Address Set

2AH	CASET(Column Address Set)_												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET(2Ah)	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st Parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
2nd Parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3rd Parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4th Parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
Description	-The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes. -Each value represents one column line in the Frame Memory.  												
Restriction	XS [15:0] always must be equal to or less than XE [15:0] When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored. 1. 128X160 memory base (GM = ’11’) (Parameter range: 0 < XS [15:0] < XE [15:0] < 127 (007Fh)): MV=”0”) (Parameter range: 0 < XS [15:0] < XE [15:0] < 159 (009Fh)): MV=”1”) 2. 132X132 memory base (GM = ’01’) (Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV=”0”) (Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV=”1”) 3. 132X162 memory base (GM = ’00’) (Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV=”0”) (Parameter range: 0 < XS [15:0] < XE [15:0] < 161 (00A1h)): MV=”1”)												

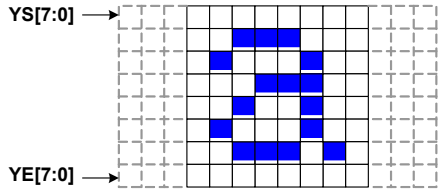
Default

GM Status	Status	Default Value		
		XS [7:0]	XE [7:0] (MV='0 ')	XE [7:0] (MV='1')
GM='11' (128x160 Memory Base)	Power On Sequence	0000h	007Fh (127)	
	S/W Reset	0000h	007Fh (127)	009Fh (159)
	H/W Reset	0000h	007Fh (127)	
GM='01' (132x132 Memory Base)	Power On Sequence	0000h	0083h (131)	
	S/W Reset	0000h	0083h (131)	0083h (131)
	H/W Reset	0000h	0083h (131)	
GM='00' (132x162 Memory Base)	Power On Sequence	0000h	0083h (131)	
	S/W Reset	0000h	0083h (131)	00A1h (161)
	H/W Reset	0000h	0083h (131)	

Flow Chart



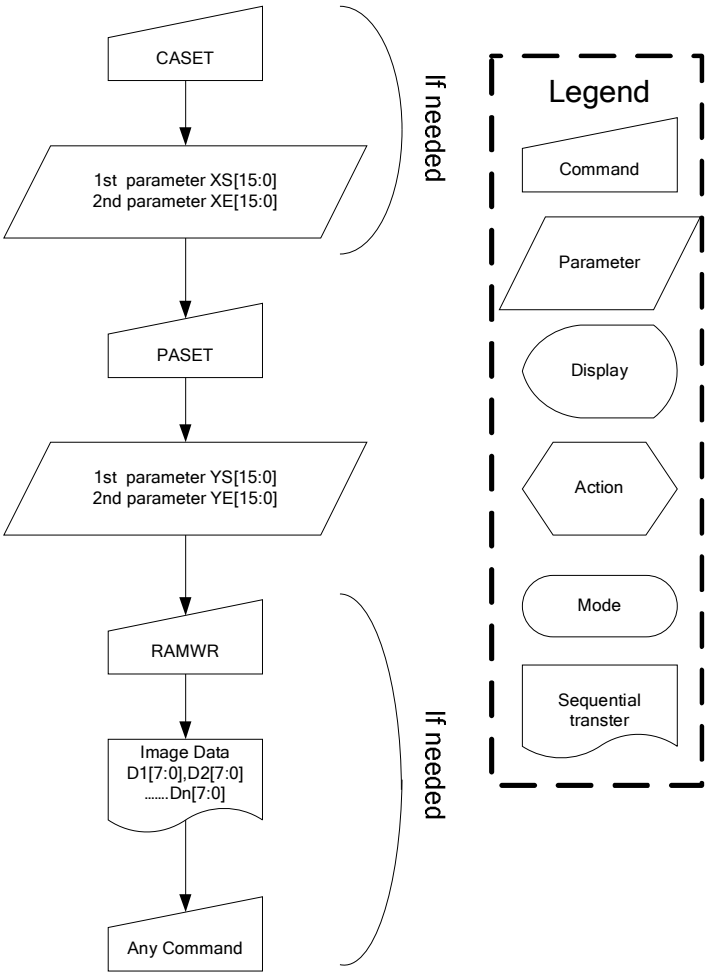
10.1.21 RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET (2Bh)	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
2nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3rd Parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
Description	The value of YS [7:0] and YE [7:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.  												
Restriction	YS [15:0] always must be equal to or less than YE [15:0] When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored. 1. 128X160 memory base (GM = '11') (Parameter range: 0 < YS [15:0] < YE [15:0] < 159 (009Fh)): MV="0" (Parameter range: 0 < YS [15:0] < YE [15:0] < 127 (007Fh)): MV="1" 2. 132X132 memory base (GM = '00') (Parameter range: 0 < YS [15:0] < YE [15:0] < 131 (00A1h)): MV="0" (Parameter range: 0 < YS [15:0] < YE [15:0] < 131 (0083h)): MV="1" 3. 132X162 memory base (GM = '00') (Parameter range: 0 < YS [15:0] < YE [15:0] < 161 (00A1h)): MV="0" (Parameter range: 0 < YS [15:0] < YE [15:0] < 131 (0083h)): MV="1"												

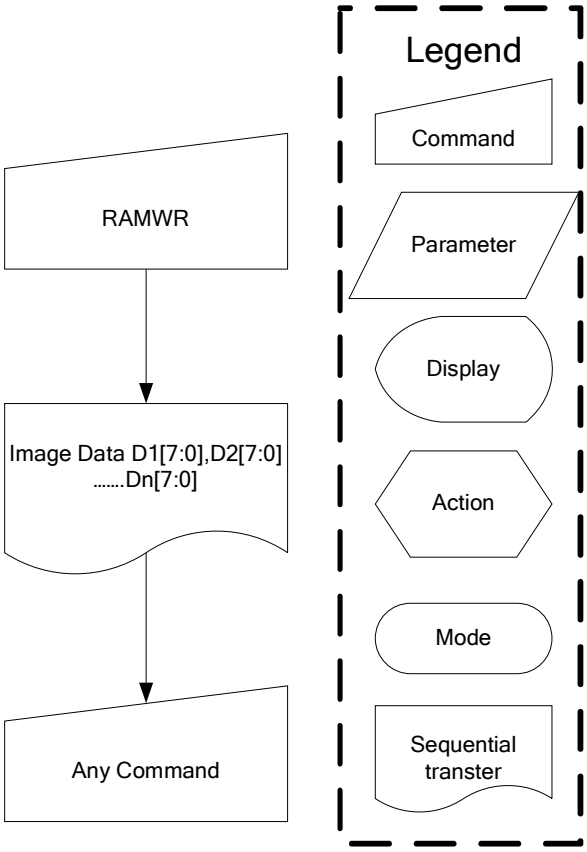
Default

GM status	Status	Default Value		
		YS [15:0]	YE [15:0] (MV='0 ')	YE [15:0] (MV='1')
GM='11' (128x160 memory base)	Power On Sequence	0000h	009Fh (159)	
	S/W Reset	0000h	009Fh (159)	007Fh (127)
	H/W Reset	0000h	009Fh (159)	
GM='01' (132x132 Memory Base)	Power On Sequence	0000h	0083h (131)	
	S/W Reset	0000h	0083h (131)	0083h (131)
	H/W Reset	0000h	0083h (131)	
GM='00' (132x162 memory base)	Power On Sequence	0000h	00A1h (161)	
	S/W Reset	0000h	00A1h (161)	0083h (131)
	H/W Reset	0000h	00A1h (161)	

Flow Chart



10.1.22 RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
|	1	↑	1	|	|	|	|	|	|	|	|	|	
Nth Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
Description	In all color modes, there is no restriction on length of parameters. 1. 128X160 memory base (GM = '11') 128x160x18-bit memory can be written by this command Memory range: (0000h, 0000h) -> (007Fh, 09Fh) 2. 132x132 memory base (GM = '01') 132x132x18-bit memory can be written on this command. Memory range: (0000h, 0000h) -> (0083h, 0083h) 3. 132x162 memory base (GM = '00') 132x162x18-bit memory can be written on this command. Memory range: (0000h, 0000h) -> (0083h, 00A1h)												
Default	Status: Power On Sequence — Default Value: Contents of memory is set randomly Status: S/W Reset — Default Value: Contents of memory is not cleared Status: H/W Reset — Default Value: Contents of memory is not cleared												
Flow Chart													

10.1.23 RGBSET (2Dh): Color Setting for 4K, 65K and 262K

2DH	RGBSET (Color Set for 4K, 65K, 262K and 16.7M)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGBSET	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)
1st Parameter	1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000	
|	1	↑	1	-	-	-	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	
|	1	↑	1	-	-	-	R315	R314	R313	R312	R311	R310	
|	1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000	
|	1	↑	1	-	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	
|	1	↑	1	-	-	-	G635	G634	G633	G632	G631	G630	
|	1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000	
|	1	↑	1	-	-	-	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	
128th Parameter	1	↑	1	-	-	-	B315	B314	B313	B312	B311	B310	

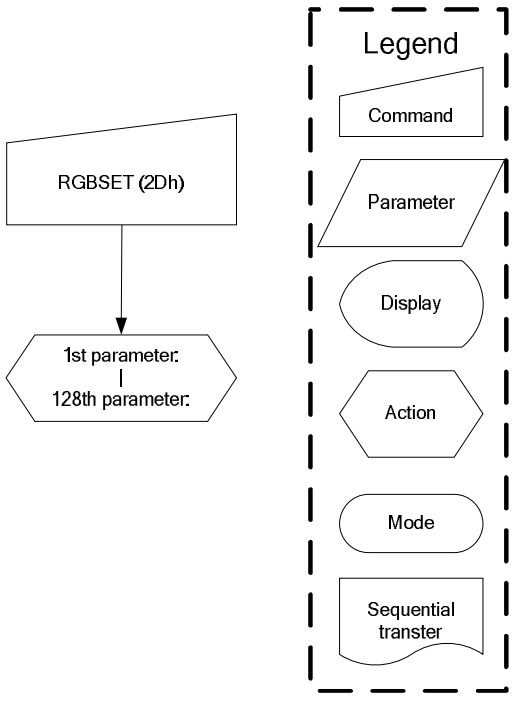
Description

This command is used to define the LUT for 12bits-to-16bits / 16-bit-to- 18bits color depth conversations.
128-Bytes must be written to the LUT regardless of the color mode. Only the values in Section 9.18 are referred.
In this condition, 4K-color (4-4-4) and 65K-color(5-6-5) data input are transferred 6(R)-6(G)-6(B) through RGB LUT table.
This command has no effect on other commands/parameters and Contents of frame memory.
Visible change takes effect next time the Frame Memory is written to.
Do not send any command before the last data is sent or LUT is not defined correctly.

Default

Status	Default Value
Power On Sequence	Random
S/W Reset	Contents of the look-up table protected
H/W Reset	Random

Flow Chart



10.1.24 RAMRD (2Eh): Memory Read

2EH	RAMHD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMHD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
|	1	1	↑	|	|	|	|	|	|	|	|	|	
(N+1)th Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	

Description

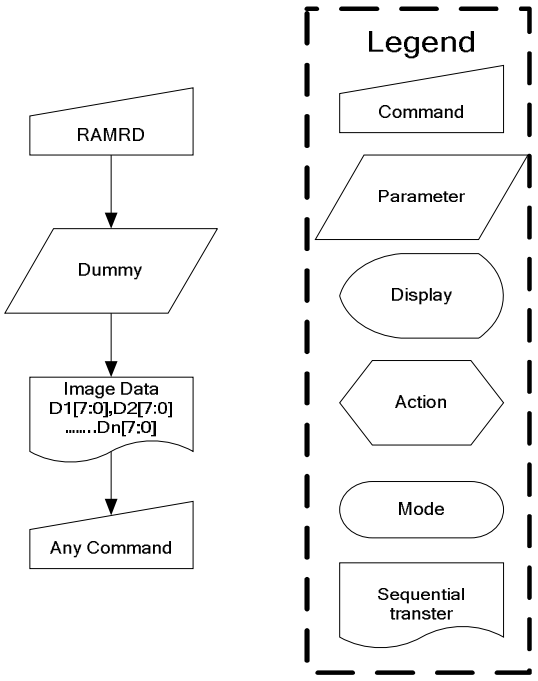
-This command is used to transfer data from frame memory to MCU.
-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
-The Start Column/Start Row positions are different in accordance with MADCTL setting.
-Then D[17:0] is read back from the frame memory and the column register and the row register incremented as section 9.10
-Frame Read can be cancelled by sending any other command.
-The data color coding is fixed to 18-bit in reading function. Please see section 9.8 “Data color coding” for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.

Note1: The Command 3Ah should be set to 66h when reading pixel data from frame memory. Please check the LUT in chapter 9.17 when using memory read function.

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart

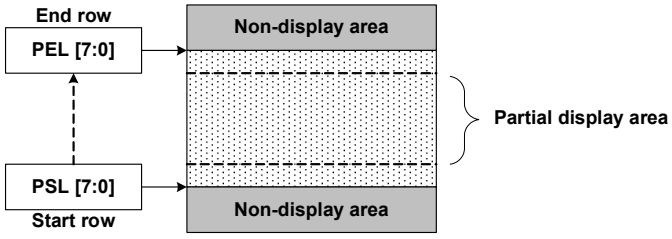


10.1.25 PTLAR (30h): Partial Area

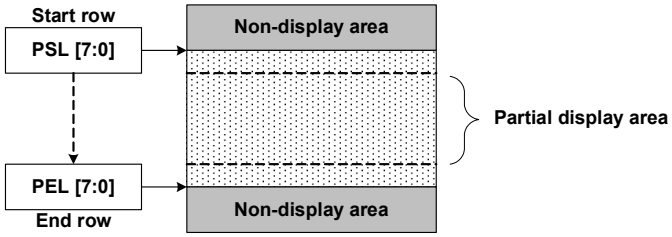
30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st Parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
2nd Parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3rd Parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4th Parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

Description

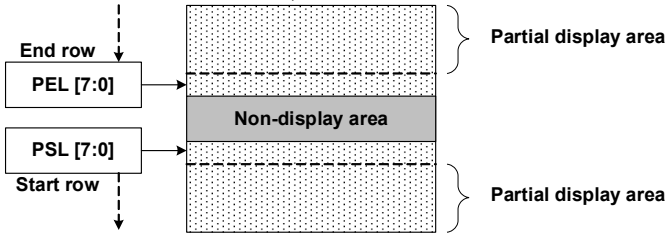
-This command defines the partial mode's display area.
-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.
-If End Row > Start Row, when MADCTL ML='0'



-If End Row > Start Row, when MADCTL ML='1'



-If End Row < Start Row, when MADCTL ML='0'

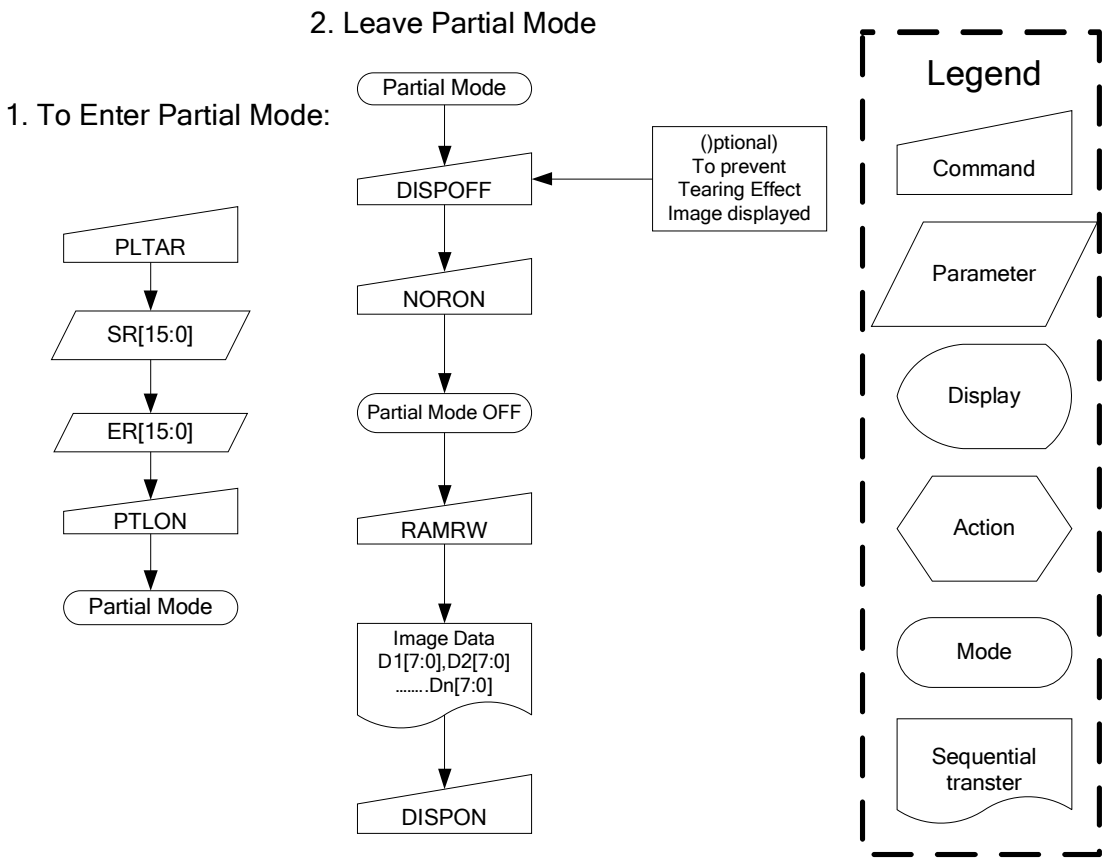


-If End Row = Start Row then the Partial Area will be one row deep.

Default

Status	Default Value			
	PSL [15:0]	PEL [15:0]		
GM[1:0]	"xx"	GM[1:0]="11"	GM[1:0]="01"	GM[1:0]="00"
Power On Sequence	0000h	009Fh	0083h	00A1h
S/W Reset	0000h	009Fh	0083h	00A1h
H/W Reset	0000h	009Fh	0083h	00A1h

Flow Chart

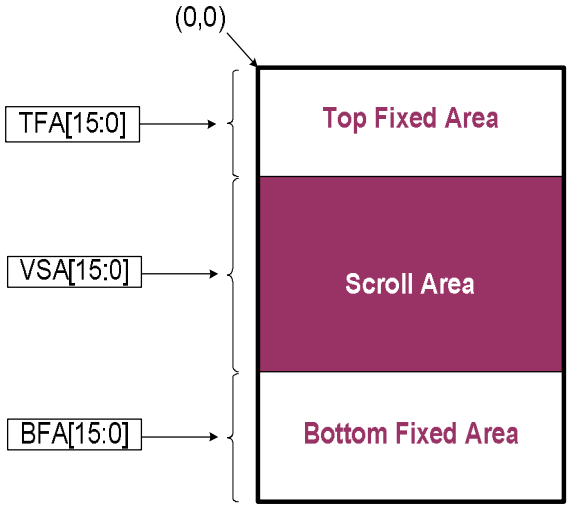


10.1.26 SCRLAR (33h): Scroll Area Set

33H	SCRLAR (Scroll Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SCRLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1st parameter	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-
2nd parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
3rd parameter	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-
4th parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
5th parameter	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-
6nd parameter	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

Description

-This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll
-When MADCTR B4=0
-The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
-The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.
-The 4th & 5th parameter BFA [6:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
TFA, VSA and BFA refer to the Frame Memory Line Pointer



Restriction

The condition is (TFA+VSA+BFA) = 162, otherwise Scrolling mode is undefined.
In Vertical Scroll Mode, MADCTR parameter MV should be set to '0'-this only affects the Frame Memory Write.
TFA[15:0], VSA[15:0] and BFA[15:0] is based on line unit.
TFA[15:0]= 0000h, 0001h, 0002h, 0003h, … , 00A2h
VSA[15:0]= 0000h, 0001h, 0002h, 0003h, … , 00A2h
BFA[15:0]= 0000h, 0001h, 0002h, 0003h, … , 00A2h

Register Availability

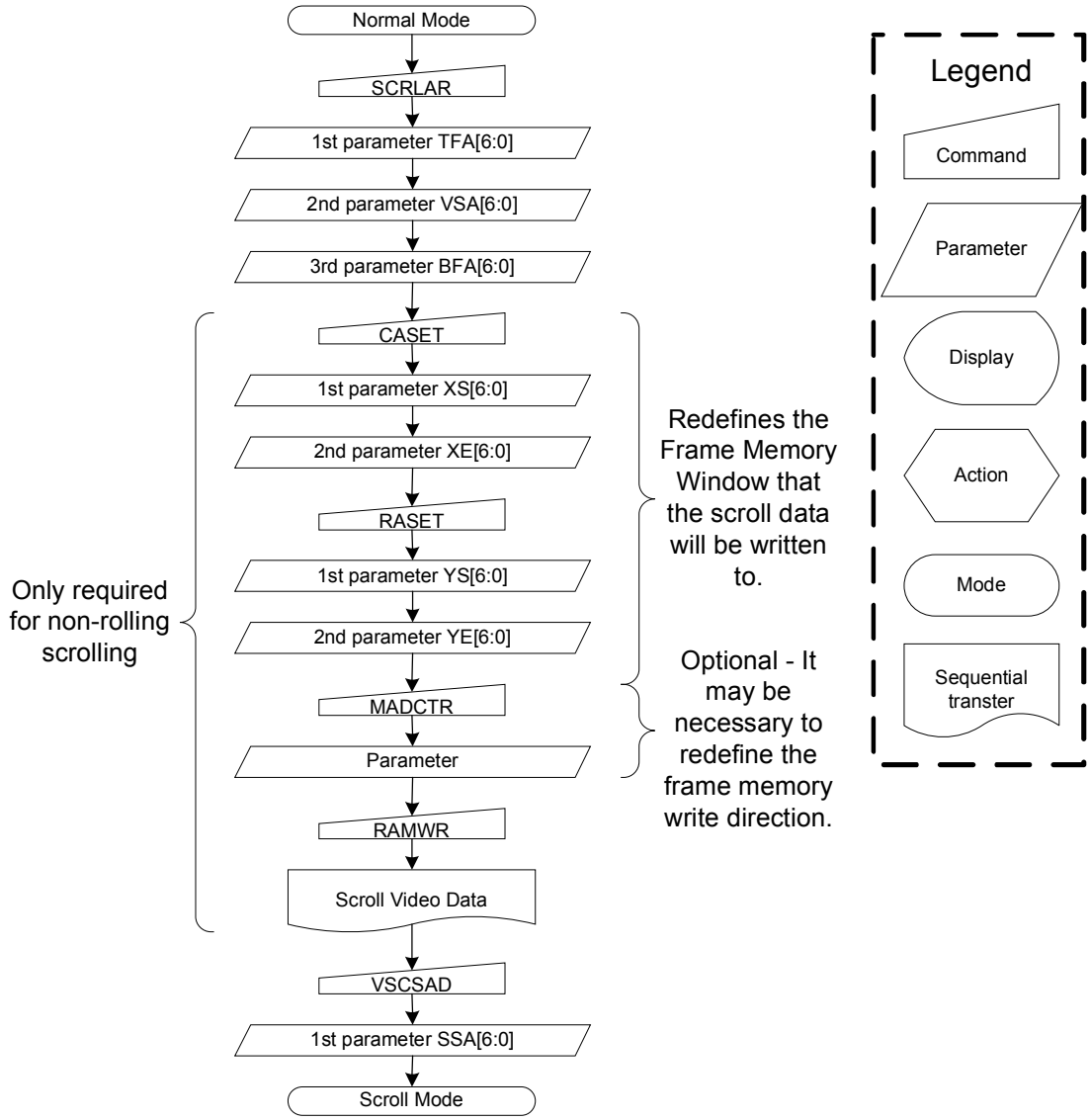
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value GM[1:0]= “11”		
Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=00A0h	BFA[15:0]=0000h
S/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A0h	BFA[15:0]=0000h
H/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A0h	BFA[15:0]=0000h
Status	Default Value GM[1:0]= “01”		
Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=0084h	BFA[15:0]=0000h
S/W Reset	TFA[15:0]=0000h	VSA[15:0]=0084h	BFA[15:0]=0000h
H/W Reset	TFA[15:0]=0000h	VSA[15:0]=0084h	BFA[15:0]=0000h
Status	Default Value GM[1:0]= “00”		
Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=00A2h	BFA[15:0]=0000h
S/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A2h	BFA[15:0]=0000h
H/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A2h	BFA[15:0]=0000h

Flow Chart

1. TO Enter Vertical Scroll Mode:



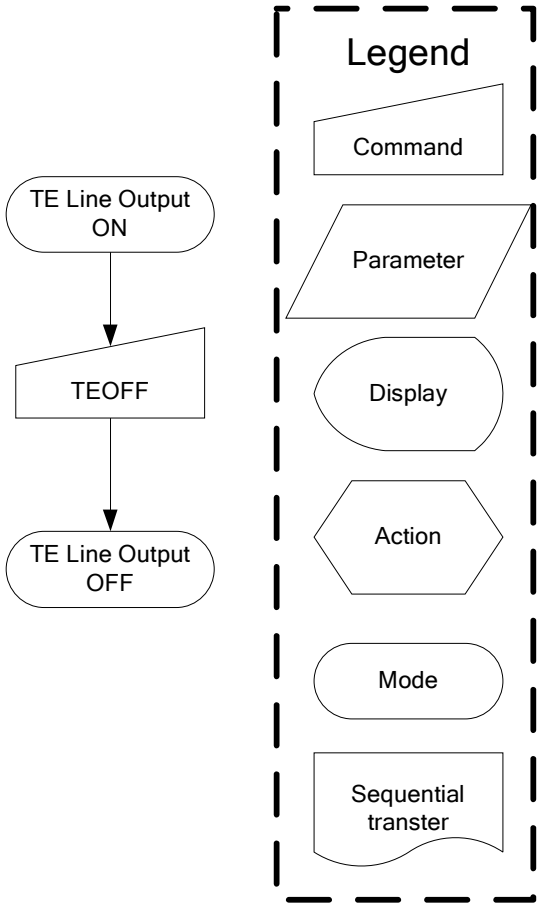
10.1.27 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
Parameter	No Parameter												-
Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												

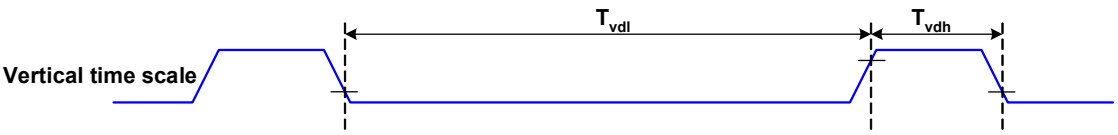
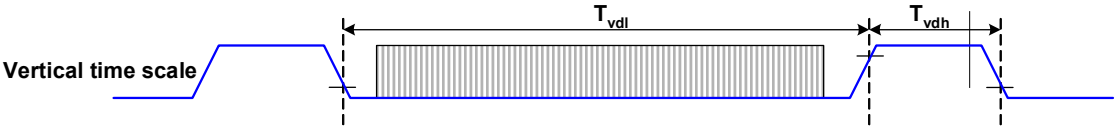
Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

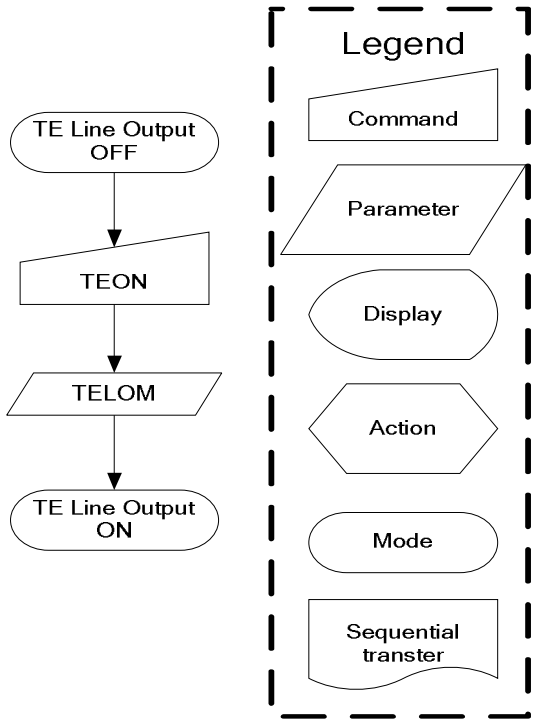
Flow Chart



10.1.28 TEON (35h): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
Parameter	1	↑	1	-	0	0	0	0	0	0	0	TEM	
Description	-This command is used to turn ON the Tearing Effect output signal from the TE signal line. -This output is not affected by changing MADCTL bit ML. -The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line: -When TEM ='0': The Tearing Effect output line consists of V-Blanking information only  -When TEM ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information  Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.												
Default													

Status	Default Value
Power On Sequence	Tearing effect off & TEM=0
S/W Reset	Tearing effect off & TEM=0
H/W Reset	Tearing effect off & TEM=0

Flow Chart	 TE Line Output OFF TEON TELOM TE Line Output ON Legend Command Parameter Display Action Mode Sequential transter

10.1.29 MADCTL (36h): Memory Data Access Control

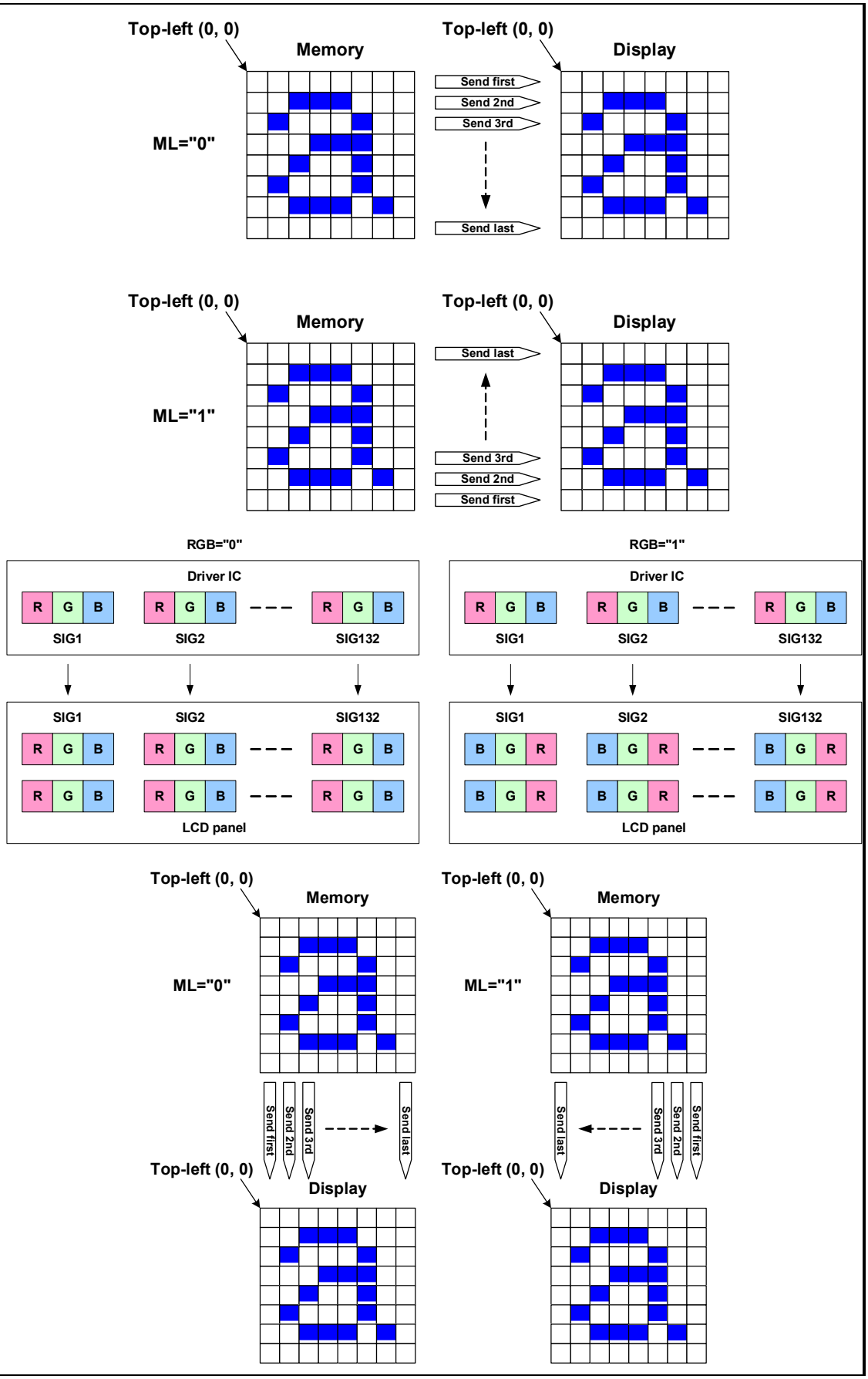
36H	MADCTL (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-	

Description

-This command defines read/ write scanning direction of frame memory.

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel)
MH	Horizontal Refresh Order	LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left

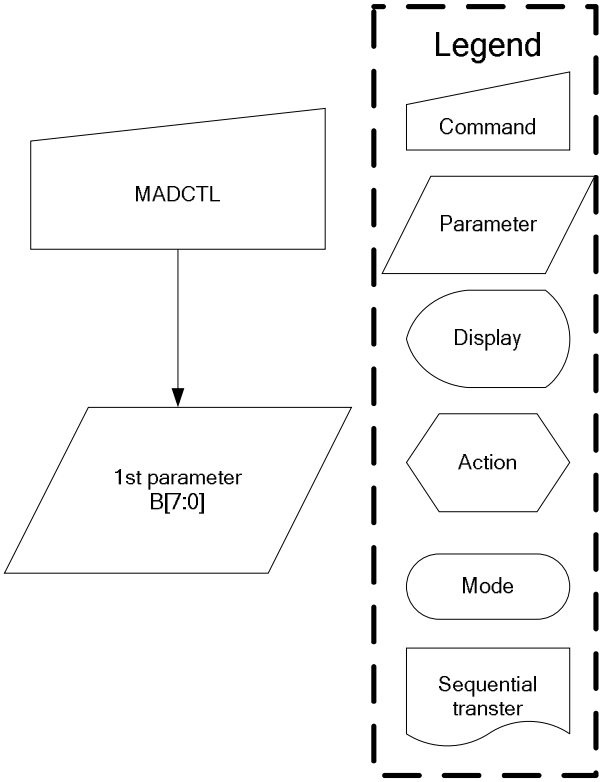
-Bit Assignment


Top-left (0, 0)
Memory
Top-left (0, 0)
Display
ML="0"
Send first
Send 2nd
Send 3rd
Send last
Top-left (0, 0)
Memory
Top-left (0, 0)
Display
ML="1"
Send last
Send 3rd
Send 2nd
Send first
RGB="0"
RGB="1"
Driver IC
R G B
SIG1
SIG2
SIG132
LCD panel
B G R
Top-left (0, 0)
Memory
ML="0"
Send first
Send 2nd
Send 3rd
Send last
Top-left (0, 0)
Display
Top-left (0, 0)
Memory
ML="1"
Send last
Send 3rd
Send 2nd
Send first
Top-left (0, 0)
Display

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0

Flow Chart

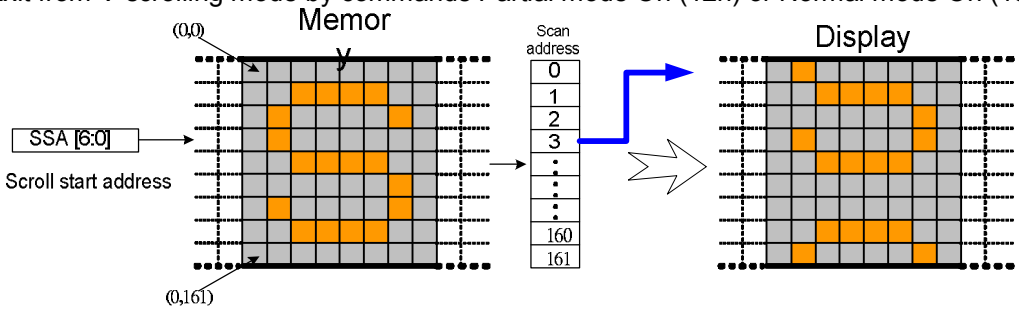


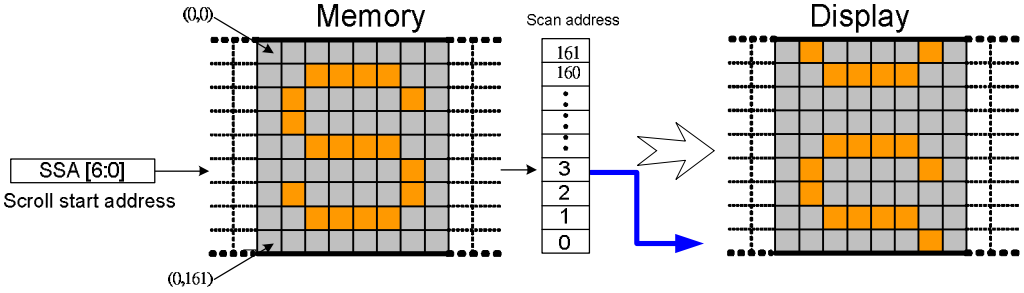
10.1.30 VSCSAD: Vertical Scroll Start Address of RAM (37h)

37H	SCRLAR (Scroll Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
Parameter1	1	↑	1	-	0	0	0	0	0	0	0	0	
Parameter2	1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	-

Description

-This command is used together with Vertical Scrolling Definition (33h).
-These two commands describe the scrolling area and the scrolling mode.
-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
-This command Start the scrolling.
-Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h)





NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
SSA refers to the Frame Memory line Pointer

Restriction

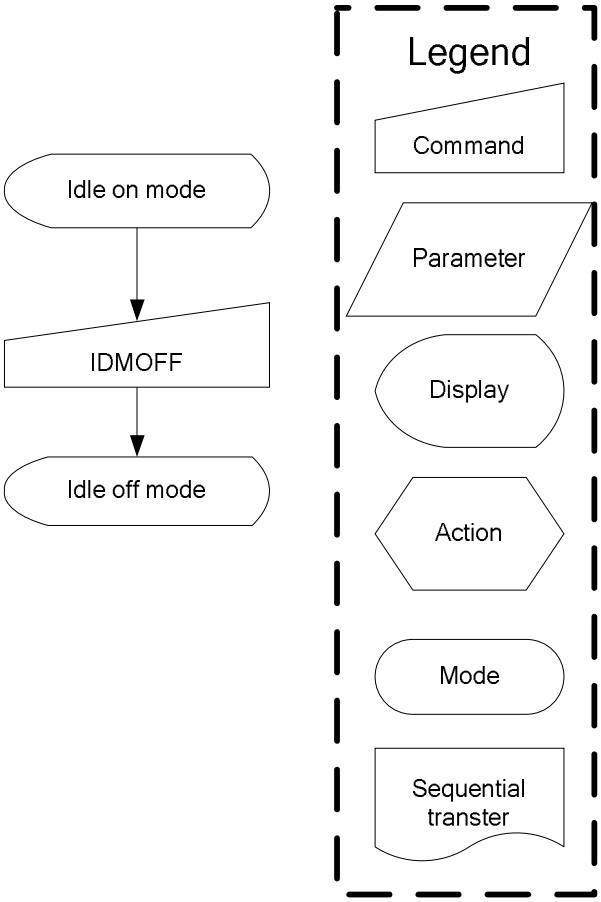
Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.
SSA [6:0] is based on line unit.
SSA [6:0] = 00h, 01h, 02h, 03h, … , A1h

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>
Flow Chart	See Vertical Scrolling Definition (33h) description.

10.1.31 IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
Parameter	No Parameter												-
Description	-This command is used to recover from Idle mode on. -In the idle off mode, 1. LCD can display 4096, 65k or 262k colors. 2. Normal frame frequency is applied.												
Default	Status / Default Value Power On Sequence: Idle Mode Off S/W Reset: Idle Mode Off H/W Reset: Idle Mode Off												
Flow Chart													

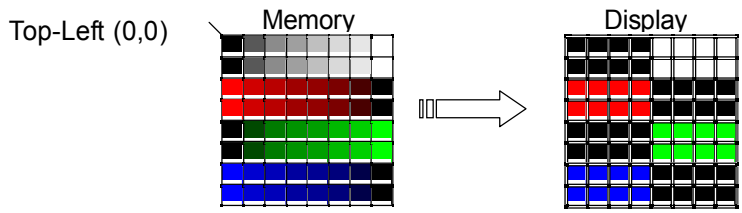
10.1.32 IDMON (39h): Idle Mode On

39H	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
Parameter	No Parameter												-

Description

-This command is used to enter into Idle mode on.
-There will be no abnormal visible effect on the display mode change transition.
-In the idle on mode,
1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)



Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

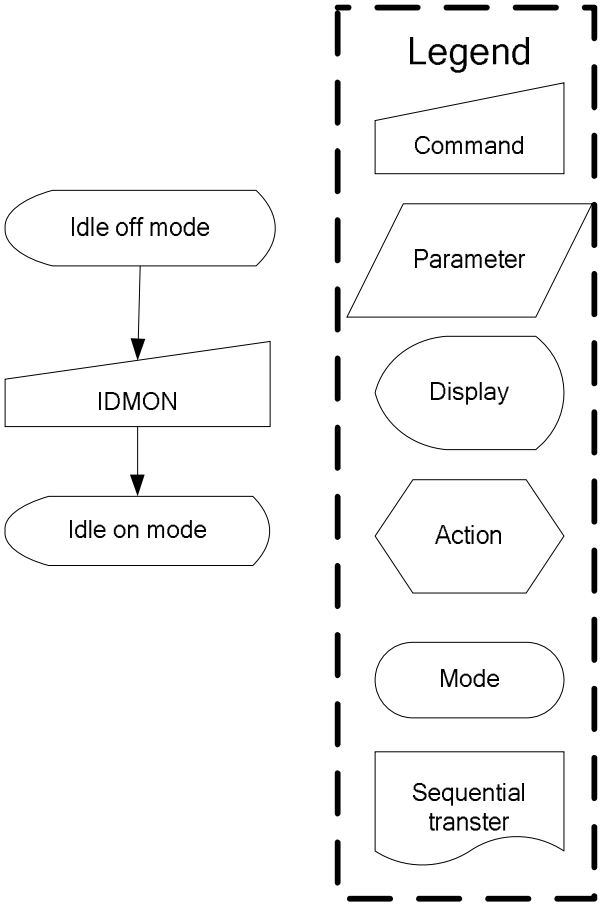
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

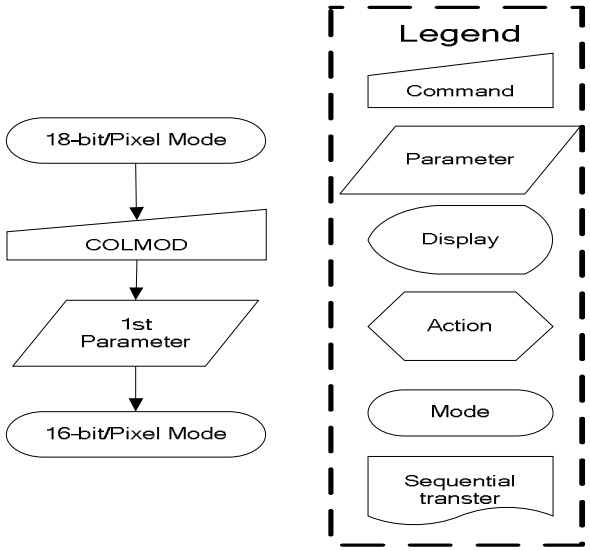
Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart



10.1.33 COLMOD (3Ah): Interface Pixel Format

<table>
<tr><th>3AH</th><th colspan="13">COLMOD (3Ah): Interface Pixel Format</th></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>COLMOD</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>(3Ah)</td></tr>
<tr><td>Parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>IFPF2</td><td>IFPF1</td><td>IFPF0</td><td></td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:
<table>
<tr><th colspan="2">IFPF[2:0]</th><th>MCU Interface Color Format</th></tr>
<tr><td>011</td><td>3</td><td>12-bit/pixel</td></tr>
<tr><td>101</td><td>5</td><td>16-bit/pixel</td></tr>
<tr><td>110</td><td>6</td><td>18-bit/pixel</td></tr>
<tr><td>111</td><td>7</td><td>No used</td></tr>
</table>
Note1: In 12-bit/Pixel, 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.
Note2: The Command 3Ah should be set at 55h when writing 16-bit/pixel data into frame memory, but 3Ah should be re-set to 66h when reading pixel data from frame memory. Please check the LUT in chapter 9.17 when using memory read function.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>IFPF[2:0]</th><th>VIPF[3:0]</th></tr>
<tr><td>Power On Sequence</td><td>0110(18-bit/Pixel)</td><td>0110(18-bit/Pixel)</td></tr>
<tr><td>S/W Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>0110(18-bit/Pixel)</td><td>0110(18-bit/Pixel)</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

10.1.34 RDID1 (DAh): Read ID1 Value

DAH	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
Description	-This read byte returns 8-bit LCD module's manufacturer ID -The 1st parameter is dummy data -The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID. NOTE: See command RDDID (04h), 2nd parameter.												

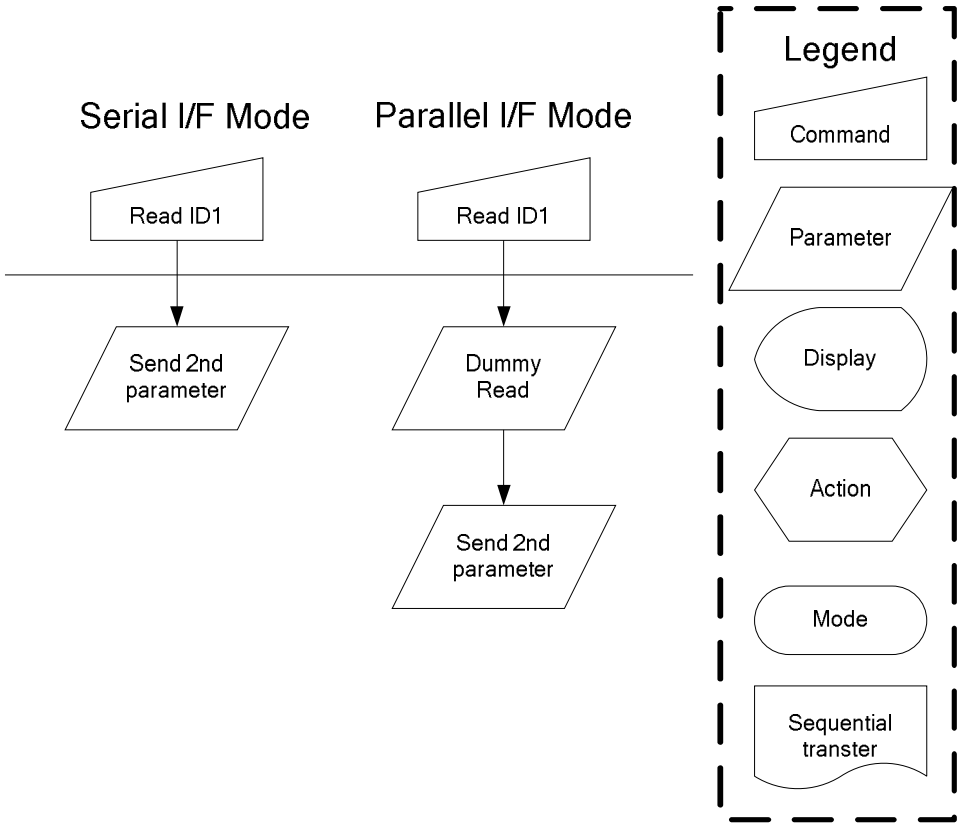
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0x7C
S/W Reset	0x7C
H/W Reset	0x7C

Flow Chart



10.1.35 RDID2 (DBh): Read ID2 Value

DBH	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

Description

-This read byte returns 8-bit LCD module/driver version ID
-The 1st parameter is dummy data
-The 2nd parameter (ID26 to ID20): LCD module/driver version ID
-Parameter Range: ID=80h to FFh

ID26 to ID20	Version	Changes
80h		
81h		
82h		
83h		

NOTE: See command RDDID (04h), 3rd parameter.

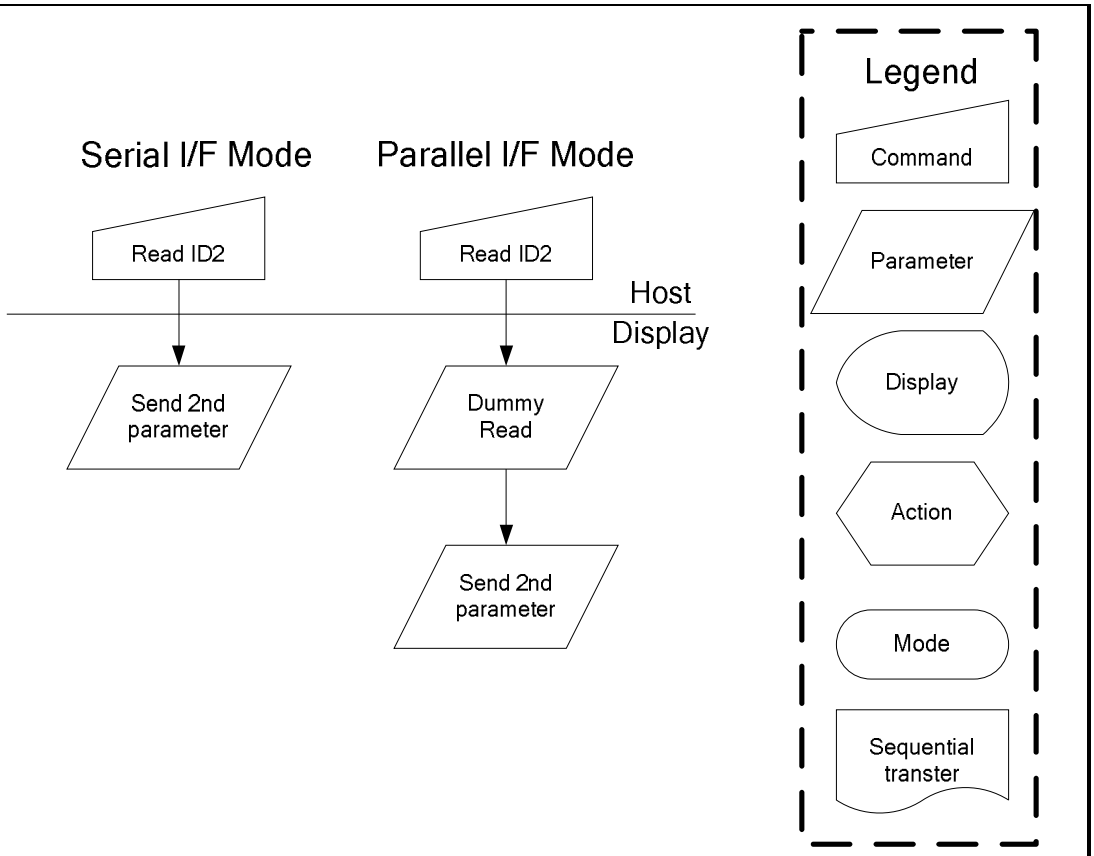
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	NV Value
S/W Reset	NV Value
H/W Reset	NV Value

Flow Chart


Serial I/F Mode
Parallel I/F Mode
Read ID2
Read ID2
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

10.1.36 RDID3 (DCh): Read ID3 Value

DCH	RDID3 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

Description

-This read byte returns 8-bit LCD module/driver ID.
-The 1st parameter is dummy data
-The 2nd parameter (ID37 to ID30): LCD module/driver ID.
NOTE: See command RDDID (04h), 4th parameter.

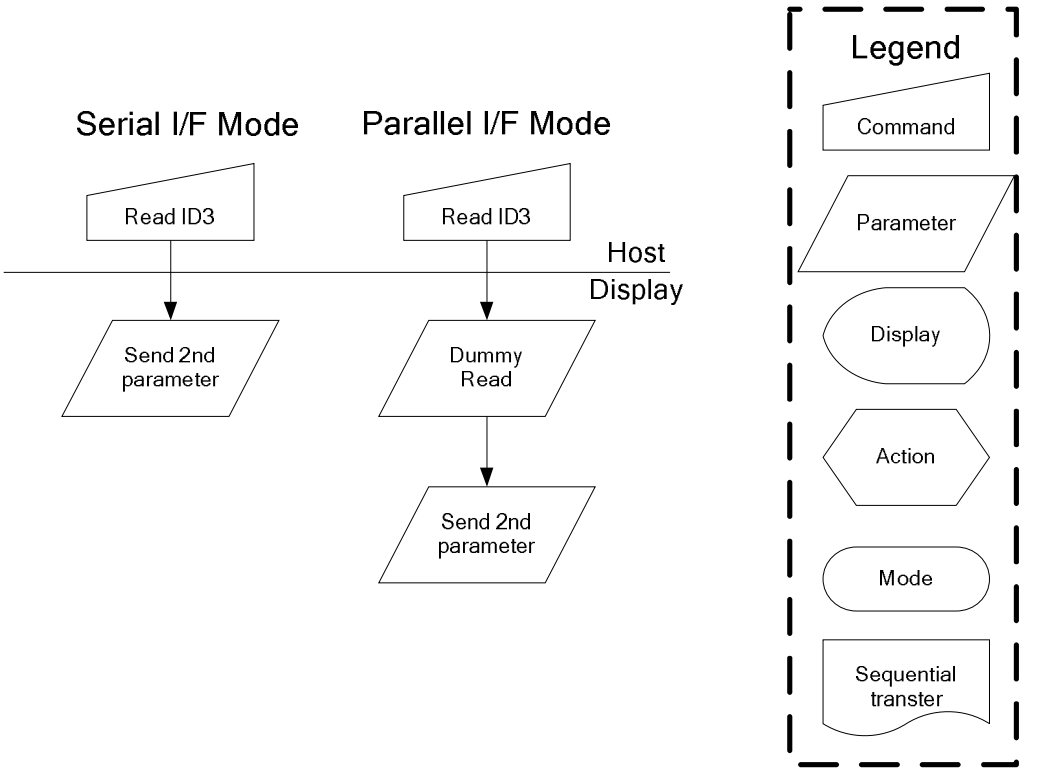
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	NV Value
S/W Reset	NV Value
H/W Reset	NV Value

Flow Chart



10.2 Panel Function Command List and Description

Table 18 Panel Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
FRMCTR1	0	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In Normal Mode (Full Colors)
		1	↑	1	-					RTNA3	RTNA2	RTNA1	RTNA0		RTNA Set 1-line Period FPA: Front Porch BPA: Back Porch
		1	↑	1	-			FPA5	FPA4	FPA3	FPA2	FPA1	FPA0		
		1	↑	1	-			BPA5	BPA4	BPA3	BPA2	BPA1	BPA0		
FRMCTR2	0	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle Mode (8-colors)
		1	↑	1	-					RTNB3	RTNB2	RTNB1	RTNB0		RTNB: Set 1-line Period FPB: Front Porch BPB: Back Porch
		1	↑	1	-			FPB5	FPB4	FPB3	FPB2	FPB1	FPB0		
		1	↑	1	-			BPB5	BPB4	BPB3	BPB2	BPB1	BPB0		
FRMCTR3	0	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	In Partial Mode + Full Colors
		1	↑	1	-					RTNC3	RTNC2	RTNC1	RTNC0		RTNC,RTND: Set 1-line Period FPC,FPD: Front Porch BPC,BPD: Back Porch
		1	↑	1	-			FPC5	FPC4	FPC3	FPC2	FPC1	FPC0		
		1	↑	1	-			BPC5	BPC4	BPC3	BPC2	BPC1	BPC0		
		1	↑	1	-					RTND3	RTND2	RTND1	RTND0		
		1	↑	1	-			FPD5	FPD4	FPD3	FPD2	FPD1	FPD0		
		1	↑	1	-			BPD5	BPD4	BPD3	BPD2	BPD1	BPD0		
INVCTR	0	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display Inversion Control
		1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC		NLA,NLB,NLC Set Inversion

Table 19 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PWCTR1	0	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	Power Control Setting
		1	↑	1	-	AVDD [2]	AVDD [1]	AVDD [0]	VRHP 4	VRHP 3	VRHP 2	VRHP 1	VRHP 0		VRH: Set the GVDD Voltage
		1	↑	1	-	0	0	0	VRHN 4	VRHN 3	VRHN 2	VRHN 1	VRHN 0		
		1	↑	1		MODE [1]	MODE [0]	0	0	0	1	0	0		
PWCTR2	0	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	Power Control Setting
		1	↑	1	-	VGH25[1]	VGH25[0]	-	-	VGLSEL[1]	VGLSEL[0]	VGHBT[1]	VGHBT[0]		BT: Set VGH/ VGL Voltage
PWCTR3	0	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	In Normal Mode (Full Colors)
		1	↑	1	-	DCA9	DCA8	SAPA 2	SAPA 1	SAPA 0	APA2	APA1	APA0		APA: Adjust the Operational Amplifier DCA: Adjust the Booster Voltage
					-	DCA7	DCA6	DCA5	DCA4	DCA3	DCA2	DCA1	DCA0		
PWCTR4	0	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)	In Idle Mode (8-colors)
		1	↑	1	-	DCB9	DCB8	SAPB 2	SAPB 1	SAPB 0	APB2	APB1	APB0		APB: Adjust the Operational Amplifier DCB: Adjust the Booster Voltage
					-	DCB7	DCB6	DCB5	DCB4	DCB3	DCB2	DCB1	DCB0		
PWCTR5	0	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	In Partial Mode + Full colors
		1	↑	1	-	DCC9	DCC8	SAPC 2	SAPC 1	SAPC 0	APC2	APC1	APC0		APC: Adjust the Operational Amplifier DCC: Adjust the Booster Circuit for Idle mode
		1	↑	1	-	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0		
VMCTR1	0	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	VCOM Control 1
		1	↑	1	-	-	-	VCOMS5	VCOMS4	VCOMS3	VCOMS2	VCOMS1	VCOMS0		VCOM Voltage Control
VMOFCTR	0	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	Set VCOM Offset control
		1	↑	1	-	-	-	-	VMF4	VMF3	VMF2	VMF1	VMF0		
WRID2	0	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	Set LCM Version Code
		1	↑	1	-	-	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]		

"-": Don't care

Note 1: C0h to C7h are fixed for about power controller

Table 20 Panel Function Command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRID3	0	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Customer Project Code
		1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Set the Project Code at ID3
NVCTR1	0	0	↑	1	-	1	1	0	1	1	0	0	1	(D9)	NVM Control Status
		1	↑	1	-	0	VMF _EN	ID2 _EN	0	0	0	0	EXT_ R		
NVCTR2	0	0	↑	1	-	1	1	0	1	1	1	1	0	(Deh)	NVM Read Command
		1	↑	1	-	1	1	1	1	0	1	0	1	F5	
		1	↑	1	-	1	0	1	0	0	1	0	1	A5	Action Code
NVCTR3	0	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	NVM Write Command Action Code
		1	↑	1	-	NVM _ CMD7	NVM _ CMD6	NVM _ CMD5	NVM _ CMD4	NVM _ CMD3	NVM _ CMD2	NVM _ CMD1	NVM _ CMD0		
		1	↑	1	-	1	0	1	0	0	1	0	1	A5	

"-": Don't care

Note 1: The D1h to D3h registers are fixed for about ID code setting.

Note 2: The D9h, Deh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)

Table 21 Panel Function Command List (4)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
GAMCTRP1	0	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Set
		1	↑	1	-	-	-	VRFP[5]	VRFP[4]	VRFP[3]	VRFP[2]	VRFP[1]	VRF0P[0]		Gamma Adjustment (+ Polarity)
		1	↑	1	-	-	-	VOS0P[5]	VOS0P[4]	VOS0P[3]	VOS0P[2]	VOS0P[1]	VOS0P[0]		
		1	↑	1	-	-	-	PKP0[5]	PKP0[4]	PKP0[3]	PKP0[2]	PKP0[1]	PKP0[0]		
		1	↑	1	-	-	-	PKP1[5]	PKP1[4]	PKP1[3]	PKP1[2]	PKP1[1]	PKP1[0]		
		1	↑	1	-	-	-	PKP2[5]	PKP2[4]	PKP2[3]	PKP2[2]	PKP2[1]	PKP2[0]		
		1	↑	1	-	-	-	PKP3[5]	PKP3[4]	PKP3[3]	PKP3[2]	PKP3[1]	PKP3[0]		
		1	↑	1	-	-	-	PKP4[5]	PKP4[4]	PKP4[3]	PKP4[2]	PKP4[1]	PKP4[0]		
		1	↑	1	-	-	-	PKP5[5]	PKP5[4]	PKP5[3]	PKP5[2]	PKP5[1]	PKP5[0]		
		1	↑	1	-	-	-	PKP6[5]	PKP6[4]	PKP6[3]	PKP6[2]	PKP6[1]	PKP6[0]		
		1	↑	1	-	-	-	PKP7[5]	PKP7[4]	PKP7[3]	PKP7[2]	PKP7[1]	PKP7[0]		
		1	↑	1	-	-	-	PKP8[5]	PKP8[4]	PKP8[3]	PKP8[2]	PKP8[1]	PKP8[0]		
		1	↑	1				PKP9[5]	PKP9[4]	PKP9[3]	PKP9[2]	PKP9[1]	PKP9[0]		
		1	↑	1	-	-	-	SELV0P[5]	SELV0P[4]	SELV0P[3]	SELV0P[2]	SELV0P[1]	SELV0P[0]		
		1	↑	1	-	-	-	SELV1P[5]	SELV1P[4]	SELV1P[3]	SELV1P[2]	SELV1P[1]	SELV1P[0]		
		1	↑	1	-	-	-	SELV62P[5]	SELV62P[4]	SELV62P[3]	SELV62P[2]	SELV62P[1]	SELV62P[0]		
		1	↑	1	-	-	-	SELV63P[5]	SELV63P[4]	SELV63P[3]	SELV63P[2]	SELV63P[1]	SELV63P[0]		
GAMCTRN1	0	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Set
		1	↑	1	-	-	-	VRF0N[5]	VRF0N[4]	VRF0N[3]	VRF0N[2]	VRF0N[1]	VRF0N[0]		Gamma Adjustment (- Polarity)
		1	↑	1	-	-	-	VOS0N[5]	VOS0N[4]	VOS0N[3]	VOS0N[2]	VOS0N[1]	VOS0N[0]		
		1	↑	1	-	-	-	PKN0[5]	PKN0[4]	PKN0[3]	PKN0[2]	PKN0[1]	PKN0[0]		
		1	↑	1	-	-	-	PKN1[5]	PKN1[4]	PKN1[3]	PKN1[2]	PKN1[1]	PKN1[0]		
		1	↑	1	-	-	-	PKN2[5]	PKN2[4]	PKN2[3]	PKN2[2]	PKN2[1]	PKN2[0]		
		1	↑	1	-	-	-	PKN3[5]	PKN3[4]	PKN3[3]	PKN3[2]	PKN3[1]	PKN3[0]		
		1	↑	1	-	-	-	PKN4[5]	PKN4[4]	PKN4[3]	PKN4[2]	PKN4[1]	PKN4[0]		
		1	↑	1	-	-	-	PKN5[5]	PKN5[4]	PKN5[3]	PKN5[2]	PKN5[1]	PKN5[0]		
		1	↑	1	-	-	-	PKN6[5]	PKN6[4]	PKN6[3]	PKN6[2]	PKN6[1]	PKN6[0]		
		1	↑	1	-	-	-	PKN7[5]	PKN7[4]	PKN7[3]	PKN7[2]	PKN7[1]	PKN7[0]		
		1	↑	1	-	-	-	PKN8[5]	PKN8[4]	PKN8[3]	PKN8[2]	PKN8[1]	PKN8[0]		
		1	↑	1	-			PKN9[5]	PKN9[4]	PKN9[3]	PKN9[2]	PKN9[1]	PKN9[0]		
		1	↑	1	-	-	-	SELV0N[5]	SELV0N[4]	SELV0N[3]	SELV0N[2]	SELV0N[1]	SELV0N[0]		
		1	↑	1	-	-	-	SELV1N[5]	SELV1N[4]	SELV1N[3]	SELV1N[2]	SELV1N[1]	SELV1N[0]		
		1	↑	1	-	-	-	SELV62N[5]	SELV62N[4]	SELV62N[3]	SELV62N[2]	SELV62N[1]	SELV62N[0]		
		1	↑	1	-	-	-	SELV63N[5]	SELV63N[4]	SELV63N[3]	SELV63N[2]	SELV63N[1]	SELV63N[0]		
GCV	0	1	↑	1	-	1	1	1	1	1	1	0	0	(FCh)	Gate clock Variable
		1	↑	1	-	GCV Enable1	GCV Enable0	0	0	Clk_ Variable1	Clk_ Variable0	0	0		

"-": Don't care

Note 1: E0-E1 registers are fixed for adjusting Gamma

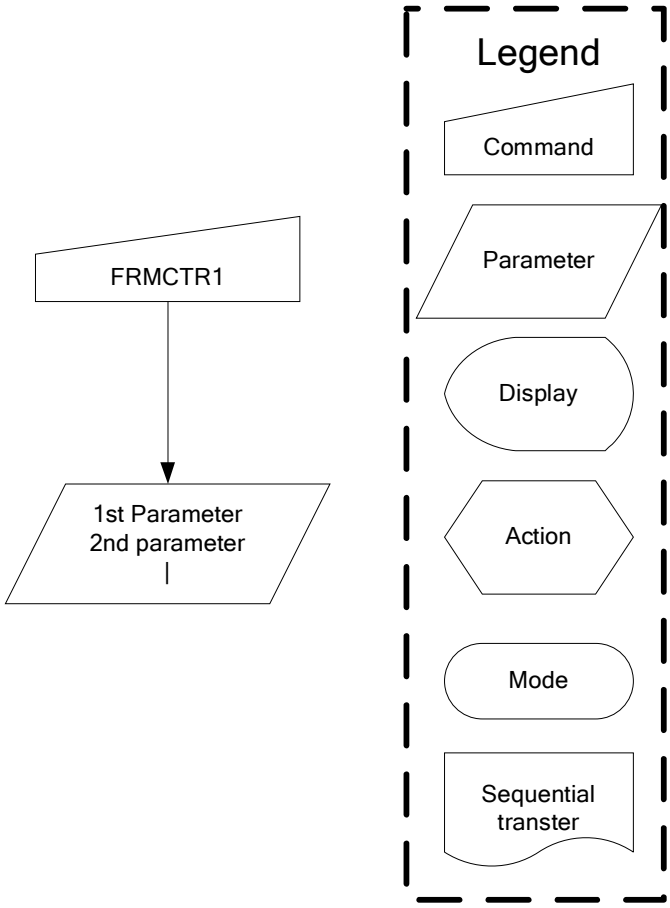
10.2.1 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1H	FRMCTR1 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st Parameter	1	↑	1	-	-	-	-	-	RTNA 3	RTNA 2	RTNA 1	RTNA 0	
2nd Parameter	1	↑	1	-	-	-	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0	
3rd Parameter	1	↑	1	-	-	-	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0	
Description	-Set the frame frequency of the full colors normal mode. - Frame rate=fosc/((RTNA x 2 + 40) x (LINE + FPA + BPA +2)) -fosc = 850kHz -FPA > 0, BPA > 0												

Default

Status	Default Value		
	GM[1:0] = "00"	GM[1:0] = "01"	GM[1:0] = "11"
Power On Sequence	05h/3Ah/3Ah	08h/3Bh/3Bh	05h/3Ch/3Ch
S/W Reset	05h/3Ah/3Ah	08h/3Bh/3Bh	05h/3Ch/3Ch
H/W Reset	05h/3Ah/3Ah	08h/3Bh/3Bh	05h/3Ch/3Ch

Flow Chart

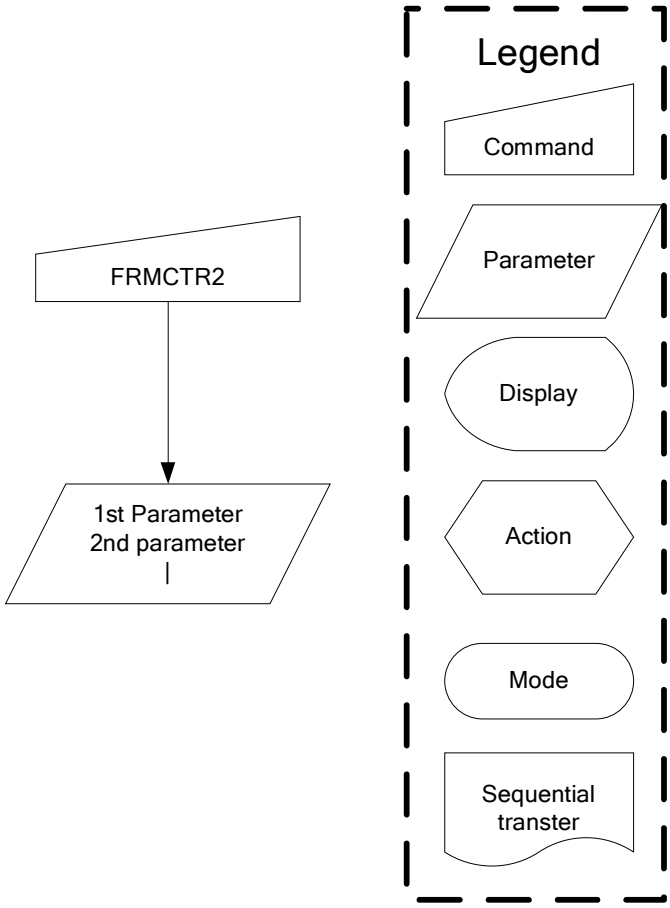


10.2.2 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

B2H	FRMCTR2 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st parameter	1	↑	1	-	-	-	-	-	RTNB 3	RTNB 2	RTNB 1	RTNB 0	
2nd parameter	1	↑	1	-	-	-	FPB5	FPB4	FPB3	FPB2	FPB1	FPB0	
3rd parameter	1	↑	1	-	-	-	BPB5	BPB4	BPB3	BPB2	BPB1	BPB0	
Description	-Set the frame frequency of the Idle mode. - Frame rate=fosc/((RTNA x 2 + 40) x (LINE + FPB + BPB +2)) -fosc = 850kHz -FPB > 0, BPB > 0												
Default													

Status	Default Value		
	GM[1:0] = “00”	GM[1:0] = “01”	GM[1:0] = “11”
Power On Sequence	05h/3Ah/3Ah	08h/3Bh/3Bh	05h/3Ch/3Ch
S/W Reset	05h/3Ah/3Ah	08h/3Bh/3Bh	05h/3Ch/3Ch
H/W Reset	05h/3Ah/3Ah	08h/3Bh/3Bh	05h/3Ch/3Ch

Flow Chart



10.2.3 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

B3H	FRMCTR3 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1st parameter	1	↑	1	-	-	-	-	-	RTNC	RTNC	RTNC	RTNC	
2nd parameter	1	↑	1	-	-	-	FPC5	FPC4	FPC3	FPC2	FPC1	FPC0	
3rd parameter	1	↑	1	-	-	-	BPC5	BPC4	BPC3	BPC2	BPC1	BPC0	
4th parameter	1	↑	1	-	-	-	-	-	RTND	RTND	RTND	RTND	
5th parameter	1	↑	1	-	-	-	FPD5	FPD4	FPD3	FPD2	FPD1	FPD0	
6th parameter	1	↑	1	-	-	-	BPD5	BPD4	BPD3	BPD2	BPD1	BPD0	

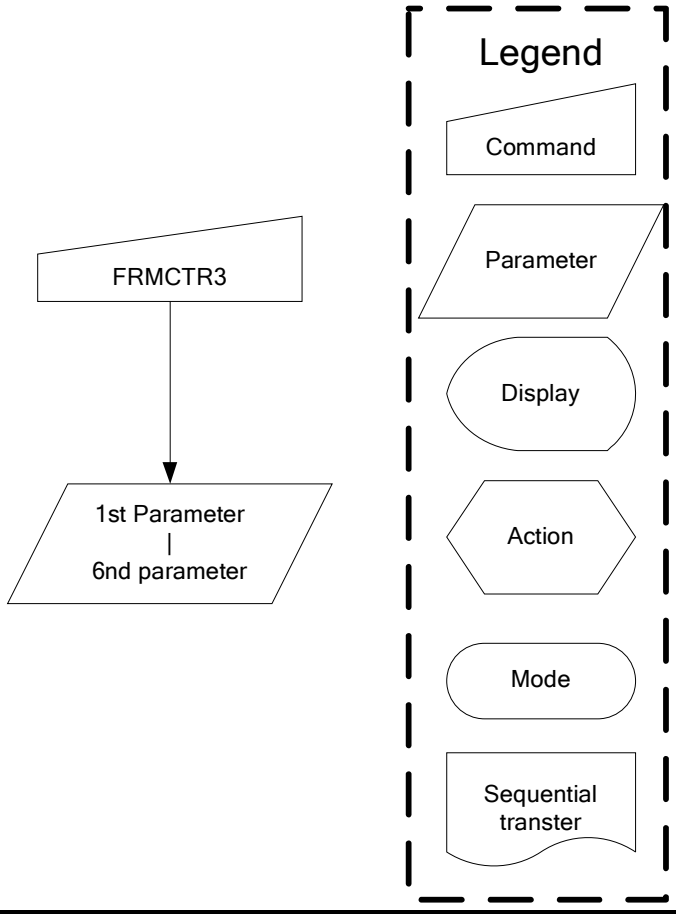
Description

-Set the frame frequency of the Partial mode/ full colors.
- 1st parameter to 3rd parameter are used in dot inversion mode.
- 4th parameter to 6th parameter are used in column inversion mode.
- Frame rate=fosc/((RTNA x 2 + 40) x (LINE + FPC + BPC +2))
-fosc = 850kHz
-FPC > 0, BPC > 0

Default

Status	Default Value		
	GM[1:0] = "00"	GM[1:0] = "01"	GM[1:0] = "11"
Power On Sequence	05h/3Ah/3Ah 05h/3Ah/3Ah	08h/3Bh/3Bh 08h/3Bh/3Bh	05h/3Ch/3Ch 05h/3Ch/3Ch
S/W Reset	05h/3Ah/3Ah 05h/3Ah/3Ah	08h/3Bh/3Bh 08h/3Bh/3Bh	05h/3Ch/3Ch 05h/3Ch/3Ch
H/W Reset	05h/3Ah/3Ah 05h/3Ah/3Ah	08h/3Bh/3Bh 08h/3Bh/3Bh	05h/3Ch/3Ch 05h/3Ch/3Ch

Flow Chart



10.2.4 INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	

Description

-Display Inversion mode control
-NLA: Inversion setting in full colors normal mode (Normal mode on)

NLA	Inversion setting in full Colors normal mode
0	Dot Inversion
1	Column Inversion

-NLB: Inversion setting in Idle mode (Idle mode on)

NLB	Inversion setting in Idle mode
0	Dot Inversion
1	Column Inversion

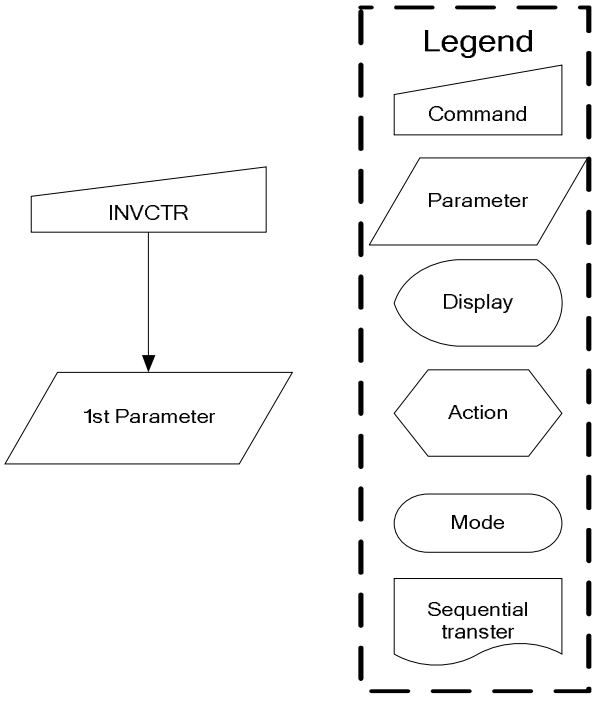
-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLC	Inversion setting in full Colors partial mode
0	Dot Inversion
1	Column Inversion

Default

Status	Default Value
	B4h
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



10.2.5 PWCTR1 (C0h): Power Control 1

C0H	PWCTR1 (Power Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st parameter	1	↑	1	-	AVDD[2]	AVDD[1]	AVDD[0]	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0	
2nd parameter	1	↑	1	-	0	0	0	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0	
3rd parameter	1	↑	1	-	MODE[1]	MODE[0]	0	0	0	1	VRHN5	VRHP5	

Description

AVDD[2:0]	AVDD
000	4.5
001	4.6
010	4.7
011	4.8
100	4.9
101	5
110	5.1
111	5.2

MODE[1:0]	FUNCTION
00	2X
01	Don't use this setting, reserve for testing.
10	AUTO
11	Don't use this setting, reserve for testing.

VRHP[5]	0	1
VRHP[4:0]	GVDD	GVDD
00000	4.7	5
00001	4.65	4.95
00010	4.6	4.9
00011	4.55	4.85
00100	4.5	4.8
00101	4.45	4.75
00110	4.4	
00111	4.35	
01000	4.3	
01001	4.25	
01010	4.2	
01011	4.15	
01100	4.1	
01101	4.05	
01110	4	
01111	3.95	
10000	3.9	
10001	3.85	
10010	3.8	
10011	3.75	
10100	3.7	
10101	3.65	
10110	3.6	
10111	3.55	
11000	3.5	
11001	3.45	
11010	3.4	
11011	3.35	
11100	3.3	
11101	3.25	
11110	3.2	
11111	3.15	

VRHN[5]	0	1
VRHN[4:0]	GVCL	GVCL
00000	-4.7	-5
00001	-4.65	-4.95
00010	-4.6	-4.9
00011	-4.55	-4.85
00100	-4.5	-4.8
00101	-4.45	-4.75
00110	-4.4	
00111	-4.35	
01000	-4.3	
01001	-4.25	
01010	-4.2	
01011	-4.15	
01100	-4.1	
01101	-4.05	
01110	-4	
01111	-3.95	
10000	-3.9	
10001	-3.85	
10010	-3.8	
10011	-3.75	
10100	-3.7	
10101	-3.65	
10110	-3.6	
10111	-3.55	
11000	-3.5	
11001	-3.45	
11010	-3.4	
11011	-3.35	
11100	-3.3	
11101	-3.25	
11110	-3.2	
11111	-3.15	

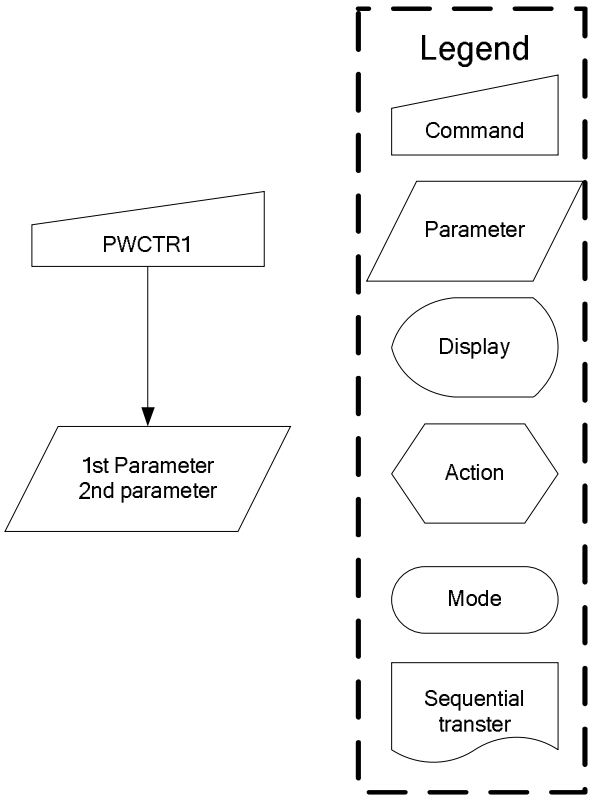
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C0h
Power On Sequence	A8h/08h/84h
S/W Reset	A8h/08h/84h
H/W Reset	A8h/08h/84h

Flow Chart



10.2.6 PWCTR2 (C1h): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st parameter	1	↑	1		VGH25[1]	VGH25[0]	-	-	VGLSEL[1]	VGLSEL[0]	VGHBT[1]	VGHBT[0]	

Description

-Set the VGH and VGL supply power level

VGH25[1:0]	V25
00	2.1
01	2.2
10	2.3
11	2.4

VGHBT[1:0]	VGH
00	2*AVDD+VGH25-0.5
01	3*AVDD-0.5
10	3*AVDD+VGH25-0.5
11	Don't use this setting, reserve for testing.

VGLSEL[1:0]	VGL
00	-7.5
01	-10
10	-12.5
11	-13

Restriction

-The deviation value of VGH/ VGL between with Measurement and Specification: Max <= 1V

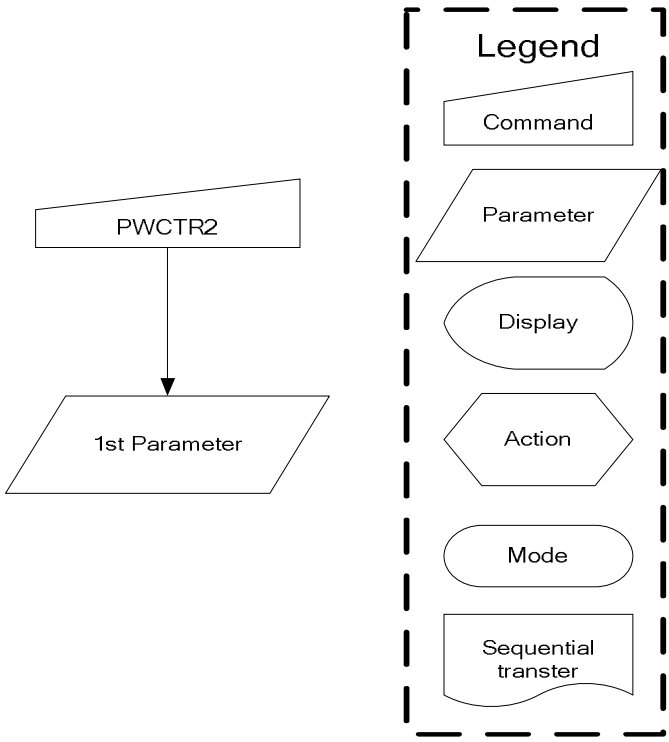
-VGH-VGL <= 32V

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C1h
Power On Sequence	C0h
S/W Reset	C0h
H/W Reset	C0h

Flow Chart	

PWCTR2
1st Parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

10.2.7 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

C2H	PWCTR3 (Power Control 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st	1	↑	1	-	DCA9	DCA8	SAPA2	SAPA1	SAPA0	APA2	APA1	APA0	
2nd	1	↑	1	-	DCA7	DCA6	DCA5	DCA4	DCA3	DCA2	DCA1	DCA0	

Description

-Set the amount of current in Operational amplifier in normal mode/full colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

AP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

SAP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

-Set the Booster circuit Step-up cycle in Normal mode/ full colors.

	DCA[9:8]	DCA[7:6]	DCA[5:4]	DCA[3:2]	DCA[1:0]
00	BCLK/1	BCLK/3	BCLK/1	BCLK/1	BCLK/1
01	BCLK/3	BCLK/1	BCLK/3	BCLK/3	BCLK/3
10	BCLK/2	BCLK/4	BCLK/2	BCLK/2	BCLK/2
11	BCLK/4	BCLK/2	BCLK/4	BCLK/4	BCLK/4

Note: BCLK is Clock frequency for Booster circuit

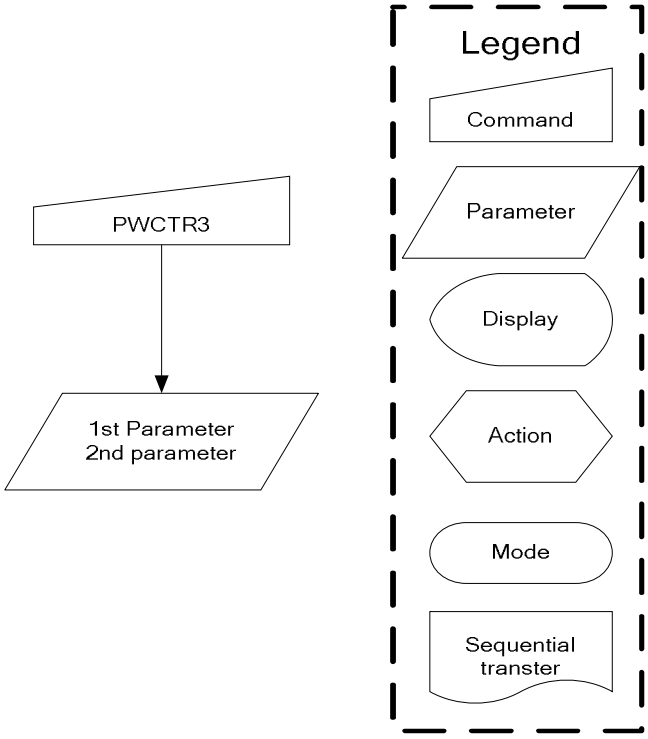
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C2h
Power On Sequence	0Ah/00h
S/W Reset	0A h/00h
H/W Reset	0A h/00h

Flow Chart



10.2.8 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

C3H	PWCTR4 (Power Control 4)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1st parameter	1	↑	1	-	DCB9	DCB8	SAPB2	SAPB1	SAPB0	APB2	APB1	APB0	
2nd parameter	1	↑	1	-	DCB7	DCB6	DCB5	DCB4	DCB3	DCB2	DCB1	DCB0	

Description

-Set the amount of current in Operational amplifier in Idle mode/8 colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

AP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

SAP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

-Set the Booster circuit Step-up cycle in Idle mode/8 colors.

	DCB[9:8]	DCB[7:6]	DCB[5:4]	DCB[3:2]	DCB[1:0]
00	BCLK/1	BCLK/3	BCLK/1	BCLK/1	BCLK/1
01	BCLK/3	BCLK/1	BCLK/3	BCLK/3	BCLK/3
10	BCLK/2	BCLK/4	BCLK/2	BCLK/2	BCLK/2
11	BCLK/4	BCLK/2	BCLK/4	BCLK/4	BCLK/4

Note: BCLK is Clock frequency for Booster circuit

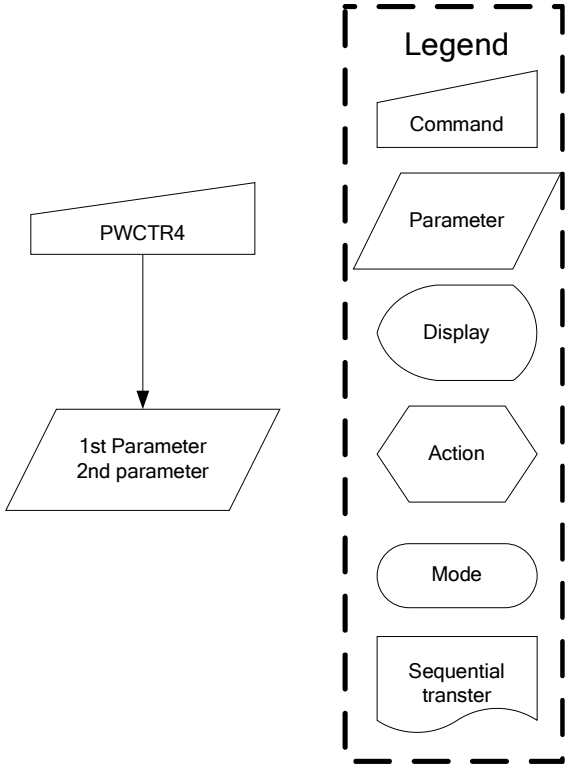
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C3h
Power On Sequence	8Ah/26h
S/W Reset	8Ah/26h
H/W Reset	8Ah/26h

Flow Chart



10.2.9 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

C4H	PWCTR5 (Power Control 5)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1st parameter	1	↑	1	-	DCC9	DCC8	SAPC2	SAPC1	SAPC0	APC2	APC1	APC0	
2nd parameter	1	↑	1	-	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0	

Description

-Set the amount of current in Operational amplifier in Partial mode/ full-colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

AP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

SAP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops
001	Small
010	Medium Low
011	Medium
100	Medium High
101	Large
110	Reserved
111	Reserved

-Set the Booster circuit Step-up cycle in Partial mode/ full-colors.

	DCC[9:8]	DCC[7:6]	DCC[5:4]	DCC[3:2]	DCC[1:0]
00	BCLK/1	BCLK/3	BCLK/1	BCLK/1	BCLK/1
01	BCLK/3	BCLK/1	BCLK/3	BCLK/3	BCLK/3
10	BCLK/2	BCLK/4	BCLK/2	BCLK/2	BCLK/2
11	BCLK/4	BCLK/2	BCLK/4	BCLK/4	BCLK/4

Note: BCLK is Clock frequency for Booster circuit

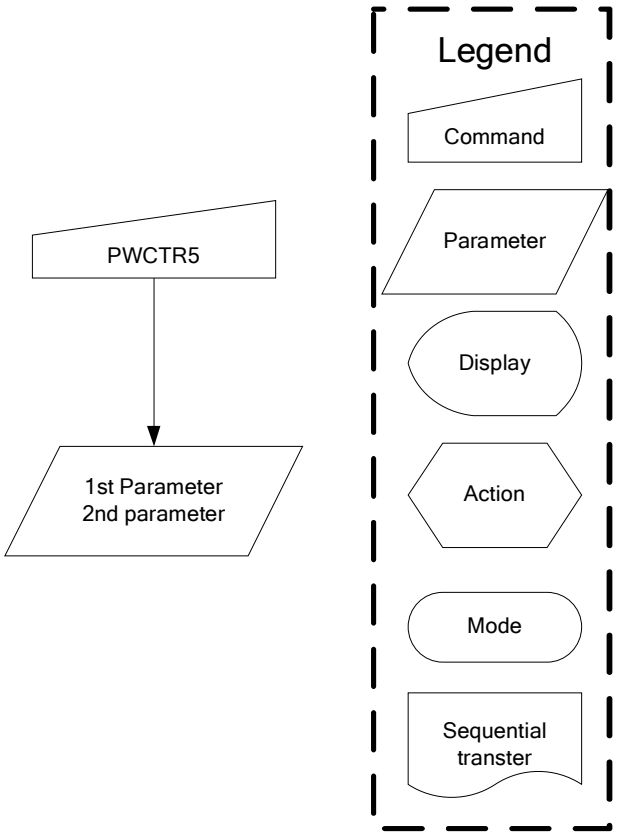
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C4h
Power On Sequence	8Ah/Eeh
S/W Reset	8Ah/Eeh
H/W Reset	8Ah/Eeh

Flow Chart



10.2.10 VMCTR1 (C5h): VCOM Control 1

C5H	VMCTR1 (VCOM Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st parameter	1	↑	1	-	-	-	VCOMS 5	VCOMS 4	VCOMS 3	VCOMS 2	VCOMS 1	VCOMS 0	

Description

VCOM voltage setting.

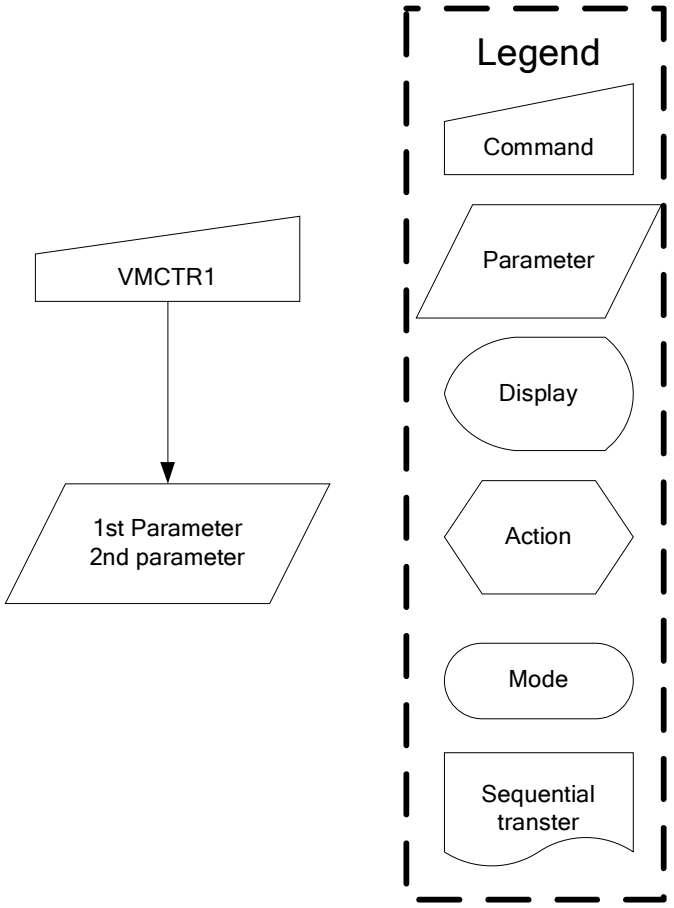
	VCOMS [5:0]	VCOM		VCOMS [5:0]	VCOM		VCOMS [5:0]	VCOM		VCOMS [5:0]	VCOM
0	000000	-0.425	16	010000	-0.825	32	100000	-1.225	48	110000	-1.625
1	000001	-0.45	17	010001	-0.85	33	100001	-1.25	49	110001	-1.65
2	000010	-0.475	18	010010	-0.875	34	100010	-1.275	50	110010	-1.675
3	000011	-0.5	19	010011	-0.9	35	100011	-1.3	51	110011	-1.7
4	000100	-0.525	20	010100	-0.925	36	100100	-1.325	52	110100	-1.725
5	000101	-0.55	21	010101	-0.95	37	100101	-1.35	53	110101	-1.75
6	000110	-0.575	22	010110	-0.975	38	100110	-1.375	54	110110	-1.775
7	000111	-0.6	23	010111	-1	39	100111	-1.4	55	110111	-1.8
8	001000	-0.625	24	011000	-1.025	40	101000	-1.425	56	111000	-1.825
9	001001	-0.65	25	011001	-1.05	41	101001	-1.45	57	111001	-1.85
10	001010	-0.675	26	011010	-1.075	42	101010	-1.475	58	111010	-1.875
11	001011	-0.7	27	011011	-1.1	43	101011	-1.5	59	111011	-1.9
12	001100	-0.725	28	011100	-1.125	44	101100	-1.525	60	111100	-1.925
13	001101	-0.75	29	011101	-1.15	45	101101	-1.55	61	111101	-1.95
14	001110	-0.775	30	011110	-1.175	46	101110	-1.575	62	111110	-1.975
15	001111	-0.8	31	011111	-1.2	47	101111	-1.6	63	111111	-2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	C5h
Power On Sequence	05h
S/W Reset	05h
H/W Reset	05h

Flow Chart	 VMCTR1 1st Parameter 2nd parameter Legend Command Parameter Display Action Mode Sequential transter

10.2.11 VMOFCTR (C7h): VCOM Offset Control

C7H	VMOFCTR (VCOM Offset Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VMOFCTR	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)
Parameter	1	↑	1	-	-	-	-	VMF4	VMF3	VMF2	VMF1	VMF0	

Description

-Set VCOM Voltage level for reduce the flicker issue
-Before use command 0xC7, the bit VMF_EN of command 0xD9 must be enabled (set to 1).

VMF[4]	VMF[3:0]	VCOM Output Level
0	0000	"VCOMS"+16d
0	0001	"VCOMS"+15d
0	|	|
0	1110	"VCOMS"+2d
0	1111	"VCOMS"+1d
1	0000	"VCOMS"
1	0001	"VCOMS"-1d
1	0010	"VCOMS"-2d
1	|	|
1	1110	"VCOMS"-14d
1	1111	"VCOMS"-15d

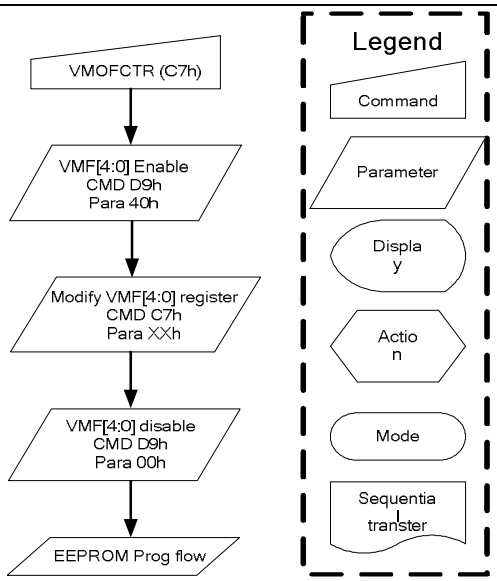
- 1d=25mV, 2d=50mV 3d=75mv….

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

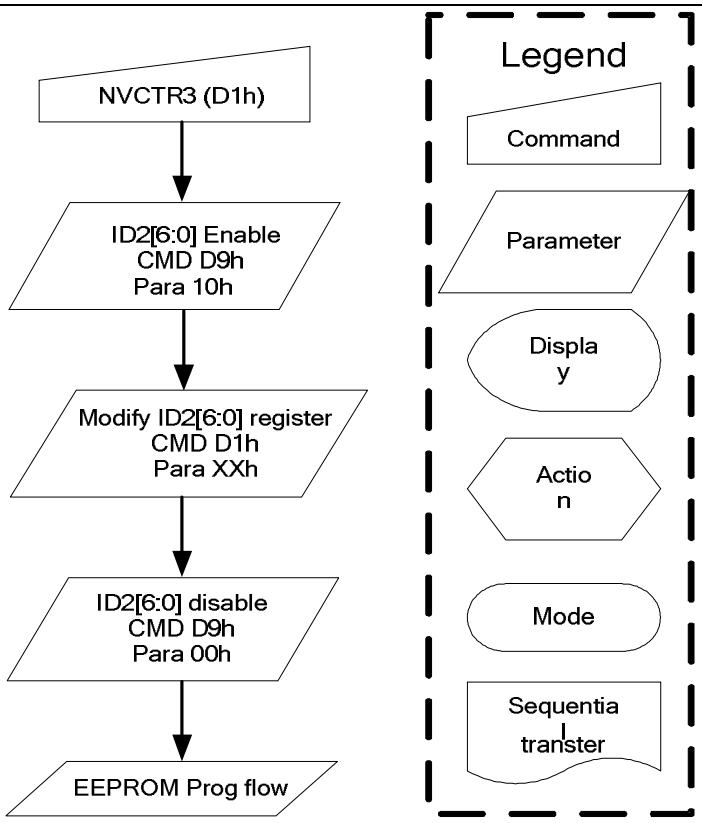
Default

Status	Default Value
	C7h
Power On Sequence	10h
S/W Reset	10h
H/W Reset	10h

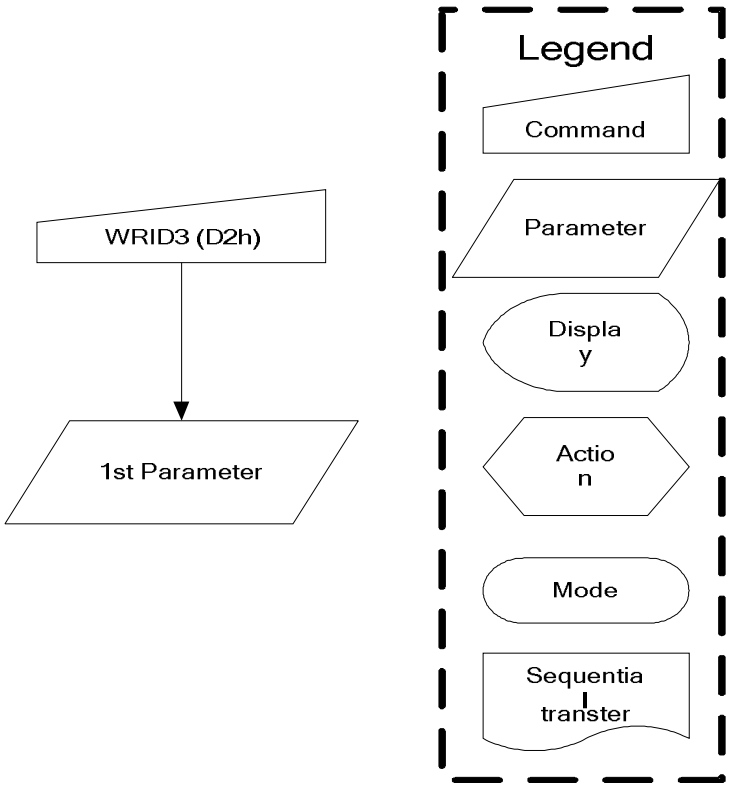
Flow Chart	

VMOFCTR (C7h)
VMF[4:0] Enable
CMD D9h
Para 40h
Modify VMF[4:0] register
CMD C7h
Para XXh
VMF[4:0] disable
CMD D9h
Para 00h
EEPROM Prog flow
Legend
Command
Parameter
Displa
y
Actio
n
Mode
Sequentia
transter

10.2.12 WRID2 (D1h): Write ID2 Value

D1H	WRID2 (Write ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
Parameter	1	↑	1	-	-	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
Description	-Write 7-bit data of LCD module version to save it to NVM. -The parameter ID2[6:0] is LCD Module version ID.												
Flow Chart													

10.2.13 WRID3 (D2h): Write ID3 Value

D2H	WRID3 (Write ID3 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRID3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
Parameter	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-
Description	-Write 8-bit data of project code module to save it to NVM. -The parameter ID3[7:0] is product project ID.												
Flow Chart													

10.2.14 NVFCTR1 (D9h): NVM Control Status

D9H	NVFCTR1 (NV Memory Function Controller 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR1	0	↑	1	-	1	1	0	0	1	0	0	1	(D9h)
Parameter	1	1	↑	-	0	VMF_EN	ID2_EN	0	0	0	0	EXT_R	

Description

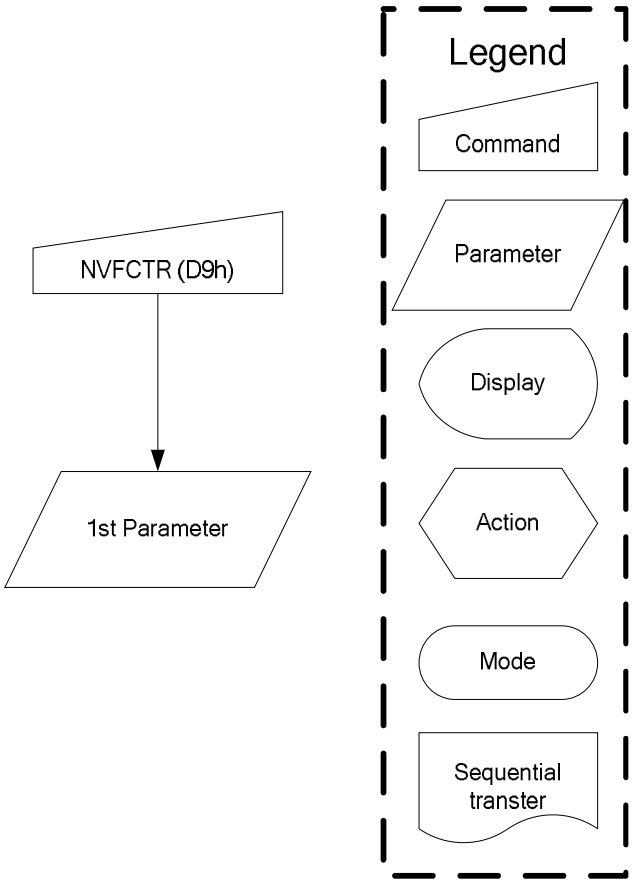
-NVM control status

Bit	Value
VMF_EN	"1" = Command C7h Enable ; "0" = Command C7h Disable
ID2_EN	"1" = Command D1h Enable ; "0" = Command D1h Disable
EXT_R	Read: Extension Command Status, "1" for Enable, "0" for Disable.

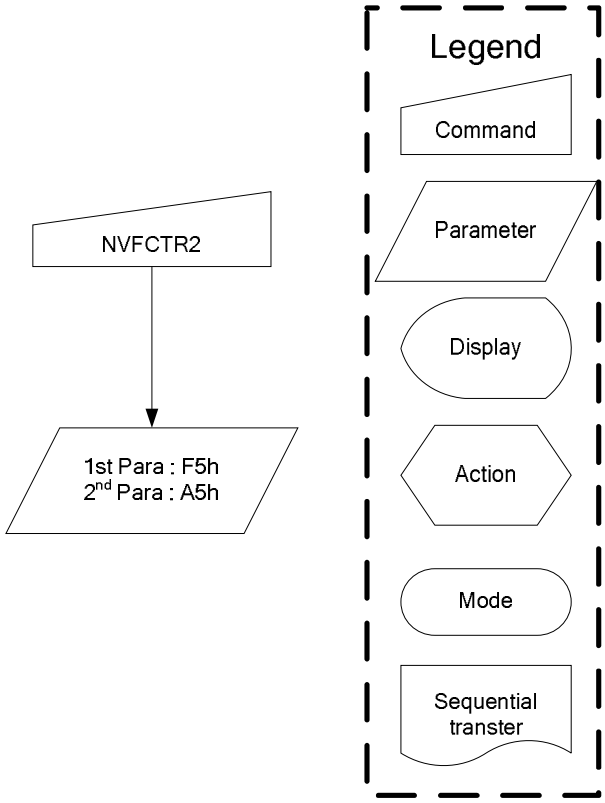
Default

Status	Default Value (D9h)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

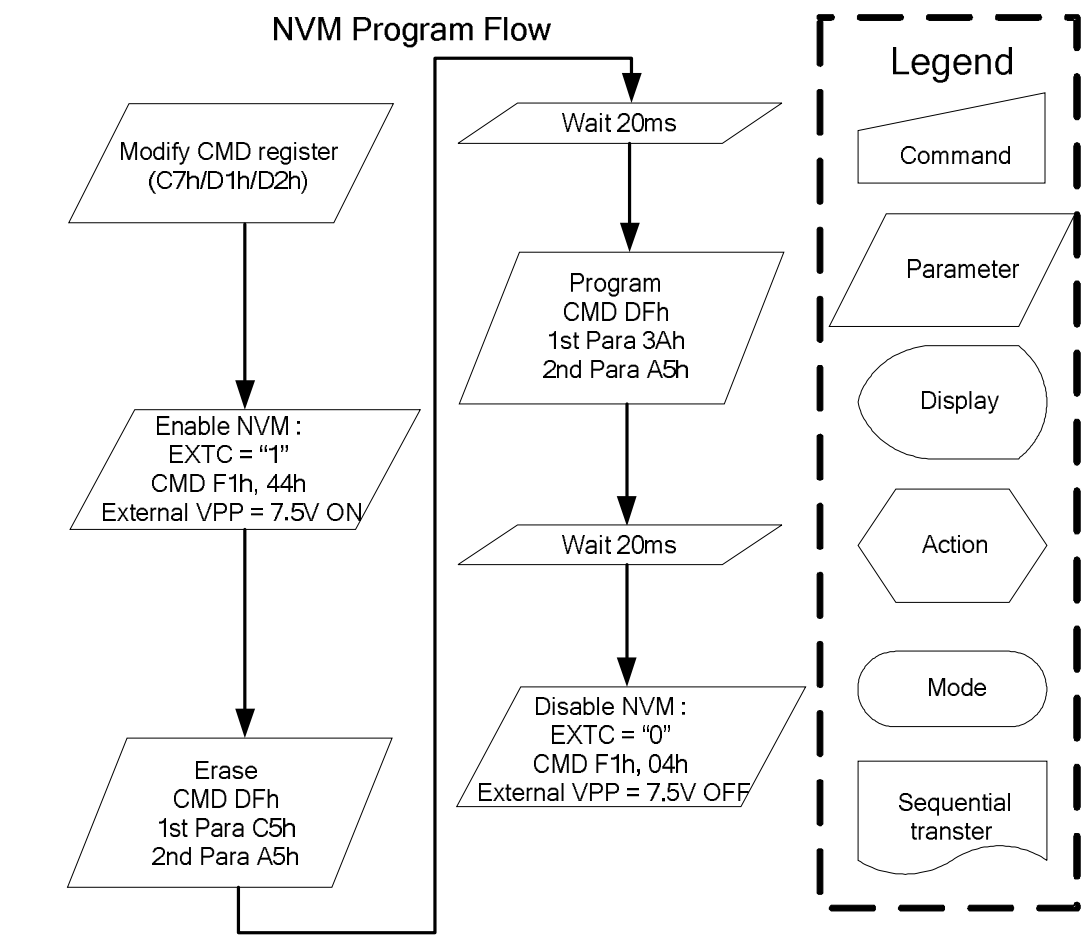
Flow Chart



10.2.15 NVFCTR2 (Deh): NVM Read Command

DEH	NVFCTR1 (NV Memory Function Controller 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR2	0	↑	1	-	1	1	0	1	1	1	1	0	(Deh)
1st Parameter	1	↑	1		1	1	1	1	0	1	0	1	F5
2nd Parameter	1	↑	1		1	0	1	0	0	1	0	1	A5
Description	NVM Read Command NOTE: "-" Don't care												
Flow Chart													

10.2.16 NVFCTR3 (DFh): NVM Write Command

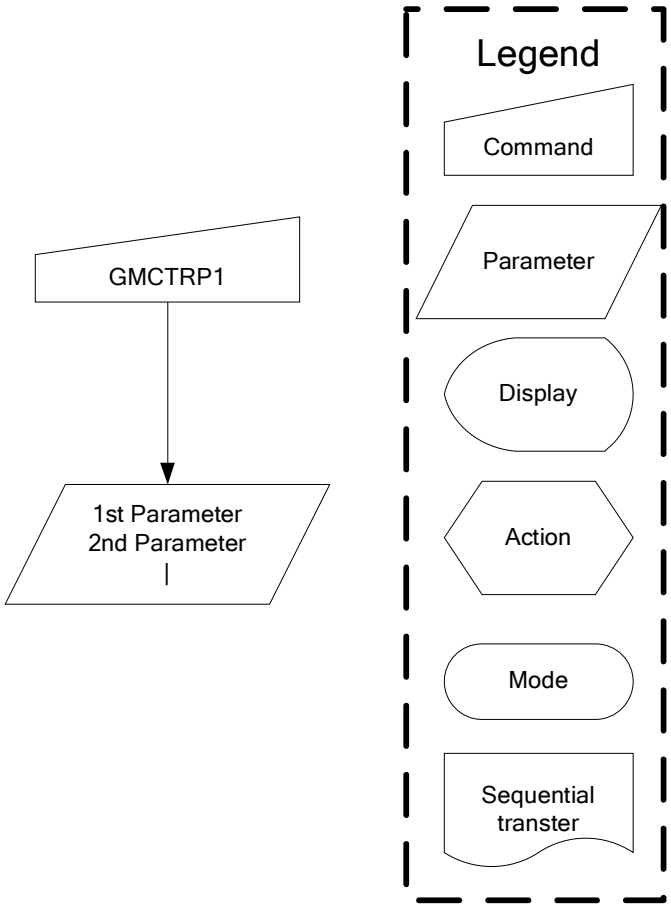
DFH	NVFCTR1 (NV Memory Function Controller 3												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR1	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)
1st Parameter	1	↑	1		NVM_CMD7	NVM_CMD6	NVM_CMD5	NVM_CMD4	NVM_CMD3	NVM_CMD2	NVM_CMD1	NVM_CMD0	
2nd Parameter	1	↑	1		1	0	1	0	0	1	0	1	A5
Description	-NVM Write Command -NVM_CMD[7:0] : Select to Program/Erase ; Program command : 3Ah ; Erase command : C5h NOTE: "-" Don't care												
Flow Chart													

10.2.17 GMCTRP1 (E0h): Gamma ('+'polarity) Correction Characteristics Setting

E0H	GMCTRP0 (Gamma '+'Polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st Parameter	1	↑	1	-	-	-	VRF0P[5]	VRF0P[4]	VF0P[3]	VRF0P[2]	VRF0P[1]	VRF0P[0]	
2nd Parameter	1	↑	1	-	-	-	VOS0P[5]	VOS0P[4]	VOS0P[3]	VOS0P[2]	VOS0P[1]	VOS0P[0]	
3rd Parameter	1	↑	1	-	-	-	PK0P[5]	PK0P[4]	PK0P[3]	PK0P[2]	PK0P[1]	PK0P[0]	
4th Parameter	1	↑	1	-	-	-	PK1P[5]	PK1P[4]	PK1P[3]	PK1P[2]	PK1P[1]	PK1P[0]	
5th Parameter	1	↑	1	-	-	-	PK2P[5]	PK2P[4]	PK2P[3]	PK2P[2]	PK2P[1]	PK2P[0]	
6th Parameter	1	↑	1	-	-	-	PK3P[5]	PK3P[4]	PK3P[3]	PK3P[2]	PK3P[1]	PK3P[0]	
7th Parameter	1	↑	1	-	-	-	PK4P[5]	PK4P[4]	PK4P[3]	PK4P[2]	PK4P[1]	PK4P[0]	
8th Parameter	1	↑	1	-	-	-	PK5P[5]	PK5P[4]	PK5P[3]	PK5P[2]	PK5P[1]	PK5P[0]	
9th Parameter	1	↑	1	-	-	-	PK6P[5]	PK6P[4]	PK6P[3]	PK6P[2]	PK6P[1]	PK6P[0]	
10th Parameter	1	↑	1	-	-	-	PK7P[5]	PK7P[4]	PK7P[3]	PK7P[2]	PK7P[1]	PK7P[0]	
11th Parameter	1	↑	1	-	-	-	PK8P[5]	PK8P[4]	PK8P[3]	PK8P[2]	PK8P[1]	PK8P[0]	
12th Parameter	1	↑	1	-	-	-	PK9P[5]	PK9P[4]	PK9P[3]	PK9P[2]	PK9P[1]	PK9P[0]	
13th Parameter	1	↑	1	-	-	-	SELV0P[5]	SELV0P[4]	SELV0P[3]	SELV0P[2]	SELV0P[1]	SELV0P[0]	
14th Parameter	1	↑	1	-	-	-	SELV1P[5]	SELV1P[4]	SELV1P[3]	SELV1P[2]	SELV1P[1]	SELV1P[0]	
15th Parameter	1	↑	1	-	-	-	SELV62P[5]	SELV62P[4]	SELV62P[3]	SELV62P[2]	SELV62P[1]	SELV62P[0]	
16th Parameter	1	↑	1	-	-	-	SELV63P[5]	SELV63P[4]	SELV63P[3]	SELV63P[2]	SELV63P[1]	SELV63P[0]	

Description

Register Group	Positive Polarity	Set-up Contents
High Level adjustment	VRF0P[5:0]	Variable resistor VRHP
Mid Level Adjustment	SELV0P[5:0]	The voltage of V0 grayscale is selected by the 64 to 1
	SELV1P[5:0]	The voltage of V1 grayscale is selected by the 64 to 1
	PK0P[5:0]	The voltage of V3 grayscale is selected by the 64 to 1
	PK1P[5:0]	The voltage of V4 grayscale is selected by the 64 to 1
	PK2P[5:0]	The voltage of V12 grayscale is selected by the 64 to 1
	PK3P[5:0]	The voltage of V20 grayscale is selected by the 64 to 1
	PK4P[5:0]	The voltage of V28 grayscale is selected by the 64 to 1
	PK5P[5:0]	The voltage of V36 grayscale is selected by the 64 to 1
	PK6P[5:0]	The voltage of V44 grayscale is selected by the 64 to 1
	PK7P[5:0]	The voltage of V52 grayscale is selected by the 64 to 1
	PK8P[5:0]	The voltage of V56 grayscale is selected by the 64 to 1
	PK9P[5:0]	The voltage of V60 grayscale is selected by the 64 to 1
	SELV62P[5:0]	The voltage of V62 grayscale is selected by the 64 to 1
	SELV63P[5:0]	The voltage of V63 grayscale is selected by the 64 to 1
Low Level Adjustment	VOS0P[5:0]	Variable Resistor VRLP

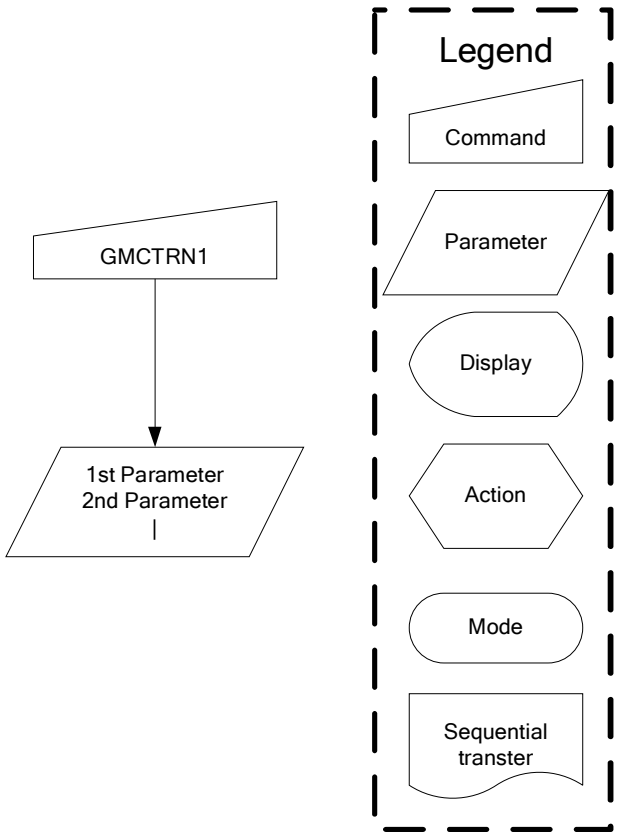
Flow Chart	 GMCTRP1 1st Parameter 2nd Parameter | Legend Command Parameter Display Action Mode Sequential transter

10.2.18 GMCTRN1 (E1h): Gamma '-'polarity Correction Characteristics Setting

E1H	GMCTRP0 (Gamma '+'Polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1st Parameter	1	↑	1	-	-	-	VRF0N[5]	VRF0N[4]	VF0N[3]	VRF0N[2]	VRF0N[1]	VRF0N[0]	
2nd Parameter	1	↑	1	-	-	-	VOS0N[5]	VOS0N[4]	VOS0N[3]	VOS0N[2]	VOS0N[1]	VOS0N[0]	
3rd Parameter	1	↑	1	-	-	-	PK0N[5]	PK0N[4]	PK0N[3]	PK0N[2]	PK0N[1]	PK0N[0]	
4th Parameter	1	↑	1	-	-	-	PK1N[5]	PK1N[4]	PK1N[3]	PK1N[2]	PK1N[1]	PK1N[0]	
5th Parameter	1	↑	1	-	-	-	PK2N[5]	PK2N[4]	PK2N[3]	PK2N[2]	PK2N[1]	PK2N[0]	
6th Parameter	1	↑	1	-	-	-	PK3N[5]	PK3N[4]	PK3N[3]	PK3N[2]	PK3N[1]	PK3N[0]	
7th Parameter	1	↑	1	-	-	-	PK4N[5]	PK4N[4]	PK4N[3]	PK4N[2]	PK4N[1]	PK4N[0]	
8th Parameter	1	↑	1	-	-	-	PK5N[5]	PK5N[4]	PK5N[3]	PK5N[2]	PK5N[1]	PK5N[0]	
9th Parameter	1	↑	1	-	-	-	PK6N[5]	PK6N[4]	PK6N[3]	PK6N[2]	PK6N[1]	PK6N[0]	
10th Parameter	1	↑	1	-	-	-	PK7N[5]	PK7N[4]	PK7N[3]	PK7N[2]	PK7N[1]	PK7N[0]	
11th Parameter	1	↑	1	-	-	-	PK8N[5]	PK8N[4]	PK8N[3]	PK8N[2]	PK8N[1]	PK8N[0]	
12th Parameter	1	↑	1	-	-	-	PK9[5]	PK9N[4]	PK9N[3]	PK9N[2]	PK9N[1]	PK9N[0]	
13th Parameter	1	↑	1	-	-	-	SELV0N[5]	SELV0N[4]	SELV0N[3]	SELV0N[2]	SELV0N[1]	SELV0N[0]	
14th Parameter	1	↑	1	-	-	-	SELV1N[5]	SELV1N[4]	SELV1N[3]	SELV1N[2]	SELV1N[1]	SELV1N[0]	
15th Parameter	1	↑	1	-	-	-	SELV62N[5]	SELV62N[4]	SELV62N[3]	SELV62N[2]	SELV62N[1]	SELV62N[0]	
16th Parameter	1	↑	1	-	-	-	SELV63N[5]	SELV63N[4]	SELV63N[3]	SELV63N[2]	SELV63N[1]	SELV63N[0]	

Description

Register Group	Negative Polarity	Set-up Contents
High level adjustment	VRF0N[5:0]	Variable resistor VRHN
Mid Level Adjustment	SELV0N[5:0]	The voltage of V0 grayscale is selected by the 64 to 1
	SELV1N[5:0]	The voltage of V1 grayscale is selected by the 64 to 1
	PK0N[5:0]	The voltage of V3 grayscale is selected by the 64 to 1
	PK1N[5:0]	The voltage of V4 grayscale is selected by the 64 to 1
	PK2N[5:0]	The voltage of V12 grayscale is selected by the 64 to 1
	PK3N[5:0]	The voltage of V20 grayscale is selected by the 64 to 1
	PK4N[5:0]	The voltage of V28 grayscale is selected by the 64 to 1
	PK5N[5:0]	The voltage of V36 grayscale is selected by the 64 to 1
	PK6N[5:0]	The voltage of V44 grayscale is selected by the 64 to 1
	PK7N[5:0]	The voltage of V52 grayscale is selected by the 64 to 1
	PK8N[5:0]	The voltage of V56 grayscale is selected by the 64 to 1
	PK9N[5:0]	The voltage of V60 grayscale is selected by the 64 to 1
	SELV62N[5:0]	The voltage of V62 grayscale is selected by the 64 to 1
	SELV63N[5:0]	The voltage of V63 grayscale is selected by the 64 to 1
Low Level Adjustment	VOS0N[5:0]	Variable Resistor VRLN

Flow Chart	

GMCTRN1
1st Parameter
2nd Parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

10.2.19 GCV(FCh): Gate Pump Clock Frequency Variable

FCH	Gate Pump Clock Frequency Variable												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR1	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)
Parameter	1	1	↑	-	GCV _Enable1	GCV _Enable0	0	0	Clk_ Variable1	Clk_ Variable0	0	0	

Description

-Automatic adjust gate pumping clock for saving power consumption.

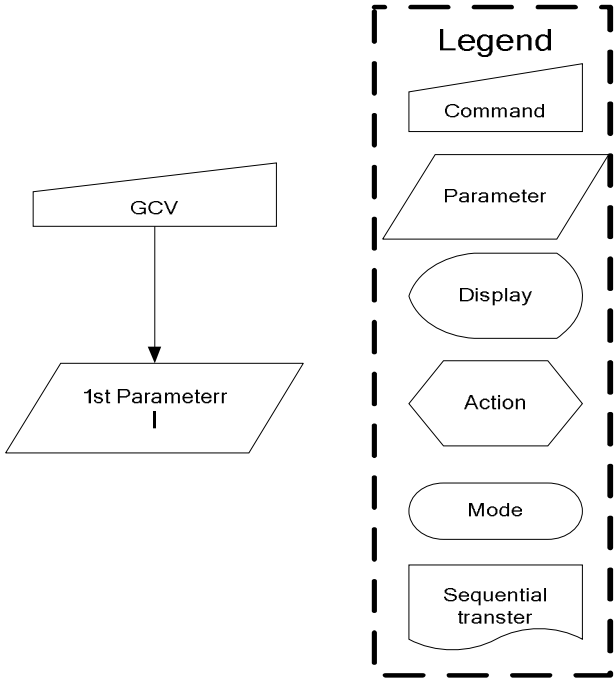
GCV_Enable[1:0]	Gate Pump Clock Frequency
00	Reserved
01	Reserved
10	Disable
11	Enable

Clk_Variable[1:0]	Save Power Ability
00	Small
01	Medium
10	High
11	Large

Default

Status	Default Value (FCh)
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

Flow Chart



11 Power Sturcture

11.1 Driver IC Operating Voltage Specification

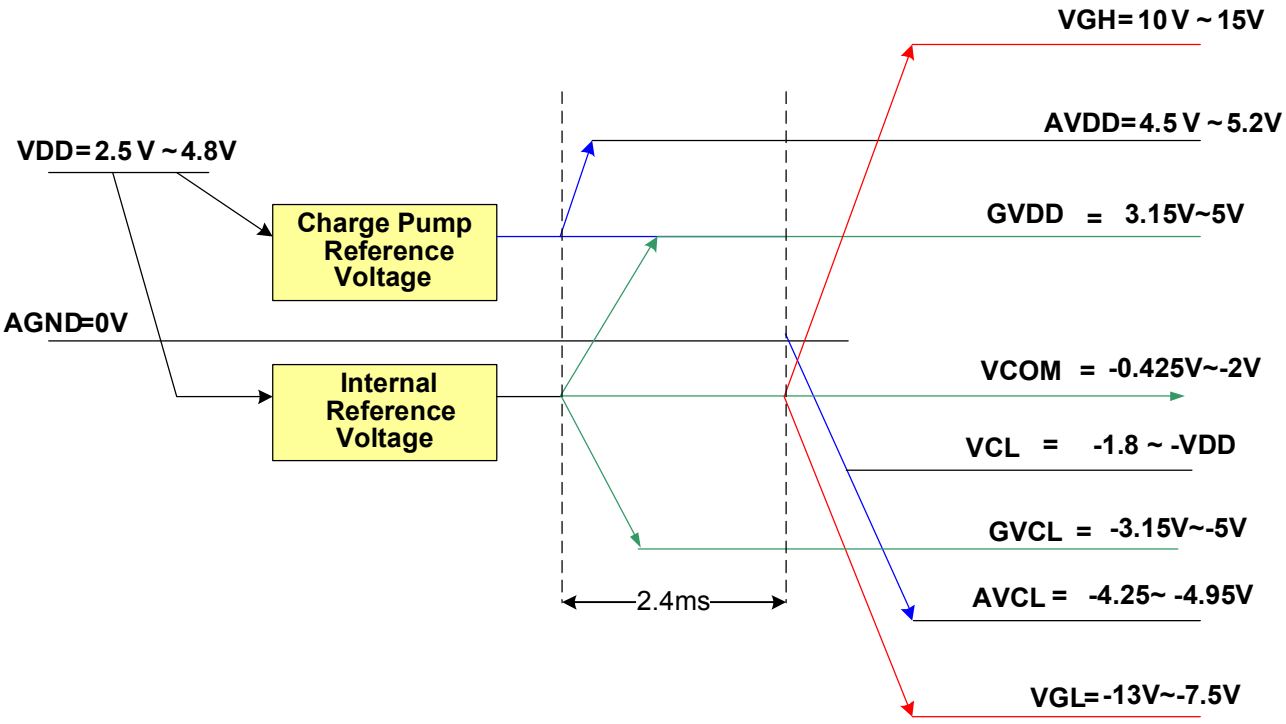


Fig 15 Power Booster Level

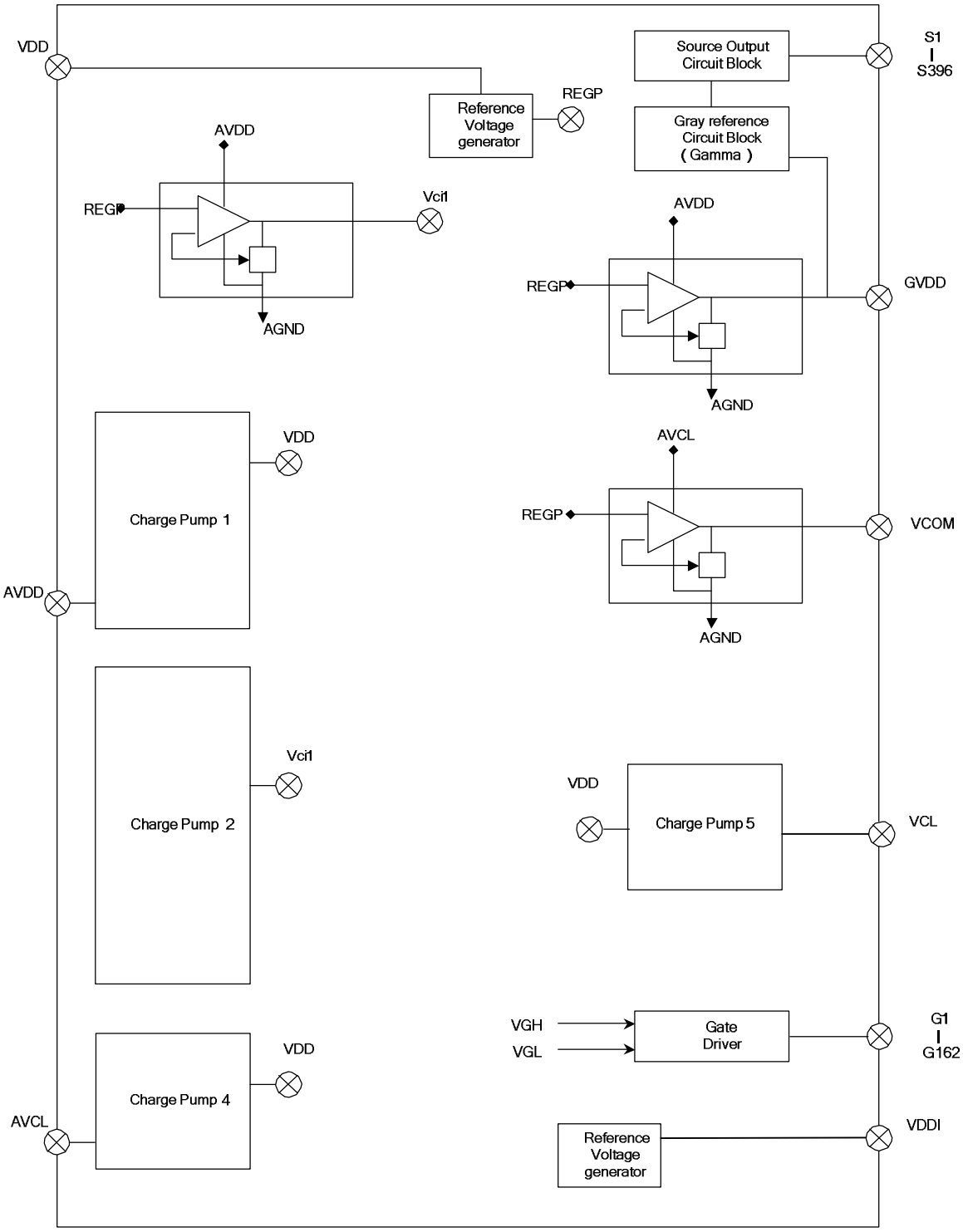
Note:

Sleep out flow: AVDD, GVDD, GVCL, VCOM switch on -> 2.4ms -> AVCL, VGH, VGL, VCL switch on -> 78.6ms

scan 2 blank frames

Sleep in flow: Scan 2 blank frames -> All analog power

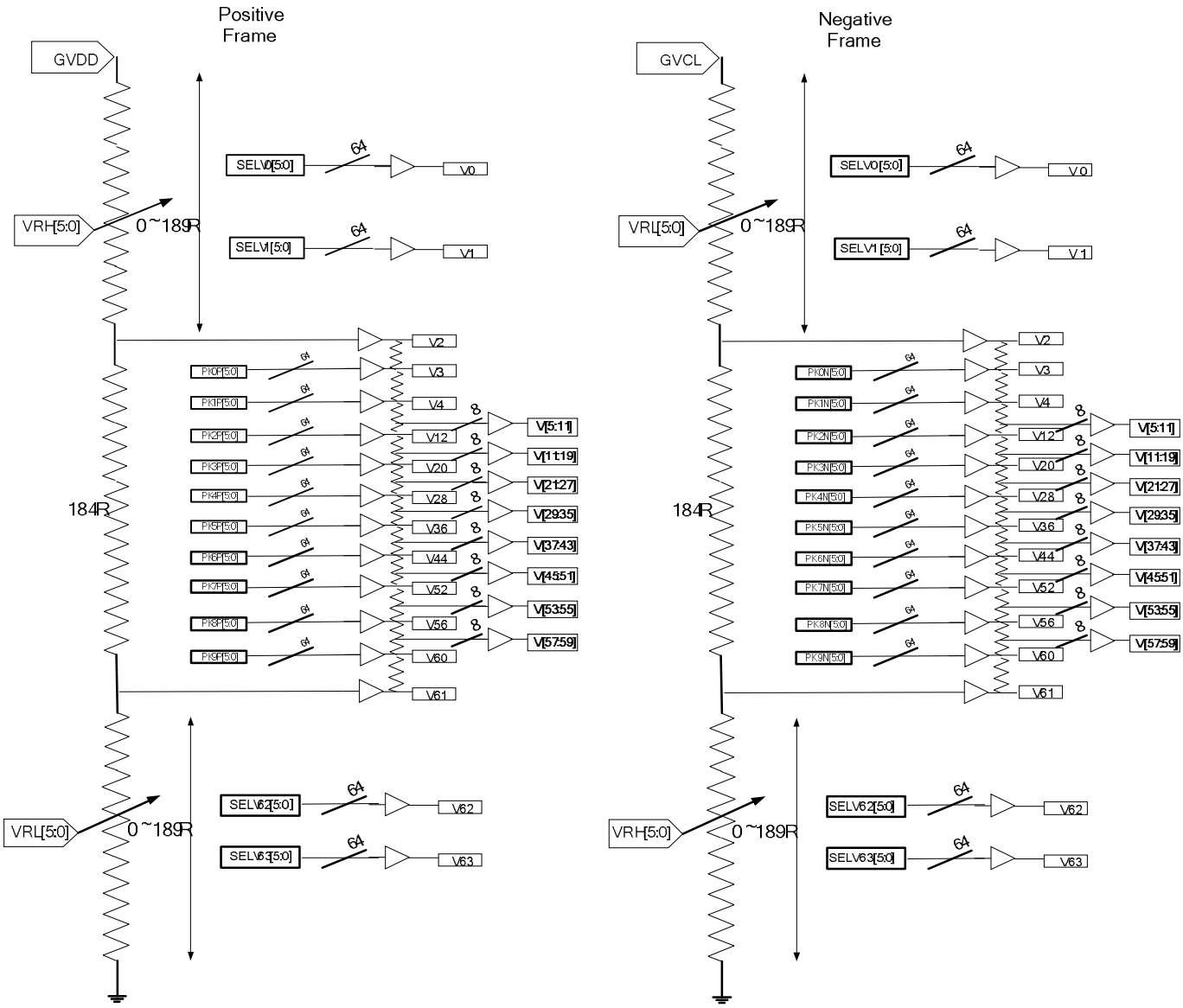
11.2 Power Booster Circuit



12 Gamma Structure

12.1 Structure of Grayscale Amplifier

16 voltage levels (VIN0-VIN15) between GVDD(GVCL) and VSS are determined by the high/ mid/ low level adjustment registers. Each mid-adjustment level is split into 64 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63 and outputs one of 64 levels.



12.2 Gamma Voltage Formula (Positive/ Negative Polarity)

Gray Level	Voltage Formula (Positive)	Voltage Formula (Negative)
0	VINP0	VINP0
1	VINP1	VINP1
2	VINP2	VINP2
3	VINP3	VINP3
4	VINP4	VINP4
5	V4-(V4-V12)*(4/32)	V4-(V4-V12)*(4/32)
6	V4-(V4-V12)*(8/32)	V4-(V4-V12)*(8/32)
7	V4-(V4-V12)*(12/32)	V4-(V4-V12)*(12/32)
8	V4-(V4-V12)*(16/32)	V4-(V4-V12)*(16/32)
9	V4-(V4-V12)*(20/32)	V4-(V4-V12)*(20/32)
10	V4-(V4-V12)*(24/32)	V4-(V4-V12)*(24/32)
11	V4-(V4-V12)*(28/32)	V4-(V4-V12)*(28/32)
12	VINP5	VINP5
13	V12-(V12-V20)*(4/32)	V12-(V12-V20)*(4/32)
14	V12-(V12-V20)*(8/32)	V12-(V12-V20)*(8/32)
15	V12-(V12-V20)*(12/32)	V12-(V12-V20)*(12/32)
16	V12-(V12-V20)*(16/32)	V12-(V12-V20)*(16/32)
17	V12-(V12-V20)*(20/32)	V12-(V12-V20)*(20/32)
18	V12-(V12-V20)*(24/32)	V12-(V12-V20)*(24/32)
19	V12-(V12-V20)*(28/32)	V12-(V12-V20)*(28/32)
20	VINP6	VINP6
21	V20-(V20-V28)*(4/32)	V20-(V20-V28)*(4/32)
22	V20-(V20-V28)*(8/32)	V20-(V20-V28)*(8/32)
23	V20-(V20-V28)*(12/32)	V20-(V20-V28)*(12/32)
24	V20-(V20-V28)*(16/32)	V20-(V20-V28)*(16/32)
25	V20-(V20-V28)*(20/32)	V20-(V20-V28)*(20/32)
26	V20-(V20-V28)*(24/32)	V20-(V20-V28)*(24/32)
27	V20-(V20-V28)*(28/32)	V20-(V20-V28)*(28/32)
28	VINP7	VINP7
29	V28-(V28-V36)* (4/32)	V28-(V28-V36)* (4/32)
30	V28-(V28-V36)* (8/32)	V28-(V28-V36)* (8/32)
31	V28-(V28-V36)* (12/32)	V28-(V28-V36)* (12/32)
32	V28-(V28-V36)* (16/32)	V28-(V28-V36)* (16/32)
33	V28-(V28-V36)* (20/32)	V28-(V28-V36)* (20/32)
34	V28-(V28-V36)* (24/32)	V28-(V28-V36)* (24/32)
35	V28-(V28-V36)* (28/32)	V28-(V28-V36)* (28/32)

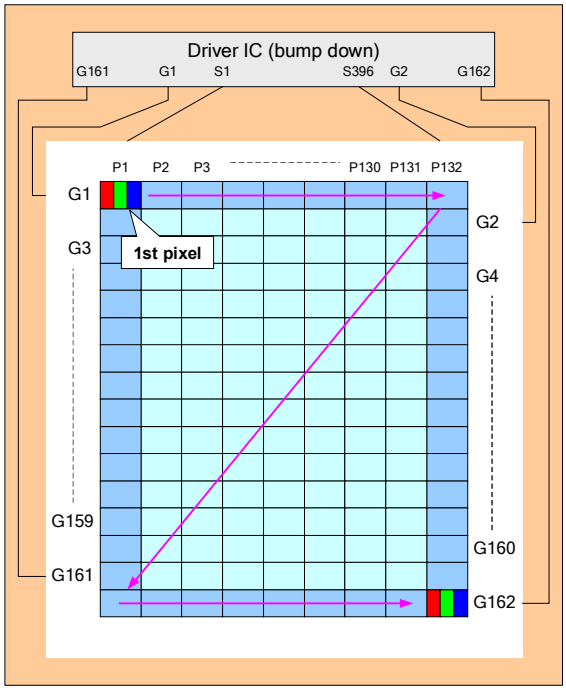
36	VINP8	VINP8
37	V36-(V36-V44)*(4/32)	V36-(V36-V44)*(4/32)
38	V36-(V36-V44)*(8/32)	V36-(V36-V44)*(8/32)
39	V36-(V36-V44)*(12/32)	V36-(V36-V44)*(12/32)
40	V36-(V36-V44)*(16/32)	V36-(V36-V44)*(16/32)
41	V36-(V36-V44)*(20/32)	V36-(V36-V44)*(20/32)
42	V36-(V36-V44)*(24/32)	V36-(V36-V44)*(24/32)
43	V36-(V36-V44)*(28/32)	V36-(V36-V44)*(28/32)
44	VINP9	VINP9
45	V44-(V44-V52)*(4/32)	V44-(V44-V52)*(4/32)
46	V44-(V44-V52)*(8/32)	V44-(V44-V52)*(8/32)
47	V44-(V44-V52)*(12/32)	V44-(V44-V52)*(12/32)
48	V44-(V44-V52)*(16/32)	V44-(V44-V52)*(16/32)
49	V44-(V44-V52)*(20/32)	V44-(V44-V52)*(20/32)
50	V44-(V44-V52)*(24/32)	V44-(V44-V52)*(24/32)
51	V44-(V44-V52)*(28/32)	V44-(V44-V52)*(28/32)
52	VINP10	VINP10
53	V52-(V52-V56)*(1/4)	V52-(V52-V56)*(1/4)
54	V52-(V52-V56)*(2/4)	V52-(V52-V56)*(2/4)
55	V52-(V52-V56)*(3/4)	V52-(V52-V56)*(3/4)
56	VINP11	VINP11
57	V56-(V56-V60)*(1/4)	V56-(V56-V60)*(1/4)
58	V56-(V56-V60)*(2/4)	V56-(V56-V60)*(2/4)
59	V56-(V56-V60)*(3/4)	V56-(V56-V60)*(3/4)
60	VINP12	VINP12
61	VINP13	VINP13
62	VINP14	VINP14
63	VINP15	VINP15

13 Example Connection with Panel Direction and Different Resolution

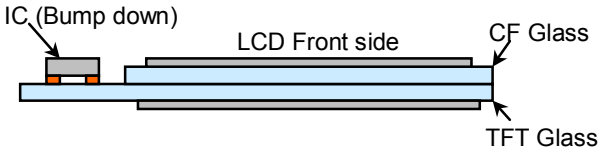
13.1 Application of Connection with Panel Direction

Case 1: (This is default case)

- 1st Pixel is at Left Top of the panel
- RGB Filter Order = RGB

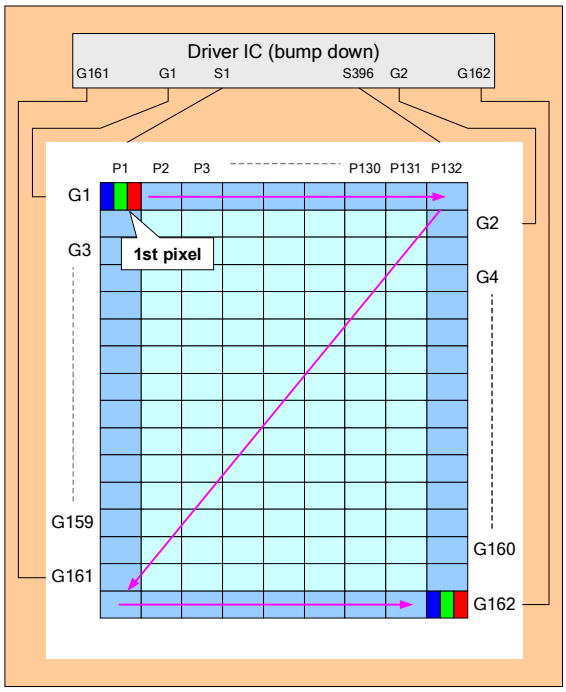


- Direction default setting (H/W)
SMX = '0'
SMY = '0'
SRGB = '0'
S1 = Filter R
S2 = Filter G
S3 = Filter B
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

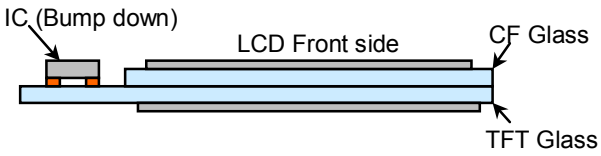


Case 2:

- 1st Pixel is at Left Top of the panel
- RGB Filter Order = BGR



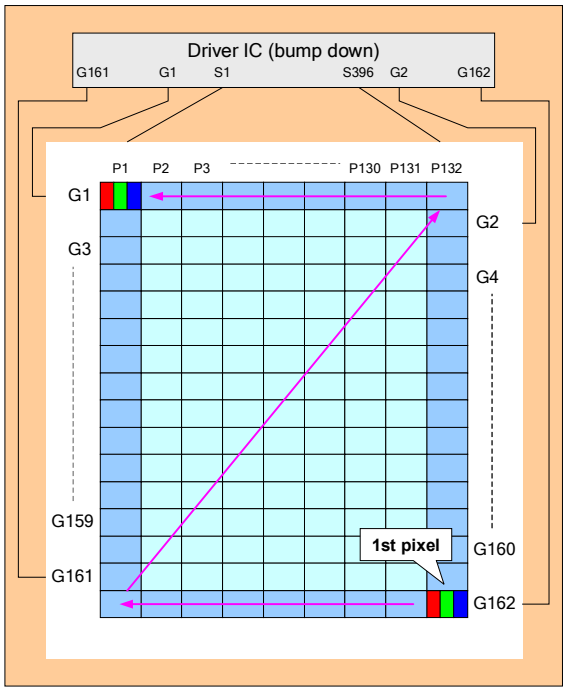
- Direction default setting (H/W)
SMX = '0'
SMY = '0'
SRGB = '1'
S1 = Filter B
S2 = Filter G
S3 = Filter R
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV



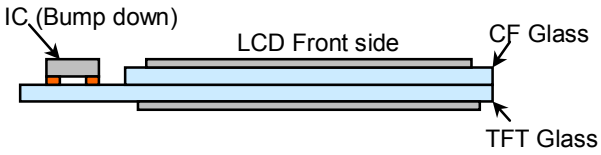
Case 3:

- 1st Pixel is at Right Bottom of the panel

- RGB Filter Order = RGB



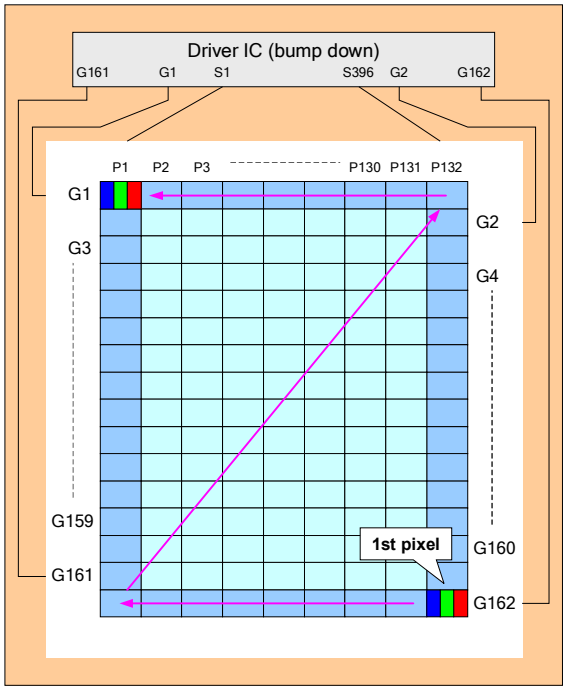
- Direction default setting (H/W)
SMX = '1'
SMY = '1'
SRGB = '0'
S1 = Filter R
S2 = Filter G
S3 = Filter B
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV



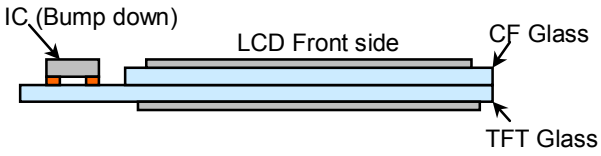
Case 4:

- 1st Pixel is at Right Bottom of the panel

- RGB Filter Order = BGR



- Direction default setting (H/W)
SMX = '1'
SMY = '1'
SRGB = '1'
S1 = Filter B
S2 = Filter G
S3 = Filter R
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV



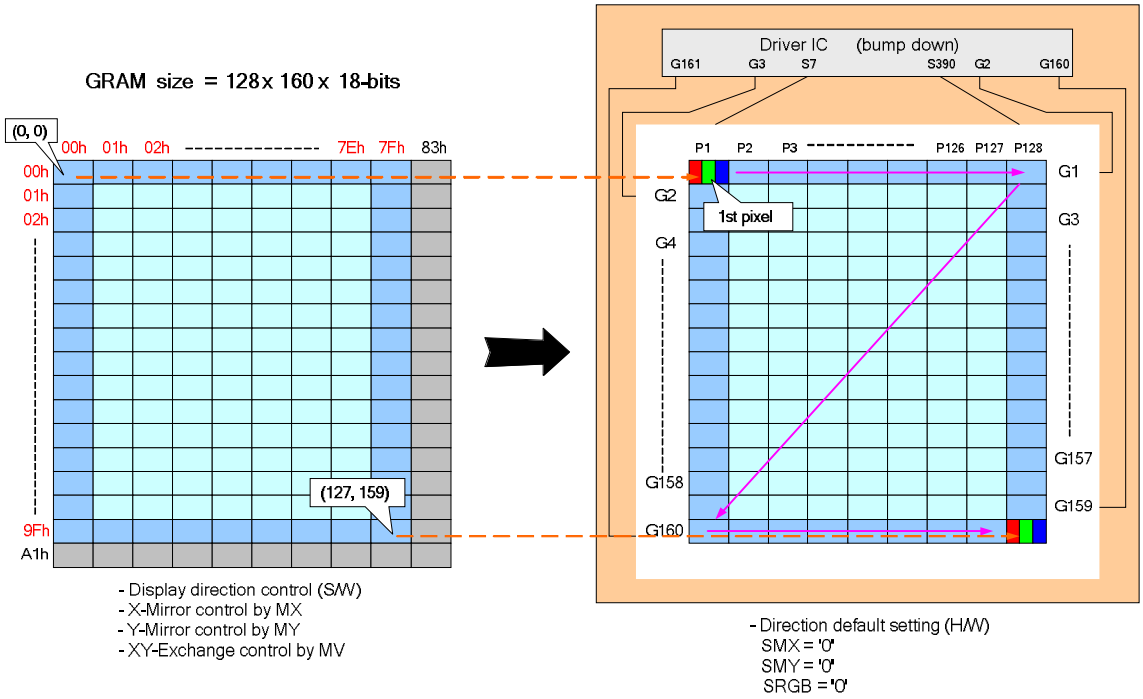
13.2 Application of Connection with Different Resolution

Case1 of Resolution (128RGB x 160) (GM[1:0] = “11”)

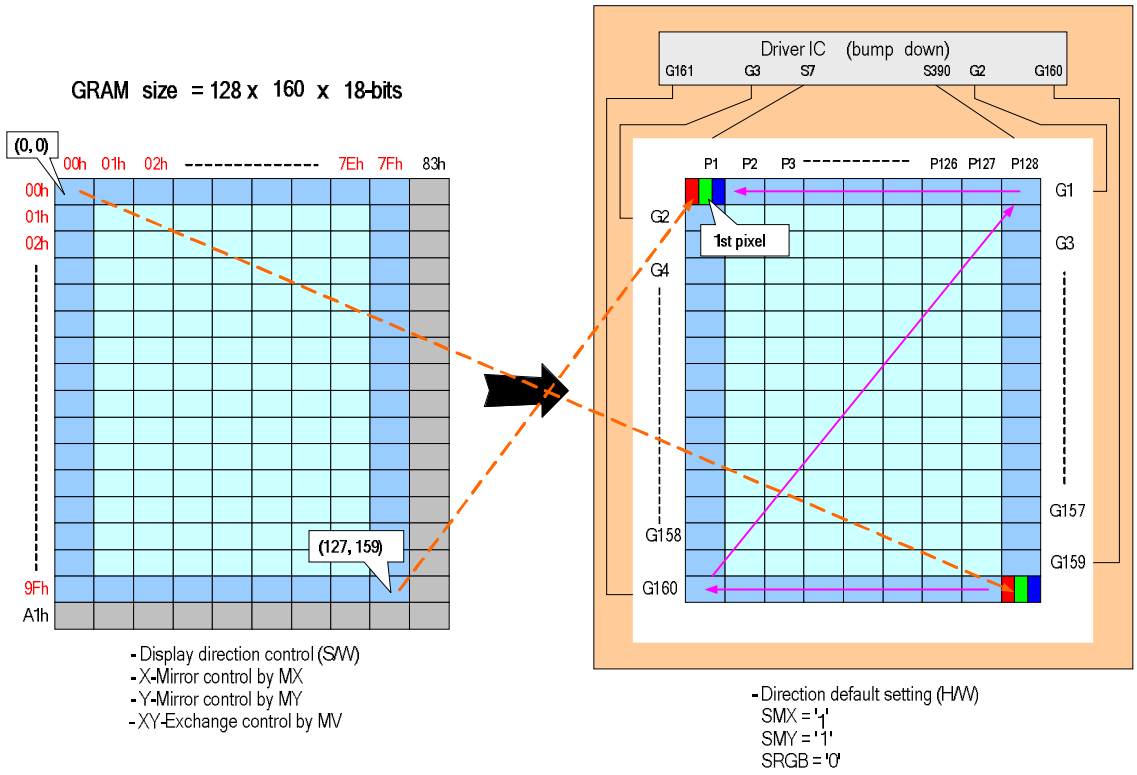
RAM Size=128 x 160 x 18-bit (Used)

Display Size = 128RGB x 160

1). Example for SMX=SMY=’0’



2). Example for SMX=SMY=’1’

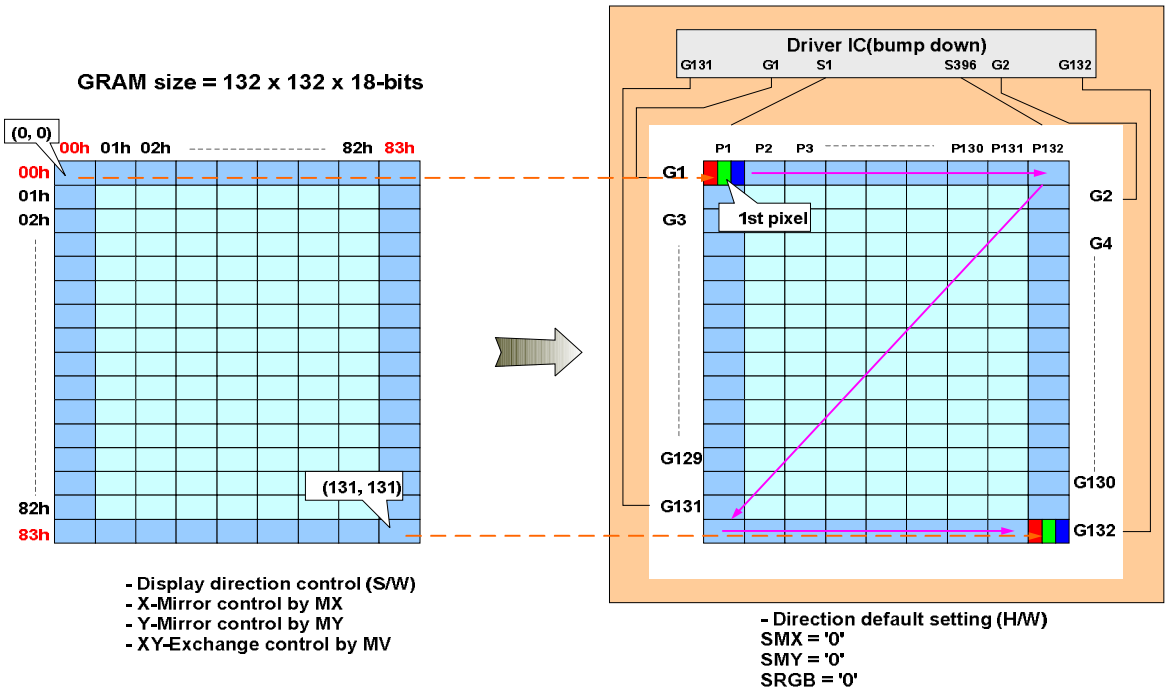


Case2 of Resolution (132RGB x 132) (GM[1:0] = “01”)

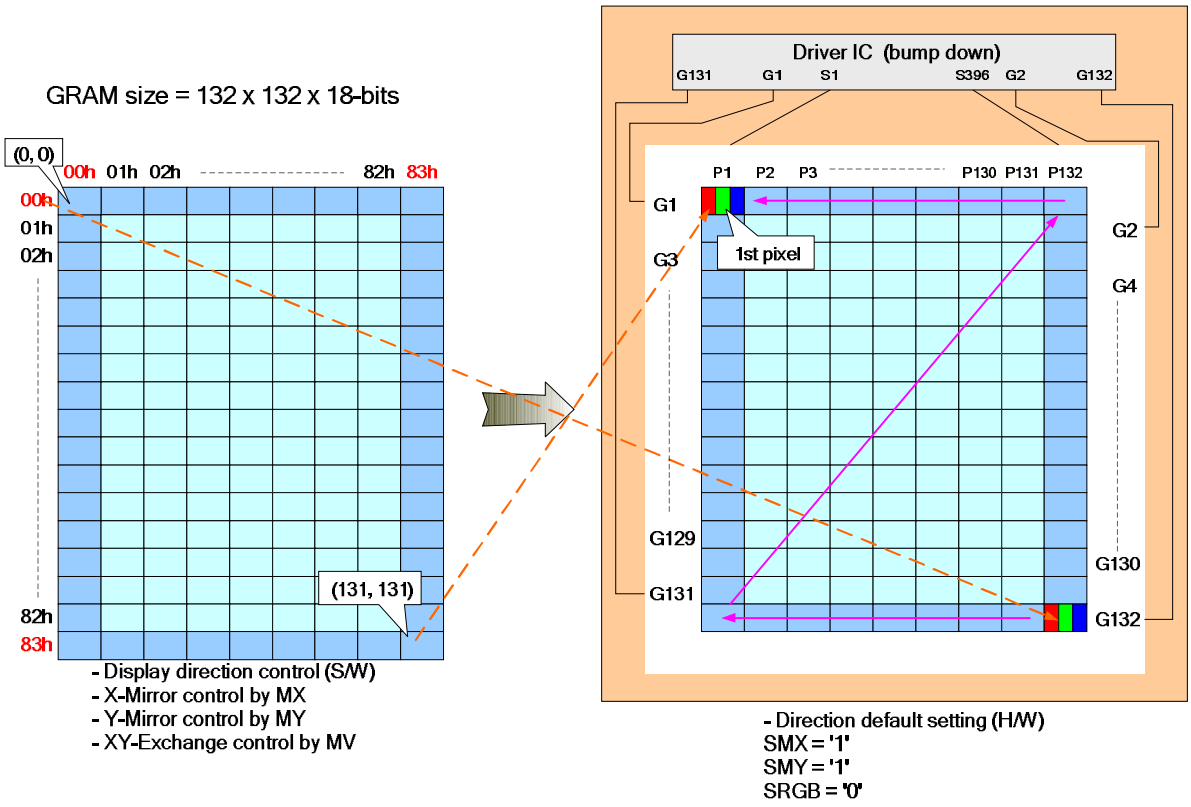
RAM size=132 x 132 x 18-bit (Used)

Display size = 132RGB x 132

1). Example for SMX=SMY=’0’



2). Example for SMX=SMY=’1’

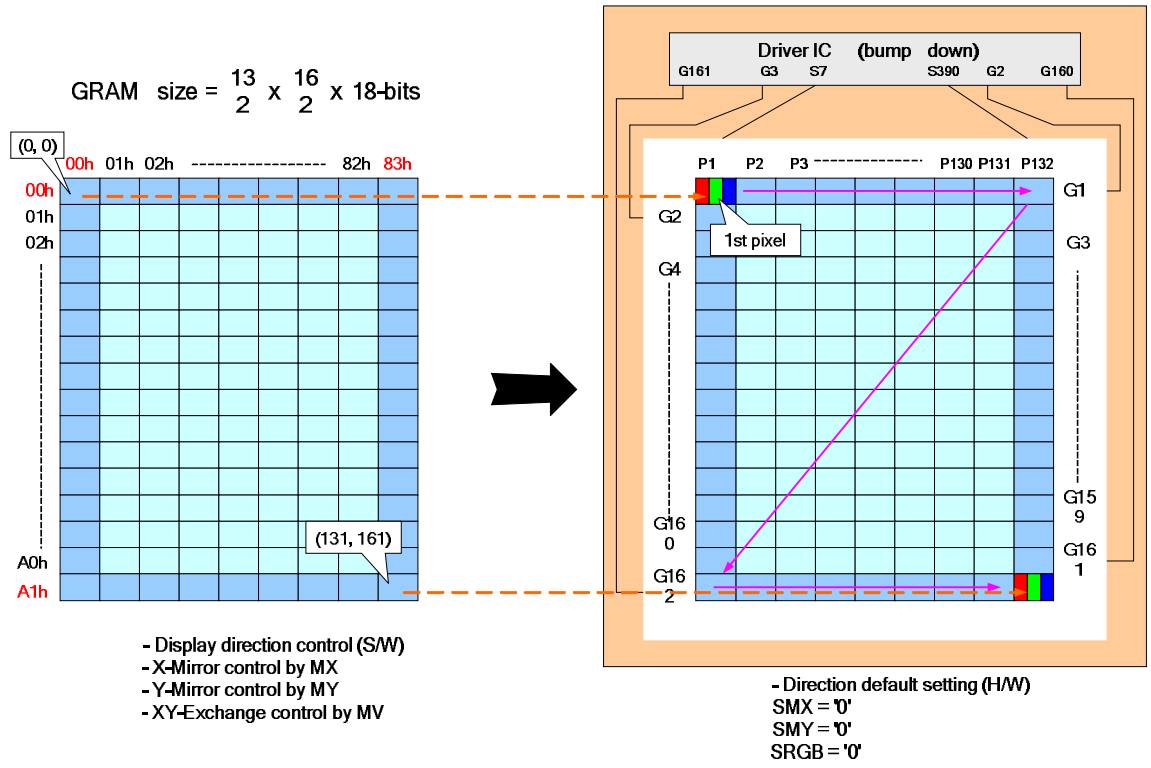


Case3 of Resolution (132RGB x 162) (GM[1:0] = “00”)

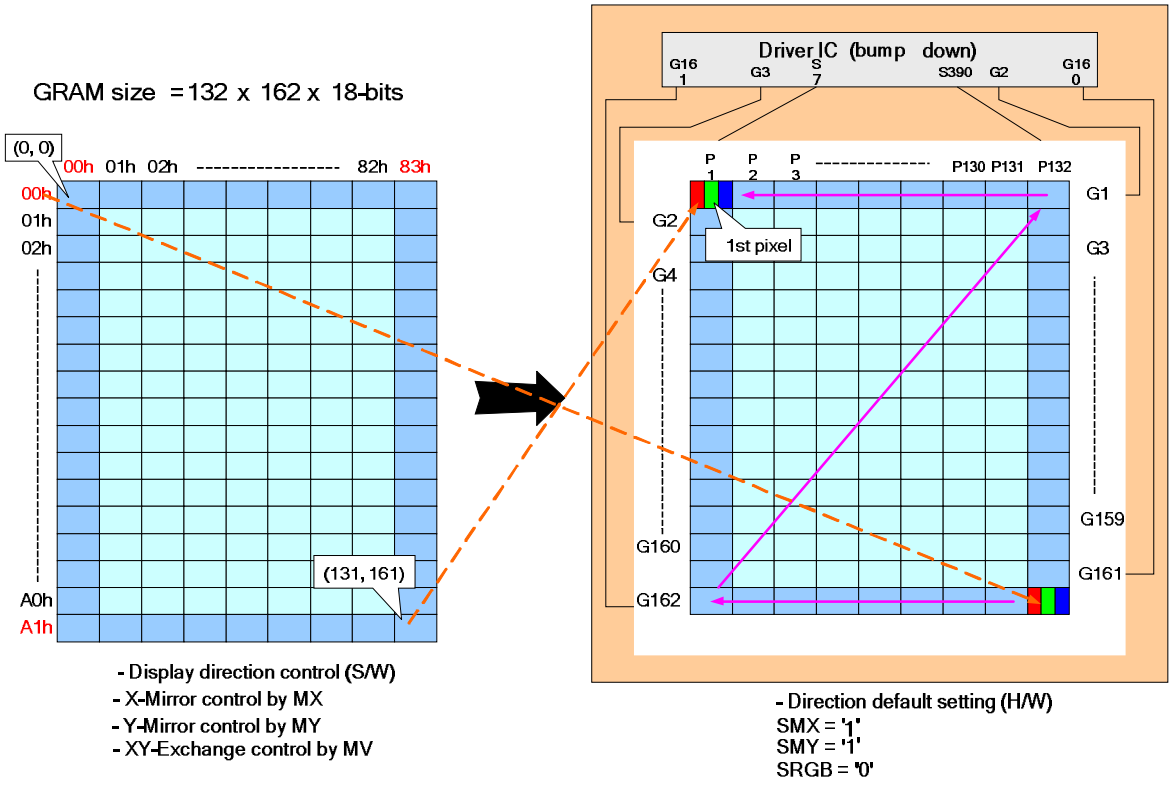
RAM Size=132 x 162 x 18-bit (Used)

Display Size = 132RGB x 162

1). Example for SMX=SMY=’0’

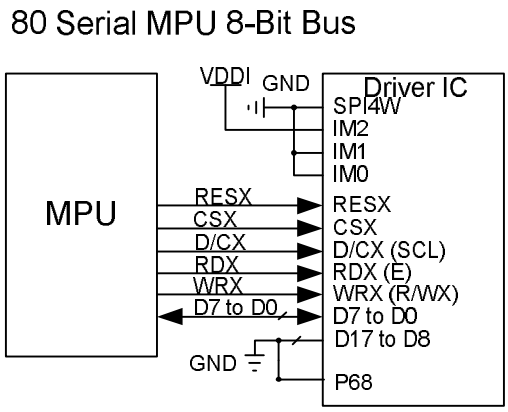


2). Example for SMX=SMY=’1’

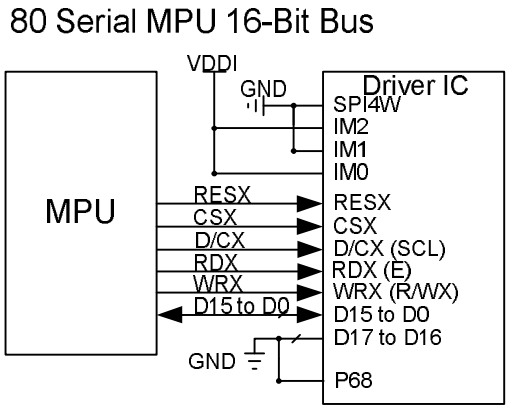


13.3 Microprocessor Interface Applications

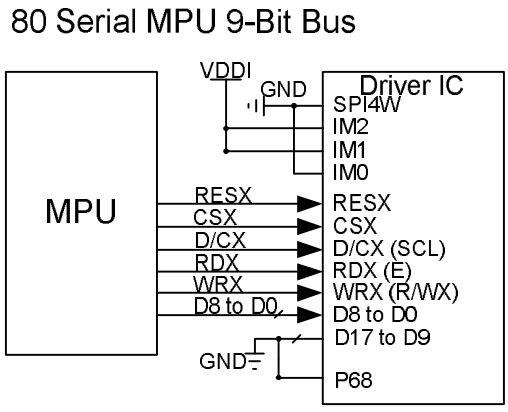
13.3.1 8080-Series MCU Interface for 8-bit Data Bus (P68=0, IM2, IM1, IM0="100")



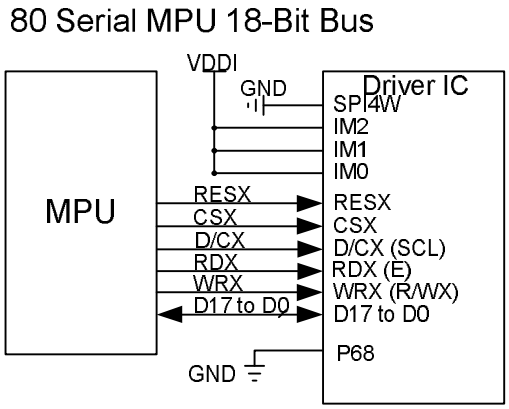
13.3.2 8080-Series MCU Interface for 16-bit Data Bus (P68=0, IM2, IM1, IM0="101")



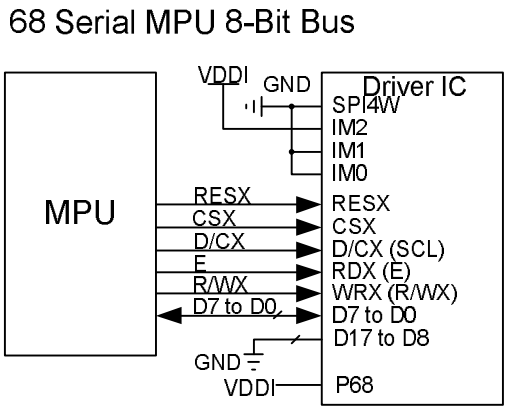
13.3.3 8080-Series MCU Interface for 9-bit Data Bus (P68=0, IM2, IM1, IM0="110")



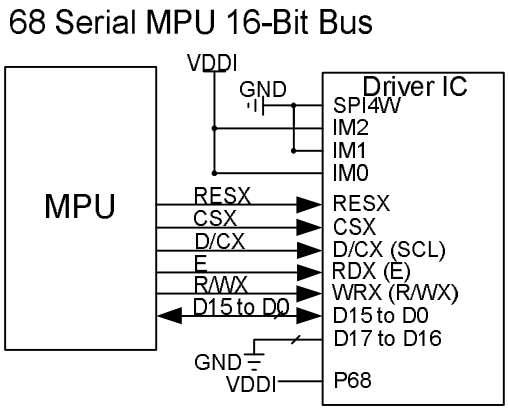
13.3.4 8080-Series MCU Interface for 18-bit Data Bus (P68=0, IM2, IM1, IM0="111")



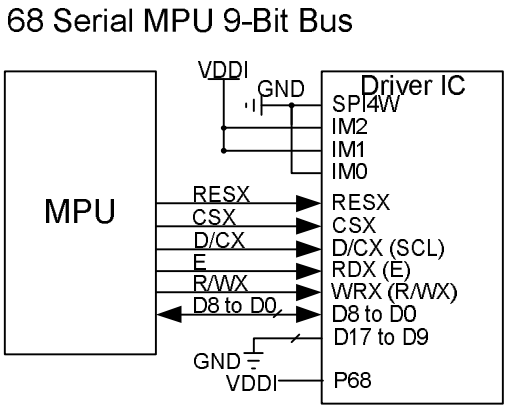
13.3.5 6800-Series MCU Interface for 8-bit Data Bus (P68=1, IM2, IM1, IM0="100")



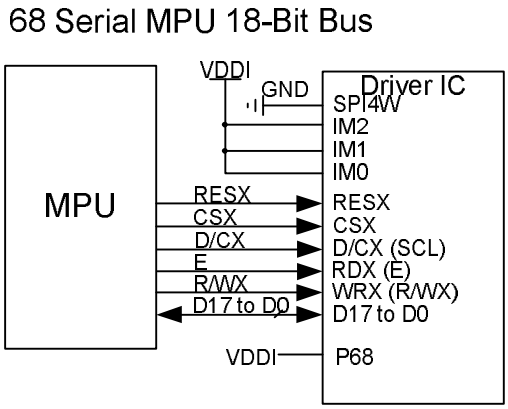
13.3.6 6800-Series MCU Interface for 16-bit Data Bus (P68=1, IM2, IM1, IM0="101")



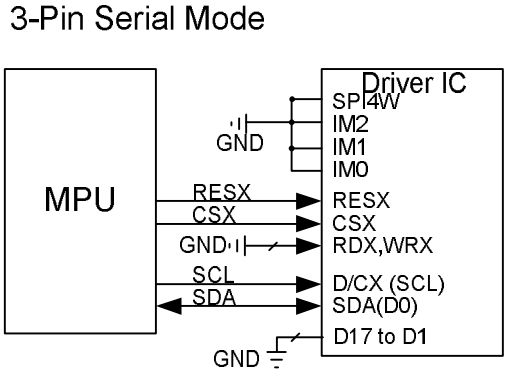
13.3.7 6800-Series MCU Interface for 9-bit Data Bus (P68=1, IM2, IM1, IM0="110")



13.3.8 6800-Series MCU Interface for 18-bit Data Bus (P68=1, IM2, IM1, IM0="111")

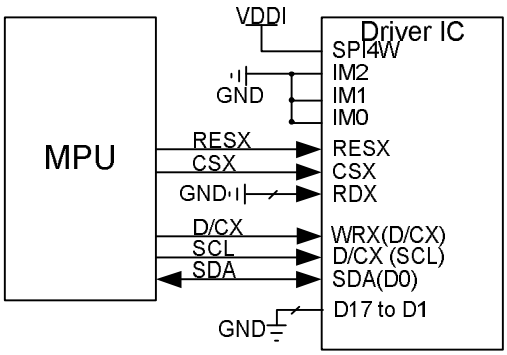


13.3..9 3-Line Serial MCU Interface (IM2, IM1, IM0="000", SPI4W=0)



13.3.10 4-Line Serial MCU Interface (IM2, IM1, IM0="000", SPI4W=1)

4-Pin Serial Mode



14 Revision History

ST7735S Specification Revision History		
Version	**Date**	**Description**
1.0	2011/06/10	First issue.
1.1	2011/11/21	Modify ID1 Value.
1.2	2011/11/26	Modify Cmd 0xFC
1.3	2012/06/20	Add 9um for Bump Height
1.4	2014/10/27	Add 250um for Chip Thickness
1.5	2015/03/03	Modify Cmd 0xFC