Table 69-5. Summary of Buffer Requirement

#		H.264	VC-1	AVS/RV	MPEG-4	MPEG-2
1	Frame buffer	7 frame (4242.5Kbyte)	6 frame (3.645 Kbyte)	6 frame (3.645 Kbyte)	4 frame (3430 Kbyte)	4 frame (2430 Kbyte)
2	Direct motion vector	708.75K byte	25.4Kbyte	25.4Kbyte	25.4Kbyte	
3	Overlap filter		7.1Kbyte			
4	De-blocking filter	11.25Kbyte	22.5Kbyte	11.25Kbyte		
5	Intra Prediction(AC-DC)	4.22Kbyte	5.625Kbyte	4.22Kbyte	5.625Kbyte	
6	MVP/MB information	5.625Kbyte	2.11Kbyte	2.11Kbyte	2.11Kbyte	
7	Slice information	131Kbyte				
8	Bit plane		3Kbyte			
9	Data-partioning					
	Total	5M byte	3.6M byte	3.6M byte	2.48M byte	2.38M byte

69.8 VPU Memory Map/Register Definition

VPU registers are all 32-bit wide, support only 32bit aligned read/write operation. VPU registers are grouped into several regions corresponding to different decoding process step. They are used for decoding process configuration and control. They can only be accessed through IP bus interface.

Please note that there are some undefined address space in VPU memory map, any read/write accessing to this register address space is ignored in the VPU. Read accessing to write only register returns ZERO value. Write accessing to read only register is ignored.

The BIT processor registers' memory map in VPU is 0xBASE_0000~0xBASE_01FC. The BIT processor registers are divided into 2 categories.

- Address 0xBASE_0000~0xBASE_00FC (64 registers address space) are hardware registers. These registers have reset values and their functions are fixed (not configurable).
- Address 0xBASE_0100~0xBASE_01FC (64 registers address space) are software registers. They have no reset values and can be configured by internal BIT processor. Their definitions may change for different firmware version, so they are not provided here. This type of registers can be used as general parameter registers between host processor and BIT processor.

- The first 32 parameter registers (address 0xBASE_0100~0xBASE_017C) are used as static parameters. Definition and functions of those registers are same for all kinds of run commands.
- The second 32 parameter registers (address 0xBASE_0180~0xBASE_01FC) are used as temporal parameters. The definition and functions of those registers may differ in different run commands.

The memory map for the hardware registers of VPU is shown in the table below.

Please refer to the VPU API document for descriptions on software registers access.

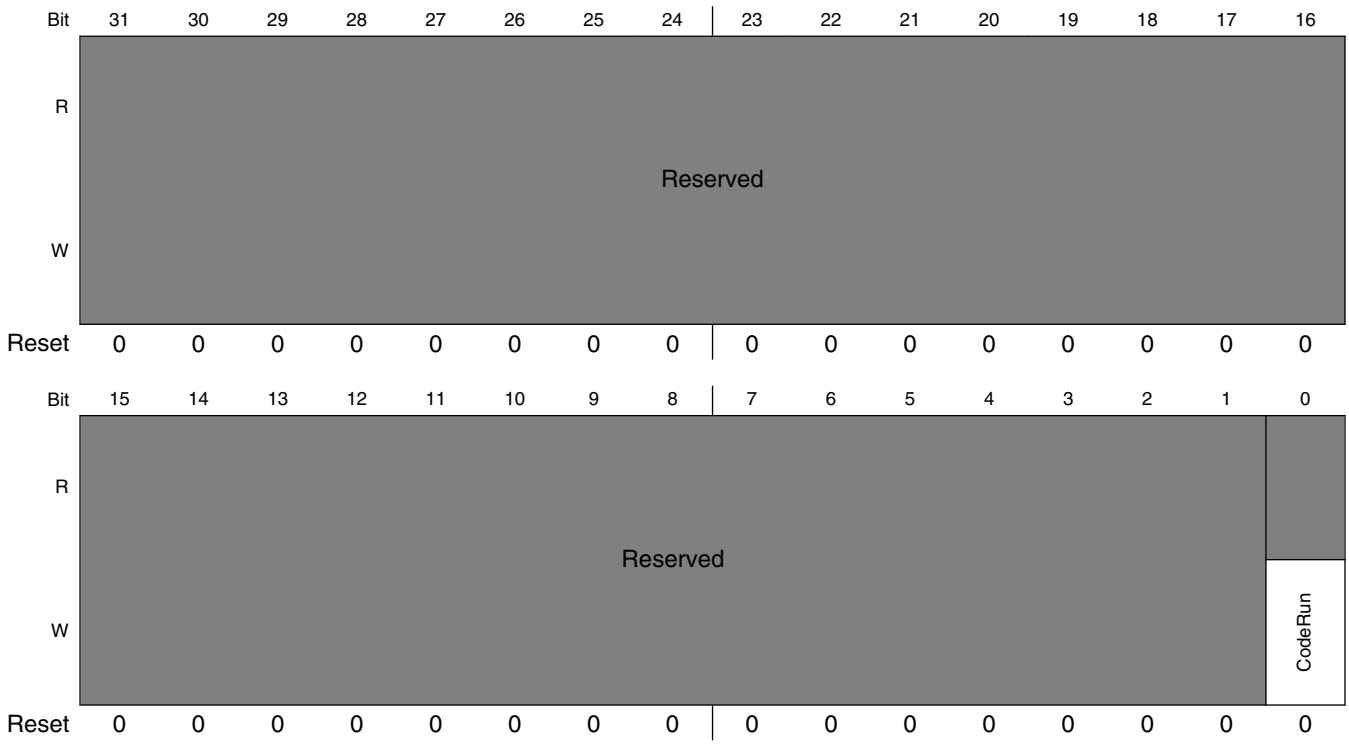
VPU memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
204_0000	BIT Processor run start (VPU_CodeRun)	32	W	0000_0000h	69.8.1/5741
204_0004	BIT Boot Code Download Data register (VPU_CodeDown)	32	W	0000_0000h	69.8.2/5741
204_0008	Host Interrupt Request to BIT (VPU_HostIntReq)	32	W	0000_0000h	69.8.3/5742
204_000C	BIT Interrupt Clear (VPU_BitIntClear)	32	W	0000_0000h	69.8.4/5743
204_0010	BIT Interrupt Status (VPU_BitIntSts)	32	R	0000_0000h	69.8.5/5744
204_0018	BIT Current PC (VPU_BitCurPc)	32	R	0000_0000h	69.8.6/5745
204_0020	BIT CODEC Busy (VPU_BitCodecBusy)	32	R	0000_0000h	69.8.7/5746

69.8.1 BIT Processor run start (VPU_CodeRun)

See the figure below for illustration of valid bits in VPU Code Run Register and the table below for description of the bit fields in the register.

Address: 204_0000h base + 0h offset = 204_0000h



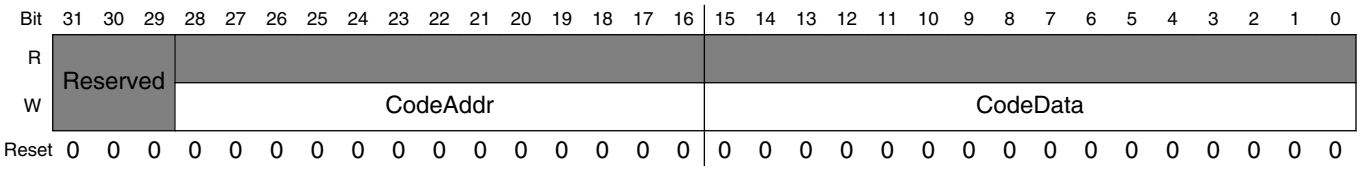
VPU_CodeRun field descriptions

Field	Description
31–1 -	This field is reserved. Reserved
0 CodeRun	VPU_CodeRun. BIT processor run start bit. 0 BIT Processor stop execution. 1 BIT Processor start execution.

69.8.2 BIT Boot Code Download Data register (VPU_CodeDown)

See the figure below for illustration of valid bits in VPU BIT Boot Code Download Data Register and the following table for description of the bit fields in the register.

Address: 204_0000h base + 4h offset = 204_0004h



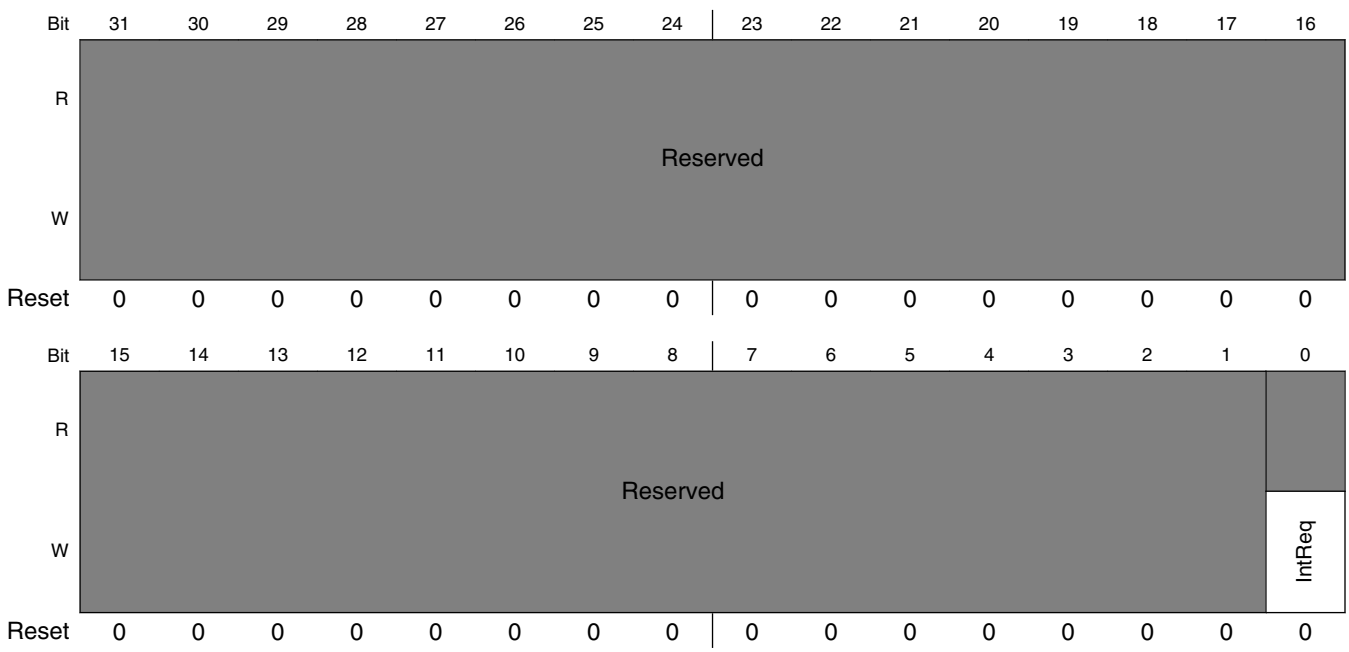
VPU_CodeDown field descriptions

Field	Description
31–29 -	This field is reserved. Reserved
28–16 CodeAddr	CodeAddr[12:0] Download address of VPU BIT boot code, which is VPU internal address of BIT processor.
CodeData	CodeData[15:0] Download data of VPU BIT boot code.

69.8.3 Host Interrupt Request to BIT (VPU_HostIntReq)

See the figure below for illustration of valid bits in VPU Host Interrupt Request Register and the following table for description of the bit fields in the register.

Address: 204_0000h base + 8h offset = 204_0008h



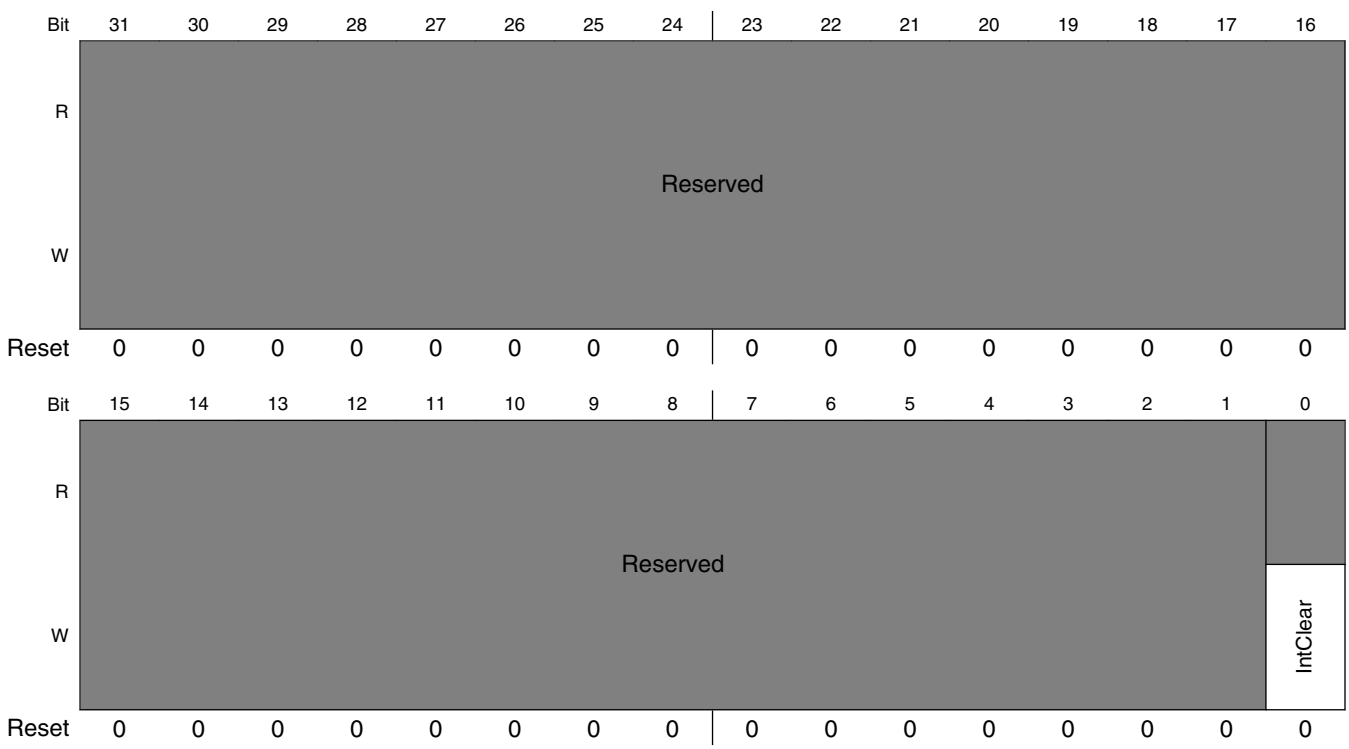
VPU_HostIntReq field descriptions

Field	Description
31–1 -	This field is reserved. Reserved
0 IntReq	IntReq. The host interrupt request bit. 0 No host interrupt is requested. 1 The host processor request interrupt to the BIT processor.

69.8.4 BIT Interrupt Clear (VPU_BitIntClear)

See the figure below for illustration of valid bits in VPU BIT Interrupt Clear Register and the following table for description of the bit fields in the register.

Address: 204_0000h base + Ch offset = 204_000Ch



VPU_BitIntClear field descriptions

Field	Description
31–1 -	This field is reserved. Reserved
0 IntClear	IntClear. BIT interrupt clear bit.

Table continues on the next page...

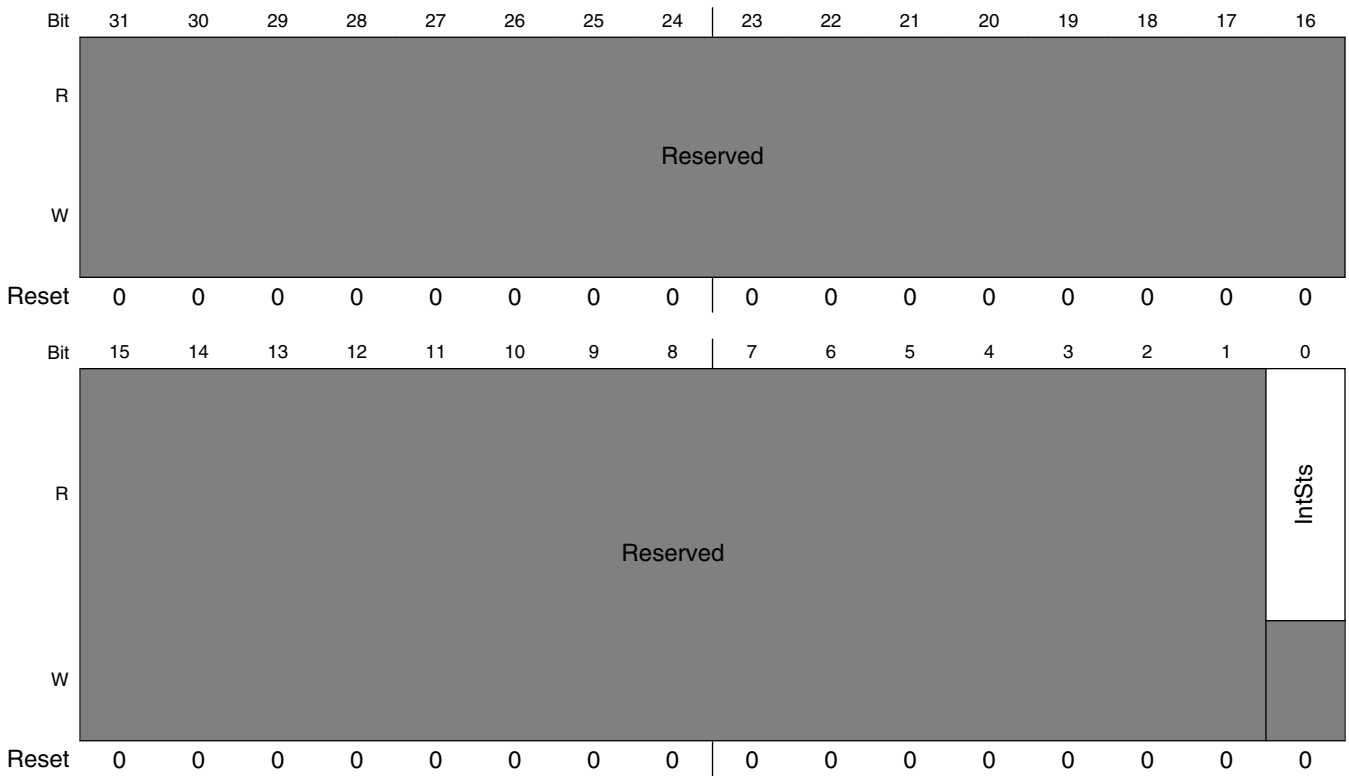
VPU_BitIntClear field descriptions (continued)

Field	Description
	0 No operation is issued. 1 Clear the BIT interrupt to the host.

69.8.5 BIT Interrupt Status (VPU_BitIntSts)

See the figure below for illustration of valid bits in VPU BIT Interrupt Status Register and the following table for description of the bit fields in the register.

Address: 204_0000h base + 10h offset = 204_0010h



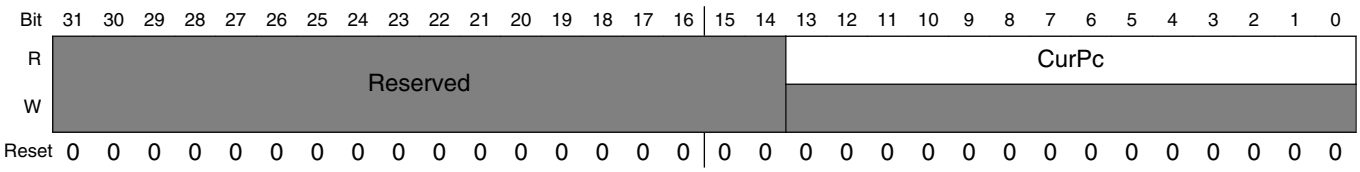
VPU_BitIntSts field descriptions

Field	Description
31–1 -	This field is reserved. Reserved
0 IntSts	IntSts. BIT interrupt status bit. 0 No BIT interrupt is asserted. 1 The BIT interrupt is asserted to the host. It is cleared when the host processor write "1" to VPU_BitIntClear register.

69.8.6 BIT Current PC (VPU_BitCurPc)

See the figure below for illustration of valid bits in VPU BIT Current PC Register and the following table for description of the bit fields in the register.

Address: 204_0000h base + 18h offset = 204_0018h



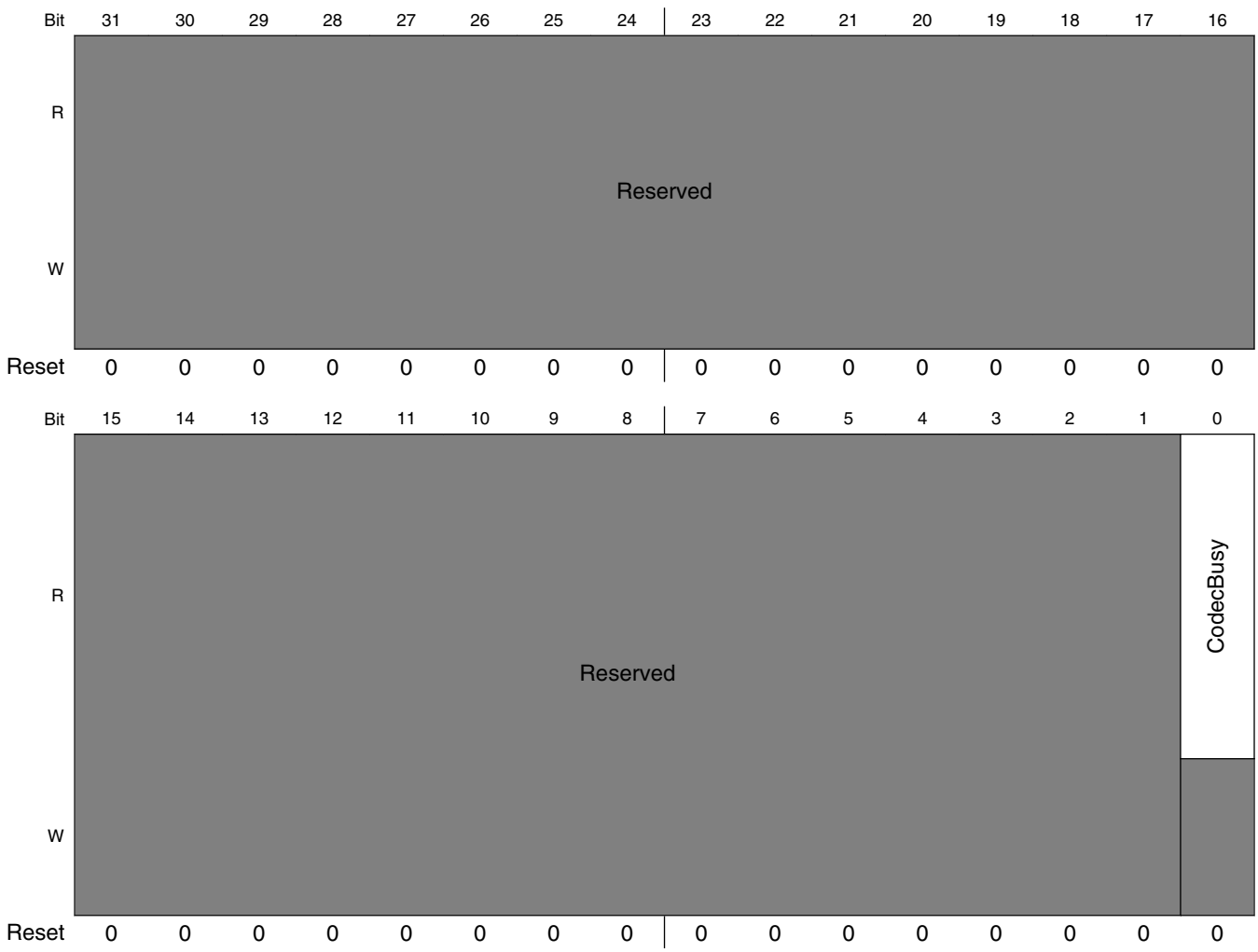
VPU_BitCurPc field descriptions

Field	Description
31–14 -	This field is reserved. Reserved
CurPc	CurPc[13:0]. BIT current PC value. Returns the current program counter of BIT processor by reading this register.

69.8.7 BIT CODEC Busy (VPU_BitCodecBusy)

See the figure below for illustration of valid bits in VPU BIT Codec Busy Register and the following table for description of the bit fields in the register.

Address: 204_0000h base + 20h offset = 204_0020h



VPU_BitCodecBusy field descriptions

Field	Description
31–1 -	This field is reserved. Reserved
0 CodecBusy	Codec busy flag for Bit processor.BIT processor write "1"to this register when the processor is running."0"means processor is waiting for a command.This value is connected to the o_vpu_idle.