    - The display is connected to the appropriate pins.
    - The simplest mapping would be
        - Map the pixel to the data bus in the same way as for 24 bpp
        - Set the values at the extra LSBs to zero.
- Parameter updates
    - The reference signature can be freely updated from frame to frame, in coordination with the changing content (since it is used only once per frame, just before the interrupt)
    - Each ROI can be freely and independently enabled/disabled between frames (since the enable bit is double buffered)
    - The size and location of a ROI can be modified while it is disabled.
    - Display interface signals polarity can be changed only when the module is disabled.
- ROI (regions of interest) don't overlap, i.e. each pixel belongs to single ROI at most.
- DCIC operation is intended for monitoring relatively static portions of graphic interface, otherwise it will be complicated software task to keep up with frame synchronization and update expected signature for each frame.
- There should be no processing done at IPU on monitored ROIs, which can't be taken in consideration by software when calculating the expected signature.

20.3 DCIC Memory Map/Register Definition

Important: All write accesses have to be full word (32-bit) accesses. No error/abort will be responded in case of different access size, but no data will be written. Similarly, there will be no error response in case of access to undefined memory space.

Read access will return 32-bit data, which may be truncated on system level in case it wasn't full word acces.

DCIC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
20E_4000	DCIC Control Register (DCIC1_DCICC)	32	R/W	0000_0070h	20.3.1/964
20E_4004	DCIC Interrupt Control Register (DCIC1_DCICIC)	32	R/W	0000_0003h	20.3.2/965
20E_4008	DCIC Status Register (DCIC1_DCICS)	32	w1c	0000_0000h	20.3.3/966
20E_4010	DCIC ROI Config Register m (DCIC1_DCICRC)	32	R/W	0000_0000h	20.3.4/967
20E_4014	DCIC ROI Size Register m (DCIC1_DCICRS)	32	R/W	0000_0000h	20.3.5/968

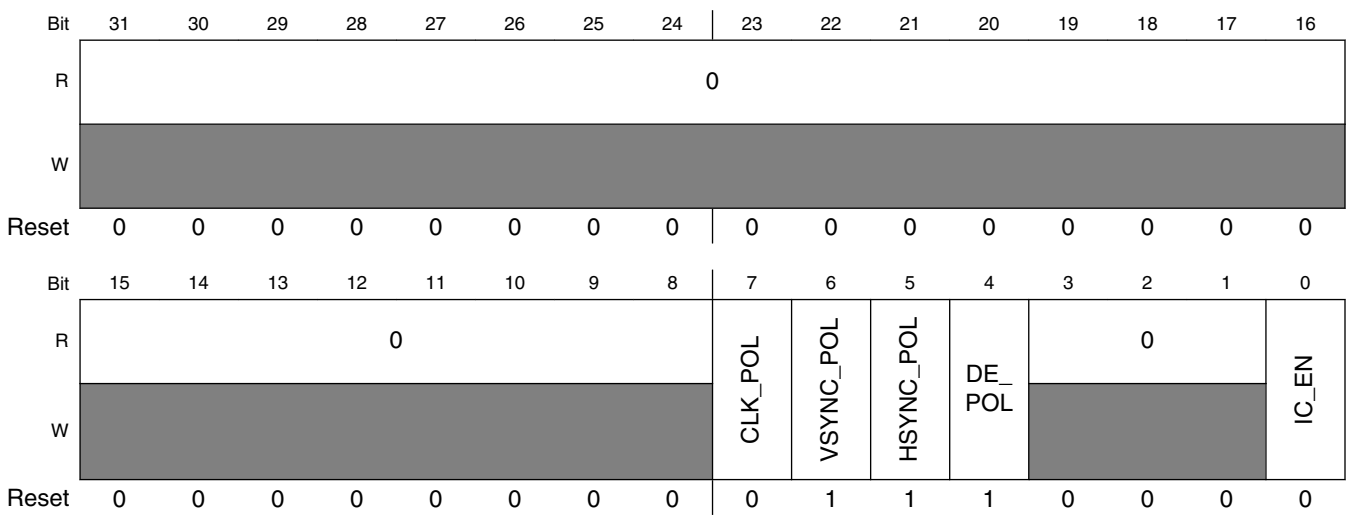
Table continues on the next page...

DCIC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
20E_4018	DCIC ROI Reference Signature Register m (DCIC1_DCICRRS)	32	R/W	0000_0000h	20.3.6/969
20E_401C	DCIC ROI Calculated Signature m (DCIC1_DCICRCS)	32	R	0000_0000h	20.3.7/969
20E_8000	DCIC Control Register (DCIC2_DCICC)	32	R/W	0000_0070h	20.3.1/964
20E_8004	DCIC Interrupt Control Register (DCIC2_DCICIC)	32	R/W	0000_0003h	20.3.2/965
20E_8008	DCIC Status Register (DCIC2_DCICS)	32	w1c	0000_0000h	20.3.3/966
20E_8010	DCIC ROI Config Register m (DCIC2_DCICRC)	32	R/W	0000_0000h	20.3.4/967
20E_8014	DCIC ROI Size Register m (DCIC2_DCICRS)	32	R/W	0000_0000h	20.3.5/968
20E_8018	DCIC ROI Reference Signature Register m (DCIC2_DCICRRS)	32	R/W	0000_0000h	20.3.6/969
20E_801C	DCIC ROI Calculated Signature m (DCIC2_DCICRCS)	32	R	0000_0000h	20.3.7/969

20.3.1 DCIC Control Register (DCICx_DCICC)

Address: Base address + 0h offset



DCICx_DCICC field descriptions

Field	Description
31–8 Reserved	This read-only field is reserved and always has the value 0.
7 CLK_POL	DISP_CLK signal polarity. 0 Not inverted (default). 1 Inverted.
6 VSYNC_POL	VSYNC_IN signal polarity.

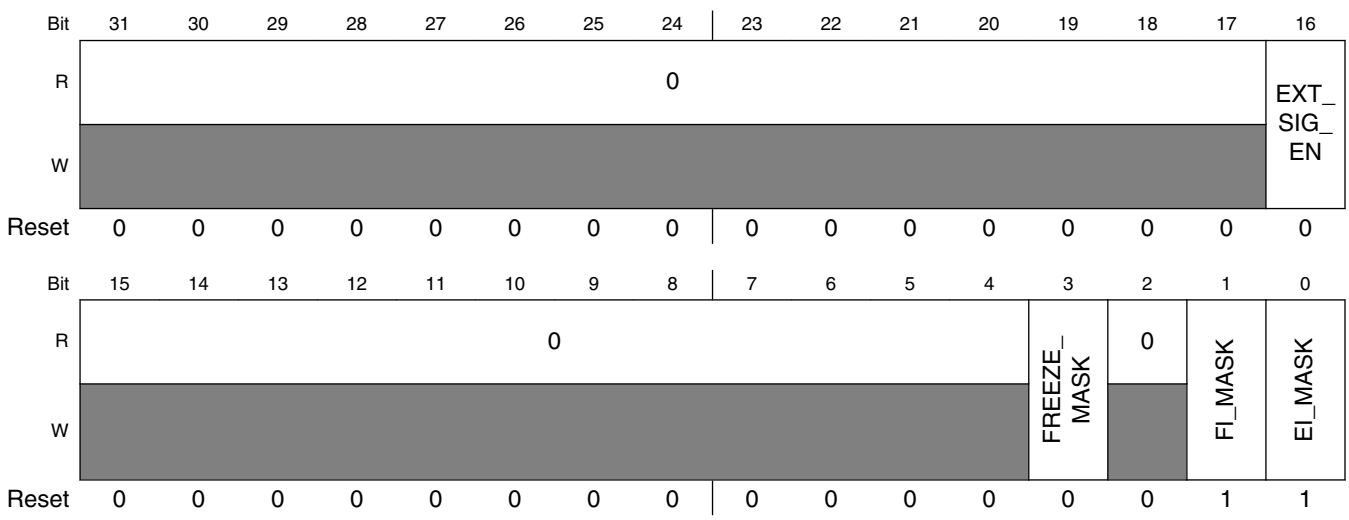
Table continues on the next page...

DCICx_DCICC field descriptions (continued)

Field	Description
	0 Active High. 1 Active Low (default).
5 HSYNC_POL	HSYNC_IN signal polarity. 0 Active High. 1 Active Low (default).
4 DE_POL	DATA_EN_IN signal polarity. 0 Active High. 1 Active Low (default).
3–1 Reserved	This read-only field is reserved and always has the value 0.
0 IC_EN	Integrity Check enable. Main enable switch. 0 Disabled 1 Enabled

20.3.2 DCIC Interrupt Control Register (DCICx_DCICIC)

Address: Base address + 4h offset



DCICx_DCICIC field descriptions

Field	Description
31–17 Reserved	This read-only field is reserved and always has the value 0.
16 EXT_SIG_EN	External controller mismatch indication signal. 0 Disabled (default) 1 Enabled

Table continues on the next page...

DCICx_DCICIC field descriptions (continued)

Field	Description
15–4 Reserved	This read-only field is reserved and always has the value 0.
3 FREEZE_MASK	Disable change of interrupt masks. "Sticky" bit which can be set once and cleared by reset only. 0 Masks change allowed (default) 1 Masks are frozen
2 Reserved	This read-only field is reserved and always has the value 0.
1 FI_MASK	Functional Interrupt mask. Can be changed only while FREEZE_MASK = 0. 0 Mask disabled - Interrupt assertion enabled 1 Mask enabled - Interrupt assertion disabled (default)
0 EI_MASK	Error Interrupt mask. Can be changed only while FREEZE_MASK = 0. 0 Mask disabled - Interrupt assertion enabled 1 Mask enabled - Interrupt assertion disabled (default)

20.3.3 DCIC Status Register (DCICx_DCICS)

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0														FI_STAT	EI_STAT
W															w1c	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

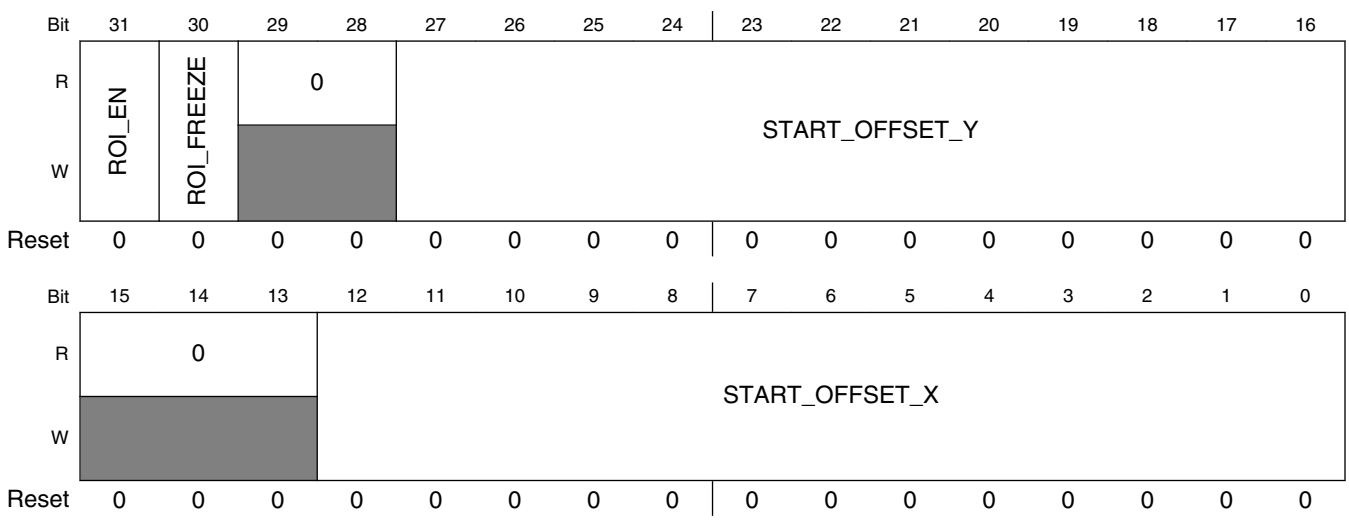
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ROI_MATCH_STAT															
W	w1c															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DCICx_DCICS field descriptions

Field	Description
31–18 Reserved	This read-only field is reserved and always has the value 0.
17 FI_STAT	Functional Interrupt status. Write "1" to clear. 0 No pending Interrupt 1 Pending Interrupt
16 EI_STAT	Error Interrupt status. Result of "OR" operation on ROI_MATCH_STAT[15:0] bits. Cleared when these bits are clear. 0 No pending Interrupt 1 Pending Interrupt
ROI_MATCH_STAT	Each set bit of this field indicates there was a mismatch at appropriate ROIs signature during the last frame. Valid only for active ROIs. Write "1" to clear. 0 ROI calculated CRC matches expected signature 1 Mismatch at ROI calculated CRC

20.3.4 DCIC ROI Config Register m (DCICx_DCICRC)

Address: Base address + 10h offset



DCICx_DCICRC field descriptions

Field	Description
31 ROI_EN	ROI #m tracking enable 0 Disabled 1 Enabled

Table continues on the next page...

DCICx_DCICRC field descriptions (continued)

Field	Description
30 ROI_FREEZE	When set, the only parameter of ROI #m that can be changed is reference signature. "Sticky" bit - can be set once and cleared by reset only. 0 ROI configuration can be changed 1 ROI configuration is frozen
29–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 START_ OFFSET_Y	Row number of ROIs upper-left corner (Y coordinate) Range: 0 to 2^12-1
15–13 Reserved	This read-only field is reserved and always has the value 0.
START_ OFFSET_X	Column number of ROIs upper-left corner (X coordinate) Range: 0 to 2^13-1

20.3.5 DCIC ROI Size Register m (DCICx_DCICRS)

Address: Base address + 14h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				END_OFFSET_Y												0			END_OFFSET_X											
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DCICx_DCICRS field descriptions

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 END_OFFSET_Y	Row number of ROIs lower-right corner (Y coordinate) Range: 1 to 2^12-1
15–13 Reserved	This read-only field is reserved and always has the value 0.
END_OFFSET_X	Column number of ROIs lower-right corner (X coordinate) Range: 1 to 2^13-1

20.3.6 DCIC ROI Reference Signature Register m (DCICx_DCICRRS)

Address: Base address + 18h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	REFERENCE_SIGNATURE																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DCICx_DCICRRS field descriptions

Field	Description
REFERENCE_ SIGNATURE	32-bit expected signature (CRC calculation result) for ROI #m

20.3.7 DCIC ROI Calculated Signature m (DCICx_DCICRCS)

Address: Base address + 1Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CALCULATED_SIGNATURE																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DCICx_DCICRCS field descriptions

Field	Description
CALCULATED_ SIGNATURE	32-bit actual signature (CRC calculation result) for ROI #m during the last frame. Updated automatically at the beginning of a next frame.