### 57.8.3 General initialization guidelines

Complete the following steps in order to properly initialize the module:

1. Enable interrupts in SNVScontrol and configuration registers.
2. Program SNVS general functions/configurations.
3. User Specific: Set lock bits.

**NOTE**

## 57.9 SNVS Memory Map/Register Definition

This section contains detailed register descriptions for the SNVS registers. Each description includes a standard register diagram and register table. The register table provides detailed descriptions of the register bit and field functions, in bit order.

SNVS registers consist of two types:

- Privileged read/write accessible
- Non-privileged read/write accessible

Privileged read/write accessible registers can only be accessed for read/write by privileged software. Unauthorized write accesses are ignored, and unauthorized read accesses return zero. Non-privileged software can access privileged access registers when the non-privileged software access enable bit is set in the SNVS_HP Command Register.

- Non-Secure
- Trusted
- Secure

Non-privileged read/write accessible registers are read/write accessible by any software.

The following table shows the SNVS memory map. The LP register values are set only on LP POR and are unaffected by System (HP) POR. The HP registers are set only on System POR and are unaffected by LP POR.

**NOTE**

For more information on security-related bitfields, see the *Security Reference Manual for i.MX 6Dual, 6Quad, 6Solo, and 6DualLite Families of Application Processors*

*(IMX6DQ6SDLSRM)* or the *Applications Processor Security Reference Manual for i.MX 6SoloLite (IMX6SLSRM).*

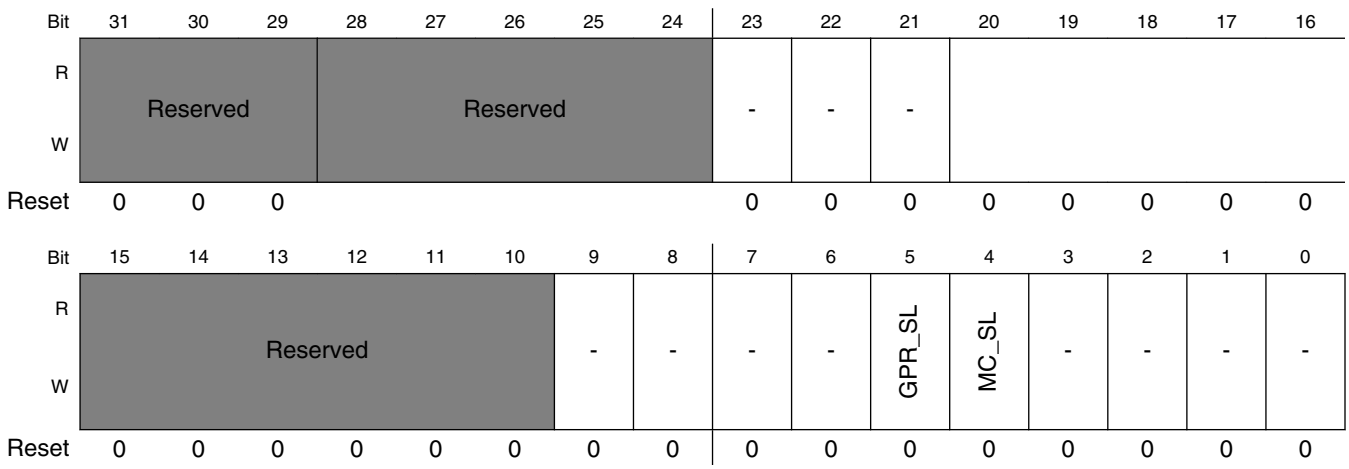
## SNVS memory map

| Offset address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|---|---|---|---|---|---|
| 20C_C000 | SNVS_HP Lock Register (SNVS_HPLR) | 32 | R/W | 0000_0000h | 57.9.1/4983 |
| 20C_C004 | SNVS_HP Command Register (SNVS_HPCOMR) | 32 | R/W | 0000_0000h | 57.9.2/4985 |
| 20C_C008 | SNVS_HP Control Register (SNVS_HPCR) | 32 | R/W | 0000_0000h | 57.9.3/4987 |
| 20C_C014 | SNVS_HP Status Register (SNVS_HPSR) | 32 | R/W | 8000_0000h | 57.9.4/4990 |
| 20C_C024 | SNVS_HP Real Time Counter MSB Register (SNVS_HPRTCMR) | 32 | R/W | 0000_0000h | 57.9.5/4992 |
| 20C_C028 | SNVS_HP Real Time Counter LSB Register (SNVS_HPRTCLR) | 32 | R/W | 0000_0000h | 57.9.6/4993 |
| 20C_C02C | SNVS_HP Time Alarm MSB Register (SNVS_HPTAMR) | 32 | R/W | 0000_0000h | 57.9.7/4993 |
| 20C_C030 | SNVS_HP Time Alarm LSB Register (SNVS_HPTALR) | 32 | R/W | 0000_0000h | 57.9.8/4994 |
| 20C_C034 | SNVS_LP Lock Register (SNVS_LPLR) | 32 | R/W | 0000_0000h | 57.9.9/4994 |
| 20C_C038 | SNVS_LP Control Register (SNVS_LPCR) | 32 | R/W | 0000_0000h | 57.9.10/ 4996 |
| 20C_C04C | SNVS_LP Status Register (SNVS_LPSR) | 32 | R/W | 0000_0008h | 57.9.11/ 4999 |
| 20C_C05C | SNVS_LP Secure Monotonic Counter MSB Register (SNVS_LPSMCMR) | 32 | R/W | 0000_0000h | 57.9.12/ 5001 |
| 20C_C060 | SNVS_LP Secure Monotonic Counter LSB Register (SNVS_LPSMCLR) | 32 | R/W | 0000_0000h | 57.9.13/ 5002 |
| 20C_C068 | SNVS_LP General Purpose Register (SNVS_LPGPR) | 32 | R/W | 0000_0000h | 57.9.14/ 5002 |
| 20C_CBF8 | SNVS_HP Version ID Register 1 (SNVS_HPVIDR1) | 32 | R | 003E_0100h | 57.9.15/ 5003 |
| 20C_CBFC | SNVS_HP Version ID Register 2 (SNVS_HPVIDR2) | 32 | R | 0000_0000h | 57.9.16/ 5003 |

## 57.9.1 SNVS_HP Lock Register (SNVS_HPLR)

The SNVS_HP Lock Register contains lock bits for the SNVS registers. This is a privileged write register.

Address: 20C_C000h base + 0h offset = 20C_C000h




**SNVS_HPLR field descriptions**

| Field | Description |
|---|---|
| 31–29<br>- | This field is reserved. |
| 23–19<br>- | This field is reserved. |
| 18<br>- | This field is reserved. |
| 17<br>- | This field is reserved. |
| 16<br>- | This field is reserved. |
| 15–10<br>- | This field is reserved. |
| 9<br>- | This field is reserved. |
| 8<br>- | This field is reserved. |
| 7<br>- | This field is reserved. |
| 6<br>- | This field is reserved. |
| 5<br>GPR_SL | General Purpose Register Soft Lock |

*Table continues on the next page...*

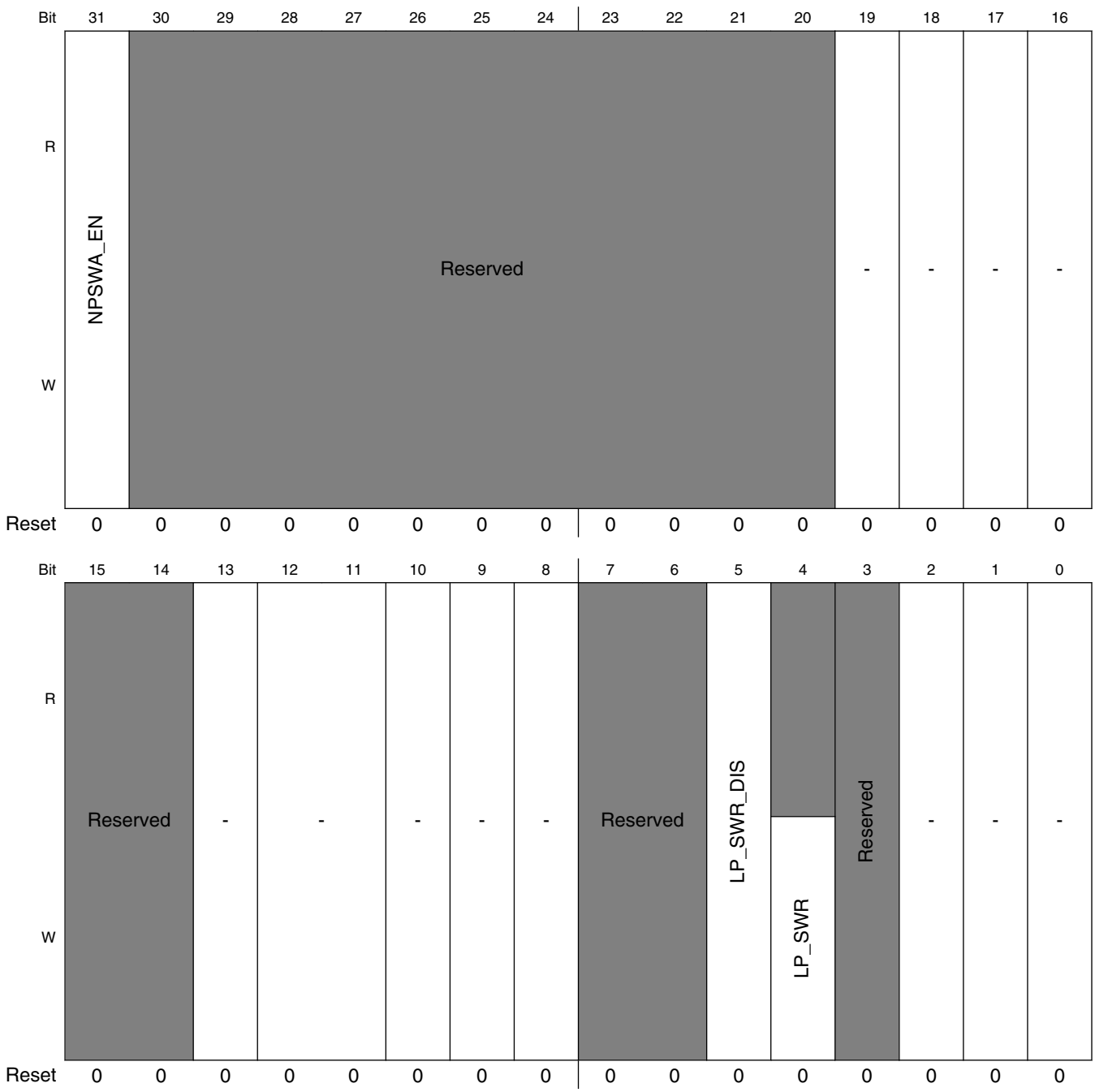
## SNVS_HPLR field descriptions (continued)

| Field | Description |
|---|---|
| | When set, prevents any writes to the GPR. Once set, this bit can only be reset by the system reset.<br><br>0 Write access is allowed<br>1 Write access is not allowed |
| 4<br>MC_SL | Monotonic Counter Soft Lock<br><br>When set, prevents any writes (increments) to the MC Registers and MC_ENV bit. Once set, this bit can only be reset by the system reset.<br><br>0 Write access (increment) is allowed<br>1 Write access (increment) is not allowed |
| 3<br>- | This field is reserved. |
| 2<br>- | This field is reserved. |
| 1<br>- | This field is reserved. |
| 0<br>- | This field is reserved. |

## 57.9.2 SNVS_HP Command Register (SNVS_HPCOMR)

The SNVS_HP Command Register contains the command, configuration, and control bits for the SNVS block. This is a privileged write register.

Address: 20C_C000h base + 4h offset = 20C_C004h



## SNVS_HPCOMR field descriptions

| Field | Description |
|---|---|
| 31<br>NPSWA_EN | Non-Privileged Software Access Enable<br>When set, allows non-privileged software to access all SNVS registers, including those that are privileged software read/write access only.<br>0 Only privileged software can access privileged registers<br>1 Any software can access privileged registers |
| 30–20<br>- | This field is reserved. |
| 19<br>- | This field is reserved. |
| 18<br>- | This field is reserved. |
| 17<br>- | This field is reserved. |
| 16<br>- | This field is reserved. |
| 15–14<br>- | This field is reserved. |
| 13<br>- | This field is reserved. |
| 12–11<br>- | This field is reserved. |
| 10<br>- | This field is reserved. |
| 9<br>- | This field is reserved. |
| 8<br>- | This field is reserved. |
| 7–6<br>- | This field is reserved. |
| 5<br>LP_SWR_DIS | LP Software Reset Disable<br>When set, disables the LP software reset. Once set, this bit can only be reset by the system reset.<br>0 LP software reset is enabled<br>1 LP software reset is disabled |
| 4<br>LP_SWR | LP Software Reset<br>When set, it resets the SNVS_LP section. This bit cannot be set when the LP_SWR_DIS bit is set. This self-clearing bit is always read as zero.<br>0 No Action<br>1 Reset LP section |
| 3<br>- | This field is reserved. |
| 2<br>- | This field is reserved. |
| 1<br>- | This field is reserved. |

*Table continues on the next page...*

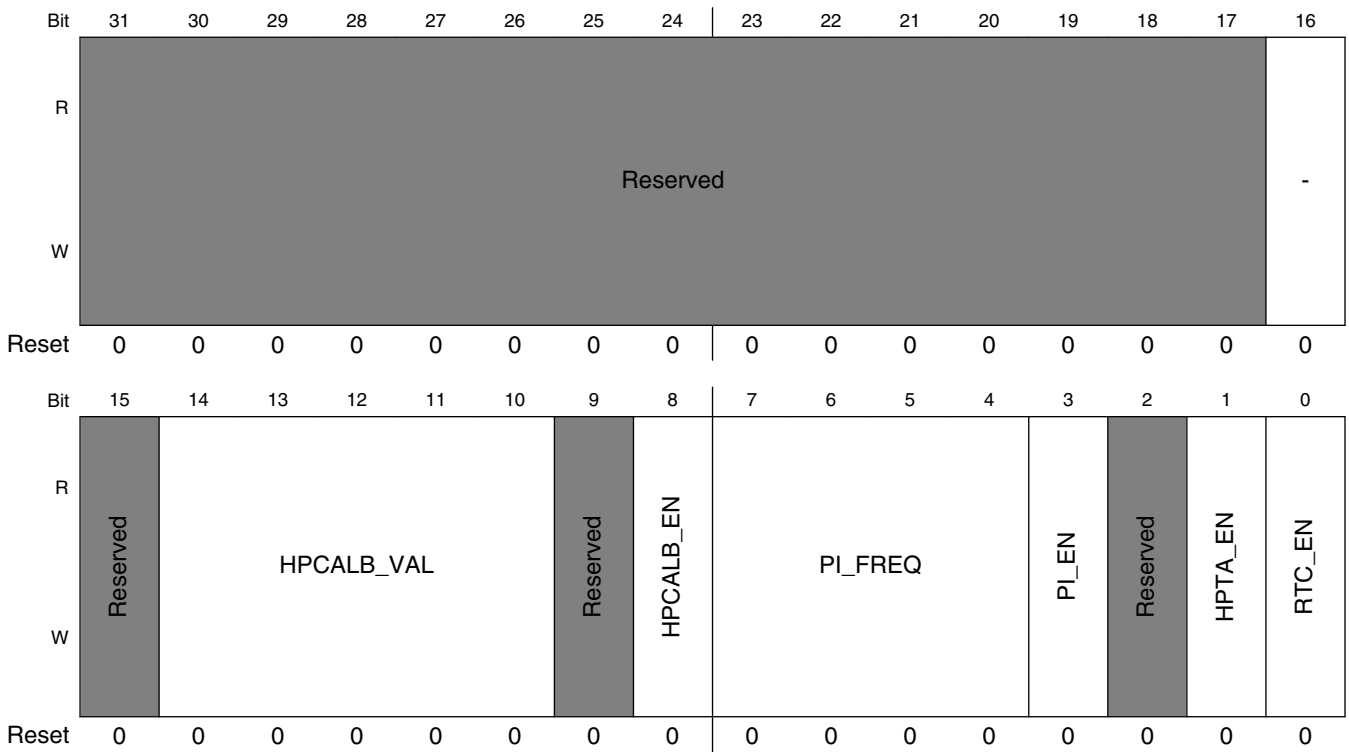
**SNVS_HPCOMR field descriptions (continued)**

| Field | Description |
|---|---|
| 0<br>- | This field is reserved. |

## 57.9.3 SNVS_HP Control Register (SNVS_HPCR)

The SNVS_HP Control Register contains various control bits of the HP section of SNVS .

Address: 20C_C000h base + 8h offset = 20C_C008h




**SNVS_HPCR field descriptions**

| Field | Description |
|---|---|
| 31–17<br>- | This field is reserved. |
| 16<br>- | This field is reserved. |
| 15<br>- | This field is reserved. |

*Table continues on the next page...*

## SNVS_HPCR field descriptions (continued)

| Field | Description |
|---|---|
| 14–10<br>HPCALB_VAL | HP Calibration Value<br>Defines signed calibration value for the HP Real Time Counter. This field can be programmed only when RTC Calibration is disabled (HPCALB_EN is not set). This is a 5-bit 2's complement value, hence the allowable calibration values are in the range from -16 to +15 counts per 32768 ticks of the counter.<br>00000 +0 counts per each 32768 ticks of the counter<br>00001 +1 counts per each 32768 ticks of the counter<br>00010 +2 counts per each 32768 ticks of the counter<br>01111 +15 counts per each 32768 ticks of the counter<br>10000 -16 counts per each 32768 ticks of the counter<br>10001 -15 counts per each 32768 ticks of the counter<br>11110 -2 counts per each 32768 ticks of the counter<br>11111 -1 counts per each 32768 ticks of the counter |
| 9<br>- | This field is reserved. |
| 8<br>HPCALB_EN | HP Real Time Counter Calibration Enabled<br>Indicates that the time calibration mechanism is enabled.<br>0 HP Timer calibration disabled<br>1 HP Timer calibration enabled |
| 7–4<br>PI_FREQ | Periodic Interrupt Frequency<br>Defines frequency of the periodic interrupt. The interrupt is generated when a zero-to-one or one-to-zero transition occurs on the selected bit of the HP Real Time Counter and Real Time Counter and Periodic Interrupt are both enabled (RTC_EN and PI_EN are set). It is recommended to program this field when Periodic Interrupt is disabled (PI_EN is not set). The possible frequencies are:<br>0000 - bit 0 of the RTC is selected as a source of the periodic interrupt<br>0001 - bit 1 of the RTC is selected as a source of the periodic interrupt<br>0010 - bit 2 of the RTC is selected as a source of the periodic interrupt<br>0011 - bit 3 of the RTC is selected as a source of the periodic interrupt<br>0100 - bit 4 of the RTC is selected as a source of the periodic interrupt<br>0101 - bit 5 of the RTC is selected as a source of the periodic interrupt<br>0110 - bit 6 of the RTC is selected as a source of the periodic interrupt<br>0111 - bit 7 of the RTC is selected as a source of the periodic interrupt<br>1000 - bit 8 of the RTC is selected as a source of the periodic interrupt<br>1001 - bit 9 of the RTC is selected as a source of the periodic interrupt<br>1010 - bit 10 of the RTC is selected as a source of the periodic interrupt<br>1011 - bit 11 of the RTC is selected as a source of the periodic interrupt<br>1100 - bit 12 of the RTC is selected as a source of the periodic interrupt<br>1101 - bit 13 of the RTC is selected as a source of the periodic interrupt<br>1110 - bit 14 of the RTC is selected as a source of the periodic interrupt<br>1111 - bit 15 of the RTC is selected as a source of the periodic interrupt |
| 3<br>PI_EN | HP Periodic Interrupt Enable<br>The periodic interrupt can be generated only if the HP Real Time Counter is enabled.<br>0 HP Periodic Interrupt is disabled<br>1 HP Periodic Interrupt is enabled |

*Table continues on the next page...*

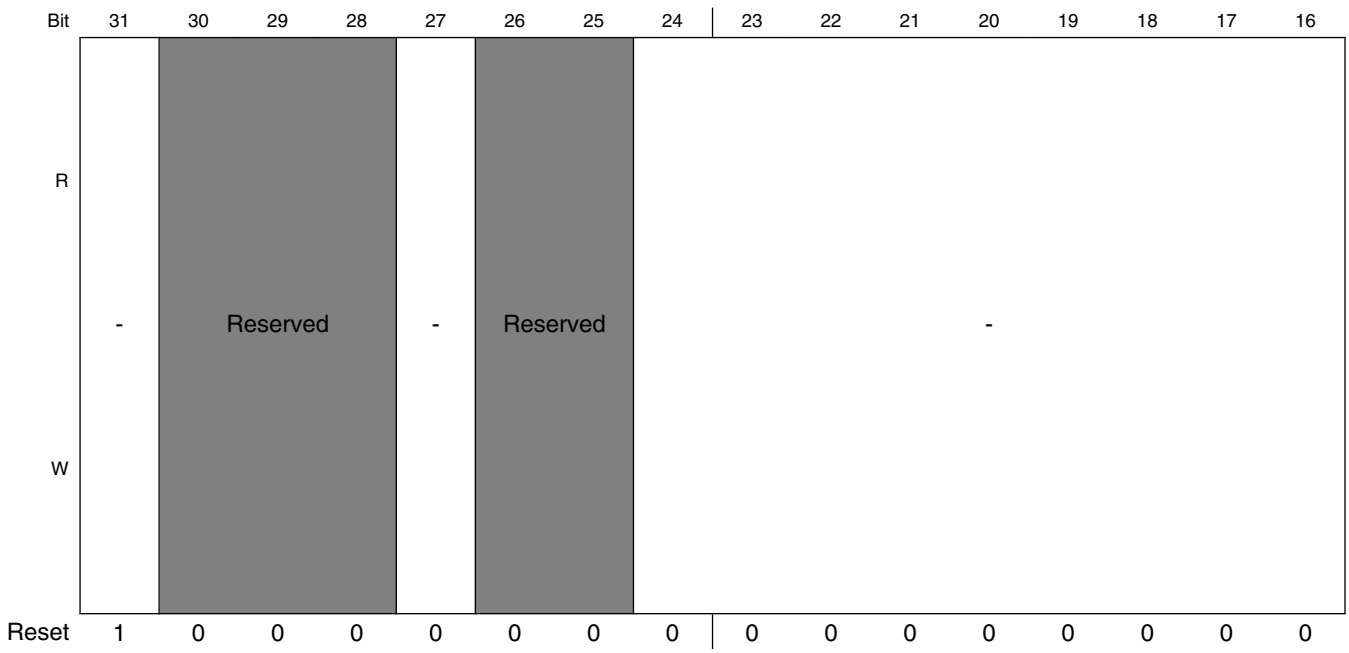
## SNVS_HPCR field descriptions (continued)

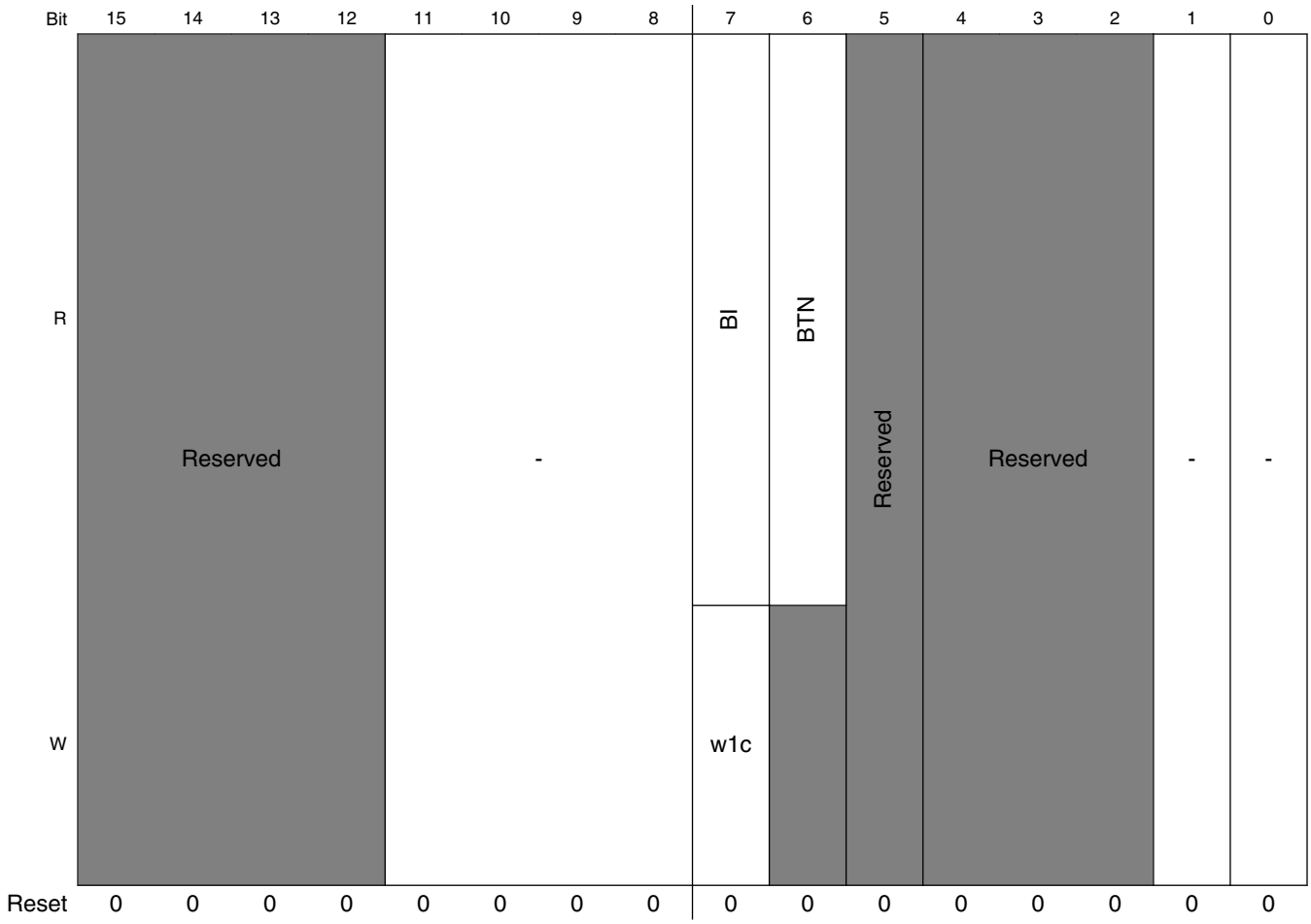
| Field | Description |
|---|---|
| 2<br>- | This field is reserved. |
| 1<br>HPTA_EN | HP Time Alarm Enable<br>When set, the time alarm interrupt is generated if the value in the HP Time Alarm Registers is equal to the value of the HP Real Time Counter.<br>0 HP Time Alarm Interrupt is disabled<br>1 HP Time Alarm Interrupt is enabled |
| 0<br>RTC_EN | HP Real Time Counter Enable<br>0 RTC is disabled<br>1 RTC is enabled |

## 57.9.4 SNVS_HP Status Register (SNVS_HPSR)

The HP Status Register reflects the internal state of the SNVS.

Address: 20C_C000h base + 14h offset = 20C_C014h






## SNVS_HPSR field descriptions

| Field | Description |
|---|---|
| 31<br>- | This field is reserved. |
| 30–28<br>- | This field is reserved. |
| 27<br>- | This field is reserved. |
| 26–25<br>- | This field is reserved. |
| 24–16<br>- | This field is reserved. |
| 15–12<br>- | This field is reserved. |
| 11–8<br>- | This field is reserved. |
| 7<br>BI | Button Interrupt. Signal ipi_snvs_btn_int_b was asserted. |
| 6<br>BTN | Value of the BTN input. This is the external button used for PMIC control. |

*Table continues on the next page...*

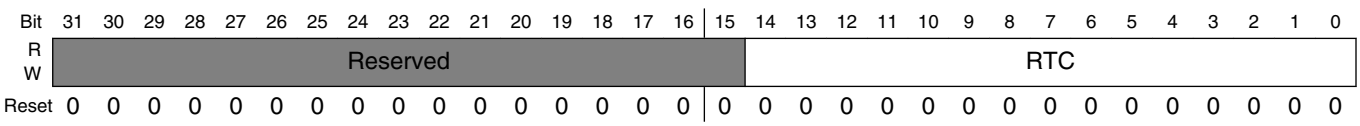
**SNVS_HPSR field descriptions (continued)**

| Field | Description |
|---|---|
| | 0: BTN not pressed<br>1: BTN pressed |
| 5<br>- | This field is reserved. |
| 4–2<br>- | This field is reserved. |
| 1<br>- | This field is reserved. |
| 0<br>- | This field is reserved. |

## 57.9.5 SNVS_HP Real Time Counter MSB Register (SNVS_HPRTCMR)

The SNVS_HP Real Time Counter MSB register contains the most significant bits of the HP Real Time Counter.

Address: 20C_C000h base + 24h offset = 20C_C024h



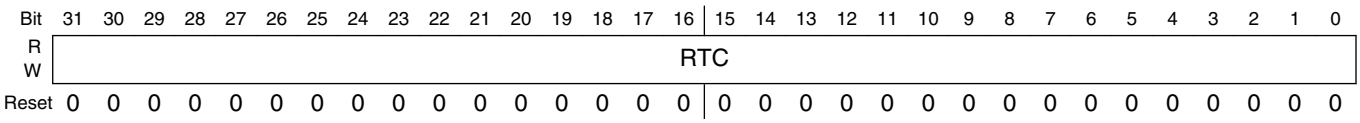

**SNVS_HPRTCMR field descriptions**

| Field | Description |
|---|---|
| 31–15<br>- | This field is reserved.<br>Reserved |
| RTC | HP Real Time Counter<br>Most significant 15 bits. This register can be programmed only when RTC is not active (RTC_EN bit is not set). |

## 57.9.6 SNVS_HP Real Time Counter LSB Register (SNVS_HPRTCLR)

The SNVS_HP Real Time Counter LSB register contains the 32 least significant bits of the HP real time counter.

Address: 20C_C000h base + 28h offset = 20C_C028h



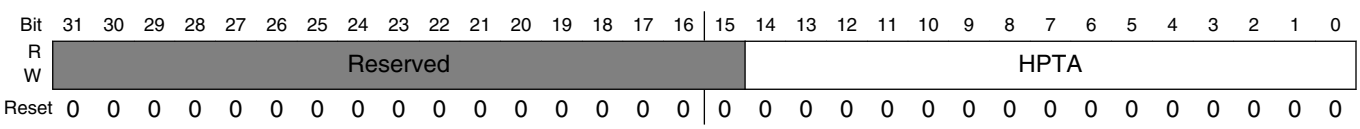

**SNVS_HPRTCLR field descriptions**

| Field | Description |
|---|---|
| RTC | HP Real Time Counter<br>Least significant 32 bits. This register can be programmed only when RTC is not active (RTC_EN bit is not set). |

## 57.9.7 SNVS_HP Time Alarm MSB Register (SNVS_HPTAMR)

The SNVS_HP Time Alarm MSB register contains the most significant bits of the SNVS_HP Time Alarm value.

Address: 20C_C000h base + 2Ch offset = 20C_C02Ch




**SNVS_HPTAMR field descriptions**

| Field | Description |
|---|---|
| 31–15<br>- | This field is reserved. |
| HPTA | HP Time Alarm<br>Most significant 15 bits. This register can be programmed only when HP time alarm is disabled (HPTA_EN bit is not set). |

## 57.9.8 SNVS_HP Time Alarm LSB Register (SNVS_HPTALR)

The SNVS_HP Time Alarm LSB register contains the 32 least significant bits of the SNVS_HP Time Alarm value.

Address: 20C_C000h base + 30h offset = 20C_C030h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | HPTA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SNVS_HPTALR field descriptions**

| Field | Description |
|---|---|
| HPTA | HP Time Alarm<br>Least significant bits. This register can be programmed only when HP time alarm is disabled (HPTA_EN bit is not set). |

## 57.9.9 SNVS_LP Lock Register (SNVS_LPLR)

The SNVS_LP Lock Register contains lock bits for the SNVS_LP registers.

Address: 20C_C000h base + 34h offset = 20C_C034h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | Reserved | | | Reserved | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | Reserved | | | | | | - | - | - | - | GPR_HL | MC_HL | - | - | - | - |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

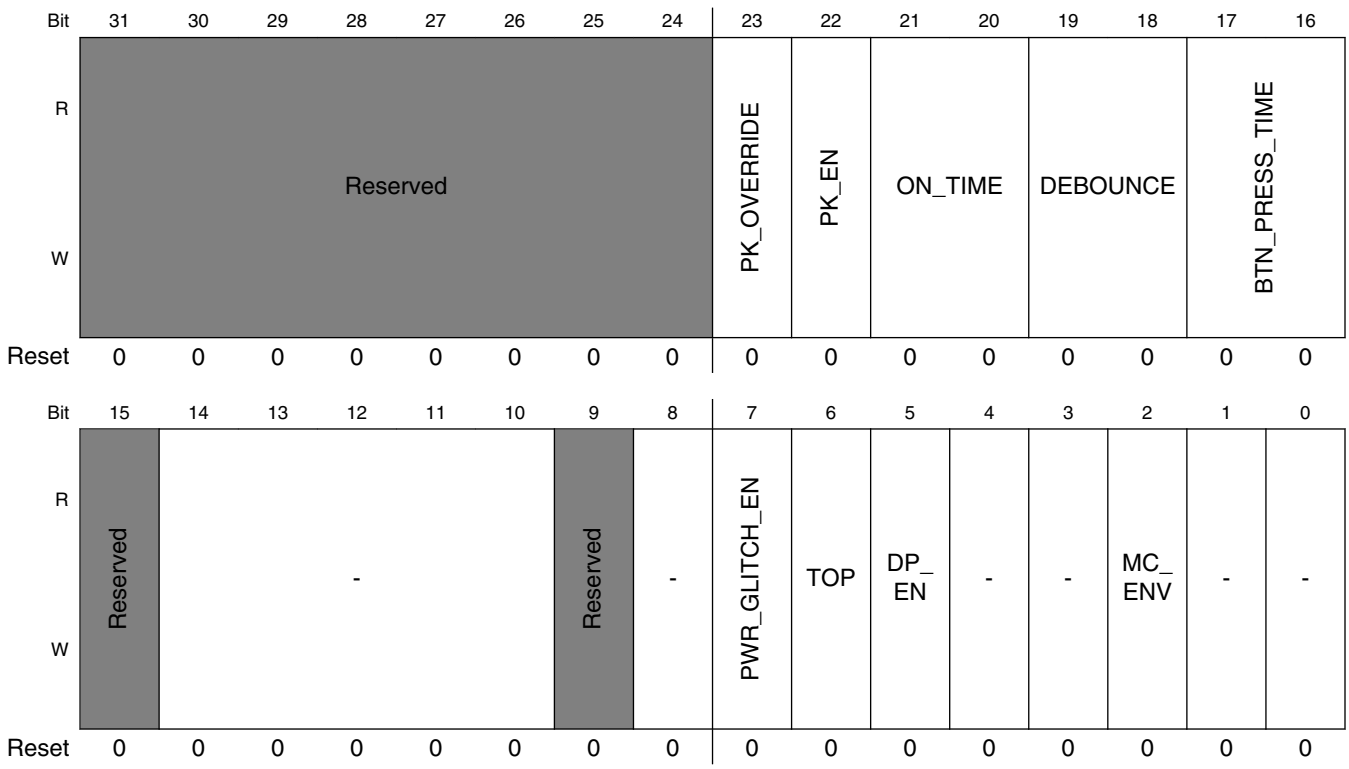
## SNVS_LPLR field descriptions

| Field | Description |
|---|---|
| 31–29<br>- | This field is reserved. |
| 23–10<br>- | This field is reserved. |
| 9<br>- | This field is reserved. |
| 8<br>- | This field is reserved. |
| 7<br>- | This field is reserved. |
| 6<br>- | This field is reserved. |
| 5<br>GPR_HL | General Purpose Register Hard Lock<br>When set, prevents any writes to the GPR. Once set, this bit can only be reset by the LP POR.<br>0 Write access is allowed.<br>1 Write access is not allowed. |
| 4<br>MC_HL | Monotonic Counter Hard Lock<br>When set, prevents any writes (increments) to the MC Registers and MC_ENV bit. Once set, this bit can only be reset by the LP POR.<br>0 Write access (increment) is allowed.<br>1 Write access (increment) is not allowed. |
| 3<br>- | This field is reserved. |
| 2<br>- | This field is reserved. |
| 1<br>- | This field is reserved. |
| 0<br>- | This field is reserved. |

## 57.9.10 SNVS_LP Control Register (SNVS_LPCR)

The SNVS_LP Control Register contains various control bits of the LP section of SNVS.

Address: 20C_C000h base + 38h offset = 20C_C038h




**SNVS_LPCR field descriptions**

| Field | Description |
|---|---|
| 31–24<br>- | This field is reserved. |
| 23<br>PK_OVERRIDE | PMIC On Request Override. The value written to PK_OVERRIDE will be asserted on output signal snvs_lp_pk_override. That signal is used to override the IOMUX control for the PMIC I/O pad. |
| 22<br>PK_EN | PMIC On Request Enable. The value written to PK_EN will be asserted on output signal snvs_lp_pk_en. That signal is used to turn off the pullup/pulldown circuitry in the PMIC I/O pad. |
| 21–20<br>ON_TIME | The ON_TIME field is used to configure the period of time after BTN is asserted before pmic_en_b is asserted to turn on the SoCpower.<br>00: 500msec off->on transition time<br>01: 50msec off->on transition time<br>10: 100msec off->on transition time<br>11: 0msec off->on transition time |

*Table continues on the next page...*

## SNVS_LPCR field descriptions (continued)

| Field | Description |
|---|---|
| 19–18<br>DEBOUNCE | This field configures the amount of debounce time for the BTN input signal.<br>00: 50msec debounce<br>01: 100msec debounce<br>10: 500msec debounce<br>11: 0msec debounce |
| 17–16<br>BTN_PRESS_TIME | Button press time out values for PMIC Logic.<br>00 : 5 secs<br>01 : 10 secs<br>10 : 15 secs<br>11 : long press disabled (pmic_en_b will not be asserted regardlessof how long BTN is asserted) |
| 15<br>- | This field is reserved. |
| 14–10<br>- | This field is reserved. |
| 9<br>- | This field is reserved. |
| 8<br>- | This field is reserved. |
| 7<br>PWR_GLITCH_EN | By default the detection of a power glitch does not cause the pmic_en_b signal to be asserted. Setting the Power Glitch Enable bit to 1 enables the power glitch event for the PMIC.<br>0 - disabled<br>1 - enabled |
| 6<br>TOP | Turn off System Power<br>Asserting this bit causes a signal to be sent to the Power Management IC to turn off the system power. This bit will clear once power is off. This bit is only valid when the Dumb PMIC is enabled.<br>0 Leave system power on.<br>1 Turn off system power. |
| 5<br>DP_EN | Dumb PMIC Enabled<br>When set, software can control the system power. When cleared, the system requires a Smart PMIC to automatically turn power off.<br>0 Smart PMIC enabled.<br>1 Dumb PMIC enabled. |
| 4<br>- | This field is reserved. |
| 3<br>- | This field is reserved. |
| 2<br>MC_ENV | Monotonic Counter Enable and Valid<br>When set, the MC can be incremented (by write transaction to the LPSMCMR or LPSMCLR). This bit cannot be changed once MC_SL or MC_HL bit is set.<br>0 MC is disabled or invalid.<br>1 MC is enabled and valid. |

*Table continues on the next page...*

## SNVS_LPCR field descriptions (continued)

| Field | Description |
|---|---|
| 1<br>- | This field is reserved. |
| 0<br>- | This field is reserved. |

## 57.9.11 SNVS_LP Status Register (SNVS_LPSR)

The SNVS_LP Status Register reflects the internal state and behavior of the SNVS_LP.

Address: 20C_C000h base + 4Ch offset = 20C_C04Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | - | - | Reserved | | | | | | | | | - | Reserved | SPO | EO | - |
| W | | | | | | | | | | | | | | w1c | w1c | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | Reserved | | | | | - | - | - | - | - | - | - | - | MCR | - | - |
| W | | | | | | | | | | | | | | w1c | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

## SNVS_LPSR field descriptions

| Field | Description |
|---|---|
| 31<br>- | This field is reserved. |
| 30<br>- | This field is reserved. |
| 29–21<br>- | This field is reserved. |
| 20<br>- | This field is reserved. |
| 19<br>- | This field is reserved. |
| 18<br>SPO | Set Power Off<br>The SPO bit is set when the set_pwr_off_irq interrupt is triggered, which happens when software writes a 1 to the TOP bit in the LPCR or when the power button is pressed longer than the configured debounce time. Writing to the SPO bit will clear the set_pwr_off_irq interrupt.<br>0 Emergency Off was not detected.<br>1 Emergency Off was detected.. |
| 17<br>EO | Emergency Off<br>This bit is set when a power off is requested.<br>0 Emergency off was not detected.<br>1 Emergency off was detected. |
| 16<br>- | This field is reserved. |
| 15–11<br>- | This field is reserved. |
| 10<br>- | This field is reserved. |
| 9<br>- | This field is reserved. |
| 8<br>- | This field is reserved. |
| 7<br>- | This field is reserved. |
| 6<br>- | This field is reserved. |
| 5<br>- | This field is reserved. |
| 4<br>- | This field is reserved. |
| 3<br>- | This field is reserved. |
| 2<br>MCR | Monotonic Counter Rollover.<br>0 MC has not reached its maximum value.<br>1 MC has reached its maximum value. |

*Table continues on the next page...*

**SNVS_LPSR field descriptions (continued)**

| Field | Description |
|---|---|
| 1<br>- | This field is reserved. |
| 0<br>- | This field is reserved. |

## 57.9.12 SNVS_LP Secure Monotonic Counter MSB Register (SNVS_LPSMCMR)

The SNVS_LP Secure Monotonic Counter MSB Register contains the monotonic counter era bits and the most significant 16 bits of the monotonic counter. The monotonic counter is incremented by one if there is a write command to the LPSMCMR or LPSMCLR register.

Address: 20C_C000h base + 5Ch offset = 20C_C05Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | MC_ERA_BITS | | | | | | | | | | | | | | | | MON_COUNTER | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

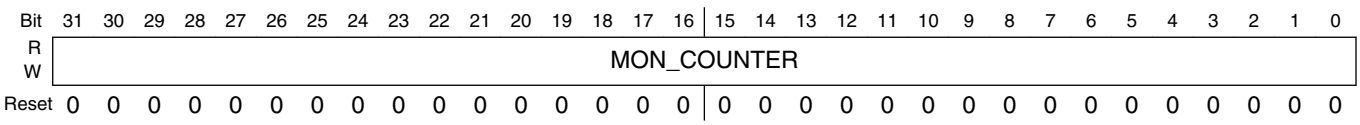
**SNVS_LPSMCMR field descriptions**

| Field | Description |
|---|---|
| 31–16<br>MC_ERA_BITS | Monotonic Counter Era Bits<br>These bits are inputs to the module and typically connect to fuses. |
| MON_COUNTER | Monotonic Counter Most Significant 16 Bits<br>The MC is incremented by one when:<br>• A write transaction to the LPSMCMR or LPSMCLR register is detected.<br>• The MC_ENV bit is set.<br>• MC_SL and MC_HL bits are not set. |

## 57.9.13 SNVS_LP Secure Monotonic Counter LSB Register (SNVS_LPSMCLR)

The SNVS_LP Secure Monotonic Counter LSB Register contains the 32 least significant bits of the monotonic counter. The MC is incremented by one if there is a write command to the LPSMCMR or LPSMCLR register.

Address: 20C_C000h base + 60h offset = 20C_C060h



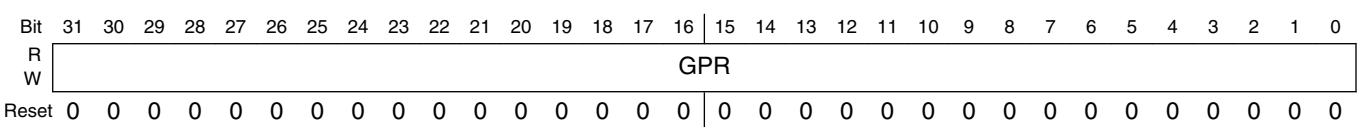

**SNVS_LPSMCLR field descriptions**

| Field | Description |
|---|---|
| MON_COUNTER | Monotonic Counter bits<br>The MC is incremented by one when:<br>• A write transaction to the LPSMCMR or LPSMCLR Register is detected.<br>• The MC_ENV bit is set.<br>• MC_SL and MC_HL bits are not set. |

## 57.9.14 SNVS_LP General Purpose Register (SNVS_LPGPR)

The SNVS_LP General Purpose Register is a read/write register located in the low power domain, which can be used by any application for retaining data during an SoC power-down mode.

Address: 20C_C000h base + 68h offset = 20C_C068h




**SNVS_LPGPR field descriptions**

| Field | Description |
|---|---|
| GPR | General Purpose Register<br>When GPR_SL or GPR_HL bit is set, the register cannot be programmed. |

## 57.9.15 SNVS_HP Version ID Register 1 (SNVS_HPVIDR1)

The SNVS_HP Version ID Register 1 is a read-only register that contains the current version of the SNVS . The version consists of a module ID, a major version number, and a minor version number.

Address: 20C_C000h base + BF8h offset = 20C_CBF8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | IP_ID | | | | | | | | | | | | | | | | MAJOR_REV | | | | | | | | MINOR_REV | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SNVS_HPVIDR1 field descriptions**

| Field | Description |
|---|---|
| 31–16<br>IP_ID | SNVS block ID |
| 15–8<br>MAJOR_REV | SNVS block major version number |
| MINOR_REV | SNVS block minor version number |

## 57.9.16 SNVS_HP Version ID Register 2 (SNVS_HPVIDR2)

The SNVS_HP Version ID Register 2 is a read-only register that indicates the current version of the SNVS. Version ID register 2 consists of the following fields: integration options, ECO revision, and configuration options.

Address: 20C_C000h base + BFCh offset = 20C_CBFCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | IP_ERA | | | | | | | | INTG_OPT | | | | | | | | ECO_REV | | | | | | | | CONFIG_OPT | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SNVS_HPVIDR2 field descriptions**

| Field | Description |
|---|---|
| 31–24<br>IP_ERA | Era of the IP design<br><br>00h - Era 1 or 2 |

*Table continues on the next page...*

## SNVS_HPVIDR2 field descriptions (continued)

| Field | Description |
|---|---|
| | 03h - Era 3<br>04h - Era 4<br>05h - Era 5 |
| 23–16<br>INTG_OPT | SNVS Integration Option |
| 15–8<br>ECO_REV | SNVS ECO Revision |
| CONFIG_OPT | SNVS Configuration Option |