58.4.3.1 Software Controlled Ownership Ending

The ROI bits will be automatically cleared when the master that owns the PRR access right clears (write) the RAR bits (Table 2).

It will then end the ownership of the PRR.

58.4.4 The Un-owned State

During the time when the peripheral is un-owned (i.e the ROI field contains all 0's), all masters have full access to it (RAR bits can then be modified by a master if ROI[1:0] = 2'b0).

In such cases it is necessary for software to ensure any necessary coherency in the resource, there is no hardware protection.

58.5 SPBA Memory Map/Register Definition

The SPBA control registers (Peripheral Right Registers) are mapped as a virtual shared peripheral.

SPBA can support up to 31 shared peripherals. Each of them has its own Peripheral Right Register (PRR) accessible within the SPBA memory-mapped registers, and consists of the Requesting Master Owner, the Resource Owner ID and the Resource Access Right fields.

SPBA memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
203_C000	Peripheral Rights Register (SPBA_PRR0)	32	R/W	0000_0007h	58.5.1/5017
203_C004	Peripheral Rights Register (SPBA_PRR1)	32	R/W	0000_0007h	58.5.1/5017
203_C008	Peripheral Rights Register (SPBA_PRR2)	32	R/W	0000_0007h	58.5.1/5017
203_C00C	Peripheral Rights Register (SPBA_PRR3)	32	R/W	0000_0007h	58.5.1/5017
203_C010	Peripheral Rights Register (SPBA_PRR4)	32	R/W	0000_0007h	58.5.1/5017
203_C014	Peripheral Rights Register (SPBA_PRR5)	32	R/W	0000_0007h	58.5.1/5017
203_C018	Peripheral Rights Register (SPBA_PRR6)	32	R/W	0000_0007h	58.5.1/5017
203_C01C	Peripheral Rights Register (SPBA_PRR7)	32	R/W	0000_0007h	58.5.1/5017
203_C020	Peripheral Rights Register (SPBA_PRR8)	32	R/W	0000_0007h	58.5.1/5017

Table continues on the next page...

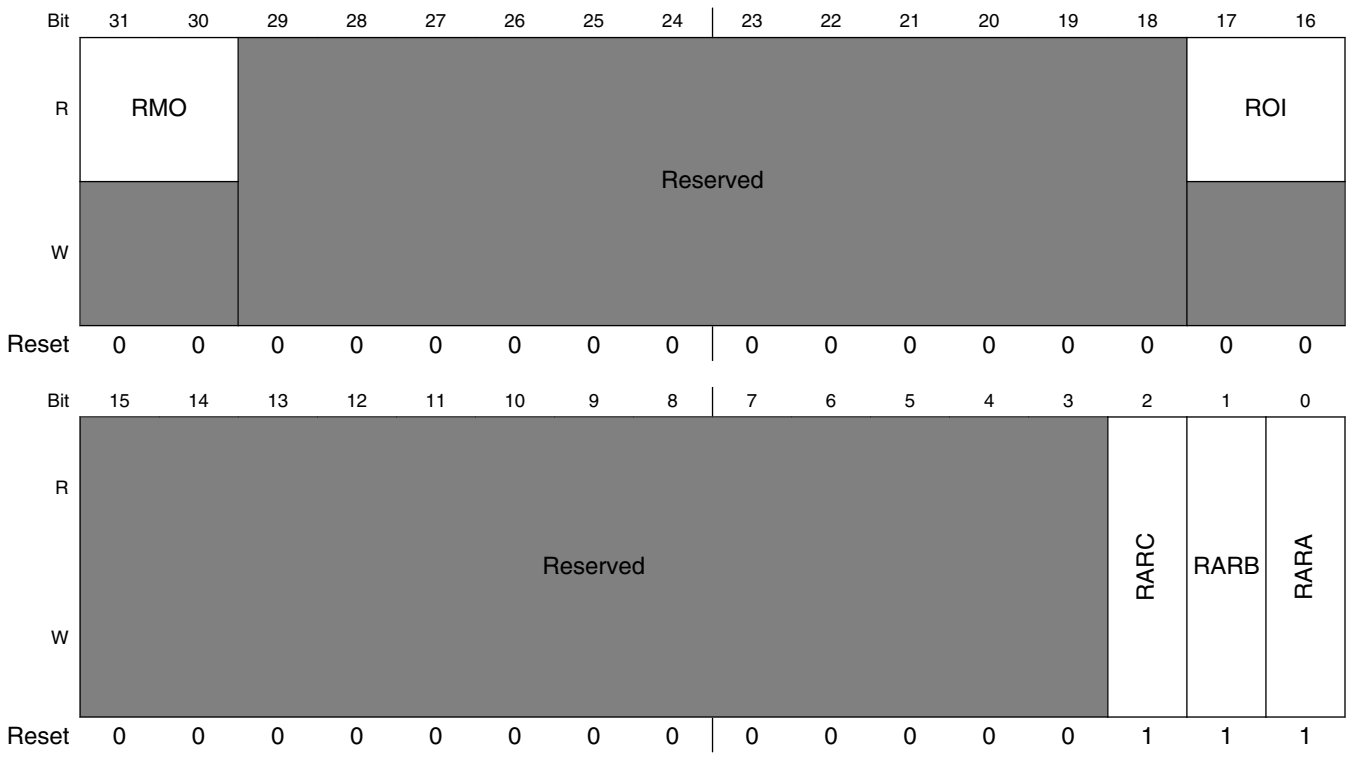
SPBA memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
203_C024	Peripheral Rights Register (SPBA_PRR9)	32	R/W	0000_0007h	58.5.1/5017
203_C028	Peripheral Rights Register (SPBA_PRR10)	32	R/W	0000_0007h	58.5.1/5017
203_C02C	Peripheral Rights Register (SPBA_PRR11)	32	R/W	0000_0007h	58.5.1/5017
203_C030	Peripheral Rights Register (SPBA_PRR12)	32	R/W	0000_0007h	58.5.1/5017
203_C034	Peripheral Rights Register (SPBA_PRR13)	32	R/W	0000_0007h	58.5.1/5017
203_C038	Peripheral Rights Register (SPBA_PRR14)	32	R/W	0000_0007h	58.5.1/5017
203_C03C	Peripheral Rights Register (SPBA_PRR15)	32	R/W	0000_0007h	58.5.1/5017
203_C040	Peripheral Rights Register (SPBA_PRR16)	32	R/W	0000_0007h	58.5.1/5017
203_C044	Peripheral Rights Register (SPBA_PRR17)	32	R/W	0000_0007h	58.5.1/5017
203_C048	Peripheral Rights Register (SPBA_PRR18)	32	R/W	0000_0007h	58.5.1/5017
203_C04C	Peripheral Rights Register (SPBA_PRR19)	32	R/W	0000_0007h	58.5.1/5017
203_C050	Peripheral Rights Register (SPBA_PRR20)	32	R/W	0000_0007h	58.5.1/5017
203_C054	Peripheral Rights Register (SPBA_PRR21)	32	R/W	0000_0007h	58.5.1/5017
203_C058	Peripheral Rights Register (SPBA_PRR22)	32	R/W	0000_0007h	58.5.1/5017
203_C05C	Peripheral Rights Register (SPBA_PRR23)	32	R/W	0000_0007h	58.5.1/5017
203_C060	Peripheral Rights Register (SPBA_PRR24)	32	R/W	0000_0007h	58.5.1/5017
203_C064	Peripheral Rights Register (SPBA_PRR25)	32	R/W	0000_0007h	58.5.1/5017
203_C068	Peripheral Rights Register (SPBA_PRR26)	32	R/W	0000_0007h	58.5.1/5017
203_C06C	Peripheral Rights Register (SPBA_PRR27)	32	R/W	0000_0007h	58.5.1/5017
203_C070	Peripheral Rights Register (SPBA_PRR28)	32	R/W	0000_0007h	58.5.1/5017
203_C074	Peripheral Rights Register (SPBA_PRR29)	32	R/W	0000_0007h	58.5.1/5017
203_C078	Peripheral Rights Register (SPBA_PRR30)	32	R/W	0000_0007h	58.5.1/5017
203_C07C	Peripheral Rights Register (SPBA_PRR31)	32	R/W	0000_0007h	58.5.1/5017

58.5.1 Peripheral Rights Register (SPBA_PRR*n*)

This register controls master ownership and access for a peripheral.

Address: 203_C000h base + 0h offset + (4d × i), where i=0d to 31d



SPBA_PRR*n* field descriptions

Field	Description
31–30 RMO	Requesting Master Owner. This 2-bit register field indicates if the corresponding resource is owned by the requesting master or not. This register is reset to 2'b0 if ROI = 2'b0. 00 **UNOWNED** — The resource is unowned. 01 Reserved. 10 **ANOTHER_MASTER** — The resource is owned by another master. 11 **REQUESTING_MASTER** — The resource is owned by the requesting master.
29–18 -	This field is reserved. Reserved
17–16 ROI	Resource Owner ID. This field indicates which master (one at a time) can access to the PRR for rights modification. This is a read-only register. After reset, ROI bits are cleared ("00" -> un-owned resource).

Table continues on the next page...

SPBA_PRR*n* field descriptions (continued)

Field	Description
	A master performing a write access to the an un-owned PRR will get its ID automatically written into ROI, while modifying RARx bits. It can then read back the RMO, RAR, ROI bits to make sure RMO returns the right value, ROI bits contain its ID and RARx bits are correctly asserted. Then no other master (whom ID is different from the one stored in ROI) will be able to modify RAR fields. Owner master of a peripheral can assert its dead_owner signal, or write 1'b0 in the RARx to release the ownership (ROI[1:0] reset to 2'b0). 00 **UNOWNED** — Unowned resource. 01 **MASTER_A** — The resource is owned by master A port. 10 **MASTER_B** — The resource is owned by master B port. 11 **MASTER_C** — The resource is owned by master C port.
15–3 -	This field is reserved. Reserved
2 RARC	Resource Access Right. Control and Status bit for master C. This field indicates whether master C can access the peripheral. From 0 up to 3 masters can have permission to access a resource (all the master can be granted on a peripheral, but only one access at a time will be granted by SPBA). 0 **PROHIBITED** — Access to peripheral is not allowed. 1 **ALLOWED** — Access to peripheral is granted.
1 RARB	Resource Access Right. Control and Status bit for master B. This field indicates whether master B can access the peripheral. From 0 up to 3 masters can have permission to access a resource (all the master can be granted on a peripheral, but only one access at a time will be granted by SPBA). 0 **PROHIBITED** — Access to peripheral is not allowed. 1 **ALLOWED** — Access to peripheral is granted.
0 RARA	Resource Access Right. Control and Status bit for master A. This field indicates whether master A can access the peripheral. From 0 up to 3 masters can have permission to access a resource (all the master can be granted on a peripheral, but only one access at a time will be granted by SPBA). 0 **PROHIBITED** — Access to peripheral is not allowed. 1 **ALLOWED** — Access to peripheral is granted.