

CSI2IPU Memory Map/Register Definition

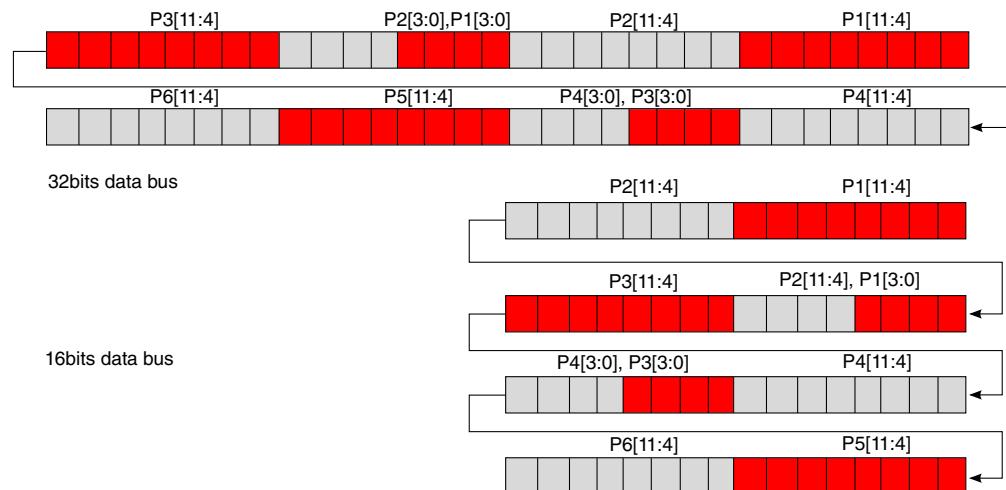


Figure 19-19. RAW-12 data reception

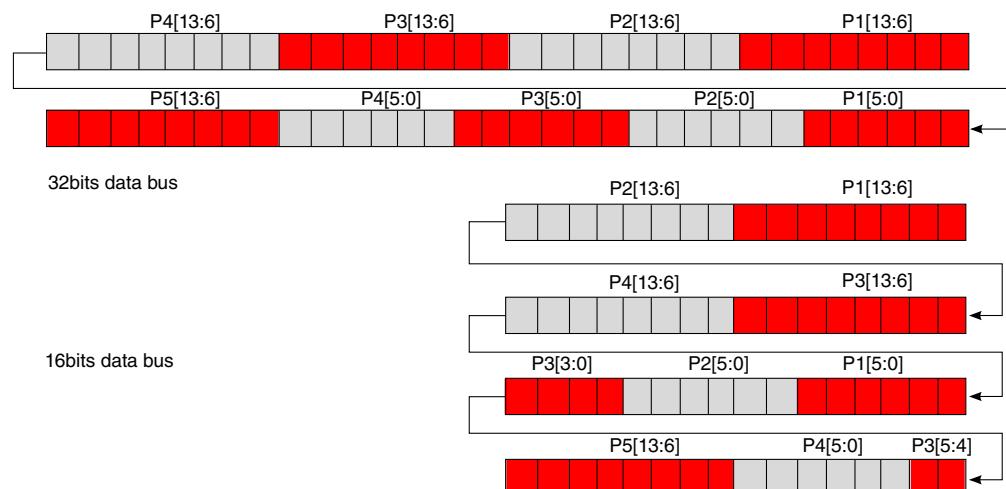


Figure 19-20. RAW-14 data reception

19.5 CSI2IPU Memory Map/Register Definition

CSI2IPU memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
21D_CF00	CSI 2 IPU Gasket Software Reset (CSI2IPU_SW_RST)	32	R/W	0000_0000h	19.5.1/955

19.5.1 CSI 2 IPU Gasket Software Reset (CSI2IPU_SW_RST)

This register describes the IPU interface signals.

Address: 21D_C000h base + F00h offset = 21D_CF00h

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

CSI2IPU_SW_RST field descriptions

Field	Description
31–4 Reserved	This read-only field is reserved and always has the value 0.
3 RGB444_FM	rgb444 mode selection 0 {4'h0,r4b4g4} 1 {r4,1'b0,g4,2'b00,b4,1'b0}
2 YUV422_8BIT_ FM	YUV422 8-bit mode selection 0 YUYV 1 UYVY
1 CLK_SEL	Clock mode selection 0 Gated Mode 1 Non-Gated Mode
0 SW_RST	Software Reset 0 Software Reset Disable 1 Software Reset Enable

