

## 42.5 HSI Memory Map/Register Definition

This section includes the module memory map and detailed descriptions of all registers.

### NOTE

The HSI registers are 32 bits wide and only support 32-bit access.

### NOTE

The term reset refers to power-on-reset. It will be specified whenever the software reset value differs from the power-on-reset.

### MIPI\_HSI memory map

| Absolute address (hex) | Register name  | Width (in bits) | Access | Reset value | Section/page                 |
|------------------------|--|-----------------|--------|-------------|------------------------------|
| 220_8000               | HSI Control Register (MIPI_HSI_CTRL)   | 32              | R/W    | C800_0000h  | <a href="#">42.5.1/3688</a>  |
| 220_8004               | HSI Tx Config Register (MIPI_HSI_TX_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.2/3690</a>  |
| 220_8008               | HSI Rx Config Register (MIPI_HSI_RX_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.3/3692</a>  |
| 220_800C               | HSI Capability Register (MIPI_HSI_CAP)   | 32              | R      | 0007_1FFFh  | <a href="#">42.5.4/3695</a>  |
| 220_8010               | HSI Tx Water Mark Level 0 Register (MIPI_HSI_TX_WML0)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.5/3696</a>  |
| 220_8014               | HSI Tx Water Mark Level 1 Register (MIPI_HSI_TX_TML1)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.6/3698</a>  |
| 220_8018               | HSI Tx Arbiter Priority 0 Register (MIPI_HSI_TX_ARB_PRI0)                          | 32              | R/W    | 0000_0000h  | <a href="#">42.5.7/3700</a>  |
| 220_801C               | HSI Tx Arbiter Priority 1 Register (MIPI_HSI_TX_ARB_PRI1)                          | 32              | R/W    | 0000_0000h  | <a href="#">42.5.8/3702</a>  |
| 220_8020               | HSI Line Status Register (MIPI_HSI_LINE_ST)  | 32              | R      | 0000_0000h  | <a href="#">42.5.9/3705</a>  |
| 220_8024               | HSI ID Bits Register (MIPI_HSI_ID_BIT)   | 32              | R/W    | 0000_0000h  | <a href="#">42.5.10/3707</a> |
| 220_8028               | Tx and Rx Fifo Threshold Configuration Register (MIPI_HSI_FIFO_THR_CONF)           | 32              | R/W    | 0000_0000h  | <a href="#">42.5.11/3708</a> |
| 220_802C               | Tx and Rx Channel Soft Reset Register (MIPI_HSI_CH_SFTRST)                         | 32              | W      | 0000_0000h  | <a href="#">42.5.12/3711</a> |
| 220_8030               | HSI Interrupt Status Register (MIPI_HSI_IRQSTAT)                                   | 32              | R/W    | 0000_0000h  | <a href="#">42.5.13/3713</a> |
| 220_8034               | HSI Interrupt Status Enable Register (MIPI_HSI_IRQSTAT_EN)                         | 32              | R/W    | 0000_0000h  | <a href="#">42.5.14/3715</a> |
| 220_8038               | HSI Interrupt Signal Enable Register (MIPI_HSI_IRQSIG_EN)                          | 32              | R/W    | 0000_0000h  | <a href="#">42.5.15/3717</a> |
| 220_803C               | HSI FIFO Threshold Interrupt Status Register (MIPI_HSI_FIFO_THR_IRQSTAT)           | 32              | R      | FFFF_0000h  | <a href="#">42.5.16/3719</a> |
| 220_8040               | HSI FIFO Threshold Interrupt Status Enable Register (MIPI_HSI_FIFO_THR_IRQSTAT_EN) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.17/3722</a> |

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**MIPI\_HSI memory map (continued)**

| Absolute address (hex) | Register name   | Width (in bits) | Access | Reset value | Section/page                  |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 220_8044               | HSI FIFO Threshold Interrupt Signal Enable Register (MIPI_HSI_FIFO THR IRQSIG_EN) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.18/ 3725</a> |
| 220_8050               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH0_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8054               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH1_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8058               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH2_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_805C               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH3_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8060               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH4_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8064               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH5_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8068               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH6_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_806C               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH7_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8070               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH8_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8074               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH9_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8078               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH10_DP)                             | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_807C               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH11_DP)                             | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8080               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH12_DP)                             | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8084               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH13_DP)                             | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8088               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH14_DP)                             | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_808C               | Tx Channel n Data Port Register (MIPI_HSI_TX_CH15_DP)                             | 32              | R/W    | 0000_0000h  | <a href="#">42.5.19/ 3728</a> |
| 220_8090               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH0_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_8094               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH1_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_8098               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH2_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_809C               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH3_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80A0               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH4_DP)                              | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |

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**MIPI\_HSI memory map (continued)**

| Absolute address (hex) | Register name  | Width (in bits) | Access | Reset value | Section/page                  |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 220_80A4               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH5_DP)                 | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80A8               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH6_DP)                 | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80AC               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH7_DP)                 | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80B0               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH8_DP)                 | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80B4               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH9_DP)                 | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80B8               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH10_DP)                | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80BC               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH11_DP)                | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80C0               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH12_DP)                | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80C4               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH13_DP)                | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80C8               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH14_DP)                | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80CC               | Rx Channel n Data Port Register (MIPI_HSI_RX_CH15_DP)                | 32              | R/W    | 0000_0000h  | <a href="#">42.5.20/ 3729</a> |
| 220_80D0               | HSI Error Interrupt Status Register (MIPI_HSI_ERR_IRQSTAT)           | 32              | R      | 0000_0000h  | <a href="#">42.5.21/ 3730</a> |
| 220_80D4               | HSI Error Interrupt Status Enable Register (MIPI_HSI_ERR_IRQSTAT_EN) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.22/ 3733</a> |
| 220_80D8               | HSI Error Interrupt Signal Enable Register (MIPI_HSI_ERR_IRQSIG_EN)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.23/ 3735</a> |
| 220_80DC               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA0_CONF)        | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/ 3737</a> |
| 220_80E0               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA1_CONF)        | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/ 3737</a> |
| 220_80E4               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA2_CONF)        | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/ 3737</a> |
| 220_80E8               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA3_CONF)        | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/ 3737</a> |
| 220_80EC               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA4_CONF)        | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/ 3737</a> |
| 220_80F0               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA5_CONF)        | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/ 3737</a> |
| 220_80F4               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA6_CONF)        | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/ 3737</a> |
| 220_80F8               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA7_CONF)        | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/ 3737</a> |

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**MIPI\_HSI memory map (continued)**

| Absolute address (hex) | Register name  | Width (in bits) | Access | Reset value | Section/page                 |
|------------------------|--|-----------------|--------|-------------|------------------------------|
| 220_80FC               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA8_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/3737</a> |
| 220_8100               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA9_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/3737</a> |
| 220_8104               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA10_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/3737</a> |
| 220_8108               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA11_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/3737</a> |
| 220_810C               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA12_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/3737</a> |
| 220_8110               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA13_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/3737</a> |
| 220_8114               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA14_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/3737</a> |
| 220_8118               | Tx DMA Channel n Configuration Register (MIPI_HSI_TDMA15_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.24/3737</a> |
| 220_811C               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA0_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8120               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA1_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8124               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA2_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8128               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA3_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_812C               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA4_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8130               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA5_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8134               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA6_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8138               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA7_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_813C               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA8_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8140               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA9_CONF)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8144               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA10_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8148               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA11_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_814C               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA12_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |
| 220_8150               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA13_CONF) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/3738</a> |

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**MIPI\_HSI memory map (continued)**

| Absolute address (hex) | Register name  | Width (in bits) | Access | Reset value | Section/page                  |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 220_8154               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA14_CONF)     | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/ 3738</a> |
| 220_8158               | Rx DMA Channel n Configuration Register (MIPI_HSI_RDMA15_CONF)     | 32              | R/W    | 0000_0000h  | <a href="#">42.5.25/ 3738</a> |
| 220_815C               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA0_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8160               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA1_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8164               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA2_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8168               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA3_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_816C               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA4_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8170               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA5_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8174               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA6_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8178               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA7_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_817C               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA8_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8180               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA9_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8184               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA10_STA_ADDR) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8188               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA11_STA_ADDR) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_818C               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA12_STA_ADDR) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8190               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA13_STA_ADDR) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8194               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA14_STA_ADDR) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_8198               | Tx DMA Channel n Start Address Register (MIPI_HSI_TDMA15_STA_ADDR) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.26/ 3739</a> |
| 220_819C               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA0_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81A0               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA1_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81A4               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA2_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81A8               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA3_STA_ADDR)  | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |

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**MIPI\_HSI memory map (continued)**

| Absolute address (hex) | Register name   | Width (in bits) | Access | Reset value | Section/page                  |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 220_81AC               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA4_STA_ADDR)       | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81B0               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA5_STA_ADDR)       | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81B4               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA6_STA_ADDR)       | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81B8               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA7_STA_ADDR)       | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81BC               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA8_STA_ADDR)       | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81C0               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA9_STA_ADDR)       | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81C4               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA10_STA_ADDR)      | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81C8               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA11_STA_ADDR)      | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81CC               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA12_STA_ADDR)      | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81D0               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA13_STA_ADDR)      | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81D4               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA14_STA_ADDR)      | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81D8               | Rx DMA Channel n Start Address Register (MIPI_HSI_RDMA15_STA_ADDR)      | 32              | R/W    | 0000_0000h  | <a href="#">42.5.27/ 3739</a> |
| 220_81DC               | DMA Interrupt Status Register (MIPI_HSI_DMA_IRQSTAT)                    | 32              | R      | 0000_0000h  | <a href="#">42.5.28/ 3740</a> |
| 220_81E0               | DMA Interrupt Enable Register (MIPI_HSI_DMA_IRQSTAT_EN)                 | 32              | R/W    | 0000_0000h  | <a href="#">42.5.29/ 3742</a> |
| 220_81E4               | DMA Interrupt Status Signal Enable Register (MIPI_HSI_DMA IRQSIG_EN)    | 32              | R/W    | 0000_0000h  | <a href="#">42.5.30/ 3744</a> |
| 220_81E8               | DMA Error Interrupt Status Register (MIPI_HSI_DMA_ERR_IRQSTAT)          | 32              | R      | 0000_0000h  | <a href="#">42.5.31/ 3747</a> |
| 220_81EC               | DMA Error Interrupt Enable Register (MIPI_HSI_DMA_ERR_IRQSTAT_EN)       | 32              | R/W    | 0000_0000h  | <a href="#">42.5.32/ 3749</a> |
| 220_81F0               | DMA Error Interrupt Signal Enable Register (MIPI_HSI_DMA_ERR_IRQSIG_EN) | 32              | R/W    | 0000_0000h  | <a href="#">42.5.33/ 3751</a> |
| 220_81F4               | DMA Single Request Enable Register (MIPI_HSI_DMA_SINGLE_REQ_EN)         | 32              | R      | 0000_0000h  | <a href="#">42.5.34/ 3754</a> |
| 220_8200               | Tx Fifo Size Configuration Register 0 (MIPI_HSI_TX_FIFO_SIZE_CONF0)     | 32              | R/W    | 5555_5555h  | <a href="#">42.5.35/ 3756</a> |
| 220_8204               | Tx Fifo Size Configuration Register 1 (MIPI_HSI_TX_FIFO_SIZE_CONF1)     | 32              | R/W    | 5555_5555h  | <a href="#">42.5.36/ 3759</a> |
| 220_8208               | Rx Fifo Size Configuration Register 0 (MIPI_HSI_RX_FIFO_SIZE_CONF0)     | 32              | R/W    | 5555_5555h  | <a href="#">42.5.37/ 3762</a> |

Table continues on the next page...

**MIPI\_HSI memory map (continued)**

| Absolute address (hex) | Register name   | Width (in bits) | Access | Reset value | Section/page                 |
|------------------------|---|-----------------|--------|-------------|------------------------------|
| 220_820C               | Rx Fifo Size Configuration Register 1 (MIPI_HSI_RX_FIFO_SIZE_CONF1) | 32              | R/W    | 5555_5555h  | <a href="#">42.5.38/3765</a> |
| 220_8210               | Tx Fifo Status Register (MIPI_HSI_TX_FIFO_STAT)                     | 32              | R      | 5555_5555h  | <a href="#">42.5.39/3768</a> |
| 220_8214               | Rx Fifo Status Register (MIPI_HSI_RX_FIFO_STAT)                     | 32              | R      | 5555_5555h  | <a href="#">42.5.40/3770</a> |
| 220_8228               | Ahb Master Config Register (MIPI_HSI_AHB_MASTER_CONF)               | 32              | R/W    | 0000_0180h  | <a href="#">42.5.41/3772</a> |
| 220_822C               | TX Break Length Register (MIPI_HSI_TX_BREAK_LEN)                    | 32              | R/W    | 0000_0025h  | <a href="#">42.5.42/3773</a> |

**42.5.1 HSI Control Register (MIPI\_HSI\_CTRL)**

This register contains module soft reset, clock gating, clock divisor and so on.

Address: 220\_8000h base + 0h offset = 220\_8000h

| Bit   | 31       | 30      | 29              | 28 | 27               | 26         | 25 | 24 | 23                | 22 | 21 | 20       | 19             | 18 | 17 | 16 |
|-------|----------|---------|-----------------|----|------------------|------------|----|----|-------------------|----|----|----------|----------------|----|----|----|
| R     | SFTRST   | CLKGATE | Reserved        |    | DMA_DISABLE      | RX_DLY_SEL |    |    | RX_FRAME_BRST_CNT |    |    |          |                |    |    |    |
| W     |          |         |                 |    |                  |            |    |    |                   |    |    |          |                |    |    |    |
| Reset | 1        | 1       | 0               | 0  | 1                | 0          | 0  | 0  | 0                 | 0  | 0  | 0        | 0              | 0  | 0  | 0  |
| Bit   | 15       | 14      | 13              | 12 | 11               | 10         | 9  | 8  | 7                 | 6  | 5  | 4        | 3              | 2  | 1  | 0  |
| R     | Reserved |         | RX_TAIL_BIT_CNT |    | DATA_TIMEOUT_CNT |            |    |    | Reserved          |    |    | TX_BREAK | TX_CLK_DIVISOR |    |    |    |
| W     |          |         |                 |    |                  |            |    |    |                   |    |    |          |                |    |    |    |
| Reset | 0        | 0       | 0               | 0  | 0                | 0          | 0  | 0  | 0                 | 0  | 0  | 0        | 0              | 0  | 0  | 0  |

**MIPI\_HSI\_CTRL field descriptions**

| Field      | Description  |
|------------|--|
| 31 SFTRST  | Set this bit to zero to enable normal HSI operation. Set this bit to one (default) to disable clocking with the HSI and hold it in its reset (lowest power) state. This bit can be turned on and then off to reset the HSI block to its default state. |
| 30 CLKGATE | This bit must be set to zero for normal operation. When set to one it gates off the clocks to the block.   |

*Table continues on the next page...*

**MIPI\_HSI\_CTRL field descriptions (continued)**

| Field                      | Description  |
|----------------------------|--|
| 29–28<br>Reserved          | This field is reserved.<br>Reserved, always set to zero.   |
| 27<br>DMA_DISABLE          | This bit must be set to zero for any DMA operation. When set to one it disable all the DMA channels.   |
| 26–24<br>RX_DLY_SEL        | These values denote the tap delay values for reception of data and flag.<br><br>000 0ns ;<br>001 1ns ;<br>010 2ns ;<br>011 3ns ;<br>100 4ns ;<br>101 5ns ;<br>110 6ns ;<br>111 7ns ;   |
| 23–16<br>RX_FRAME_BRST_CNT | This value is to limit the continuous Frame transmission count in Pipelined Data flow.<br><br>The Receiver Frame Burst counter shall be able to support upto 256 frames of continuous transfer.<br><br>7'h00 256 frames transmission count is set.<br>7'h01 1 frames transmission count is set.<br>7'h02 2 frames transmission count is set.<br>7'hff 255 frames transmission count is set.  |
| 15–14<br>Reserved          | This field is reserved.<br>Reserved.   |
| 13–12<br>RX_TAIL_BIT_CNT   | The value determines the length of the Tailing bit counter.<br><br>The receiver shall start Receiver Tailing bit counter after<br>the nth frame programmed in Rx Frame Burst counter is received.<br><br>The receiver shall then drive ready to logic one if the receiver<br>Tailing-bit counter has completed with no errors detected,<br>and the receiver has enough room for at least one new frame.<br><br>00 800-> tx_refclk<br>01 400-> tx_refclk<br>10 200-> tx_refclk<br>11 100-> tx_refclk  |
| 11–8<br>DATA_TIMEOUT_CNT   | This value determines the interval by which DATA timeouts are detected.<br><br>This data timeout counter logic is used only for Receive operations.<br><br>The counter should start counting when data in any of the RX channel fifo is less than the threshold value<br>and<br>resets to zero when there is a threshold reached interrupt from any of the RX buffers.<br><br>The counter value should be zero, when RX fifo is empty. An interrupt will be asserted to the host driver,<br>when the counter value reaches the data timeout counter value.<br><br>1110 HSI Tx Clock x 2 ^ 27<br>0001 HSI Tx Clock x 2 ^ 14<br>0000 HSI Tx Clock x 2 ^ 13 |

*Table continues on the next page...*

**MIPI\_HSI\_CTRL field descriptions (continued)**

| Field           | Description  |
|-----------------|--|
| 7–5<br>Reserved | This field is reserved.<br>Reserved.   |
| 4<br>TX_BREAK   | Setting this bit to one trigger a transmission break at HSI Tx. Once this bit is set to one, the HSI controller will send a series zeros on HSI_TX_DATA port according to the tx break count. It will be automatically cleared, when the send is finished.   |
| TX_CLK_DIVISOR  | This register holds the divisor of the base clock (tx_refclk) frequency for HSI Tx clock (internal clock used to drive Transmitter interface).<br><br>1000 tx_refclk divided by 256<br>0111 tx_refclk divided by 128<br>0110 tx_refclk divided by 64<br>0101 tx_refclk divided by 32<br>0100 tx_refclk divided by 16<br>0011 tx_refclk divided by 8<br>0010 tx_refclk divided by 4<br>0001 tx_refclk divided by 2<br>0000 tx_refclk divided by 1 |

**42.5.2 HSI Tx Config Register (MIPI\_HSI\_TX\_CONF)**

This register contains the configurations of tx channel enable/disable, tx wakeup and tx trans mode.

Address: 220\_8000h base + 4h offset = 220\_8004h

| Bit   | 31       | 30      | 29      | 28      | 27          | 26      | 25     | 24     | 23       | 22     | 21     | 20     | 19     | 18         | 17     | 16     |
|-------|----------|---------|---------|---------|-------------|---------|--------|--------|----------|--------|--------|--------|--------|------------|--------|--------|
| R     | CH15_EN  | CH14_EN | CH13_EN | CH12_EN | CH11_EN     | CH10_EN | CH9_EN | CH8_EN | CH7_EN   | CH6_EN | CH5_EN | CH4_EN | CH3_EN | CH2_EN     | CH1_EN | CH0_EN |
| W     | 0        | 0       | 0       | 0       | 0           | 0       | 0      | 0      | 0        | 0      | 0      | 0      | 0      | 0          | 0      | 0      |
| Reset | 0        | 0       | 0       | 0       | 0           | 0       | 0      | 0      | 0        | 0      | 0      | 0      | 0      | 0          | 0      | 0      |
| Bit   | 15       | 14      | 13      | 12      | 11          | 10      | 9      | 8      | 7        | 6      | 5      | 4      | 3      | 2          | 1      | 0      |
| R     | Reserved |         |         |         | TIMEOUT_CNT |         |        |        | Reserved |        |        |        | WAKEUP | TRANS_MODE |        |        |
| W     | 0        | 0       | 0       | 0       | 0           | 0       | 0      | 0      | 0        | 0      | 0      | 0      | 0      | 0          | 0      | 0      |
| Reset | 0        | 0       | 0       | 0       | 0           | 0       | 0      | 0      | 0        | 0      | 0      | 0      | 0      | 0          | 0      | 0      |

**MIPI\_HSI\_TX\_CONF field descriptions**

| Field               | Description  |
|---------------------|--|
| 31<br>CH15_EN       | 1 Tx Ch15 is Enabled.<br>0 Tx Ch15 is Disabled.  |
| 30<br>CH14_EN       | 1 Tx Ch14 is Enabled.<br>0 Tx Ch14 is Disabled.  |
| 29<br>CH13_EN       | 1 Tx Ch13 is Enabled.<br>0 Tx Ch13 is Disabled.  |
| 28<br>CH12_EN       | 1 Tx Ch12 is Enabled.<br>0 Tx Ch12 is Disabled.  |
| 27<br>CH11_EN       | 1 Tx Ch11 is Enabled.<br>0 Tx Ch11 is Disabled.  |
| 26<br>CH10_EN       | 1 Tx Ch10 is Enabled.<br>0 Tx Ch10 is Disabled.  |
| 25<br>CH9_EN        | 1 Tx Ch9 is Enabled.<br>0 Tx Ch9 is Disabled.  |
| 24<br>CH8_EN        | 1 Tx Ch8 is Enabled.<br>0 Tx Ch8 is Disabled.  |
| 23<br>CH7_EN        | 1 Tx Ch7 is Enabled.<br>0 Tx Ch7 is Disabled.  |
| 22<br>CH6_EN        | 1 Tx Ch6 is Enabled.<br>0 Tx Ch6 is Disabled.  |
| 21<br>CH5_EN        | 1 Tx Ch5 is Enabled.<br>0 Tx Ch5 is Disabled.  |
| 20<br>CH4_EN        | 1 Tx Ch4 is Enabled.<br>0 Tx Ch4 is Disabled.  |
| 19<br>CH3_EN        | 1 Tx Ch3 is Enabled.<br>0 Tx Ch3 is Disabled.  |
| 18<br>CH2_EN        | 1 Tx Ch2 is Enabled.<br>0 Tx Ch2 is Disabled.  |
| 17<br>CH1_EN        | 1 Tx Ch1 is Enabled.<br>0 Tx Ch1 is Disabled.  |
| 16<br>CH0_EN        | 1 Tx Ch0 is Enabled.<br>0 Tx Ch0 is Disabled.  |
| 15–12<br>Reserved   | This field is reserved.<br>Reserved.   |
| 11–8<br>TIMEOUT_CNT | 0000 tx timeout value $2^{14}$ tx_refclk<br>0001 tx timeout value $2^{15}$ tx_refclk<br>0010 tx timeout value $2^{16}$ tx_refclk<br>0011 tx timeout value $2^{17}$ tx_refclk<br>1110 tx timeout value $2^{28}$ tx_refclk<br>1111 tx timeout value $2^{29}$ tx_refclk |
| 7–2<br>Reserved     | This field is reserved.<br>Reserved.   |
| 1<br>WAKEUP         | When this bit gets set to one, HSI transmitter sends HSI_TX_WAKE signal to Rx of other device. For a transmit operation this bit should be one.  |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_CONF field descriptions (continued)**

| Field      | Description  |  |
|------------|--|--|
|            | 0 Transmitter is in Sleep State<br>1 Transmitter is in Wakeup State. |  |
| TRANS_MODE | 0 Stream Transmission Mode<br>1 Frame Transmission Mode              |  |

**42.5.3 HSI Rx Config Register (MIPI\_HSI\_RX\_CONF)**

This register contains the configurations of rx channel enable/disable, rx wakeup and rx trans mode, rx data flow.

Address: 220\_8000h base + 8h offset = 220\_8008h

| Bit   | 31       | 30          | 29      | 28      | 27      | 26      | 25     | 24     | 23     | 22       | 21     | 20              | 19       | 18     | 17     | 16        |
|-------|----------|-------------|---------|---------|---------|---------|--------|--------|--------|----------|--------|-----------------|----------|--------|--------|-----------|
| R     | CH15_EN  | CH14_EN     | CH13_EN | CH12_EN | CH11_EN | CH10_EN | CH9_EN | CH8_EN | CH7_EN | CH6_EN   | CH5_EN | CH4_EN          | CH3_EN   | CH2_EN | CH1_EN | CH0_EN    |
| W     |          |             |         |         |         |         |        |        |        |          |        |                 |          |        |        |           |
| Reset | 0        | 0           | 0       | 0       | 0       | 0       | 0      | 0      | 0      | 0        | 0      | 0               | 0        | 0      | 0      | 0         |
| Bit   | 15       | 14          | 13      | 12      | 11      | 10      | 9      | 8      | 7      | 6        | 5      | 4               | 3        | 2      | 1      | 0         |
| R     | Reserved | TIMEOUT_CNT |         |         |         |         |        |        |        | Reserved |        | TAIL_BIT_CNT_EN | REC_MODE | WAKE   |        | DATA_FLOW |
| W     |          |             |         |         |         |         |        |        |        |          |        |                 |          |        |        |           |
| Reset | 0        | 0           | 0       | 0       | 0       | 0       | 0      | 0      | 0      | 0        | 0      | 0               | 0        | 0      | 0      | 0         |

**MIPI\_HSI\_RX\_CONF field descriptions**

| Field         | Description                                     |  |
|---------------|---|--|
| 31<br>CH15_EN | 1 Rx Ch15 is Enabled.<br>0 Rx Ch15 is Disabled. |  |
| 30<br>CH14_EN | 1 Rx Ch14 is Enabled.<br>0 Rx Ch14 is Disabled. |  |

Table continues on the next page...

**MIPI\_HSI\_RX\_CONF field descriptions (continued)**

| Field               | Description  |
|---------------------|--|
| 29<br>CH13_EN       | 1 Rx Ch13 is Enabled.<br>0 Rx Ch13 is Disabled.  |
| 28<br>CH12_EN       | 1 Rx Ch12 is Enabled.<br>0 Rx Ch12 is Disabled.  |
| 27<br>CH11_EN       | 1 Rx Ch11 is Enabled.<br>0 Rx Ch11 is Disabled.  |
| 26<br>CH10_EN       | 1 Rx Ch10 is Enabled.<br>0 Rx Ch10 is Disabled.  |
| 25<br>CH9_EN        | 1 Rx Ch9 is Enabled.<br>0 Rx Ch9 is Disabled.  |
| 24<br>CH8_EN        | 1 Rx Ch8 is Enabled.<br>0 Rx Ch8 is Disabled.  |
| 23<br>CH7_EN        | 1 Rx Ch7 is Enabled.<br>0 Rx Ch7 is Disabled.  |
| 22<br>CH6_EN        | 1 Rx Ch6 is Enabled.<br>0 Rx Ch6 is Disabled.  |
| 21<br>CH5_EN        | 1 Rx Ch5 is Enabled.<br>0 Rx Ch5 is Disabled.  |
| 20<br>CH4_EN        | 1 Rx Ch4 is Enabled.<br>0 Rx Ch4 is Disabled.  |
| 19<br>CH3_EN        | 1 Rx Ch3 is Enabled.<br>0 Rx Ch3 is Disabled.  |
| 18<br>CH2_EN        | 1 Rx Ch2 is Enabled.<br>0 Rx Ch2 is Disabled.  |
| 17<br>CH1_EN        | 1 Rx Ch1 is Enabled.<br>0 Rx Ch1 is Disabled.  |
| 16<br>CH0_EN        | 1 Rx Ch0 is Enabled.<br>0 Rx Ch0 is Disabled.  |
| 15<br>Reserved      | This field is reserved.<br>Reserved.   |
| 14–8<br>TIMEOUT_CNT | Receive Frame Timeout Counter:<br><br>The counter shall be started when the first bit of the Frame has been found. The counter shall be stopped once the receiver has received the correct number of bits for a Frame. If the counter expires before Frame reception is completed, the receiver will signal to the protocol layer that it has found an incomplete Frame and asserts Rx Error Interrupt.<br><br>7'h0 14800 ---> tx_refclk<br>7'h1 16400 ---> tx_refclk<br>7'h2 18000 ---> tx_refclk<br>7'h4 19600 ---> tx_refclk<br>7'h8 21200 ---> tx_refclk<br>7'h10 22800 ---> tx_refclk<br>7'h20 24400 ---> tx_refclk |

*Table continues on the next page...*

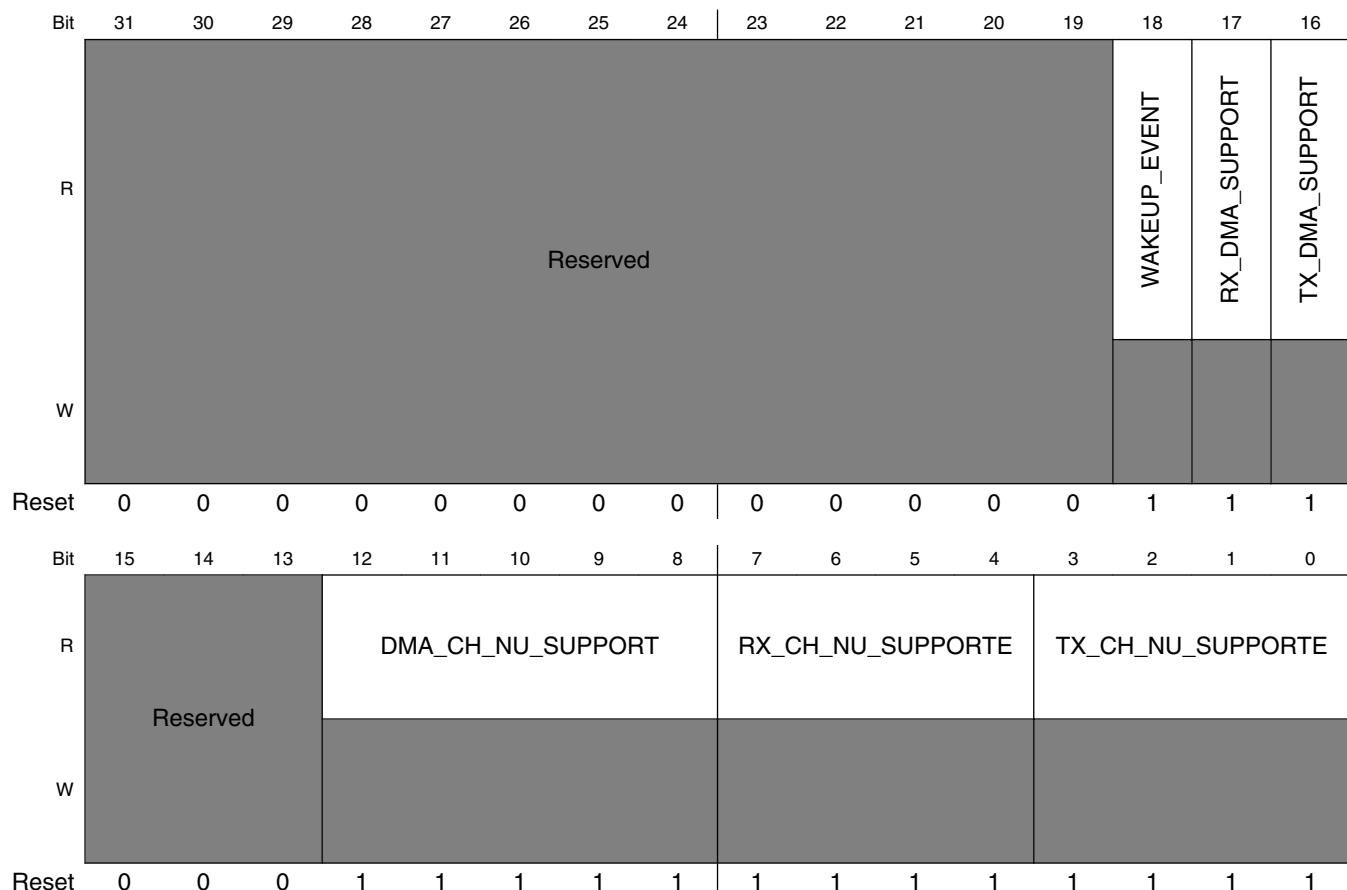
**MIPI\_HSI\_RX\_CONF field descriptions (continued)**

| Field                    | Description   |
|--------------------------|---|
|                          | 7'h40 26000 ---> tx_refclk  |
| 7–5<br>Reserved          | This field is reserved.<br>Reserved.  |
| 4<br>TAIL_BIT_CNT_<br>EN | 0 Tailing bit counter disable<br>1 Tailing bit counter Enable   |
| 3<br>REC_MODE            | 0 Stream Receive Mode<br>1 Frame Receive Mode   |
| 2<br>WAKE                | 0 Receiver is in Sleep State<br>1 Receiver is in Wakeup State   |
| DATA_FLOW                | 00 Synchronized Data Flow<br>01 Pipelined Data Flow<br>10 Receiver Real-time Data Flow<br>11 Reserved |

## 42.5.4 HSI Capability Register (MIPI\_HSI\_CAP)

This register contains the HSI controller Capability information.

Address: 220\_8000h base + Ch offset = 220\_800Ch



**MIPI\_HSI\_CAP field descriptions**

| Field                | Description   |
|----------------------|---|
| 31–19<br>Reserved    | This field is reserved.<br>Reserved.                            |
| 18<br>WAKEUP_EVENT   | 0 Wakeup Event is supported<br>1 Wakeup Event is not supported. |
| 17<br>RX_DMA_SUPPORT | 1 DMA is supported.<br>0 Not supported                          |
| 16<br>TX_DMA_SUPPORT | 1 DMA is supported.<br>0 Not supported                          |

*Table continues on the next page...*

**MIPI\_HSI\_CAP field descriptions (continued)**

| Field                         | Description  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| 15–13<br>Reserved             | This field is reserved.<br>Reserved.   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 12–8<br>DMA_CH_NU_<br>SUPPORT | 00000 1 DMA supported<br>00001 2 DMA supported<br>00010 3 DMA supported<br>00011 4 DMA supported<br>00100 5 DMA supported<br>00101 6 DMA supported<br>11110 31 DMA supported<br>11111 32 DMA supported |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 7–4<br>RX_CH_NU_<br>SUPPORT   | 0000 1 Rx channel supported<br>0001 2 Rx channels supported<br>1111 16 Rx channels supported   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| TX_CH_NU_<br>SUPPORT          | 0000 1 Tx channel supported<br>0001 2 Tx channels supported<br>1111 16 Tx channels supported   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**42.5.5 HSI Tx Water Mark Level 0 Register (MIPI\_HSI\_TX\_WML0)**

This register contains HSI controller Tx channel Water Mark Level information.

Address: 220\_8000h base + 10h offset = 220\_8010h

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24   | 23 | 22 | 21   | 20 | 19 | 18   | 17 | 16 | 15   | 14 | 13 | 12  | 11 | 10 | 9   | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|----|----|----|------|----|----|------|----|----|------|----|----|------|----|----|------|----|----|-----|----|----|-----|---|---|---|---|---|---|---|---|---|
| R     | CH15 |    |    |    | CH14 |    |    | CH13 |    |    | CH12 |    |    | CH11 |    |    | CH10 |    |    | CH9 |    |    | CH8 |   |   |   |   |   |   |   |   |   |
| W     | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0    | 0  | 0  | 0    | 0  | 0  | 0    | 0  | 0  | 0    | 0  | 0  | 0   | 0  | 0  | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0    | 0  | 0  | 0    | 0  | 0  | 0    | 0  | 0  | 0    | 0  | 0  | 0   | 0  | 0  | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |

**MIPI\_HSI\_TX\_WML0 field descriptions**

| Field         | Description   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| 31–28<br>CH15 | This value denotes the WML of Tx Channel 15.<br>When > 1010 Reserved<br><br>0000 1<br>0001 2<br>0010 4<br>1000 256<br>1001 512<br>1010 1024 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 27–24<br>CH14 | This value denotes the WML of Tx Channel 14.<br>When > 1010 reserved  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_WML0 field descriptions (continued)**

| Field         | Description  |
|---------------|--|
|               | 0000 1<br>0001 2<br>0010 4<br>1000 256<br>1001 512<br>1010 1024  |
| 23–20<br>CH13 | <p>This value denotes the WML of Tx Channel 13.</p> <p>When &gt; 1010 reserved</p> <p>0000 1<br/>0001 2<br/>0010 4<br/>1000 256<br/>1001 512<br/>1010 1024</p> |
| 19–16<br>CH12 | <p>This value denotes the WML of Tx Channel 12.</p> <p>When &gt; 1010 reserved</p> <p>0000 1<br/>0001 2<br/>0010 4<br/>1000 256<br/>1001 512<br/>1010 1024</p> |
| 15–12<br>CH11 | <p>This value denotes the WML of Tx Channel 11.</p> <p>When &gt; 1010 reserved</p> <p>0000 1<br/>0001 2<br/>0010 4<br/>1000 256<br/>1001 512<br/>1010 1024</p> |
| 11–8<br>CH10  | <p>This value denotes the WML of Tx Channel 10.</p> <p>When &gt; 1010 reserved</p> <p>0000 1<br/>0001 2<br/>0010 4<br/>1000 256<br/>1001 512<br/>1010 1024</p> |
| 7–4<br>CH9    | <p>This value denotes the WML of Tx Channel 9.</p> <p>When &gt; 1010 reserved</p> <p>0000 1<br/>0001 2</p>   |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_WML0 field descriptions (continued)**

| Field | Description  |
|-------|--|
|       | 0010 4<br>1000 256<br>1001 512<br>1010 1024  |
| CH8   | This value denotes the WML of Tx Channel 8.<br>When > 1010 reserved<br>0000 1<br>0001 2<br>0010 4<br>1000 256<br>1001 512<br>1010 1024 |

**42.5.6 HSI Tx Water Mark Level 1 Register (MIPI\_HSI\_TX\_TML1)**

This register contains HSI controller Tx channel Water Mark Level information.

This register contains HSI controller Tx channel bandwidth information.

Address: 220\_8000h base + 14h offset = 220\_8014h

| Bit   | 31  | 30 | 29 | 28 | 27  | 26 | 25 | 24  | 23 | 22 | 21  | 20 | 19 | 18 | 17 | 16  | 15 | 14 | 13  | 12 | 11 | 10  | 9 | 8 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|----|----|----|-----|----|----|-----|----|----|-----|----|----|----|----|-----|----|----|-----|----|----|-----|---|---|-----|---|---|---|---|---|---|---|
| R     | CH7 |    |    |    | CH6 |    |    | CH5 |    |    | CH4 |    |    |    |    | CH3 |    |    | CH2 |    |    | CH1 |   |   | CH0 |   |   |   |   |   |   |   |
| Reset | 0   | 0  | 0  | 0  | 0   | 0  | 0  | 0   | 0  | 0  | 0   | 0  | 0  | 0  | 0  | 0   | 0  | 0  | 0   | 0  | 0  | 0   | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0 | 0 |   |

**MIPI\_HSI\_TX\_TML1 field descriptions**

| Field        | Description  |
|--------------|--|
| 31–28<br>CH7 | This value denotes the WML of Tx Channel 7.<br>When > 1010 reserved<br>0000 1<br>0001 2<br>0010 4<br>1000 256<br>1001 512<br>1010 1024 |
| 27–24<br>CH6 | This value denotes the WML of Tx Channel 6.<br>When > 1010 reserved<br>0000 1<br>0001 2<br>0010 4<br>1000 256                          |

Table continues on the next page...

**MIPI\_HSI\_TX\_TML1 field descriptions (continued)**

| Field        | Description  |
|--------------|--|
|              | 1001 512<br>1010 1024  |
| 23–20<br>CH5 | This value denotes the WML of Tx Channel 5.<br>When > 1010 reserved<br><br>0000 1<br>0001 2<br>0010 4<br>1000 256<br>1001 512<br>1010 1024 |
| 19–16<br>CH4 | This value denotes the WML of Tx Channel 4.<br>When > 1010 reserved<br><br>0000 1<br>0001 2<br>0010 4<br>1000 256<br>1001 512<br>1010 1024 |
| 15–12<br>CH3 | This value denotes the WML of Tx Channel 3.<br>When > 1010 reserved<br><br>0000 1<br>0001 2<br>0010 4<br>1000 256<br>1001 512<br>1010 1024 |
| 11–8<br>CH2  | This value denotes the WML of Tx Channel 2.<br>When > 1010 reserved<br><br>0000 1<br>0001 2<br>0010 4<br>1000 256<br>1001 512<br>1010 1024 |
| 7–4<br>CH1   | This value denotes the WML of Tx Channel 1.<br>When > 1010 reserved<br><br>0000 1<br>0001 2<br>0010 4<br>1000 256                          |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_TML1 field descriptions (continued)**

| Field | Description  |
|-------|--|
|       | 1001 512<br>1010 1024  |
| CH0   | This value denotes the WML of Tx Channel 0.<br>When > 1010 reserved<br><br>0000 1<br>0001 2<br>0010 4<br>1000 256<br>1001 512<br>1010 1024 |

### 42.5.7 HSI Tx Arbiter Priority 0 Register (MIPI\_HSI\_TX\_ARB\_PRI0)

This is HSI Tx Arbiter Priority Register.

Address: 220\_8000h base + 18h offset = 220\_8018h

| Bit   | 31  | 30 | 29  | 28 | 27  | 26 | 25  | 24 | 23  | 22 | 21  | 20 | 19  | 18 | 17  | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|----|-----|----|-----|----|-----|----|-----|----|-----|----|-----|----|-----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R     | CH7 |    | CH6 |    | CH5 |    | CH4 |    | CH3 |    | CH2 |    | CH1 |    | CH0 |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset | 0   | 0  | 0   | 0  | 0   | 0  | 0   | 0  | 0   | 0  | 0   | 0  | 0   | 0  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |

**MIPI\_HSI\_TX\_ARB\_PRI0 field descriptions**

| Field        | Description   |
|--------------|---|
| 31–28<br>CH7 | This value denotes the priority of Tx Channel 7.<br>When > 1010 reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority<br>1110 15th priority<br>1111 16th priority |
| 27–24<br>CH6 | This value denotes the priority of Tx Channel 6.<br>When > 1010 reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority   |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_ARB\_PRI0 field descriptions (continued)**

| Field        | Description   |
|--------------|---|
|              | 1110 15th priority<br>1111 16th priority  |
| 23–20<br>CH5 | This value denotes the priority of Tx Channel 5.<br>When > 1010 reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority<br>1110 15th priority<br>1111 16th priority |
| 19–16<br>CH4 | This value denotes the priority of Tx Channel 4.<br>When > 1010 reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority<br>1110 15th priority<br>1111 16th priority |
| 15–12<br>CH3 | This value denotes the priority of Tx Channel 3.<br>When > 1010 reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority<br>1110 15th priority<br>1111 16th priority |
| 11–8<br>CH2  | This value denotes the priority of Tx Channel 2.<br>When > 1010 reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority<br>1110 15th priority<br>1111 16th priority |
| 7–4<br>CH1   | This value denotes the priority of Tx Channel 1.<br>When > 1010 reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority   |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_ARB\_PRI0 field descriptions (continued)**

| Field | Description   |
|-------|---|
|       | 1110 15th priority<br>1111 16th priority  |
| CH0   | This value denotes the priority of Tx Channel 0.<br>When > 1010 reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority<br>1110 15th priority<br>1111 16th priority |

### 42.5.8 HSI Tx Arbiter Priority 1 Register (MIPI\_HSI\_TX\_ARB\_PRI1)

Address: 220\_8000h base + 1Ch offset = 220\_801Ch

| Bit | 31   | 30 | 29   | 28 | 27   | 26 | 25   | 24 | 23   | 22 | 21   | 20 | 19  | 18 | 17  | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|------|----|------|----|------|----|------|----|------|----|------|----|-----|----|-----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R   | CH15 |    | CH14 |    | CH13 |    | CH12 |    | CH11 |    | CH10 |    | CH9 |    | CH8 |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| W   | 0    | 0  | 0    | 0  | 0    | 0  | 0    | 0  | 0    | 0  | 0    | 0  | 0   | 0  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |

**MIPI\_HSI\_TX\_ARB\_PRI1 field descriptions**

| Field         | Description  |
|---------------|--|
| 31–28<br>CH15 | This value denotes the priority of Tx Channel 15.<br>When > 1010 Reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority<br>1110 15th priority<br>1111 16th priority |
| 27–24<br>CH14 | This value denotes the priority of Tx Channel 14.<br>When > 1010 reserved<br><br>0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority<br>1110 15th priority<br>1111 16th priority |
| 23–20<br>CH13 | This value denotes the priority of Tx Channel 13.<br>When > 1010 reserved  |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_ARB\_PRI1 field descriptions (continued)**

| Field         | Description   |
|---------------|---|
|               | 0000 1st priority<br>0001 2nd priority<br>0010 3rd priority<br>1101 14th priority<br>1110 15th priority<br>1111 16th priority   |
| 19–16<br>CH12 | <p>This value denotes the priority of Tx Channel 12.</p> <p>When &gt; 1010 reserved</p> <p>0000 1st priority<br/>0001 2nd priority<br/>0010 3rd priority<br/>1101 14th priority<br/>1110 15th priority<br/>1111 16th priority</p> |
| 15–12<br>CH11 | <p>This value denotes the priority of Tx Channel 11.</p> <p>When &gt; 1010 reserved</p> <p>0000 1st priority<br/>0001 2nd priority<br/>0010 3rd priority<br/>1101 14th priority<br/>1110 15th priority<br/>1111 16th priority</p> |
| 11–8<br>CH10  | <p>This value denotes the priority of Tx Channel 10.</p> <p>When &gt; 1010 reserved</p> <p>0000 1st priority<br/>0001 2nd priority<br/>0010 3rd priority<br/>1101 14th priority<br/>1110 15th priority<br/>1111 16th priority</p> |
| 7–4<br>CH9    | <p>This value denotes the priority of Tx Channel 9.</p> <p>When &gt; 1010 reserved</p> <p>0000 1st priority<br/>0001 2nd priority<br/>0010 3rd priority<br/>1101 14th priority<br/>1110 15th priority<br/>1111 16th priority</p>  |
| CH8           | <p>This value denotes the priority of Tx Channel 8.</p> <p>When &gt; 1010 reserved</p> <p>0000 1st priority<br/>0001 2nd priority</p>   |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_ARB\_PRI1 field descriptions (continued)**

| Field | Description        |
|-------|--------------------|
|       | 0010 3rd priority  |
|       | 1101 14th priority |
|       | 1110 15th priority |
|       | 1111 16th priority |

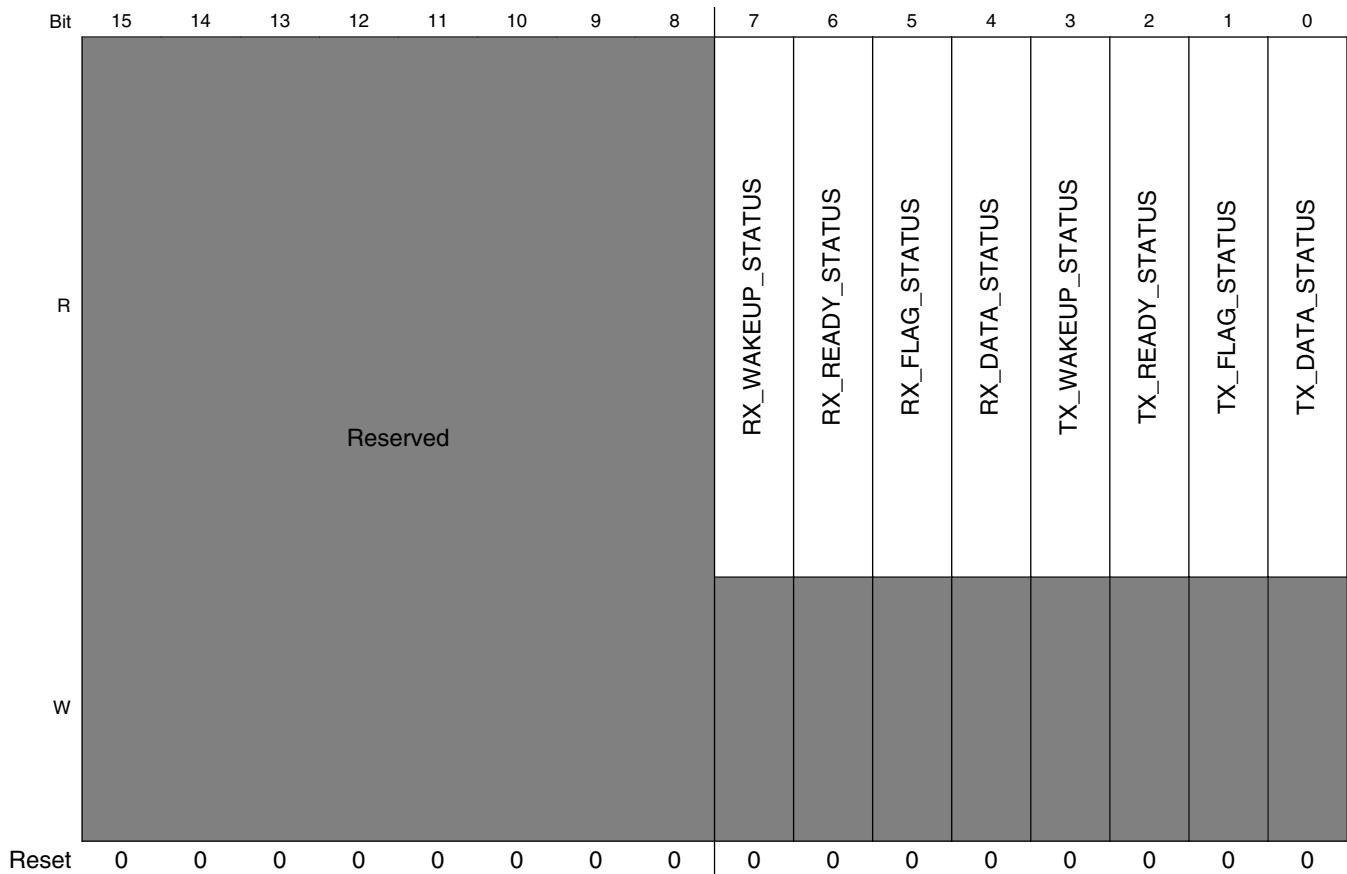
### 42.5.9 HSI Line Status Register (MIPI\_HSI\_LINE\_ST)

This register contains the HSI controller line status for debug.

Address: 220\_8000h base + 20h offset = 220\_8020h

| Bit      | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |  | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|----------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| R        |    |    |    |    |    |    |    |    |  |    |    |    |    |    |    |    |    |
|          |    |    |    |    |    |    |    |    |  |    |    |    |    |    |    |    |    |
|          |    |    |    |    |    |    |    |    |  |    |    |    |    |    |    |    |    |
|          |    |    |    |    |    |    |    |    |  |    |    |    |    |    |    |    |    |
|          |    |    |    |    |    |    |    |    |  |    |    |    |    |    |    |    |    |
| Reserved |    |    |    |    |    |    |    |    |  |    |    |    |    |    |    |    |    |
| W        |    |    |    |    |    |    |    |    |  |    |    |    |    |    |    |    |    |
| Reset    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

## HSI Memory Map/Register Definition



### MIPI\_HSI\_LINE\_ST field descriptions

| Field                 | Description  |
|-----------------------|--|
| 31–8<br>Reserved      | This field is reserved.<br>Reserved, always set to zero. |
| 7<br>RX_WAKEUP_STATUS | This field reflects the rx_wake pin(only for debug).     |
| 6<br>RX_READY_STATUS  | This field reflects the rx_rdy pin(only for debug).      |
| 5<br>RX_FLAG_STATUS   | This field reflects the rx_flag pin(only for debug).     |
| 4<br>RX_DATA_STATUS   | This field reflects the rx_data pin(only for debug).     |
| 3<br>TX_WAKEUP_STATUS | This field reflects the tx_wake pin(only for debug).     |
| 2<br>TX_READY_STATUS  | This field reflects the tx_ready pin(only for debug).    |

Table continues on the next page...

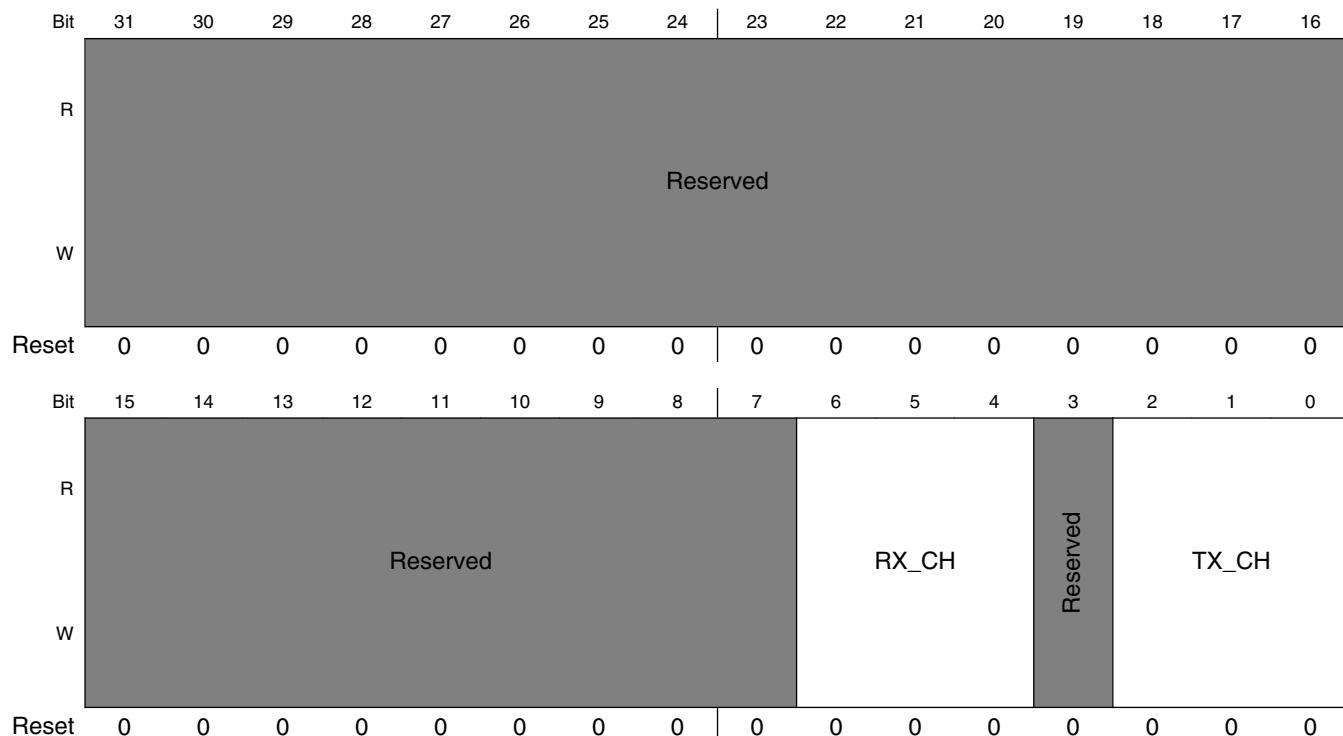
**MIPI\_HSI\_LINE\_ST field descriptions (continued)**

| Field               | Description  |
|---------------------|--|
| 1<br>TX_FLAG_STATUS | This field reflects the tx_flag pin(only for debug). |
| 0<br>TX_DATA_STATUS | This field reflects the tx_data pin(only for debug). |

**42.5.10 HSI ID Bits Register (MIPI\_HSI\_ID\_BIT)**

This register contains the configurations of tx channel enable/disable, , tx wakup and tx trans mode.

Address: 220\_8000h base + 24h offset = 220\_8024h

**MIPI\_HSI\_ID\_BIT field descriptions**

| Field            | Description  |
|------------------|--|
| 31–7<br>Reserved | This field is reserved.<br>Reserved, always set to zero.                                 |
| 6–4<br>RX_CH     | This bit sets the number of channel ID bits per frame or stream for a Receive operation. |

*Table continues on the next page...*

**MIPI\_HSI\_ID\_BIT field descriptions (continued)**

| Field      | Description   |
|------------|---|
|            | 0 0 bit<br>1 1 bit<br>2 2 bits<br>3 3 bits<br>4 4 bits  |
| 3 Reserved | This field is reserved.<br>Reserved, always set to zero.  |
| TX_CH      | This bit sets the number of channel ID bits per frame or stream for a transmit operation.<br><br>0 0 bit<br>1 1 bit<br>2 2 bits<br>3 3 bits<br>4 4 bits |

### 42.5.11 Tx and Rx Fifo Threshold Configuration Register (MIPI\_HSI\_FIFO\_THR\_CONF)

This register sets the threshold level for each Tx and Rx channel fifo

Address: 220\_8000h base + 28h offset = 220\_8028h

| Bit   | 31      | 30      | 29      | 28      | 27      | 26      | 25     | 24     | 23     | 22     | 21     | 20     | 19     | 18     | 17     | 16     |
|-------|---------|---------|---------|---------|---------|---------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| R     | TX_CH15 | TX_CH14 | TX_CH13 | TX_CH12 | TX_CH11 | TX_CH10 | TX_CH9 | TX_CH8 | TX_CH7 | TX_CH6 | TX_CH5 | TX_CH4 | TX_CH3 | TX_CH2 | TX_CH1 | TX_CH0 |
| W     |         |         |         |         |         |         |        |        |        |        |        |        |        |        |        |        |
| Reset | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
| Bit   | 15      | 14      | 13      | 12      | 11      | 10      | 9      | 8      | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| R     | RX_CH15 | RX_CH14 | RX_CH13 | RX_CH12 | RX_CH11 | RX_CH10 | RX_CH9 | RX_CH8 | RX_CH7 | RX_CH6 | RX_CH5 | RX_CH4 | RX_CH3 | RX_CH2 | RX_CH1 | RX_CH0 |
| W     |         |         |         |         |         |         |        |        |        |        |        |        |        |        |        |        |
| Reset | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      |

**MIPI\_HSI\_FIFO\_THR\_CONF field descriptions**

| Field      | Description  |
|------------|--|
| 31 TX_CH15 | 0 Half Empty (fifo size / 2)<br>1 Almost Empty (fifo size / 4) |

*Table continues on the next page...*

**MIPI\_HSI\_FIFO\_THR\_CONF field descriptions (continued)**

| Field         | Description |                                  |
|---------------|-------------|----------------------------------|
| 30<br>TX_CH14 | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 29<br>TX_CH13 | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 28<br>TX_CH12 | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 27<br>TX_CH11 | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 26<br>TX_CH10 | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 25<br>TX_CH9  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 24<br>TX_CH8  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 23<br>TX_CH7  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 22<br>TX_CH6  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 21<br>TX_CH5  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 20<br>TX_CH4  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 19<br>TX_CH3  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 18<br>TX_CH2  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 17<br>TX_CH1  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 16<br>TX_CH0  | 0           | Half Empty (fifo size / 2)       |
|               | 1           | Almost Empty (fifo size / 4)     |
| 15<br>RX_CH15 | 0           | Half Full (fifo size / 2)        |
|               | 1           | Almost Full (3/4th of fifo size) |
| 14<br>RX_CH14 | 0           | Half Full (fifo size / 2)        |
|               | 1           | Almost Full (3/4th of fifo size) |
| 13<br>RX_CH13 | 0           | Half Full (fifo size / 2)        |
|               | 1           | Almost Full (3/4th of fifo size) |
| 12<br>RX_CH12 | 0           | Half Full (fifo size / 2)        |
|               | 1           | Almost Full (3/4th of fifo size) |
| 11<br>RX_CH11 | 0           | Half Full (fifo size / 2)        |
|               | 1           | Almost Full (3/4th of fifo size) |
| 10<br>RX_CH10 | 0           | Half Full (fifo size / 2)        |
|               | 1           | Almost Full (3/4th of fifo size) |

Table continues on the next page...

**MIPI\_HSI\_FIFO\_THR\_CONF field descriptions (continued)**

| Field       | Description |                                  |
|-------------|-------------|----------------------------------|
| 9<br>RX_CH9 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |
| 8<br>RX_CH8 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |
| 7<br>RX_CH7 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |
| 6<br>RX_CH6 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |
| 5<br>RX_CH5 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |
| 4<br>RX_CH4 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |
| 3<br>RX_CH3 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |
| 2<br>RX_CH2 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |
| 1<br>RX_CH1 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |
| 0<br>RX_CH0 | 0           | Half Full (fifo size / 2)        |
|             | 1           | Almost Full (3/4th of fifo size) |

## 42.5.12 Tx and Rx Channel Soft Reset Register (MIPI\_HSI\_CH\_SFTRST)

This register is used to reset each Tx and Rx Channel

Address: 220\_8000h base + 2Ch offset = 220\_802Ch

| Bit   | 31      | 30      | 29      | 28      | 27      | 26      | 25     | 24     | 23     | 22     | 21     | 20     | 19     | 18     | 17     | 16     |
|-------|---------|---------|---------|---------|---------|---------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| R     |         |         |         |         |         |         |        |        |        |        |        |        |        |        |        |        |
| W     | TX_CH15 | TX_CH14 | TX_CH13 | TX_CH12 | TX_CH11 | TX_CH10 | TX_CH9 | TX_CH8 | TX_CH7 | TX_CH6 | TX_CH5 | TX_CH4 | TX_CH3 | TX_CH2 | TX_CH1 | TX_CH0 |
| Reset | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
| Bit   | 15      | 14      | 13      | 12      | 11      | 10      | 9      | 8      | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| R     |         |         |         |         |         |         |        |        |        |        |        |        |        |        |        |        |
| W     | RX_CH15 | RX_CH14 | RX_CH13 | RX_CH12 | RX_CH11 | RX_CH10 | RX_CH9 | RX_CH8 | RX_CH7 | RX_CH6 | RX_CH5 | RX_CH4 | RX_CH3 | RX_CH2 | RX_CH1 | RX_CH0 |
| Reset | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      |

### MIPI\_HSI\_CH\_SFTRST field descriptions

| Field         | Description  |
|---------------|--|
| 31<br>TX_CH15 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 15 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 30<br>TX_CH14 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 14 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 29<br>TX_CH13 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 13 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 28<br>TX_CH12 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 12 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 27<br>TX_CH11 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 11 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 26<br>TX_CH10 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 10 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 25<br>TX_CH9  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 9 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |

Table continues on the next page...

**MIPI\_HSI\_CH\_SFTRST field descriptions (continued)**

| Field         | Description  |
|---------------|--|
| 24<br>TX_CH8  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 8 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 23<br>TX_CH7  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 7 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 22<br>TX_CH6  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 6 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 21<br>TX_CH5  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 5 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 20<br>TX_CH4  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 4 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 19<br>TX_CH3  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 3 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 18<br>TX_CH2  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 2 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 17<br>TX_CH1  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 1 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 16<br>TX_CH0  | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Tx Channel 0 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 15<br>RX_CH15 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 15 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 14<br>RX_CH14 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 14 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 13<br>RX_CH13 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 13 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 12<br>RX_CH12 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 12 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 11<br>RX_CH11 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 11 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 10<br>RX_CH10 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 10 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 9<br>RX_CH9   | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 9 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 8<br>RX_CH8   | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 8 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 7<br>RX_CH7   | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 7 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 6<br>RX_CH6   | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 6 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 5<br>RX_CH5   | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 5 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 4<br>RX_CH4   | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 4 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 3<br>RX_CH3   | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 3 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |
| 2<br>RX_CH2   | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 2 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically.  |

*Table continues on the next page...*

**MIPI\_HSI\_CH\_SFTRST field descriptions (continued)**

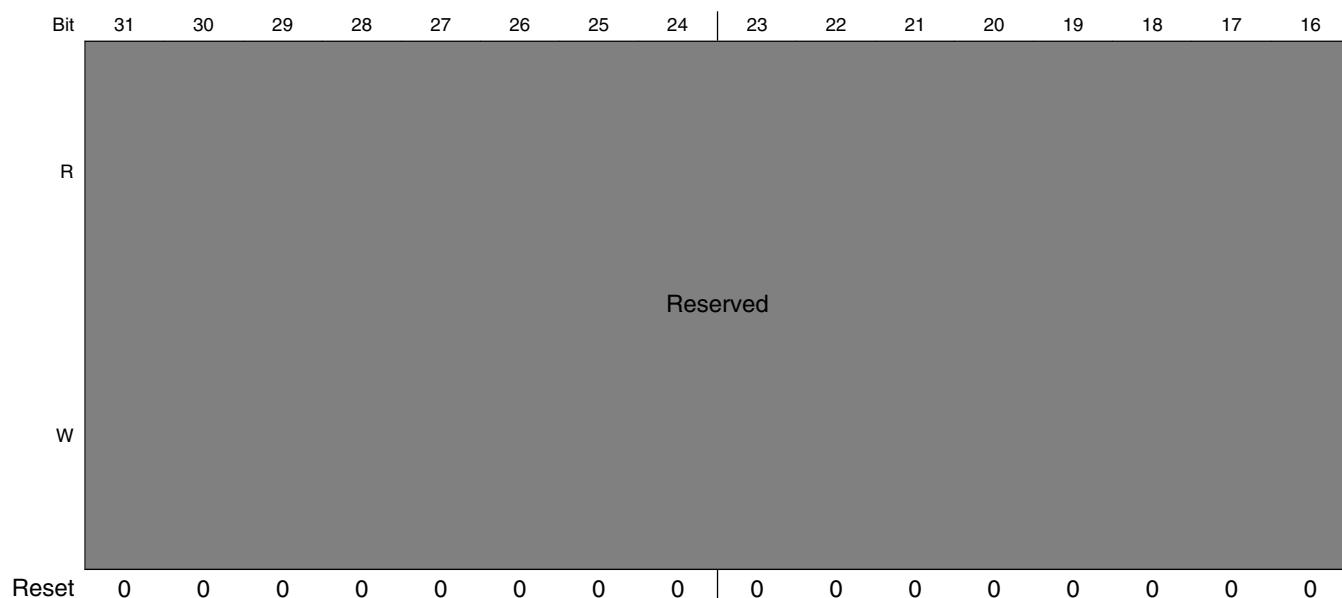
| Field       | Description   |
|-------------|---|
| 1<br>RX_CH1 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 1 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |
| 0<br>RX_CH0 | Set this bit to zero to enable normal HSI operation. Set this bit to one to reset Rx Channel 0 (DMA and Fifo). When the reset operation complete, this bit will turn to zero automatically. |

**42.5.13 HSI Interrupt Status Register (MIPI\_HSI\_IRQSTAT)**

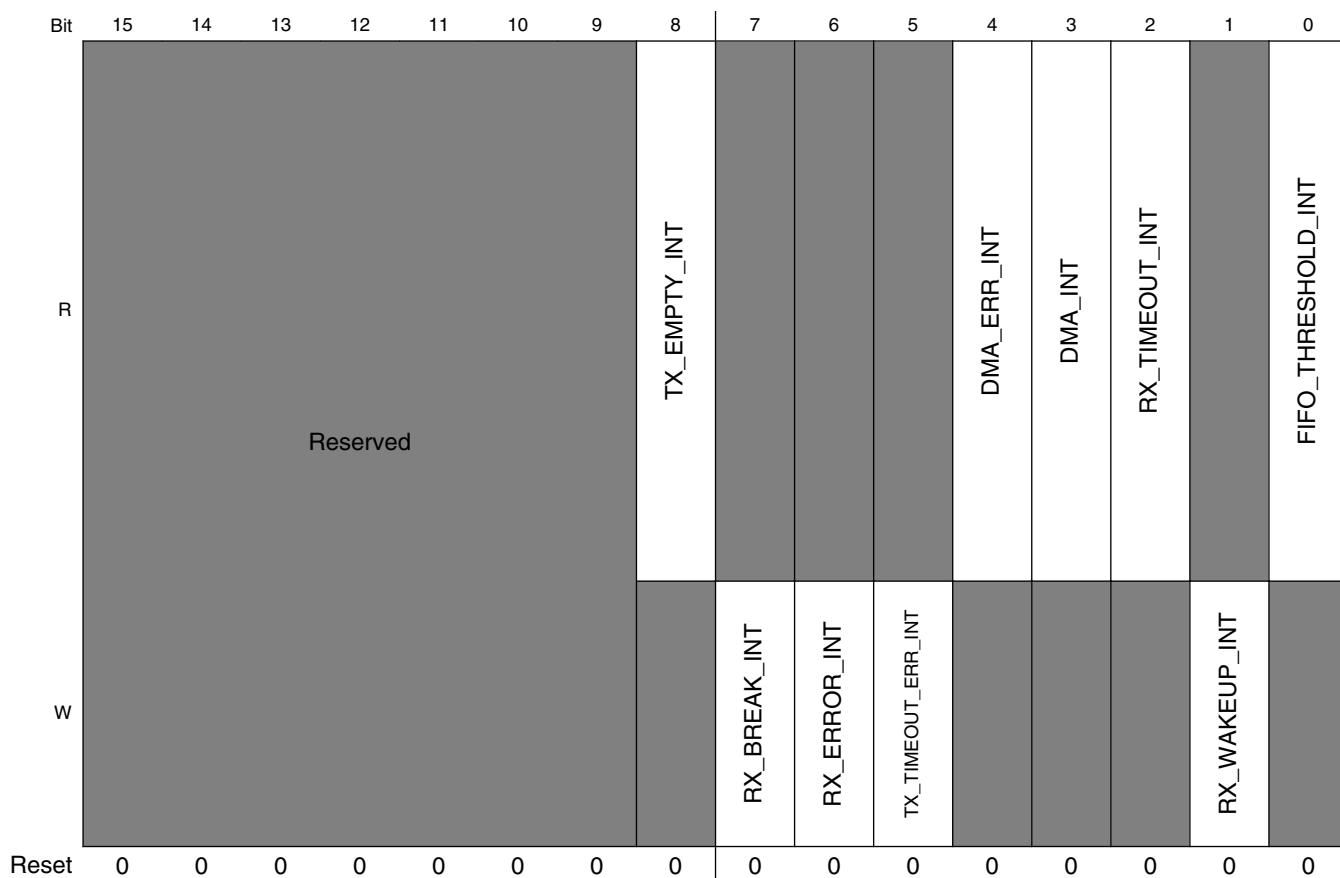
This is HSI controller Interrupt Status Register.

This register contains the HSI controller Interrupt Status.

Address: 220\_8000h base + 30h offset = 220\_8030h



## HSI Memory Map/Register Definition



### MIPI\_HSI\_IRQSTAT field descriptions

| Field                   | Description   |
|-------------------------|---|
| 31–9<br>Reserved        | This field is reserved.<br>Reserved, always set to zero.  |
| 8<br>TX_EMPTY_INT       | 1 All tx channel empty and tx state IDLE Interrupt Status<br>0 not All tx channel empty and tx state IDLE Interrupt Status  |
| 7<br>RX_BREAK_INT       | 0 No Error.<br>1 Error.   |
| 6<br>RX_ERROR_INT       | 0 No Error.<br>1 Error.   |
| 5<br>TX_TIMEOUT_ERR_INT | 0 No Error.<br>1 Error.   |
| 4<br>DMA_ERR_INT        | If any bit in the DMA Error Interrupt Status Register is set, then this bit is set.<br>on seeing this bit set, the ocp driver will read the Error Interrupt Status Register.<br>0 No Error.<br>1 Error. |
| 3<br>DMA_INT            | This bit is set when a Transmit or Receive Operation is completed for DMA.  |

*Table continues on the next page...*

**MIPI\_HSI\_IRQSTAT field descriptions (continued)**

| Field                   | Description   |
|-------------------------|---|
| 2<br>RX_TIMEOUT_INT     | If any bit in the HSI Error Interrupt Status Register is set, then this bit is set.<br>on seeing this bit set, the ocp driver will read the Error Interrupt Status Register.<br>0 No Error.<br>1 Error. |
| 1<br>RX_WAKEUP_INT      | 1 Receiver Wakeup event is occurred<br>0 Receiver Wakeup event is not occurred  |
| 0<br>FIFO_THRESHOLD_INT | 1 Threshold amount of data reached in TX/Rx FIFO Interrupt Status<br>0 Threshold amount of data not reached in TX/Rx FIFO Interrupt Status  |

### 42.5.14 HSI Interrupt Status Enable Register (MIPI\_HSI\_IRQSTAT\_EN)

This register contains the HSI controller Interrupt Status Enable.

Address: 220\_8000h base + 34h offset = 220\_8034h

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| W     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| R     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| W     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**MIPI\_HSI\_IRQSTAT\_EN field descriptions**

| Field            | Description  |
|------------------|--|
| 31–9<br>Reserved | This field is reserved.<br>Reserved, always set to zero. |

*Table continues on the next page...*

**MIPI\_HSI\_IRQSTAT\_EN field descriptions (continued)**

| Field                   | Description |   |
|-------------------------|-------------|---|
| 8<br>TX_EMPTY_INT       | 1           | Interrupt status enabled for TX_EMPTY_INT_STATUS interrupt.       |
|                         | 0           | Interrupt status masked TX_EMPTY_INT_STATUS interrupt.            |
| 7<br>RX_BREAK_INT       | 1           | Interrupt status enabled for RX_BREAK status interrupt.           |
|                         | 0           | Interrupt status masked RX_BREAK status interrupt.                |
| 6<br>RX_ERROR_INT       | 1           | Interrupt status enabled for RX_ERROR status interrupt.           |
|                         | 0           | Interrupt status masked RX_ERROR status interrupt.                |
| 5<br>TX_TIMEOUT_ERR_INT | 1           | Interrupt status enabled for TX_TIMEOUT_ERR status interrupt.     |
|                         | 0           | Interrupt status masked TX_TIMEOUT_ERR status interrupt.          |
| 4<br>DMA_ERR_INT        | 1           | Interrupt status enabled for DMA_ERROR_INT_STATUS interrupt.      |
|                         | 0           | Interrupt status masked DMA_ERROR_INT_STATUS interrupt.           |
| 3<br>DMA_INT            | 1           | Interrupt status enabled for DMA_INT_STATUS interrupt.            |
|                         | 0           | Interrupt status masked DMA_INT_STATUS interrupt.                 |
| 2<br>RX_TIMEOUT_INT     | 1           | Interrupt status enabled for RX_TIMEOUT_INT_STATUS interrupt.     |
|                         | 0           | Interrupt status masked RX_TIMEOUT_INT_STATUS interrupt.          |
| 1<br>RX_WAKEUP_INT      | 1           | Interrupt status enabled for RX_WAKEUP_INT_STATUS interrupt.      |
|                         | 0           | Interrupt status masked RX_WAKEUP_INT_STATUS interrupt.           |
| 0<br>FIFO_THRESHOLD_INT | 1           | Interrupt status enabled for FIFO_THRESHOLD_INT_STATUS interrupt. |
|                         | 0           | Interrupt status masked FIFO_THRESHOLD_INT_STATUS interrupt.      |

## 42.5.15 HSI Interrupt Signal Enable Register (MIPI\_HSI\_IRQSIG\_EN)

This register contains the HSI controller Interrupt Signal Enable.

Address: 220\_8000h base + 38h offset = 220\_8038h

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22           | 21                 | 20          | 19      | 18             | 17            | 16                 |
|-------|----------|----|----|----|----|----|----|----|--------------|--------------|--------------------|-------------|---------|----------------|---------------|--------------------|
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0            | 0                  | 0           | 0       | 0              | 0             | 0                  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7            | 6            | 5                  | 4           | 3       | 2              | 1             | 0                  |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0            | 0                  | 0           | 0       | 0              | 0             | 0                  |
| R     | Reserved |    |    |    |    |    |    |    | RX_BREAK_INT | RX_ERROR_INT | TX_TIMEOUT_ERR_INT | DMA_ERR_INT | DMA_INT | RX_TIMEOUT_INT | RX_WAKEUP_INT | FIFO_THRESHOLD_INT |
| W     | Reserved |    |    |    |    |    |    |    | 1            | 0            | 0                  | 0           | 0       | 0              | 0             | 0                  |

### MIPI\_HSI\_IRQSIG\_EN field descriptions

| Field                   | Description   |
|-------------------------|---|
| 31–9<br>Reserved        | This field is reserved.<br>Reserved, always set to zero.  |
| 8<br>TX_EMPTY_INT       | Setting this bit will enable interrupt generation on interrupt line.<br>1   Interrupt signal enabled for HSI TX_EMPTY interrupt.<br>0   Interrupt signal masked for HSI TX_EMPTY interrupt.         |
| 7<br>RX_BREAK_INT       | Setting this bit will enable interrupt generation on interrupt line.<br>1   Interrupt signal enabled for RX_BREAK interrupt.<br>0   Interrupt signal masked for RX_BREAK interrupt.                 |
| 6<br>RX_ERROR_INT       | Setting this bit will enable interrupt generation on interrupt line.<br>1   Interrupt signal enabled for RX Error interrupt.<br>0   Interrupt signal masked for RX Error interrupt.                 |
| 5<br>TX_TIMEOUT_ERR_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1   Interrupt signal enabled for TX Timeout Error interrupt.<br>0   Interrupt signal masked for TX Timeout Error interrupt. |

Table continues on the next page...

**MIPI\_HSI\_IRQSIG\_EN field descriptions (continued)**

| Field                | Description   |
|----------------------|---|
| 4 DMA_ERR_INT        | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for DMA Error interrupt.<br>0 Interrupt signal masked for DMA Error interrupt.                   |
| 3 DMA_INT            | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for DMA Completed interrupt.<br>0 Interrupt signal masked for DMA Completed interrupt.           |
| 2 RX_TIMEOUT_INT     | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for RX TIMEOUT interrupt.<br>0 Interrupt signal masked for RX TIMEOUT interrupt.                 |
| 1 RX_WAKEUP_INT      | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for HSI RX Wakeup interrupt.<br>0 Interrupt signal masked for HSI RX Wakeup interrupt.           |
| 0 FIFO_THRESHOLD_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for HSI FIFO_THRESHOLD interrupt.<br>0 Interrupt signal masked for HSI FIFO_THRESHOLD interrupt. |

## 42.5.16 HSI FIFO Threshold Interrupt Status Register (MIPI\_HSI\_FIFO\_THR\_IRQSTAT)

This register contains the HSI controller FIFO Threshold Interrupt Status.

Address: 220\_8000h base + 3Ch offset = 220\_803Ch

| Bit   | 31          | 30          | 29          | 28          | 27          | 26          | 25         | 24         | 23         | 22         | 21         | 20         | 19         | 18         | 17         | 16         |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| R     | TX_CH15_INT | TX_CH14_INT | TX_CH13_INT | TX_CH12_INT | TX_CH11_INT | TX_CH10_INT | TX_CH9_INT | TX_CH8_INT | TX_CH7_INT | TX_CH6_INT | TX_CH5_INT | TX_CH4_INT | TX_CH3_INT | TX_CH2_INT | TX_CH1_INT | TX_CH0_INT |
| W     |             |             |             |             |             |             |            |            |            |            |            |            |            |            |            |            |
| Reset | 1           | 1           | 1           | 1           | 1           | 1           | 1          | 1          | 1          | 1          | 1          | 1          | 1          | 1          | 1          | 1          |
| Bit   | 15          | 14          | 13          | 12          | 11          | 10          | 9          | 8          | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| R     | RX_CH15_INT | RX_CH14_INT | RX_CH13_INT | RX_CH12_INT | RX_CH11_INT | RX_CH10_INT | RX_CH9_INT | RX_CH8_INT | RX_CH7_INT | RX_CH6_INT | RX_CH5_INT | RX_CH4_INT | RX_CH3_INT | RX_CH2_INT | RX_CH1_INT | RX_CH0_INT |
| W     |             |             |             |             |             |             |            |            |            |            |            |            |            |            |            |            |
| Reset | 0           | 0           | 0           | 0           | 0           | 0           | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          |

**MIPI\_HSI\_FIFO\_THR\_IRQSTAT field descriptions**

| Field             | Description |  |
|-------------------|-------------|--|
| 31<br>TX_CH15_INT | 1           | Threshold amount of data reached in Tx Channel 15 FIFO     |
|                   | 0           | Threshold amount of data not reached in Tx Channel 15 FIFO |
| 30<br>TX_CH14_INT | 1           | Threshold amount of data reached in Tx Channel 14 FIFO     |
|                   | 0           | Threshold amount of data not reached in Tx Channel 14 FIFO |
| 29<br>TX_CH13_INT | 1           | Threshold amount of data reached in Tx Channel 13 FIFO     |
|                   | 0           | Threshold amount of data not reached in Tx Channel 13 FIFO |
| 28<br>TX_CH12_INT | 1           | Threshold amount of data reached in Tx Channel 12 FIFO     |
|                   | 0           | Threshold amount of data not reached in Tx Channel 12 FIFO |
| 27<br>TX_CH11_INT | 1           | Threshold amount of data reached in Tx Channel 11 FIFO     |
|                   | 0           | Threshold amount of data not reached in Tx Channel 11 FIFO |
| 26<br>TX_CH10_INT | 1           | Threshold amount of data reached in Tx Channel 10 FIFO     |
|                   | 0           | Threshold amount of data not reached in Tx Channel 10 FIFO |
| 25<br>TX_CH9_INT  | 1           | Threshold amount of data reached in Tx Channel 9 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 9 FIFO  |
| 24<br>TX_CH8_INT  | 1           | Threshold amount of data reached in Tx Channel 8 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 8 FIFO  |
| 23<br>TX_CH7_INT  | 1           | Threshold amount of data reached in Tx Channel 7 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 7 FIFO  |
| 22<br>TX_CH6_INT  | 1           | Threshold amount of data reached in Tx Channel 6 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 6 FIFO  |
| 21<br>TX_CH5_INT  | 1           | Threshold amount of data reached in Tx Channel 5 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 5 FIFO  |
| 20<br>TX_CH4_INT  | 1           | Threshold amount of data reached in Tx Channel 4 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 4 FIFO  |
| 19<br>TX_CH3_INT  | 1           | Threshold amount of data reached in Tx Channel 3 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 3 FIFO  |
| 18<br>TX_CH2_INT  | 1           | Threshold amount of data reached in Tx Channel 2 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 2 FIFO  |
| 17<br>TX_CH1_INT  | 1           | Threshold amount of data reached in Tx Channel 1 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 1 FIFO  |
| 16<br>TX_CH0_INT  | 1           | Threshold amount of data reached in Tx Channel 0 FIFO      |
|                   | 0           | Threshold amount of data not reached in Tx Channel 0 FIFO  |
| 15<br>RX_CH15_INT | 1           | Threshold amount of data reached in Rx Channel 15 FIFO     |
|                   | 0           | Threshold amount of data not reached in Rx Channel 15 FIFO |
| 14<br>RX_CH14_INT | 1           | Threshold amount of data reached in Rx Channel 14 FIFO     |
|                   | 0           | Threshold amount of data not reached in Rx Channel 14 FIFO |
| 13<br>RX_CH13_INT | 1           | Threshold amount of data reached in Rx Channel 13 FIFO     |
|                   | 0           | Threshold amount of data not reached in Rx Channel 13 FIFO |
| 12<br>RX_CH12_INT | 1           | Threshold amount of data reached in Rx Channel 12 FIFO     |
|                   | 0           | Threshold amount of data not reached in Rx Channel 12 FIFO |
| 11<br>RX_CH11_INT | 1           | Threshold amount of data reached in Rx Channel 11 FIFO     |
|                   | 0           | Threshold amount of data not reached in Rx Channel 11 FIFO |

*Table continues on the next page...*

**MIPI\_HSI\_FIFO\_THR\_IRQSTAT field descriptions (continued)**

| Field             | Description |  |
|-------------------|-------------|--|
| 10<br>RX_CH10_INT | 1           | Threshold amount of data reached in Rx Channel 10 FIFO     |
|                   | 0           | Threshold amount of data not reached in Rx Channel 10 FIFO |
| 9<br>RX_CH9_INT   | 1           | Threshold amount of data reached in Rx Channel 9 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 9 FIFO  |
| 8<br>RX_CH8_INT   | 1           | Threshold amount of data reached in Rx Channel 8 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 8 FIFO  |
| 7<br>RX_CH7_INT   | 1           | Threshold amount of data reached in Rx Channel 7 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 7 FIFO  |
| 6<br>RX_CH6_INT   | 1           | Threshold amount of data reached in Rx Channel 6 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 6 FIFO  |
| 5<br>RX_CH5_INT   | 1           | Threshold amount of data reached in Rx Channel 5 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 5 FIFO  |
| 4<br>RX_CH4_INT   | 1           | Threshold amount of data reached in Rx Channel 4 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 4 FIFO  |
| 3<br>RX_CH3_INT   | 1           | Threshold amount of data reached in Rx Channel 3 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 3 FIFO  |
| 2<br>RX_CH2_INT   | 1           | Threshold amount of data reached in Rx Channel 2 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 2 FIFO  |
| 1<br>RX_CH1_INT   | 1           | Threshold amount of data reached in Rx Channel 1 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 1 FIFO  |
| 0<br>RX_CH0_INT   | 1           | Threshold amount of data reached in Rx Channel 0 FIFO      |
|                   | 0           | Threshold amount of data not reached in Rx Channel 0 FIFO  |

## 42.5.17 HSI FIFO Threshold Interrupt Status Enable Register (MIPI\_HSI\_FIFO\_THR\_IRQSTAT\_EN)

This register contains the HSI controller FIFO Threshold Interrupt Status Enable.

Address: 220\_8000h base + 40h offset = 220\_8040h

| Bit   | 31          | 30          | 29          | 28          | 27          | 26          | 25         | 24         | 23         | 22         | 21         | 20         | 19         | 18         | 17         | 16         |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| R     | TX_CH15_INT | TX_CH14_INT | TX_CH13_INT | TX_CH12_INT | TX_CH11_INT | TX_CH10_INT | TX_CH9_INT | TX_CH8_INT | TX_CH7_INT | TX_CH6_INT | TX_CH5_INT | TX_CH4_INT | TX_CH3_INT | TX_CH2_INT | TX_CH1_INT | TX_CH0_INT |
| W     |             |             |             |             |             |             |            |            |            |            |            |            |            |            |            |            |
| Reset | 0           | 0           | 0           | 0           | 0           | 0           | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          |
| Bit   | 15          | 14          | 13          | 12          | 11          | 10          | 9          | 8          | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| R     | RX_CH15_INT | RX_CH14_INT | RX_CH13_INT | RX_CH12_INT | RX_CH11_INT | RX_CH10_INT | RX_CH9_INT | RX_CH8_INT | RX_CH7_INT | RX_CH6_INT | RX_CH5_INT | RX_CH4_INT | RX_CH3_INT | RX_CH2_INT | RX_CH1_INT | RX_CH0_INT |
| W     |             |             |             |             |             |             |            |            |            |            |            |            |            |            |            |            |
| Reset | 0           | 0           | 0           | 0           | 0           | 0           | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          |

### MIPI\_HSI\_FIFO\_THR\_IRQSTAT\_EN field descriptions

| Field             | Description   |
|-------------------|---|
| 31<br>TX_CH15_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1   Interrupt signal enabled for Tx Ch15 threshold Reached interrupt.<br>0   Interrupt signal masked for Tx Ch15 threshold Reached interrupt. |
| 30<br>TX_CH14_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1   Interrupt signal enabled for Tx Ch14 threshold Reached interrupt.<br>0   Interrupt signal masked for Tx Ch14 threshold Reached interrupt. |
| 29<br>TX_CH13_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1   Interrupt signal enabled for Tx Ch13 threshold Reached interrupt.<br>0   Interrupt signal masked for Tx Ch13 threshold Reached interrupt. |
| 28<br>TX_CH12_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1   Interrupt signal enabled for Tx Ch12 threshold Reached interrupt.<br>0   Interrupt signal masked for Tx Ch12 threshold Reached interrupt. |
| 27<br>TX_CH11_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1   Interrupt signal enabled for Tx Ch11 threshold Reached interrupt.<br>0   Interrupt signal masked for Tx Ch11 threshold Reached interrupt. |

Table continues on the next page...

**MIPI\_HSI\_FIFO\_THR\_IRQSTAT\_EN field descriptions (continued)**

| Field             | Description   |
|-------------------|---|
| 26<br>TX_CH10_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch10 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch10 threshold Reached interrupt. |
| 25<br>TX_CH9_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch9 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch9 threshold Reached interrupt.   |
| 24<br>TX_CH8_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch8 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch8 threshold Reached interrupt.   |
| 23<br>TX_CH7_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch7 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch7 threshold Reached interrupt.   |
| 22<br>TX_CH6_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch6 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch6 threshold Reached interrupt.   |
| 21<br>TX_CH5_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch5 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch5 threshold Reached interrupt.   |
| 20<br>TX_CH4_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch4 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch4 threshold Reached interrupt.   |
| 19<br>TX_CH3_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch3 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch3 threshold Reached interrupt.   |
| 18<br>TX_CH2_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch2 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch2 threshold Reached interrupt.   |
| 17<br>TX_CH1_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch1 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch1 threshold Reached interrupt.   |
| 16<br>TX_CH0_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch0 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch0 threshold Reached interrupt.   |
| 15<br>RX_CH15_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch15 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch15 threshold Reached interrupt. |

*Table continues on the next page...*

**MIPI\_HSI\_FIFO\_THR\_IRQSTAT\_EN field descriptions (continued)**

| Field             | Description   |
|-------------------|---|
| 14<br>RX_CH14_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch14 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch14 threshold Reached interrupt. |
| 13<br>RX_CH13_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch13 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch13 threshold Reached interrupt. |
| 12<br>RX_CH12_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch12 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch12 threshold Reached interrupt. |
| 11<br>RX_CH11_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch11 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch11 threshold Reached interrupt. |
| 10<br>RX_CH10_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch10 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch10 threshold Reached interrupt. |
| 9<br>RX_CH9_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch9 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch9 threshold Reached interrupt.   |
| 8<br>RX_CH8_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch8 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch8 threshold Reached interrupt.   |
| 7<br>RX_CH7_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch7 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch7 threshold Reached interrupt.   |
| 6<br>RX_CH6_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch6 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch6 threshold Reached interrupt.   |
| 5<br>RX_CH5_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch5 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch5 threshold Reached interrupt.   |
| 4<br>RX_CH4_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch4 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch4 threshold Reached interrupt.   |
| 3<br>RX_CH3_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch3 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch3 threshold Reached interrupt.   |

*Table continues on the next page...*

**MIPI\_HSI\_FIFO\_THR\_IRQSTAT\_EN field descriptions (continued)**

| Field           | Description   |
|-----------------|---|
| 2<br>RX_CH2_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch2 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch2 threshold Reached interrupt. |
| 1<br>RX_CH1_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch1 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch1 threshold Reached interrupt. |
| 0<br>RX_CH0_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch0 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch0 threshold Reached interrupt. |

### 42.5.18 HSI FIFO Threshold Interrupt Signal Enable Register (MIPI\_HSI\_FIFO\_THR\_IRQSIG\_EN)

This register contains the HSI controller FIFO Threshold Interrupt Enable.

Address: 220\_8000h base + 44h offset = 220\_8044h

|       |             |             |             |             |             |             |            |            |            |            |            |            |            |            |            |            |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| Bit   | 31          | 30          | 29          | 28          | 27          | 26          | 25         | 24         | 23         | 22         | 21         | 20         | 19         | 18         | 17         | 16         |
| R     | TX_CH15_INT | TX_CH14_INT | TX_CH13_INT | TX_CH12_INT | TX_CH11_INT | TX_CH10_INT | TX_CH9_INT | TX_CH8_INT | TX_CH7_INT | TX_CH6_INT | TX_CH5_INT | TX_CH4_INT | TX_CH3_INT | TX_CH2_INT | TX_CH1_INT | TX_CH0_INT |
| W     |             |             |             |             |             |             |            |            |            |            |            |            |            |            |            |            |
| Reset | 0           | 0           | 0           | 0           | 0           | 0           | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          |
| Bit   | 15          | 14          | 13          | 12          | 11          | 10          | 9          | 8          | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| R     | RX_CH15_INT | RX_CH14_INT | RX_CH13_INT | RX_CH12_INT | RX_CH11_INT | RX_CH10_INT | RX_CH9_INT | RX_CH8_INT | RX_CH7_INT | RX_CH6_INT | RX_CH5_INT | RX_CH4_INT | RX_CH3_INT | RX_CH2_INT | RX_CH1_INT | RX_CH0_INT |
| W     |             |             |             |             |             |             |            |            |            |            |            |            |            |            |            |            |
| Reset | 0           | 0           | 0           | 0           | 0           | 0           | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          |

**MIPI\_HSI\_FIFO\_THR\_IRQSIG\_EN field descriptions**

| Field             | Description   |
|-------------------|---|
| 31<br>TX_CH15_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch15 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch15 threshold Reached interrupt. |

*Table continues on the next page...*

**MIPI\_HSI\_FIFO\_THR\_IRQSIG\_EN field descriptions (continued)**

| Field             | Description   |
|-------------------|---|
| 30<br>TX_CH14_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch14 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch14 threshold Reached interrupt. |
| 29<br>TX_CH13_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch13 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch13 threshold Reached interrupt. |
| 28<br>TX_CH12_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch12 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch12 threshold Reached interrupt. |
| 27<br>TX_CH11_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch11 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch11 threshold Reached interrupt. |
| 26<br>TX_CH10_INT | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch10 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch10 threshold Reached interrupt. |
| 25<br>TX_CH9_INT  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch9 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch9 threshold Reached interrupt.   |
| 24<br>TX_CH8_INT  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch8 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch8 threshold Reached interrupt.   |
| 23<br>TX_CH7_INT  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch7 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch7 threshold Reached interrupt.   |
| 22<br>TX_CH6_INT  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch6 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch6 threshold Reached interrupt.   |
| 21<br>TX_CH5_INT  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch5 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch5 threshold Reached interrupt.   |
| 20<br>TX_CH4_INT  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch4 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch4 threshold Reached interrupt.   |
| 19<br>TX_CH3_INT  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for Tx Ch3 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch3 threshold Reached interrupt.   |

*Table continues on the next page...*

**MIPI\_HSI\_FIFO\_THR\_IRQSIG\_EN field descriptions (continued)**

| Field             | Description   |
|-------------------|---|
| 18<br>TX_CH2_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch2 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch2 threshold Reached interrupt.   |
| 17<br>TX_CH1_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch1 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch1 threshold Reached interrupt.   |
| 16<br>TX_CH0_INT  | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Tx Ch0 threshold Reached interrupt.<br>0 Interrupt signal masked for Tx Ch0 threshold Reached interrupt.   |
| 15<br>RX_CH15_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch15 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch15 threshold Reached interrupt. |
| 14<br>RX_CH14_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch14 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch14 threshold Reached interrupt. |
| 13<br>RX_CH13_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch13 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch13 threshold Reached interrupt. |
| 12<br>RX_CH12_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch12 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch12 threshold Reached interrupt. |
| 11<br>RX_CH11_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch11 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch11 threshold Reached interrupt. |
| 10<br>RX_CH10_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch10 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch10 threshold Reached interrupt. |
| 9<br>RX_CH9_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch9 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch9 threshold Reached interrupt.   |
| 8<br>RX_CH8_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch8 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch8 threshold Reached interrupt.   |
| 7<br>RX_CH7_INT   | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch7 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch7 threshold Reached interrupt.   |

*Table continues on the next page...*

**MIPI\_HSI\_FIFO\_THR\_IRQSIG\_EN field descriptions (continued)**

| Field           | Description   |
|-----------------|---|
| 6<br>RX_CH6_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch6 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch6 threshold Reached interrupt. |
| 5<br>RX_CH5_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch5 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch5 threshold Reached interrupt. |
| 4<br>RX_CH4_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch4 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch4 threshold Reached interrupt. |
| 3<br>RX_CH3_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch3 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch3 threshold Reached interrupt. |
| 2<br>RX_CH2_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch2 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch2 threshold Reached interrupt. |
| 1<br>RX_CH1_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch1 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch1 threshold Reached interrupt. |
| 0<br>RX_CH0_INT | Setting this bit will enable interrupt generation on interrupt line.<br><br>1 Interrupt signal enabled for Rx Ch0 threshold Reached interrupt.<br>0 Interrupt signal masked for Rx Ch0 threshold Reached interrupt. |

**42.5.19 Tx Channel n Data Port Register (MIPI\_HSI\_TX\_CHn\_DP)**

This Register is connected to fifo data port for Tx Channel n.

Address: 220\_8000h base + 50h offset + (4d × i), where i=0d to 15d

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| W   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

Reset 0

**MIPI\_HSI\_TX\_CHn\_DP field descriptions**

| Field | Description   |
|-------|---|
| DATA  | Software could Write/Read this bits to access Tx Channel n. |

## 42.5.20 Rx Channel n Data Port Register (MIPI\_HSI\_RX\_CHn\_DP)

This Register is connected to fifo data port for Rx Channel n.

Address: 220\_8000h base + 90h offset + (4d × i), where i=0d to 15d

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| W   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**MIPI\_HSI\_RX\_CHn\_DP field descriptions**

| Field | Description   |
|-------|---|
| DATA  | Software could Write/Read this bits to access Rx Channel n. |

## 42.5.21 HSI Error Interrupt Status Register (MIPI\_HSI\_ERR\_IRQSTAT)

This register contains the HSI controller Error Interrupt Status.

Address: 220\_8000h base + D0h offset = 220\_80D0h

| Bit   | 31                  | 30                  | 29                  | 28                  | 27                  | 26                  | 25                 | 24                 | 23                 | 22                 | 21                 | 20                 | 19                 | 18                 | 17                 | 16                 |
|-------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| R     | RX_CH15_TIMEOUT_INT | RX_CH14_TIMEOUT_INT | RX_CH13_TIMEOUT_INT | RX_CH12_TIMEOUT_INT | RX_CH11_TIMEOUT_INT | RX_CH10_TIMEOUT_INT | RX_CH9_TIMEOUT_INT | RX_CH8_TIMEOUT_INT | RX_CH7_TIMEOUT_INT | RX_CH6_TIMEOUT_INT | RX_CH5_TIMEOUT_INT | RX_CH4_TIMEOUT_INT | RX_CH3_TIMEOUT_INT | RX_CH2_TIMEOUT_INT | RX_CH1_TIMEOUT_INT | RX_CH0_TIMEOUT_INT |
| W     |                     |                     |                     |                     |                     |                     |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |
| Reset | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  |
| Bit   | 15                  | 14                  | 13                  | 12                  | 11                  | 10                  | 9                  | 8                  | 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
| R     |                     |                     |                     |                     |                     |                     |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |
| W     |                     |                     |                     |                     |                     |                     |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |
| Reset | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  |

### MIPI\_HSI\_ERR\_IRQSTAT field descriptions

| Field                         | Description  |
|-------------------------------|--|
| 31<br>RX_CH15_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch15 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch15 buffer and then read HSI Status register to find the further status of the Rx ch15 Buffer.<br><br>The host driver has to read the Rx ch15 fifo on Dword basis, till the fifo is completely empty. |

Table continues on the next page...

**MIPI\_HSI\_ERR\_IRQSTAT field descriptions (continued)**

| Field                         | Description  |
|-------------------------------|--|
| 30<br>RX_CH14_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch14 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch14 buffer and then read HSI Status register to find the further status of the Rx ch14 Buffer.<br><br>The host driver has to read the Rx ch14 fifo on Dword basis, till the fifo is completely empty. |
| 29<br>RX_CH13_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch13 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch13 buffer and then read HSI Status register to find the further status of the Rx ch13 Buffer.<br><br>The host driver has to read the Rx ch13 fifo on Dword basis, till the fifo is completely empty. |
| 28<br>RX_CH12_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch12 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch12 buffer and then read HSI Status register to find the further status of the Rx ch12 Buffer.<br><br>The host driver has to read the Rx ch12 fifo on Dword basis, till the fifo is completely empty. |
| 27<br>RX_CH11_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch11 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch11 buffer and then read HSI Status register to find the further status of the Rx ch11 Buffer.<br><br>The host driver has to read the Rx ch11 fifo on Dword basis, till the fifo is completely empty. |
| 26<br>RX_CH10_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch10 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch10 buffer and then read HSI Status register to find the further status of the Rx ch10 Buffer.<br><br>The host driver has to read the Rx ch10 fifo on Dword basis, till the fifo is completely empty. |
| 25<br>RX_CH9_<br>TIMEOUT_INT  | This status bit is set when data timeout counter for ch9 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch9 buffer and then read HSI Status register to find the further status of the Rx ch9 Buffer.<br><br>The host driver has to read the Rx ch9 fifo on Dword basis, till the fifo is completely empty.     |
| 24<br>RX_CH8_<br>TIMEOUT_INT  | This status bit is set when data timeout counter for ch8 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch8 buffer and then read HSI Status register to find the further status of the Rx ch8 Buffer.<br><br>The host driver has to read the Rx ch8 fifo on Dword basis, till the fifo is completely empty.     |
| 23<br>RX_CH7_<br>TIMEOUT_INT  | This status bit is set when data timeout counter for ch7 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch7 buffer and then read HSI Status register to find the further status of the Rx ch7 Buffer.<br><br>The host driver has to read the Rx ch7 fifo on Dword basis, till the fifo is completely empty.     |
| 22<br>RX_CH6_<br>TIMEOUT_INT  | This status bit is set when data timeout counter for ch6 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch6 buffer and then read HSI Status register to find the further status of the Rx ch6 Buffer.<br><br>The host driver has to read the Rx ch6 fifo on Dword basis, till the fifo is completely empty.     |
| 21<br>RX_CH5_<br>TIMEOUT_INT  | This status bit is set when data timeout counter for ch5 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch5 buffer and then read HSI Status register to find the further status of the Rx ch5 Buffer.<br><br>The host driver has to read the Rx ch5 fifo on Dword basis, till the fifo is completely empty.     |
| 20<br>RX_CH4_<br>TIMEOUT_INT  | This status bit is set when data timeout counter for ch4 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch4 buffer and then read HSI Status register to find the further status of the Rx ch4 Buffer.<br><br>The host driver has to read the Rx ch4 fifo on Dword basis, till the fifo is completely empty.     |

*Table continues on the next page...*

**MIPI\_HSI\_ERR\_IRQSTAT field descriptions (continued)**

| Field                        | Description  |
|------------------------------|--|
| 19<br>RX_CH3_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch3 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch3 buffer and then read HSI Status register to find the further status of the Rx ch3 Buffer.<br><br>The host driver has to read the Rx ch3 fifo on Dword basis, till the fifo is completely empty. |
| 18<br>RX_CH2_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch2 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch2 buffer and then read HSI Status register to find the further status of the Rx ch2 Buffer.<br><br>The host driver has to read the Rx ch2 fifo on Dword basis, till the fifo is completely empty. |
| 17<br>RX_CH1_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch1 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch1 buffer and then read HSI Status register to find the further status of the Rx ch1 Buffer.<br><br>The host driver has to read the Rx ch1 fifo on Dword basis, till the fifo is completely empty. |
| 16<br>RX_CH0_<br>TIMEOUT_INT | This status bit is set when data timeout counter for ch0 reaches the data timeout counter value. On receiving the interrupt the host driver should read 1Dword of data from Rx ch0 buffer and then read HSI Status register to find the further status of the Rx ch0 Buffer.<br><br>The host driver has to read the Rx ch0 fifo on Dword basis, till the fifo is completely empty. |
| Reserved                     | This field is reserved.<br>Reserved, always set to zero.   |

## 42.5.22 HSI Error Interrupt Status Enable Register (MIPI\_HSI\_ERR\_IRQSTAT\_EN)

This register contains the HSI controller Error Interrupt Status Enable.

Address: 220\_8000h base + D4h offset = 220\_80D4h

| Bit   | 31                     | 30                     | 29                     | 28                     | 27                     | 26                     | 25                    | 24                    | 23                    | 22                    | 21                    | 20                    | 19                    | 18                    | 17                    | 16                    |
|-------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| R     | RX_CH15_TIMEOUT_INT_EN | RX_CH14_TIMEOUT_INT_EN | RX_CH13_TIMEOUT_INT_EN | RX_CH12_TIMEOUT_INT_EN | RX_CH11_TIMEOUT_INT_EN | RX_CH10_TIMEOUT_INT_EN | RX_CH9_TIMEOUT_INT_EN | RX_CH8_TIMEOUT_INT_EN | RX_CH7_TIMEOUT_INT_EN | RX_CH6_TIMEOUT_INT_EN | RX_CH5_TIMEOUT_INT_EN | RX_CH4_TIMEOUT_INT_EN | RX_CH3_TIMEOUT_INT_EN | RX_CH2_TIMEOUT_INT_EN | RX_CH1_TIMEOUT_INT_EN | RX_CH0_TIMEOUT_INT_EN |
| W     |                        |                        |                        |                        |                        |                        |                       |                       |                       |                       |                       |                       |                       |                       |                       |                       |
| Reset | 0                      | 0                      | 0                      | 0                      | 0                      | 0                      | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     |
| Bit   | 15                     | 14                     | 13                     | 12                     | 11                     | 10                     | 9                     | 8                     | 7                     | 6                     | 5                     | 4                     | 3                     | 2                     | 1                     | 0                     |
| R     |                        |                        |                        |                        |                        |                        |                       |                       |                       |                       |                       |                       |                       |                       |                       |                       |
| W     |                        |                        |                        |                        |                        |                        |                       |                       |                       |                       |                       |                       |                       |                       |                       |                       |
| Reset | 0                      | 0                      | 0                      | 0                      | 0                      | 0                      | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     |

### MIPI\_HSI\_ERR\_IRQSTAT\_EN field descriptions

| Field                        | Description   |
|------------------------------|---|
| 31<br>RX_CH15_TIMEOUT_INT_EN | 1 Interrupt status enabled for data timeout for ch15 interrupt.<br>0 Interrupt status masked for data timeout for ch15 interrupt. |
| 30<br>RX_CH14_TIMEOUT_INT_EN | 1 Interrupt status enabled for data timeout for ch14 interrupt.<br>0 Interrupt status masked for data timeout for ch14 interrupt. |
| 29<br>RX_CH13_TIMEOUT_INT_EN | 1 Interrupt status enabled for data timeout for ch13 interrupt.<br>0 Interrupt status masked for data timeout for ch13 interrupt. |
| 28<br>RX_CH12_TIMEOUT_INT_EN | 1 Interrupt status enabled for data timeout for ch12 interrupt.<br>0 Interrupt status masked for data timeout for ch12 interrupt. |

Table continues on the next page...

**MIPI\_HSI\_ERR\_IRQSTAT\_EN field descriptions (continued)**

| Field                                | Description   |
|--------------------------------------|---|
| 27<br>RX_CH11_<br>TIMEOUT_INT_<br>EN | 1 Interrupt status enabled for data timeout for ch11 interrupt.<br>0 Interrupt status masked for data timeout for ch11 interrupt. |
| 26<br>RX_CH10_<br>TIMEOUT_INT_<br>EN | 1 Interrupt status enabled for data timeout for ch10 interrupt.<br>0 Interrupt status masked for data timeout for ch10 interrupt. |
| 25<br>RX_CH9_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch9 interrupt.<br>0 Interrupt status masked for data timeout for ch9 interrupt.   |
| 24<br>RX_CH8_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch8 interrupt.<br>0 Interrupt status masked for data timeout for ch8 interrupt.   |
| 23<br>RX_CH7_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch7 interrupt.<br>0 Interrupt status masked for data timeout for ch7 interrupt.   |
| 22<br>RX_CH6_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch6 interrupt.<br>0 Interrupt status masked for data timeout for ch6 interrupt.   |
| 21<br>RX_CH5_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch5 interrupt.<br>0 Interrupt status masked for data timeout for ch5 interrupt.   |
| 20<br>RX_CH4_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch4 interrupt.<br>0 Interrupt status masked for data timeout for ch4 interrupt.   |
| 19<br>RX_CH3_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch3 interrupt.<br>0 Interrupt status masked for data timeout for ch3 interrupt.   |
| 18<br>RX_CH2_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch2 interrupt.<br>0 Interrupt status masked for data timeout for ch2 interrupt.   |
| 17<br>RX_CH1_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch1 interrupt.<br>0 Interrupt status masked for data timeout for ch1 interrupt.   |
| 16<br>RX_CH0_<br>TIMEOUT_INT_<br>EN  | 1 Interrupt status enabled for data timeout for ch0 interrupt.<br>0 Interrupt status masked for data timeout for ch0 interrupt.   |
| Reserved                             | This field is reserved.<br>Reserved, always set to zero.  |

### 42.5.23 HSI Error Interrupt Signal Enable Register (MIPI\_HSI\_ERR\_IRQSIG\_EN)

This register contains the HSI controller Error Interrupt Signal Enable.

Address: 220\_8000h base + D8h offset = 220\_80D8h

| Bit   | 31                     | 30                     | 29                     | 28                     | 27                     | 26                     | 25                    | 24                    | 23                    | 22                    | 21                    | 20                    | 19                    | 18                    | 17                    | 16                    |
|-------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| R     | RX_CH15_TIMEOUT_INT_EN | RX_CH14_TIMEOUT_INT_EN | RX_CH13_TIMEOUT_INT_EN | RX_CH12_TIMEOUT_INT_EN | RX_CH11_TIMEOUT_INT_EN | RX_CH10_TIMEOUT_INT_EN | RX_CH9_TIMEOUT_INT_EN | RX_CH8_TIMEOUT_INT_EN | RX_CH7_TIMEOUT_INT_EN | RX_CH6_TIMEOUT_INT_EN | RX_CH5_TIMEOUT_INT_EN | RX_CH4_TIMEOUT_INT_EN | RX_CH3_TIMEOUT_INT_EN | RX_CH2_TIMEOUT_INT_EN | RX_CH1_TIMEOUT_INT_EN | RX_CH0_TIMEOUT_INT_EN |
| W     |                        |                        |                        |                        |                        |                        |                       |                       |                       |                       |                       |                       |                       |                       |                       |                       |
| Reset | 0                      | 0                      | 0                      | 0                      | 0                      | 0                      | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     |
| Bit   | 15                     | 14                     | 13                     | 12                     | 11                     | 10                     | 9                     | 8                     | 7                     | 6                     | 5                     | 4                     | 3                     | 2                     | 1                     | 0                     |
| R     | Reserved               |                        |                        |                        |                        |                        |                       |                       |                       |                       |                       |                       |                       |                       |                       |                       |
| W     |                        |                        |                        |                        |                        |                        |                       |                       |                       |                       |                       |                       |                       |                       |                       |                       |
| Reset | 0                      | 0                      | 0                      | 0                      | 0                      | 0                      | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     |

#### MIPI\_HSI\_ERR\_IRQSIG\_EN field descriptions

| Field                     | Description   |
|---------------------------|---|
| 31 RX_CH15_TIMEOUT_INT_EN | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch15 interrupt.<br>0 Interrupt signal masked for data timeout for ch15 interrupt. |
| 30 RX_CH14_TIMEOUT_INT_EN | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch14 interrupt.<br>0 Interrupt signal masked for data timeout for ch14 interrupt. |
| 29 RX_CH13_TIMEOUT_INT_EN | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch13 interrupt.<br>0 Interrupt signal masked for data timeout for ch13 interrupt. |
| 28 RX_CH12_TIMEOUT_INT_EN | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch12 interrupt.<br>0 Interrupt signal masked for data timeout for ch12 interrupt. |

Table continues on the next page...

**MIPI\_HSI\_ERR\_IRQSIG\_EN field descriptions (continued)**

| Field                                | Description   |
|--------------------------------------|---|
| 27<br>RX_CH11_<br>TIMEOUT_INT_<br>EN | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch11 interrupt.<br>0 Interrupt signal masked for data timeout for ch11 interrupt. |
| 26<br>RX_CH10_<br>TIMEOUT_INT_<br>EN | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch10 interrupt.<br>0 Interrupt signal masked for data timeout for ch10 interrupt. |
| 25<br>RX_CH9_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch9 interrupt.<br>0 Interrupt signal masked for data timeout for ch9 interrupt.   |
| 24<br>RX_CH8_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch8 interrupt.<br>0 Interrupt signal masked for data timeout for ch8 interrupt.   |
| 23<br>RX_CH7_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch7 interrupt.<br>0 Interrupt signal masked for data timeout for ch7 interrupt.   |
| 22<br>RX_CH6_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch6 interrupt.<br>0 Interrupt signal masked for data timeout for ch6 interrupt.   |
| 21<br>RX_CH5_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch5 interrupt.<br>0 Interrupt signal masked for data timeout for ch5 interrupt.   |
| 20<br>RX_CH4_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch4 interrupt.<br>0 Interrupt signal masked for data timeout for ch4 interrupt.   |
| 19<br>RX_CH3_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch3 interrupt.<br>0 Interrupt signal masked for data timeout for ch3 interrupt.   |
| 18<br>RX_CH2_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch2 interrupt.<br>0 Interrupt signal masked for data timeout for ch2 interrupt.   |
| 17<br>RX_CH1_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch1 interrupt.<br>0 Interrupt signal masked for data timeout for ch1 interrupt.   |
| 16<br>RX_CH0_<br>TIMEOUT_INT_<br>EN  | Setting this bit will enable interrupt generation on interrupt line.<br>1 Interrupt signal enabled for data timeout for ch0 interrupt.<br>0 Interrupt signal masked for data timeout for ch0 interrupt.   |
| Reserved                             | This field is reserved.   |

*Table continues on the next page...*

**MIPI\_HSI\_ERR\_IRQSIG\_EN field descriptions (continued)**

| Field | Description                   |
|-------|-------------------------------|
|       | Reserved, always set to zero. |

## 42.5.24 Tx DMA Channel n Configuration Register (MIPI\_HSI\_TDMA*n*\_CONF)

This register contains the configurations of enable/disable, burst size and transfer count for Tx DMA channel n.

Address: 220\_8000h base + DCh offset + (4d × i), where i=0d to 15d

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R     | ENABLE | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| W     |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| R     |        |    |    |    |    |    |    |    |    |    |    |    |    | 0  |    |    |
| W     |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**MIPI\_HSI\_TDMA*n*\_CONF field descriptions**

| Field                | Description  |
|----------------------|--|
| 31<br>ENABLE         | Setting this bit enables the internal Tx DMA channel n.  |
| 30–29<br>Reserved    | This read-only field is reserved and always has the value 0.   |
| 28–25<br>BURST_SIZE  | Burst size for Tx DMA channel n. The unit is Dword.<br>The burst size should not be larger than relevant TRANS_LENGTH and FIFO_SIZE.<br>h0 1Dword to transfer for each burst<br>h1 2Dword to transfer for each burst<br>h2 4Dword to transfer for each burst<br>h10 1024Dword to transfer for each burst |
| 24–5<br>TRANS_LENGTH | Transfer data length for Tx DMA channel n. The unit is Dword.<br>h1 1Dword to transfer<br>h2 2Dwords to transfer   |

Table continues on the next page...

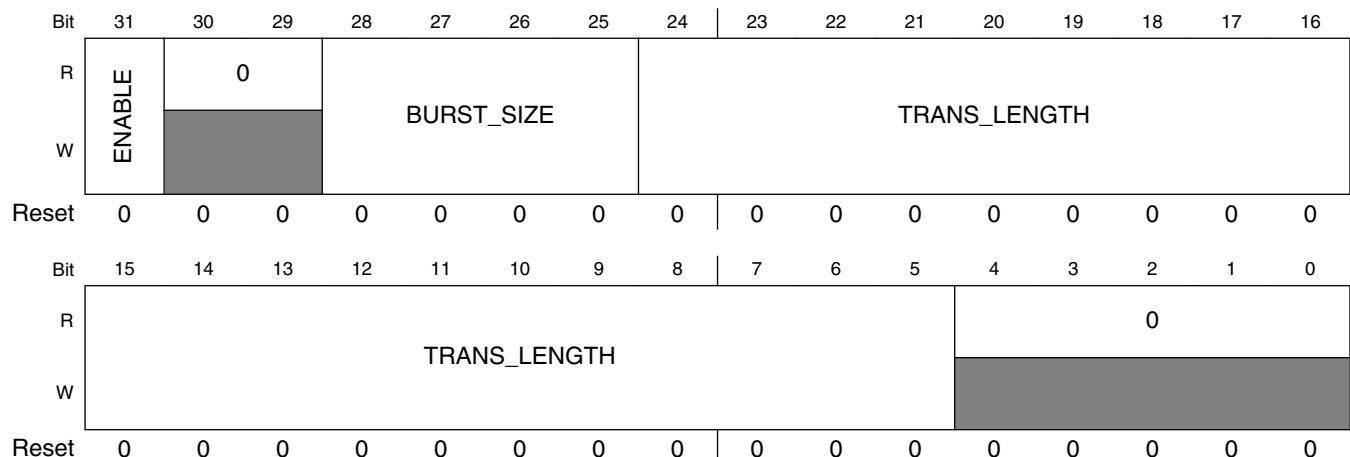
**MIPI\_HSI\_TDMA $n$ \_CONF field descriptions (continued)**

| Field    | Description  |
|----------|--|
|          | fffff 1048575Dwords to transfer                              |
| Reserved | This read-only field is reserved and always has the value 0. |

## 42.5.25 Rx DMA Channel n Configuration Register (MIPI\_HSI\_RDMA $n$ \_CONF)

This register contains the configurations of enable/disable, burst size and transfer count for Rx DMA channel n.

Address: 220\_8000h base + 11Ch offset + (4d × i), where i=0d to 15d

**MIPI\_HSI\_RDMA $n$ \_CONF field descriptions**

| Field                | Description  |
|----------------------|--|
| 31<br>ENABLE         | Setting this bit enables the internal Rx DMA channel n.  |
| 30–29<br>Reserved    | This read-only field is reserved and always has the value 0.   |
| 28–25<br>BURST_SIZE  | Burst size for Rx DMA channel n. The unit is Dword.<br>The burst size should not be larger than relevant TRANS_LENGTH and FIFO_SIZE.<br>h0 1Dword to transfer for each burst<br>h1 2Dword to transfer for each burst<br>h2 4Dword to transfer for each burst<br>h10 1024Dword to transfer for each burst |
| 24–5<br>TRANS_LENGTH | Transfer data length for Rx DMA channel 0. The unit is Dword.<br>h1 1Dword to transfer   |

*Table continues on the next page...*

**MIPI\_HSI\_RDMA $n$ \_CONF field descriptions (continued)**

| Field    | Description  |
|----------|--|
|          | h2 2Dwords to transfer<br>hfffff 1048575Dwords to transfer   |
| Reserved | This read-only field is reserved and always has the value 0. |

**42.5.26 Tx DMA Channel n Start Address Register (MIPI\_HSI\_TDMA $n$ \_STA\_ADDR)**

This Register contains the physical Start Address HSI for Tx DMA Channel n.

Address: 220\_8000h base + 15Ch offset + (4d × i), where i=0d to 15d

| Bit | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R   | DS_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0 |   |   |   |
| W   |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0 |   |   |   |

**MIPI\_HSI\_TDMA $n$ \_STA\_ADDR field descriptions**

| Field           | Description  |
|-----------------|--|
| 31–2<br>DS_ADDR | The Physical Start Address for Tx DMA Channel n. DWord aligned |
| Reserved        | This read-only field is reserved and always has the value 0.   |

**42.5.27 Rx DMA Channel n Start Address Register (MIPI\_HSI\_RDMA $n$ \_STA\_ADDR)**

This Register contains the physical Start Address HSI for Rx DMA Channel n.

Address: 220\_8000h base + 19Ch offset + (4d × i), where i=0d to 15d

| Bit | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R   | DS_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0 |   |   |   |
| W   |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0 |   |   |   |

**MIPI\_HSI\_RDMA $n$ \_STA\_ADDR field descriptions**

| Field           | Description  |
|-----------------|--|
| 31–2<br>DS_ADDR | The Physical Start Address for Rx DMA Channel n. DWord aligned |
| Reserved        | This read-only field is reserved and always has the value 0.   |

## 42.5.28 DMA Interrupt Status Register (MIPI\_HSI\_DMA\_IRQSTAT)

This register contains all the interrupt status for HSI internal DMA

Address: 220\_8000h base + 1DCh offset = 220\_81DCh

| Bit   | 31     | 30     | 29     | 28     | 27     | 26     | 25    | 24    | 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| R     | TDMA15 | TDMA14 | TDMA13 | TDMA12 | TDMA11 | TDMA10 | TDMA9 | TDMA8 | TDMA7 | TDMA6 | TDMA5 | TDMA4 | TDMA3 | TDMA2 | TDMA1 | TDMA0 |
| W     |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Bit   | 15     | 14     | 13     | 12     | 11     | 10     | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| R     | RDMA15 | RDMA14 | RDMA13 | RDMA12 | RDMA11 | RDMA10 | RDMA9 | RDMA8 | RDMA7 | RDMA6 | RDMA5 | RDMA4 | RDMA3 | RDMA2 | RDMA1 | RDMA0 |
| W     |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**MIPI\_HSI\_DMA\_IRQSTAT field descriptions**

| Field        | Description                      |
|--------------|----------------------------------|
| 31<br>TDMA15 | TDMA Channel 15 interrupt status |
| 30<br>TDMA14 | TDMA Channel 14 interrupt status |
| 29<br>TDMA13 | TDMA Channel 13 interrupt status |
| 28<br>TDMA12 | TDMA Channel 12 interrupt status |
| 27<br>TDMA11 | TDMA Channel 11 interrupt status |
| 26<br>TDMA10 | TDMA Channel 10 interrupt status |
| 25<br>TDMA9  | TDMA Channel 9 interrupt status  |
| 24<br>TDMA8  | TDMA Channel 8 interrupt status  |
| 23<br>TDMA7  | TDMA Channel 7 interrupt status  |
| 22<br>TDMA6  | TDMA Channel 6 interrupt status  |
| 21<br>TDMA5  | TDMA Channel 5 interrupt status  |
| 20<br>TDMA4  | TDMA Channel 4 interrupt status  |
| 19<br>TDMA3  | TDMA Channel 3 interrupt status  |
| 18<br>TDMA2  | TDMA Channel 2 interrupt status  |
| 17<br>TDMA1  | TDMA Channel 1 interrupt status  |
| 16<br>TDMA0  | TDMA Channel 0 interrupt status  |
| 15<br>RDMA15 | RDMA Channel 15 interrupt status |
| 14<br>RDMA14 | RDMA Channel 14 interrupt status |
| 13<br>RDMA13 | RDMA Channel 13 interrupt status |
| 12<br>RDMA12 | RDMA Channel 12 interrupt status |
| 11<br>RDMA11 | RDMA Channel 11 interrupt status |
| 10<br>RDMA10 | RDMA Channel 10 interrupt status |
| 9<br>RDMA9   | RDMA Channel 9 interrupt status  |

*Table continues on the next page...*

**MIPI\_HSI\_DMA\_IRQSTAT field descriptions (continued)**

| Field      | Description                     |
|------------|---------------------------------|
| 8<br>RDMA8 | RDMA Channel 8 interrupt status |
| 7<br>RDMA7 | RDMA Channel 7 interrupt status |
| 6<br>RDMA6 | RDMA Channel 6 interrupt status |
| 5<br>RDMA5 | RDMA Channel 5 interrupt status |
| 4<br>RDMA4 | RDMA Channel 4 interrupt status |
| 3<br>RDMA3 | RDMA Channel 3 interrupt status |
| 2<br>RDMA2 | RDMA Channel 2 interrupt status |
| 1<br>RDMA1 | RDMA Channel 1 interrupt status |
| 0<br>RDMA0 | RDMA Channel 0 interrupt status |

### 42.5.29 DMA Interrupt Enable Register (**MIPI\_HSI\_DMA\_IRQSTAT\_EN**)

This Register is used to select which DMA interrupt could send to HIS Interrupt Status Register

Address: 220\_8000h base + 1E0h offset = 220\_81E0h

| Bit   | 31     | 30     | 29     | 28     | 27     | 26     | 25    | 24    | 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| R     | TDMA15 | TDMA14 | TDMA13 | TDMA12 | TDMA11 | TDMA10 | TDMA9 | TDMA8 | TDMA7 | TDMA6 | TDMA5 | TDMA4 | TDMA3 | TDMA2 | TDMA1 | TDMA0 |
| W     | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Bit   | 15     | 14     | 13     | 12     | 11     | 10     | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| R     | RDMA15 | RDMA14 | RDMA13 | RDMA12 | RDMA11 | RDMA10 | RDMA9 | RDMA8 | RDMA7 | RDMA6 | RDMA5 | RDMA4 | RDMA3 | RDMA2 | RDMA1 | RDMA0 |
| W     | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**MIPI\_HSI\_DMA\_IRQSTAT\_EN field descriptions**

| Field        | Description                      |
|--------------|----------------------------------|
| 31<br>TDMA15 | TDMA Channel 15 interrupt Enable |
| 30<br>TDMA14 | TDMA Channel 14 interrupt Enable |
| 29<br>TDMA13 | TDMA Channel 13 interrupt Enable |
| 28<br>TDMA12 | TDMA Channel 12 interrupt Enable |
| 27<br>TDMA11 | TDMA Channel 11 interrupt Enable |
| 26<br>TDMA10 | TDMA Channel 10 interrupt Enable |
| 25<br>TDMA9  | TDMA Channel 9 interrupt Enable  |
| 24<br>TDMA8  | TDMA Channel 8 interrupt Enable  |
| 23<br>TDMA7  | TDMA Channel 7 interrupt Enable  |
| 22<br>TDMA6  | TDMA Channel 6 interrupt Enable  |
| 21<br>TDMA5  | TDMA Channel 5 interrupt Enable  |
| 20<br>TDMA4  | TDMA Channel 4 interrupt Enable  |
| 19<br>TDMA3  | TDMA Channel 3 interrupt Enable  |
| 18<br>TDMA2  | TDMA Channel 2 interrupt Enable  |
| 17<br>TDMA1  | TDMA Channel 1 interrupt Enable  |
| 16<br>TDMA0  | TDMA Channel 0 interrupt Enable  |
| 15<br>RDMA15 | RDMA Channel 15 interrupt Enable |
| 14<br>RDMA14 | RDMA Channel 14 interrupt Enable |
| 13<br>RDMA13 | RDMA Channel 13 interrupt Enable |
| 12<br>RDMA12 | RDMA Channel 12 interrupt Enable |
| 11<br>RDMA11 | RDMA Channel 11 interrupt Enable |
| 10<br>RDMA10 | RDMA Channel 10 interrupt Enable |
| 9<br>RDMA9   | RDMA Channel 9 interrupt Enable  |

*Table continues on the next page...*

**MIPI\_HSI\_DMA\_IRQSTAT\_EN field descriptions (continued)**

| Field      | Description                     |
|------------|---------------------------------|
| 8<br>RDMA8 | RDMA Channel 8 interrupt Enable |
| 7<br>RDMA7 | RDMA Channel 7 interrupt Enable |
| 6<br>RDMA6 | RDMA Channel 6 interrupt Enable |
| 5<br>RDMA5 | RDMA Channel 5 interrupt Enable |
| 4<br>RDMA4 | RDMA Channel 4 interrupt Enable |
| 3<br>RDMA3 | RDMA Channel 3 interrupt Enable |
| 2<br>RDMA2 | RDMA Channel 2 interrupt Enable |
| 1<br>RDMA1 | RDMA Channel 1 interrupt Enable |
| 0<br>RDMA0 | RDMA Channel 0 interrupt Enable |

### 42.5.30 DMA Interrupt Status Signal Enable Register (MIPI\_HSI\_DMA\_IRQSIG\_EN)

This Register is used to select which DMA interrupt status could send to HIS Interrupt Status Register

Address: 220\_8000h base + 1E4h offset = 220\_81E4h

| Bit   | 31     | 30     | 29     | 28     | 27     | 26     | 25    | 24    | 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| R     | TDMA15 | TDMA14 | TDMA13 | TDMA12 | TDMA11 | TDMA10 | TDMA9 | TDMA8 | TDMA7 | TDMA6 | TDMA5 | TDMA4 | TDMA3 | TDMA2 | TDMA1 | TDMA0 |
| W     | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Bit   | 15     | 14     | 13     | 12     | 11     | 10     | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| R     | RDMA15 | RDMA14 | RDMA13 | RDMA12 | RDMA11 | RDMA10 | RDMA9 | RDMA8 | RDMA7 | RDMA6 | RDMA5 | RDMA4 | RDMA3 | RDMA2 | RDMA1 | RDMA0 |
| W     | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**MIPI\_HSI\_DMA\_IRQSIG\_EN field descriptions**

| Field        | Description                             |
|--------------|---|
| 31<br>TDMA15 | TDMA Channel 15 interrupt status enable |
| 30<br>TDMA14 | TDMA Channel 14 interrupt status enable |
| 29<br>TDMA13 | TDMA Channel 13 interrupt status enable |
| 28<br>TDMA12 | TDMA Channel 12 interrupt status enable |
| 27<br>TDMA11 | TDMA Channel 11 interrupt status enable |
| 26<br>TDMA10 | TDMA Channel 10 interrupt status enable |
| 25<br>TDMA9  | TDMA Channel 9 interrupt status enable  |
| 24<br>TDMA8  | TDMA Channel 8 interrupt status enable  |
| 23<br>TDMA7  | TDMA Channel 7 interrupt status enable  |
| 22<br>TDMA6  | TDMA Channel 6 interrupt status enable  |
| 21<br>TDMA5  | TDMA Channel 5 interrupt status enable  |
| 20<br>TDMA4  | TDMA Channel 4 interrupt status enable  |
| 19<br>TDMA3  | TDMA Channel 3 interrupt status enable  |
| 18<br>TDMA2  | TDMA Channel 2 interrupt status enable  |
| 17<br>TDMA1  | TDMA Channel 1 interrupt status enable  |
| 16<br>TDMA0  | TDMA Channel 0 interrupt status enable  |
| 15<br>RDMA15 | RDMA Channel 15 interrupt status enable |
| 14<br>RDMA14 | RDMA Channel 14 interrupt status enable |
| 13<br>RDMA13 | RDMA Channel 13 interrupt status enable |
| 12<br>RDMA12 | RDMA Channel 12 interrupt status enable |
| 11<br>RDMA11 | RDMA Channel 11 interrupt status enable |
| 10<br>RDMA10 | RDMA Channel 10 interrupt status enable |
| 9<br>RDMA9   | RDMA Channel 9 interrupt status enable  |

*Table continues on the next page...*

**MIPI\_HSI\_DMA IRQSIG\_EN field descriptions (continued)**

| Field      | Description                            |
|------------|--|
| 8<br>RDMA8 | RDMA Channel 8 interrupt status enable |
| 7<br>RDMA7 | RDMA Channel 7 interrupt status enable |
| 6<br>RDMA6 | RDMA Channel 6 interrupt status enable |
| 5<br>RDMA5 | RDMA Channel 5 interrupt status enable |
| 4<br>RDMA4 | RDMA Channel 4 interrupt status enable |
| 3<br>RDMA3 | RDMA Channel 3 interrupt status enable |
| 2<br>RDMA2 | RDMA Channel 2 interrupt status enable |
| 1<br>RDMA1 | RDMA Channel 1 interrupt status enable |
| 0<br>RDMA0 | RDMA Channel 0 interrupt status enable |

### 42.5.31 DMA Error Interrupt Status Register (MIPI\_HSI\_DMA\_ERR\_IRQSTAT)

This register contains all the error interrupt status for HSI internal DMA

Address: 220\_8000h base + 1E8h offset = 220\_81E8h

| Bit   | 31     | 30     | 29     | 28     | 27     | 26     | 25    | 24    | 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| R     | TDMA15 | TDMA14 | TDMA13 | TDMA12 | TDMA11 | TDMA10 | TDMA9 | TDMA8 | TDMA7 | TDMA6 | TDMA5 | TDMA4 | TDMA3 | TDMA2 | TDMA1 | TDMA0 |
| W     |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Bit   | 15     | 14     | 13     | 12     | 11     | 10     | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| R     | RDMA15 | RDMA14 | RDMA13 | RDMA12 | RDMA11 | RDMA10 | RDMA9 | RDMA8 | RDMA7 | RDMA6 | RDMA5 | RDMA4 | RDMA3 | RDMA2 | RDMA1 | RDMA0 |
| W     |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**MIPI\_HSI\_DMA\_ERR\_IRQSTAT field descriptions**

| Field        | Description                            |
|--------------|--|
| 31<br>TDMA15 | TDMA Channel 15 error interrupt status |
| 30<br>TDMA14 | TDMA Channel 14 error interrupt status |

*Table continues on the next page...*

**MIPI\_HSI\_DMA\_ERR\_IRQSTAT field descriptions (continued)**

| Field        | Description                            |
|--------------|--|
| 29<br>TDMA13 | TDMA Channel 13 error interrupt status |
| 28<br>TDMA12 | TDMA Channel 12 error interrupt status |
| 27<br>TDMA11 | TDMA Channel 11 error interrupt status |
| 26<br>TDMA10 | TDMA Channel 10 error interrupt status |
| 25<br>TDMA9  | TDMA Channel 9 error interrupt status  |
| 24<br>TDMA8  | TDMA Channel 8 error interrupt status  |
| 23<br>TDMA7  | TDMA Channel 7 error interrupt status  |
| 22<br>TDMA6  | TDMA Channel 6 error interrupt status  |
| 21<br>TDMA5  | TDMA Channel 5 error interrupt status  |
| 20<br>TDMA4  | TDMA Channel 4 error interrupt status  |
| 19<br>TDMA3  | TDMA Channel 3 error interrupt status  |
| 18<br>TDMA2  | TDMA Channel 2 error interrupt status  |
| 17<br>TDMA1  | TDMA Channel 1 error interrupt status  |
| 16<br>TDMA0  | TDMA Channel 0 error interrupt status  |
| 15<br>RDMA15 | RDMA Channel 15 error interrupt status |
| 14<br>RDMA14 | RDMA Channel 14 error interrupt status |
| 13<br>RDMA13 | RDMA Channel 13 error interrupt status |
| 12<br>RDMA12 | RDMA Channel 12 error interrupt status |
| 11<br>RDMA11 | RDMA Channel 11 error interrupt status |
| 10<br>RDMA10 | RDMA Channel 10 error interrupt status |
| 9<br>RDMA9   | RDMA Channel 9 error interrupt status  |
| 8<br>RDMA8   | RDMA Channel 8 error interrupt status  |
| 7<br>RDMA7   | RDMA Channel 7 error interrupt status  |

*Table continues on the next page...*

**MIPI\_HSI\_DMA\_ERR\_IRQSTAT field descriptions (continued)**

| Field      | Description                           |
|------------|---------------------------------------|
| 6<br>RDMA6 | RDMA Channel 6 error interrupt status |
| 5<br>RDMA5 | RDMA Channel 5 error interrupt status |
| 4<br>RDMA4 | RDMA Channel 4 error interrupt status |
| 3<br>RDMA3 | RDMA Channel 3 error interrupt status |
| 2<br>RDMA2 | RDMA Channel 2 error interrupt status |
| 1<br>RDMA1 | RDMA Channel 1 error interrupt status |
| 0<br>RDMA0 | RDMA Channel 0 error interrupt status |

### 42.5.32 DMA Error Interrupt Enable Register (MIPI\_HSI\_DMA\_ERR\_IRQSTAT\_EN)

This register is used to select which DMA error interrupt could send to HIS Interrupt Status Register

Address: 220\_8000h base + 1ECh offset = 220\_81ECh

|       |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit   | 31     | 30     | 29     | 28     | 27     | 26     | 25    | 24    | 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
| R     | TDMA15 | TDMA14 | TDMA13 | TDMA12 | TDMA11 | TDMA10 | TDMA9 | TDMA8 | TDMA7 | TDMA6 | TDMA5 | TDMA4 | TDMA3 | TDMA2 | TDMA1 | TDMA0 |
| W     | TDMA15 | TDMA14 | TDMA13 | TDMA12 | TDMA11 | TDMA10 | TDMA9 | TDMA8 | TDMA7 | TDMA6 | TDMA5 | TDMA4 | TDMA3 | TDMA2 | TDMA1 | TDMA0 |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Bit   | 15     | 14     | 13     | 12     | 11     | 10     | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| R     | RDMA15 | RDMA14 | RDMA13 | RDMA12 | RDMA11 | RDMA10 | RDMA9 | RDMA8 | RDMA7 | RDMA6 | RDMA5 | RDMA4 | RDMA3 | RDMA2 | RDMA1 | RDMA0 |
| W     | RDMA15 | RDMA14 | RDMA13 | RDMA12 | RDMA11 | RDMA10 | RDMA9 | RDMA8 | RDMA7 | RDMA6 | RDMA5 | RDMA4 | RDMA3 | RDMA2 | RDMA1 | RDMA0 |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**MIPI\_HSI\_DMA\_ERR\_IRQSTAT\_EN field descriptions**

| Field        | Description                            |
|--------------|--|
| 31<br>TDMA15 | TDMA Channel 15 error interrupt enable |

*Table continues on the next page...*

**MIPI\_HSI\_DMA\_ERR\_IRQSTAT\_EN field descriptions (continued)**

| Field        | Description                            |
|--------------|--|
| 30<br>TDMA14 | TDMA Channel 14 error interrupt enable |
| 29<br>TDMA13 | TDMA Channel 13 error interrupt enable |
| 28<br>TDMA12 | TDMA Channel 12 error interrupt enable |
| 27<br>TDMA11 | TDMA Channel 11 error interrupt enable |
| 26<br>TDMA10 | TDMA Channel 10 error interrupt enable |
| 25<br>TDMA9  | TDMA Channel 9 error interrupt enable  |
| 24<br>TDMA8  | TDMA Channel 8 error interrupt enable  |
| 23<br>TDMA7  | TDMA Channel 7 error interrupt enable  |
| 22<br>TDMA6  | TDMA Channel 6 error interrupt enable  |
| 21<br>TDMA5  | TDMA Channel 5 error interrupt enable  |
| 20<br>TDMA4  | TDMA Channel 4 error interrupt enable  |
| 19<br>TDMA3  | TDMA Channel 3 error interrupt enable  |
| 18<br>TDMA2  | TDMA Channel 2 error interrupt enable  |
| 17<br>TDMA1  | TDMA Channel 1 error interrupt enable  |
| 16<br>TDMA0  | TDMA Channel 0 error interrupt enable  |
| 15<br>RDMA15 | RDMA Channel 15 error interrupt enable |
| 14<br>RDMA14 | RDMA Channel 14 error interrupt enable |
| 13<br>RDMA13 | RDMA Channel 13 error interrupt enable |
| 12<br>RDMA12 | RDMA Channel 12 error interrupt enable |
| 11<br>RDMA11 | RDMA Channel 11 error interrupt enable |
| 10<br>RDMA10 | RDMA Channel 10 error interrupt enable |
| 9<br>RDMA9   | RDMA Channel 9 error interrupt enable  |
| 8<br>RDMA8   | RDMA Channel 8 error interrupt enable  |

*Table continues on the next page...*

**MIPI\_HSI\_DMA\_ERR\_IRQSTAT\_EN field descriptions (continued)**

| Field      | Description                           |
|------------|---------------------------------------|
| 7<br>RDMA7 | RDMA Channel 7 error interrupt enable |
| 6<br>RDMA6 | RDMA Channel 6 error interrupt enable |
| 5<br>RDMA5 | RDMA Channel 5 error interrupt enable |
| 4<br>RDMA4 | RDMA Channel 4 error interrupt enable |
| 3<br>RDMA3 | RDMA Channel 3 error interrupt enable |
| 2<br>RDMA2 | RDMA Channel 2 error interrupt enable |
| 1<br>RDMA1 | RDMA Channel 1 error interrupt enable |
| 0<br>RDMA0 | RDMA Channel 0 error interrupt enable |

### 42.5.33 DMA Error Interrupt Signal Enable Register (MIPI\_HSI\_DMA\_ERR\_IRQSIG\_EN)

This Register is used to select which DMA error interrupt status could send to HIS Interrupt Status Register

Address: 220\_8000h base + 1F0h offset = 220\_81F0h

| Bit   | 31     | 30     | 29     | 28     | 27     | 26     | 25    | 24    | 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| R     | TDMA15 | TDMA14 | TDMA13 | TDMA12 | TDMA11 | TDMA10 | TDMA9 | TDMA8 | TDMA7 | TDMA6 | TDMA5 | TDMA4 | TDMA3 | TDMA2 | TDMA1 | TDMA0 |
| W     |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Bit   | 15     | 14     | 13     | 12     | 11     | 10     | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| R     | RDMA15 | RDMA14 | RDMA13 | RDMA12 | RDMA11 | RDMA10 | RDMA9 | RDMA8 | RDMA7 | RDMA6 | RDMA5 | RDMA4 | RDMA3 | RDMA2 | RDMA1 | RDMA0 |
| W     |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**MIPI\_HSI\_DMA\_ERR\_IRQSIG\_EN field descriptions**

| Field        | Description                                   |
|--------------|---|
| 31<br>TDMA15 | TDMA Channel 15 error interrupt status enable |
| 30<br>TDMA14 | TDMA Channel 14 error interrupt status enable |
| 29<br>TDMA13 | TDMA Channel 13 error interrupt status enable |
| 28<br>TDMA12 | TDMA Channel 12 error interrupt status enable |
| 27<br>TDMA11 | TDMA Channel 11 error interrupt status enable |
| 26<br>TDMA10 | TDMA Channel 10 error interrupt status enable |
| 25<br>TDMA9  | TDMA Channel 9 error interrupt status enable  |
| 24<br>TDMA8  | TDMA Channel 8 error interrupt status enable  |
| 23<br>TDMA7  | TDMA Channel 7 error interrupt status enable  |
| 22<br>TDMA6  | TDMA Channel 6 error interrupt status enable  |
| 21<br>TDMA5  | TDMA Channel 5 error interrupt status enable  |
| 20<br>TDMA4  | TDMA Channel 4 error interrupt status enable  |
| 19<br>TDMA3  | TDMA Channel 3 error interrupt status enable  |
| 18<br>TDMA2  | TDMA Channel 2 error interrupt status enable  |
| 17<br>TDMA1  | TDMA Channel 1 error interrupt status enable  |
| 16<br>TDMA0  | TDMA Channel 0 error interrupt status enable  |
| 15<br>RDMA15 | RDMA Channel 15 error interrupt status enable |
| 14<br>RDMA14 | RDMA Channel 14 error interrupt status enable |
| 13<br>RDMA13 | RDMA Channel 13 error interrupt status enable |
| 12<br>RDMA12 | RDMA Channel 12 error interrupt status enable |
| 11<br>RDMA11 | RDMA Channel 11 error interrupt status enable |
| 10<br>RDMA10 | RDMA Channel 10 error interrupt status enable |
| 9<br>RDMA9   | RDMA Channel 9 error interrupt status enable  |

*Table continues on the next page...*

**MIPI\_HSI\_DMA\_ERR\_IRQSIG\_EN field descriptions (continued)**

| Field      | Description                                  |
|------------|--|
| 8<br>RDMA8 | RDMA Channel 8 error interrupt status enable |
| 7<br>RDMA7 | RDMA Channel 7 error interrupt status enable |
| 6<br>RDMA6 | RDMA Channel 6 error interrupt status enable |
| 5<br>RDMA5 | RDMA Channel 5 error interrupt status enable |
| 4<br>RDMA4 | RDMA Channel 4 error interrupt status enable |
| 3<br>RDMA3 | RDMA Channel 3 error interrupt status enable |
| 2<br>RDMA2 | RDMA Channel 2 error interrupt status enable |
| 1<br>RDMA1 | RDMA Channel 1 error interrupt status enable |
| 0<br>RDMA0 | RDMA Channel 0 error interrupt status enable |

### 42.5.34 DMA Single Request Enable Register (MIPI\_HSI\_DMA\_SINGLE\_REQ\_EN)

This Register is used to debug

Address: 220\_8000h base + 1F4h offset = 220\_81F4h

| Bit   | 31     | 30     | 29     | 28     | 27     | 26     | 25    | 24    | 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| R     | TDMA15 | TDMA14 | TDMA13 | TDMA12 | TDMA11 | TDMA10 | TDMA9 | TDMA8 | TDMA7 | TDMA6 | TDMA5 | TDMA4 | TDMA3 | TDMA2 | TDMA1 | TDMA0 |
| W     |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Bit   | 15     | 14     | 13     | 12     | 11     | 10     | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| R     | RDMA15 | RDMA14 | RDMA13 | RDMA12 | RDMA11 | RDMA10 | RDMA9 | RDMA8 | RDMA7 | RDMA6 | RDMA5 | RDMA4 | RDMA3 | RDMA2 | RDMA1 | RDMA0 |
| W     |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

#### MIPI\_HSI\_DMA\_SINGLE\_REQ\_EN field descriptions

| Field     | Description   |
|-----------|---|
| 31 TDMA15 | When the remain DMA data less than one DMA burst size in Tx Dma Channe 15, this bit will be set automatically |
| 30 TDMA14 | When the remain DMA data less than one DMA burst size in Tx Dma Channe 14, this bit will be set automatically |

Table continues on the next page...

**MIPI\_HSI\_DMA\_SINGLE\_REQ\_EN field descriptions (continued)**

| Field        | Description   |
|--------------|---|
| 29<br>TDMA13 | When the remain DMA data less than one DMA burst size in Tx Dma Channe 13, this bit will be set automatically |
| 28<br>TDMA12 | When the remain DMA data less than one DMA burst size in Tx Dma Channe 12, this bit will be set automatically |
| 27<br>TDMA11 | When the remain DMA data less than one DMA burst size in Tx Dma Channe 11, this bit will be set automatically |
| 26<br>TDMA10 | When the remain DMA data less than one DMA burst size in Tx Dma Channe 10, this bit will be set automatically |
| 25<br>TDMA9  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 9, this bit will be set automatically  |
| 24<br>TDMA8  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 8, this bit will be set automatically  |
| 23<br>TDMA7  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 7, this bit will be set automatically  |
| 22<br>TDMA6  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 6, this bit will be set automatically  |
| 21<br>TDMA5  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 5, this bit will be set automatically  |
| 20<br>TDMA4  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 4, this bit will be set automatically  |
| 19<br>TDMA3  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 3, this bit will be set automatically  |
| 18<br>TDMA2  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 2, this bit will be set automatically  |
| 17<br>TDMA1  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 1, this bit will be set automatically  |
| 16<br>TDMA0  | When the remain DMA data less than one DMA burst size in Tx Dma Channe 0, this bit will be set automatically  |
| 15<br>RDMA15 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 15, this bit will be set automatically |
| 14<br>RDMA14 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 14, this bit will be set automatically |
| 13<br>RDMA13 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 13, this bit will be set automatically |
| 12<br>RDMA12 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 12, this bit will be set automatically |
| 11<br>RDMA11 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 11, this bit will be set automatically |
| 10<br>RDMA10 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 10, this bit will be set automatically |
| 9<br>RDMA9   | When the remain DMA data less than one DMA burst size in Rx Dma Channe 9, this bit will be set automatically  |
| 8<br>RDMA8   | When the remain DMA data less than one DMA burst size in Rx Dma Channe 8, this bit will be set automatically  |
| 7<br>RDMA7   | When the remain DMA data less than one DMA burst size in Rx Dma Channe 7, this bit will be set automatically  |

*Table continues on the next page...*

**MIPI\_HSI\_DMA\_SINGLE\_REQ\_EN field descriptions (continued)**

| Field      | Description  |
|------------|--|
| 6<br>RDMA6 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 6, this bit will be set automatically |
| 5<br>RDMA5 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 5, this bit will be set automatically |
| 4<br>RDMA4 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 4, this bit will be set automatically |
| 3<br>RDMA3 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 3, this bit will be set automatically |
| 2<br>RDMA2 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 2, this bit will be set automatically |
| 1<br>RDMA1 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 1, this bit will be set automatically |
| 0<br>RDMA0 | When the remain DMA data less than one DMA burst size in Rx Dma Channe 0, this bit will be set automatically |

### 42.5.35 Tx Fifo Size Configuration Register 0 (**MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF0**)

This register is used to config each Tx fifo size

Address: 220\_8000h base + 200h offset = 220\_8200h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| W   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

Reset 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1

**MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF0 field descriptions**

| Field         | Description   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
|---------------|---|------|----------------------------------|------|-----------------------------------|------|-----------------------------------|------|-----------------------------------|------|------------------------------------|------|------------------------------------|------|------------------------------------|------|-------------------------------------|------|-------------------------------------|------|-------------------------------------|
| 31–28<br>CH15 | <p>This field is used to set the buffer size for channel 15.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 15 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 15 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 15 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 15 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 15 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 15 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 15 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 15 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 15 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 15 buffer size is 512Dwords</td></tr> </tbody> </table> | 0000 | channel 15 buffer size is 1Dword | 0001 | channel 15 buffer size is 2Dwords | 0010 | channel 15 buffer size is 4Dwords | 0011 | channel 15 buffer size is 8Dwords | 0100 | channel 15 buffer size is 16Dwords | 0101 | channel 15 buffer size is 32Dwords | 0110 | channel 15 buffer size is 64Dwords | 0111 | channel 15 buffer size is 128Dwords | 1000 | channel 15 buffer size is 256Dwords | 1001 | channel 15 buffer size is 512Dwords |
| 0000          | channel 15 buffer size is 1Dword  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
| 0001          | channel 15 buffer size is 2Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
| 0010          | channel 15 buffer size is 4Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
| 0011          | channel 15 buffer size is 8Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
| 0100          | channel 15 buffer size is 16Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
| 0101          | channel 15 buffer size is 32Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
| 0110          | channel 15 buffer size is 64Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
| 0111          | channel 15 buffer size is 128Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
| 1000          | channel 15 buffer size is 256Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |
| 1001          | channel 15 buffer size is 512Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF0 field descriptions (continued)**

| Field         | Description   |
|---------------|---|
|               | 1010 channel 15 buffer size is 1024Dwords<br>1111-1011 Reserved   |
| 27–24<br>CH14 | <p>This field is used to set the buffer size for channel 14.<br/>All the allowed combinations of bit setting are listed here .</p> <p>0000 channel 14 buffer size is 1Dword<br/>           0001 channel 14 buffer size is 2Dwords<br/>           0010 channel 14 buffer size is 4Dwords<br/>           0011 channel 14 buffer size is 8Dwords<br/>           0100 channel 14 buffer size is 16Dwords<br/>           0101 channel 14 buffer size is 32Dwords<br/>           0110 channel 14 buffer size is 64Dwords<br/>           0111 channel 14 buffer size is 128Dwords<br/>           1000 channel 14 buffer size is 256Dwords<br/>           1001 channel 14 buffer size is 512Dwords<br/>           1010 channel 14 buffer size is 1024Dwords<br/>           1111-1011 Reserved</p> |
| 23–20<br>CH13 | <p>This field is used to set the buffer size for channel 13.<br/>All the allowed combinations of bit setting are listed here .</p> <p>0000 channel 13 buffer size is 1Dword<br/>           0001 channel 13 buffer size is 2Dwords<br/>           0010 channel 13 buffer size is 4Dwords<br/>           0011 channel 13 buffer size is 8Dwords<br/>           0100 channel 13 buffer size is 16Dwords<br/>           0101 channel 13 buffer size is 32Dwords<br/>           0110 channel 13 buffer size is 64Dwords<br/>           0111 channel 13 buffer size is 128Dwords<br/>           1000 channel 13 buffer size is 256Dwords<br/>           1001 channel 13 buffer size is 512Dwords<br/>           1010 channel 13 buffer size is 1024Dwords<br/>           1111-1011 Reserved</p> |
| 19–16<br>CH12 | <p>This field is used to set the buffer size for channel 12.<br/>All the allowed combinations of bit setting are listed here .</p> <p>0000 channel 12 buffer size is 1Dword<br/>           0001 channel 12 buffer size is 2Dwords<br/>           0010 channel 12 buffer size is 4Dwords<br/>           0011 channel 12 buffer size is 8Dwords<br/>           0100 channel 12 buffer size is 16Dwords<br/>           0101 channel 12 buffer size is 32Dwords<br/>           0110 channel 12 buffer size is 64Dwords<br/>           0111 channel 12 buffer size is 128Dwords<br/>           1000 channel 12 buffer size is 256Dwords<br/>           1001 channel 12 buffer size is 512Dwords<br/>           1010 channel 12 buffer size is 1024Dwords<br/>           1111-1011 Reserved</p> |

Table continues on the next page...

**MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF0 field descriptions (continued)**

| Field         | Description  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
|---------------|--|------|----------------------------------|------|-----------------------------------|------|-----------------------------------|------|-----------------------------------|------|------------------------------------|------|------------------------------------|------|------------------------------------|------|-------------------------------------|------|-------------------------------------|------|-------------------------------------|------|--------------------------------------|-----------|----------|
| 15–12<br>CH11 | <p>This field is used to set the buffer size for channel 11.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 11 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 11 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 11 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 11 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 11 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 11 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 11 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 11 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 11 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 11 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 11 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 11 buffer size is 1Dword | 0001 | channel 11 buffer size is 2Dwords | 0010 | channel 11 buffer size is 4Dwords | 0011 | channel 11 buffer size is 8Dwords | 0100 | channel 11 buffer size is 16Dwords | 0101 | channel 11 buffer size is 32Dwords | 0110 | channel 11 buffer size is 64Dwords | 0111 | channel 11 buffer size is 128Dwords | 1000 | channel 11 buffer size is 256Dwords | 1001 | channel 11 buffer size is 512Dwords | 1010 | channel 11 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000          | channel 11 buffer size is 1Dword   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0001          | channel 11 buffer size is 2Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0010          | channel 11 buffer size is 4Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0011          | channel 11 buffer size is 8Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0100          | channel 11 buffer size is 16Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0101          | channel 11 buffer size is 32Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0110          | channel 11 buffer size is 64Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0111          | channel 11 buffer size is 128Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1000          | channel 11 buffer size is 256Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1001          | channel 11 buffer size is 512Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1010          | channel 11 buffer size is 1024Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1111-1011     | Reserved   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 11–8<br>CH10  | <p>This field is used to set the buffer size for channel 10.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 10 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 10 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 10 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 10 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 10 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 10 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 10 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 10 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 10 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 10 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 10 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 10 buffer size is 1Dword | 0001 | channel 10 buffer size is 2Dwords | 0010 | channel 10 buffer size is 4Dwords | 0011 | channel 10 buffer size is 8Dwords | 0100 | channel 10 buffer size is 16Dwords | 0101 | channel 10 buffer size is 32Dwords | 0110 | channel 10 buffer size is 64Dwords | 0111 | channel 10 buffer size is 128Dwords | 1000 | channel 10 buffer size is 256Dwords | 1001 | channel 10 buffer size is 512Dwords | 1010 | channel 10 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000          | channel 10 buffer size is 1Dword   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0001          | channel 10 buffer size is 2Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0010          | channel 10 buffer size is 4Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0011          | channel 10 buffer size is 8Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0100          | channel 10 buffer size is 16Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0101          | channel 10 buffer size is 32Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0110          | channel 10 buffer size is 64Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0111          | channel 10 buffer size is 128Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1000          | channel 10 buffer size is 256Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1001          | channel 10 buffer size is 512Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1010          | channel 10 buffer size is 1024Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1111-1011     | Reserved   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 7–4<br>CH9    | <p>This field is used to set the buffer size for channel 9.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 9 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 9 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 9 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 9 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 9 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 9 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 9 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 9 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 9 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 9 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 9 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table>             | 0000 | channel 9 buffer size is 1Dword  | 0001 | channel 9 buffer size is 2Dwords  | 0010 | channel 9 buffer size is 4Dwords  | 0011 | channel 9 buffer size is 8Dwords  | 0100 | channel 9 buffer size is 16Dwords  | 0101 | channel 9 buffer size is 32Dwords  | 0110 | channel 9 buffer size is 64Dwords  | 0111 | channel 9 buffer size is 128Dwords  | 1000 | channel 9 buffer size is 256Dwords  | 1001 | channel 9 buffer size is 512Dwords  | 1010 | channel 9 buffer size is 1024Dwords  | 1111-1011 | Reserved |
| 0000          | channel 9 buffer size is 1Dword  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0001          | channel 9 buffer size is 2Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0010          | channel 9 buffer size is 4Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0011          | channel 9 buffer size is 8Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0100          | channel 9 buffer size is 16Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0101          | channel 9 buffer size is 32Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0110          | channel 9 buffer size is 64Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0111          | channel 9 buffer size is 128Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1000          | channel 9 buffer size is 256Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1001          | channel 9 buffer size is 512Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1010          | channel 9 buffer size is 1024Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1111-1011     | Reserved   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| CH8           | This field is used to set the buffer size for channel 8.   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF0 field descriptions (continued)**

| Field     | Description   |
|-----------|---|
|           | All the allowed combinations of bit setting are listed here . |
| 0000      | channel 8 buffer size is 1Dword                               |
| 0001      | channel 8 buffer size is 2Dwords                              |
| 0010      | channel 8 buffer size is 4Dwords                              |
| 0011      | channel 8 buffer size is 8Dwords                              |
| 0100      | channel 8 buffer size is 16Dwords                             |
| 0101      | channel 8 buffer size is 32Dwords                             |
| 0110      | channel 8 buffer size is 64Dwords                             |
| 0111      | channel 8 buffer size is 128Dwords                            |
| 1000      | channel 8 buffer size is 256Dwords                            |
| 1001      | channel 8 buffer size is 512Dwords                            |
| 1010      | channel 8 buffer size is 1024Dwords                           |
| 1111-1011 | Reserved  |

**42.5.36 Tx Fifo Size Configuration Register 1  
(MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF1)**

This register is used to config each Tx fifo size

Address: 220\_8000h base + 204h offset = 220\_8204h

| Bit   | 31  | 30 | 29  | 28 | 27  | 26 | 25  | 24 | 23  | 22 | 21  | 20 | 19  | 18 | 17  | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|----|-----|----|-----|----|-----|----|-----|----|-----|----|-----|----|-----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R     | CH7 |    | CH6 |    | CH5 |    | CH4 |    | CH3 |    | CH2 |    | CH1 |    | CH0 |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| W     | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |   |
| Reset | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |   |

**MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF1 field descriptions**

| Field        | Description   |
|--------------|---|
| 31–28<br>CH7 | This field is used to set the buffer size for channel 7.<br>All the allowed combinations of bit setting are listed here . |
| 0000         | channel 7 buffer size is 1Dword   |
| 0001         | channel 7 buffer size is 2Dwords  |
| 0010         | channel 7 buffer size is 4Dwords  |
| 0011         | channel 7 buffer size is 8Dwords  |
| 0100         | channel 7 buffer size is 16Dwords   |
| 0101         | channel 7 buffer size is 32Dwords   |
| 0110         | channel 7 buffer size is 64Dwords   |
| 0111         | channel 7 buffer size is 128Dwords  |
| 1000         | channel 7 buffer size is 256Dwords  |
| 1001         | channel 7 buffer size is 512Dwords  |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF1 field descriptions (continued)**

| Field        | Description   |
|--------------|---|
|              | 1010 channel 7 buffer size is 1024Dwords<br>1111-1011 Reserved  |
| 27–24<br>CH6 | <p>This field is used to set the buffer size for channel 6.</p> <p>All the allowed combinations of bit setting are listed here .</p> <ul style="list-style-type: none"> <li>0000 channel 6 buffer size is 1Dword</li> <li>0001 channel 6 buffer size is 2Dwords</li> <li>0010 channel 6 buffer size is 4Dwords</li> <li>0011 channel 6 buffer size is 8Dwords</li> <li>0100 channel 6 buffer size is 16Dwords</li> <li>0101 channel 6 buffer size is 32Dwords</li> <li>0110 channel 6 buffer size is 64Dwords</li> <li>0111 channel 6 buffer size is 128Dwords</li> <li>1000 channel 6 buffer size is 256Dwords</li> <li>1001 channel 6 buffer size is 512Dwords</li> <li>1010 channel 6 buffer size is 1024Dwords</li> <li>1111-1011 Reserved</li> </ul> |
| 23–20<br>CH5 | <p>This field is used to set the buffer size for channel 5.</p> <p>All the allowed combinations of bit setting are listed here .</p> <ul style="list-style-type: none"> <li>0000 channel 5 buffer size is 1Dword</li> <li>0001 channel 5 buffer size is 2Dwords</li> <li>0010 channel 5 buffer size is 4Dwords</li> <li>0011 channel 5 buffer size is 8Dwords</li> <li>0100 channel 5 buffer size is 16Dwords</li> <li>0101 channel 5 buffer size is 32Dwords</li> <li>0110 channel 5 buffer size is 64Dwords</li> <li>0111 channel 5 buffer size is 128Dwords</li> <li>1000 channel 5 buffer size is 256Dwords</li> <li>1001 channel 5 buffer size is 512Dwords</li> <li>1010 channel 5 buffer size is 1024Dwords</li> <li>1111-1011 Reserved</li> </ul> |
| 19–16<br>CH4 | <p>This field is used to set the buffer size for channel 4.</p> <p>All the allowed combinations of bit setting are listed here .</p> <ul style="list-style-type: none"> <li>0000 channel 4 buffer size is 1Dword</li> <li>0001 channel 4 buffer size is 2Dwords</li> <li>0010 channel 4 buffer size is 4Dwords</li> <li>0011 channel 4 buffer size is 8Dwords</li> <li>0100 channel 4 buffer size is 16Dwords</li> <li>0101 channel 4 buffer size is 32Dwords</li> <li>0110 channel 4 buffer size is 64Dwords</li> <li>0111 channel 4 buffer size is 128Dwords</li> <li>1000 channel 4 buffer size is 256Dwords</li> <li>1001 channel 4 buffer size is 512Dwords</li> <li>1010 channel 4 buffer size is 1024Dwords</li> <li>1111-1011 Reserved</li> </ul> |

Table continues on the next page...

**MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF1 field descriptions (continued)**

| Field        | Description  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
|--------------|--|------|---------------------------------|------|----------------------------------|------|----------------------------------|------|----------------------------------|------|-----------------------------------|------|-----------------------------------|------|-----------------------------------|------|------------------------------------|------|------------------------------------|------|------------------------------------|------|-------------------------------------|-----------|----------|
| 15–12<br>CH3 | <p>This field is used to set the buffer size for channel 3.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 3 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 3 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 3 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 3 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 3 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 3 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 3 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 3 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 3 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 3 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 3 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 3 buffer size is 1Dword | 0001 | channel 3 buffer size is 2Dwords | 0010 | channel 3 buffer size is 4Dwords | 0011 | channel 3 buffer size is 8Dwords | 0100 | channel 3 buffer size is 16Dwords | 0101 | channel 3 buffer size is 32Dwords | 0110 | channel 3 buffer size is 64Dwords | 0111 | channel 3 buffer size is 128Dwords | 1000 | channel 3 buffer size is 256Dwords | 1001 | channel 3 buffer size is 512Dwords | 1010 | channel 3 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000         | channel 3 buffer size is 1Dword  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0001         | channel 3 buffer size is 2Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0010         | channel 3 buffer size is 4Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0011         | channel 3 buffer size is 8Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0100         | channel 3 buffer size is 16Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0101         | channel 3 buffer size is 32Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0110         | channel 3 buffer size is 64Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0111         | channel 3 buffer size is 128Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1000         | channel 3 buffer size is 256Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1001         | channel 3 buffer size is 512Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1010         | channel 3 buffer size is 1024Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1111-1011    | Reserved   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 11–8<br>CH2  | <p>This field is used to set the buffer size for channel 2.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 2 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 2 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 2 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 2 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 2 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 2 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 2 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 2 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 2 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 2 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 2 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 2 buffer size is 1Dword | 0001 | channel 2 buffer size is 2Dwords | 0010 | channel 2 buffer size is 4Dwords | 0011 | channel 2 buffer size is 8Dwords | 0100 | channel 2 buffer size is 16Dwords | 0101 | channel 2 buffer size is 32Dwords | 0110 | channel 2 buffer size is 64Dwords | 0111 | channel 2 buffer size is 128Dwords | 1000 | channel 2 buffer size is 256Dwords | 1001 | channel 2 buffer size is 512Dwords | 1010 | channel 2 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000         | channel 2 buffer size is 1Dword  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0001         | channel 2 buffer size is 2Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0010         | channel 2 buffer size is 4Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0011         | channel 2 buffer size is 8Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0100         | channel 2 buffer size is 16Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0101         | channel 2 buffer size is 32Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0110         | channel 2 buffer size is 64Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0111         | channel 2 buffer size is 128Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1000         | channel 2 buffer size is 256Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1001         | channel 2 buffer size is 512Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1010         | channel 2 buffer size is 1024Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1111-1011    | Reserved   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 7–4<br>CH1   | <p>This field is used to set the buffer size for channel 1.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 1 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 1 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 1 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 1 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 1 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 1 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 1 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 1 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 1 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 1 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 1 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 1 buffer size is 1Dword | 0001 | channel 1 buffer size is 2Dwords | 0010 | channel 1 buffer size is 4Dwords | 0011 | channel 1 buffer size is 8Dwords | 0100 | channel 1 buffer size is 16Dwords | 0101 | channel 1 buffer size is 32Dwords | 0110 | channel 1 buffer size is 64Dwords | 0111 | channel 1 buffer size is 128Dwords | 1000 | channel 1 buffer size is 256Dwords | 1001 | channel 1 buffer size is 512Dwords | 1010 | channel 1 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000         | channel 1 buffer size is 1Dword  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0001         | channel 1 buffer size is 2Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0010         | channel 1 buffer size is 4Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0011         | channel 1 buffer size is 8Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0100         | channel 1 buffer size is 16Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0101         | channel 1 buffer size is 32Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0110         | channel 1 buffer size is 64Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0111         | channel 1 buffer size is 128Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1000         | channel 1 buffer size is 256Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1001         | channel 1 buffer size is 512Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1010         | channel 1 buffer size is 1024Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1111-1011    | Reserved   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| CH0          | This field is used to set the buffer size for channel 0.   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_FIFO\_SIZE\_CONF1 field descriptions (continued)**

| Field     | Description   |
|-----------|---|
|           | All the allowed combinations of bit setting are listed here . |
| 0000      | channel 0 buffer size is 1Dword                               |
| 0001      | channel 0 buffer size is 2Dwords                              |
| 0010      | channel 0 buffer size is 4Dwords                              |
| 0011      | channel 0 buffer size is 8Dwords                              |
| 0100      | channel 0 buffer size is 16Dwords                             |
| 0101      | channel 0 buffer size is 32Dwords                             |
| 0110      | channel 0 buffer size is 64Dwords                             |
| 0111      | channel 0 buffer size is 128Dwords                            |
| 1000      | channel 0 buffer size is 256Dwords                            |
| 1001      | channel 0 buffer size is 512Dwords                            |
| 1010      | channel 0 buffer size is 1024Dwords                           |
| 1111-1011 | Reserved  |

### 42.5.37 Rx Fifo Size Configuration Register 0 (MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF0)

This register is used to config each Rx fifo size

Address: 220\_8000h base + 208h offset = 220\_8208h

| Bit   | 31 | 30   | 29 | 28   | 27 | 26   | 25 | 24   | 23 | 22   | 21 | 20   | 19 | 18  | 17 | 16  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|----|------|----|------|----|------|----|------|----|------|----|------|----|-----|----|-----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R     |    | CH15 |    | CH14 |    | CH13 |    | CH12 |    | CH11 |    | CH10 |    | CH9 |    | CH8 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| W     | 0  | 1    | 0  | 1    | 0  | 1    | 0  | 1    | 0  | 1    | 0  | 1    | 0  | 1   | 0  | 1   | 0  | 1  | 0  | 1  | 0  | 1  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |   |
| Reset | 0  | 1    | 0  | 1    | 0  | 1    | 0  | 1    | 0  | 1    | 0  | 1    | 0  | 1   | 0  | 1   | 0  | 1  | 0  | 1  | 0  | 1  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |   |

**MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF0 field descriptions**

| Field         | Description  |
|---------------|--|
| 31–28<br>CH15 | This field is used to set the buffer size for channel 15.<br>All the allowed combinations of bit setting are listed here . |
| 0000          | channel 15 buffer size is 1Dword   |
| 0001          | channel 15 buffer size is 2Dwords  |
| 0010          | channel 15 buffer size is 4Dwords  |
| 0011          | channel 15 buffer size is 8Dwords  |
| 0100          | channel 15 buffer size is 16Dwords   |
| 0101          | channel 15 buffer size is 32Dwords   |
| 0110          | channel 15 buffer size is 64Dwords   |
| 0111          | channel 15 buffer size is 128Dwords  |
| 1000          | channel 15 buffer size is 256Dwords  |
| 1001          | channel 15 buffer size is 512Dwords  |

*Table continues on the next page...*

**MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF0 field descriptions (continued)**

| Field         | Description  |
|---------------|--|
|               | 1010 channel 15 buffer size is 1024Dwords<br>1111-1011 Reserved  |
| 27–24<br>CH14 | <p>This field is used to set the buffer size for channel 14.<br/>All the allowed combinations of bit setting are listed here .</p> <p>0000 channel 14 buffer size is 1Dword<br/>           0001 channel 14 buffer size is 2Dwords<br/>           0010 channel 14 buffer size is 4Dwords<br/>           0011 channel 14 buffer size is 8Dwords<br/>           0100 channel 14 buffer size is 16Dwords<br/>           0101 channel 14 buffer size is 32Dwords<br/>           0110 channel 14 buffer size is 64Dwords<br/>           0111 channel 14 buffer size is 128Dwords<br/>           1000 channel 14 buffer size is 256Dwords<br/>           1001 channel 14 buffer size is 512Dwords<br/>           1010 channel 14 buffer size is 1024Dwords<br/>           1111-1011 Reserved</p>  |
| 23–20<br>CH13 | <p>This field is used to set the buffer size for channel 13.<br/>All the allowed combinations of bit setting are listed here .</p> <p>0000 channel 13 buffer size is 1Dword<br/>           0001 channel 13 buffer size is 2Dwords<br/>           0010 channel 13 buffer size is 4Dwords<br/>           0011 channel 13 buffer size is 8Dwords<br/>           0100 channel 13 buffer size is 16Dwords<br/>           0101 channel 13 buffer size is 32Dwords<br/>           0110 channel 13 buffer size is 64Dwords<br/>           0111 channel 13 buffer size is 128Dwords<br/>           1000 channel 13 buffer size is 256Dwords<br/>           1001 channel 13 buffer size is 512Dwords<br/>           1010 channel 13 buffer size is 1024Dwords<br/>           1111 b1011 Reserved</p> |
| 19–16<br>CH12 | <p>This field is used to set the buffer size for channel 12.<br/>All the allowed combinations of bit setting are listed here .</p> <p>0000 channel 12 buffer size is 1Dword<br/>           0001 channel 12 buffer size is 2Dwords<br/>           0010 channel 12 buffer size is 4Dwords<br/>           0011 channel 12 buffer size is 8Dwords<br/>           0100 channel 12 buffer size is 16Dwords<br/>           0101 channel 12 buffer size is 32Dwords<br/>           0110 channel 12 buffer size is 64Dwords<br/>           0111 channel 12 buffer size is 128Dwords<br/>           1000 channel 12 buffer size is 256Dwords<br/>           1001 channel 12 buffer size is 512Dwords<br/>           1010 channel 12 buffer size is 1024Dwords<br/>           1111-1011 Reserved</p>  |

Table continues on the next page...

**MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF0 field descriptions (continued)**

| Field         | Description  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
|---------------|--|------|----------------------------------|------|-----------------------------------|------|-----------------------------------|------|-----------------------------------|------|------------------------------------|------|------------------------------------|------|------------------------------------|------|-------------------------------------|------|-------------------------------------|------|-------------------------------------|------|--------------------------------------|-----------|----------|
| 15–12<br>CH11 | <p>This field is used to set the buffer size for channel 11.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 11 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 11 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 11 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 11 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 11 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 11 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 11 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 11 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 11 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 11 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 11 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 11 buffer size is 1Dword | 0001 | channel 11 buffer size is 2Dwords | 0010 | channel 11 buffer size is 4Dwords | 0011 | channel 11 buffer size is 8Dwords | 0100 | channel 11 buffer size is 16Dwords | 0101 | channel 11 buffer size is 32Dwords | 0110 | channel 11 buffer size is 64Dwords | 0111 | channel 11 buffer size is 128Dwords | 1000 | channel 11 buffer size is 256Dwords | 1001 | channel 11 buffer size is 512Dwords | 1010 | channel 11 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000          | channel 11 buffer size is 1Dword   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0001          | channel 11 buffer size is 2Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0010          | channel 11 buffer size is 4Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0011          | channel 11 buffer size is 8Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0100          | channel 11 buffer size is 16Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0101          | channel 11 buffer size is 32Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0110          | channel 11 buffer size is 64Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0111          | channel 11 buffer size is 128Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1000          | channel 11 buffer size is 256Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1001          | channel 11 buffer size is 512Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1010          | channel 11 buffer size is 1024Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1111-1011     | Reserved   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 11–8<br>CH10  | <p>This field is used to set the buffer size for channel 10.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 10 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 10 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 10 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 10 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 10 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 10 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 10 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 10 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 10 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 10 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 10 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 10 buffer size is 1Dword | 0001 | channel 10 buffer size is 2Dwords | 0010 | channel 10 buffer size is 4Dwords | 0011 | channel 10 buffer size is 8Dwords | 0100 | channel 10 buffer size is 16Dwords | 0101 | channel 10 buffer size is 32Dwords | 0110 | channel 10 buffer size is 64Dwords | 0111 | channel 10 buffer size is 128Dwords | 1000 | channel 10 buffer size is 256Dwords | 1001 | channel 10 buffer size is 512Dwords | 1010 | channel 10 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000          | channel 10 buffer size is 1Dword   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0001          | channel 10 buffer size is 2Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0010          | channel 10 buffer size is 4Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0011          | channel 10 buffer size is 8Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0100          | channel 10 buffer size is 16Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0101          | channel 10 buffer size is 32Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0110          | channel 10 buffer size is 64Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0111          | channel 10 buffer size is 128Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1000          | channel 10 buffer size is 256Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1001          | channel 10 buffer size is 512Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1010          | channel 10 buffer size is 1024Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1111-1011     | Reserved   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 7–4<br>CH9    | <p>This field is used to set the buffer size for channel 9.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 9 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 9 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 9 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 9 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 9 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 9 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 9 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 9 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 9 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 9 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 9 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table>             | 0000 | channel 9 buffer size is 1Dword  | 0001 | channel 9 buffer size is 2Dwords  | 0010 | channel 9 buffer size is 4Dwords  | 0011 | channel 9 buffer size is 8Dwords  | 0100 | channel 9 buffer size is 16Dwords  | 0101 | channel 9 buffer size is 32Dwords  | 0110 | channel 9 buffer size is 64Dwords  | 0111 | channel 9 buffer size is 128Dwords  | 1000 | channel 9 buffer size is 256Dwords  | 1001 | channel 9 buffer size is 512Dwords  | 1010 | channel 9 buffer size is 1024Dwords  | 1111-1011 | Reserved |
| 0000          | channel 9 buffer size is 1Dword  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0001          | channel 9 buffer size is 2Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0010          | channel 9 buffer size is 4Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0011          | channel 9 buffer size is 8Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0100          | channel 9 buffer size is 16Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0101          | channel 9 buffer size is 32Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0110          | channel 9 buffer size is 64Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 0111          | channel 9 buffer size is 128Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1000          | channel 9 buffer size is 256Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1001          | channel 9 buffer size is 512Dwords   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1010          | channel 9 buffer size is 1024Dwords  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| 1111-1011     | Reserved   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |
| CH8           | This field is used to set the buffer size for channel 8.   |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |      |                                     |      |                                     |      |                                      |           |          |

*Table continues on the next page...*

**MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF0 field descriptions (continued)**

| Field     | Description   |
|-----------|---|
|           | All the allowed combinations of bit setting are listed here . |
| 0000      | channel 8 buffer size is 1Dword                               |
| 0001      | channel 8 buffer size is 2Dwords                              |
| 0010      | channel 8 buffer size is 4Dwords                              |
| 0011      | channel 8 buffer size is 8Dwords                              |
| 0100      | channel 8 buffer size is 16Dwords                             |
| 0101      | channel 8 buffer size is 32Dwords                             |
| 0110      | channel 8 buffer size is 64Dwords                             |
| 0111      | channel 8 buffer size is 128Dwords                            |
| 1000      | channel 8 buffer size is 256Dwords                            |
| 1001      | channel 8 buffer size is 512Dwords                            |
| 1010      | channel 8 buffer size is 1024Dwords                           |
| 1111-1011 | Reserved  |

**42.5.38 Rx Fifo Size Configuration Register 1  
(MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF1)**

This register is used to config each Rx fifo size

Address: 220\_8000h base + 20Ch offset = 220\_820Ch

| Bit   | 31  | 30 | 29  | 28 | 27  | 26 | 25  | 24 | 23  | 22 | 21  | 20 | 19  | 18 | 17  | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|----|-----|----|-----|----|-----|----|-----|----|-----|----|-----|----|-----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R     | CH7 |    | CH6 |    | CH5 |    | CH4 |    | CH3 |    | CH2 |    | CH1 |    | CH0 |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| W     | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |   |   |
| Reset | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0   | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |   |   |

**MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF1 field descriptions**

| Field        | Description   |
|--------------|---|
| 31–28<br>CH7 | This field is used to set the buffer size for channel 7.<br>All the allowed combinations of bit setting are listed here . |
| 0000         | channel 7 buffer size is 1Dword   |
| 0001         | channel 7 buffer size is 2Dwords  |
| 0010         | channel 7 buffer size is 4Dwords  |
| 0011         | channel 7 buffer size is 8Dwords  |
| 0100         | channel 7 buffer size is 16Dwords   |
| 0101         | channel 7 buffer size is 32Dwords   |
| 0110         | channel 7 buffer size is 64Dwords   |
| 0111         | channel 7 buffer size is 128Dwords  |
| 1000         | channel 7 buffer size is 256Dwords  |
| 1001         | channel 7 buffer size is 512Dwords  |

*Table continues on the next page...*

**MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF1 field descriptions (continued)**

| Field        | Description   |
|--------------|---|
|              | 1010 channel 7 buffer size is 1024Dwords<br>1111-1011 Reserved  |
| 27–24<br>CH6 | <p>This field is used to set the buffer size for channel 6.</p> <p>All the allowed combinations of bit setting are listed here .</p> <ul style="list-style-type: none"> <li>0000 channel 6 buffer size is 1Dword</li> <li>0001 channel 6 buffer size is 2Dwords</li> <li>0010 channel 6 buffer size is 4Dwords</li> <li>0011 channel 6 buffer size is 8Dwords</li> <li>0100 channel 6 buffer size is 16Dwords</li> <li>0101 channel 6 buffer size is 32Dwords</li> <li>0110 channel 6 buffer size is 64Dwords</li> <li>0111 channel 6 buffer size is 128Dwords</li> <li>1000 channel 6 buffer size is 256Dwords</li> <li>1001 channel 6 buffer size is 512Dwords</li> <li>1010 channel 6 buffer size is 1024Dwords</li> <li>1111-1011 Reserved</li> </ul> |
| 23–20<br>CH5 | <p>This field is used to set the buffer size for channel 5.</p> <p>All the allowed combinations of bit setting are listed here .</p> <ul style="list-style-type: none"> <li>0000 channel 5 buffer size is 1Dword</li> <li>0001 channel 5 buffer size is 2Dwords</li> <li>0010 channel 5 buffer size is 4Dwords</li> <li>0011 channel 5 buffer size is 8Dwords</li> <li>0100 channel 5 buffer size is 16Dwords</li> <li>0101 channel 5 buffer size is 32Dwords</li> <li>0110 channel 5 buffer size is 64Dwords</li> <li>0111 channel 5 buffer size is 128Dwords</li> <li>1000 channel 5 buffer size is 256Dwords</li> <li>1001 channel 5 buffer size is 512Dwords</li> <li>1010 channel 5 buffer size is 1024Dwords</li> <li>1111-1011 Reserved</li> </ul> |
| 19–16<br>CH4 | <p>This field is used to set the buffer size for channel 4.</p> <p>All the allowed combinations of bit setting are listed here .</p> <ul style="list-style-type: none"> <li>0000 channel 4 buffer size is 1Dword</li> <li>0001 channel 4 buffer size is 2Dwords</li> <li>0010 channel 4 buffer size is 4Dwords</li> <li>0011 channel 4 buffer size is 8Dwords</li> <li>0100 channel 4 buffer size is 16Dwords</li> <li>0101 channel 4 buffer size is 32Dwords</li> <li>0110 channel 4 buffer size is 64Dwords</li> <li>0111 channel 4 buffer size is 128Dwords</li> <li>1000 channel 4 buffer size is 256Dwords</li> <li>1001 channel 4 buffer size is 512Dwords</li> <li>1010 channel 4 buffer size is 1024Dwords</li> <li>1111-1011 Reserved</li> </ul> |

Table continues on the next page...

**MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF1 field descriptions (continued)**

| Field        | Description  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
|--------------|--|------|---------------------------------|------|----------------------------------|------|----------------------------------|------|----------------------------------|------|-----------------------------------|------|-----------------------------------|------|-----------------------------------|------|------------------------------------|------|------------------------------------|------|------------------------------------|------|-------------------------------------|-----------|----------|
| 15–12<br>CH3 | <p>This field is used to set the buffer size for channel 3.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 3 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 3 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 3 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 3 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 3 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 3 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 3 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 3 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 3 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 3 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 3 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 3 buffer size is 1Dword | 0001 | channel 3 buffer size is 2Dwords | 0010 | channel 3 buffer size is 4Dwords | 0011 | channel 3 buffer size is 8Dwords | 0100 | channel 3 buffer size is 16Dwords | 0101 | channel 3 buffer size is 32Dwords | 0110 | channel 3 buffer size is 64Dwords | 0111 | channel 3 buffer size is 128Dwords | 1000 | channel 3 buffer size is 256Dwords | 1001 | channel 3 buffer size is 512Dwords | 1010 | channel 3 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000         | channel 3 buffer size is 1Dword  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0001         | channel 3 buffer size is 2Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0010         | channel 3 buffer size is 4Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0011         | channel 3 buffer size is 8Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0100         | channel 3 buffer size is 16Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0101         | channel 3 buffer size is 32Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0110         | channel 3 buffer size is 64Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0111         | channel 3 buffer size is 128Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1000         | channel 3 buffer size is 256Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1001         | channel 3 buffer size is 512Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1010         | channel 3 buffer size is 1024Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1111-1011    | Reserved   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 11–8<br>CH2  | <p>This field is used to set the buffer size for channel 2.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 2 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 2 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 2 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 2 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 2 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 2 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 2 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 2 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 2 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 2 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 2 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 2 buffer size is 1Dword | 0001 | channel 2 buffer size is 2Dwords | 0010 | channel 2 buffer size is 4Dwords | 0011 | channel 2 buffer size is 8Dwords | 0100 | channel 2 buffer size is 16Dwords | 0101 | channel 2 buffer size is 32Dwords | 0110 | channel 2 buffer size is 64Dwords | 0111 | channel 2 buffer size is 128Dwords | 1000 | channel 2 buffer size is 256Dwords | 1001 | channel 2 buffer size is 512Dwords | 1010 | channel 2 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000         | channel 2 buffer size is 1Dword  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0001         | channel 2 buffer size is 2Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0010         | channel 2 buffer size is 4Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0011         | channel 2 buffer size is 8Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0100         | channel 2 buffer size is 16Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0101         | channel 2 buffer size is 32Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0110         | channel 2 buffer size is 64Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0111         | channel 2 buffer size is 128Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1000         | channel 2 buffer size is 256Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1001         | channel 2 buffer size is 512Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1010         | channel 2 buffer size is 1024Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1111-1011    | Reserved   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 7–4<br>CH1   | <p>This field is used to set the buffer size for channel 1.</p> <p>All the allowed combinations of bit setting are listed here .</p> <table> <tbody> <tr><td>0000</td><td>channel 1 buffer size is 1Dword</td></tr> <tr><td>0001</td><td>channel 1 buffer size is 2Dwords</td></tr> <tr><td>0010</td><td>channel 1 buffer size is 4Dwords</td></tr> <tr><td>0011</td><td>channel 1 buffer size is 8Dwords</td></tr> <tr><td>0100</td><td>channel 1 buffer size is 16Dwords</td></tr> <tr><td>0101</td><td>channel 1 buffer size is 32Dwords</td></tr> <tr><td>0110</td><td>channel 1 buffer size is 64Dwords</td></tr> <tr><td>0111</td><td>channel 1 buffer size is 128Dwords</td></tr> <tr><td>1000</td><td>channel 1 buffer size is 256Dwords</td></tr> <tr><td>1001</td><td>channel 1 buffer size is 512Dwords</td></tr> <tr><td>1010</td><td>channel 1 buffer size is 1024Dwords</td></tr> <tr><td>1111-1011</td><td>Reserved</td></tr> </tbody> </table> | 0000 | channel 1 buffer size is 1Dword | 0001 | channel 1 buffer size is 2Dwords | 0010 | channel 1 buffer size is 4Dwords | 0011 | channel 1 buffer size is 8Dwords | 0100 | channel 1 buffer size is 16Dwords | 0101 | channel 1 buffer size is 32Dwords | 0110 | channel 1 buffer size is 64Dwords | 0111 | channel 1 buffer size is 128Dwords | 1000 | channel 1 buffer size is 256Dwords | 1001 | channel 1 buffer size is 512Dwords | 1010 | channel 1 buffer size is 1024Dwords | 1111-1011 | Reserved |
| 0000         | channel 1 buffer size is 1Dword  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0001         | channel 1 buffer size is 2Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0010         | channel 1 buffer size is 4Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0011         | channel 1 buffer size is 8Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0100         | channel 1 buffer size is 16Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0101         | channel 1 buffer size is 32Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0110         | channel 1 buffer size is 64Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 0111         | channel 1 buffer size is 128Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1000         | channel 1 buffer size is 256Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1001         | channel 1 buffer size is 512Dwords   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1010         | channel 1 buffer size is 1024Dwords  |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| 1111-1011    | Reserved   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |
| CH0          | This field is used to set the buffer size for channel 0.   |      |                                 |      |                                  |      |                                  |      |                                  |      |                                   |      |                                   |      |                                   |      |                                    |      |                                    |      |                                    |      |                                     |           |          |

*Table continues on the next page...*

**MIPI\_HSI\_RX\_FIFO\_SIZE\_CONF1 field descriptions (continued)**

| Field     | Description   |
|-----------|---|
|           | All the allowed combinations of bit setting are listed here . |
| 0000      | channel 0 buffer size is 1Dword                               |
| 0001      | channel 0 buffer size is 2Dwords                              |
| 0010      | channel 0 buffer size is 4Dwords                              |
| 0011      | channel 0 buffer size is 8Dwords                              |
| 0100      | channel 0 buffer size is 16Dwords                             |
| 0101      | channel 0 buffer size is 32Dwords                             |
| 0110      | channel 0 buffer size is 64Dwords                             |
| 0111      | channel 0 buffer size is 128Dwords                            |
| 1000      | channel 0 buffer size is 256Dwords                            |
| 1001      | channel 0 buffer size is 512Dwords                            |
| 1010      | channel 0 buffer size is 1024Dwords                           |
| 1111-1011 | Reserved  |

**42.5.39 Tx Fifo Status Register (MIPI\_HSI\_TX\_FIFO\_STAT)**

This register contains full and empty status for each Tx channel fifo

Address: 220\_8000h base + 210h offset = 220\_8210h

| Bit   | 31   | 30 | 29   | 28 | 27   | 26 | 25   | 24 | 23   | 22 | 21   | 20 | 19  | 18 | 17  | 16 |
|-------|------|----|------|----|------|----|------|----|------|----|------|----|-----|----|-----|----|
| R     | CH15 |    | CH14 |    | CH13 |    | CH12 |    | CH11 |    | CH10 |    | CH9 |    | CH8 |    |
| W     |      |    |      |    |      |    |      |    |      |    |      |    |     |    |     |    |
| Reset | 0    | 1  | 0    | 1  | 0    | 1  | 0    | 1  | 0    | 1  | 0    | 1  | 0   | 1  | 0   | 1  |
| Bit   | 15   | 14 | 13   | 12 | 11   | 10 | 9    | 8  | 7    | 6  | 5    | 4  | 3   | 2  | 1   | 0  |
| R     | CH7  |    | CH6  |    | CH5  |    | CH4  |    | CH3  |    | CH2  |    | CH1 |    | CH0 |    |
| W     |      |    |      |    |      |    |      |    |      |    |      |    |     |    |     |    |
| Reset | 0    | 1  | 0    | 1  | 0    | 1  | 0    | 1  | 0    | 1  | 0    | 1  | 0   | 1  | 0   | 1  |

**MIPI\_HSI\_TX\_FIFO\_STAT field descriptions**

| Field         | Description  |
|---------------|--|
| 31–30<br>CH15 | 00 Tx channel 15 fifo not Empty and Full;<br>01 Tx channel 15 fifo Empty;<br>10 Tx channel 15 fifo Full;<br>11 Reserved. |
| 29–28<br>CH14 | 00 Tx channel 14 fifo not Empty and Full;<br>01 Tx channel 14 fifo Empty;<br>10 Tx channel 14 fifo Full;<br>11 Reserved. |

Table continues on the next page...

**MIPI\_HSI\_TX\_FIFO\_STAT field descriptions (continued)**

| Field         | Description  |
|---------------|--|
| 27–26<br>CH13 | 00 Tx channel 13 fifo not Empty and Full;<br>01 Tx channel 13 fifo Empty;<br>10 Tx channel 13 fifo Full;<br>11 Reserved. |
| 25–24<br>CH12 | 00 Tx channel 12 fifo not Empty and Full;<br>01 Tx channel 12 fifo Empty;<br>10 Tx channel 12 fifo Full;<br>11 Reserved. |
| 23–22<br>CH11 | 00 Tx channel 11 fifo not Empty and Full;<br>01 Tx channel 11 fifo Empty;<br>10 Tx channel 11 fifo Full;<br>11 Reserved. |
| 21–20<br>CH10 | 00 Tx channel 10 fifo not Empty and Full;<br>01 Tx channel 10 fifo Empty;<br>10 Tx channel 10 fifo Full;<br>11 Reserved. |
| 19–18<br>CH9  | 00 Tx channel 9 fifo not Empty and Full;<br>01 Tx channel 9 fifo Empty;<br>10 Tx channel 9 fifo Full;<br>11 Reserved.    |
| 17–16<br>CH8  | 00 Tx channel 8 fifo not Empty and Full;<br>01 Tx channel 8 fifo Empty;<br>10 Tx channel 8 fifo Full;<br>11 Reserved.    |
| 15–14<br>CH7  | 00 Tx channel 7 fifo not Empty and Full;<br>01 Tx channel 7 fifo Empty;<br>10 Tx channel 7 fifo Full;<br>11 Reserved.    |
| 13–12<br>CH6  | 00 Tx channel 6 fifo not Empty and Full;<br>01 Tx channel 6 fifo Empty;<br>10 Tx channel 6 fifo Full;<br>11 Reserved.    |
| 11–10<br>CH5  | 00 Tx channel 5 fifo not Empty and Full;<br>01 Tx channel 5 fifo Empty;<br>10 Tx channel 5 fifo Full;<br>11 Reserved.    |
| 9–8<br>CH4    | 00 Tx channel 4 fifo not Empty and Full;<br>01 Tx channel 4 fifo Empty;<br>10 Tx channel 4 fifo Full;<br>11 Reserved.    |
| 7–6<br>CH3    | 00 Tx channel 3 fifo not Empty and Full;<br>01 Tx channel 3 fifo Empty;<br>10 Tx channel 3 fifo Full;<br>11 Reserved.    |

*Table continues on the next page...*

**MIPI\_HSI\_TX\_FIFO\_STAT field descriptions (continued)**

| Field      | Description   |
|------------|---|
| 5–4<br>CH2 | 00 Tx channel 2 fifo not Empty and Full;<br>01 Tx channel 2 fifo Empty;<br>10 Tx channel 2 fifo Full;<br>11 Reserved. |
| 3–2<br>CH1 | 00 Tx channel 1 fifo not Empty and Full;<br>01 Tx channel 1 fifo Empty;<br>10 Tx channel 1 fifo Full;<br>11 Reserved. |
| CH0        | 00 Tx channel 0 fifo not Empty and Full;<br>01 Tx channel 0 fifo Empty;<br>10 Tx channel 0 fifo Full;<br>11 Reserved. |

**42.5.40 Rx Fifo Status Register (MIPI\_HSI\_RX\_FIFO\_STAT)**

This register contains full and empty status for each Rx channel fifo

Address: 220\_8000h base + 214h offset = 220\_8214h

|       |      |      |      |      |      |      |     |     |    |    |    |    |    |    |    |    |
|-------|------|------|------|------|------|------|-----|-----|----|----|----|----|----|----|----|----|
| Bit   | 31   | 30   | 29   | 28   | 27   | 26   | 25  | 24  | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R     | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 |    |    |    |    |    |    |    |    |
| W     |      |      |      |      |      |      |     |     |    |    |    |    |    |    |    |    |
| Reset | 0    | 1    | 0    | 1    | 0    | 1    | 0   | 1   | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  |
| Bit   | 15   | 14   | 13   | 12   | 11   | 10   | 9   | 8   | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| R     | CH7  | CH6  | CH5  | CH4  | CH3  | CH2  | CH1 | CH0 |    |    |    |    |    |    |    |    |
| W     |      |      |      |      |      |      |     |     |    |    |    |    |    |    |    |    |
| Reset | 0    | 1    | 0    | 1    | 0    | 1    | 0   | 1   | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  |

**MIPI\_HSI\_RX\_FIFO\_STAT field descriptions**

| Field         | Description  |
|---------------|--|
| 31–30<br>CH15 | 00 Rx channel 15 fifo not Empty and Full;<br>01 Rx channel 15 fifo Empty;<br>10 Rx channel 15 fifo Full;<br>11 Reserved. |
| 29–28<br>CH14 | 00 Rx channel 14 fifo not Empty and Full;<br>01 Rx channel 14 fifo Empty;<br>10 Rx channel 14 fifo Full;<br>11 Reserved. |

*Table continues on the next page...*

**MIPI\_HSI\_RX\_FIFO\_STAT field descriptions (continued)**

| Field         | Description  |
|---------------|--|
| 27–26<br>CH13 | 00 Rx channel 13 fifo not Empty and Full;<br>01 Rx channel 13 fifo Empty;<br>10 Rx channel 13 fifo Full;<br>11 Reserved. |
| 25–24<br>CH12 | 00 Rx channel 12 fifo not Empty and Full;<br>01 Rx channel 12 fifo Empty;<br>10 Rx channel 12 fifo Full;<br>11 Reserved. |
| 23–22<br>CH11 | 00 Rx channel 11 fifo not Empty and Full;<br>01 Rx channel 11 fifo Empty;<br>10 Rx channel 11 fifo Full;<br>11 Reserved. |
| 21–20<br>CH10 | 00 Rx channel 10 fifo not Empty and Full;<br>01 Rx channel 10 fifo Empty;<br>10 Rx channel 10 fifo Full;<br>11 Reserved. |
| 19–18<br>CH9  | 00 Rx channel 9 fifo not Empty and Full;<br>01 Rx channel 9 fifo Empty;<br>10 Rx channel 9 fifo Full;<br>11 Reserved.    |
| 17–16<br>CH8  | 00 Rx channel 8 fifo not Empty and Full;<br>01 Rx channel 8 fifo Empty;<br>10 Rx channel 8 fifo Full;<br>11 Reserved.    |
| 15–14<br>CH7  | 00 Rx channel 7 fifo not Empty and Full;<br>01 Rx channel 7 fifo Empty;<br>10 Rx channel 7 fifo Full;<br>11 Reserved.    |
| 13–12<br>CH6  | 00 Rx channel 6 fifo not Empty and Full;<br>01 Rx channel 6 fifo Empty;<br>10 Rx channel 6 fifo Full;<br>11 Reserved.    |
| 11–10<br>CH5  | 00 Rx channel 5 fifo not Empty and Full;<br>01 Rx channel 5 fifo Empty;<br>10 Rx channel 5 fifo Full;<br>11 Reserved.    |
| 9–8<br>CH4    | 00 Rx channel 4 fifo not Empty and Full;<br>01 Rx channel 4 fifo Empty;<br>10 Rx channel 4 fifo Full;<br>11 Reserved.    |
| 7–6<br>CH3    | 00 Rx channel 3 fifo not Empty and Full;<br>01 Rx channel 3 fifo Empty;<br>10 Rx channel 3 fifo Full;<br>11 Reserved.    |

*Table continues on the next page...*

**MIPI\_HSI\_RX\_FIFO\_STAT field descriptions (continued)**

| Field      | Description   |
|------------|---|
| 5–4<br>CH2 | 00 Rx channel 2 fifo not Empty and Full;<br>01 Rx channel 2 fifo Empty;<br>10 Rx channel 2 fifo Full;<br>11 Reserved. |
| 3–2<br>CH1 | 00 Rx channel 1 fifo not Empty and Full;<br>01 Rx channel 1 fifo Empty;<br>10 Rx channel 1 fifo Full;<br>11 Reserved. |
| CH0        | 00 Rx channel 0 fifo not Empty and Full;<br>01 Rx channel 0 fifo Empty;<br>10 Rx channel 0 fifo Full;<br>11 Reserved. |

### 42.5.41 Ahb Master Config Register (MIPI\_HSI\_AHB\_MASTER\_CONF)

This register used to config hsi internal ahb master

Address: 220\_8000h base + 228h offset = 220\_8228h

|        |          |    |    |    |    |               |    |    |          |    |                     |    |    |    |    |    |
|--------|----------|----|----|----|----|---------------|----|----|----------|----|---------------------|----|----|----|----|----|
| Bit    | 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 | 23       | 22 | 21                  | 20 | 19 | 18 | 17 | 16 |
| R<br>W | Reserved |    |    |    |    |               |    |    |          |    |                     |    |    |    |    |    |
| Reset  | 0        | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0        | 0  | 0                   | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  | 7        | 6  | 5                   | 4  | 3  | 2  | 1  | 0  |
| R<br>W | Reserved |    |    |    |    | DP_HOLD_CYCLE |    |    | DMA_MODE |    | DMA_INSERT_IDLE_NUM |    |    |    |    |    |
| Reset  | 0        | 0  | 0  | 0  | 0  | 0             | 0  | 1  | 1        | 0  | 0                   | 0  | 0  | 0  | 0  |    |

**MIPI\_HSI\_AHB\_MASTER\_CONF field descriptions**

| Field                | Description   |
|----------------------|---|
| 31–10<br>Reserved    | This field is reserved.<br>Reserved, always set to zero.  |
| 9–6<br>DP_HOLD_CYCLE | These bits used to set the number of cycles for DP access fifo.   |
| 5–4<br>DMA_MODE      | 00 Once AHB master get hgrant from bus, it will set htrans "IDLE" for serval ahb cycles.In the serval cycles, once it found dataport is accessing fifo, it will release bus.<br>01 Once AHB master get hgrant from bus, it will set htrans "IDLE" for serval ahb cycles.After the serval cycles, once it found dataport is accessing fifo, it will keep on sending "IDLE" out untill dataport finish accessing fifo.<br>1x Once AHB master get hgrant from bus, dataport can not access fifo untill a dma operation done. |

Table continues on the next page...

**MIPI\_HSI\_AHB\_MASTER\_CONF field descriptions (continued)**

| Field               | Description  |
|---------------------|--|
| DMA_INSERT_IDLE_NUM | These bits used to set the number of "IDLE" cycles when DMA_MODE == 2'b0x. |

**42.5.42 TX Break Length Register (MIPI\_HSI\_TX\_BREAK\_LEN)**

This register used to set tx break length

Address: 220\_8000h base + 22Ch offset = 220\_822Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| W   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

Reset 0 1 0 0 1 0 1

**MIPI\_HSI\_TX\_BREAK\_LEN field descriptions**

| Field            | Description   |
|------------------|---|
| 31–6<br>Reserved | This field is reserved.<br>Reserved, always set to zero.                  |
| COUNT            | The tx break length count.<br><br>6'h00 64<br><br>6'h01 1<br><br>6'h3f 63 |

