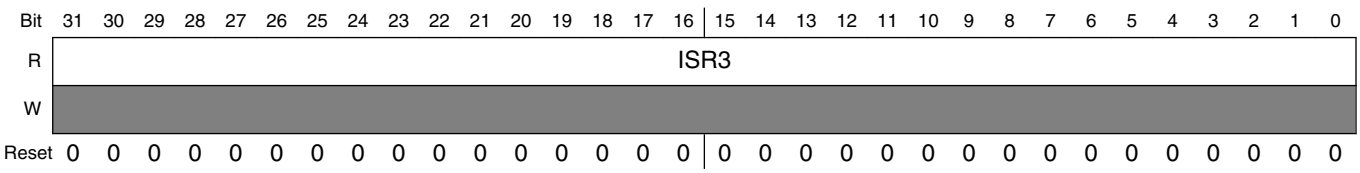
## 27.8.9 IRQ status resister 3 (GPC_ISR3)

ISR3 Register - status of irq [127:96].

Address: 20D_C000h base + 20h offset = 20D_C020h



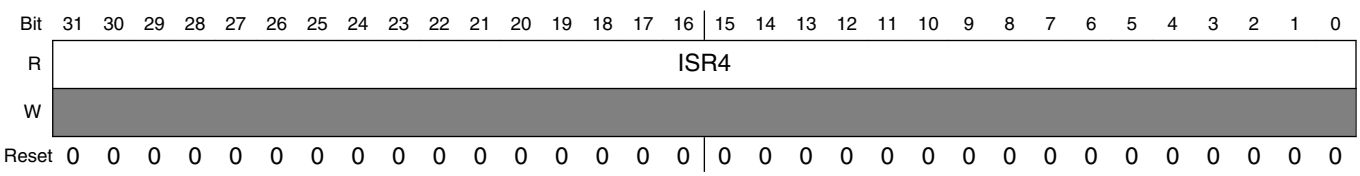

**GPC_ISR3 field descriptions**

| Field | Description |
|---|---|
| ISR3 | IRQ[127:96] status, read only |

## 27.8.10 IRQ status resister 4 (GPC_ISR4)

ISR4 Register - status of irq [159:128].

Address: 20D_C000h base + 24h offset = 20D_C024h




**GPC_ISR4 field descriptions**

| Field | Description |
|---|---|
| ISR4 | IRQ[159:128] status, read only |

# 27.9 PGC Memory Map/Register Definition

The PGC registers can be accessed only in supervisor mode.

Attempts to access registers when not in supervisor mode or attempts to access an unimplemented address location might trigger a bus transfer error. (The hardware asserts the signal ips_xfr_err if the PGC has been integrated with resp_sel tied low.) In this case, software should take appropriate action (such as ignore the error, log the error, or initiate a soft reset).

All PGC registers are byte-accessible.

**NOTE**

The base address of each PGC module instantiation is specified in the GPC module. Absolute address values will be calculated by [GPC base address] + [PGC CPU/GPU/DISPLAY Offset].

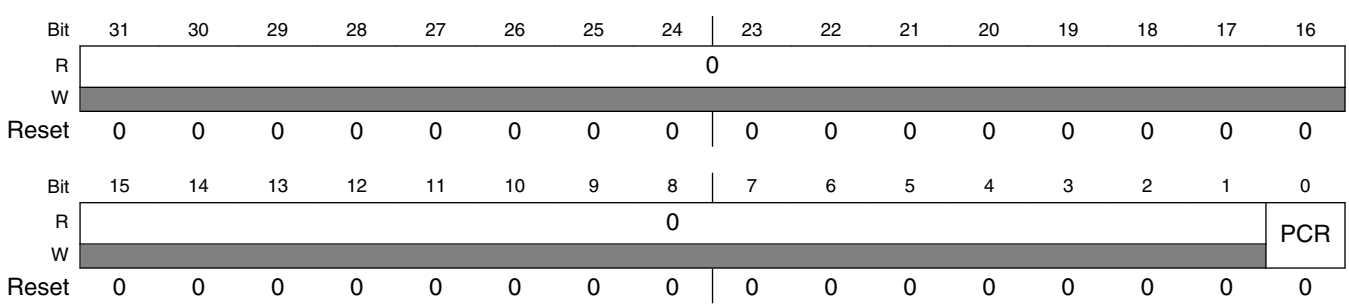
**PGC memory map**

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|---|---|---|---|---|---|
| 20D_C260 | PGC Control Register (PGC_GPU_CTRL) | 32 | R/W | 0000_0000h | 27.9.1/1386 |
| 20D_C264 | Power Up Sequence Control Register (PGC_GPU_PUPSCR) | 32 | R/W | 0000_0F01h | 27.9.2/1387 |
| 20D_C268 | Pull Down Sequence Control Register (PGC_GPU_PDNSCR) | 32 | R/W | 0000_0101h | 27.9.3/1388 |
| 20D_C26C | Power Gating Controller Status Register (PGC_GPU_SR) | 32 | R/W | 0000_0000h | 27.9.4/1388 |
| 20D_C2A0 | PGC Control Register (PGC_CPU_CTRL) | 32 | R/W | 0000_0000h | 27.9.5/1389 |
| 20D_C2A4 | Power Up Sequence Control Register (PGC_CPU_PUPSCR) | 32 | R/W | 0000_0F01h | 27.9.6/1390 |
| 20D_C2A8 | Pull Down Sequence Control Register (PGC_CPU_PDNSCR) | 32 | R/W | 0000_0101h | 27.9.7/1390 |
| 20D_C2AC | Power Gating Controller Status Register (PGC_CPU_SR) | 32 | R/W | 0000_0000h | 27.9.8/1391 |

## 27.9.1 PGC Control Register (PGC_GPU_CTRL)

The PGCR enables the response to a power-down request.

Address: 20D_C000h base + 260h offset = 20D_C260h



**PGC_GPU_CTRL field descriptions**

| Field | Description |
|---|---|
| 31–1<br>Reserved | This read-only field is reserved and always has the value 0. |
| 0<br>PCR | Power Control<br>**NOTE:** PCR must not change from power-down request (pdn_req) assertion until the target subsystem is completely powered up.<br>0 Do not switch off power even if pdn_req is asserted.<br>1 Switch off power when pdn_req is asserted. |

## 27.9.2 Power Up Sequence Control Register (PGC_GPU_PUPSCR)

The PUPSCR contains the power-up timing parameters.

Address: 20D_C000h base + 264h offset = 20D_C264h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | | | | | | | | | | | | | | | | SW2ISO | | | | | | | | 0 | | SW | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

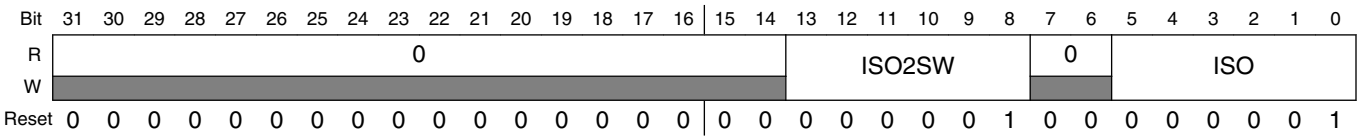
**PGC_GPU_PUPSCR field descriptions**

| Field | Description |
|---|---|
| 31–14<br>Reserved | This read-only field is reserved and always has the value 0. |
| 13–8<br>SW2ISO | After asserting power toggle on/off signal (switch_b), the PGC waits a number of IPG clocks equal to the value of SW2ISO before negating isolation.<br>**NOTE:** SW2ISO must not be programmed to zero. |
| 7–6<br>Reserved | This read-only field is reserved and always has the value 0. |
| SW | After a power-up request (pup_req assertion), the PGC waits a number of IPG clocks equal to the value of SW before asserting power toggle on/off signal (switch_b).<br>**NOTE:** SW must not be programmed to zero.<br>**NOTE:** The PGC clock is generated from the IPG_CLK_ROOT. for frequency configuration of the IPG_CLK_ROOT. See Clock Controller Module (CCM). |

## 27.9.3 Pull Down Sequence Control Register (PGC_GPU_PDNSCR)

The PDNSCR contains the power-down timing parameters.

Address: 20D_C000h base + 268h offset = 20D_C268h



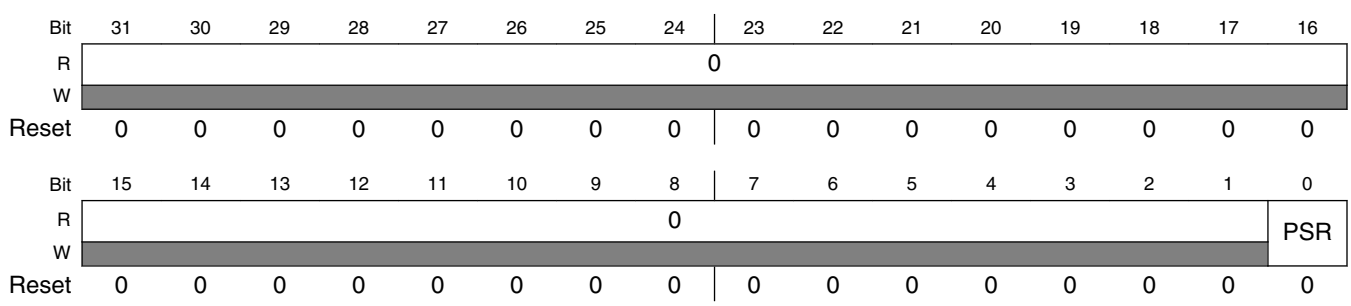

**PGC_GPU_PDNSCR field descriptions**

| Field | Description |
|---|---|
| 31–14<br>Reserved | This read-only field is reserved and always has the value 0. |
| 13–8<br>ISO2SW | After asserting isolation, the PGC waits a number of IPG clocks equal to the value of ISO2SW before negating power toggle on/off signal (switch_b).<br><br>**NOTE:** ISO2SW must not be programmed to zero. |
| 7–6<br>Reserved | This read-only field is reserved and always has the value 0. |
| ISO | After a power-down request (pdn_req assertion), the PGC waits a number of IPG clocks equal to the value of ISO before asserting isolation.<br><br>**NOTE:** ISO must not be programmed to zero. |

## 27.9.4 Power Gating Controller Status Register (PGC_GPU_SR)

The PDNSCR contains the power-down timing parameters.

Address: 20D_C000h base + 26Ch offset = 20D_C26Ch



**PGC_GPU_SR field descriptions**

| Field | Description |
|---|---|
| 31–1<br>Reserved | This read-only field is reserved and always has the value 0. |
| 0<br>PSR | Power status. When in functional (or software-controlled debug) mode, PGC hardware sets PSR as soon as any of the power control output changes its state to one. Write one to clear this bit. Software should clear this bit after power up; otherwise, PSR continues to reflect the power status of the initial power down.<br>0 The target subsystem was not powered down for the previous power-down request.<br>1 The target subsystem was powered down for the previous power-down request. |

## 27.9.5 PGC Control Register (PGC_CPU_CTRL)

The PGCR enables the response to a power-down request.

Address: 20D_C000h base + 2A0h offset = 20D_C2A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | | | | | | | | | | | | | | | PCR |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PGC_CPU_CTRL field descriptions**

| Field | Description |
|---|---|
| 31–1<br>Reserved | This read-only field is reserved and always has the value 0. |
| 0<br>PCR | Power Control<br>**NOTE:** PCR must not change from power-down request (pdn_req) assertion until the target subsystem is completely powered up.<br>0 Do not switch off power even if pdn_req is asserted.<br>1 Switch off power when pdn_req is asserted. |

## 27.9.6 Power Up Sequence Control Register (PGC_CPU_PUPSCR)

The PUPSCR contains the power-up timing parameters.

Address: 20D_C000h base + 2A4h offset = 20D_C2A4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | | | | | | | | | | | | | | | | | | SW2ISO | | | | | | 0 | | SW | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**PGC_CPU_PUPSCR field descriptions**

| Field | Description |
|---|---|
| 31–14<br>Reserved | This read-only field is reserved and always has the value 0. |
| 13–8<br>SW2ISO | After asserting , the PGC waits a number of 32k clocks equal to the value of SW2ISO before negating isolation.<br>**NOTE:** SW2ISO must not be programmed to zero. The SW2ISO value should be chosen such that the delay before negating isolation is greater than the LDO ramp-up time. |
| 7–6<br>Reserved | This read-only field is reserved and always has the value 0. |
| SW | After a power-up request (pup_req assertion), the PGC waits a number of 32k clocks equal to the value of SW before asserting .<br>**NOTE:** SW must not be programmed to zero. |

## 27.9.7 Pull Down Sequence Control Register (PGC_CPU_PDNSCR)

The PDNSCR contains the power-down timing parameters.

Address: 20D_C000h base + 2A8h offset = 20D_C2A8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | | | | | | | | | | | | | | | | | | ISO2SW | | | | | | 0 | | ISO | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |