

65.6 USB Core Memory Map/Register Definition

USBC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
218_4000	Identification register (USBC_UOG_ID)	32	R	E401_FA05h	65.6.1/5444
218_4004	Hardware General (USBC_UOG_HWGENERAL)	32	R	0000_0015h	65.6.2/5445
218_4008	Host Hardware Parameters (USBC_UOG_HWHOST)	32	R	1002_0001h	65.6.3/5446
218_400C	Device Hardware Parameters (USBC_UOG_HWDEVICE)	32	R	0000_0011h	65.6.4/5447
218_4010	TX Buffer Hardware Parameters (USBC_UOG_HWTXBUF)	32	R	8008_0B08h	65.6.5/5448
218_4014	RX Buffer Hardware Parameters (USBC_UOG_HWRXBUF)	32	R	0000_0808h	65.6.6/5448
218_4080	General Purpose Timer #0 Load (USBC_UOG_GPTIMER0LD)	32	R/W	0000_0000h	65.6.7/5449
218_4084	General Purpose Timer #0 Controller (USBC_UOG_GPTIMER0CTRL)	32	R/W	0000_0000h	65.6.8/5449
218_4088	General Purpose Timer #1 Load (USBC_UOG_GPTIMER1LD)	32	R/W	0000_0000h	65.6.9/5451
218_408C	General Purpose Timer #1 Controller (USBC_UOG_GPTIMER1CTRL)	32	R/W	0000_0000h	65.6.10/5451
218_4090	System Bus Config (USBC_UOG_SBUSCFG)	32	R/W	0000_0002h	65.6.11/5452
218_4100	Capability Registers Length (USBC_UOG_CAPLENGTH)	8	R	40h	65.6.12/5453
218_4102	Host Controller Interface Version (USBC_UOG_HCIVERSION)	16	R	0100h	65.6.13/5454
218_4104	Host Controller Structural Parameters (USBC_UOG_HCSPARAMS)	32	R	0001_0011h	65.6.14/5454
218_4108	Host Controller Capability Parameters (USBC_UOG_HCCPARAMS)	32	R	0000_0006h	65.6.15/5456
218_4120	Device Controller Interface Version (USBC_UOG_DCIVERSION)	16	R	0001h	65.6.16/5458
218_4124	Device Controller Capability Parameters (USBC_UOG_DCCPARAMS)	32	R	0000_0188h	65.6.17/5459
218_4140	USB Command Register (USBC_UOG_USBCMD)	32	R/W	0008_0000h	65.6.18/5460
218_4144	USB Status Register (USBC_UOG_USBSTS)	32	R/W	0000_0000h	65.6.19/5464
218_4148	Interrupt Enable Register (USBC_UOG_USBINTR)	32	R/W	0000_0000h	65.6.20/5468
218_414C	USB Frame Index (USBC_UOG_FRINDEX)	32	R/W	0000_0000h	65.6.21/5470
218_4154	Frame List Base Address (USBC_UOG_PERIODICLISTBASE)	32	R/W	0000_0000h	65.6.22/5471

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USBC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
218_4154	Device Address (USBC_UOG_DEVICEADDR)	32	R/W	0000_0000h	65.6.23/ 5471
218_4158	Next Asynch. Address (USBC_UOG_ASYNCLISTADDR)	32	R/W	0000_0000h	65.6.24/ 5472
218_4158	Endpoint List Address (USBC_UOG_ENDPTLISTADDR)	32	R/W	0000_0000h	65.6.25/ 5473
218_4160	Programmable Burst Size (USBC_UOG_BURSTSIZE)	32	R/W	0000_0000h	65.6.26/ 5474
218_4164	TX FIFO Fill Tuning (USBC_UOG_TXFILLTUNING)	32	R/W	0000_0808h	65.6.27/ 5474
218_4178	Endpoint NAK (USBC_UOG_ENDPTNAK)	32	R/W	0000_0000h	65.6.28/ 5476
218_417C	Endpoint NAK Enable (USBC_UOG_ENDPTNAKEN)	32	R/W	0000_0000h	65.6.29/ 5476
218_4180	Configure Flag Register (USBC_UOG_CONFIGFLAG)	32	R/W	0000_0001h	65.6.30/ 5477
218_4184	Port Status & Control (USBC_UOG_PORTSC1)	32	R/W	1000_0000h	65.6.31/ 5478
218_41A4	On-The-Go Status & control (USBC_UOG_OTGSC)	32	R/W	0000_0120h	65.6.32/ 5484
218_41A8	USB Device Mode (USBC_UOG_USBMODE)	32	R/W	0000_0000h	65.6.33/ 5488
218_41AC	Endpoint Setup Status (USBC_UOG_ENDPTSETUPSTAT)	32	R/W	0000_0000h	65.6.34/ 5490
218_41B0	Endpoint Prime (USBC_UOG_ENDPTPRIME)	32	R/W	0000_0000h	65.6.35/ 5490
218_41B4	Endpoint Flush (USBC_UOG_ENDPTFLUSH)	32	R/W	0000_0000h	65.6.36/ 5491
218_41B8	Endpoint Status (USBC_UOG_ENDPTSTAT)	32	R	0000_0000h	65.6.37/ 5492
218_41BC	Endpoint Complete (USBC_UOG_ENDPTCOMPLETE)	32	R/W	0000_0000h	65.6.38/ 5493
218_41C0	Endpoint Control0 (USBC_UOG_ENDPTCTRL0)	32	R/W	0080_0080h	65.6.39/ 5494
218_41C4	Endpoint Control 1 (USBC_UOG_ENDPTCTRL1)	32	R/W	0000_0000h	65.6.40/ 5495
218_41C8	Endpoint Control 2 (USBC_UOG_ENDPTCTRL2)	32	R/W	0000_0000h	65.6.41/ 5498
218_41CC	Endpoint Control 3 (USBC_UOG_ENDPTCTRL3)	32	R/W	0000_0000h	65.6.42/ 5501
218_41D0	Endpoint Control 4 (USBC_UOG_ENDPTCTRL4)	32	R/W	0000_0000h	65.6.43/ 5503
218_41D4	Endpoint Control 5 (USBC_UOG_ENDPTCTRL5)	32	R/W	0000_0000h	65.6.44/ 5506

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USBC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
218_41D8	Endpoint Control 6 (USBC_UOG_ENDPTCTRL6)	32	R/W	0000_0000h	65.6.45/5509
218_41DC	Endpoint Control 7 (USBC_UOG_ENDPTCTRL7)	32	R/W	0000_0000h	65.6.46/5511
218_4200	Identification register (USBC_UH1_ID)	32	R	E401_FA05h	65.6.1/5444
218_4204	Hardware General (USBC_UH1_HWGENERAL)	32	R	0000_0015h	65.6.2/5445
218_4208	Host Hardware Parameters (USBC_UH1_HWHOST)	32	R	1002_0001h	65.6.3/5446
218_4210	TX Buffer Hardware Parameters (USBC_UH1_HWTXBUF)	32	R	8008_0B08h	65.6.5/5448
218_4214	RX Buffer Hardware Parameters (USBC_UH1_HWRXBUF)	32	R	0000_0808h	65.6.6/5448
218_4280	General Purpose Timer #0 Load (USBC_UH1_GPTIMER0LD)	32	R/W	0000_0000h	65.6.7/5449
218_4284	General Purpose Timer #0 Controller (USBC_UH1_GPTIMER0CTRL)	32	R/W	0000_0000h	65.6.8/5449
218_4288	General Purpose Timer #1 Load (USBC_UH1_GPTIMER1LD)	32	R/W	0000_0000h	65.6.9/5451
218_428C	General Purpose Timer #1 Controller (USBC_UH1_GPTIMER1CTRL)	32	R/W	0000_0000h	65.6.10/5451
218_4290	System Bus Config (USBC_UH1_SBUSCFG)	32	R/W	0000_0002h	65.6.11/5452
218_4300	Capability Registers Length (USBC_UH1_CAPLENGTH)	8	R	40h	65.6.12/5453
218_4302	Host Controller Interface Version (USBC_UH1_HCIVERSION)	16	R	0100h	65.6.13/5454
218_4304	Host Controller Structural Parameters (USBC_UH1_HCSPARAMS)	32	R	0001_0011h	65.6.14/5454
218_4308	Host Controller Capability Parameters (USBC_UH1_HCCPARAMS)	32	R	0000_0006h	65.6.15/5456
218_4340	USB Command Register (USBC_UH1_USBCMD)	32	R/W	0008_0000h	65.6.18/5460
218_4344	USB Status Register (USBC_UH1_USBSTS)	32	R/W	0000_0000h	65.6.19/5464
218_4348	Interrupt Enable Register (USBC_UH1_USBINTR)	32	R/W	0000_0000h	65.6.20/5468
218_434C	USB Frame Index (USBC_UH1_FRINDEX)	32	R/W	0000_0000h	65.6.21/5470
218_4354	Frame List Base Address (USBC_UH1_PERIODICLISTBASE)	32	R/W	0000_0000h	65.6.22/5471
218_4358	Next Asynch. Address (USBC_UH1_ASYNCLISTADDR)	32	R/W	0000_0000h	65.6.24/5472
218_4360	Programmable Burst Size (USBC_UH1_BURSTSIZE)	32	R/W	0000_0000h	65.6.26/5474
218_4364	TX FIFO Fill Tuning (USBC_UH1_TXFILLTUNING)	32	R/W	0000_0808h	65.6.27/5474

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USBC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
218_4380	Configure Flag Register (USBC_UH1_CONFIGFLAG)	32	R/W	0000_0001h	65.6.30/5477
218_4384	Port Status & Control (USBC_UH1_PORTSC1)	32	R/W	1000_0000h	65.6.31/5478
218_43A8	USB Device Mode (USBC_UH1_USBMODE)	32	R/W	0000_0000h	65.6.33/5488
218_4400	Identification register (USBC_UH2_ID)	32	R	E401_FA05h	65.6.1/5444
218_4404	Hardware General (USBC_UH2_HWGENERAL)	32	R	0000_0015h	65.6.2/5445
218_4408	Host Hardware Parameters (USBC_UH2_HWHOST)	32	R	1002_0001h	65.6.3/5446
218_4410	TX Buffer Hardware Parameters (USBC_UH2_HWTXBUF)	32	R	8008_0B08h	65.6.5/5448
218_4414	RX Buffer Hardware Parameters (USBC_UH2_HWRXBUF)	32	R	0000_0808h	65.6.6/5448
218_4480	General Purpose Timer #0 Load (USBC_UH2_GPTIMER0LD)	32	R/W	0000_0000h	65.6.7/5449
218_4484	General Purpose Timer #0 Controller (USBC_UH2_GPTIMER0CTRL)	32	R/W	0000_0000h	65.6.8/5449
218_4488	General Purpose Timer #1 Load (USBC_UH2_GPTIMER1LD)	32	R/W	0000_0000h	65.6.9/5451
218_448C	General Purpose Timer #1 Controller (USBC_UH2_GPTIMER1CTRL)	32	R/W	0000_0000h	65.6.10/5451
218_4490	System Bus Config (USBC_UH2_SBUSCFG)	32	R/W	0000_0002h	65.6.11/5452
218_4500	Capability Registers Length (USBC_UH2_CAPLENGTH)	8	R	40h	65.6.12/5453
218_4502	Host Controller Interface Version (USBC_UH2_HCIVERSION)	16	R	0100h	65.6.13/5454
218_4504	Host Controller Structural Parameters (USBC_UH2_HCSPARAMS)	32	R	0001_0011h	65.6.14/5454
218_4508	Host Controller Capability Parameters (USBC_UH2_HCCPARAMS)	32	R	0000_0006h	65.6.15/5456
218_4540	USB Command Register (USBC_UH2_USBCMD)	32	R/W	0008_0000h	65.6.18/5460
218_4544	USB Status Register (USBC_UH2_USBSTS)	32	R/W	0000_0000h	65.6.19/5464
218_4548	Interrupt Enable Register (USBC_UH2_USBINTR)	32	R/W	0000_0000h	65.6.20/5468
218_454C	USB Frame Index (USBC_UH2_FRINDEX)	32	R/W	0000_0000h	65.6.21/5470
218_4554	Frame List Base Address (USBC_UH2_PERIODICLISTBASE)	32	R/W	0000_0000h	65.6.22/5471
218_4558	Next Asynch. Address (USBC_UH2_ASYNCLISTADDR)	32	R/W	0000_0000h	65.6.24/5472
218_4560	Programmable Burst Size (USBC_UH2_BURSTSIZE)	32	R/W	0000_0000h	65.6.26/5474

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USBC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
218_4564	TX FIFO Fill Tuning (USBC_UH2_TXFILLTUNING)	32	R/W	0000_0808h	65.6.27/ 5474
218_4580	Configure Flag Register (USBC_UH2_CONFIGFLAG)	32	R/W	0000_0001h	65.6.30/ 5477
218_4584	Port Status & Control (USBC_UH2_PORTSC1)	32	R/W	1000_0000h	65.6.31/ 5478
218_45A8	USB Device Mode (USBC_UH2_USBMODE)	32	R/W	0000_0000h	65.6.33/ 5488
218_4600	Identification register (USBC_UH3_ID)	32	R	E401_FA05h	65.6.1/5444
218_4604	Hardware General (USBC_UH3_HWGENERAL)	32	R	0000_0015h	65.6.2/5445
218_4608	Host Hardware Parameters (USBC_UH3_HWHOST)	32	R	1002_0001h	65.6.3/5446
218_4610	TX Buffer Hardware Parameters (USBC_UH3_HWTXBUF)	32	R	8008_0B08h	65.6.5/5448
218_4614	RX Buffer Hardware Parameters (USBC_UH3_HWRXBUF)	32	R	0000_0808h	65.6.6/5448
218_4680	General Purpose Timer #0 Load (USBC_UH3_GPTIMER0LD)	32	R/W	0000_0000h	65.6.7/5449
218_4684	General Purpose Timer #0 Controller (USBC_UH3_GPTIMER0CTRL)	32	R/W	0000_0000h	65.6.8/5449
218_4688	General Purpose Timer #1 Load (USBC_UH3_GPTIMER1LD)	32	R/W	0000_0000h	65.6.9/5451
218_468C	General Purpose Timer #1 Controller (USBC_UH3_GPTIMER1CTRL)	32	R/W	0000_0000h	65.6.10/ 5451
218_4690	System Bus Config (USBC_UH3_SBUSCFG)	32	R/W	0000_0002h	65.6.11/ 5452
218_4700	Capability Registers Length (USBC_UH3_CAPLENGTH)	8	R	40h	65.6.12/ 5453
218_4702	Host Controller Interface Version (USBC_UH3_HCIVERSION)	16	R	0100h	65.6.13/ 5454
218_4704	Host Controller Structural Parameters (USBC_UH3_HCSPARAMS)	32	R	0001_0011h	65.6.14/ 5454
218_4708	Host Controller Capability Parameters (USBC_UH3_HCCPARAMS)	32	R	0000_0006h	65.6.15/ 5456
218_4740	USB Command Register (USBC_UH3_USBCMD)	32	R/W	0008_0000h	65.6.18/ 5460
218_4744	USB Status Register (USBC_UH3_USBSTS)	32	R/W	0000_0000h	65.6.19/ 5464
218_4748	Interrupt Enable Register (USBC_UH3_USBINTR)	32	R/W	0000_0000h	65.6.20/ 5468
218_474C	USB Frame Index (USBC_UH3_FRINDEX)	32	R/W	0000_0000h	65.6.21/ 5470
218_4754	Frame List Base Address (USBC_UH3_PERIODICLISTBASE)	32	R/W	0000_0000h	65.6.22/ 5471
218_4758	Next Asynch. Address (USBC_UH3_ASYNCLISTADDR)	32	R/W	0000_0000h	65.6.24/ 5472

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USBC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
218_4760	Programmable Burst Size (USBC_UH3_BURSTSIZE)	32	R/W	0000_0000h	65.6.26/ 5474
218_4764	TX FIFO Fill Tuning (USBC_UH3_TXFILLTUNING)	32	R/W	0000_0808h	65.6.27/ 5474
218_4780	Configure Flag Register (USBC_UH3_CONFIGFLAG)	32	R/W	0000_0001h	65.6.30/ 5477
218_4784	Port Status & Control (USBC_UH3_PORTSC1)	32	R/W	1000_0000h	65.6.31/ 5478
218_47A8	USB Device Mode (USBC_UH3_USBMODE)	32	R/W	0000_0000h	65.6.33/ 5488

65.6.1 Identification register (USBC_n_ID)

The ID register identifies the USB 2.0 High-Speed core and its revision.

Address: 218_4000h base + 0h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved								REVISION							
W																
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved				NID				Reserved		ID					
W																
Reset	1	1	1	1	1	0	1	0	0	0	0	0	0	1	0	1

USBC_n_ID field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23–16 REVISION	Revision number of the controller core.
15–14 -	This field is reserved. Reserved
13–8 NID	Complement version of ID
7–6 -	This field is reserved. Reserved
ID	Configuration number.

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USBC_n_ID field descriptions (continued)

Field	Description
	This number is set to 0x05 and indicates that the peripheral is USB 2.0 High-Speed core.

65.6.2 Hardware General (USBC_n_HWGENERAL)

General hardware parameters as defined in System Level Issues and Core Configuration.

NOTE

The reset value could vary from instance to instance. Please see the detail in bit field description and ignore reset value in summary table in this case!

Address: 218_4000h base + 4h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved					SM		PHYM			PHYW		Reserved			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1

USBC_n_HWGENERAL field descriptions

Field	Description
31–11 -	This field is reserved. Reserved
10–9 SM	Serial interface mode capability SM bit reset value is '00b' 00 No Serial Engine, always use parallel signalling. 01 Serial Engine present, always use serial signalling for FS/LS. 10 Software programmable - Reset to use parallel signalling for FS/LS 11 Software programmable - Reset to use serial signalling for FS/LS
8–6 PHYM	Transciever type PHYM bit reset value: '0000b' for OTG controller core, '0100b' for Host-only controller core. 000 UTMI/UTMI+ 001 ULPI DDR 010 ULPI 011 Serial Only 100 Software programmable - reset to UTMI/UTMI+ 101 Software programmable - reset to ULPI DDR

Table continues on the next page...

USBC_n_HWGENERAL field descriptions (continued)

Field	Description
	110 Software programmable - reset to ULPI 111 Software programmable - reset to Serial 1000 IC-USB 1001 Software programmable - reset to IC-USB 1010 HSIC 1011 Software programmable - reset to HSIC
5–4 PHYW	Data width of the transciever connected to the controller core. PHYW bit reset value is '01b'. 00 8 bit wide data bus Software non-programmable 01 16 bit wide data bus Software non-programmable 10 Reset to 8 bit wide data bus Software programmable 11 Reset to 16 bit wide data bus Software programmable
-	This field is reserved. Reserved

65.6.3 Host Hardware Parameters (USBC_n_HWHOST)

Address: 218_4000h base + 8h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	Reserved																
W																	
Reset	0	0	0	1	0	0	0	0		0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	Reserved												NPORT	HC			
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	1	0

USBC_n_HWHOST field descriptions

Field	Description
31–4 -	This field is reserved. Reserved
3–1 NPORT	The Nmber of downstream ports supported by the host controller is (NPORT+1). NOTE: When these bits value is '000', it indicates a single-port host controller.

Table continues on the next page...

USBC_n_HWHOST field descriptions (continued)

Field	Description
0 HC	Host Capable. Indicating whether host operation mode is supported or not. 1 Supported 0 Not supported

65.6.4 Device Hardware Parameters (USBC_n_HWDEVICE)**NOTE**

This register is only available in OTG core.

Address: 218_4000h base + Ch offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

USBC_n_HWDEVICE field descriptions

Field	Description
31–6 -	This field is reserved. Reserved
5–1 DEVEP	Device Endpoint Number
0 DC	Device Capable. Indicating whether device operation mode is supported or not. 1 Supported 0 Not supported

65.6.5 TX Buffer Hardware Parameters (USBC_n_HWTXBUF)

Address: 218_4000h base + 10h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved										TXCHANADD				Reserved										TXBURST							
W																																
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1	0	0	0

USBC_n_HWTXBUF field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23–16 TXCHANADD	TX FIFO Buffer size is: $(2^{TXCHANADD}) * 4$ Bytes. These bits are set to '08h', so buffer size is 256*4 Bytes. For the OTG controller operating in device mode, this is the FIFO buffer size per endpoint. As the OTG controller has 8 TX endpoint, there are 8 of these buffers. For the OTG controller operating in host mode, or for Host-only controller, the entire buffer memory is used as a single TX buffer. Therefore, there is only 1 of this buffer
15–8 -	This field is reserved. Reserved
TXBURST	Default burst size for memory to TX buffer transfer. This is reset value of TXPBURST bits in USB core register USB_n_BURSTSIZE. Please see Programmable Burst Size (USBC_n_BURSTSIZE) .

65.6.6 RX Buffer Hardware Parameters (USBC_n_HWRXBUF)

Address: 218_4000h base + 14h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved										RXADD				RXBURST																	
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	

USBC_n_HWRXBUF field descriptions

Field	Description
31–16 -	This field is reserved. Reserved
15–8 RXADD	Buffer total size for all receive endpoints is (2^{RXADD}) . RX Buffer size is: $(2^{RXADD}) * 4$ Bytes. These bits are set to '08h', so buffer size is 256*4 Bytes.

Table continues on the next page...

USBC_n_HWRXBUF field descriptions (continued)

Field	Description
	There is a single Receive FIFO buffer in the USB controller. The buffer is shared for all endpoints for the OTG controller in device mode.
RXBURST	Default burst size for memory to RX buffer transfer. This is reset value of RXPBURST bits in USB core register USB_n_BURSTSIZEx. Please see Programmable Burst Size (USBC_n_BURSTSIZEx) .

65.6.7 General Purpose Timer #0 Load (USBC_n_GPTIMER0LD)

This register controls load value of the count timer in register n_GPTIMER0CTRL.
Please see [General Purpose Timer #0 Controller \(USBC_n_GPTIMER0CTRL\)](#).

Address: 218_4000h base + 80h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																																	
W																																	

Reset 0

USBC_n_GPTIMER0LD field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
GPTLD	General Purpose Timer Load Value These bit fields are loaded to GPTCNT bits when GPTRST bit is set '1b'. This value represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. NOTE: Max value is 0xFFFFFFF or 16.777215 seconds.

65.6.8 General Purpose Timer #0 Controller (USBC_n_GPTIMER0CTRL)

This register contains the control for this countdown timer and a data field can be queried to determine the running count value. This timer has granularity on 1 us and can be programmed to a little over 16 seconds. There are two counter modes which are described in the register table below. When the timer counter value transitions to zero, an interrupt could be generated if enable.

USB Core Memory Map/Register Definition

Interrupt status bit is TI0 bit in n_USBSTS register (See [USB Status Register \(USBC_n_USBSTS\)](#)), interrupt enable bit is TIE0 bit in n_USBINTR register. (See [Interrupt Enable Register \(USBC_n_USBINTR\)](#) .)

Address: 218_4000h base + 84h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	GPTRUN	GPTRST	Reserved						GPTMODE							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									GPTCNT							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_GPTIMER0CTRL field descriptions

Field	Description
31 GPTRUN	General Purpose Timer Run GPTCNT bits are not effected when setting or clearing this bit. 0 Stop counting 1 Run
30 G PTRST	General Purpose Timer Reset 0 No action 1 Load counter value from GPTLD bits in n_GPTIMER0LD
29–25 -	This field is reserved. Reserved
24 GPTMODE	General Purpose Timer Mode In one shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by software; In repeat mode, the timer will count down to zero, generate an interrupt and automatically reload the counter value from GPTLD bits to start again. 0 One Shot Mode 1 Repeat Mode
GPTCNT	General Purpose Timer Counter. This field is the count value of the countdown timer.

65.6.9 General Purpose Timer #1 Load (USBC_n_GPTIMER1LD)

This register controls load value of the count timer in register n_GPTIMER1CTRL. Please see [General Purpose Timer #1 Controller \(USBC_n_GPTIMER1CTRL\)](#).

Address: 218_4000h base + 88h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

USBC_n_GPTIMER1LD field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
GPTLD	General Purpose Timer Load Value These bit fields are loaded to GPTCNT bits when GPTRST bit is set '1b'. This value represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. NOTE: Max value is 0xFFFFFFF or 16.777215 seconds.

65.6.10 General Purpose Timer #1 Controller (USBC_n_GPTIMER1CTRL)

This register contains the control for this countdown timer and a data field can be queried to determine the running count value. This timer has granularity on 1 us and can be programmed to a little over 16 seconds. There are two counter modes which are described in the register table below. When the timer counter value transitions to zero, an interrupt could be generated if enable.

Interrupt status bit is TI1 bit in USB_n_USBSTS register (See [USB Status Register \(USBC_n_USBSTS\)](#)), interrupt enable bit is TIE1 bit in n_USBINTR register (See [Interrupt Enable Register \(USBC_n_USBINTR\)](#)).

USB Core Memory Map/Register Definition

Address: 218_4000h base + 8Ch offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	GPTRUN	GPTRST						GPTMODE								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									GPTCNT							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_GPTIMER1CTRL field descriptions

Field	Description
31 GPTRUN	General Purpose Timer Run GPTCNT bits are not effected when setting or clearing this bit. 0 Stop counting 1 Run
30 GPTRST	General Purpose Timer Reset 0 No action 1 Load counter value from GPTLD bits in USB_n_GPTIMER0LD
29–25 -	This field is reserved. Reserved
24 GPTMODE	General Purpose Timer Mode In one shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by software. In repeat mode, the timer will count down to zero, generate an interrupt and automatically reload the counter value from GPTLD bits to start again. 0 One Shot Mode 1 Repeat Mode
GPTCNT	General Purpose Timer Counter. This field is the count value of the countdown timer.

65.6.11 System Bus Config (USBC_n_SBUSCFG)

Address: 218_4000h base + 90h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

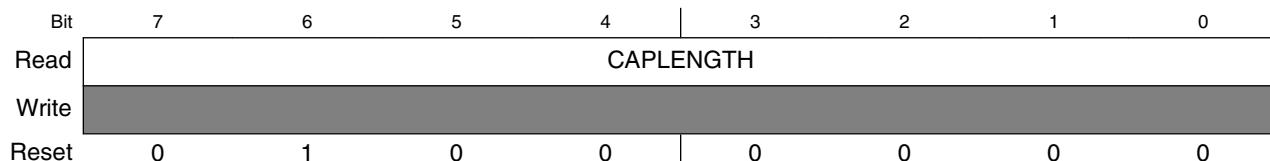
USBC_n_SBUSCFG field descriptions

Field	Description
31–3 -	This field is reserved. Reserved
AHBBRST	AHB master interface Burst configuration These bits control AHB master transfer type sequence (or priority). NOTE: This register overrides n_BURSTSIZEx register when its value is not zero. 000 Incremental burst of unspecified length only 001 INCR4 burst, then single transfer 010 INCR8 burst, INCR4 burst, then single transfer 011 INCR16 burst, INCR8 burst, INCR4 burst, then single transfer 100 Reserved, don't use 101 INCR4 burst, then incremental burst of unspecified length 110 INCR8 burst, INCR4 burst, then incremental burst of unspecified length 111 INCR16 burst, INCR8 burst, INCR4 burst, then incremental burst of unspecified length

65.6.12 Capability Registers Length (USBC_n_CAPLENGTH)

The Capability Registers Length register contains the address offset to the Operational registers relative to the CAPLENGTH register.

Address: 218_4000h base + 100h offset + (512d × i), where i=0d to 3d

**USBC_n_CAPLENGTH field descriptions**

Field	Description
CAPLENGTH	These bits are used as an offset to add to register base to find the beginning of the Operational Register. Default value is '40h'.

65.6.13 Host Controller Interface Version (USBC_n_HCIVERSION)

This is a 2-byte register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

Address: 218_4000h base + 102h offset + (512d × i), where i=0d to 3d

Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
Read	HCIVERSION																
Write																	
Reset	0	0	0	0	0	0	0	1		0	0	0	0	0	0	0	0

USBC_n_HCIVERSION field descriptions

Field	Description
HCIVERSION	Host Controller Interface Version Number Default value is '10h', which means EHCI rev1.0.

65.6.14 Host Controller Structural Parameters (USBC_n_HCSPARAMS)

The following figure shows the port steering logic capabilities of Host Control Structural Parameters (n_HCSPARAMS).

Address: 218_4000h base + 104h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R																	
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R																	
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	1	0	0	0	1

USBC_n_HCSPARAMS field descriptions

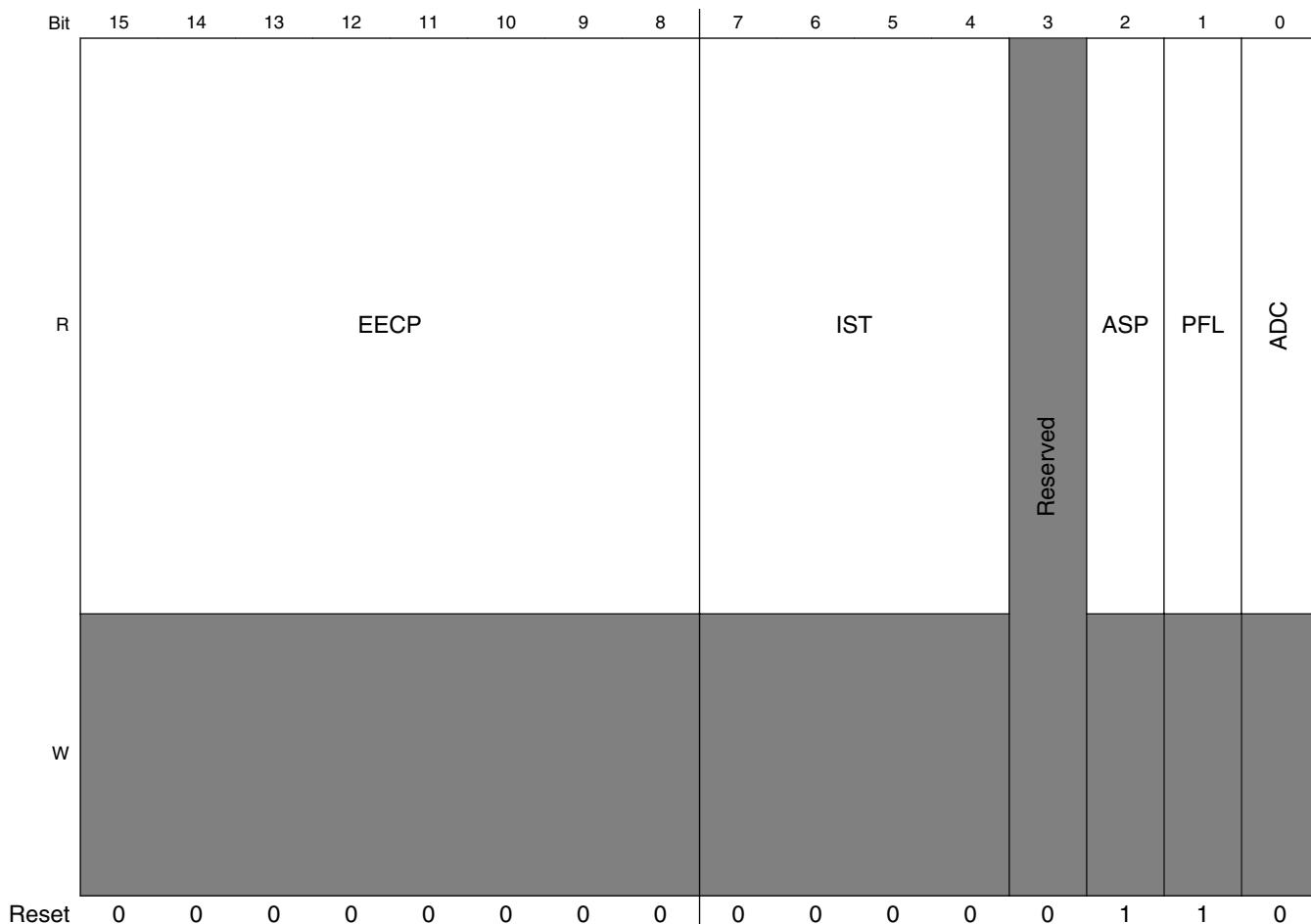
Field	Description
31–28 -	This field is reserved. Reserved
27–24 N_TT	Number of Transaction Translators (N_TT). Default value '0000b' This field indicates the number of embedded transaction translators associated with the USB2.0 host controller. These bits would be set to '0001b' for Multi-Port Host, and '0000b' for Single-Port Host.
23–20 N_PTT	Number of Ports per Transaction Translator (N_PTT). Default value '0000b' This field indicates the number of ports assigned to each transaction translator within the USB2.0 host controller. These bits would be set to equal N_PORTS for Multi-Port Host, and '0000b' for Single-Port Host.
19–17 -	This field is reserved. Reserved
16 PI	Port Indicators (P_INDICATOR) This bit indicates whether the ports support port indicator control. When set to one, the port status and control registers include a read/writeable field for controlling the state of the port indicator This bit is "1b" in all controller core.
15–12 N_CC	Number of Companion Controller (N_CC). This field indicates the number of companion controllers associated with this USB2.0 host controller. These bits are '0000b' in all controller core. 0 There is no internal Companion Controller and port-ownership hand-off is not supported. 1 There are internal companion controller(s) and port-ownership hand-offs is supported.
11–8 N_PCC	Number of Ports per Companion Controller This field indicates the number of ports supported per internal Companion Controller. It is used to indicate the port routing configuration to the system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2 then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, etc. In the previous example, the N_PCC could have been 4, where the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC. These bits are '0000b' in all controller core.
7–5 -	This field is reserved. Reserved
4 PPC	Port Power Control This field indicates whether the host controller implementation includes port power control. A one indicates the ports have port power switches. A zero indicates the ports do not have port power switches. The value of this field affects the functionality of the Port Power field in each port status and control register
N_PORTS	Number of downstream ports. This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register. Valid values are in the range of 1h to Fh. A zero in this field is undefined. These bits are always set to '0001b' because all controller cores are Single-Port Host.

65.6.15 Host Controller Capability Parameters (USBC_n_HCCPARAMS)

This register identifies multiple mode control (time-base bit functionality), addressing capability.

Address: 218_4000h base + 108h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
W	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**USBC_n_HCCPARAMS field descriptions**

Field	Description
31–16 -	This field is reserved. Reserved
15–8 EECP	EHCI Extended Capabilities Pointer. This field indicates the existence of a capabilities list. A value of 00h indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain the consistency of the PCI header defined for this class of device. NOTE: These bits are set '00h' in all controller core.
7–4 IST	Isochronous Scheduling Threshold. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit [7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame. These bits are set '00h' in all controller core.
3 -	This field is reserved. Reserved

Table continues on the next page...

USBC_n_HCCPARAMS field descriptions (continued)

Field	Description
2 ASP	<p>Asynchronous Schedule Park Capability</p> <p>If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the <i>Asynchronous Schedule Park Mode Enable</i> and <i>Asynchronous Schedule Park Mode Count</i> fields in the USBCMD register.</p> <p>NOTE: ASP bit reset value: '00b' for OTG controller core, '11b' for Host-only controller core.</p>
1 PFL	<p>Programmable Frame List Flag</p> <p>If this bit is set to zero, then the system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and must be set to zero.</p> <p>If set to a one, then the system software can specify and use a smaller frame list and configure the host controller via the USBCMD register Frame List Size field. The frame list must always be aligned on a 4K-page boundary. This requirement ensures that the frame list is always physically contiguous.</p> <p>This bit is set '1b' in all controller core.</p>
0 ADC	64-bit Addressing Capability
	This bit is set '0b' in all controller core, no 64-bit addressing capability is supported.

65.6.16 Device Controller Interface Version (USBC_n_DCIVERSION)

This register indicates the two-byte BCD encoding of the device controller interface version number.

Address: 218_4000h base + 120h offset + (512d × i), where i=0d to 0d

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	DCIVERSION															
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

USBC_n_DCIVERSION field descriptions

Field	Description
DCIVERSION	<p>Device Controller Interface Version Number</p> <p>Default value is '01h', which means rev0.1.</p>

65.6.17 Device Controller Capability Parameters (USBC_n_DCCPARAMS)

These fields describe the overall device capability of the controller.

NOTE

This register is only available in OTG controller core.

Address: 218_4000h base + 124h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved								HC	DC	Reserved		DEN			
W																
Reset	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0

USBC_n_DCCPARAMS field descriptions

Field	Description
31–9 -	This field is reserved. Reserved
8 HC	Host Capable When this bit is 1, this controller is capable of operating as an EHCI compatible USB 2.0 host controller.
7 DC	Device Capable When this bit is 1, this controller is capable of operating as a USB 2.0 device.
6–5 -	This field is reserved. Reserved
DEN	Device Endpoint Number This field indicates the number of endpoints built into the device controller. If this controller is not device capable, then this field will be zero. Valid values are 0 - 15.

65.6.18 USB Command Register (USBC_n_USBCMD)

The Command Register indicates the command to be executed by the serial bus host/device controller. Writing to the register causes a command to be executed.

Address: 218_4000h base + 140h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved								ITC							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	FS_2	ATDTW	SUTW	Reserved	ASPE	Reserved	ASP	Reserved	IAA	ASE	PSE	FS_1	RST	RS		
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_USBCMD field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23–16 ITC	Interrupt Threshold Control -Read/Write. The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. ITC contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. Value Maximum Interrupt Interval 0x00 Immediate (no threshold) 0x01 1 micro-frame 0x02 2 micro-frames 0x04 4 micro-frames 0x08 8 micro-frames 0x10 16 micro-frames

Table continues on the next page...

USBC_n_USBCMD field descriptions (continued)

Field	Description
	<p>0x20 32 micro-frames 0x40 64 micro-frames</p>
15 FS_2	<p>See also bits 3-2 Frame List Size - (Read/Write or Read Only). [host mode only] This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index.</p> <p>NOTE: This field is made up from USBCMD bits 15, 3 and 2.</p> <p>Value Meaning</p> <ul style="list-style-type: none"> 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes)
14 ATDTW	<p>Add dTD TripWire - Read/Write. [device mode only] This bit is used as a semaphore to ensure proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set and cleared by software. This bit would also be cleared by hardware when state machine is hazard region for which adding a dTD to a primed endpoint may go unrecognized.</p>
13 SUTW	<p>Setup TripWire - Read/Write. [device mode only] This bit is used as a semaphore to ensure that the setup data payload of 8 bytes is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off (SLOM bit in USB core register n_USBMODE, see USB Device Mode (USBC_n_USBMODE)) then there is a hazard when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set and cleared by software. This bit would also be cleared by hardware when a hazard detected.</p>
12 -	This field is reserved. Reserved
11 ASPE	<p>Asynchronous Schedule Park Mode Enable - Read/Write. If the <i>Asynchronous Park Capability</i> bit in the HCCPARAMS register is a one, then this bit defaults to a 1h and is R/W. Otherwise the bit must be a zero and is RO. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is a zero, Park mode is disabled.</p> <p>NOTE: ASPE bit reset value: '0b' for OTG controller core, '1b' for Host-only controller core.</p>
10 -	This field is reserved. Reserved
9–8 ASP	<p>Asynchronous Schedule Park Mode Count - Read/Write. If the <i>Asynchronous Park Capability</i> bit in the HCCPARAMS register is a one, then this field defaults to 3h and is R/W. Otherwise it defaults to zero and is Read-Only. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the</p>

Table continues on the next page...

USBC_n_USBCMD field descriptions (continued)

Field	Description
	<p>Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 1h to 3h. Software must not write a zero to this bit when <i>Park Mode Enable</i> is a one as this will result in undefined behavior.</p> <p>This field is set to 3h in all controller core.</p>
7 -	<p>This field is reserved. Reserved</p>
6 IAA	<p>Interrupt on Async Advance Doorbell - Read/Write.</p> <p>This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell.</p> <p>When the host controller has evicted all appropriate cached schedule states, it sets the Interrupt on Async Advance status bit in the USBSTS register. If the Interrupt on Sync Advance Enable bit in the USBINTR register is one, then the host controller will assert an interrupt at the next interrupt threshold.</p> <p>The host controller sets this bit to zero after it has set the Interrupt on Sync Advance status bit in the USBSTS register to one. Software should not write a one to this bit when the asynchronous schedule is inactive. Doing so will yield undefined results.</p> <p>This bit is only used in host mode. Writing a one to this bit when device mode is selected will have undefined results.</p>
5 ASE	<p>Asynchronous Schedule Enable - Read/Write. Default 0b.</p> <p>This bit controls whether the host controller skips processing the Asynchronous Schedule.</p> <p>Only the host controller uses this bit.</p> <p>Values Meaning</p> <ul style="list-style-type: none"> 0 Do not process the Asynchronous Schedule. 1 Use the ASYNCLISTADDR register to access the Asynchronous Schedule.
4 PSE	<p>Periodic Schedule Enable- Read/Write. Default 0b.</p> <p>This bit controls whether the host controller skips processing the Periodic Schedule.</p> <p>Only the host controller uses this bit.</p> <p>Values Meaning</p> <ul style="list-style-type: none"> 0 Do not process the Periodic Schedule 1 Use the PERIODICLISTBASE register to access the Periodic Schedule.
3–2 FS_1	See description at bit 15
1 RST	<p>Controller Reset (RESET) - Read/Write. Software uses this bit to reset the controller. This bit is set to zero by the Host/Device Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.</p> <p>Host operation mode:</p> <p>When software writes a one to this bit, the Controller resets its internal pipelines, timers, counters, state machines etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. Software should not set this bit to a one when the HCHalted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.</p> <p>Device operation mode:</p>

Table continues on the next page...

USBC_n_USBCMD field descriptions (continued)

Field	Description
	When software writes a one to this bit, the Controller resets its internal pipelines, timers, counters, state machines etc. to their initial value. Writing a one to this bit when the device is in the attached state is not recommended, because the effect on an attached host is undefined. In order to ensure that the device is not in an attached state before initiating a device controller reset, all primed endpoints should be flushed and the USBCMD Run/Stop bit should be set to 0.
0 RS	<p>Run/Stop (RS) - Read/Write. Default 0b. 1=Run. 0=Stop.</p> <p>Host operation mode:</p> <p>When set to '1b', the Controller proceeds with the execution of the schedule. The Controller continues execution as long as this bit is set to a one. When this bit is set to 0, the Host Controller completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the Controller has finished the transaction and has entered the stopped state. Software should not write a one to this field unless the controller is in the Halted state (that is, HCHalted in the USBSTS register is a one).</p> <p>Device operation mode:</p> <p>Writing a one to this bit will cause the controller to enable a pull-up on D+ and initiate an attach event. This control bit is not directly connected to the pull-up enable, as the pull-up will become disabled upon transitioning into high-speed mode. Software should use this bit to prevent an attach event before the controller has been properly initialized. Writing a 0 to this will cause a detach event.</p>

65.6.19 USB Status Register (USBC_n_USBSTS)

This register indicates various states of the Host/Device Controller and any pending interrupts. This register does not indicate status resulting from a transaction on the serial bus.

Address: 218_4000h base + 144h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																NAK1
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Detailed description: The register is 32 bits wide. Bits 31-26 are reserved. Bit 25 is TI1, bit 24 is TI0, both are read-only. Bits 23-16 are reserved. Bit 15 is NAK1, which is write-only. All other bits (22, 21, 20, 19, 18, 17) are read-only. The register is initialized to 0x00000000 at reset.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
	AS	PS	RCL	HCH	Reserved	ULPII	Reserved	SLI	SRI	URI	AAI	SEI	FRI	PCI	UEI	UI
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_USBSTS field descriptions

Field	Description
31–26 -	This field is reserved. Reserved
25 TI1	General Purpose Timer Interrupt 1(GPTINT1)--R/WC. This bit is set when the counter in the GPTIMER1CTRL register transitions to zero, writing a one to this bit will clear it.
24 TI0	General Purpose Timer Interrupt 0(GPTINT0)--R/WC. This bit is set when the counter in the GPTIMER0CTRL register transitions to zero, writing a one to this bit clears it.
23–17 -	This field is reserved. Reserved
16 NAKI	NAK Interrupt Bit--RO. This bit is set by hardware when for a particular endpoint both the TX/RX Endpoint NAK bit and corresponding TX/RX Endpoint NAK Enable bit are set. This bit is automatically cleared by hardware when all Enabled TX/RX Endpoint NAK bits are cleared.
15 AS	Asynchronous Schedule Status - Read Only. This bit reports the current real status of the Asynchronous Schedule. When set to zero the asynchronous schedule status is disabled and if set to one the status is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0). Only used in the host operation mode.
14 PS	Periodic Schedule Status - Read Only.

Table continues on the next page...

USBC_n_USBSTS field descriptions (continued)

Field	Description
	<p>This bit reports the current real status of the Periodic Schedule. When set to zero the periodic schedule is disabled, and if set to one the status is enabled. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).</p> <p>Only used in the host operation mode.</p>
13 RCL	<p>Reclamation - Read Only.</p> <p>This is a read-only status bit used to detect an empty asynchronous schedule.</p> <p>Only used in the host operation mode.</p>
12 HCH	<p>HCHalted - Read Only.</p> <p>This bit is a zero whenever the Run/Stop bit is a one. The Controller sets this bit to one after it has stopped executing because of the Run/Stop bit being set to 0, either by software or by the Controller hardware (for example, an internal error).</p> <p>Only used in the host operation mode.</p> <p>Default value is '0b' for OTG core, and '1b' for Host1/Host2/Host3 core.</p> <p>This is because OTG core is not operating as host in default. Please see CM bit in USB_n_USBMODE register.</p> <p>NOTE: HCH bit reset value: '0b' for OTG controller core, '1b' for Host-only controller core.</p>
11 -	<p>This field is reserved.</p> <p>Reserved</p>
10 ULPII	<p>ULPI Interrupt - R/WC.</p> <p>This bit will be set '1b' by hardware when there is an event completion in ULPI viewport.</p> <p>This bit is usable only if the controller support UPLI interface mode.</p>
9 -	<p>This field is reserved.</p> <p>Reserved</p>
8 SLI	<p>DCSuspend - R/WC.</p> <p>When a controller enters a suspend state from an active state, this bit will be set to a one. The device controller clears the bit upon exiting from a suspend state.</p> <p>Only used in device operation mode.</p>
7 SRI	<p>SOF Received - R/WC.</p> <p>When the device controller detects a Start Of (micro) Frame, this bit will be set to a one. When a SOF is extremely late, the device controller will automatically set this bit to indicate that an SOF was expected. Therefore, this bit will be set roughly every 1ms in device FS mode and every 125ms in HS mode and will be synchronized to the actual SOF that is received.</p> <p>Because the device controller is initialized to FS before connect, this bit will be set at an interval of 1ms during the prelude to connect and chirp.</p> <p>In host mode, this bit will be set every 125us and can be used by host controller driver as a time base.</p> <p>Software writes a 1 to this bit to clear it.</p>
6 URI	<p>USB Reset Received - R/WC.</p> <p>When the device controller detects a USB Reset and enters the default state, this bit will be set to a one. Software can write a 1 to this bit to clear the USB Reset Received status bit.</p> <p>Only used in device operation mode.</p>

Table continues on the next page...

USBC_n_USBSTS field descriptions (continued)

Field	Description
5 AAI	<p>Interrupt on Async Advance - R/WC.</p> <p>System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the n_USBCMD register. This status bit indicates the assertion of that interrupt source.</p> <p>Only used in host operation mode.</p>
4 SEI	<p>System Error- R/WC.</p> <p>This bit is will be set to '1b' when an Error response is seen to a read on the system interface.</p>
3 FRI	<p>Frame List Rollover - R/WC.</p> <p>The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example. If the frame list size (as programmed in the Frame List Size field of the USB_n_USBCMD register) is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FHINDEX [12] toggles.</p> <p>Only used in host operation mode.</p>
2 PCI	<p>Port Change Detect - R/WC.</p> <p>The Host Controller sets this bit to a one when on any port a Connect Status occurs, a Port Enable/Disable Change occurs, or the Force Port Resume bit is set as the result of a J-K transition on the suspended port.</p> <p>The Device Controller sets this bit to a one when the port controller enters the full or high-speed operational state. When the port controller exits the full or high-speed operation states due to Reset or Suspend events, the notification mechanisms are the USB Reset Received bit and the DCSuspend bits respectively.</p>
1 UEI	<p>USB Error Interrupt (USBERRINT) - R/WC.</p> <p>When completion of a USB transaction results in an error condition, this bit is set by the Host/Device Controller. This bit is set along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt on complete (IOC) bit set</p> <p>The device controller detects resume signaling only.</p>
0 UI	<p>USB Interrupt (USBINT) - R/WC.</p> <p>This bit is set by the Host/Device Controller when the cause of an interrupt is a completion of a USB transaction where the Transfer Descriptor (TD) has an interrupt on complete (IOC) bit set.</p> <p>This bit is also set by the Host/Device Controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.</p>

65.6.20 Interrupt Enable Register (USBC_n_USBINTR)

The interrupts to software are enabled with this register. An interrupt is generated when a bit is set and the corresponding interrupt source is active. The USB Status register (n_USBSTS) still shows interrupt sources even if they are disabled by the n_USBINTR register, allowing polling of interrupt events by the software.

Address: 218_4000h base + 148h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R							TIE1	TIE0					UPIE	UAIE	Reserved	NAKE	
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R				-		ULPIE		Reserved	SLE	SRE	URE	AAE	SEE	FRE	PCE	UEE	UE
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

USBC_n_USBINTR field descriptions

Field	Description
31–26 -	This field is reserved. Reserved
25 TIE1	General Purpose Timer #1 Interrupt Enable When this bit is one and the TI1 bit in n_USBSTS register is a one the controller will issue an interrupt.
24 TIE0	General Purpose Timer #0 Interrupt Enable When this bit is one and the TI0 bit in n_USBSTS register is a one the controller will issue an interrupt.
23–20 -	This field is reserved. Reserved
19 UPIE	USB Host Periodic Interrupt Enable

Table continues on the next page...

USBC_n_USBINTR field descriptions (continued)

Field	Description
	When this bit is one, and the UPI bit in the n_USBSTS register is one, host controller will issue an interrupt at the next interrupt threshold.
18 UAIE	USB Host Asynchronous Interrupt Enable When this bit is one, and the UAI bit in the n_USBSTS register is one, host controller will issue an interrupt at the next interrupt threshold.
17 -	This field is reserved. Reserved
16 NAKE	NAK Interrupt Enable When this bit is one and the NAKI bit in n_USBSTS register is a one the controller will issue an interrupt.
15–11 -	These bits are reserved and should be set to zero.
10 ULPIE	ULPI Interrupt Enable When this bit is one and the UPLII bit in n_USBSTS register is a one the controller will issue an interrupt. This bit is usable only if the controller support UPLI interface mode.
9 -	This field is reserved. Reserved
8 SLE	Sleep Interrupt Enable When this bit is one and the SLI bit in n_n_USBSTS register is a one the controller will issue an interrupt. Only used in device operation mode.
7 SRE	SOF Received Interrupt Enable When this bit is one and the SRI bit in n_USBSTS register is a one the controller will issue an interrupt.
6 URE	USB Reset Interrupt Enable When this bit is one and the URI bit in n_USBSTS register is a one the controller will issue an interrupt. Only used in device operation mode.
5 AAE	Async Advance Interrupt Enable When this bit is one and the AAI bit in n_USBSTS register is a one the controller will issue an interrupt. Only used in host operation mode.
4 SEE	System Error Interrupt Enable When this bit is one and the SEI bit in n_USBSTS register is a one the controller will issue an interrupt. Only used in host operation mode.
3 FRE	Frame List Rollover Interrupt Enable When this bit is one and the FRI bit in n_USBSTS register is a one the controller will issue an interrupt. Only used in host operation mode.
2 PCE	Port Change Detect Interrupt Enable When this bit is one and the PCI bit in n_USBSTS register is a one the controller will issue an interrupt.
1 UEE	USB Error Interrupt Enable When this bit is one and the UEI bit in n_USBSTS register is a one the controller will issue an interrupt.
0 UE	USB Interrupt Enalbe When this bit is one and the UI bit in n_USBSTS register is a one the controller will issue an interrupt.

65.6.21 USB Frame Index (USBC_n_FRINDEX)

This register is used by the host controller to index the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [N: 3] are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by system software in the Frame List Size field in the n_USBCMD register.

This register must be written as a DWord. Byte writes produce-undefined results. This register cannot be written unless the Host Controller is in the 'Halted' state as indicated by the HCHalted bit. A write to this register while the Run/Stop hit is set to a one produces undefined results. Writes to this register also affect the SOF value.

In device mode this register is read only and, the device controller updates the FRINDEX [13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX [13:3] will be checked against the SOF marker. If FRINDEX [13:3] is different from the SOF marker, FRINDEX [13:3] will be set to the SOF value and FRINDEX [2:0] will be set to zero (that is, SOF for 1 ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX [2:0] will be increment (that is, SOF for 125 us micro-frame.).

Address: 218_4000h base + 14Ch offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

USBC_n_FRINDEX field descriptions

Field	Description
31–14 -	This field is reserved. Reserved
FRINDEX	Frame Index. The value, in this register, increments at the end of each time frame (micro-frame). Bits [N: 3] are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following illustrates values of N based on the value of the Frame List Size field in the USBCMD register, when used in host mode. USBCMD [Frame List Size] Number Elements N In device mode the value is the current frame number of the last frame transmitted. It is not used as an index. In either mode bits 2:0 indicate the current microframe. 000 (1024) 12 001 (512) 11

Table continues on the next page...

USBC_n_FRINDEX field descriptions (continued)

Field	Description
	010 (256) 10
	011 (128) 9
	100 (64) 8
	101 (32) 7
	110 (16) 6
	111 (8) 5

**65.6.22 Frame List Base Address
(USBC_n_PERIODICLISTBASE)**

Host Controller only

This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. HCD loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the Frame Index Register (USB_n_FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.

Address: 218_4000h base + 154h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

USBC_n_PERIODICLISTBASE field descriptions

Field	Description
31–12 BASEADR	Base Address (Low). These bits correspond to memory address signals [31:12], respectively. Only used by the host controller.
-	This field is reserved. Reserved

65.6.23 Device Address (USBC_n_DEVICEADDR)

Device Controller only

USB Core Memory Map/Register Definition

The upper seven bits of this register represent the device address. After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. Software shall reprogram the address after receiving a SET_ADDRESS descriptor.

Address: 218_4000h base + 154h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R								USBADRA								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_DEVICEADDR field descriptions

Field	Description
31–25 USBADR	Device Address. These bits correspond to the USB device address
24 USBADRA	Device Address Advance. Default=0. When this bit is '0', any writes to USBADR are instantaneous. When this bit is written to a '1' at the same time or before USBADR is written, the write to the USBADR field is staged and held in a hidden register. After an IN occurs on endpoint 0 and is ACKed, USBADR will be loaded from the holding register. Hardware will automatically clear this bit on the following conditions: 1) IN is ACKed to endpoint 0. (USBADR is updated from staging register). 2) OUT/SETUP occur to endpoint 0. (USBADR is not updated). 3) Device Reset occurs (USBADR is reset to 0). NOTE: After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism will ensure this specification is met when the DCD can not write of the device address within 2ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA=1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR will be programmed instantly at the correct time and meet the 2ms USB requirement.
-	This field is reserved. Reserved

65.6.24 Next Asynch. Address (USBC_n_ASYNCLISTADDR)

Host Controller only

This 32-bit register contains the address of the next asynchronous queue head to be executed by the host. Bits [4:0] of this register cannot be modified by the system software and will always return a zero when read.

Address: 218_4000h base + 158h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

USBC_n_ASYNCLISTADDR field descriptions

Field	Description
31–5 ASYBASE	<p>Link Pointer Low (LPL).</p> <p>These bits correspond to memory address signals [31:5], respectively. This field may only reference a Queue Head (QH).</p> <p>Only used by the host controller.</p>
-	<p>This field is reserved.</p> <p>Reserved</p>

65.6.25 Endpoint List Address (USBC_n_ENDPTLISTADDR)

Device Controller only

In device mode, this register contains the address of the top of the endpoint list in system memory. Bits [10:0] of this register cannot be modified by the system software and will always return a zero when read.

The memory structure referenced by this physical memory pointer is assumed 64-byte.

Address: 218_4000h base + 158h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

USBC_n_ENDPTLISTADDR field descriptions

Field	Description
31–11 EPBASE	<p>Endpoint List Pointer(Low). These bits correspond to memory address signals [31:11], respectively. This field will reference a list of up to 32 Queue Head (OH) (that is, one queue head per endpoint & direction).</p>
-	<p>This field is reserved.</p> <p>Reserved</p>

65.6.26 Programmable Burst Size (USBC_n_BURSTSIZE)

This register is used to control the burst size used during data movement on the AHB master interface. This register is ignored if AHBBRST bits in SBUSCFG register is non-zero value.

Address: 218_4000h base + 160h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																																	
W																																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

USBC_n_BURSTSIZE field descriptions

Field	Description
31–17 -	This field is reserved. Reserved
16–8 TXPBURST	Programmable TX Burst Size. Default value is determined by TXBURST bits in n_HWTXBUF. This register represents the maximum length of a the burst in 32-bit words while moving data from system memory to the USB bus.
RXPBURST	Programmable RX Burst Size. Default value is determined by TXBURST bits in n_HWRXBUF. This register represents the maximum length of a the burst in 32-bit words while moving data from the USB bus to system memory.

65.6.27 TX FIFO Fill Tuning (USBC_n_TXFILLTUNING)

The fields in this register control performance tuning associated with how the host controller posts data to the TX latency FIFO before moving the data onto the USB bus. The specific areas of performance include the how much data to post into the FIFO and an estimate for how long that operation should take in the target system.

Definitions:

T_0 = Standard packet overhead

T_1 = Time to send data payload

T_{ff} = Time to fetch packet into TX FIFO up to specified level.

T_s = Total Packet Flight Time (send-only) packet

$T_s = T_0 + T_1$

T_p = Total Packet Time (fetch and send) packet

$$T_p = T_{ff} + T_0 + T_1$$

Upon discovery of a transmit (OUT/SETUP) packet in the data structures, host controller checks to ensure T_p remains before the end of the [micro]frame. If so it proceeds to pre-fill the TX FIFO. If at anytime during the pre-fill operation the time remaining the [micro]frame is $< T_s$ then the packet attempt ceases and the packet is tried at a later time. Although this is not an error condition and the host controller will eventually recover, a mark will be made the scheduler health counter to note the occurrence of a "back-off" event. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that will begin after the next SOF. Too many back-off events can waste bandwidth and power on the system bus and thus should be minimized (not necessarily eliminated). Back-offs can be minimized with use of the n_TSCHHEALTH (T_{ff}) described below.

NOTE

The reset value could vary from instance to instance. Please see the detail in bit field description and ignore reset value in summary table in this case!

Address: 218_4000h base + 164h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

USBC_n_TXFILLTUNING field descriptions

Field	Description
31–22 -	This field is reserved. Reserved
21–16 TXFIFOTHRES	FIFO Burst Threshold. (Read/Write) This register controls the number of data bursts that are posted to the TX latency FIFO in host mode before the packet begins on to the bus. The minimum value is 2 and this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory. This value is ignored if the Stream Disable bit in USB_n_USBMODE register is set. Default value is '00h' for OTG controller core, and '02h' for Host-only controller core.
15–13 -	This field is reserved. Reserved
12–8 TXSCHHEALTH	Scheduler Health Counter. (Read/Write To Clear) This register increments when the host controller fails to fill the TX latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next Start-Of-Frame. This health counter measures the number of times this occurs to provide feedback to selecting a proper TXSCHOH. Writing to this register will clear the counter and this counter will max. at 31. Default value is '08h' for OTG controller core, and '00h' for Host-only controller core.

Table continues on the next page...

USBC_n_TXFILLTUNING field descriptions (continued)

Field	Description
TXSCHOH	<p>Scheduler Overhead. (Read/Write) [Default = 0]</p> <p>This register adds an additional fixed offset to the schedule time estimator described above as Tff. As an approximation, the value chosen for this register should limit the number of back-off events captured in the TXSCHHEALTH to less than 10 per second in a highly utilized bus. Choosing a value that is too high for this register is not desired as it can needlessly reduce USB utilization. The time unit represented in this register is 1.267us when a device is connected in High-Speed Mode. The time unit represented in this register is 6.333us when a device is connected in Low/Full Speed Mode.</p> <p>Default value is '08h' for OTG controller core, and '00h' for Host-only controller core.</p>

65.6.28 Endpoint NAK (USBC_n_ENDPTNAK)

Address: 218_4000h base + 178h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved						EPTN						Reserved						EPRN													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

USBC_n_ENDPTNAK field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23–16 EPTN	TX Endpoint NAK - R/WC. Each TX endpoint has 1 bit in this field. The bit is set when the device sends a NAK handshake on a received IN token for the corresponding endpoint. Bit [N] - Endpoint #[N], N is 0-7
15–8 -	This field is reserved. Reserved
EPRN	RX Endpoint NAK - R/WC. Each RX endpoint has 1 bit in this field. The bit is set when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint. Bit [N] - Endpoint #[N], N is 0-7

65.6.29 Endpoint NAK Enable (USBC_n_ENDPTNAKEN)

Address: 218_4000h base + 17Ch offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved						EPTNE						Reserved						EPRNE													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

USBC_n_ENDPTNAKEN field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23–16 EPTNE	TX Endpoint NAK Enable - R/W. Each bit is an enable bit for the corresponding TX Endpoint NAK bit. If this bit is set and the corresponding TX Endpoint NAK bit is set, the NAK Interrupt bit is set. Bit [N] - Endpoint #[N], N is 0-7
15–8 -	This field is reserved. Reserved
EPRNE	RX Endpoint NAK Enable - R/W. Each bit is an enable bit for the corresponding RX Endpoint NAK bit. If this bit is set and the corresponding RX Endpoint NAK bit is set, the NAK Interrupt bit is set. Bit [N] - Endpoint #[N], N is 0-7

65.6.30 Configure Flag Register (USBC_n_CONFIGFLAG)

Address: 218_4000h base + 180h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
	R	Reserved															
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
	R	Reserved															CF
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	1

USBC_n_CONFIGFLAG field descriptions

Field	Description
31–1 -	This field is reserved. Reserved
0 CF	Configure Flag Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic. 0 Port routing control logic default-routes each port to an implementation dependent classic host controller. 1 Port routing control logic default-routes all ports to this host controller.

65.6.31 Port Status & Control (USBC_n_PORTSC1)

Host Controller

A host controller could implement one to eight port status and control registers. The number is determined by N_PORTS bits in HWSPARAMs register (please see [Host Controller Structural Parameters \(USBC_n_HCSPARAMS\)](#)). Software could read this parameter register to determine how many ports need service.

All controller cores are Single-Port Host, so there is only one port status and control register for each controller core.

This register is only reset by power on reset or controller core reset. The initial conditions of a port are:

- No device connected
- Port disabled

If the port supports power control, this state remains until port power is supplied (by software).

Device Controller

A device controller has only port register one (PORTSC1) and it does not support power control. Port control in device mode is only used for status port reset, suspend, and current connect status. It is also used to initiate test mode or force signaling and allows software to put the PHY into low power suspend mode and disable the PHY clock.

Address: 218_4000h base + 184h offset + (512d × i), where i=0d to 3d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W	PTS_1	STS	PTW	PSPD	PTS ₂	PFSC	PHCD	WKOC	WKDC	WKCN				PTC		
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PIC	PO	PP	LS	HSP	PR	SUSP	FPR	OCC	OCA	PEC	PE	CSC	CCS		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_PORTSC1 field descriptions

Field	Description
31–30 PTS_1	<p>Bit field {bit25, bit31, bit30}:</p> <p>"000b" UTMI/UTMI+</p> <p>"001b" Reserved</p> <p>"010b" ULPi</p> <p>"011b" Serial/USB 1.1 PHY/IC-USB (FS Only)</p> <p>"100b" HSIC</p> <p>Parallel Transceiver Select (bit25, bit31, bi30).</p> <p>For OTG core, it is Read-Only. Reset value is 000b.</p> <p>For Host1/Host2/Host3 core, it is Read/Write. Reset value is 000b.</p> <p>NOTE: All USB port interface modes are listed in this field description, but not all are supported. For detail feature of each controller core, please see Features. The behaviour is unknown when unsupported interface mode is selected.</p>
29 STS	<p>Serial Transceiver Select - Read Only</p> <p>Serial Transceiver Select</p> <p>1 Serial Interface Engine is selected</p> <p>0 Parallel Interface signals is selected</p> <p>Serial Interface Engine can be used in combination with UTMI+/ULPI physical interface to provide FS/LS signaling instead of the parallel interface signals.</p> <p>When this bit is set '1b', serial interface engine will be used instead of parallel interface signals.</p> <p>This bit has no effect unless PTS bits is set to select UTMI+/ULPI interface.</p> <p>The Serial/USB1.1 PHY/IC-USB will use the serial interface engine for FS/LS signaling regardless of this bit value.</p>
28 PTW	<p>Parallel Transceiver Width</p> <p>This bit has no effect if serial interface engine is used.</p> <p>For OTG/Host1/Host2/Host3 core, it is Read-Only. Reset value is '1b'.</p>

Table continues on the next page...

USBC_n_PORTSC1 field descriptions (continued)

Field	Description
	<p>0 Select the 8-bit UTMI interface [60MHz] 1 Select the 16-bit UTMI interface [30MHz]</p>
27–26 PSPD	<p>Port Speed - Read Only. This register field indicates the speed at which the port is operating.</p> <p>00 Full Speed 01 Low Speed 10 High Speed 11 Undefined</p>
25 PTS_2	See description at bits 31-30
24 PFSC	<p>Port Force Full Speed Connect - Read/Write. Default = 0b. When this bit is set to '1b', the port will be forced to only connect at Full Speed, It disables the chirp sequence that allows the port to identify itself as High Speed.</p> <p>1 Forced to full speed 0 Normal operation</p>
23 PHCD	<p>PHY Low Power Suspend - Clock Disable (PLPSCD) - Read/Write. Default = 0b. When this bit is set to '1b', the PHY clock is disabled. Reading this bit will indicate the status of the PHY clock.</p> <p>NOTE: The PHY clock cannot be disabled if it is being used as the system clock. In device mode, The PHY can be put into Low Power Suspend when the device is not running (USBCMD Run/Stop=0b) or the host has signaled suspend (PORTSC1 SUSPEND=1b). PHY Low power suspend will be cleared automatically when the host initiates resume. Before forcing a resume from the device, the device controller driver must clear this bit. In host mode, the PHY can be put into Low Power Suspend when the downstream device has been put into suspend mode or when no downstream device is connected. Low power suspend is completely under the control of software.</p> <p>1 Disable PHY clock 0 Enable PHY clock</p>
22 WKOC	<p>Wake on Over-current Enable (WKOC_E) - Read/Write. Default = 0b. Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. This field is zero if <i>Port Power(Port Status & Control (USBC_n_PORTSC1))</i> is zero.</p>
21 WKDC	<p>Wake on Disconnect Enable (WKDSCNNT_E) - Read/Write. Default=0b. Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if <i>Port Power(Port Status & Control (USBC_n_PORTSC1))</i> is zero or in device mode.</p>
20 WKCN	<p>Wake on Connect Enable (WKCNNT_E) - Read/Write. Default=0b. Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. This field is zero if <i>Port Power(Port Status & Control (USBC_n_PORTSC1))</i> is zero or in device mode.</p>
19–16 PTC	<p>Port Test Control - Read/Write. Default = 0000b. Refer to Port Test Mode for the operational model for using these test modes and the USB Specification Revision 2.0, Chapter 7 for details on each test mode.</p>

Table continues on the next page...

USBC_n_PORTSC1 field descriptions (continued)

Field	Description																		
	<p>The FORCE_ENABLE_FS and FORCE_ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point.</p> <p>NOTE: <i>Low speed operations are not supported as a peripheral device.</i></p> <p>Any other value than zero indicates that the port is operating in test mode.</p> <p>Value Specific Test</p> <table> <tr><td>0000</td><td>TEST_MODE_DISABLE</td></tr> <tr><td>0001</td><td>J_STATE</td></tr> <tr><td>0010</td><td>K_STATE</td></tr> <tr><td>0011</td><td>SE0 (host) / NAK (device)</td></tr> <tr><td>0100</td><td>Packet</td></tr> <tr><td>0101</td><td>FORCE_ENABLE_HS</td></tr> <tr><td>0110</td><td>FORCE_ENABLE_FS</td></tr> <tr><td>0111</td><td>FORCE_ENABLE_LS</td></tr> <tr><td>1000-1111</td><td>Reserved</td></tr> </table>	0000	TEST_MODE_DISABLE	0001	J_STATE	0010	K_STATE	0011	SE0 (host) / NAK (device)	0100	Packet	0101	FORCE_ENABLE_HS	0110	FORCE_ENABLE_FS	0111	FORCE_ENABLE_LS	1000-1111	Reserved
0000	TEST_MODE_DISABLE																		
0001	J_STATE																		
0010	K_STATE																		
0011	SE0 (host) / NAK (device)																		
0100	Packet																		
0101	FORCE_ENABLE_HS																		
0110	FORCE_ENABLE_FS																		
0111	FORCE_ENABLE_LS																		
1000-1111	Reserved																		
15–14 PIC	<p>Port Indicator Control - Read/Write. Default = Ob.</p> <p>Writing to this field has no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero.</p> <p>Refer to the USB Specification Revision 2.0 for a description on how these bits are to be used.</p> <p>This field is zero if <i>Port Power</i> is zero.</p> <p>Bit Value Meaning</p> <table> <tr><td>00</td><td>Port indicators are off</td></tr> <tr><td>01</td><td>Amber</td></tr> <tr><td>10</td><td>Green</td></tr> <tr><td>11</td><td>Undefined</td></tr> </table>	00	Port indicators are off	01	Amber	10	Green	11	Undefined										
00	Port indicators are off																		
01	Amber																		
10	Green																		
11	Undefined																		
13 PO	<p>Port Owner-Read/Write. Default = 0.</p> <p>This bit unconditionally goes to a 0 when the configured bit in the CONFIGFLAG register makes a 0 to 1 transition. This bit unconditionally goes to 1 whenever the Configured bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that an internal companion controller owns and controls the port.</p> <p>Port owner handoff is not supported in all controller cores, therefore this bit will always be 0.</p>																		
12 PP	<p>Port Power (PP)-Read/Write or Read Only.</p> <p>The function of this bit depends on the value of the Port Power Switching (PPC) field in the HCSPARAMS register. The behavior is as follows:</p> <p>PPC PP Operation</p> <p>0 1b Read Only - Host controller does not have port power control switches. Each port is hard-wired to power.</p> <p>1 1b/0b - Read/Write. Host/OTG controller requires port power control switches. This bit represents the current setting of the switch (0=off, 1=on). When power is not available on a port (that is, PP equals a 0), the port is non-functional and will not report attaches, detaches, etc.</p>																		

Table continues on the next page...

USBC_n_PORTSC1 field descriptions (continued)

Field	Description
	<p>When an over-current condition is detected on a powered port and PPC is a one, the PP bit in each affected port may be transitional by the host controller driver from a one to a zero (removing power from the port).</p> <p>This feature is implemented in all controller cores (PPC = 1).</p>
11–10 LS	<p>Line Status-Read Only. These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines.</p> <p>In host mode, the use of linestate by the host controller driver is not necessary (unlike EHCI), because the port controller state machine and the port routing manage the connection of LS and FS.</p> <p>In device mode, the use of linestate by the device controller driver is not necessary.</p> <p>The encoding of the bits are:</p> <p>Bits [11:10] Meaning</p> <ul style="list-style-type: none"> 00 SE0 10 J-state 01 K-state 11 Undefined
9 HSP	<p>High-Speed Port - Read Only. Default = 0b.</p> <p>When the bit is one, the host/device connected to the port is in high-speed mode and if set to zero, the host/device connected to the port is not in a high-speed mode.</p> <p>NOTE: HSP is redundant with PSPD(bit 27, 26) but remained for compatibility.</p>
8 PR	<p>Port Reset - Read/Write or Read Only. Default = 0b.</p> <p>In Host Mode: Read/Write. 1=Port is in Reset. 0=Port is not in Reset. Default 0.</p> <p>When software writes a one to this bit the bus-reset sequence as defined in the USB Specification Revision 2.0 is started. <i>This bit will automatically change to zero after the reset sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the reset duration is timed in the driver.</i></p> <p>In Device Mode: This bit is a read only status bit. Device reset from the USB bus is also indicated in the USBSTS register.</p> <p>This field is zero if Port Power/Port Status & Control (USBC_n_PORTSC1) is zero.</p>
7 SUSP	<p>Suspend - Read/Write or Read Only. Default = 0b.</p> <p>1=Port in suspend state. 0=Port not in suspend state.</p> <p>In Host Mode: Read/Write.</p> <p>Port Enabled Bit and Suspend bit of this register define the port states as follows:</p> <p>Bits [Port Enabled, Suspend] Port State</p> <ul style="list-style-type: none"> 0x Disable 10 Enable 11 Suspend <p>When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the</p>

Table continues on the next page...

USBC_{_n}_PORTSC1 field descriptions (continued)

Field	Description
	<p>The host controller will unconditionally set this bit to zero when software sets the <i>Force Port Resume</i> bit to zero. The host controller ignores a write of zero to this bit.</p> <p>If host software sets this bit to a one when the port is not enabled (that is, <i>Port enabled</i> bit is a zero) the results are undefined.</p> <p>This field is zero if <i>Port Power/Port Status & Control (USBC_{_n}_PORTSC1)</i> is zero in host mode.</p> <p>In Device Mode: Read Only.</p> <p>In device mode this bit is a read only status bit.</p>
6 FPR	<p>Force Port Resume -Read/Write. 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. Default = 0.</p> <p>In Host Mode:</p> <p>Software sets this bit to one to drive resume signaling. The Host Controller sets this bit to one if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the <i>Port Change Detect</i> bit in the USBSTS register is also set to one. <i>This bit will automatically change to zero after the resume sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the resume duration is timed in the driver.</i></p> <p>Note that when the Host controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. This bit will remain a one until the port has switched to the high-speed idle. Writing a zero has no effect because the port controller will time the resume operation clear the bit the port control state switches to HS or FS idle.</p> <p>This field is zero if <i>Port Power/Port Status & Control (USBC_{_n}_PORTSC1)</i> is zero in host mode.</p> <p>This bit is not-EHCI compatible.</p> <p>In Device mode:</p> <p>After the device has been in Suspend State for 5ms or more, software must set this bit to one to drive resume signaling before clearing. The Device Controller will set this bit to one if a J-to-K transition is detected while the port is in the Suspend state. The bit will be cleared when the device returns to normal operation. Also, when this bit wil be cleared because a K-to-J transition detected, the <i>Port Change Detect</i> bit in the USBSTS register is also set to one.</p>
5 OCC	<p>Over-current Change-R/WC. Default=0.</p> <p>This bit is set '1b' by hardware when there is a change to Over-current Active. Software can clear this bit by writing a one to this bit position.</p>
4 OCA	<p>Over-current Active-Read Only. Default 0.</p> <p>This bit will automatically transition from one to zero when the over current condition is removed.</p> <p>1 This port currently has an over-current condition 0 This port does not have an over-current condition.</p>
3 PEC	<p>Port Enable/Disable Change-R/WC. 1=Port enabled/disabled status has changed. 0=No change. Default = 0.</p> <p>In Host Mode:</p> <p>For the root hub, this bit is set to a one only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification). Software clears this by writing a one to it.</p> <p>This field is zero if <i>Port Power/Port Status & Control (USBC_{_n}_PORTSC1)</i> is zero.</p> <p>In Device mode:</p>

Table continues on the next page...

USBC_{_n} PORTSC1 field descriptions (continued)

Field	Description
2 PE	<p>The device port is always enabled, so this bit is always '0b'.</p> <p>In Host Mode:</p> <p>Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events.</p> <p>When the port is disabled, (0b) downstream propagation of data is blocked except for reset.</p> <p>This field is zero if <i>Port Power(Port Status & Control (USBC_{_n} PORTSC1))</i> is zero in host mode.</p> <p>In Device Mode:</p> <p>The device port is always enabled, so this bit is always '1b'.</p>
1 CSC	<p>Connect Status Change-R/WC. 1 =Change in Current Connect Status. 0=No change. Default 0.</p> <p>In Host Mode:</p> <p>Indicates a change has occurred in the port's Current Connect Status. The host/device controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (that is, the bit will remain set). Software clears this bit by writing a one to it.</p> <p>This field is zero if <i>Port Power(Port Status & Control (USBC_{_n} PORTSC1))</i> is zero in host mode.</p> <p>In Device Mode:</p> <p>This bit is undefined in device controller mode.</p>
0 CCS	<p>Current Connect Status-Read Only.</p> <p>In Host Mode:</p> <p>1=Device is present on port. 0=No device is present. Default = 0. This value reflects the current state of the port, and may not correspond directly to the event that caused the <i>Connect Status Change</i> bit (Bit 1) to be set.</p> <p>This field is zero if <i>Port Power(Port Status & Control (USBC_{_n} PORTSC1))</i> is zero in host mode.</p> <p>In Device Mode:</p> <p>1=Attached. 0=Not Attached. Default=0. A one indicates that the device successfully attached and is operating in either high speed or full speed as indicated by the High Speed Port bit in this register. A zero indicates that the device did not attach successfully or was forcibly disconnected by the software writing a zero to the Run bit in the USBCMD register. It does not state the device being disconnected or suspended.</p>

65.6.32 On-The-Go Status & control (USBC_{_n} OTGSC)

This register is available only in OTG controller core. It has four sections:

- OTG Interrupt enables (Read/Write)
- OTG Interrupt status (Read/Write to Clear)

- OTG Status inputs (Read Only)
- OTG Controls (Read/Write)

The status inputs are debounced using a 1 ms time constant. Values on the status inputs that do not persist for more than 1 ms does not cause an update of the status input register, or cause an OTG interrupt.

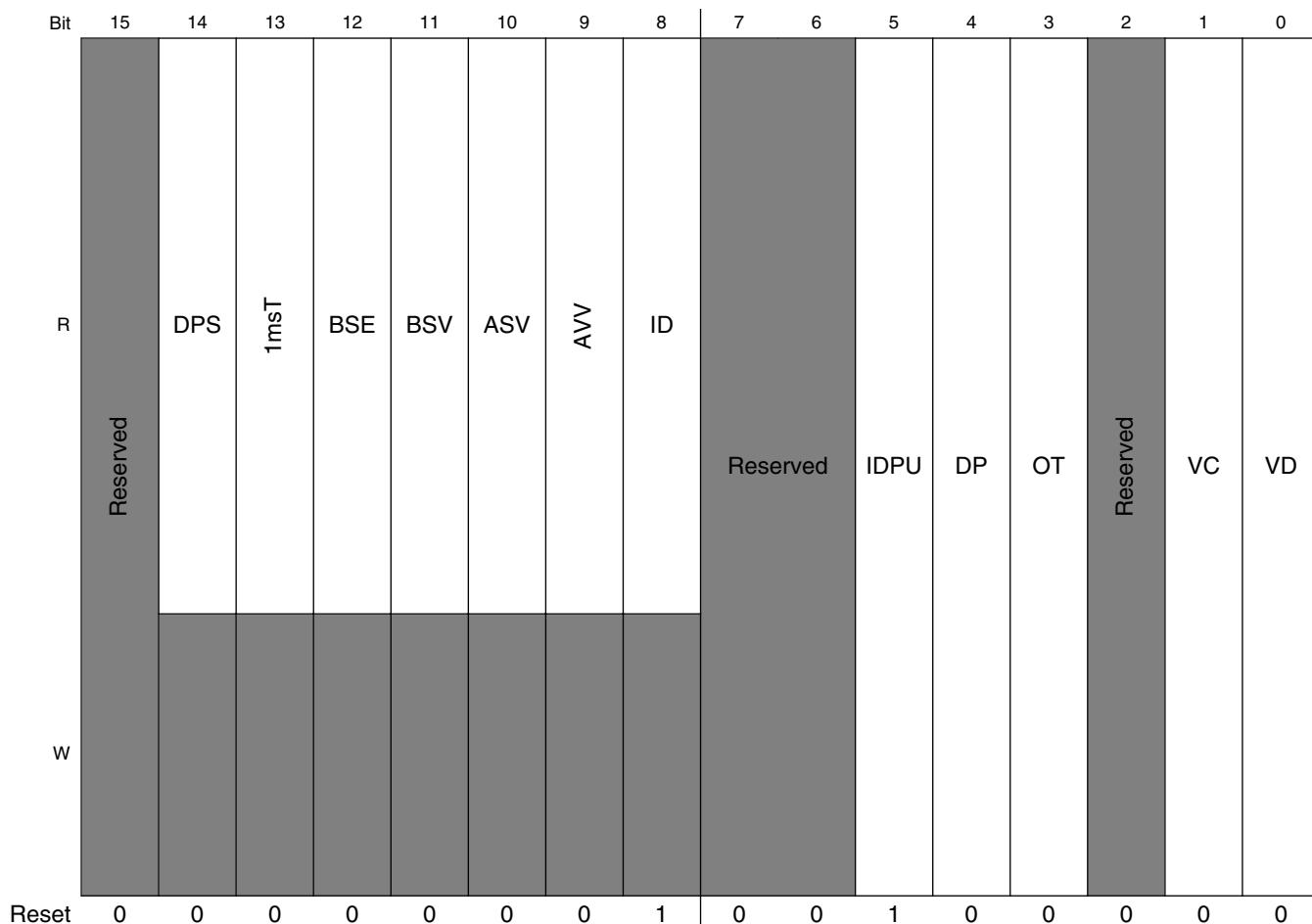
See also [USB Device Mode \(USBC_n_USBMODE\) register](#).

Address: 218_4000h base + 1A4h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved	DPIE	1msE	BSEIE	BSVIE	ASVIE	AVVIE	IDIE	Reserved	DPIS	1msS	BSEIS	BSVIS	ASVIS	AVVIS	IDIS
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

USB Core Memory Map/Register Definition



USBC_n_OTGSC field descriptions

Field	Description
31 -	This field is reserved. Reserved
30 DPIE	Data Pulse Interrupt Enable
29 1msE	1 millisecond timer Interrupt Enable - Read/Write
28 BSEIE	B Session End Interrupt Enable - Read/Write. Setting this bit enables the B session end interrupt.
27 BSVIE	B Session Valid Interrupt Enable - Read/Write. Setting this bit enables the B session valid interrupt.
26 ASVIE	A Session Valid Interrupt Enable - Read/Write. Setting this bit enables the A session valid interrupt.
25 AVVIE	A VBus Valid Interrupt Enable - Read/Write. Setting this bit enables the A VBus valid interrupt.
24 IDIE	USB ID Interrupt Enable - Read/Write. Setting this bit enables the USB ID interrupt.

Table continues on the next page...

USBC_n_OTGSC field descriptions (continued)

Field	Description
23 -	This field is reserved. Reserved
22 DPIS	Data Pulse Interrupt Status - Read/Write to Clear. This bit is set when data bus pulsing occurs on DP or DM. Data bus pulsing is only detected when USBMODE.CM = Host (11) and PORTSC1(0)[PP] = 0. Software must write a one to clear this bit.
21 1msS	1 millisecond timer Interrupt Status - Read/Write to Clear. This bit is set once every millisecond. Software must write a one to clear this bit.
20 BSEIS	B Session End Interrupt Status - Read/Write to Clear. This bit is set when VBus has fallen below the B session end threshold. Software must write a one to clear this bit
19 BSVIS	B Session Valid Interrupt Status - Read/Write to Clear. This bit is set when VBus has either risen above or fallen below the B session valid threshold. Software must write a one to clear this bit.
18 ASVIS	A Session Valid Interrupt Status - Read/Write to Clear. This bit is set when VBus has either risen above or fallen below the A session valid threshold. Software must write a one to clear this bit.
17 AVVIS	A VBus Valid Interrupt Status - Read/Write to Clear. This bit is set when VBus has either risen above or fallen below the VBus valid threshold on an A device. Software must write a one to clear this bit.
16 IDIS	USB ID Interrupt Status - Read/Write. This bit is set when a change on the ID input has been detected. Software must write a one to clear this bit.
15 -	This field is reserved. Reserved
14 DPS	Data Bus Pulsing Status - Read Only. A '1' indicates data bus pulsing is being detected on the port.
13 1msT	1 millisecond timer toggle - Read Only. This bit toggles once per millisecond.
12 BSE	B Session End - Read Only. Indicates VBus is below the B session end threshold.
11 BSV	B Session Valid - Read Only. Indicates VBus is above the B session valid threshold.
10 ASV	A Session Valid - Read Only. Indicates VBus is above the A session valid threshold.
9 AVV	A VBus Valid - Read Only. Indicates VBus is above the A VBus valid threshold.
8 ID	USB ID - Read Only.

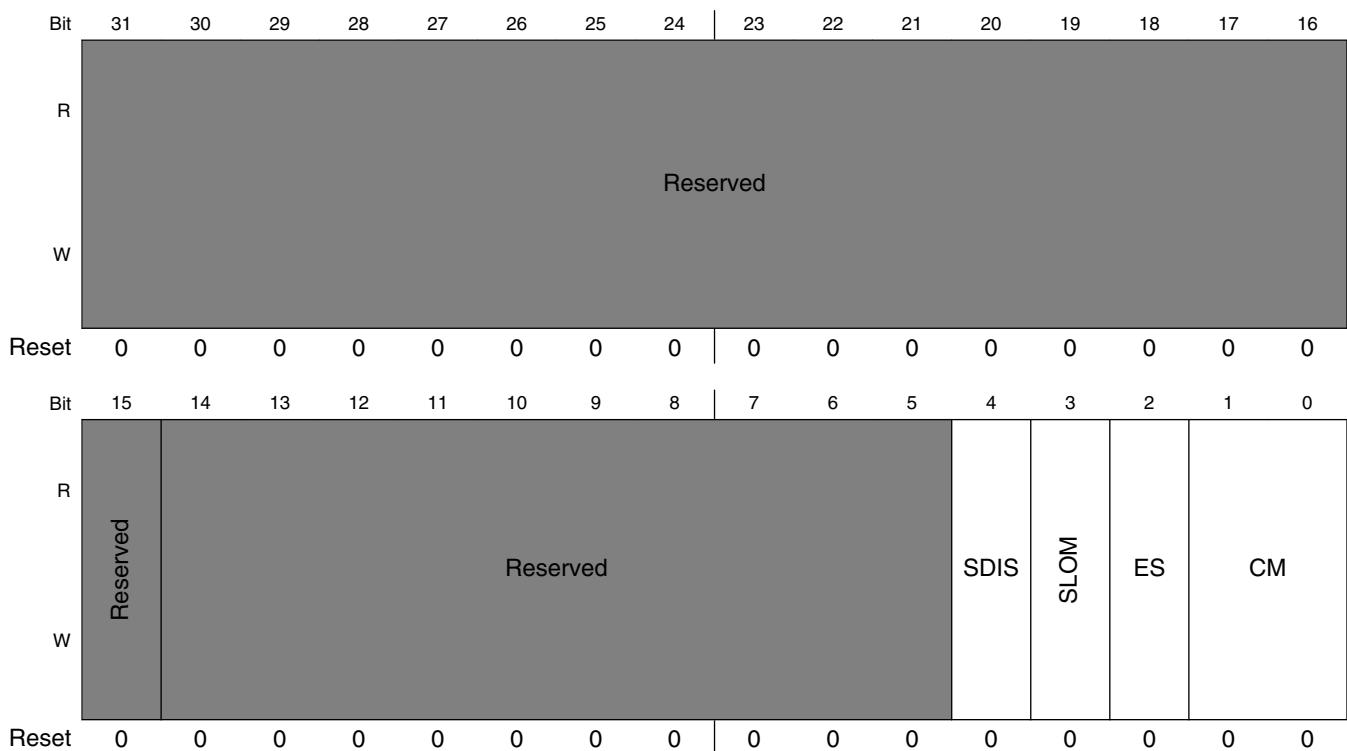
Table continues on the next page...

USBC_n_OTGSC field descriptions (continued)

Field	Description
	0 = A device, 1 = B device
7–6 -	This field is reserved. Reserved
5 IDPU	ID Pullup - Read/Write This bit provide control over the ID pull-up resister; 0 = off, 1 = on [default]. When this bit is 0, the ID input will not be sampled.
4 DP	Data Pulsing - Read/Write. Setting this bit causes the pullup on DP to be asserted for data pulsing during SRP.
3 OT	OTG Termination - Read/Write. This bit must be set when the OTG device is in device mode, this controls the pulldown on DM.
2 -	This field is reserved. Reserved
1 VC	VBUS Charge - Read/Write. Setting this bit causes the VBus line to be charged. This is used for VBus pulsing during SRP.
0 VD	VBUS_Discharge - Read/Write. Setting this bit causes VBus to discharge through a resistor.

65.6.33 USB Device Mode (USBC_n_USBMODE)

Address: 218_4000h base + 1A8h offset + (512d × i), where i=0d to 3d



USBC_n_USBMODE field descriptions

Field	Description
31–16 -	This field is reserved. Reserved
15 -	This field is reserved. Reserved
14–5 -	This field is reserved. Reserved
4 SDIS	<p>Stream Disable Mode. (0 - Inactive [default]; 1 - Active)</p> <p>Device Mode: Setting to a '1' disables double priming on both RX and TX for low bandwidth systems. This mode ensures that when the RX and TX buffers are sufficient to contain an entire packet that the standard double buffering scheme is disabled to prevent overruns/underruns in bandwidth limited systems. Note: In High Speed Mode, all packets received are responded to with a NYET handshake when stream disable is active.</p> <p>Host Mode: Setting to a '1' ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the RX and TX buffers are sufficient to contain the entire packet. Enabling stream disable also has the effect of ensuring the TX latency is filled to capacity before the packet is launched onto the USB.</p> <p>NOTE: Time duration to pre-fill the FIFO becomes significant when stream disable is active. See TX FIFO Fill Tuning (USBC_n_TXFILLTUNING) and TXTTFILLTUNING [MPH Only] to characterize the adjustments needed for the scheduler when using this feature.</p> <p>NOTE: The use of this feature substantially limits of the overall USB performance that can be achieved.</p>
3 SLOM	<p>Setup Lockout Mode. In device mode, this bit controls behavior of the setup lock mechanism. See Control Endpoint Operation Model .</p> <p>0 Setup Lockouts On (default); 1 Setup Lockouts Off (DCD requires use of Setup Data Buffer Tripwire in USB Command Register (USBC_n_USBCMD)).</p>
2 ES	<p>Endian Select - Read/Write. This bit can change the byte alignment of the transfer buffers to match the host microprocessor. The bit fields in the microprocessor interface and the data structures are unaffected by the value of this bit because they are based upon the 32-bit word.</p> <p>Bit Meaning</p> <p>0 Little Endian [Default] 1 Big Endian</p>
CM	<p>Controller Mode - R/WO. Controller mode is defaulted to the proper mode for host only and device only implementations. For those designs that contain both host & device capability, the controller defaults to an idle state and needs to be initialized to the desired operating mode after reset. For combination host/device controllers, this register can only be written once after reset. If it is necessary to switch modes, software must reset the controller by writing to the <i>RESET</i> bit in the USBCMD register before reprogramming this register.</p> <p>For OTG controller core, reset value is '00b'.</p> <p>For Host-only controller core, reset value is '11b'.</p> <p>00 Idle [Default for combination host/device] 01 Reserved 10 Device Controller [Default for device only controller] 11 Host Controller [Default for host only controller]</p>

65.6.34 Endpoint Setup Status (USBC_n_ENDPTSETUPSTAT)

Address: 218_4000h base + 1ACh offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved															ENDPTSETUPSTAT																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

USBC_n_ENDPTSETUPSTAT field descriptions

Field	Description
31–16 -	This field is reserved. Reserved
ENDPTSETUPSTAT	Setup Endpoint Status. For every setup transaction that is received, a corresponding bit in this register is set to one. Software must clear or acknowledge the setup transfer by writing a one to a respective bit after it has read the setup data from Queue head. The response to a setup packet as in the order of operations and total response time is crucial to limit bus time outs while the setup lock our mechanism is engaged. See Managing Endpoints in the Device Operational Model. This register is only used in device mode.

65.6.35 Endpoint Prime (USBC_n_ENDPTPRIME)

This register is only used in device mode.

When software sets the prime bit for a given endpoint, the device controller loads the transfer descriptor, pointed to by the queue head, such that the endpoint is ready to transmit or receive when the host sends a request (IN/OUT token). The endpoint will NAK all requests from the host until the endpoint is primed. The controller will automatically re-prime the endpoint with a new transfer descriptor when one is found via the next_dtd pointer of the current transfer descriptor. Hence, the prime bit must only be set by software when a descriptor is added to the queue head.

Address: 218_4000h base + 1B0h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved										PETB										Reserved								PERB			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

USBC_n_ENDPTPRIME field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23–16 PETB	Prime Endpoint Transmit Buffer - R/WS. For each endpoint a corresponding bit is used to request that a buffer is prepared for a transmit operation in order to respond to a USB IN/INTERRUPT transaction.

Table continues on the next page...

USBC_n_ENDPTPRIME field descriptions (continued)

Field	Description
	<p>Software should write a one to the corresponding bit when posting a new transfer descriptor to an endpoint queue head. Hardware automatically uses this bit to begin parsing for a new transfer descriptor from the queue head and prepare a transmit buffer. Hardware clears this bit when the associated endpoint(s) is (are) successfully primed.</p> <p>NOTE: These bits are momentarily set by hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated.</p> <p>PETB[N] - Endpoint #N, N is in 0..7</p>
15–8 -	This field is reserved. Reserved
PERB	<p>Prime Endpoint Receive Buffer - R/WS. For each endpoint, a corresponding bit is used to request a buffer prepare for a receive operation for when a USB host initiates a USB OUT transaction. Software should write a one to the corresponding bit whenever posting a new transfer descriptor to an endpoint queue head. Hardware automatically uses this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. Hardware clears this bit when the associated endpoint(s) is (are) successfully primed.</p> <p>NOTE: These bits are momentarily set by hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated.</p> <p>PERB[N] - Endpoint #N, N is in 0..7</p>

65.6.36 Endpoint Flush (USBC_n_ENDPTFLUSH)

This register is only used in device mode.

Address: 218_4000h base + 1B4h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved					FETB					Reserved					FERB																
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

USBC_n_ENDPTFLUSH field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23–16 FETB	Flush Endpoint Transmit Buffer - R/WS. Writing one to a bit(s) in this register causes the associated endpoint(s) to clear any primed buffers. If a packet is in progress for one of the associated endpoints, then that transfer continues until completion. Hardware clears this register after the endpoint flush operation is successful.
	FETB[N] - Endpoint #N, N is in 0..7
15–8 -	This field is reserved. Reserved

Table continues on the next page...

USBC_n_ENDPTFLUSH field descriptions (continued)

Field	Description
FERB	Flush Endpoint Receive Buffer - R/Ws. Writing one to a bit(s) causes the associated endpoint(s) to clear any primed buffers. If a packet is in progress for one of the associated endpoints, then that transfer continues until completion. Hardware clears this register after the endpoint flush operation is successful. FERB[N] - Endpoint #N, N is in 0..7

65.6.37 Endpoint Status (USBC_n_ENDPTSTAT)

This register is only used in device mode.

Address: 218_4000h base + 1B8h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved					ETBR					Reserved					ERBR																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

USBC_n_ENDPTSTAT field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23–16 ETBR	Endpoint Transmit Buffer Ready -- Read Only. One bit for each endpoint indicates status of the respective endpoint buffer. This bit is set to one by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There is always a delay between setting a bit in the ENDPTPRIME register and endpoint indicating ready. This delay time varies based upon the current USB traffic and the number of bits set in the ENDPRIME register. Buffer ready is cleared by USB reset, by the USB DMA system, or through the ENDPTFLUSH register. NOTE: These bits are momentarily cleared by hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ETBR[N] - Endpoint #N, N is in 0..7
15–8 -	This field is reserved. Reserved
ERBR	Endpoint Receive Buffer Ready -- Read Only. One bit for each endpoint indicates status of the respective endpoint buffer. This bit is set to a one by the hardware as a response to receiving a command from a corresponding bit in the ENDPRIME register. There is always a delay between setting a bit in the ENDPRIME register and endpoint indicating ready. This delay time varies based upon the current USB traffic and the number of bits set in the ENDPRIME register. Buffer ready is cleared by USB reset, by the USB DMA system, or through the ENDPTFLUSH register. NOTE: These bits are momentarily cleared by hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ERBR[N] - Endpoint #N, N is in 0..7

65.6.38 Endpoint Complete (USBC_n_ENDPTCOMPLETE)

This register is only used in device mode.

Address: 218_4000h base + 1BCh offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved								ETCE								Reserved								ERCE							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

USBC_n_ENDPTCOMPLETE field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23–16 ETCE	Endpoint Transmit Complete Event - R/WC. Each bit indicates a transmit event (IN/INTERRUPT) occurred and software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set in the Transfer Descriptor, then this bit is set simultaneously with the <i>USB/INT</i> . Writing one clears the corresponding bit in this register. ETCE[N] - Endpoint #N, N is in 0..7
15–8 -	This field is reserved. Reserved
ERCE	Endpoint Receive Complete Event - RW/C. Each bit indicates a received event (OUT/SETUP) occurred and software should read the corresponding endpoint queue to determine the transfer status. If the corresponding IOC bit is set in the Transfer Descriptor, then this bit is set simultaneously with the <i>USB/INT</i> . Writing one clears the corresponding bit in this register. ERCE[N] - Endpoint #N, N is in 0..7

65.6.39 Endpoint Control0 (USBC_n_ENDPTCTRL0)

Every Device implements Endpoint 0 as a control endpoint.

Address: 218_4000h base + 1C0h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved								TXE	Reserved			TXT	Reserved		
W														TXS		
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved								RXE	Reserved			RXT	Reserved		
W														RXS		
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

USBC_n_ENDPTCTRL0 field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23 TXE	TX Endpoint Enable 1 Enabled Endpoint0 is always enabled.
22–20 -	This field is reserved. Reserved
19–18 TXT	TX Endpoint Type - Read/Write 00 - Control Endpoint0 is fixed as a Control End Point.
17 -	This field is reserved. Reserved
16 TXS	TX Endpoint Stall - Read/Write

Table continues on the next page...

USBC_n_ENDPTCTRL0 field descriptions (continued)

Field	Description
	0 End Point OK [Default] 1 End Point Stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues returning STALL until the bit is cleared by software or it is automatically cleared upon receipt of a new SETUP request.
15–8 -	This field is reserved. Reserved
7 RXE	RX Endpoint Enable 1 Enabled Endpoint0 is always enabled.
6–4 -	This field is reserved. Reserved
3–2 RXT	RX Endpoint Type - Read/Write 00 Control Endpoint0 is fixed as a Control End Point.
1 -	This field is reserved. Reserved
0 RXS	RX Endpoint Stall - Read/Write 0 End Point OK. [Default] 1 End Point Stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues returning STALL until the bit is cleared by software or it is automatically cleared upon receipt of a new SETUP request.

65.6.40 Endpoint Control 1 (USBC_n_ENDPTCTRL1)

This is endpoint control register for endpoint 1 in device operation mode.

NOTE

If one endpoint direction is enabled and the paired endpoint of opposite direction is disabled then the unused direction type must be changed from the default control-type to any other type (that is Bulk-type). leaving an unconfigured endpoint control causes undefined behavior for the data pid tracking on the active endpoint/direction.

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Address: 218_4000h base + 1C4h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
									TXE	TXR	TXI					
W												Reserved				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
									RXE	RXR	RXI					
W												Reserved				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_ENDPTCTRL1 field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23 TXE	TX Endpoint Enable 0 Disabled [Default] 1 Enabled An Endpoint should be enabled only after it has been configured.
22 TXR	TX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the Host and device.
21 TXI	TX Data Toggle Inhibit 0 PID Sequencing Enabled. [Default] 1 PID Sequencing Disabled. This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20 -	This field is reserved. Reserved
19–18 TXT	TX Endpoint Type - Read/Write 00 Control 01 Isochronous

Table continues on the next page...

USBC_n_ENDPTCTRL1 field descriptions (continued)

Field	Description
	10 Bulk 11 Interrupt
17 TXD	TX Endpoint Data Source - Read/Write 0 Dual Port Memory Buffer/DMA Engine [DEFAULT] Should always be written as 0.
16 TXS	TX Endpoint Stall - Read/Write 0 End Point OK 1 End Point Stalled This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint. Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above. NOTE: For CONTROL type endpoint, there is a slight delay (50 clocks max) between the ENDPTSETUPSTAT begin cleared and hardware continuing to clear this bit. In most systems, it is unlikely the DCD software will observe this delay. Take care that the STALL bit is not set immediately after writing a '1' to it. Please follow this procedure: continually write this STALL bit until it is set or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15–8 -	This field is reserved. Reserved
7 RXE	RX Endpoint Enable 0 Disabled [Default] 1 Enabled An Endpoint should be enabled only after it has been configured.
6 RXR	RX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the host and device.
5 RXI	RX Data Toggle Inhibit 0 Disabled [Default] 1 Enabled This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always accept data packet regardless of their data PID.
4 -	This field is reserved. Reserved.
3–2 RXT	RX Endpoint Type - Read/Write 00 Control 01 Isochronous 10 Bulk 11 Reserved

Table continues on the next page...

USBC_n_ENDPTCTRL1 field descriptions (continued)

Field	Description
1 RXD	RX Endpoint Data Sink - Read/Write - TBD 0 Dual Port Memory Buffer/DMA Engine [Default] Should always be written as zero.
0 RXS	RX Endpoint Stall - Read/Write 0 End Point OK. [Default] 1 End Point Stalled This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt a SETUP request if this Endpoint is configured as a Control Endpoint, Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.

65.6.41 Endpoint Control 2 (USBC_n_ENDPTCTRL2)

This is endpoint control register for endpoint 2 in device operation mode.

NOTE

If one endpoint direction is enabled and the paired endpoint of opposite direction is disabled then the unused direction type must be changed from the default control-type to any other type (that is Bulk-type). leaving an unconfigured endpoint control causes undefined behavior for the data pid tracking on the active endpoint/direction.

Address: 218_4000h base + 1C8h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
									TXE	TXR	TXI		TXT	TXD	TXS	
W									0	0	0	0	0	0	0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									RXE	RXR	RXI	Reserved				
W									0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_ENDPTCTRL2 field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23 TXE	TX Endpoint Enable 0 Disabled [Default] 1 Enabled An Endpoint should be enabled only after it has been configured.
22 TXR	TX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the Host and device.
21 TXI	TX Data Toggle Inhibit 0 PID Sequencing Enabled. [Default] 1 PID Sequencing Disabled. This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20 -	This field is reserved. Reserved
19–18 TXT	TX Endpoint Type - Read/Write 00 Control 01 Isochronous 10 Bulk 11 Interrupt
17 TxD	TX Endpoint Data Source - Read/Write 0 Dual Port Memory Buffer/DMA Engine [DEFAULT] Should always be written as 0.
16 TXS	TX Endpoint Stall - Read/Write 0 End Point OK 1 End Point Stalled

Table continues on the next page...

USBC_n_ENDPTCTRL2 field descriptions (continued)

Field	Description
	<p>This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint.</p> <p>Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.</p> <p>NOTE: For CONTROL type endpoint, there is a slight delay (50 clocks max) between the ENDPTSETUPSTAT begin cleared and hardware continuing to clear this bit. In most systems, it is unlikely the DCD software will observe this delay. Take care that the STALL bit is not set immediately after writing a '1' to it. Please follow this procedure: continually write this STALL bit until it is set or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.</p>
15–8 -	This field is reserved. Reserved
7 RXE	<p>RX Endpoint Enable</p> <p>0 Disabled [Default]</p> <p>1 Enabled</p> <p>An Endpoint should be enabled only after it has been configured.</p>
6 RXR	<p>RX Data Toggle Reset (WS)</p> <p>Write 1 - Reset PID Sequence</p> <p>Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the host and device.</p>
5 RXI	<p>RX Data Toggle Inhibit</p> <p>0 Disabled [Default]</p> <p>1 Enabled</p> <p>This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always accept data packet regardless of their data PID.</p>
4 -	This field is reserved. Reserved.
3–2 RXT	<p>RX Endpoint Type - Read/Write</p> <p>00 Control</p> <p>01 Isochronous</p> <p>10 Bulk</p> <p>11 Reserved</p>
1 RXD	<p>RX Endpoint Data Sink - Read/Write - TBD</p> <p>0 Dual Port Memory Buffer/DMA Engine [Default]</p> <p>Should always be written as zero.</p>
0 RXS	<p>RX Endpoint Stall - Read/Write</p> <p>0 End Point OK. [Default]</p> <p>1 End Point Stalled</p> <p>This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt a SETUP request if this Endpoint is configured as a Control Endpoint,</p>

Table continues on the next page...

USBC_n_ENDPTCTRL2 field descriptions (continued)

Field	Description
	Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.

65.6.42 Endpoint Control 3 (USBC_n_ENDPTCTRL3)

This is endpoint control register for endpoint 3 in device operation mode.

NOTE

If one endpoint direction is enabled and the paired endpoint of opposite direction is disabled then the unused direction type must be changed from the default control-type to any other type (that is Bulk-type). leaving an unconfigured endpoint control causes undefined behavior for the data pid tracking on the active endpoint/direction.

Address: 218_4000h base + 1CCh offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved								TXE	TXR	TXI	Reserved	TXT	TXD	TXS	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved								RXE	RXR	RXI	Reserved	RXT	RXD	RXS	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_ENDPTCTRL3 field descriptions

Field	Description
31–24 -	This field is reserved. Reserved

Table continues on the next page...

USBC_n_ENDPTCTRL3 field descriptions (continued)

Field	Description
23 TXE	<p>TX Endpoint Enable</p> <p>0 Disabled [Default]</p> <p>1 Enabled</p> <p>An Endpoint should be enabled only after it has been configured.</p>
22 TXR	<p>TX Data Toggle Reset (WS)</p> <p>Write 1 - Reset PID Sequence</p> <p>Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the Host and device.</p>
21 TXI	<p>TX Data Toggle Inhibit</p> <p>0 PID Sequencing Enabled. [Default]</p> <p>1 PID Sequencing Disabled.</p> <p>This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.</p>
20 -	This field is reserved. Reserved
19–18 TXT	<p>TX Endpoint Type - Read/Write</p> <p>00 Control</p> <p>01 Isochronous</p> <p>10 Bulk</p> <p>11 Interrupt</p>
17 TXD	<p>TX Endpoint Data Source - Read/Write</p> <p>0 Dual Port Memory Buffer/DMA Engine [DEFAULT]</p> <p>Should always be written as 0.</p>
16 TXS	<p>TX Endpoint Stall - Read/Write</p> <p>0 End Point OK</p> <p>1 End Point Stalled</p> <p>This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint.</p> <p>Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.</p> <p>NOTE: For CONTROL type endpoint, there is a slight delay (50 clocks max) between the ENDPTSETUPSTAT begin cleared and hardware continuing to clear this bit. In most systems, it is unlikely the DCD software will observe this delay. Take care that the STALL bit is not set immediately after writing a '1' to it. Please follow this procedure: continually write this STALL bit until it is set or until a new setup has ben received by checking the associated ENDPTSETUPSTAT bit.</p>
15–8 -	This field is reserved. Reserved
7 RXE	RX Endpoint Enable
	0 Disabled [Default]

Table continues on the next page...

USBC_n_ENDPTCTRL3 field descriptions (continued)

Field	Description
	1 Enabled An Endpoint should be enabled only after it has been configured.
6 RXR	RX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the host and device.
5 RXI	RX Data Toggle Inhibit 0 Disabled [Default] 1 Enabled This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always accept data packet regardless of their data PID.
4 -	This field is reserved. Reserved.
3–2 RXT	RX Endpoint Type - Read/Write 00 Control 01 Isochronous 10 Bulk 11 Reserved
1 RXD	RX Endpoint Data Sink - Read/Write - TBD 0 Dual Port Memory Buffer/DMA Engine [Default] Should always be written as zero.
0 RXS	RX Endpoint Stall - Read/Write 0 End Point OK. [Default] 1 End Point Stalled This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt a SETUP request if this Endpoint is configured as a Control Endpoint, Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.

65.6.43 Endpoint Control 4 (USBC_n_ENDPTCTRL4)

This is endpoint control register for endpoint 4 in device operation mode.

NOTE

If one endpoint direction is enabled and the paired endpoint of opposite direction is disabled then the unused direction type must be changed from the default control-type to any other type (that is Bulk-type). leaving an unconfigured endpoint control

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causes undefined behavior for the data pid tracking on the active endpoint/direction.

Address: 218_4000h base + 1D0h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
									TXE	TXR	TXI					
W												Reserved				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									RXE	RXR	RXI					
												Reserved				
W													RXT	RXD	RXS	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_ENDPTCTRL4 field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23 TXE	TX Endpoint Enable 0 Disabled [Default] 1 Enabled An Endpoint should be enabled only after it has been configured.
22 TXR	TX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the Host and device.
21 TXI	TX Data Toggle Inhibit 0 PID Sequencing Enabled. [Default] 1 PID Sequencing Disabled. This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20 -	This field is reserved. Reserved

Table continues on the next page...

USBC_n_ENDPTCTRL4 field descriptions (continued)

Field	Description
19–18 TXT	TX Endpoint Type - Read/Write 00 Control 01 Isochronous 10 Bulk 11 Interrupt
17 TXD	TX Endpoint Data Source - Read/Write 0 Dual Port Memory Buffer/DMA Engine [DEFAULT] Should always be written as 0.
16 TXS	TX Endpoint Stall - Read/Write 0 End Point OK 1 End Point Stalled This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint. Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above. NOTE: For CONTROL type endpoint, there is a slight delay (50 clocks max) between the ENDPTSETUPSTAT begin cleared and hardware continuing to clear this bit. In most systems, it is unlikely the DCD software will observe this delay. Take care that the STALL bit is not set immediately after writing a '1' to it. Please follow this procedure: continually write this STALL bit until it is set or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15–8 -	This field is reserved. Reserved
7 RXE	RX Endpoint Enable 0 Disabled [Default] 1 Enabled An Endpoint should be enabled only after it has been configured.
6 RXR	RX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the host and device.
5 RXI	RX Data Toggle Inhibit 0 Disabled [Default] 1 Enabled This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always accept data packet regardless of their data PID.
4 -	This field is reserved. Reserved.
3–2 RXT	RX Endpoint Type - Read/Write 00 Control

Table continues on the next page...

USBC_{_n}_ENDPTCTRL4 field descriptions (continued)

Field	Description
	01 Isochronous 10 Bulk 11 Reserved
1 RXD	RX Endpoint Data Sink - Read/Write - TBD 0 Dual Port Memory Buffer/DMA Engine [Default] Should always be written as zero.
0 RXS	RX Endpoint Stall - Read/Write 0 End Point OK. [Default] 1 End Point Stalled This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt a SETUP request if this Endpoint is configured as a Control Endpoint, Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.

65.6.44 Endpoint Control 5 (USBC_{_n}_ENDPTCTRL5)

This is endpoint control register for endpoint 5 in device operation mode.

NOTE

If one endpoint direction is enabled and the paired endpoint of opposite direction is disabled then the unused direction type must be changed from the default control-type to any other type (that is Bulk-type). leaving an unconfigured endpoint control causes undefined behavior for the data pid tracking on the active endpoint/direction.

Address: 218_4000h base + 1D4h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved

TXE TXR TXI Reserved Reserved TXT TXD TXS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									RXE	RXR	RXI	Reserved				
W									0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_ENDPTCTRL5 field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23 TXE	TX Endpoint Enable 0 Disabled [Default] 1 Enabled An Endpoint should be enabled only after it has been configured.
22 TXR	TX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the Host and device.
21 TXI	TX Data Toggle Inhibit 0 PID Sequencing Enabled. [Default] 1 PID Sequencing Disabled. This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20 -	This field is reserved. Reserved
19–18 TXT	TX Endpoint Type - Read/Write 00 Control 01 Isochronous 10 Bulk 11 Interrupt
17 TxD	TX Endpoint Data Source - Read/Write 0 Dual Port Memory Buffer/DMA Engine [DEFAULT] Should always be written as 0.
16 TXS	TX Endpoint Stall - Read/Write 0 End Point OK 1 End Point Stalled

Table continues on the next page...

USBC_n_ENDPTCTRL5 field descriptions (continued)

Field	Description
	<p>This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint.</p> <p>Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.</p> <p>NOTE: For CONTROL type endpoint, there is a slight delay (50 clocks max) between the ENDPTSETUPSTAT begin cleared and hardware continuing to clear this bit. In most systems, it is unlikely the DCD software will observe this delay. Take care that the STALL bit is not set immediately after writing a '1' to it. Please follow this procedure: continually write this STALL bit until it is set or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.</p>
15–8 -	This field is reserved. Reserved
7 RXE	<p>RX Endpoint Enable</p> <p>0 Disabled [Default]</p> <p>1 Enabled</p> <p>An Endpoint should be enabled only after it has been configured.</p>
6 RXR	<p>RX Data Toggle Reset (WS)</p> <p>Write 1 - Reset PID Sequence</p> <p>Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the host and device.</p>
5 RXI	<p>RX Data Toggle Inhibit</p> <p>0 Disabled [Default]</p> <p>1 Enabled</p> <p>This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always accept data packet regardless of their data PID.</p>
4 -	This field is reserved. Reserved.
3–2 RXT	<p>RX Endpoint Type - Read/Write</p> <p>00 Control</p> <p>01 Isochronous</p> <p>10 Bulk</p> <p>11 Reserved</p>
1 RXD	<p>RX Endpoint Data Sink - Read/Write - TBD</p> <p>0 Dual Port Memory Buffer/DMA Engine [Default]</p> <p>Should always be written as zero.</p>
0 RXS	<p>RX Endpoint Stall - Read/Write</p> <p>0 End Point OK. [Default]</p> <p>1 End Point Stalled</p> <p>This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt a SETUP request if this Endpoint is configured as a Control Endpoint,</p>

Table continues on the next page...

USBC_n_ENDPTCTRL5 field descriptions (continued)

Field	Description
	Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.

65.6.45 Endpoint Control 6 (USBC_n_ENDPTCTRL6)

This is endpoint control register for endpoint 6 in device operation mode.

NOTE

If one endpoint direction is enabled and the paired endpoint of opposite direction is disabled then the unused direction type must be changed from the default control-type to any other type (that is Bulk-type). leaving an unconfigured endpoint control causes undefined behavior for the data pid tracking on the active endpoint/direction.

Address: 218_4000h base + 1D8h offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved								TXE	TXR	TXI	Reserved	TXT	TXD	TXS	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved								RXE	RXR	RXI	Reserved	RXT	RXD	RXS	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_ENDPTCTRL6 field descriptions

Field	Description
31–24 -	This field is reserved. Reserved

Table continues on the next page...

USBC_n_ENDPTCTRL6 field descriptions (continued)

Field	Description
23 TXE	<p>TX Endpoint Enable</p> <p>0 Disabled [Default]</p> <p>1 Enabled</p> <p>An Endpoint should be enabled only after it has been configured.</p>
22 TXR	<p>TX Data Toggle Reset (WS)</p> <p>Write 1 - Reset PID Sequence</p> <p>Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the Host and device.</p>
21 TXI	<p>TX Data Toggle Inhibit</p> <p>0 PID Sequencing Enabled. [Default]</p> <p>1 PID Sequencing Disabled.</p> <p>This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.</p>
20 -	This field is reserved. Reserved
19–18 TXT	<p>TX Endpoint Type - Read/Write</p> <p>00 Control</p> <p>01 Isochronous</p> <p>10 Bulk</p> <p>11 Interrupt</p>
17 TXD	<p>TX Endpoint Data Source - Read/Write</p> <p>0 Dual Port Memory Buffer/DMA Engine [DEFAULT]</p> <p>Should always be written as 0.</p>
16 TXS	<p>TX Endpoint Stall - Read/Write</p> <p>0 End Point OK</p> <p>1 End Point Stalled</p> <p>This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint.</p> <p>Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.</p> <p>NOTE: For CONTROL type endpoint, there is a slight delay (50 clocks max) between the ENDPTSETUPSTAT begin cleared and hardware continuing to clear this bit. In most systems, it is unlikely the DCD software will observe this delay. Take care that the STALL bit is not set immediately after writing a '1' to it. Please follow this procedure: continually write this STALL bit until it is set or until a new setup has ben received by checking the associated ENDPTSETUPSTAT bit.</p>
15–8 -	This field is reserved. Reserved
7 RXE	RX Endpoint Enable
	0 Disabled [Default]

Table continues on the next page...

USBC_n_ENDPTCTRL6 field descriptions (continued)

Field	Description
	1 Enabled An Endpoint should be enabled only after it has been configured.
6 RXR	RX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the host and device.
5 RXI	RX Data Toggle Inhibit 0 Disabled [Default] 1 Enabled This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always accept data packet regardless of their data PID.
4 -	This field is reserved. Reserved.
3–2 RXT	RX Endpoint Type - Read/Write 00 Control 01 Isochronous 10 Bulk 11 Reserved
1 RXD	RX Endpoint Data Sink - Read/Write - TBD 0 Dual Port Memory Buffer/DMA Engine [Default] Should always be written as zero.
0 RXS	RX Endpoint Stall - Read/Write 0 End Point OK. [Default] 1 End Point Stalled This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt a SETUP request if this Endpoint is configured as a Control Endpoint, Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.

65.6.46 Endpoint Control 7 (USBC_n_ENDPTCTRL7)

This is endpoint control register for endpoint 7 in device operation mode.

NOTE

If one endpoint direction is enabled and the paired endpoint of opposite direction is disabled then the unused direction type must be changed from the default control-type to any other type (that is Bulk-type). leaving an unconfigured endpoint control

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causes undefined behavior for the data pid tracking on the active endpoint/direction.

Address: 218_4000h base + 1DCh offset + (512d × i), where i=0d to 0d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved								TXE	TXR	TXI	Reserved		TXT	TXD	TXS
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved								RXE	RXR	RXI	Reserved		RXT	RXD	RXS
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBC_n_ENDPTCTRL7 field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23 TXE	TX Endpoint Enable 0 Disabled [Default] 1 Enabled An Endpoint should be enabled only after it has been configured.
22 TXR	TX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the Host and device.
21 TXI	TX Data Toggle Inhibit 0 PID Sequencing Enabled. [Default] 1 PID Sequencing Disabled. This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20 -	This field is reserved. Reserved

Table continues on the next page...

USBC_n_ENDPTCTRL7 field descriptions (continued)

Field	Description
19–18 TXT	TX Endpoint Type - Read/Write 00 Control 01 Isochronous 10 Bulk 11 Interrupt
17 TXD	TX Endpoint Data Source - Read/Write 0 Dual Port Memory Buffer/DMA Engine [DEFAULT] Should always be written as 0.
16 TXS	TX Endpoint Stall - Read/Write 0 End Point OK 1 End Point Stalled This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint. Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above. NOTE: For CONTROL type endpoint, there is a slight delay (50 clocks max) between the ENDPTSETUPSTAT begin cleared and hardware continuing to clear this bit. In most systems, it is unlikely the DCD software will observe this delay. Take care that the STALL bit is not set immediately after writing a '1' to it. Please follow this procedure: continually write this STALL bit until it is set or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15–8 -	This field is reserved. Reserved
7 RXE	RX Endpoint Enable 0 Disabled [Default] 1 Enabled An Endpoint should be enabled only after it has been configured.
6 RXR	RX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the host and device.
5 RXI	RX Data Toggle Inhibit 0 Disabled [Default] 1 Enabled This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always accept data packet regardless of their data PID.
4 -	This field is reserved. Reserved.
3–2 RXT	RX Endpoint Type - Read/Write 00 Control

Table continues on the next page...

USBC_n_ENDPTCTRL7 field descriptions (continued)

Field	Description
	01 Isochronous 10 Bulk 11 Reserved
1 RXD	RX Endpoint Data Sink - Read/Write - TBD 0 Dual Port Memory Buffer/DMA Engine [Default] Should always be written as zero.
0 RXS	RX Endpoint Stall - Read/Write 0 End Point OK. [Default] 1 End Point Stalled This bit is set automatically upon receipt of a SETUP request if this Endpoint is not configured as a Control Endpoint. It is cleared automatically upon receipt a SETUP request if this Endpoint is configured as a Control Endpoint, Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It continues to returning STALL until this bit is either cleared by software or automatically cleared as above.