

68.3.4 Double buffering

All configuration registers (all registers excluding IVDOAE, VDOAIS, VDOAST, and VDOATD) are double buffered. This means that on start, their content is copied to internal registers.

Writing new settings to VDOA's configuration registers will affect the following transfer.

68.4 VDOA Memory Map/Register Definition

VDOA memory map

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|-----------------------------------------------------------------------|-----------------|--------|-------------|------------------------------|
| 21E_4000 | VDOA Control Register (VDOA_VDOAC) | 32 | R/W | 0000_0000h | 68.4.1/5694 |
| 21E_4004 | VDOA Start and Reset (VDOA_VDOASRR) | 32 | R/W | 0000_0000h | 68.4.2/5695 |
| 21E_4008 | VDOA Interrupt Enable Register (VDOA_VDOAIE) | 32 | R/W | 0000_0000h | 68.4.3/5696 |
| 21E_400C | VDOA Interrupt Status Register (VDOA_VDOAIST) | 32 | w1c | 0000_0000h | 68.4.4/5696 |
| 21E_4010 | VDOA Frame Parameters Register (VDOA_VDOAFP) | 32 | R/W | 0000_0000h | 68.4.5/5697 |
| 21E_4014 | VDOA IPU External Buffer 0 Frame 0 Address Register (VDOA_VDOAIEBA00) | 32 | R/W | 0000_0000h | 68.4.6/5697 |
| 21E_4018 | VDOA IPU External Buffer 0 Frame 1 Address Register (VDOA_VDOAIEBA01) | 32 | R/W | 0000_0000h | 68.4.7/5698 |
| 21E_401C | VDOA IPU External Buffer 0 Frame 2 Address Register (VDOA_VDOAIEBA02) | 32 | R/W | 0000_0000h | 68.4.8/5698 |
| 21E_4020 | VDOA IPU External Buffer 1 Frame 0 Address Register (VDOA_VDOAIEBA10) | 32 | R/W | 0000_0000h | 68.4.9/5698 |
| 21E_4024 | VDOA IPU External Buffer 1 Frame 1 Address Register (VDOA_VDOAIEBA11) | 32 | R/W | 0000_0000h | 68.4.10/5699 |
| 21E_4028 | VDOA IPU External Buffer 1 Frame 2 Address Register (VDOA_VDOAIEBA12) | 32 | R/W | 0000_0000h | 68.4.11/5699 |
| 21E_402C | VDOA IPU Stride Line Register (VDOA_VDOASL) | 32 | R/W | 0000_0000h | 68.4.12/5700 |
| 21E_4030 | VDOA IPU U (Chroma) Buffer Offset Register (VDOA_VDOAIUBO) | 32 | R/W | 0000_0000h | 68.4.13/5700 |
| 21E_4034 | VDOA VPU External Buffer 0 Address Register (VDOA_VDOAVEBA0) | 32 | R/W | 0000_0000h | 68.4.14/5701 |
| 21E_4038 | VDOA VPU External Buffer 1 Address Register (VDOA_VDOAVEBA1) | 32 | R/W | 0000_0000h | 68.4.15/5701 |
| 21E_403C | VDOA VPU External Buffer 2 Address Register (VDOA_VDOAVEBA2) | 32 | R/W | 0000_0000h | 68.4.16/5701 |
| 21E_4040 | VDOA VPU U (Chroma) Buffer Offset Register (VDOA_VDOAVUBO) | 32 | R/W | 0000_0000h | 68.4.17/5702 |
| 21E_4044 | VDOA Status Register (VDOA_VDOASR) | 32 | R | 0000_0000h | 68.4.18/5703 |

68.4.1 VDOA Control Register (VDOA_VDOAC)

Address: 21E_4000h base + 0h offset = 21E_4000h

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|------|-----|----|------|----|------|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | ISEL | PFS | SO | SYNC | NF | BNDM | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAC field descriptions

| Field | Description |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31–7 Reserved | This read-only field is reserved and always has the value 0. |
| 6 ISEL | IPU SELECT - determines in sync mode which of the two sets of hand shake pins is used 0 vdoa_buf_rdy_and_ipu_buf_eob_0 — Use vdoa_buf_rdy[0] and ipu_buf_eob[0] 1 vdoa_buf_rdy_and_ipu_buf_eob_1 — Use vdoa_buf_rdy[1] and ipu_buf_eob[1] |
| 5 PFS | Pixel Format Select - Pixel format of data written to / read from IPU. Note Data from VPU is always assumed to have partial interleaved 4:2:0 format 0 4_2_0 — partially interleaved 4:2:0 1 4_2_2 — interleaved 4:2:2 Y1U1Y2V1 |
| 4 SO | Scan Order 0 PROGRESSIVE — Scan order is progressive 1 INTERLACED — Scan order is interlaced |
| 3 SYNC | SYNC MODE - defines whether the VDOA will transfer a full frame (or 2 frames) continuously or will transfer a band at a time and wait for IPU signal to continue 0 NO_SYNC_MODE — None SYNC mode (default) 1 SYNC_MODE — Sync mode |
| 2 NF | Number of frames - Determines whether to transfer 1 frame or three frames 0 1_FRAME — One frame (default) 1 3_FRAMES — Three frames |
| BNDM | BNDM Band Size 00 BAND_HEIGHT_8 — Band height = 8 lines.- Supported only for interlaced scan (SO=1) 01 BAND_HEIGHT_16 — Band height = 16 lines. |

Table continues on the next page...

VDOA_VDOAC field descriptions (continued)

| Field | Description |
|-------|-------------------------------------------------|
| 10 | BAND_HEIGHT_32 — Band height = 32 lines. |
| 11 | reserved |

68.4.2 VDOA Start and Reset (VDOA_VDOASRR)

Address: 21E_4000h base + 4h offset = 21E_4004h

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|-------|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | Start | SWRST |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOASRR field descriptions

| Field | Description |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| 1 Start | Start Transfer - Start a VDOA data transfer according to all parameters. Note: During run this bit is read only In IDLE - 0 Ignored 1 START_TRANSFER — Start a new transfer All registers we copied internally so any write to them will take place only in next transfer (double buffer) |
| 0 SWRST | Software reset - Finish outstanding AXI transfer and reset all internal registers the configuration registers are mnot cleared |

68.4.3 VDOA Interrupt Enable Register (VDOA_VDOAIE)

Address: 21E_4000h base + 8h offset = 21E_4008h

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|-------|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | EITERR | EIEOT |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAIE field descriptions

| Field | Description |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| 1 EITERR | EITERR - Enable Interrupt Transfer access Error - Enables Interrupt on AXI access Error 0 IRQ_DISABLED — interrupt disable (default) 1 IRQ_ENABLED — Interrupt Enabled |
| 0 EIEOT | EIEOT - Enable Interrupt End Of Transfer- Enables Interrupt on end of transfer 0 IRQ_DISABLED — interrupt disable (default) 1 IRQ_ENABLED — Interrupt Enabled |

68.4.4 VDOA Interrupt Status Register (VDOA_VDOAIST)

Address: 21E_4000h base + Ch offset = 21E_400Ch

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | TERR | EOT |
| W | | | | | | | | | | | | | | | w1c | w1c |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAIST field descriptions

| Field | Description |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| 1 TERR | Axi Access had an access error see ERRW bit in 0XBASE_0044 (VDOASR) for type of access (read write) if EITERR is set an interrupt will be generated |
| 0 EOT | End Of transfer - Transfer was completed if EIEOT is set an interrupt will be generated |

68.4.5 VDOA Frame Parameters Register (VDOA_VDOAFP)

Address: 21E_4000h base + 10h offset = 21E_4010h

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAFP field descriptions

| Field | Description |
|-------------------|----------------------------------------------------------------------------------------------------------|
| 31–29 Reserved | This read-only field is reserved and always has the value 0. |
| 28–16 FH | Number of pixels in one column, of the frame. Note the 3 LSB are RO and will always be 0 (multiply of 8) |
| 15–14 Reserved | This read-only field is reserved and always has the value 0. |
| FW | Number of pixels in one row, of the frame. Note the 3 LSB are RO and will always be 0 (multiply of 8) |

68.4.6 VDOA IPU External Buffer 0 Frame 0 Address Register (VDOA_VDOAIEBA00)

Address: 21E_4000h base + 14h offset = 21E_4014h

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAIEBA00 field descriptions

| Field | Description |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------|
| IEBA00 | External Address of Frame 0 output (IPU) buffer 0 - Note that the 3 LSB are always 0 (aligned to 8 address) Used for all transfer types |

68.4.7 VDOA IPU External Buffer 0 Frame 1 Address Register (VDOA_VDOAIEBA01)

Address: 21E_4000h base + 18h offset = 21E_4018h

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAIEBA01 field descriptions

| Field | Description |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IEBA01 | External Address of Frame 1 output (IPU) buffer 0 - Note that the 3 LSB are always 0 (aligned to 8 address) Used when transferring 3 frames (NF=1) only |

68.4.8 VDOA IPU External Buffer 0 Frame 2 Address Register (VDOA_VDOAIEBA02)

Address: 21E_4000h base + 1Ch offset = 21E_401Ch

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAIEBA02 field descriptions

| Field | Description |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IEBA02 | External Address of Frame 2 output (IPU) buffer 0 - Note that the 3 LSB are always 0 (aligned to 8 address) Used when transferring 3 frames (NF=1) only |

68.4.9 VDOA IPU External Buffer 1 Frame 0 Address Register (VDOA_VDOAIEBA10)

Address: 21E_4000h base + 20h offset = 21E_4020h

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAIEBA10 field descriptions

| Field | Description |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------|
| IEBA10 | External Address of Frame 0 output (IPU) buffer 1 - Note that the 3 LSB are always 0 (aligned to 8 address) Used in sync mode (SYNC=1) only |

68.4.10 VDOA IPU External Buffer 1 Frame 1 Address Register (VDOA_VDOAIEBA11)

Address: 21E_4000h base + 24h offset = 21E_4024h

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAIEBA11 field descriptions

| Field | Description |
|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IEBA11 | External Address of Frame 1 output (IPU) buffer 1 - Note that the 3 LSB are always 0 (aligned to 8 address) This register is used only in sync mode (SYNC=1), 3 frames transfer (NF=1) |

68.4.11 VDOA IPU External Buffer 1 Frame 2 Address Register (VDOA_VDOAIEBA12)

Address: 21E_4000h base + 28h offset = 21E_4028h

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAIEBA12 field descriptions

| Field | Description |
|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IEBA12 | External Address of Frame 2 output (IPU) buffer 1 - Note that the 3 LSB are always 0 (aligned to 8 address) This register is used only in sync mode (SYNC=1), 3 frames transfer (NF=1) |

68.4.12 VDOA IPU Stride Line Register (VDOA_VDOASL)

Address: 21E_4000h base + 2Ch offset = 21E_402Ch

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOASL field descriptions

| Field | Description |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31–30 Reserved | This read-only field is reserved and always has the value 0. |
| 29–16 VSLY | VPU Stride Line - Address vertical scaling factor in bytes for memory access. Also number of maximum bytes in the "Y" component row according to memory limitations. |
| 15 Reserved | This read-only field is reserved and always has the value 0. |
| ISLY | IPU Stride Line - Address vertical scaling factor in bytes for memory access; also number of maximum bytes in the "Y" component row. - Note for 4:2:2 format ISLY will be doubled since each pixel consists of two bytes. |

68.4.13 VDOA IPU U (Chroma) Buffer Offset Register (VDOA_VDOAIUBO)

Address: 21E_4000h base + 30h offset = 21E_4030h

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | IUBO | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

VDOA_VDOAIUBO field descriptions

| Field | Description |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31–27 Reserved | This read-only field is reserved and always has the value 0. |
| IUBO | The offset of Chroma (UV) Buffer for all IPU output frames i.e Buffer Chroma address will be VDOAIEBAnm+VDOAIUBO - Note that the 3 LSB are always 0 (aligned to 8 address). This parameter is used only for PFL = 4:2:0 |

68.4.14 VDOA VPU External Buffer 0 Address Register (VDOA_VDOAVEBA0)

Address: 21E_4000h base + 34h offset = 21E_4034h

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | VEBA0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAVEBA0 field descriptions

| Field | Description |
|-------|--------------------------------------------------------------------------------------------------------------------|
| VEBA0 | Address of Frame 0 VPU buffers - Note that the 3 LSB are always 0 (aligned to 8 address) Used for all transfers |

68.4.15 VDOA VPU External Buffer 1 Address Register (VDOA_VDOAVEBA1)

Address: 21E_4000h base + 38h offset = 21E_4038h

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | VEBA1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAVEBA1 field descriptions

| Field | Description |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------|
| VEBA1 | Address of Frame 1 VPU buffers - Note that the 3 LSB are always 0 (aligned to 8 address) Used when transferring three frame (NF=1) only |

68.4.16 VDOA VPU External Buffer 2 Address Register (VDOA_VDOAVEBA2)

Address: 21E_4000h base + 3Ch offset = 21E_403Ch

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | VEBA2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VDOA_VDOAVEBA2 field descriptions

| Field | Description |
|-------|------------------------------------------------------------------------------------------|
| VEBA2 | Address of Frame 2 VPU buffers - Note that the 3 LSB are always 0 (aligned to 8 address) |

VDOA_VDOAVEBA2 field descriptions (continued)

| Field | Description |
|-------|------------------------------------------------|
| | Used when transferring three frame (NF=1) only |

68.4.17 VDOA VPU U (Chroma) Buffer Offset Register (VDOA_VDOAVUBO)

Address: 21E_4000h base + 40h offset = 21E_4040h

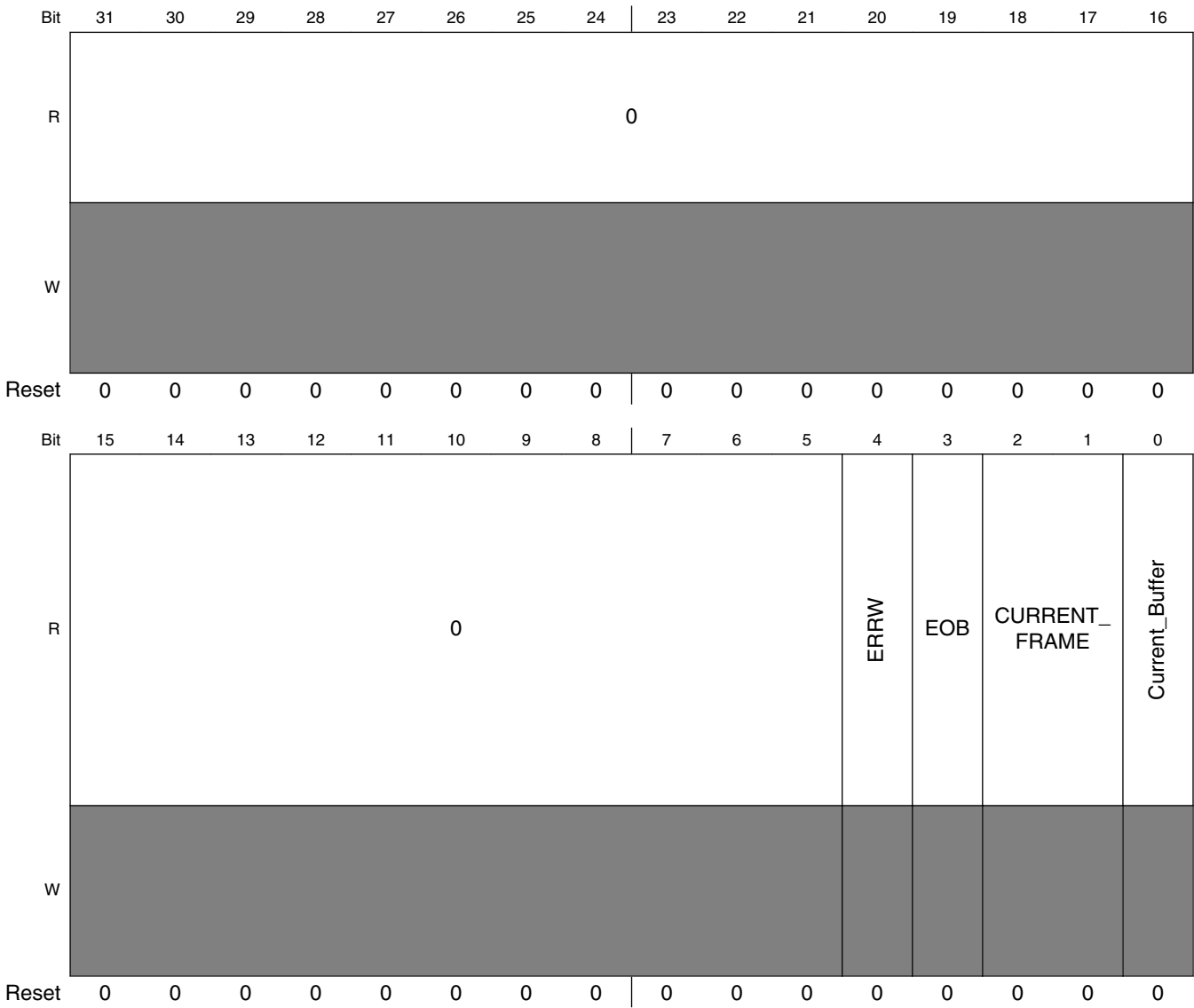
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | VUBO | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

VDOA_VDOAVUBO field descriptions

| Field | Description |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31–27 Reserved | This read-only field is reserved and always has the value 0. |
| VUBO | The offset of Chroma (UV) Buffer for all VPU input frames i.e Chroma Buffer address will be VDOAVEBAm+VDOAVUBO - Note that the 3 LSB are always 0 (aligned to 8 address) |

68.4.18 VDOA Status Register (VDOA_VDOASR)

Address: 21E_4000h base + 44h offset = 21E_4044h



VDOA_VDOASR field descriptions

| Field | Description |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 ERRW | Error Write - Indicates that the last access that failed was a read or a write.This field is valid only when TERR bit is set in VDOA Interrupt Status Register - VDOAIST 0 READ_ERROR — Read Error 1 WRITE_ERROR — Write Error |

Table continues on the next page...

VDOA_VDOASR field descriptions (continued)

| Field | Description |
|--------------------------|------------------------------------------------------------------------------------------------------------------------|
| 3 EOB | End of Band- Indicates that the VDOA has finished transferring a band in SYNC mode and is waiting for IPU to continue. |
| 2-1 CURRENT_ FRAME | Current Frame - When working on 3 frames the index of the frame currently transferred |
| 0 Current_Buffer | Current Buffer - for Double buffer shows the index of the buffer currently transferred |