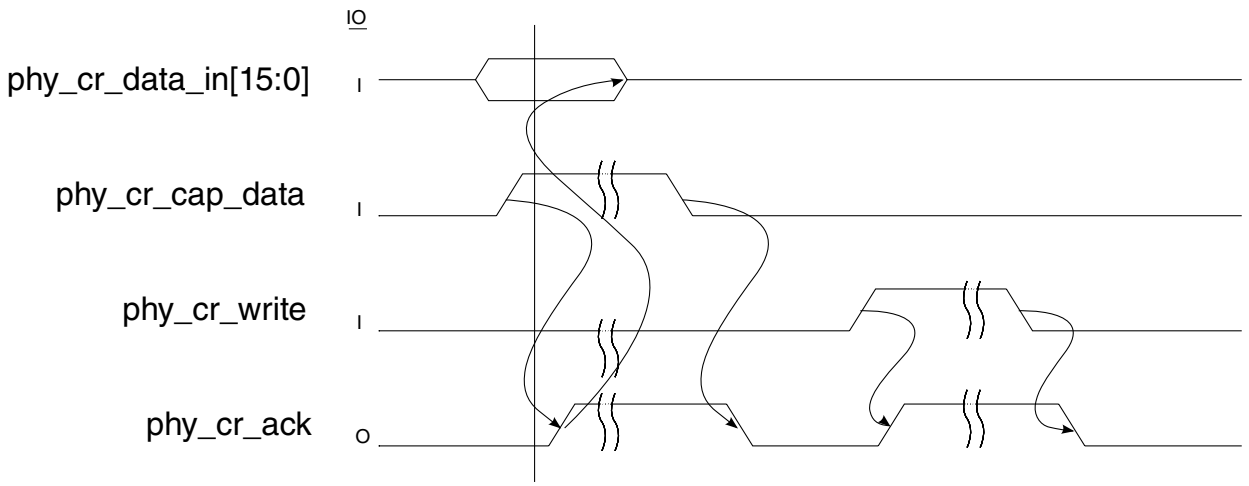


Figure 49-3. CR Bus Write Transaction

NOTE

In all cases, phy_cr_ack will de-assert when the command (phy_cr_cap_addr, phy_cr_cap_data, phy_cr_read, cr_write) is removed.

If the Control Register port is not going to be used, tie the input signals as follows,

- phy_cr_cap_addr =1'b0
- phy_cr_cap_data =1'b0
- phy_cr_data_in = 16'b0
- phy_cr_read = 1'b0
- phy_cr_write = 1'b0
- No connect (leave floating) the following:
- phy_cr_data_out[15:0]
- phy_cr_ack.

49.5 Control Memory Map/Register Definition

NOTE

PCIe PHY registers are only accessible by the corresponding controller (PCIE_PHY_CTRL_R and PCIE_PHY_STS_R) or in debug through the JTAG port. PCIe PHY is not memory mapped to processor address space, so the absolute addresses shown is the relative address and is not valid.

PCIE_PHY memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	Register ID Low 16 bits (PCIE_PHY_IDCODE_LO)	16	R	0000h	49.5.1/4377
1	Register ID High 16 bits (PCIE_PHY_IDCODE_HI)	16	R	0000h	49.5.2/4377
2	Debug Register (PCIE_PHY_DEBUG)	16	R/W	000Ah	49.5.3/4378
3	Debug Register (PCIE_PHY_RTUNE_DEBUG)	16	R/W	0000h	49.5.4/4378
4	PCIE_PHY_RTUNE_STAT	16	R/W	0000h	49.5.5/4379
5	PCIE_PHY_SS_PHASE	16	R/W	0000h	49.5.6/4379
6	PCIE_PHY_SS_FREQ	16	R/W	3327h	49.5.7/4380
10	PCIE_PHY_ATEOVRD	16	R/W	0000h	49.5.8/4380
11	PCIE_PHY_MPLL_OVRD_IN_LO	16	R/W	004Ch	49.5.9/4381
11	PCIE_PHY_MPLL_OVRD_IN_HI	16	R/W	004Ch	49.5.10/ 4382
13	PCIE_PHY_SSC_OVRD_IN	16	R/W	0000h	49.5.11/ 4383
14	PCIE_PHY_BS_OVRD_IN	16	R/W	0000h	49.5.12/ 4384
15	PCIE_PHY_LEVEL_OVRD_IN	16	R/W	0000h	49.5.13/ 4385
16	PCIE_PHY_SUP_OVRD_OUT	16	R/W	0101h	49.5.14/ 4385
17	PCIE_PHY_MPLL_ASIC_IN	16	R	0000h	49.5.15/ 4386
18	PCIE_PHY_BS_ASIC_IN	16	R	0000h	49.5.16/ 4387
19	PCIE_PHY_LEVEL_ASIC_IN	16	R	0000h	49.5.17/ 4388
1A	PCIE_PHY_SSC_ASIC_IN	16	R	0000h	49.5.18/ 4389
1B	PCIE_PHY_SUP_ASIC_OUT	16	R	0000h	49.5.19/ 4389
1C	PCIE_PHY_ATEOVRD_STATUS	16	R	0000h	49.5.20/ 4390
20	PCIE_PHY_SCOPE_ENABLES	16	R/W	0000h	49.5.21/ 4391
21	PCIE_PHY_SCOPE_SAMPLES	16	R/W	0100h	49.5.22/ 4392
22	PCIE_PHY_SCOPE_COUNT	16	R/W	FFFFh	49.5.23/ 4392
23	PCIE_PHY_SCOPE_CTL	16	R/W	0000h	49.5.24/ 4393
24	PCIE_PHY_SCOPE_MASK_000	16	R/W	0000h	49.5.25/ 4393
25	PCIE_PHY_SCOPE_MASK_001	16	R/W	0000h	49.5.25/ 4393

Table continues on the next page...

PCIE_PHY memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
26	PCIE_PHY_SCOPE_MASK_010	16	R/W	0000h	49.5.25/ 4393
27	PCIE_PHY_SCOPE_MASK_011	16	R/W	0000h	49.5.25/ 4393
28	PCIE_PHY_SCOPE_MASK_100	16	R/W	0000h	49.5.25/ 4393
29	PCIE_PHY_SCOPE_MASK_101	16	R/W	0000h	49.5.25/ 4393
2A	PCIE_PHY_SCOPE_MASK_110	16	R/W	0000h	49.5.25/ 4393
2B	PCIE_PHY_SCOPE_MASK_111	16	R/W	0000h	49.5.25/ 4393
30	PCIE_PHY_MPLL_LOOP_CTL	16	R/W	00C0h	49.5.26/ 4394
32	PCIE_PHY_MPLL_ATB_MEAS2	16	R/W	0000h	49.5.27/ 4394
33	PCIE_PHY_MPLL_OVR	16	R/W	0000h	49.5.28/ 4395
34	PCIE_PHY_RTUNE_RTUNE_CTRL	16	R/W	0000h	49.5.29/ 4396
1000	PCIE_PHY_TX_OVRD_IN_LO	16	R/W	0000h	49.5.30/ 4397
1001	PCIE_PHY_TX_OVRD_IN_HI	16	R/W	0000h	49.5.31/ 4399
1003	PCIE_PHY_TX_OVRD_DRV_LO	16	R/W	0000h	49.5.32/ 4400
1004	PCIE_PHY_TX_OVRD_OUT	16	R/W	0000h	49.5.33/ 4400
1005	PCIE_PHY_RX_OVRD_IN_LO	16	R/W	0000h	49.5.34/ 4401
1006	PCIE_PHY_RX_OVRD_IN_HI	16	R/W	0000h	49.5.35/ 4402
1007	PCIE_PHY_RX_OVRD_OUT	16	R/W	0000h	49.5.36/ 4403
1008	PCIE_PHY_TX_ASIC_IN	16	R	0000h	49.5.37/ 4404
1009	PCIE_PHY_TX_ASIC_DRV_LO	16	R	0000h	49.5.38/ 4405
100A	PCIE_PHY_TX_ASIC_DRV_HI	16	R	0000h	49.5.39/ 4406
100B	PCIE_PHY_TX_ASIC_OUT	16	R	0000h	49.5.40/ 4406
100C	PCIE_PHY_RX_ASIC_IN	16	R	0000h	49.5.41/ 4407

Table continues on the next page...

PCIE_PHY memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
100D	PCIE_PHY_RX_ASIC_OUT	16	R	0000h	49.5.42/ 4408
1011	PCIE_PHY_TX_VMD_FSM_TX_VCM_0	16	R	0000h	49.5.43/ 4409
1012	PCIE_PHY_TX_VMD_FSM_TX_VCM_1	16	R	0000h	49.5.44/ 4409
1013	PCIE_PHY_TX_VMD_FSM_TX_VCM_DEBUG_IN	16	R/W	0000h	49.5.45/ 4410
1014	PCIE_PHY_TX_VMD_FSM_TX_VCM_DEBUG_OUT	16	R	0000h	49.5.46/ 4411
1015	PCIE_PHY_TX_LBERT_CTL	16	R/W	0000h	49.5.47/ 4411
1016	PCIE_PHY_RX_LBERT_CTL	16	R/W	0000h	49.5.48/ 4412
1017	PCIE_PHY_RX_LBERT_ERR	16	R/W	0000h	49.5.49/ 4413
1018	PCIE_PHY_RX_SCOPE_CTL	16	R/W	0000h	49.5.50/ 4413
1019	PCIE_PHY_RX_SCOPE_PHASE	16	R/W	0000h	49.5.51/ 4414
101A	PCIE_PHY_RX_DPLL_FREQ	16	R/W	0000h	49.5.52/ 4414
101B	PCIE_PHY_RX_CDR_CTL	16	R/W	000Fh	49.5.53/ 4415
101C	PCIE_PHY_RX_CDR_CDR_FSM_DEBUG	16	R	0000h	49.5.54/ 4416
101D	PCIE_PHY_RX_CDR_LOCK_VEC_OVRD	16	R/W	8000h	49.5.55/ 4417
101E	PCIE_PHY_RX_CDR_LOCK_VEC	16	R	0000h	49.5.56/ 4418
101F	PCIE_PHY_RX_CDR_ADAP_FSM	16	R	0000h	49.5.57/ 4418
1020	PCIE_PHY_RX_ATB0	16	R/W	0000h	49.5.58/ 4419
1021	PCIE_PHY_RX_ATB1	16	R/W	0000h	49.5.59/ 4420
1022	PCIE_PHY_RX_ENPWR0	16	R/W	0000h	49.5.60/ 4420
1023	PCIE_PHY_RX_PMIX_PHASE	16	R/W	0000h	49.5.61/ 4421
1024	PCIE_PHY_RX_ENPWR1	16	R/W	0000h	49.5.62/ 4422
1025	PCIE_PHY_RX_ENPWR2	16	R/W	0000h	49.5.63/ 4423

Table continues on the next page...

PCIE_PHY memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
1026	PCIE_PHY_RX_SCOPE	16	R/W	0000h	49.5.64/ 4424
102B	PCIE_PHY_TX_TXDRV_CNTRL	16	R/W	0000h	49.5.65/ 4425
102C	PCIE_PHY_TX_POWER_CTL	16	R/W	0000h	49.5.66/ 4426
102D	PCIE_PHY_TX_ALT_BLOCK	16	R/W	0000h	49.5.67/ 4427
102E	PCIE_PHY_TX_ALT_AND_LOOPBACK	16	R/W	0000h	49.5.68/ 4428
102F	PCIE_PHY_TX_TX_ATB_REG	16	R/W	0000h	49.5.69/ 4429

49.5.1 Register ID Low 16 bits (PCIE_PHY_IDCODE_LO)

Address: 0h base + 0h offset = 0h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	IDCODE_LO															
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_IDCODE_LO field descriptions

Field	Description
IDCODE_LO	Data

49.5.2 Register ID High 16 bits (PCIE_PHY_IDCODE_HI)

Address: 0h base + 1h offset = 1h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	IDCODE_HI															
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_IDCODE_HI field descriptions

Field	Description
IDCODE_HI	Data

49.5.3 Debug Register (PCIE_PHY_DEBUG)

Address: 0h base + 2h offset = 2h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	Reserved										DTB_SEL		TX_VREF_SEL			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

PCIE_PHY_DEBUG field descriptions

Field	Description
15–6 -	This field is reserved. Reserved
6–5 DTB_SEL	Description: The lane DTB's are ORed together with the support DTB signals selected with the following encodings. 00 None 01 reset_ctl DTB output 10 Scope DTB output 11 rtune DTB output
TX_VREF_SEL	-

49.5.4 Debug Register (PCIE_PHY_RTUNE_DEBUG)

Address: 0h base + 3h offset = 3h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved	VALUE						
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	VALUE			TYPE		SET_VAL	MAN_TUNE	FLIP_COMP
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RTUNE_DEBUG field descriptions

Field	Description
15 -	This field is reserved. Reserved
14–5 VALUE	Value to use when triggering SET_VAL field. Only the 6 LSB's are used when setting Rx cal or Tx cal values.
4–3 TYPE	Type of manual tuning or register read/write to execute. 00 ADC, or read/write rt_value 01 Rx tune, or read/write rx_cal_val (only 6 bits)

Table continues on the next page...

PCIE_PHY_RTUNE_DEBUG field descriptions (continued)

Field	Description
	10 Tx tune, or read/write tx_cal_val (only 6 bits) 11 Resref detect (no affect when triggering SET_VAL fi
2 SET_VAL	Sets value. Write a 1 to manually write the register specified by the TYPE field to the value in the VALUE field.
1 MAN_TUNE	Write a 1 to perform a manual tuning specified by the TYPE field. Starting a manual tune while a tune is currently running can cause unpredictable results. For use only when you know what the part is doing (with respect to resistor tuning). **NOTE:** Write a 1 to perform an operation. Subsequent writes with the bit set will trigger the operation. No need to clear (0) the bit between writes.
0 FLIP_COMP	Inverts Analog Comparator Output.

49.5.5 PCIE_PHY_RTUNE_STAT

Address: 0h base + 4h offset = 4h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Reserved								STAT							
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_RTUNE_STAT field descriptions

Field	Description
15–10 -	This field is reserved. Reserved
STAT	Current value of the register specifed by the RTUNE_DEBUG[TYPE] field.

49.5.6 PCIE_PHY_SS_PHASE

Address: 0h base + 5h offset = 5h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	Reserved								DTHR							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_SS_PHASE field descriptions

Field	Description
15–10 -	This field is reserved. Reserved
DTHR	Current value of the register specifed by the RTUNE_DEBUG[TYPE] field.

49.5.7 PCIE_PHY_SS_FREQ

Address: 0h base + 6h offset = 6h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved	FREQ_ OVRD	FREQ_PK					
Reset	0	0	1	1	0	0	1	1

Bit	7	6	5	4	3	2	1	0
Read Write	FREQ_PK	FREQ_CNT_INIT						
Reset	0	0	1	0	0	1	1	1

PCIE_PHY_SS_FREQ field descriptions

Field	Description
15 -	This field is reserved. Reserved
14 FREQ_OVRD	Frequency register override. Spread spectrum clocking must be enabled to read from or write to this register. **NOTE:** Must be set for PHASE writes to stick.
13–7 FREQ_PK	Peak frequency value (for changing direction). Spread spectrum clocking must be enabled to read from or write to this register.
FREQ_CNT_INIT	Initial frequency counter value. Spread spectrum clocking must be enabled to read from or write to this register.

49.5.8 PCIE_PHY_ATEOVRD

Address: 0h base + 10h offset = 10h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				ateovrd_en	ref_usb2_en	ref_clkdiv2	Reserved
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_ATEOVRD field descriptions

Field	Description
15–4 -	This field is reserved. Reserved
3 ateovrd_en	Override enable for ATE signals.

Table continues on the next page...

PCIE_PHY_ATEOVRD field descriptions (continued)

Field	Description
2 ref_usb2_en	Override value for HSPHY ref_clk enable.
1 ref_clkdiv2	Override value for SSP ref_clk prescaler.
0 -	This field is reserved. Reserved

49.5.9 PCIE_PHY_MPLL_OVRD_IN_LO

Address: 0h base + 11h offset = 11h

Bit	15	14	13	12	11	10	9	8
Read Write	RES_ACK_IN_OVRD	RES_ACK_IN	RES_REQ_IN_OVRD	RES_REQ_IN	RTUNE_REQ_OVRD	RTUNE_REQ	MPLL_MULTIPLIER_OVRD	MPLL_MULTIPLIER
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	MPLL_MULTIPLIER						MPLL_EN_OVRD	MPLL_EN
Reset	0	1	0	0	1	1	0	0

PCIE_PHY_MPLL_OVRD_IN_LO field descriptions

Field	Description
15 RES_ACK_IN_OVRD	Override enable for res_ack_in.
14 RES_ACK_IN	Override value for res_ack_in.
13 RES_REQ_IN_OVRD	Override enable for res_req_in.
12 RES_REQ_IN	Override value for res_req_in.
11 RTUNE_REQ_OVRD	Override enable for rtune_req.
10 RTUNE_REQ	Override value for rtune_req.
9 MPLL_MULTIPLIER_OVRD	Override enable for mpll_multiplier.

Table continues on the next page...

PCIE_PHY_MPLL_OVRD_IN_LO field descriptions (continued)

Field	Description
8–2 MPLL_ MULTIPLIER	Override value for mpll_multiplier.
1 MPLL_EN_ OVRD	Override enable for mpll_en.
0 MPLL_EN	Override value for mpll_en.

49.5.10 PCIE_PHY_MPLL_OVRD_IN_HI

Address: 0h base + 11h offset = 11h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved					MPLL_RST	FSEL_OVR	FSEL
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	FSEL		MPLL_ WORD_ CLK_EN_ OVRD	MPLL_ WORD_ CLK_EN	MPLL_ DWORD_ CLK_EN_ OVRD	MPLL_ DWORD_ CLK_EN	MPLL_ QWORD_ CLK_EN_ OVRD	MPLL_ QWORD_ CLK_EN
Reset	0	1	0	0	1	1	0	0

PCIE_PHY_MPLL_OVRD_IN_HI field descriptions

Field	Description
15–11 -	This field is reserved. Reserved.
10 MPLL_RST	Resets the MPLL state machine. Writing the register with this bit set will reset the MPLL power-up/down FSM, regardless of the current state of the register bit.
9 FSEL_OVR	Override enable for fsel[2:0].
8–6 FSEL	: Override value for fsel[2:0].
5 MPLL_WORD_ CLK_EN_OVRD	Override enable for mpll_word_clk_en.
4 MPLL_WORD_ CLK_EN	Override value for mpll_word_clk_en.
3 MPLL_DWORD_ CLK_EN_OVRD	Override enable for mpll_dword_clk_en.

Table continues on the next page...

PCIE_PHY_MPLL_OVRD_IN_HI field descriptions (continued)

Field	Description
2 MPLL_DWORD_CLK_EN	Override value for mpll_dword_clk_en.
1 MPLL_QWORD_CLK_EN_OVRD	Override enable for mpll_qword_clk_en.
0 MPLL_QWORD_CLK_EN	Override value for mpll_qword_clk_en.

49.5.11 PCIE_PHY_SSC_OVRD_IN

Address: 0h base + 13h offset = 13h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Reserved				SSC_OVRD_IN_EN	SSC_EN	SSC_RANGE		SSC_REF_CLK_SEL							
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_SSC_OVRD_IN field descriptions

Field	Description
15–12 -	This field is reserved. Reserved
11 SSC_OVRD_IN_EN	Override enable for Spread Spectrum generator.
10 SSC_EN	Override value for SSC enable.
9–8 SSC_RANGE	Override value for SSC modulation range.
SSC_REF_CLK_SEL	Override value for reference clock scaling.

49.5.12 PCIE_PHY_BS_OVRD_IN

Address: 0h base + 14h offset = 14h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved				EN	INVERT	INIT	HIGHZ
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	CLAMP	EXTEST_ AC	EXTEST	PRELOAD	UPDATE_ DR	CAPTURE_ DR	SHIFT_DR	IN
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_BS_OVRD_IN field descriptions

Field	Description
15–12 -	This field is reserved. Reserved.
11 EN	Enables override values for all inputs controlled by this register.
10 INVERT	Override value for bs_invert.
9 INIT	Override value for bs_init.
8 HIGHZ	Override value for bs_highz.
7 CLAMP	Override value for bs_clamp.
6 EXTEST_AC	Override value for bs_extest_ac.
5 EXTEST	Override value for bs_extest.
4 PRELOAD	Override value for bs_preload.
3 UPDATE_DR	Override value for bs_update_dr.
2 CAPTURE_DR	Override value for bs_capture_dr
1 SHIFT_DR	Override value for bs_shift_dr.
0 IN	Override value for bs_shift_dr.

49.5.13 PCIE_PHY_LEVEL_OVRD_IN

Address: 0h base + 15h offset = 15h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read / Write	Reserved					EN	ACJT_LEVEL					LOS_LEVEL				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_LEVEL_OVRD_IN field descriptions

Field	Description
15–11 -	This field is reserved. Reserved.
10 EN	Enables override values for all inputs controlled by this register.
9–5 ACJT_LEVEL	Override value for acjt_level.
LOS_LEVEL	Override value for los_level.

49.5.14 PCIE_PHY_SUP_OVRD_OUT

Address: 0h base + 16h offset = 16h

Bit	15	14	13	12	11	10	9	8
Read / Write	Reserved						MPLL_STATE_OVRD	MPLL_STATE
Reset	0	0	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
Read / Write	BS_OUT_OVRD	BS_OUT	RTUNE_ACK_OVRD	RTUNE_ACK	RES_REQ_OUT_OVRD	RES_REQ_OUT	RES_ACK_OUT_OVRD	RES_ACK_OUT
Reset	0	0	0	0	0	0	0	1

PCIE_PHY_SUP_OVRD_OUT field descriptions

Field	Description
15–10 -	This field is reserved. Reserved.
9 MPLL_STATE_OVRD	Override enable for mpll_state output.
8 MPLL_STATE	Override value for mpll_state output.
7 BS_OUT_OVRD	Override enable for bs_out output.

Table continues on the next page...

PCIE_PHY_SUP_OVRD_OUT field descriptions (continued)

Field	Description
6 BS_OUT	Override value for bs_out output.
5 RTUNE_ACK_ OVRD	Override enable for rtune_ack output.
4 RTUNE_ACK	Override value for rtune_ack output.
3 RES_REQ_ OUT_OVRD	Override enable for res_req_out output.
2 RES_REQ_OUT	Override value for res_req_out output.
1 RES_ACK_OUT_ OVRD	Override enable for res_ack_out output.
0 RES_ACK_OUT	Override value for res_ack_out output.

49.5.15 PCIE_PHY_MPLL_ASIC_IN

Address: 0h base + 17h offset = 17h

Bit	15	14	13	12	11	10	9	8
Read	Reserved		MPLL_ WORD_ CLK_EN	MPLL_ DWORD_ CLK_EN	MPLL_ QWORD_ CLK_EN	RES_ACK_ IN	RES_REQ_ IN	RTUNE_ REQ
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	MPLL_MULTIPLIER							MPLL_EN
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_MPLL_ASIC_IN field descriptions

Field	Description
15–14 -	This field is reserved. Reserved.
13 MPLL_WORD_ CLK_EN	Value from ASIC for mpll_word_clk_en.

Table continues on the next page...

PCIE_PHY_MPLL_ASIC_IN field descriptions (continued)

Field	Description
12 MPLL_DWORD_CLK_EN	Value from ASIC for mpll_dword_clk_en.
11 MPLL_QWORD_CLK_EN	Value from ASIC for mpll_qword_clk_en.
10 RES_ACK_IN	Value from ASIC for res_ack_in.
9 RES_REQ_IN	Value from ASIC for res_req_in.
8 RTUNE_REQ	Value from ASIC for rtune_req.
7–1 MPLL_MULTIPLIER	Value from ASIC for mpll_multiplier.
0 MPLL_EN	Value from ASIC for mpll_en.

49.5.16 PCIE_PHY_BS_ASIC_IN

Address: 0h base + 18h offset = 18h

Bit	15	14	13	12	11	10	9	8
Read	Reserved					INVERT	INIT	HIGHZ
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	CLAMP	EXTEST_AC	EXTEST	PRELOAD	UPDATE_DR	CAPTURE_DR	SHIFT_DR	IN
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_BS_ASIC_IN field descriptions

Field	Description
15–11 -	This field is reserved. Reserved.
10 INVERT	Value from ASIC for bs_invert.
9 INIT	Value from ASIC for bs_init.
8 HIGHZ	Value from ASIC for bs_highz.

Table continues on the next page...

PCIE_PHY_BS_ASIC_IN field descriptions (continued)

Field	Description
7 CLAMP	Value from ASIC for bs_clamp.
6 EXTEST_AC	Value from ASIC for bs_extest_ac.
5 EXTEST	Value from ASIC for bs_extest.
4 PRELOAD	Value from ASIC for bs_preload.
3 UPDATE_DR	Value from ASIC for bs_update_dr.
2 CAPTURE_DR	Value from ASIC for bs_capture_dr.
1 SHIFT_DR	Value from ASIC for bs_shift_dr.
0 IN	Value from ASIC for bs_in.

49.5.17 PCIE_PHY_LEVEL_ASIC_IN

Address: 0h base + 19h offset = 19h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Reserved						ACJT_LEVEL					LOS_LEVEL				
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_LEVEL_ASIC_IN field descriptions

Field	Description
15–10 -	This field is reserved. Reserved.
9–5 ACJT_LEVEL	Value from ASIC for acjt_level.
LOS_LEVEL	Value from ASIC for los_level.

49.5.18 PCIE_PHY_SSC_ASIC_IN

Address: 0h base + 1Ah offset = 1Ah

Bit	15	14	13	12	11	10	9	8
Read	Reserved		SS_EN	SSC_RANGE		SSC_REF_CLK_SEL		
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	SSC_REF_CLK_SEL						FSEL	
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_SSC_ASIC_IN field descriptions

Field	Description
15–14 -	This field is reserved. Reserved.
13 SS_EN	Value from ASIC for ssc_en.
12–11 SSC_RANGE	Value from ASIC for ssc_range.
10–3 SSC_REF_CLK_SEL	Value from ASIC for ssc_ref_clk_sel
FSEL	Value from ASIC for fsel.

49.5.19 PCIE_PHY_SUP_ASIC_OUT

Address: 0h base + 1Bh offset = 1Bh

Bit	15	14	13	12	11	10	9	8
Read	Reserved							
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	Reserved			MPLL_STATE	BS_OUT	RTUNE_ACK	RES_REQ_OUT	RES_ACK_OUT
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_SUP_ASIC_OUT field descriptions

Field	Description
15–5 -	This field is reserved. Reserved.
4 MPLL_STATE	Value from PHY for mpll_state output.
3 BS_OUT	Value from PHY for bs_out output.
2 RTUNE_ACK	Value from PHY for rtune_ack output.
1 RES_REQ_OUT	Value from PHY for res_req_out output.
0 RES_ACK_OUT	Value from PHY for res_ack_out output.

49.5.20 PCIE_PHY_ATEOVRD_STATUS

Address: 0h base + 1Ch offset = 1Ch

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Reserved							REF_SSP_EN	REF_USE_PAD	PHY_RESET_IN	REF_CLKDIV2_IN	REF_USB2_EN_IN	ATEOVRD_EN	PHY_RESET_OUT	REF_CLKDIV2_OUT	REF_USB2_EN_OUT
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_ATEOVRD_STATUS field descriptions

Field	Description
15–9 -	This field is reserved. Reserved.
8 REF_SSP_EN	Value from ASIC for ref_ssp_en.
7 REF_USE_PAD	Value from ASIC for ref_use_pad
6 PHY_RESET_IN	Value from ASIC for phy_reset
5 REF_CLKDIV2_IN	Value from ASIC for ref_clkdiv2.
4 REF_USB2_EN_IN	Value from ASIC for ref_usb2_en.
3 ATEOVRD_EN	When set, values from ATEOVRD register are sent to PHY.
2 PHY_RESET_OUT	Value from ATEOVRD for phy_reset.
1 REF_CLKDIV2_OUT	Value from ATEOVRD for ref_clkdiv2.
0 REF_USB2_EN_OUT	Value from ATEOVRD for ref_usb2_en.

49.5.21 PCIE_PHY_SCOPE_ENABLES

Address: 0h base + 20h offset = 20h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Reserved													MASK_SATURATION_MODE	MASK_EN	XOR_EN
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_SCOPE_ENABLES field descriptions

Field	Description
15–3 -	This field is reserved. Reserved.

Table continues on the next page...

PCIE_PHY_SCOPE_ENABLES field descriptions (continued)

Field	Description
2 MASK_ SATURATION_ MODE	Method of mask saturation. 1 Saturates when the first mask_counter reaches sample_limit. 0 Saturates when all mask_counters have reached sample_limit.
1 MASK_EN	Enables scope_mask input for tracking count values. Clears registers when deasserted.
0 XOR_EN	Uses scope_xor input for count values.

49.5.22 PCIE_PHY_SCOPE_SAMPLES

Address: 0h base + 21h offset = 21h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	SAMPLES															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

PCIE_PHY_SCOPE_SAMPLES field descriptions

Field	Description
SAMPLES	Number of samples to count.

49.5.23 PCIE_PHY_SCOPE_COUNT

Address: 0h base + 22h offset = 22h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	COUNT															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

PCIE_PHY_SCOPE_COUNT field descriptions

Field	Description
COUNT	A write to this register starts the counting process. The value of FFFF indicates counting still in progress. If in MASK mode, asserting MASK_EN also starts the counting

49.5.24 PCIE_PHY_SCOPE_CTL

Address: 0h base + 23h offset = 23h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved						COUNT	MASK_ SATURATI ON
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_SCOPE_CTL field descriptions

Field	Description
15–2 -	This field is reserved. Reserved.
1 COUNT	A write to this register starts the counting process. The value of FFFF indicates counting still in progress. If in MASK mode, asserting MASK_EN also starts the counting
0 MASK_ SATURATION	When asserted, mask registers have saturated.

49.5.25 PCIE_PHY_SCOPE_MASK*n*

Address: 0h base + 24h offset + (1d × i), where i=0d to 7d

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	MASK_VAL_n															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_SCOPE_MASK*n* field descriptions

Field	Description
MASK_VAL_n	Starting count value of mask register. Scope must be enabled to read from or write to this register.

49.5.26 PCIE_PHY_MPLL_LOOP_CTL

Address: 0h base + 30h offset = 30h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	PROP_CNTRL				INT_CNTRL		VBF_SF	VMB
Reset	1	1	0	0	0	0	0	0

PCIE_PHY_MPLL_LOOP_CTL field descriptions

Field	Description
15–8 -	This field is reserved. Reserved.
7–4 PROP_CNTRL	Charge pump proportional current setting.
3–2 INT_CNTRL	Charge pump integrating current setting.
1 VBF_SF	Measures MPLL VBF_SF (RC filtered gate voltage for VPSF source follower).
0 VMB	Measures MPLL master bias voltage.

49.5.27 PCIE_PHY_MPLL_ATB_MEAS2

Address: 0h base + 32h offset = 32h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	Reserved								IVCO_FILT	VCNTRL_M	VCNTRL_P	ATB_SENSE_SEL	MEAS_TEMP	FRC_PMIX_VPMIX	EN_MPMIX_VPMIX	EN_MPMIX_TST
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_MPLL_ATB_MEAS2 field descriptions

Field	Description
15–8 -	This field is reserved. Reserved.
7 IVCO_FILT	Puts filtered version of ivco on atb_s_p

Table continues on the next page...

PCIE_PHY_MPLL_ATB_MEAS2 field descriptions (continued)

Field	Description
6 VCNTRL_M	Puts dcc output vcntrl_p on atb_s_m
5 VCNTRL_P	Puts dcc output vcntrl_m on atb_s_p
4 ATB_SENSE_SEL	connects internal atb sense bus to external bus
3 MEAS_TEMP	Instructs POR block to measure the temperature.
2 FRC_PMIX_VPMIX	Forces mpll_pmix_vreg to use atb_s_m as its input instead of vbg.
1 EN_MPMIX_VPMIX	Puts vreg_pmix on atb_s_p.
0 EN_MPMIX_TST	Enables XOR gate to test linearity of MPLL phase mixer.

49.5.28 PCIE_PHY_MPLL_OVR

Address: 0h base + 33h offset = 33h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	PWRON_LCL	EN_PWRON_LCL	GS_LCL	EN_GS_LCL	RST_LCL	EN_RST_LCL	PMIX_CLK_SEL_LCL	EN_PMIX_CLK_SEL_LCL
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_MPLL_OVR field descriptions

Field	Description
15–8 -	This field is reserved. Reserved.

Table continues on the next page...

PCIE_PHY_MPLL_OVR field descriptions (continued)

Field	Description
7 PWRON_LCL	local power_on value
6 EN_PWRON_LCL	Enables local control of power_on
5 GS_LCL	local gear_shift value
4 EN_GS_LCL	Enables local control of gear_shift
3 RST_LCL	local Reset value
2 EN_RST_LCL	enable local control of reset
1 PMIX_CLK_SEL_LCL	local pmix_clk_sel value
0 EN_PMIX_CLK_SEL_LCL	enable local control of pmix_clk_sel

49.5.29 PCIE_PHY_RTUNE_RTUNE_CTRL

Address: 0h base + 34h offset = 34h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	RT_PWroN_FRC_ON	X4_FRC_OFF	RT_DAC_MODE		RT_DAC_CHOP	RT_ATB	RT_SEL_ATBP	RT_SEL_ATBF
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RTUNE_RTUNE_CTRL field descriptions

Field	Description
15–8 -	This field is reserved. Reserved.
7 RT_PWroN_FRC_ON	When set, forces RTUNE block to be on
6 X4_FRC_OFF	When set, do not multiply test current by 4
5–4 RT_DAC_MODE	Margin DAC mode control bits

Table continues on the next page...

PCIE_PHY_RTUNE_RTUNE_CTRL field descriptions (continued)

Field	Description
	00 powerdown 01 DAC drives atb_s_p/m directly 10 DAC drives atb_s_p/m to the RX in margining mode 11 illegal state
3 RT_DAC_CHOP	Margin DAC chop control bit
2 RT_ATB	RTUNE ATB mode control bit 1 RTUNE performs ADC on ATB input 0 not accessing ATB
1 RT_SEL_ATBP	RTUNE ATB sense input select bit 1 atb_s_p 0 atb_s_m
0 RT_SEL_ATBF	RTUNE ATB input slect bit 1 atb_fm 0 atb_s_p/m

49.5.30 PCIE_PHY_TX_OVRD_IN_LO

Address: 0h base + 1000h offset = 1000h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved		TX_DETECT_RX_REQ_OVRD	TX_DETECT_RX_REQ	TX_BEACON_EN_OVRD	TX_BEACON_EN	TX_CM_EN_OVRD	TX_CM_EN
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	TX_EN_OVRD	TX_EN	TX_DATA_EN_OVRD	TX_DATA_EN	TX_INVERT_OVRD	TX_INVERT	TX_LOOPBK_EN_OVRD	LOOPBK_EN
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_OVRD_IN_LO field descriptions

Field	Description
15–14 -	This field is reserved. Reserved.

Table continues on the next page...

PCIE_PHY_TX_OVRD_IN_LO field descriptions (continued)

Field	Description
13 TX_DETECT_ RX_REQ_OVRD	Override enable for tx_detect_rx_req
12 TX_DETECT_ RX_REQ	Override value for tx_detect_rx_req
11 TX_BEACON_ EN_OVRD	Override enable for tx_beacon_en
10 TX_BEACON_ EN	Override value for tx_beacon_en
9 TX_CM_EN_ OVRD	Override enable for tx_cm_en
8 TX_CM_EN	Override value for tx_cm_en
7 TX_EN_OVRD	Override enable for tx_en
6 TX_EN	Override value for tx_en
5 TX_DATA_EN_ OVRD	Override enable for tx_data_en
4 TX_DATA_EN	Override value for tx_data_en
3 TX_INVERT_ OVRD	Override enable for tx_invert
2 TX_INVERT	Override value for tx_invert
1 TX_LOOPBK_ EN_OVRD	Override enable for loopbk_en
0 LOOPBK_EN	Override value for loopbk_en

49.5.31 PCIE_PHY_TX_OVRD_IN_HI

Address: 0h base + 1001h offset = 1001h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	TX_ RESET_ OVRD	TX_RESET	TX_ NYQUIST_ DATA	TX_CLK_ OUT_EN_ OVRD	TX_CLK_ OUT_EN	TX_RATE_ OVRD	TX_RATE	
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_OVRD_IN_HI field descriptions

Field	Description
15–8 -	This field is reserved. Reserved.
7 TX_RESET_ OVRD	Override enable for tx_reset
6 TX_RESET	Override value for tx_reset
5 TX_NYQUIST_ DATA	Override incoming data to nyquist
4 TX_CLK_OUT_ EN_OVRD	Override enable for tx_clk_out_en.
3 TX_CLK_OUT_ EN	Override incomming tx_clk_out_en.
2 TX_RATE_ OVRD	Override enable for tx_rate.
TX_RATE	Override incomming tx lane rate.

49.5.32 PCIE_PHY_TX_OVRD_DRV_LO

Address: 0h base + 1003h offset = 1003h

Bit	15	14	13	12	11	10	9	8
Read / Write	Reserved	EN	PREEMPH					
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read / Write	PREEMPH	AMPLITUDE						
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_OVRD_DRV_LO field descriptions

Field	Description
15 -	This field is reserved. Reserved.
14 EN	Enables override values for all inputs controlled by this register
13–7 PREEMPH	Override value for transmit preemphasis
AMPLITUDE	Override value for transmit amplitude.

49.5.33 PCIE_PHY_TX_OVRD_OUT

Address: 0h base + 1004h offset = 1004h

Bit	15	14	13	12	11	10	9	8
Read / Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	TX_STATE_OVRD	TX_STATE	TX_CM_STATE_OVRD	TX_CM_STATE	TX_DETECT_RX_ACK_OVRD	TX_DETECT_RX_ACK	DETECT_RX_RES_OVRD	DETECT_RX_RES
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_OVRD_OUT field descriptions

Field	Description
15–8 -	This field is reserved. Reserved.
7 TX_STATE_OVRD	Override enable for tx_state

Table continues on the next page...

PCIE_PHY_TX_OVRD_OUT field descriptions (continued)

Field	Description
6 TX_STATE	Override value for tx_state
5 TX_CM_STATE_OVRD	Override enable for tx_cm_state
4 TX_CM_STATE	Override value for tx_cm_state
3 TX_DETECT_RX_ACK_OVRD	Override enable for tx_detect_rx_ack
2 TX_DETECT_RX_ACK	Override value for tx_detect_rx_ack
1 DETECT_RX_RES_OVRD	Override enable for tx_detect_rx_res
0 DETECT_RX_RES	Override value for tx_detect_rx_res

49.5.34 PCIE_PHY_RX_OVRD_IN_LO

Address: 0h base + 1005h offset = 1005h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Reserved		RX_LOS_EN_OVRD	RX_LOS_EN	RX_TERM_EN_OVRD	RX_TERM_EN	RX_BIT_SHIFT_OVRD	RX_BIT_SHIFT	RX_ALIGN_EN_OVRD	RX_ALIGN_EN	RX_DATA_EN_OVRD	RX_DATA_EN	RX_PLL_EN_OVRD	RX_PLL_EN	RX_INVERT_OVRD	RX_INVERT
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_RX_OVRD_IN_LO field descriptions

Field	Description
15–14 -	This field is reserved. Reserved.
13 RX_LOS_EN_OVRD	Override enable for rx_los_en
12 RX_LOS_EN	Override value for rx_los_en
11 RX_TERM_EN_OVRD	Override enable for rx_term_en

Table continues on the next page...

PCIE_PHY_RX_OVRD_IN_LO field descriptions (continued)

Field	Description
10 RX_TERM_EN	Override value for rx_term_en
9 RX_BIT_SHIFT_OVRD	Override enable for rx_bit_shift
8 RX_BIT_SHIFT	Override value for rx_bit_shift
7 RX_ALIGN_EN_OVRD	Override enable for rx_align_en
6 RX_ALIGN_EN	Override value for rx_align_en
5 RX_DATA_EN_OVRD	Override enable for rx_data_en
4 RX_DATA_EN	Override value for rx_data_en
3 RX_PLL_EN_OVRD	Override enable for rx_pll_en
2 RX_PLL_EN	Override value for rx_pll_en
1 RX_INVERT_OVRD	Override enable for rx_invert
0 RX_INVERT	Override value for rx_invert

49.5.35 PCIE_PHY_RX_OVRD_IN_HI

Address: 0h base + 1006h offset = 1006h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved		RX_RESET_OVRD	RX_RESET	RX_EQ_OVRD	RX_EQ		
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	RX_EQ_EN_OVRD	RX_EQ_EN	RX_LOS_FILTER_OVRD	RX_LOS_FILTER		RX_RATE_OVRD	RX_RATE	
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_OVRD_IN_HI field descriptions

Field	Description
15–14 -	This field is reserved. Reserved.
13 RX_RESET_ OVRD	Override enable for rx_reset
12 RX_RESET	Override value for rx_reset
11 RX_EQ_OVRD	Override enable for rx_eq
10–8 RX_EQ	Override value for rx_eq
7 RX_EQ_EN_ OVRD	Override enable for rx_eq_en
6 RX_EQ_EN	Override value for rx_eq_en
5 RX_LOS_ FILTER_OVRD	Override enable for rx_los_filter
4–3 RX_LOS_ FILTER	Override value for rx_los_filter
2 RX_RATE_ OVRD	Override enable for rx_rate
RX_RATE	Override value for rx_rate

49.5.36 PCIE_PHY_RX_OVRD_OUT

Address: 0h base + 1007h offset = 1007h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved	ZERO_ DATA	LOS_OVRD	LOS	PLL_ STATE_ OVRD	PLL_STATE	VALID_ OVRD	VALID
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_OVRD_OUT field descriptions

Field	Description
15–7 -	This field is reserved. Reserved.
6 ZERO_DATA	Override data output to all zeros
5 LOS_OVRD	Override value for rx_los
4 LOS	Override value for rx_los
3 PLL_STATE_ OVRD	Override enable for rx_pll_state
2 PLL_STATE	Override value for rx_pll_state
1 VALID_OVRD	Override enable for rx_valid
0 VALID	Override value for rx_valid

49.5.37 PCIE_PHY_TX_ASIC_IN

Address: 0h base + 1008h offset = 1008h

Bit	15	14	13	12	11	10	9	8
Read	Reserved					TX_CLK_ OUT_EN	DETECT_ RX_REQ	BEACON_ EN
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	CM_EN	TX_EN	DATA_EN	TX_RESET	INVERT	LOOPBK_ EN	TX_RATE	
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_ASIC_IN field descriptions

Field	Description
15–11 -	This field is reserved. Reserved.
10 TX_CLK_OUT_ EN	Value from ASIC for tx_clk_out_en

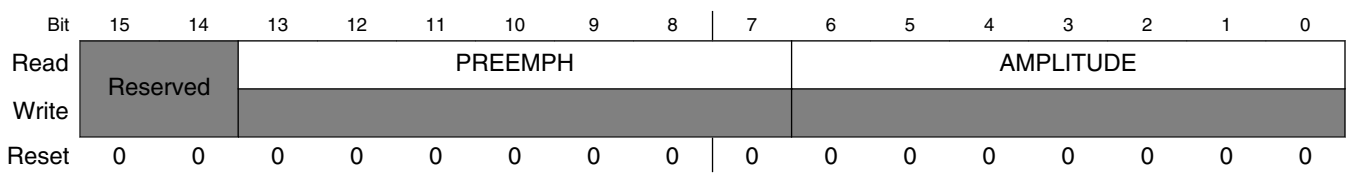
Table continues on the next page...

PCIE_PHY_TX_ASIC_IN field descriptions (continued)

Field	Description
9 DETECT_RX_ REQ	Value from ASIC for tx_detect_rx_req
8 BEACON_EN	Value from ASIC for tx_beacon_en
7 CM_EN	Value from ASIC for tx_cm_en
6 TX_EN	Value from ASIC for tx_en
5 DATA_EN	Value from ASIC for tx_data_en
4 TX_RESET	Value from ASIC for tx_reset
3 INVERT	Value from ASIC for tx_invert
2 LOOPBK_EN	Value from ASIC for loopbk_en
TX_RATE	Value from ASIC for tx_rate

49.5.38 PCIE_PHY_TX_ASIC_DRV_LO

Address: 0h base + 1009h offset = 1009h



PCIE_PHY_TX_ASIC_DRV_LO field descriptions

Field	Description
15–14 -	This field is reserved. Reserved.
13–7 PREEMPH	Value from ASIC for tx_preemph
AMPLITUDE	Value from ASIC for tx_amplitude

49.5.39 PCIE_PHY_TX_ASIC_DRV_HI

Address: 0h base + 100Ah offset = 100Ah

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Reserved											TERM_OFFSET				
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_TX_ASIC_DRV_HI field descriptions

Field	Description
15–5 -	This field is reserved. Reserved.
TERM_OFFSET	Value from ASIC for tx_term_offset

49.5.40 PCIE_PHY_TX_ASIC_OUT

Address: 0h base + 100Bh offset = 100Bh

Bit	15	14	13	12	11	10	9	8
Read	Reserved							
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	Reserved			STATE	CM_STATE	DETECT_ RX_ACK	0	DETECT_ RX_RES
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_ASIC_OUT field descriptions

Field	Description
15–5 -	This field is reserved. Reserved.
4 STATE	Value from PHY for tx_state
3 CM_STATE	Value from PHY for tx_cm_state
2 DETECT_RX_ ACK	Value from PHY for tx_detect_rx_ack

Table continues on the next page...

PCIE_PHY_TX_ASIC_OUT field descriptions (continued)

Field	Description
1 Reserved	This read-only field is reserved and always has the value 0.
0 DETECT_RX_RES	Value from PHY for tx_detect_rx_res

49.5.41 PCIE_PHY_RX_ASIC_IN

Address: 0h base + 100Ch offset = 100Ch

Bit	15	14	13	12	11	10	9	8
Read	RX_EQ_EN	RX_EQ			LOS_FILTER		LOS_EN	TERM_EN
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	CLK_SHIFT	ALIGN_EN	DATA_EN	PLL_EN	RX_RESET	INVERT	RX_RATE	
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_ASIC_IN field descriptions

Field	Description
15 RX_EQ_EN	Value from ASIC for rx_eq_en
14–12 RX_EQ	Value from ASIC for rx_eq
11–10 LOS_FILTER	Value from ASIC for rx_los_filter
9 LOS_EN	Value from ASIC for rx_los_en
8 TERM_EN	Value from ASIC for rx_term_en
7 CLK_SHIFT	Value from ASIC for rx_bit_shift
6 ALIGN_EN	Value from ASIC for rx_align_en
5 DATA_EN	Value from ASIC for rx_data_en
4 PLL_EN	Value from ASIC for rx_pll_en
3 RX_RESET	Value from ASIC for rx_reset

Table continues on the next page...

PCIE_PHY_RX_ASIC_IN field descriptions (continued)

Field	Description
2 INVERT	Value from ASIC for rx_invert
RX_RATE	Value from ASIC for rx_rate

49.5.42 PCIE_PHY_RX_ASIC_OUT

Address: 0h base + 100Dh offset = 100Dh

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	Reserved					LOS	PLL_STATE	VALID
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_ASIC_OUT field descriptions

Field	Description
15–3 -	This field is reserved. Reserved.
2 LOS	Value from PHY for rx_los
1 PLL_STATE	Value from PHY for rx_pll_state
0 VALID	Value from PHY for rx_valid

49.5.43 PCIE_PHY_TX_VMD_FSM_TX_VCM_0

Address: 0h base + 1011h offset = 1011h

Bit	15	14	13	12	11	10	9	8
Read	Reserved	DONE	N_USE					
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	N_USE	N_TRISTATE						
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_VMD_FSM_TX_VCM_0 field descriptions

Field	Description
15 -	This field is reserved. Reserved.
14 DONE	Configuration is done
13–7 N_USE	Value from VMD for legs to use
N_TRISTATE	Value from VMD for number of tristate legs.

49.5.44 PCIE_PHY_TX_VMD_FSM_TX_VCM_1

Address: 0h base + 1012h offset = 1012h

Bit	15	14	13	12	11	10	9	8
Read	FIXED_ DONE	TRA_DONE	N_FIXED					
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	N_FIXED	N_TRAILER						
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_VMD_FSM_TX_VCM_1 field descriptions

Field	Description
15 FIXED_DONE	N_FIXED Multiplication has completed.
14 TRA_DONE	N_TRAILER Multiplication has completed.
13–7 N_FIXED	Value from VMD for number of fixed driver legs.
N_TRAILER	Value from VMD for number of trailer legs.

49.5.45 PCIE_PHY_TX_VMD_FSM_TX_VCM_DEBUG_IN

Address: 0h base + 1013h offset = 1013h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

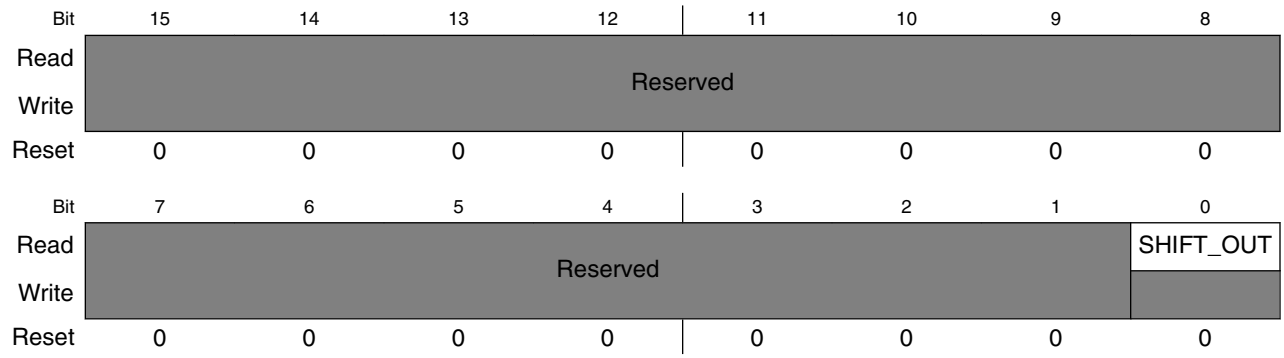
Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				CONFIG_ OVRD	CONFIG_ LOAD	CONFIG_ CLK	CONFIG_ DATA
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_VMD_FSM_TX_VCM_DEBUG_IN field descriptions

Field	Description
15–4 -	This field is reserved. Reserved
3 CONFIG_OVRD	Override the Voltage Mode Driver Configuration FSM and access the shift chain directly.
2 CONFIG_LOAD	Override value for the Voltage Mode Driver Configuration FSM's config load.
1 CONFIG_CLK	Override value for the Voltage Mode Driver Configuration FSM's config clk.
0 CONFIG_DATA	Override value for the Voltage Mode Driver Configuration FSM's config data.

49.5.46 PCIE_PHY_TX_VMD_FSM_TX_VCM_DEBUG_OUT

Address: 0h base + 1014h offset = 1014h

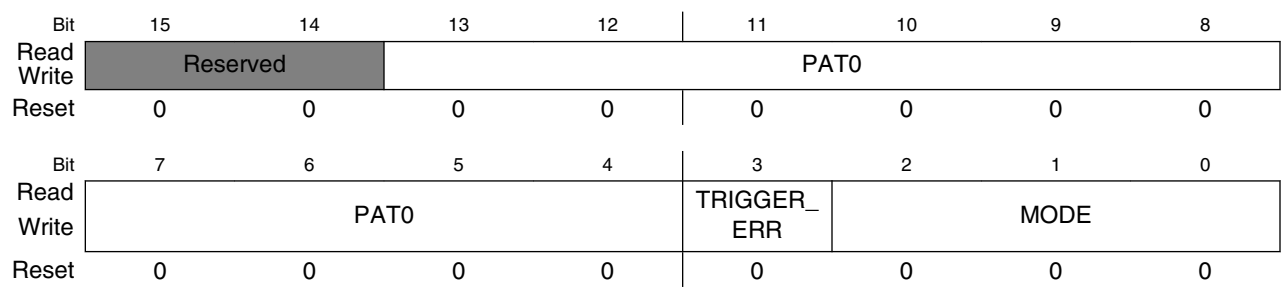


PCIE_PHY_TX_VMD_FSM_TX_VCM_DEBUG_OUT field descriptions

Field	Description
15–1 -	This field is reserved. Reserved
0 SHIFT_OUT	Current value from TX_ANAs configuration shift register.

49.5.47 PCIE_PHY_TX_LBERT_CTL

Address: 0h base + 1015h offset = 1015h



PCIE_PHY_TX_LBERT_CTL field descriptions

Field	Description
15–14 -	This field is reserved. Reserved
13–4 PAT0	Pattern for modes 3-5
3 TRIGGER_ERR	Insert a single error into a lsb Any write of a 1 to this bit will insert an error
MODE	Pattern to generate When changing modes, you must first change to disabled.

Table continues on the next page...

PCIE_PHY_TX_LBERT_CTL field descriptions (continued)

Field	Description
	6 DC-balanced word (PAT0) 5 Fixed word (PAT0) 4 lfsr7. X^7 + X^6 + 1 3 lfsr15. X^15 + X^14 + 1 2 lfsr23. X^23 + X^18 + 1 1 lfsr31. X^31 + X^28 + 1 0 Disabled

49.5.48 PCIE_PHY_RX_LBERT_CTL

Address: 0h base + 1016h offset = 1016h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				SYNC	MODE		
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_LBERT_CTL field descriptions

Field	Description
15–4 -	This field is reserved. Reserved
3 SYNC	Synchronize pattern matcher LFSR with incoming data A write of a one to this bit will reset the error counter and start a synchronization of the PM. There is no need to write this back to zero to run normally.
MODE	Pattern to match When changing modes, you must first change to disabled. 7 d[n] = 6 d[n] = !d[n-10] 5 d[n] = d[n-10] 4 lfsr7 : X^7 + X^6 + 1 3 lfsr15: X^15 + X^14 + 1 2 lfsr23. X^23 + X^18 + 1 1 lfsr31. X^31 + X^28 + 1 0 Disabled

49.5.49 PCIE_PHY_RX_LBERT_ERR

Address: 0h base + 1017h offset = 1017h

Bit	15	14	13	12	11	10	9	8
Read Write	OV14	COUNT						
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	COUNT							
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_LBERT_ERR field descriptions

Field	Description
15 OV14	If active, multiply COUNT by 128. If OV14=1 and COUNT=2^15-1, signals overflow of counter
COUNT	A read of this register, or a sync of the PM resets the error count. Current error count If OV14 field is active, then multiply count by 128

49.5.50 PCIE_PHY_RX_SCOPE_CTL

Address: 0h base + 1018h offset = 1018h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	Reserved													MODE		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_RX_SCOPE_CTL field descriptions

Field	Description
15–3 -	This field is reserved. Reserved
MODE	Sampling mode of counters. **NOTE:** WORD is 20 bits. 0 Off 1 Sample data every WORD *(1 + DELAY) bits 2 Sample data every WORD *(1 + DELAY) + 1 bits 3 Sample data every WORD *(1 + DELAY) + 2 bits 4 Sample data every clk and assert XOR and MASK increment

49.5.51 PCIE_PHY_RX_SCOPE_PHASE

Address: 0h base + 1019h offset = 1019h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved	BASE					SCOPE_DELAY	
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	SCOPE_ SEL	UPDATE	SAMPLE_PHASE					
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_SCOPE_PHASE field descriptions

Field	Description
15 -	This field is reserved. Reserved
14–10 BASE	which bit to sample when MODE = 1 or 4
9–8 SCOPE_DELAY	How many clocks to delay the analog scope_data.
7 SCOPE_SEL	Select sampling mode. 0 Before AFE sampling 1 After AFE sampling
6 UPDATE	Update Sampling phase. Write a 1.
SAMPLE_ PHASE	Sampling Phase

49.5.52 PCIE_PHY_RX_DPLL_FREQ

Address: 0h base + 101Ah offset = 101Ah

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved			VAL				
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	VAL							DTHR
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_DPLL_FREQ field descriptions

Field	Description
15–13 -	This field is reserved. Reserved
12–1 VAL	Freq is 1.526*VAL ppm from the reference When mpll_slow is set, the ppm is half the eqn above
0 DTHR	Bits below the useful resolution

49.5.53 PCIE_PHY_RX_CDR_CTL

Address: 0h base + 101Bh offset = 101Bh

Bit	15	14	13	12	11	10	9	8
Read Write	DTB_SEL				ALWAYS_ REALIGN	FAST_ START	FRUG_VALUE	
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	PHUG_VALUE		OVRD_ DPLL_GAIN	PHDET_ POL	PHDET_EDGE		PHDET_EN	
Reset	0	0	0	0	1	1	1	1

PCIE_PHY_RX_CDR_CTL field descriptions

Field	Description
15–12 DTB_SEL	Select to drive various signals onto the DTB. 0 disabled 1 pll_ana_rst,pll_count from rx_pwr_ctl 2 com_good_high/low from aligner 3 com_bad_high/low from aligner 4 shift_in_prog,ana_odd_data from aligner 5 Low bits of XAUI align FSM state
11 ALWAYS_ REALIGN	realign on any misaligned comma
10 FAST_START	decrease startup steps by 50%
9–8 FRUG_VALUE	override value for FRUG
7–6 PHUG_VALUE	override value for PHUG
5 OVRD_DPLL_ GAIN	Override PHUG and FRUG values
4 PHDET_POL	Reverse polarity of phase error

Table continues on the next page...

PCIE_PHY_RX_CDR_CTL field descriptions (continued)

Field	Description
3–2 PHDET_EDGE	Edges to use for phase detection. 11 Use both edges 10 Use rising edges only 01 Use falling edges only 00 Ignore all edges
PHDET_EN	Enables phase detecter. top bit is odd slicers, bottom is even

49.5.54 PCIE_PHY_RX_CDR_CDR_FSM_DEBUG

Address: 0h base + 101Ch offset = 101Ch

Bit	15	14	13	12	11	10	9	8
Read	adap_rx_eq			rx_eq_ctr			rx_ana_eq	
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	rx_ana_eq	adap_rx_ valid	cdr_en_ adap	cdr_en_eq	aligned	cdr_rx_valid	cdr_timeout	cdr_en
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_CDR_CDR_FSM_DEBUG field descriptions

Field	Description
15–13 adap_rx_eq	Equalization setting from adaptation FSM.
12–10 rx_eq_ctr	Initial centre point from equalization FSM.
9–7 rx_ana_eq	Equalization setting to Analog.
6 adap_rx_valid	Adaptation has completed and locked
5 cdr_en_adap	Adapatation loop is enabling the CDR.
4 cdr_en_eq	Equalization loop is enabling the CDR.
3 aligned	Datapath is bit-aligned.
2 cdr_rx_valid	CDR has locked to incoming data stream.

Table continues on the next page...

PCIE_PHY_RX_CDR_CDR_FSM_DEBUG field descriptions (continued)

Field	Description
1 cdr_timeout	CDR has not locked to datastream and has timed-out.
0 cdr_en	CDR has been enabled.

49.5.55 PCIE_PHY_RX_CDR_LOCK_VEC_OVRD

Address: 0h base + 101Dh offset = 101Dh

Bit	15	14	13	12	11	10	9	8
Read Write	adap_ctr_level					adap_ polarity	lock_vector_ ovrd	lock_vector_ en
Reset	1	0	0	0	0	0	0	0

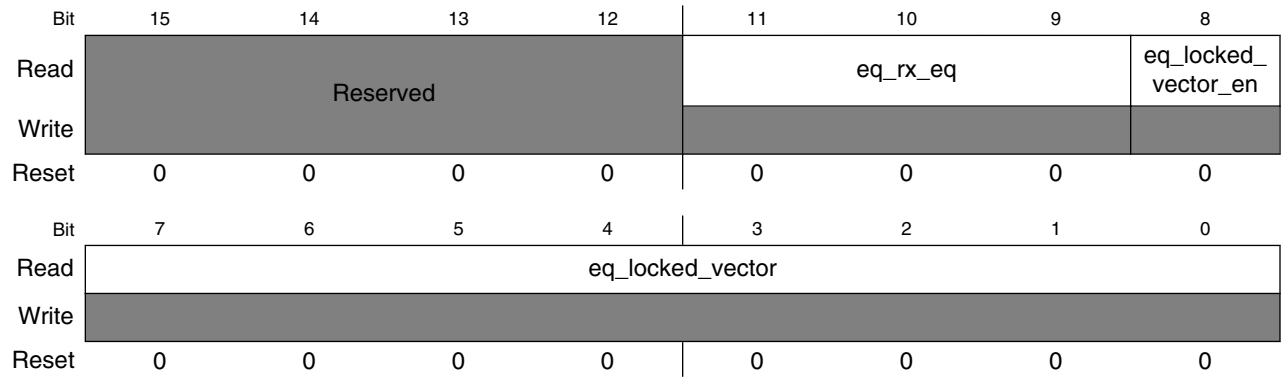
Bit	7	6	5	4	3	2	1	0
Read Write	lock_vector							
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_CDR_LOCK_VEC_OVRD field descriptions

Field	Description
15–11 adap_ctr_level	Amount of earlies that increment the adaptation counter (times 16).
10 adap_polarity	If asserted invert default adaptation adjustment for equalization. IF early decrease equalization. Normal mode is to decrease.
9 lock_vector_ovrd	Override enable for the rx_eq outputs.
8 lock_vector_en	Override value for the locked_vector output completion.
lock_vector	Override value for the locked_vector.

49.5.56 PCIE_PHY_RX_CDR_LOCK_VEC

Address: 0h base + 101Eh offset = 101Eh

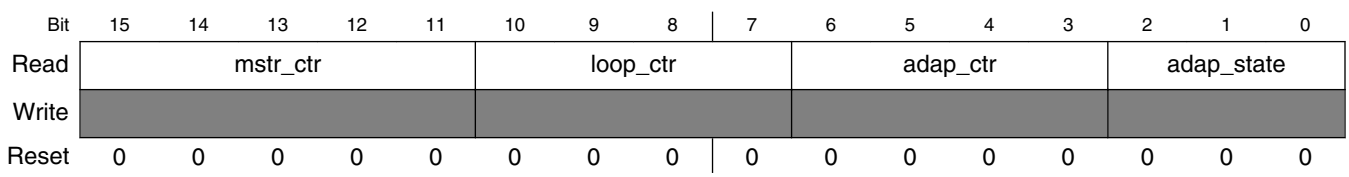


PCIE_PHY_RX_CDR_LOCK_VEC field descriptions

Field	Description
15–12 -	This field is reserved. Reserved
11–9 eq_rx_eq	Equalization setting from the Equalization Loop.
8 eq_locked_ vector_en	Equalization locked vector has been filled.
eq_locked_vector	Results of equalization loop.

49.5.57 PCIE_PHY_RX_CDR_ADAP_FSM

Address: 0h base + 101Fh offset = 101Fh



PCIE_PHY_RX_CDR_ADAP_FSM field descriptions

Field	Description
15–11 mstr_ctr	Master count register.
10–7 loop_ctr	Loop count register.
6–3 adap_ctr	Adaptation count register.

Table continues on the next page...

PCIE_PHY_RX_CDR_ADAP_FSM field descriptions (continued)

Field	Description
adap_state	Adaptation State. 000 ADAP_RESET 001 ADAP_LOCK 010 ADAP_SUFF 011 ADAP_LOOP 100 ADAP_MSTR 101 ADAP_DONE

49.5.58 PCIE_PHY_RX_ATB0

Address: 0h base + 1020h offset = 1020h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Reserved								EN_ATB	EN_ATB	EN_MARG	EN_ATB_RM_F	EN_ATB_RM_S	EN_ATB_RP_F	EN_ATB_RP_S	EN_ATB_VOFF
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_RX_ATB0 field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 EN_ATB	Enables ATB sensing and forcing on internal Rx nodes.
6 EN_ATB	Enables margining mode in receiver; requires atb_f_m to be high-Z!.
5 EN_MARG	Enables atb_force_p on negative-side termination resistor.
4 EN_ATB_RM_F	Enables atb_sense_m on negative-side termination resistor.
3 EN_ATB_RM_S	Enables atb_force_p on positive-side termination resistor.
2 EN_ATB_RP_F	Enables atb_sense_p on positive-side termination resistor.
1 EN_ATB_RP_S	Puts rxafe outputs vo_p on atb_s_p and vo_m on atb_s_m.
0 EN_ATB_VOFF	Puts rxafe voff_p on atb_s_p and voff_m on atb_s_m.

49.5.59 PCIE_PHY_RX_ATB1

Address: 0h base + 1021h offset = 1021h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	VLOS_MAX	VLOS_MIN	EN_ATB_ VLOS	EN_ATB_ VRF	MEAS_GD	MEAS_VP	EN_VLOS_ USB3	NC0
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_ATB1 field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 VLOS_MAX	Sets LOS reference voltage. (VLOS_MAX, VLOS_MIN): (1,1): None (1,0): Maximum (0,1): Minimum (0,0): Nominal
6 VLOS_MIN	Sets LOS reference voltage. (VLOS_MAX, VLOS_MIN): (1,1): None (1,0): Maximum (0,1): Minimum (0,0): Nominal
5 EN_ATB_VLOS	Enables sensing of LOS reference voltage on atb_sense_p.
4 EN_ATB_VRF	Enables sensing of vref_rx on atb_sense_p.
3 MEAS_GD	Enables sensing of local gd in Rx; ties gd to atb_sense_m.
2 MEAS_VP	Enables sensing of local vp in Rx; ties vp to atb_sense_p.
1 EN_VLOS_USB3	Enables LOS levels to be those for USB3; otherwise, PCI Express levels.
0 NC0	Enables/disables Rx termination resistor.

49.5.60 PCIE_PHY_RX_ENPWR0

Address: 0h base + 1022h offset = 1022h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	CTL_ RXPWRON	LCL_ RXPWRON	CTL_EN_ LOS	LCL_EN_ LOS	CTL_RXCK	LCL_RXCK	CTL_ACJT	LCL_ACJT
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_ENPWR0 field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 CTL_RXPWRON	Enables override of Rx block power.
6 LCL_RXPWRON	Enables/disables Rx slicers.
5 CTL_EN_LOS	Enables override of LOS block state.
4 LCL_EN_LOS	Enables/disables LOS block.
3 CTL_RXCK	Enables override of Rx clock circuit state.
2 LCL_RXCK	Enables/disables en_rx_clock (Rx clock enable).
1 CTL_ACJT	Enables override of ACJTAG block state.
0 LCL_ACJT	Enables/disables ACJTAG block.

49.5.61 PCIE_PHY_RX_PMIX_PHASE

Address: 0h base + 1023h offset = 1023h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	Reserved								PHASE							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_RX_PMIX_PHASE field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
PHASE	Write to bits 8-1 of the Phase Select register in the phase mixer.

49.5.62 PCIE_PHY_RX_ENPWR1

Address: 0h base + 1024h offset = 1024h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	LCL_ RXTERM	CTL_ RXTERM	LCL_BST			CTL_BST	LCL_ PHASE_ REG_RST	CTL_ PHASE_ REG_RST
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_ENPWR1 field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 LCL_RXTERM	Enables/disables Rx termination.
6 CTL_RXTERM	Enables override of rx_term_en.
5–3 LCL_BST	Rx boost (equalization) value
2 CTL_BST	Enables override of Rx boost (equalization) value.
1 LCL_PHASE_ REG_RST	Reset Phase register.
0 CTL_PHASE_ REG_RST	Enables override of Phase register reset.

49.5.63 PCIE_PHY_RX_ENPWR2

Address: 0h base + 1025h offset = 1025h

Bit	15	14	13	12	11	10	9	8
Read	Reserved							
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	EN_RXPMIX_TST	EN_RXPMIX_VPMIX	EN_RXPMIX_VRX	EN_RXPMIX_VOSC	EN_RXPMIX_FRC_VPMIX	RX_SCOPE_ATB_2	RX_SCOPE_ATB_1	RX_SCOPE_ATB_0
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_ENPWR2 field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 EN_RXPMIX_TST	Enables XOR gate to test linearity of Rx phase mixer using atb_s_p and atb_s_m.
6 EN_RXPMIX_VPMIX	Puts vreg_pmix on atb_s_p.
5 EN_RXPMIX_VRX	Puts vreg_rx on atb_s_p.
4 EN_RXPMIX_VOSC	Puts vreg_vosc on atb_s_p.
3 EN_RXPMIX_FRC_VPMIX	Instructs rx_pmix_vreg_pmix to use atb_s_m as a reference instead of vbg.
2 RX_SCOPE_ATB_2	Puts XOR of Rx scope PMIX input and output on atb_s_p.
1 RX_SCOPE_ATB_1	Puts Rx scope regulated VP on atb_s_p.
0 RX_SCOPE_ATB_0	Instructs Rx scope regulated VP to use atb_f_p as reference instead of VP.

49.5.64 PCIE_PHY_RX_SCOPE

Address: 0h base + 1026h offset = 1026h

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	NC_SCOPE_2			RX_ SCOPE_ SLEW	RX_ SCOPE_ FDIV20	NC_SCOPE_3		
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_RX_SCOPE field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7–5 NC_SCOPE_2	NC
4 RX_SCOPE_ SLEW	Sets high for low Rx clock frqeuencies (625 MHz) for Rx scope to work correctly.
3 RX_SCOPE_ FDIV20	Divides scope output clock by 20 instead of 10.
NC_SCOPE_3	NC

49.5.65 PCIE_PHY_TX_TXDRV_CNTRL

Address: 0h base + 102Bh offset = 102Bh

Bit	15	14	13	12	11	10	9	8
Read	Reserved							
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	PULL_DN_REG	PULL_UP_REG	OVRD_PULL_UP	VCM_HOLD_REG	OVRD_VCM_HOLD	Reserved	Reserved	Reserved
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_TXDRV_CNTRL field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 PULL_DN_REG	Register bit that causes the calibrated Tx bits to pull down in common mode fashion. If pull_dn_reg and tx_pull_up are both high, then pull_dn_reg wins (takes precedence").
6 PULL_UP_REG	Register override for tx_pull_up; selected when ovrd_pull_up is high; causes calibrated TX bits to pull up in common mode fashion, unless pull_dn_reg is high.
5 OVRD_PULL_UP	Selects loval value of pull_up_reg instead of tx_pull_up.
4 VCM_HOLD_REG	Register override for tx_vcm_hold; selected when ovrd_vcm_hold is high; controls the TX common mode hold circuitry.
3 OVRD_VCM_HOLD	Selects local value of vcm_hold_reg instead of tx_vcm_hold to control state of TX common mode hold circuitry.
2 NOCONN_8	This field is reserved. Reserved
1 NOCONN_7	This field is reserved. Reserved
0 NOCONN_6	This field is reserved. Reserved

49.5.66 PCIE_PHY_TX_POWER_CTL

Address: 0h base + 102Ch offset = 102Ch

Bit	15	14	13	12	11	10	9	8
Read	Reserved							
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	OVRD_EN	SERIAL_ EN_REG	CLK_EN_ REG	DATA_EN_ REG	REFGEN_ EN_REG	TX_DIV_ CLK_EN	REFGEN_ PDN_REG	Reserved
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_POWER_CTL field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 OVRD_EN	Enables local overrides for all signals in this register.
6 SERIAL_EN_ REG	Value for tx_serial_en when OVRD_EN is 1.
5 CLK_EN_REG	Value for tx_clk_en when OVRD_EN is 1.
4 DATA_EN_REG	Value for tx_data_en when OVRD_EN is 1.
3 REFGEN_EN_ REG	Register override value for tx_refgen_en; turns on the pmos_bias refgen block and the rxdetect comparators.
2 TX_DIV_CLK_ EN	Enables the div clock that is output from the Tx to the undersampler, more appropriately called tx_sampler_clk_en; this clock is output after the optional divide-by-2/ 4; tx_clk_en must be high to output a clock.
1 REFGEN_PDN_ REG	Value for refgen_pwdn when OVRD_EN is 1.
0 NOCONN_5	This field is reserved. Reserved

49.5.67 PCIE_PHY_TX_ALT_BLOCK

Address: 0h base + 102Dh offset = 102Dh

Bit	15	14	13	12	11	10	9	8
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read Write	EN_ALT_BUS	DRV_SOURCE_REG		JTAG_DATA_REG	ALT_OSC_VP	ALT_OSC_VPH	ALT_OSC_VPHREG	OVRD_ALT_BUS
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_ALT_BLOCK field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 EN_ALT_BUS	Enables the Tx for alt bus mode, powers up the pmos_bias block, and so on; required if manually running the alt bus features.
6–5 DRV_SOURCE_REG	Value for tx_data_source when OVRD_ALT_BUS is 1 11 JTAG data common mode for test 10 LFPS oscillator differential 01 JTAG data differential 00 Serializer data or alt oscillator vp/vph/vphreg/vptx if selected
4 JTAG_DATA_REG	Value for jtag_data when OVRD_ALT_BUS is 1.
3 ALT_OSC_VP	Enables and connects the vp oscillator to the transmit pins; must set drv_source_reg bus correctly.
2 ALT_OSC_VPH	Enables and connects the vph oscillator to the transmit pins; must set drv_source_reg bus correctly.
1 ALT_OSC_VPHREG	Enables and connects the vphreg oscillator to the transmit pins; must set drv_source_reg bus correctly.
0 OVRD_ALT_BUS	Enables local overrides for alt-bus control signals.

49.5.68 PCIE_PHY_TX_ALT_AND_LOOPBACK

Address: 0h base + 102Eh offset = 102Eh

Bit	15	14	13	12	11	10	9	8
Read	Reserved							
Write								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	OVRD_TX_LB	TX_LB_EN_REG	ALT_VPTX_OSC	Reserved	Reserved	Reserved	Reserved	Reserved
Write								
Reset	0	0	0	0	0	0	0	0

PCIE_PHY_TX_ALT_AND_LOOPBACK field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 OVRD_TX_LB	Enables the override of the tx_lb_en pin.
6 TX_LB_EN_REG	Value of the tx_lb_en pin when OVRD_TX_LB is enabled.
5 ALT_VPTX_OSC	Enables and connects the vptx oscillator to the transmit pins; must set drv_source_reg bus correctly.
4 NOCONN_04	This field is reserved. Reserved
3 NOCONN_03	This field is reserved. Reserved
2 NOCONN_02	This field is reserved. Reserved
1 NOCONN_01	This field is reserved. Reserved
0 NOCONN_00	This field is reserved. Reserved

49.5.69 PCIE_PHY_TX_TX_ATB_REG

Address: 0h base + 102Fh offset = 102Fh

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Reserved								ATB_PBIAS	ATB_VCM_REP	ATB_RXDETREF	ATB_TXFP	ATB_TXFM	ATB_TXSP	ATB_TXSM	ATB_VCM
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PHY_TX_TX_ATB_REG field descriptions

Field	Description
15–8 -	This field is reserved. Reserved
7 ATB_PBIAS	Connects real pmos_bias voltage for Tx PMOS driver pull-up path to atb_s_p and local ground at the pmos_bias block to atb_s_m.
6 ATB_VCM_REP	Connects common mode replica voltage in pmos_bias block to atb_s_p and local ground to atb_s_m.
5 ATB_RXDETREF	Connects Rx detect block reference voltage to atb_s_p and local ground to atb_s_m.
4 ATB_TXFP	Connects tx_p to atb_f_p.
3 ATB_TXFM	Connects tx_m to atb_f_m.
2 ATB_TXSP	Connects tx_p to atb_s_p.
1 ATB_TXSM	Connects tx_m to atb_s_m.
0 ATB_VCM	Connects tx_p/tx_m common mode voltage onto atb_s_p and local ground onto atb_s_m.