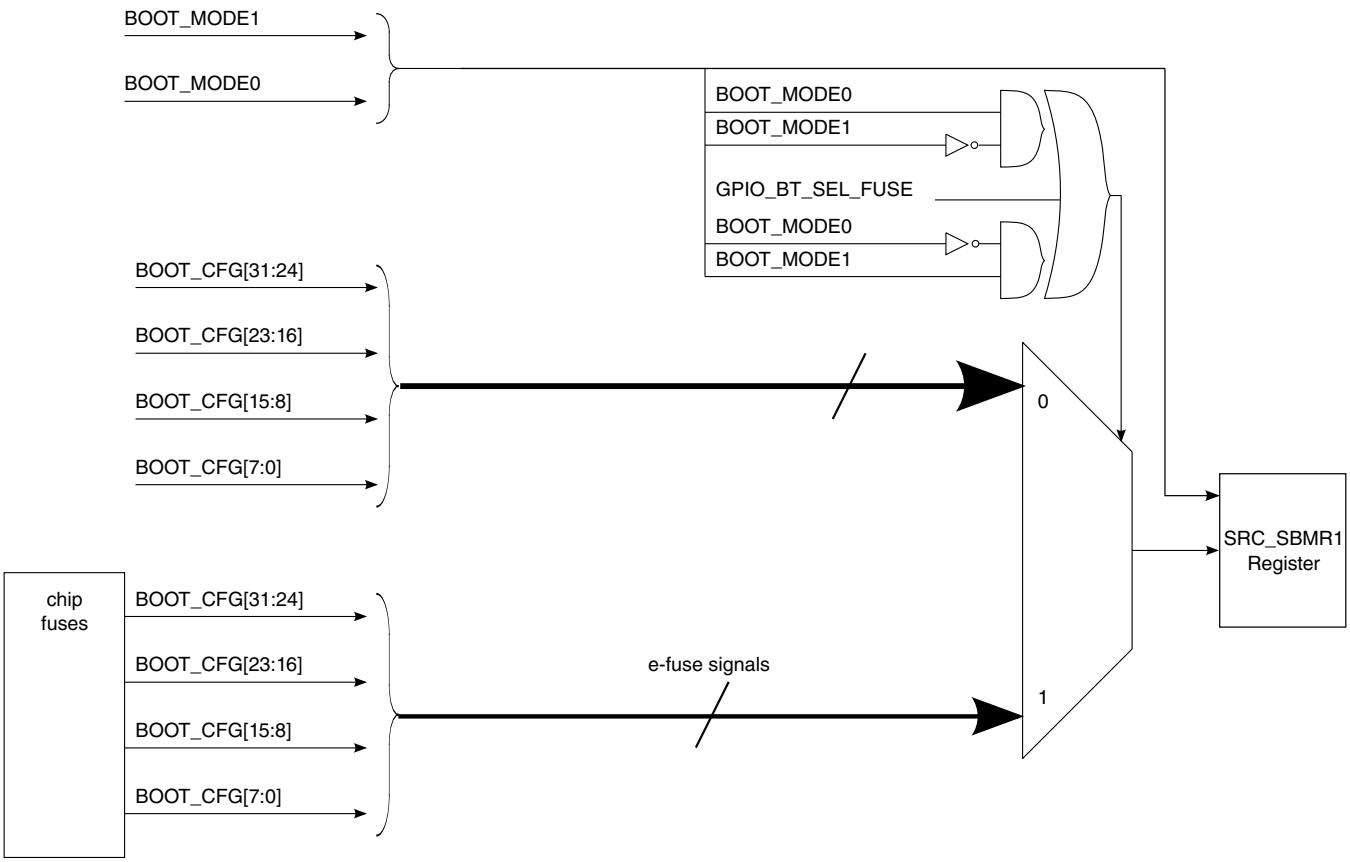


Figure 60-6. Boot mode information

60.7 SRC Memory Map/Register Definition

SRC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
20D_8000	SRC Control Register (SRC_SCR)	32	R/W	0000_0521h	60.7.1/5070
20D_8004	SRC Boot Mode Register 1 (SRC_SBMR1)	32	R	0000_0000h	60.7.2/5074
20D_8008	SRC Reset Status Register (SRC_SRSR)	32	R/W	0000_0001h	60.7.3/5075
20D_8014	SRC Interrupt Status Register (SRC_SISR)	32	R	0000_0000h	60.7.4/5077
20D_8018	SRC Interrupt Mask Register (SRC_SIMR)	32	R/W	0000_001Fh	60.7.5/5079
20D_801C	SRC Boot Mode Register 2 (SRC_SBMR2)	32	R	0000_0000h	60.7.6/5080
20D_8020	SRC General Purpose Register 1 (SRC_GPR1)	32	R/W	0000_0000h	60.7.7/5081
20D_8024	SRC General Purpose Register 2 (SRC_GPR2)	32	R/W	0000_0000h	60.7.8/5081
20D_8028	SRC General Purpose Register 3 (SRC_GPR3)	32	R/W	0000_0000h	60.7.9/5082

Table continues on the next page...

SRC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
20D_802C	SRC General Purpose Register 4 (SRC_GPR4)	32	R/W	0000_0000h	60.7.10/ 5082
20D_8030	SRC General Purpose Register 5 (SRC_GPR5)	32	R/W	0000_0000h	60.7.11/ 5082
20D_8034	SRC General Purpose Register 6 (SRC_GPR6)	32	R/W	0000_0000h	60.7.12/ 5083
20D_8038	SRC General Purpose Register 7 (SRC_GPR7)	32	R/W	0000_0000h	60.7.13/ 5083
20D_803C	SRC General Purpose Register 8 (SRC_GPR8)	32	R/W	0000_0000h	60.7.14/ 5083
20D_8040	SRC General Purpose Register 9 (SRC_GPR9)	32	R/W	0000_0000h	60.7.15/ 5084
20D_8044	SRC General Purpose Register 10 (SRC_GPR10)	32	R/W	0000_0000h	60.7.16/ 5085

60.7.1 SRC Control Register (SRC_SCR)

The Reset control register (SCR), contains bits that control operation of the reset controller.

Address: 20D_8000h base + 0h offset = 20D_8000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0						dbg_rst_msk_pg	core3_enable	core2_enable	core1_enable	cores_dbg_rst	core3_dbg_rst	core2_dbg_rst	core1_dbg_rst	core0_dbg_rst	core3_rst
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	core2_rst	core1_rst	core0_rst	sw_ipu2_rst	eim_rst	mask_wdog_rst				warm_rst_ bypass_ count		sw_open_vg_rst	sw_ipu1_rst	sw_ vpu_ rst	sw_ gpu_ rst	warm_reset_ enable
W																
Reset	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1

SRC_SCR field descriptions

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.
25 dbg_rst_msk_pg	Do not assert debug resets after power gating event of core 0 do not mask core debug resets (debug resets will be asserted after power gating event) 1 mask core debug resets (debug resets won't be asserted after power gating event)
24 core3_enable	core3 enable. **NOTE:** core0 cannot be disabled 0 core3 is disabled 1 core3 is enabled
23 core2_enable	core2 enable. **NOTE:** core0 cannot be disabled 0 core2 is disabled 1 core2 is enabled
22 core1_enable	core1 enable. **NOTE:** core0 cannot be disabled 0 core1 is disabled 1 core1 is enabled
21 cores_dbg_rst	Software reset for debug of arm platform only. **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. 0 do not assert arm platform debug reset 1 assert arm platform debug reset
20 core3_dbg_rst	Software reset for core3 debug only. **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. 0 do not assert core3 debug reset 1 assert core3 debug reset
19 core2_dbg_rst	Software reset for core2 debug only. **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. 0 do not assert core2 debug reset 1 assert core2 debug reset
18 core1_dbg_rst	Software reset for core1 debug only. **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. 0 do not assert core1 debug reset 1 assert core1 debug reset

Table continues on the next page...

SRC_SCR field descriptions (continued)

Field	Description
17 core0_dbg_rst	Software reset for core0 debug only. **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. 0 do not assert core0 debug reset 1 assert core0 debug reset
16 core3_rst	Software reset for core3 only. **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. 0 do not assert core3 reset 1 assert core3 reset
15 core2_rst	Software reset for core2 only. **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. 0 do not assert core2 reset 1 assert core2 reset
14 core1_rst	Software reset for core1 only. **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. 0 do not assert core1 reset 1 assert core1 reset
13 core0_rst	Software reset for core0 only. **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. 0 do not assert core0 reset 1 assert core0 reset
12 sw_ipu2_rst	Software reset for ipu2 **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. Software can determine that the reset has finished once this bit is cleared. Software can also configure SRC to generate interrupt once the software has finished. Please refer to SRC_SISR register for details. 0 do not assert ipu2 reset 1 assert ipu2 reset
11 eim_rst	EIM reset is needed in order to reconfigure the eim chip select. The software reset bit must de-asserted. The eim chip select configuration should be updated. The software bit must be re-asserted since this is not self-refresh.
10–7 mask_wdog_rst	Mask wdog_rst_b source. If these 4 bits are coded from A to 5 then, the wdog_rst_b input to SRC will be masked and the wdog_rst_b will not create a reset to the chip.

Table continues on the next page...

SRC_SCR field descriptions (continued)

Field	Description
	NOTE: During the time the WDOG event is masked using SRC logic, it is likely that the WDOG Reset Status Register (WRSR) bit 1 (which indicates a WDOG timeout event) will get asserted. software / OS developer must prepare for this case. Re-enabling the WDOG is possible, by un-masking it in SRC, though it must be preceded by servicing the WDOG. However, for the case that the event has been asserted, the status bit (WRSR bit-1) will remain asserted, regardless of servicing the WDOG module. (Hardware reset is the only way to cause the de-assertion of that bit). any other code will be coded to 1010 i.e. wdog_rst_b is not masked 0101 wdog_rst_b is masked 1010 wdog_rst_b is not masked (default)
6–5 warm_rst_ bypass_count	Defines the XTALI cycles to count before bypassing the MMDC acknowledge for WARM reset. If the MMDC acknowledge will not be asserted before this counter has elapsed, then a COLD reset will be initiated. 00 Counter not to be used - system will wait until MMDC acknowledge until it is asserted. 01 Wait 16 XTALI cycles before changing WARM reset to a COLD reset. 10 Wait 32 XTALI cycles before changing WARM reset to a COLD reset. 11 Wait 64 XTALI cycles before changing WARM reset to a COLD reset
4 sw_open_vg_rst	Software reset for open_vg **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. Software can determine that the reset has finished once this bit is cleared. Software can also configure SRC to generate interrupt once the software has finished. Please refer to SRC_SISR register for details. **NOTE:** The reset process will involve 8 open_vg cycles before negating the open_vg reset, to allow reset assertion to propagate into open_vg. 0 do not assert open_vg reset 1 assert open_vg reset
3 sw_ipu1_rst	Software reset for IPU1 **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. Software can determine that the reset has finished once this bit is cleared. Software can also configure SRC to generate interrupt once the software has finished. Please refer to SRC_SISR register for details. 0 do not assert IPU1 reset 1 assert IPU1 reset
2 sw_vpu_rst	Software reset for VPU **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. Software can determine that the reset has finished once this bit is cleared. Software can also configure SRC to generate interrupt once the software has finished. Please refer to SRC_SISR register for details. **NOTE:** The reset process will involve 8 VPU cycles before negating the VPU reset, to allow reset assertion to propagate into VPU. 0 do not assert VPU reset 1 assert VPU reset

Table continues on the next page...

SRC_SCR field descriptions (continued)

Field	Description
1 sw_gpu_rst	Software reset for GPU **NOTE:** This is a self clearing bit. Once it is set to 1, the reset process will begin, and once it finishes, this bit will be self cleared. Software can determine that the reset has finished once this bit is cleared. Software can also configure SRC to generate interrupt once the software has finished. Please refer to SRC_SISR register for details. **NOTE:** The reset process will involve 8 GPU cycles before negating the GPU reset, to allow reset assertion to propagate into GPU. 0 do not assert GPU reset 1 assert GPU reset
0 warm_reset_ enable	WARM reset enable bit. WARM reset will be enabled only if warm_reset_enable bit is set. Otherwise all WARM reset sources will generate COLD reset. 0 WARM reset disabled 1 WARM reset enabled

60.7.2 SRC Boot Mode Register 1 (SRC_SBMR1)

The Boot Mode register (SBMR) contains bits that reflect the status of Boot Mode Pins of the chip. The reset value is configuration dependent (depending on boot/fuses/IO pads).

Address: 20D_8000h base + 4h offset = 20D_8004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BOOT_CFG4[7:0]								BOOT_CFG3[7:0]								BOOT_CFG2[7:0]								BOOT_CFG1[7:0]							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRC_SBMR1 field descriptions

Field	Description
31–24 BOOT_ CFG4[7:0]	Refer to fusemap.
23–16 BOOT_ CFG3[7:0]	Refer to fusemap.
15–8 BOOT_ CFG2[7:0]	Refer to fusemap.
BOOT_ CFG1[7:0]	Refer to fusemap.

60.7.3 SRC Reset Status Register (SRC_SRSR)

The SRSR is a write to one clear register which records the source of the reset events for the chip. The SRC reset status register will capture all the reset sources that have occurred. This register is reset on ipp_reset_b. This is a read-write register.

For bit[6-0] - writing zero does not have any effect. Writing one will clear the corresponding bit. The individual bits can be cleared by writing one to that bit. When the system comes out of reset, this register will have bits set corresponding to all the reset sources that occurred during system reset. Software has to take care to clear this register by writing one after every reset that occurs so that the register will contain the information of recently occurred reset.

Address: 20D_8000h base + 8h offset = 20D_8008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															warm_boot
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

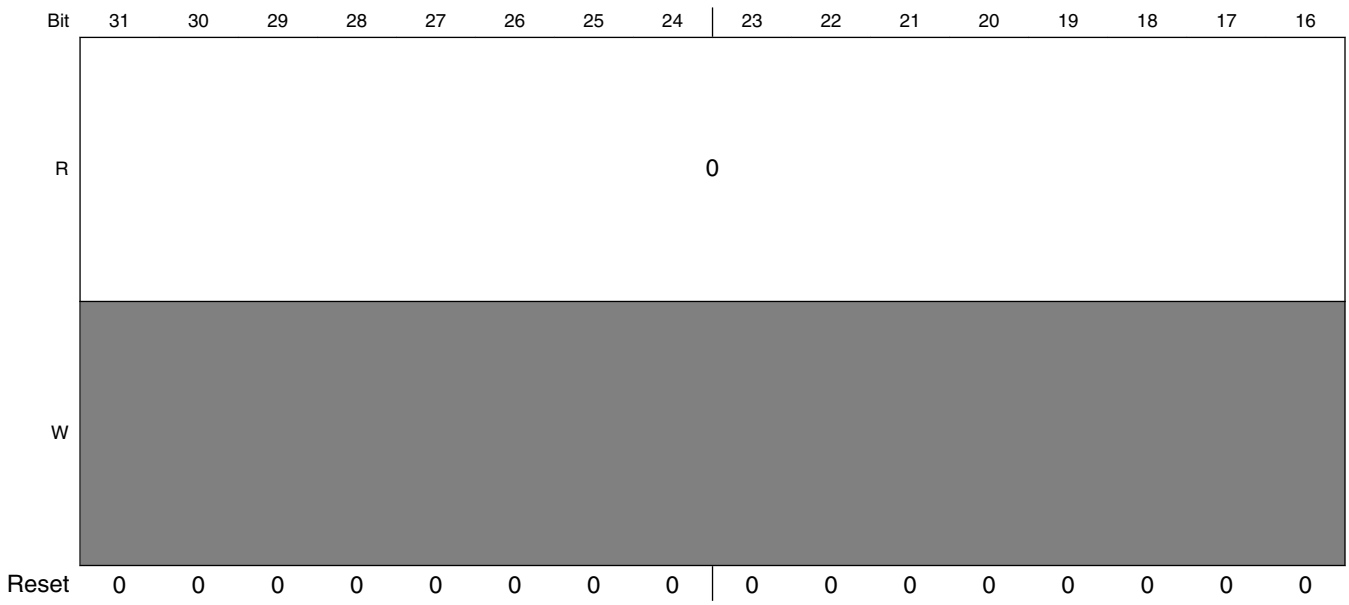
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0									jtag_sw_rst	jtag_rst_b	wdog_rst_b	ipp_user_reset_b	csu_reset_b	0	ipp_reset_b
W										w1c	w1c	w1c	w1c	w1c		w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

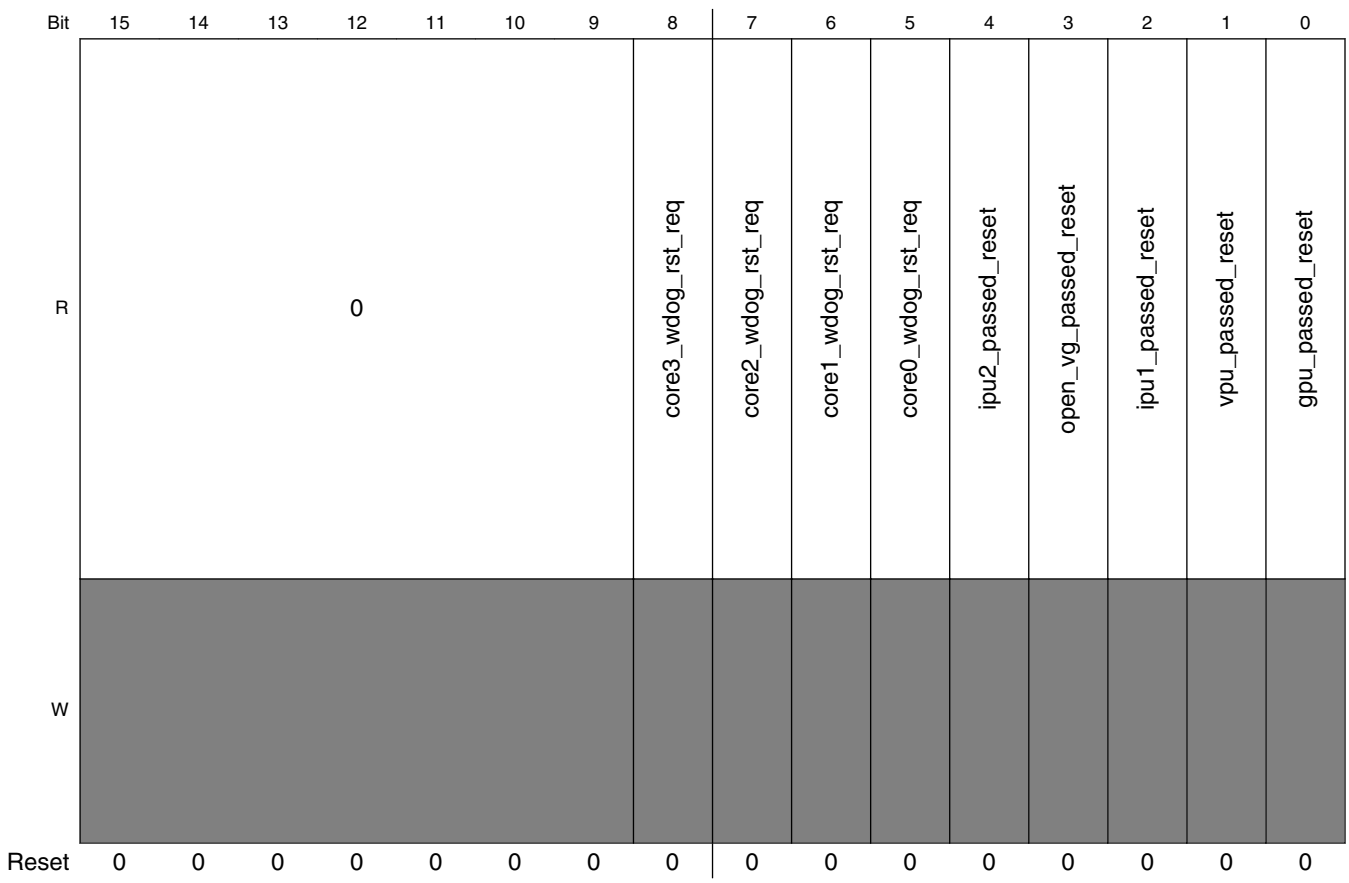
SRC_SRSR field descriptions

Field	Description
31–17 Reserved	This read-only field is reserved and always has the value 0.
16 warm_boot	WARM boot indication shows that WARM boot was initiated by software. This indicates to the software that it saved the needed information in the memory before initiating the WARM reset. In this case, software will set this bit to '1', before initiating the WARM reset. The warm_boot bit should be used as indication only after a warm_reset sequence. Software should clear this bit after warm_reset to indicate that the next warm_reset is not performed with warm_boot. Please refer to Reset Sequence and De-Assertion for details on warm_reset. 0 WARM boot process not initiated by software. 1 WARM boot initiated by software.
15–7 Reserved	This read-only field is reserved and always has the value 0.
6 jtag_sw_rst	JTAG software reset. Indicates whether the reset was the result of software reset from JTAG. 0 Reset is not a result of software reset from JTAG. 1 Reset is a result of software reset from JTAG.
5 jtag_rst_b	HIGH - Z JTAG reset. Indicates whether the reset was the result of HIGH-Z reset from JTAG. 0 Reset is not a result of HIGH-Z reset from JTAG. 1 Reset is a result of HIGH-Z reset from JTAG.
4 wdog_rst_b	IC Watchdog Time-out reset. Indicates whether the reset was the result of the watchdog time-out event. 0 Reset is not a result of the watchdog time-out event. 1 Reset is a result of the watchdog time-out event.
3 ipp_user_reset_b	Indicates whether the reset was the result of the ipp_user_reset_b qualified reset. 0 Reset is not a result of the ipp_user_reset_b qualified as COLD reset event. 1 Reset is a result of the ipp_user_reset_b qualified as COLD reset event.
2 csu_reset_b	Indicates whether the reset was the result of the csu_reset_b input. **NOTE:** If case the csu_reset_b occurred during a WARM reset process, during the phase that ipg_clk is not available yet, then the occurrence of CSU reset will not be reflected in this bit. 0 Reset is not a result of the csu_reset_b event. 1 Reset is a result of the csu_reset_b event.
1 Reserved	This read-only field is reserved and always has the value 0.
0 ipp_reset_b	Indicates whether reset was the result of ipp_reset_b pin (Power-up sequence) 0 Reset is not a result of ipp_reset_b pin. 1 Reset is a result of ipp_reset_b pin.

60.7.4 SRC Interrupt Status Register (SRC_SISR)

Address: 20D_8000h base + 14h offset = 20D_8014h



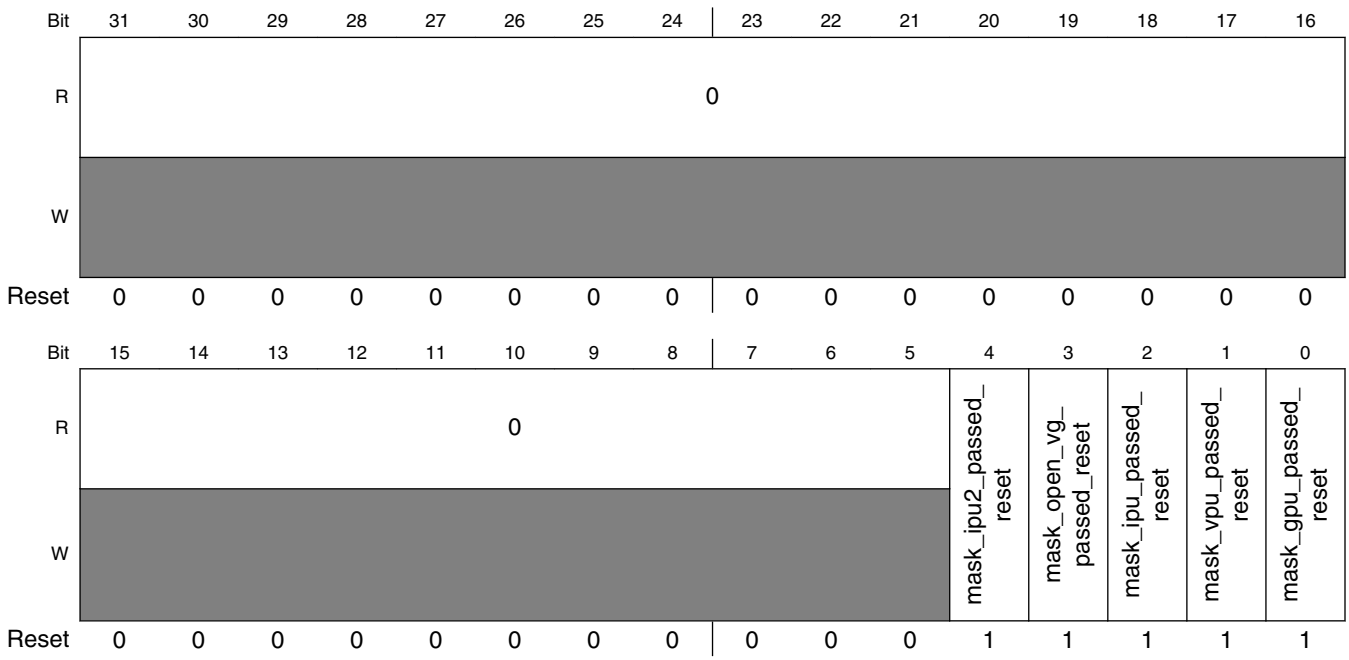


SRC_SISR field descriptions

Field	Description
31–9 Reserved	This read-only field is reserved and always has the value 0.
8 core3_wdog_rst_req	WDOG reset request from core3. Read-only status bit.
7 core2_wdog_rst_req	WDOG reset request from core2. Read-only status bit.
6 core1_wdog_rst_req	WDOG reset request from core1. Read-only status bit.
5 core0_wdog_rst_req	WDOG reset request from core0. Read-only status bit.
4 ipu2_passed_reset	Interrupt generated to indicate that ipu2 passed software reset and is ready to be used 0 interrupt generated not due to ipu2 passed reset 1 interrupt generated due to ipu2 passed reset
3 open_vg_passed_reset	Interrupt generated to indicate that open_vg passed software reset and is ready to be used 0 interrupt generated not due to open_vg passed reset 1 interrupt generated due to open_vg passed reset
2 ipu1_passed_reset	Interrupt generated to indicate that ipu passed software reset and is ready to be used 0 interrupt generated not due to ipu passed reset 1 interrupt generated due to ipu passed reset
1 vpu_passed_reset	Interrupt generated to indicate that VPU passed software reset and is ready to be used 0 interrupt generated not due to VPU passed reset 1 interrupt generated due to VPU passed reset
0 gpu_passed_reset	Interrupt generated to indicate that GPU passed software reset and is ready to be used 0 interrupt generated not due to GPU passed reset 1 interrupt generated due to GPU passed reset

60.7.5 SRC Interrupt Mask Register (SRC_SIMR)

Address: 20D_8000h base + 18h offset = 20D_8018h



SRC_SIMR field descriptions

Field	Description
31–5 Reserved	This read-only field is reserved and always has the value 0.
4 mask_ipu2_passed_reset	mask interrupt generation due to ipu2 passing reset 0 do not mask interrupt due to ipu2 passed reset - interrupt will be created 1 mask interrupt due to ipu2 passed reset
3 mask_open_vg_passed_reset	mask interrupt generation due to open_vg passed reset 0 do not mask interrupt due to open_vg passed reset - interrupt will be created 1 mask interrupt due to open_vg passed reset
2 mask_ipu_passed_reset	mask interrupt generation due to ipu passed reset 0 do not mask interrupt due to ipu passed reset - interrupt will be created 1 mask interrupt due to ipu passed reset
1 mask_vpu_passed_reset	mask interrupt generation due to VPU passed reset 0 do not mask interrupt due to VPU passed reset - interrupt will be created 1 mask interrupt due to VPU passed reset
0 mask_gpu_passed_reset	mask interrupt generation due to GPU passed reset 0 do not mask interrupt due to GPU passed reset - interrupt will be created 1 mask interrupt due to GPU passed reset

60.7.6 SRC Boot Mode Register 2 (SRC_SBMR2)

The Boot Mode register (SBMR), contains bits that reflect the status of Boot Mode Pins of the chip. The default values for those bits depends on the values of pins/fuses during reset sequence, hence the question mark on their default value.

Address: 20D_8000h base + 1Ch offset = 20D_801Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0						BMOD[1:0]		0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0											BT_FUSE_SEL	DIR_BT_DIS	0	SEC_CONFIG[1:0]	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRC_SBMR2 field descriptions

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.
25–24 BMOD[1:0]	BMOD[1:0] shows the latched state of the BOOT_MODE1 and BOOT_MODE0 signals on the rising edge of POR_B. See the Boot mode pin settings section of System Boot.
23–5 Reserved	This read-only field is reserved and always has the value 0.
4 BT_FUSE_SEL	BT_FUSE_SEL (connected to gpio bt_fuse_sel) shows the state of the BT_FUSE_SEL fuse. See Fusemap for additional information on this fuse.
3 DIR_BT_DIS	DIR_BT_DIS shows the state of the DIR_BT_DIS fuse. See Chapter 5, Fusemap for additional information on this fuse.
2 Reserved	This read-only field is reserved and always has the value 0.
SEC_ CONFIG[1:0]	SECONFIG[1] shows the state of the SECONFIG[1] fuse. See Fusemap for additional information on this fuse. SECONFIG[0] shows the state of the SECONFIG[0] fuse. This fuse is shown as reserved in Fusemap (address 0x440[1]) because it does not have a user-relevant function.

60.7.7 SRC General Purpose Register 1 (SRC_GPR1)

Address: 20D_8000h base + 20h offset = 20D_8020h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PERSISTENT_ENTRY0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRC_GPR1 field descriptions

Field	Description
PERSISTENT_ ENTRY0	Holds entry function for core0 for waking-up from low power mode. The SRC ensures that the register value will persist across system resets.

60.7.8 SRC General Purpose Register 2 (SRC_GPR2)

Address: 20D_8000h base + 24h offset = 20D_8024h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PERSISTENT_ARG0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRC_GPR2 field descriptions

Field	Description
PERSISTENT_ ARG0	Holds argument of entry function for core0 for waking-up from low power mode. The SRC ensures that the register value will persist across system resets.

60.7.9 SRC General Purpose Register 3 (SRC_GPR3)

Address: 20D_8000h base + 28h offset = 20D_8028h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PERSISTENT_ENTRY1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRC_GPR3 field descriptions

Field	Description
PERSISTENT_ENTRY1	Holds entry function for core1. The SRC ensures that the register value will persist across system resets.

60.7.10 SRC General Purpose Register 4 (SRC_GPR4)

Address: 20D_8000h base + 2Ch offset = 20D_802Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PERSISTENT_ARG1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRC_GPR4 field descriptions

Field	Description
PERSISTENT_ARG1	Holds argument of entry function for core1. The SRC ensures that the register value will persist across system resets.

60.7.11 SRC General Purpose Register 5 (SRC_GPR5)

Address: 20D_8000h base + 30h offset = 20D_8030h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PERSISTENT_ENTRY2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRC_GPR5 field descriptions

Field	Description
PERSISTENT_ENTRY2	Holds entry function for core2 (i.MX 6Quad only). The SRC ensures that the register value will persist across system resets.

60.7.12 SRC General Purpose Register 6 (SRC_GPR6)

Address: 20D_8000h base + 34h offset = 20D_8034h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PERSISTENT_ARG2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRC_GPR6 field descriptions

Field	Description
PERSISTENT_ARG2	Holds argument of entry function for core2 (i.MX 6Quad only). The SRC ensures that the register value will persist across system resets.

60.7.13 SRC General Purpose Register 7 (SRC_GPR7)

Address: 20D_8000h base + 38h offset = 20D_8038h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PERSISTENT_ENTRY3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRC_GPR7 field descriptions

Field	Description
PERSISTENT_ENTRY3	Holds entry function for core3 (i.MX 6Quad only). The SRC ensures that the register value will persist across system resets.

60.7.14 SRC General Purpose Register 8 (SRC_GPR8)

Address: 20D_8000h base + 3Ch offset = 20D_803Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PERSISTENT_ARG3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

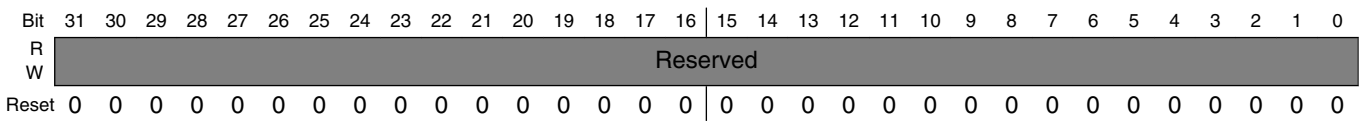
SRC_GPR8 field descriptions

Field	Description
PERSISTENT_ARG3	Holds argument of entry function for core3 (i.MX 6Quad only). The SRC ensures that the register value will persist across system resets.

60.7.15 SRC General Purpose Register 9 (SRC_GPR9)

Reserved for Internal Use.

Address: 20D_8000h base + 40h offset = 20D_8040h

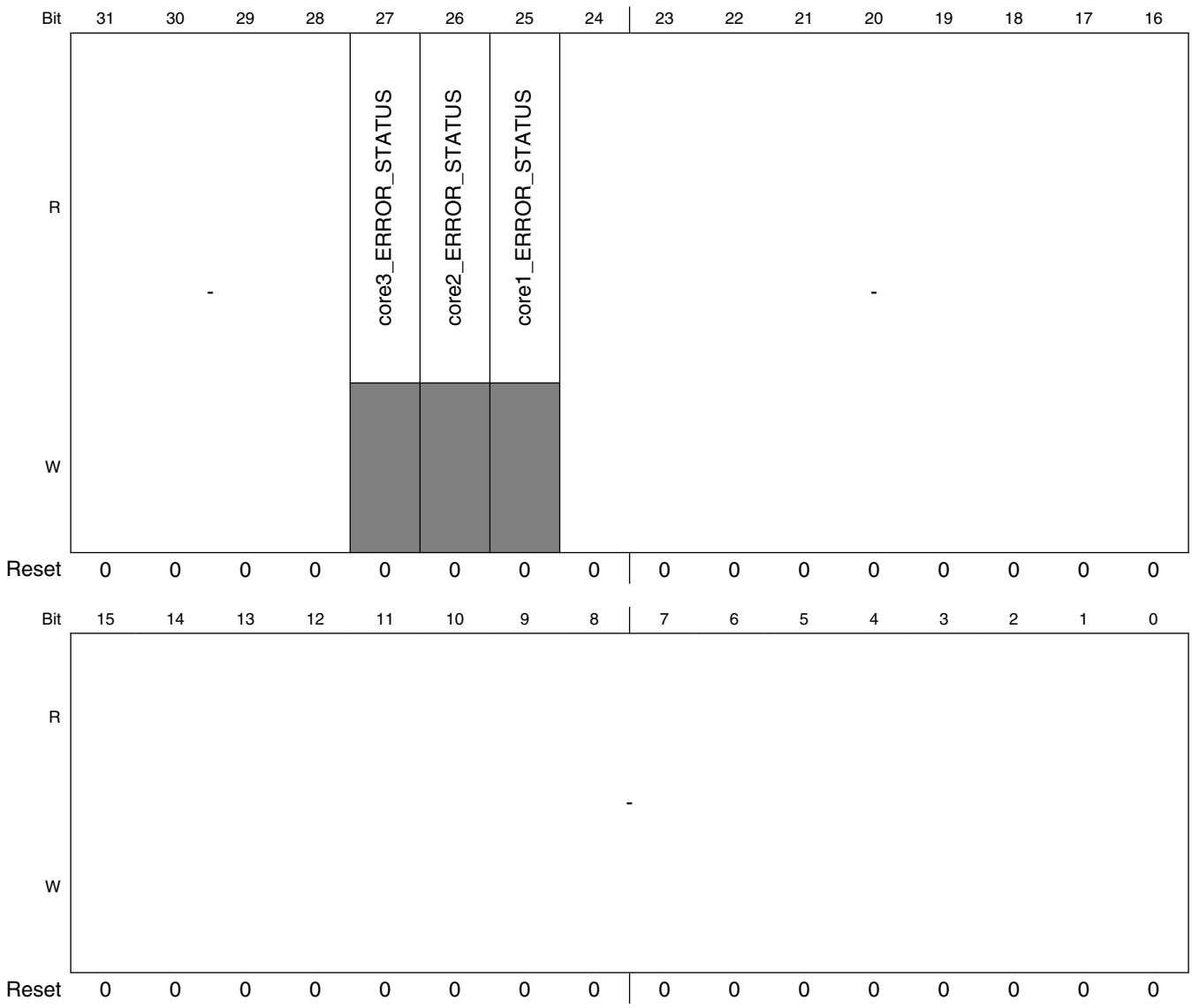


SRC_GPR9 field descriptions

Field	Description
-	This field is reserved. Reserved.

60.7.16 SRC General Purpose Register 10 (SRC_GPR10)

Address: 20D_8000h base + 44h offset = 20D_8044h



SRC_GPR10 field descriptions

Field	Description
31–28 -	Read/write bit, for general purpose **NOTE:** Reset only by POR
27 core3_ERROR_ STATUS	core3 error status bit (i.MX 6Quad Only).

Table continues on the next page...

SRC_GPR10 field descriptions (continued)

Field	Description
26 core2_ERROR_ STATUS	core2 error status bit (i.MX 6Quad Only).
25 core1_ERROR_ STATUS	core1 error status bit.
-	Read/write bits, for general purpose **NOTE:** Reset only by POR