27.8 GPC Memory Map/Register Definition

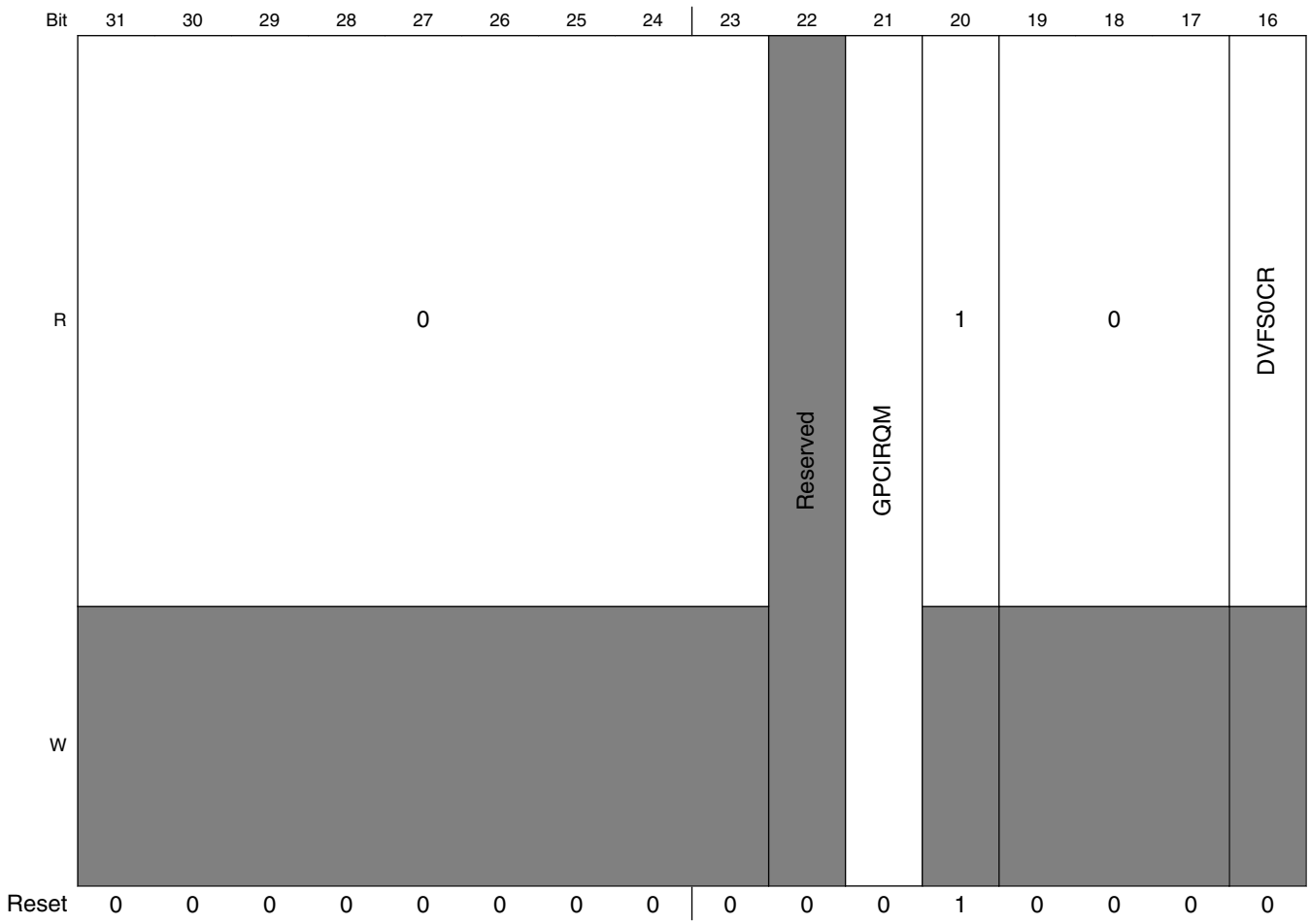
Detailed descriptions of each register can be found below.

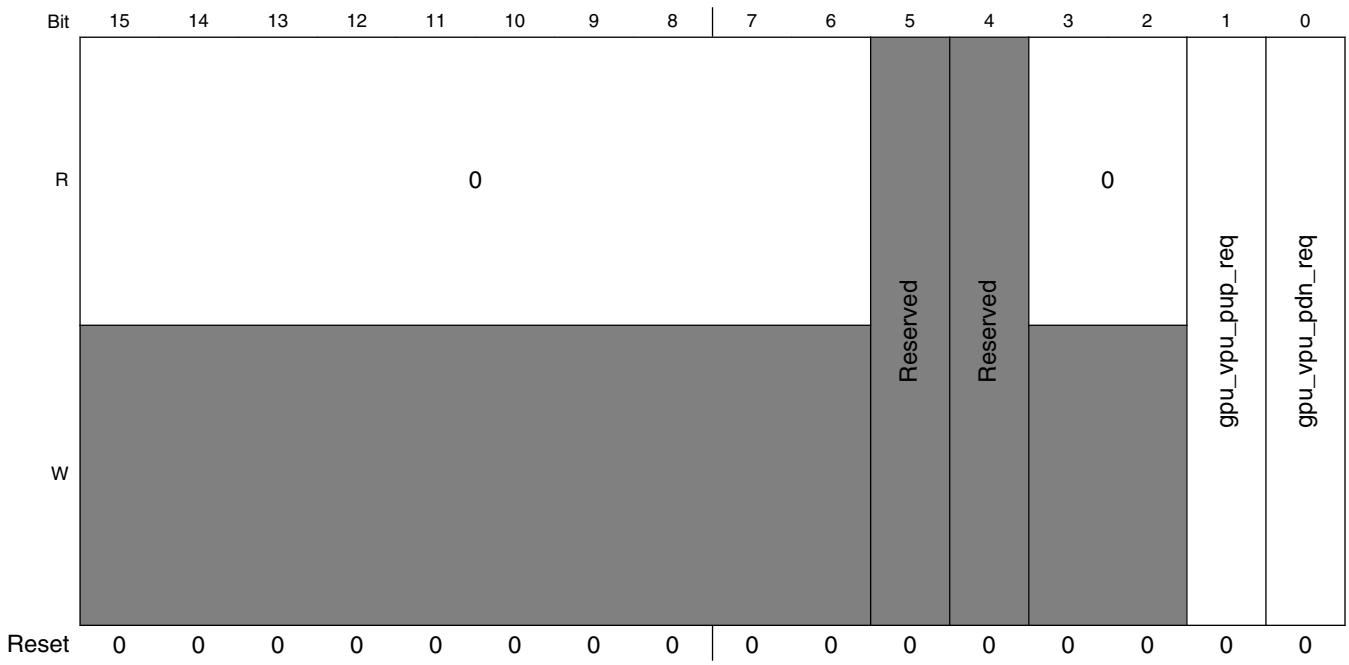
GPC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
20D_C000	GPC Interface control register (GPC_CNTR)	32	R/W	0010_0000h	27.8.1/1379
20D_C004	GPC Power Gating Register (GPC_PGR)	32	R/W	0000_0000h	27.8.2/1382
20D_C008	IRQ masking register 1 (GPC_IMR1)	32	R/W	0000_0000h	27.8.3/1382
20D_C00C	IRQ masking register 2 (GPC_IMR2)	32	R/W	0000_0000h	27.8.4/1383
20D_C010	IRQ masking register 3 (GPC_IMR3)	32	R/W	0000_0000h	27.8.5/1383
20D_C014	IRQ masking register 4 (GPC_IMR4)	32	R/W	0000_0000h	27.8.6/1383
20D_C018	IRQ status resister 1 (GPC_ISR1)	32	R	0000_0000h	27.8.7/1384
20D_C01C	IRQ status resister 2 (GPC_ISR2)	32	R	0000_0000h	27.8.8/1384
20D_C020	IRQ status resister 3 (GPC_ISR3)	32	R	0000_0000h	27.8.9/1385
20D_C024	IRQ status resister 4 (GPC_ISR4)	32	R	0000_0000h	27.8.10/ 1385

27.8.1 GPC Interface control register (GPC_CNTR)

Address: 20D_C000h base + 0h offset = 20D_C000h



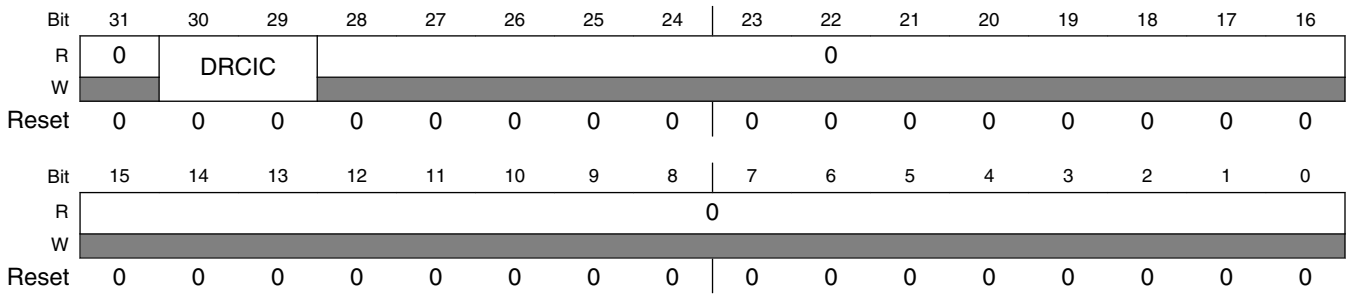


GPC_CNTR field descriptions

Field	Description
31–23 Reserved	This read-only field is reserved and always has the value 0.
22 -	This field is reserved. Reserved
21 GPCIRQM	GPC interrupt/event masking 1 interrupt/event is masked 0 not masked
20 Reserved	This read-only field is reserved and always has the value 1.
19–17 Reserved	This read-only field is reserved and always has the value 0.
16 DVFS0CR	DVFS0 (ARM) Change request (bit is read-only) 1 DVFS0 is requesting for frequency/voltage update 0 DVFS0 has no request
15–6 Reserved	This read-only field is reserved and always has the value 0.
5 -	This field is reserved. Reserved
4 -	This field is reserved. Reserved
3–2 Reserved	This read-only field is reserved and always has the value 0.
1 gpu_vpu_pup_req	GPU/VPU Power Up request. Self-cleared bit. * Note: Power switch for GPU/VPU power domain is controlled by ANALOG configuration, not GPU/VPU PGC signals 1 Request Power Up sequence to start for GPU/VPU 0 no request
0 gpu_vpu_pdn_req	GPU/VPU Power Down request. Self-cleared bit. * Note: Power switch for GPU/VPU power domain is controlled by ANALOG configuration, not GPU/VPU PGC signals 1 Request Power Down sequence to start for GPU/VPU 0 no request

27.8.2 GPC Power Gating Register (GPC_PGR)

Address: 20D_C000h base + 4h offset = 20D_C004h



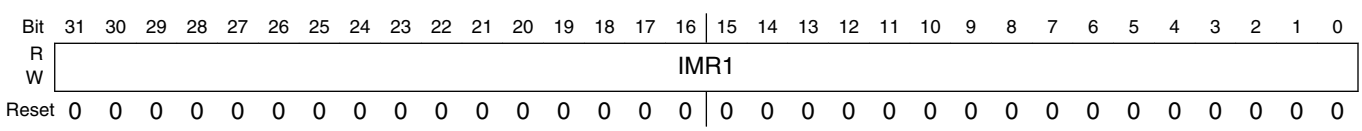
GPC_PGR field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 DRCIC	Debug ref cir in mux control 00 ccm_cosr_1_clk_in 01 ccm_cosr_2_clk_in 10 restricted 11 restricted
Reserved	This read-only field is reserved and always has the value 0.

27.8.3 IRQ masking register 1 (GPC_IMR1)

IMR1 Register - masking of irq[63:32].

Address: 20D_C000h base + 8h offset = 20D_C008h



GPC_IMR1 field descriptions

Field	Description
IMR1	IRQ[63:32] masking bits: 1-irq masked, 0-irq is not masked

27.8.4 IRQ masking register 2 (GPC_IMR2)

IMR2 Register - masking of irq[95:64].

Address: 20D_C000h base + Ch offset = 20D_C00Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	IMR2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPC_IMR2 field descriptions

Field	Description
IMR2	IRQ[95:64] masking bits: 1-irq masked, 0-irq is not masked

27.8.5 IRQ masking register 3 (GPC_IMR3)

IMR3 Register - masking of irq[127:96].

Address: 20D_C000h base + 10h offset = 20D_C010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	IMR3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPC_IMR3 field descriptions

Field	Description
IMR3	IRQ[127:96] masking bits: 1-irq masked, 0-irq is not masked

27.8.6 IRQ masking register 4 (GPC_IMR4)

IMR4 Register - masking of irq[159:128].

Address: 20D_C000h base + 14h offset = 20D_C014h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	IMR4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

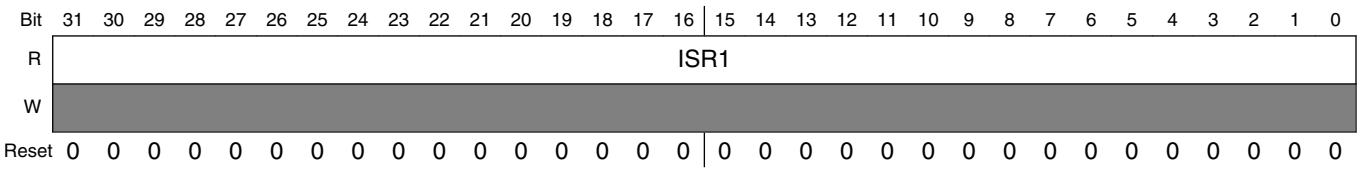
GPC_IMR4 field descriptions

Field	Description
IMR4	IRQ[159:128] masking bits: 1-irq masked, 0-irq is not masked

27.8.7 IRQ status resister 1 (GPC_ISR1)

ISR1 Register - status of irq [63:32].

Address: 20D_C000h base + 18h offset = 20D_C018h



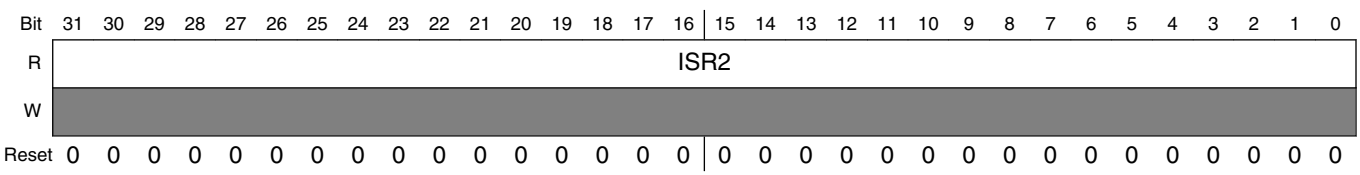
GPC_ISR1 field descriptions

Field	Description
ISR1	IRQ[63:32] status, read only

27.8.8 IRQ status resister 2 (GPC_ISR2)

ISR2 Register - status of irq [95:64].

Address: 20D_C000h base + 1Ch offset = 20D_C01Ch



GPC_ISR2 field descriptions

Field	Description
ISR2	IRQ[95:64] status, read only