

For the keys that require a very precise order (such as game keys), individual GPIO pins may be more useful.

## 38.6 KPP Memory Map/Register Definition

The KPP contains four registers.

**KPP memory map**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
20B_8000	Keypad Control Register (KPP_KPCR)	16	R/W	0000h	<a href="#">38.6.1/3554</a>
20B_8002	Keypad Status Register (KPP_KPSR)	16	R/W	0400h	<a href="#">38.6.2/3555</a>
20B_8004	Keypad Data Direction Register (KPP_KDDR)	16	R/W	0000h	<a href="#">38.6.3/3557</a>
20B_8006	Keypad Data Register (KPP_KPDR)	16	R/W	0000h	<a href="#">38.6.4/3557</a>

### 38.6.1 Keypad Control Register (KPP\_KPCR)

The Keypad Control Register determines which of the eight possible column strobes are to be open drain when configured as outputs, and which of the eight row sense lines are considered in generating an interrupt to the core.

It is up to the programmer to ensure that pins being used for functions other than the keypad are properly disabled. The KPP\_KPCR register is byte- or half-word-addressable.

Address: 20B\_8000h base + 0h offset = 20B\_8000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	KCO								KRE							
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**KPP\_KPCR field descriptions**

Field	Description
15–8 KCO	Keypad Column Strobe Open-Drain Enable. Setting a column open-drain enable bit (KCO7-KCO0) disables the pull-up driver on that pin. Clearing the bit allows the pin to drive to the high state. This bit has no effect when the pin is configured as an input.  <b>NOTE:</b> Configuration of external port control logic (for example, IOMUX) should be done properly so that the KPP controls an open-drain enable of the pin.  0 <b>TOTEM_POLE</b> — Column strobe output is totem pole drive. 1 <b>OPEN_DRAIN</b> — Column strobe output is open drain.

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**KPP\_KPCR field descriptions (continued)**

Field	Description
KRE	Keypad Row Enable. Setting a row enable control bit in this register enables the corresponding row line to participate in interrupt generation. Likewise, clearing a bit disables that row from being used to generate an interrupt. This register is cleared by a reset, disabling all rows. The row-enable logic is independent of the programmed direction of the pin. Writing a "0" to the data register of the pins configured as outputs will cause a keypad interrupt to be generated if the row enable associated with that bit is set.  0 Row is not included in the keypad key press detect. 1 Row is included in the keypad key press detect.

**38.6.2 Keypad Status Register (KPP\_KPSR)**

The Keypad Status Register reflects the state of the key press detect circuit. The KPP\_KPSR register is byte- or half-word-addressable.

Address: 20B\_8000h base + 2h offset = 20B\_8002h

Bit	15	14	13	12	11	10	9	8
Read	0						KRIE	KDIE
Write								
Reset	0	0	0	0	0	1	0	0
Bit	7	6	5	4	3	2	1	0
Read	0				0	0	KPKR	KPKD
Write					KRSS	KDSC	w1c	w1c
Reset	0	0	0	0	0	0	0	0

**KPP\_KPSR field descriptions**

Field	Description
15–10 Reserved	This read-only field is reserved and always has the value 0.
9 KRIE	Keypad Release Interrupt Enable. The software should ensure that the interrupt for a Key Release event is masked until it has entered the key pressed state, and vice versa, unless this activity is desired (as might be the case when a repeated interrupt is to be generated). The synchronizer chains are capable of being initialized to detect repeated key presses or releases. If they are not initialized when the corresponding event flag is cleared, false interrupts may be generated for depress (or release) events shorter than the length of the corresponding chain.  0 No interrupt request is generated when KPKR is set. 1 An interrupt request is generated when KPKR is set.
8 KDIE	Keypad Key Depress Interrupt Enable. Software should ensure that the interrupt for a Key Release event is masked until it has entered the key pressed state, and vice-versa, unless this activity is desired (as might be the case when a repeated interrupt is to be generated). The synchronizer chains are capable of being initialized to detect repeated key presses or releases. If they are not initialized when the corresponding event flag is cleared, false interrupts may be generated for depress (or release) events shorter than the length of the corresponding chain.

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**KPP\_KPSR field descriptions (continued)**

Field	Description
	0 No interrupt request is generated when KPKD is set. 1 An interrupt request is generated when KPKD is set.
7–4 Reserved	This read-only field is reserved and always has the value 0.
3 KRSS	Key Release Synchronizer Set. Self-clear bit. The Key release synchronizer is set by writing a logic one into this bit. Reads return a value of "0". 0 No effect 1 Set bits which sets keypad release synchronizer chain
2 KDSC	Key Depress Synchronizer Clear. Self-clear bit. The Key depress synchronizer is cleared by writing a logic "1" into this bit. Reads return a value of "0". 0 No effect 1 Set bits that clear the keypad depress synchronizer chain
1 KPKR	Keypad Key Release. The keypad key release (KPKR) status bit is set when all enabled rows are detected high after synchronization (the KPKR status bit will be set when cleared by a reset). The KPKR bit may be used to generate a maskable key release interrupt. The key release synchronizer may be set high by software after scanning the keypad to ensure a known state. Due to the logic function of the release and depress synchronizer chains, it is possible to see the re-assertion of a status flag (KPKD or KPKR) if it is cleared by software prior to the system exiting the state it represents. Reset value of register is "0" as long as reset is asserted. However when reset is de-asserted, the value of the register depends upon the external row pins and can become "1". 0 No key release detected 1 All keys have been released
0 KPKD	Keypad Key Depress. The keypad key depress (KPKD) status bit is set when one or more enabled rows are detected low after synchronization. The KPKD status bit remains set until cleared by the software. The KPKD bit may be used to generate a maskable key depress interrupt. If desired, the software may clear the key press synchronizer chain to allow a repeated interrupt to be generated while a key remains pressed. In this case, a new interrupt will be generated after the synchronizer delay (4 cycles of the low frequency reference clock elapses if a key remains pressed. This functionality can be used to detect a long key press. This allows detection of additional key presses of the same key or other keys. Due to the logic function of the release and depress synchronizer chains, it is possible to see the re-assertion of a status flag (KPKD or KPKR) if it is cleared by the software prior to the system exiting the state it represents. 0 No key presses detected 1 A key has been depressed

### 38.6.3 Keypad Data Direction Register (KPP\_KDDR)

The bits in the KPP\_KDDR control the direction of the keypad port pins. The upper eight bits in the register affect the pins designated as column strobes, while the lower eight bits affect the row sense pins. Setting any bit in this register configures the corresponding pin as an output. Clearing any bit in this register configures the corresponding port pin as an input. For the Keypad Row DDR, an internal pull-up is enabled if the corresponding bit is clear. This register is cleared by a reset, configuring all pins as inputs. The KPP\_KDDR register is byte- or half-word addressable.

#### NOTE

When a pin is used as row pin for keypad purposes, all corresponding pull-ups should be enabled at the upper level (for example, IOMUX) when the bit in KRDD is cleared.

Address: 20B\_8000h base + 4h offset = 20B\_8004h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	KCDD								KRDD							
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### KPP\_KDDR field descriptions

Field	Description
15–8 KCDD	Keypad Column Data Direction Register. Setting a bit configures the corresponding COL $n$ pin as an output (where $n = 7$ through 0).  0 <b>INPUT</b> — COL $n$ pin is configured as an input. 1 <b>OUTPUT</b> — COL $n$ pin is configured as an output.
KRDD	Keypad Row Data Direction. Setting a bit configures the corresponding ROW $n$ pin as an output (where $n = 7$ through 0).  0 <b>INPUT</b> — ROW $n$ pin configured as an input. 1 <b>OUTPUT</b> — ROW $n$ pin configured as an output.

### 38.6.4 Keypad Data Register (KPP\_KPDR)

This 16-bit register is used to access the column and row data. Data written to this register is stored in an internal latch, and for each pin configured as an output, the stored data is driven onto the pin. A read of this register returns the value on the pin for those bits configured as inputs. Otherwise, the value read is the value stored in the register.

**KPP Memory Map/Register Definition**

The KPP\_KPDR register is byte- or half-word addressable. This register is not initialized by a reset. Valid data should be written to this register before any bits are configured as outputs.

Address: 20B\_8000h base + 6h offset = 20B\_8006h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	KCD								KRD							
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**KPP\_KPDR field descriptions**

Field	Description
15–8 KCD	Keypad Column Data. A read of these bits returns the value on the pin for those bits configured as inputs. Otherwise, the value read is the value stored in the register.  0 Read/Write "0" from/to column ports 1 Read/Write "1" from/to column ports
KRD	Keypad Row Data. A read of these bits returns the value on the pin for those bits configured as inputs. Otherwise, the value read is the value stored in the register.  0 Read/Write "0" from/to row ports 1 Read/Write "1" from/to row ports