Three JTAG security levels are envisioned, as shown in the table below.

**Table 46-2. JTAG Security Level Control Bits**

| Security Mode | JTAG_SMODE | Description |
|---|---|---|
| No Debug | 2'b11 | The highest security level. |
| Secure JTAG | 2'b01 | Limit the JTAG access by using key based authentication mechanism. |
| JTAG Enable | 2'b00 | Low Security, all JTAG features are enabled. |

## 46.4 Fuse Map

See the Fusemap chapter of this reference manual for more information.

## 46.5 OCOTP Memory Map/Register Definition

OCOTP Hardware Register Format Summary

**OCOTP memory map**

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|---|---|---|---|---|---|
| 21B_C000 | OTP Controller Control Register (OCOTP_CTRL) | 32 | R/W | 0000_0000h | 46.5.1/4032 |
| 21B_C004 | OTP Controller Control Register (OCOTP_CTRL_SET) | 32 | R/W | 0000_0000h | 46.5.1/4032 |
| 21B_C008 | OTP Controller Control Register (OCOTP_CTRL_CLR) | 32 | R/W | 0000_0000h | 46.5.1/4032 |
| 21B_C00C | OTP Controller Control Register (OCOTP_CTRL_TOG) | 32 | R/W | 0000_0000h | 46.5.1/4032 |
| 21B_C010 | OTP Controller Timing Register (OCOTP_TIMING) | 32 | R/W | 0146_1299h | 46.5.2/4034 |
| 21B_C020 | OTP Controller Write Data Register (OCOTP_DATA) | 32 | R/W | 0000_0000h | 46.5.3/4035 |
| 21B_C030 | OTP Controller Write Data Register (OCOTP_READ_CTRL) | 32 | R/W | 0000_0000h | 46.5.4/4035 |
| 21B_C040 | OTP Controller Read Data Register (OCOTP_READ_FUSE_DATA) | 32 | R/W | 0000_0000h | 46.5.5/4036 |
| 21B_C050 | Sticky bit Register (OCOTP_SW_STICKY) | 32 | R/W | 0000_0000h | 46.5.6/4037 |
| 21B_C060 | Software Controllable Signals Register (OCOTP_SCS) | 32 | R/W | 0000_0000h | 46.5.7/4038 |
| 21B_C064 | Software Controllable Signals Register (OCOTP_SCS_SET) | 32 | R/W | 0000_0000h | 46.5.7/4038 |
| 21B_C068 | Software Controllable Signals Register (OCOTP_SCS_CLR) | 32 | R/W | 0000_0000h | 46.5.7/4038 |
| 21B_C06C | Software Controllable Signals Register (OCOTP_SCS_TOG) | 32 | R/W | 0000_0000h | 46.5.7/4038 |
| 21B_C090 | OTP Controller Version Register (OCOTP_VERSION) | 32 | R | 0200_0000h | 46.5.8/4039 |

*Table continues on the next page...*

## OCOTP memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|---|---|---|---|---|---|
| 21B_C400 | Value of OTP Bank0 Word0 (Lock controls) (OCOTP_LOCK) | 32 | R | 0000_0000h | 46.5.9/4039 |
| 21B_C410 | Value of OTP Bank0 Word1 (Configuration and Manufacturing Info.) (OCOTP_CFG0) | 32 | R/W | 0000_0000h | 46.5.10/ 4042 |
| 21B_C420 | Value of OTP Bank0 Word2 (Configuration and Manufacturing Info.) (OCOTP_CFG1) | 32 | R/W | 0000_0000h | 46.5.11/ 4043 |
| 21B_C430 | Value of OTP Bank0 Word3 (Configuration and Manufacturing Info.) (OCOTP_CFG2) | 32 | R/W | 0000_0000h | 46.5.12/ 4043 |
| 21B_C440 | Value of OTP Bank0 Word4 (Configuration and Manufacturing Info.) (OCOTP_CFG3) | 32 | R/W | 0000_0000h | 46.5.13/ 4044 |
| 21B_C450 | Value of OTP Bank0 Word5 (Configuration and Manufacturing Info.) (OCOTP_CFG4) | 32 | R/W | 0000_0000h | 46.5.14/ 4044 |
| 21B_C460 | Value of OTP Bank0 Word6 (Configuration and Manufacturing Info.) (OCOTP_CFG5) | 32 | R/W | 0000_0000h | 46.5.15/ 4045 |
| 21B_C470 | Value of OTP Bank0 Word7 (Configuration and Manufacturing Info.) (OCOTP_CFG6) | 32 | R/W | 0000_0000h | 46.5.16/ 4045 |
| 21B_C480 | Value of OTP Bank1 Word0 (Memory Related Info.) (OCOTP_MEM0) | 32 | R/W | 0000_0000h | 46.5.17/ 4046 |
| 21B_C490 | Value of OTP Bank1 Word1 (Memory Related Info.) (OCOTP_MEM1) | 32 | R/W | 0000_0000h | 46.5.18/ 4046 |
| 21B_C4A0 | Value of OTP Bank1 Word2 (Memory Related Info.) (OCOTP_MEM2) | 32 | R/W | 0000_0000h | 46.5.19/ 4047 |
| 21B_C4B0 | Value of OTP Bank1 Word3 (Memory Related Info.) (OCOTP_MEM3) | 32 | R/W | 0000_0000h | 46.5.20/ 4047 |
| 21B_C4C0 | Value of OTP Bank1 Word4 (Memory Related Info.) (OCOTP_MEM4) | 32 | R/W | 0000_0000h | 46.5.21/ 4048 |
| 21B_C4D0 | Value of OTP Bank1 Word5 (Memory Related Info.) (OCOTP_ANA0) | 32 | R/W | 0000_0000h | 46.5.22/ 4048 |
| 21B_C4E0 | Value of OTP Bank1 Word6 (General Purpose Customer Defined Info.) (OCOTP_ANA1) | 32 | R/W | 0000_0000h | 46.5.23/ 4049 |
| 21B_C4F0 | Value of OTP Bank1 Word7 (General Purpose Customer Defined Info.) (OCOTP_ANA2) | 32 | R/W | 0000_0000h | 46.5.24/ 4049 |
| 21B_C580 | Shadow Register for OTP Bank3 Word0 (SRK Hash) (OCOTP_SRK0) | 32 | R/W | 0000_0000h | 46.5.25/ 4050 |
| 21B_C590 | Shadow Register for OTP Bank3 Word1 (SRK Hash) (OCOTP_SRK1) | 32 | R/W | 0000_0000h | 46.5.26/ 4050 |
| 21B_C5A0 | Shadow Register for OTP Bank3 Word2 (SRK Hash) (OCOTP_SRK2) | 32 | R/W | 0000_0000h | 46.5.27/ 4051 |
| 21B_C5B0 | Shadow Register for OTP Bank3 Word3 (SRK Hash) (OCOTP_SRK3) | 32 | R/W | 0000_0000h | 46.5.28/ 4051 |
| 21B_C5C0 | Shadow Register for OTP Bank3 Word4 (SRK Hash) (OCOTP_SRK4) | 32 | R/W | 0000_0000h | 46.5.29/ 4052 |
| 21B_C5D0 | Shadow Register for OTP Bank3 Word5 (SRK Hash) (OCOTP_SRK5) | 32 | R/W | 0000_0000h | 46.5.30/ 4052 |

*Table continues on the next page...*

**OCOTP memory map (continued)**

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|---|---|---|---|---|---|
| 21B_C5E0 | Shadow Register for OTP Bank3 Word6 (SRK Hash) (OCOTP_SRK6) | 32 | R/W | 0000_0000h | 46.5.31/ 4053 |
| 21B_C5F0 | Shadow Register for OTP Bank3 Word7 (SRK Hash) (OCOTP_SRK7) | 32 | R/W | 0000_0000h | 46.5.32/ 4053 |
| 21B_C600 | Value of OTP Bank4 Word0 (Secure JTAG Response Field) (OCOTP_RESP0) | 32 | R/W | 0000_0000h | 46.5.33/ 4054 |
| 21B_C610 | Value of OTP Bank4 Word1 (Secure JTAG Response Field) (OCOTP_HSJC_RESP1) | 32 | R/W | 0000_0000h | 46.5.34/ 4054 |
| 21B_C620 | Value of OTP Bank4 Word2 (MAC Address) (OCOTP_MAC0) | 32 | R/W | 0000_0000h | 46.5.35/ 4055 |
| 21B_C630 | Value of OTP Bank4 Word3 (MAC Address) (OCOTP_MAC1) | 32 | R/W | 0000_0000h | 46.5.36/ 4055 |
| 21B_C660 | Value of OTP Bank4 Word6 (HW Capabilities) (OCOTP_GP1) | 32 | R/W | 0000_0000h | 46.5.37/ 4056 |
| 21B_C670 | Value of OTP Bank4 Word7 (HW Capabilities) (OCOTP_GP2) | 32 | R/W | 0000_0000h | 46.5.38/ 4056 |
| 21B_C6D0 | Value of OTP Bank5 Word5 (HW Capabilities) (OCOTP_MISC_CONF) | 32 | R/W | 0000_0000h | 46.5.39/ 4057 |
| 21B_C6E0 | Value of OTP Bank5 Word6 (HW Capabilities) (OCOTP_FIELD_RETURN) | 32 | R/W | 0000_0000h | 46.5.40/ 4057 |
| 21B_C6F0 | Value of OTP Bank5 Word7 (HW Capabilities) (OCOTP_SRK_REVOKE) | 32 | R/W | 0000_0000h | 46.5.41/ 4058 |

## 46.5.1 OTP Controller Control Register (OCOTP_CTRL*n*)

The OCOTP Control and Status Register specifies the copy state, as well as the control required for random access of the OTP memory

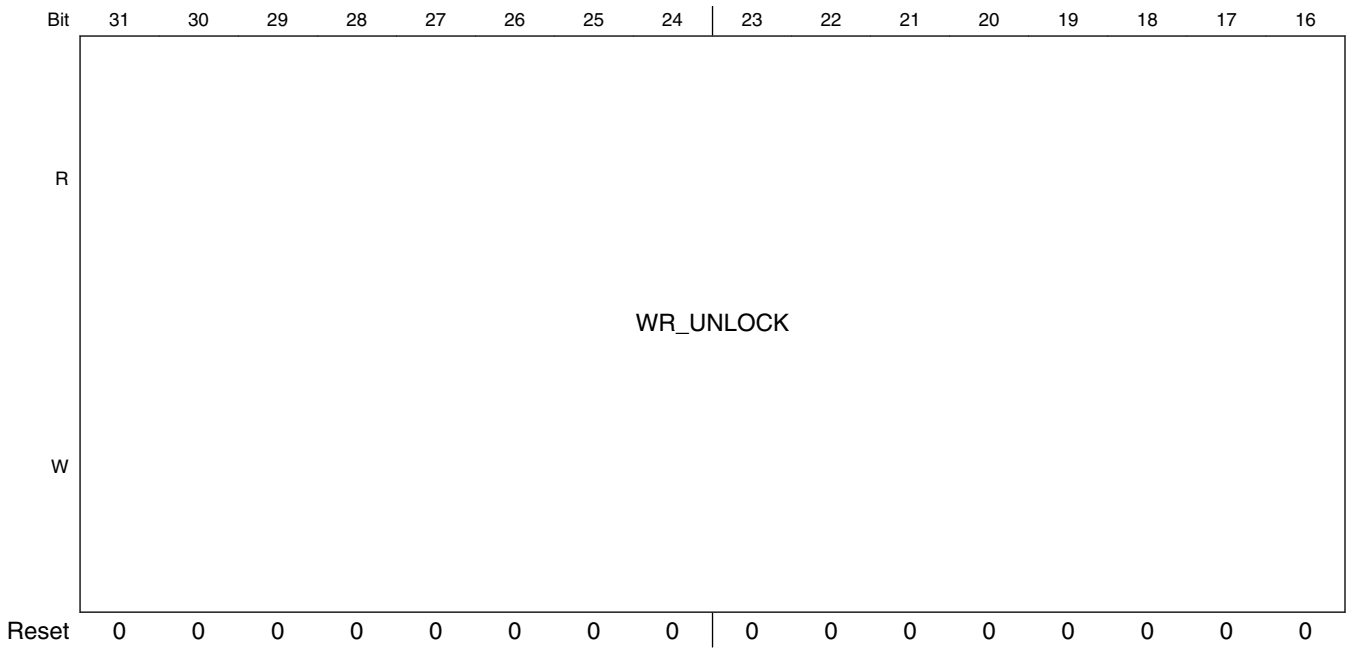
OCOTP_CTRL: 0x000

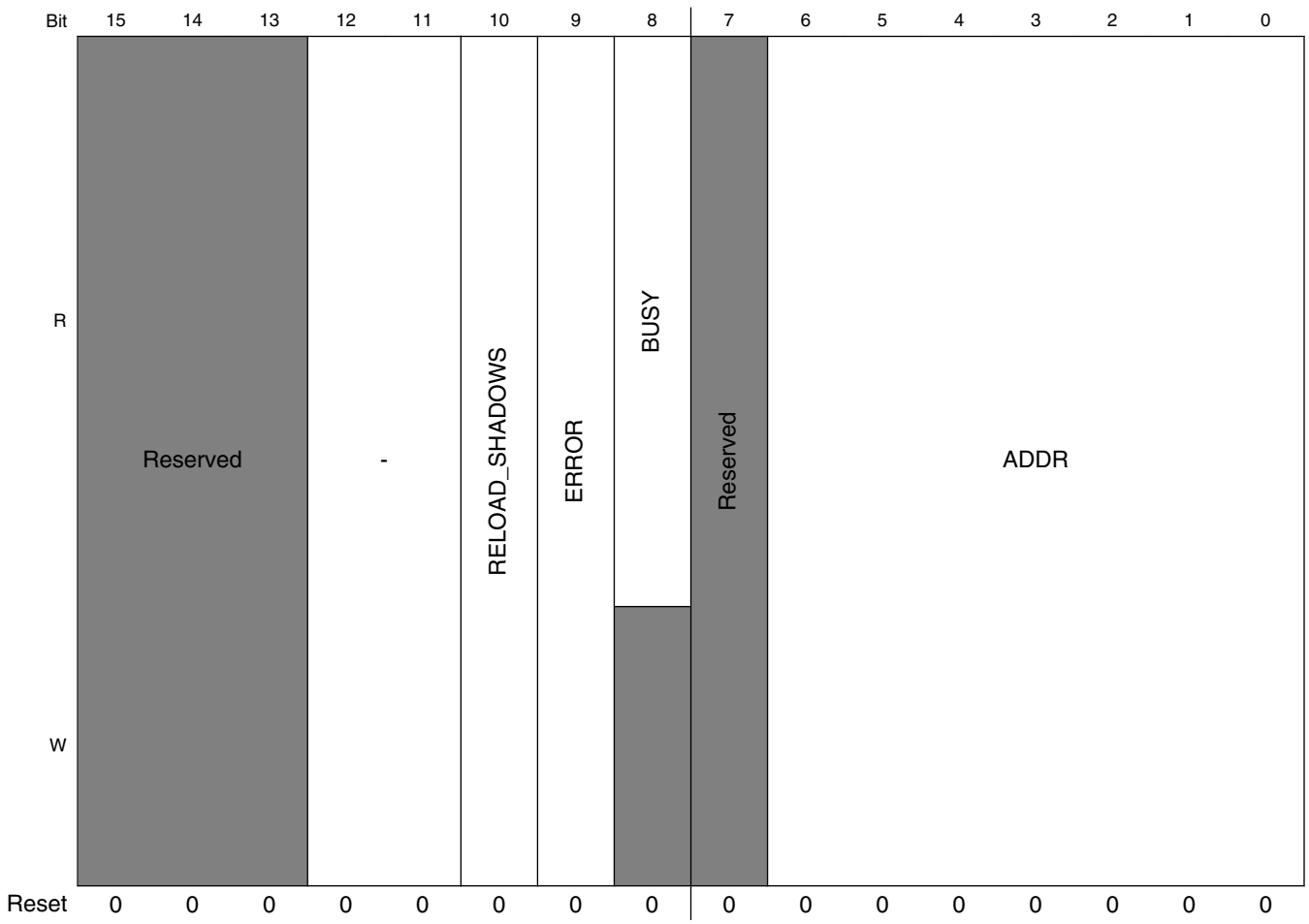
The OCOTP Control and Status Register provides the necessary software interface for performing read and write operations to the On-Chip OTP (One-Time Programmable ROM). The control fields such as WR_UNLOCK, ADDR and BUSY/ERROR may be used in conjuction with the HW_OCOTP_DATA register to perform write operations. Read operations to the On-Chip OTP are involving ADDR, BUSY/ERROR bit field and HW_OCOTP_READ_CTRL register. Read value is saved in HW_OCOTP_READ_FUSE_DATA register.

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 0h offset + (4d × i), where i=0d to 3d



**OCOTP_CTRL*n* field descriptions**

| Field | Description |
|---|---|
| 31–16<br>WR_UNLOCK | Write 0x3E77 to enable OTP write accesses. NOTE: This register must be unlocked on a write-by-write basis (a write is initiated when HW_OCOTP_DATA is written), so the UNLOCK bitfield must contain the correct key value during all writes to HW_OCOTP_DATA, otherwise a write shall not be initiated. This field is automatically cleared after a successful write completion (clearing of BUSY).<br><br>0x3E77 **KEY** — Key needed to unlock HW_OCOTP_DATA register. |
| 15–13<br>- | This field is reserved.<br>Reserved |
| 12–11<br>- | Reserved |
| 10<br>RELOAD_<br>SHADOWS | Set to force re-loading the shadow registers (HW/SW capability and LOCK). This operation will automatically set BUSY. Once the shadow registers have been re-loaded, BUSY and RELOAD_SHADOWS are automatically cleared by the controller. |
| 9<br>ERROR | Set by the controller when an access to a locked region(OTP or shadow register) is requested. Must be cleared before any further access can be performed. This bit can only be set by the controller. This bit is also set if the Pin interface is active and software requests an access to the OTP. In this instance, the ERROR bit cannot be cleared until the Pin interface access has completed. Reset this bit by writing a one to the SCT clear address space and not by a general write. |
| 8<br>BUSY | OTP controller status bit. When active, no new write access or read access to OTP(including RELOAD_SHADOWS) can be performed. Cleared by controller when access complete. After reset (or after setting RELOAD_SHADOWS), this bit is set by the controller until the HW/SW and LOCK registers are successfully copied, after which time it is automatically cleared by the controller. |
| 7<br>- | This field is reserved.<br>Reserved |
| ADDR | OTP write and read access address register. Specifies one of 128 word address locations (0x00 - 0x7f). If a valid access is accepted by the controller, the controller makes an internal copy of this value. This internal copy will not update until the access is complete. |

## 46.5.2 OTP Controller Timing Register (OCOTP_TIMING)

The OCOTP Data Register is used for OTP Programming

This register specifies timing parameters for programming and reading the OCOTP fuse array.

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 10h offset = 21B_C010h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | | | | WAIT | | | | | | STROBE_READ | | | | | | RELAX | | | | STROBE_PROG | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

**OCOTP_TIMING field descriptions**

| Field | Description |
|---|---|
| 31–28<br>Reserved | This read-only field is reserved and always has the value 0. |
| 27–22<br>WAIT | This count value specifies time interval between auto read and write access in one time program. It is given in number of ipg_clk periods. |
| 21–16<br>STROBE_READ | This count value specifies the strobe period in one time read OTP. Trd = ((STROBE_READ+1)- 2*(RELAX +1)) /ipg_clk_freq. It is given in number of ipg_clk periods. |
| 15–12<br>RELAX | This count value specifies the time to add to all default timing parameters other than the Tpgm and Trd. It is given in number of ipg_clk periods. |
| STROBE_PROG | This count value specifies the strobe period in one time write OTP. Tpgm = ((STROBE_PROG+1)- 2*(RELAX+1)) /ipg_clk_freq. It is given in number of ipg_clk periods. |

## 46.5.3 OTP Controller Write Data Register (OCOTP_DATA)

The OCOTP Data Register is used for OTP Programming

This register is used in conjuction with HW_OCOTP_CTRL to perform one-time writes to the OTP. Please see the "Software Write Sequence" section for operating details.

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 20h offset = 21B_C020h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_DATA field descriptions**

| Field | Description |
|---|---|
| DATA | Used to initiate a write to OTP. Please see the "Software Write Sequence" section for operating details. |

## 46.5.4 OTP Controller Write Data Register (OCOTP_READ_CTRL)

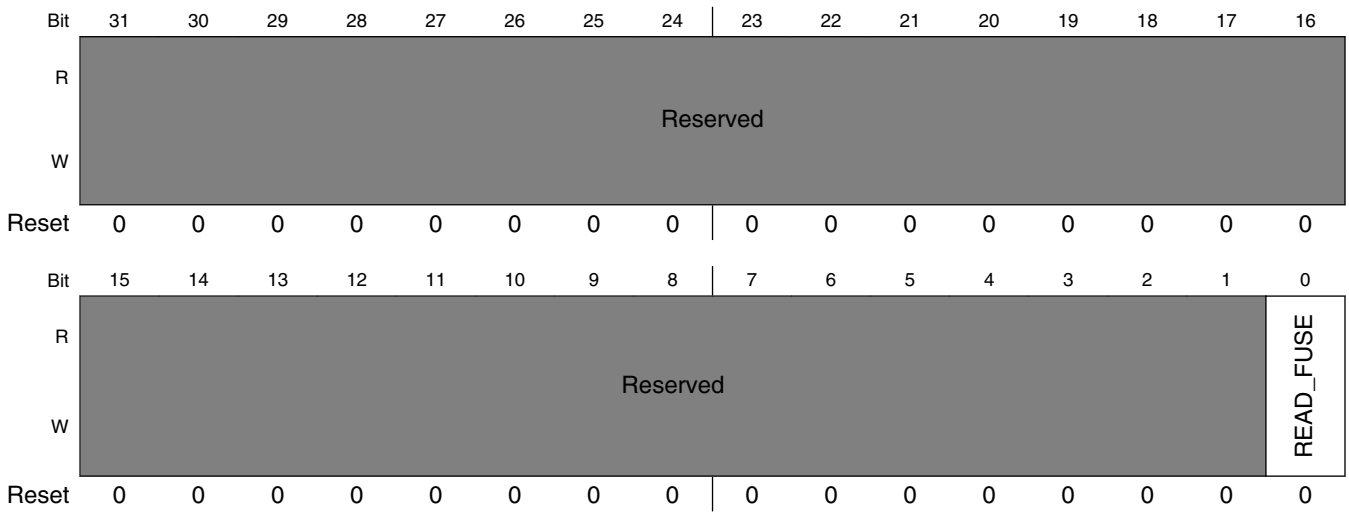
The OCOTP Register is used for OTP Read

This register is used in conjuction with HW_OCOTP_CTRL to perform one time read to the OTP. Please see the "Software read Sequence" section for operating details.

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 30h offset = 21B_C030h




**OCOTP_READ_CTRL field descriptions**

| Field | Description |
|---|---|
| 31–1<br>- | This field is reserved.<br>Reserved |
| 0<br>READ_FUSE | Used to initiate a read to OTP. Please see the "Software read Sequence" section for operating details. |

## 46.5.5 OTP Controller Read Data Register (OCOTP_READ_FUSE_DATA)

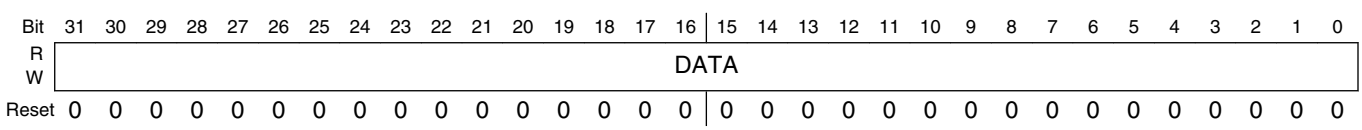
The OCOTP Data Register is used for OTP Read

The data read from OTP

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 40h offset = 21B_C040h




**OCOTP_READ_FUSE_DATA field descriptions**

| Field | Description |
|---|---|
| DATA | The data read from OTP |

## 46.5.6 Sticky bit Register (OCOTP_SW_STICKY)

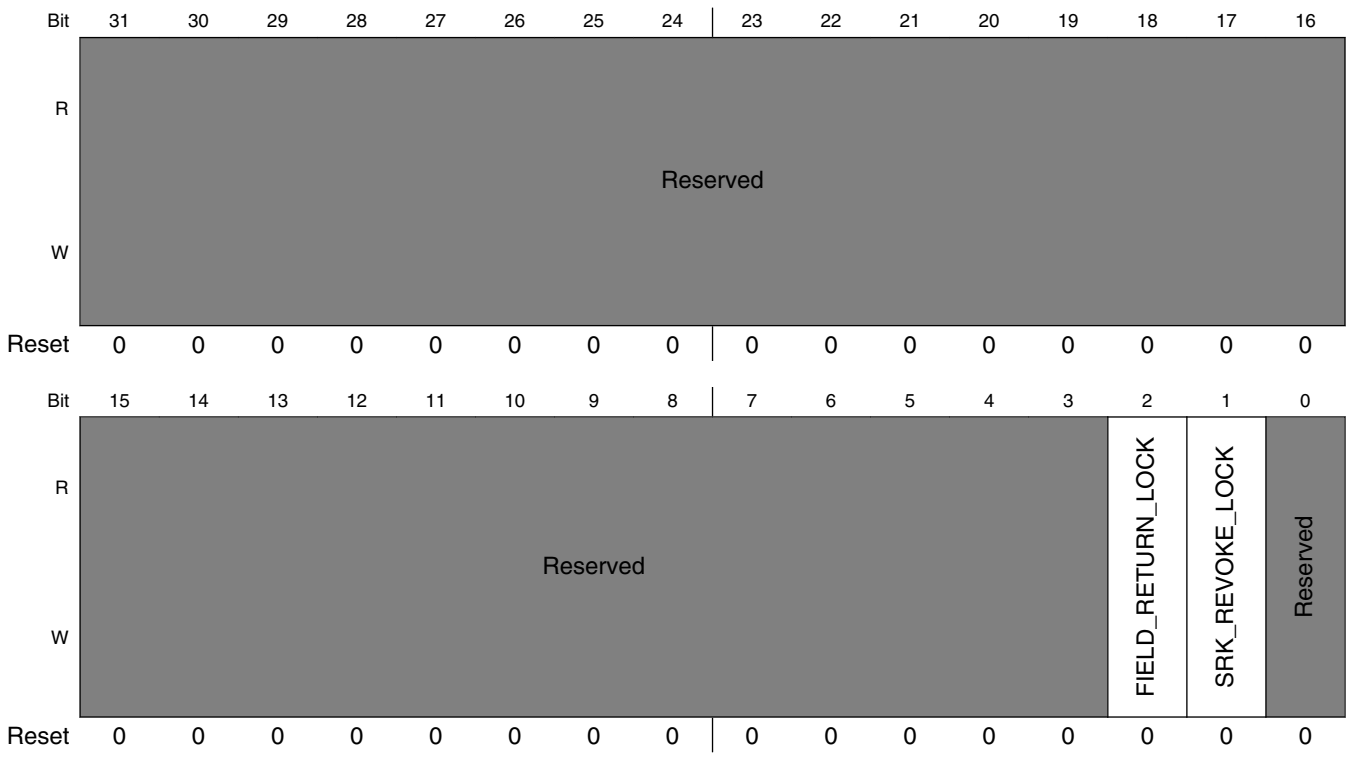
Some SW sticky bits .

Some sticky bits are used by SW to lock some fuse area , shadow registers and other features.

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 50h offset = 21B_C050h




**OCOTP_SW_STICKY field descriptions**

| Field | Description |
|---|---|
| 31–3<br>- | This field is reserved.<br>Reserved |
| 2<br>FIELD_<br>RETURN_LOCK | Shadow register write and OTP write lock for FIELD_RETURN region. When set, the writing of this region's shadow register and OTP fuse word are blocked.Once this bit is set, it is always high unless a POR is issued. |
| 1<br>SRK_REVOKE_<br>LOCK | Shadow register write and OTP write lock for SRK_REVOKE, MC_ERA and AP_BI_VER regions. When set, the writing of these region's shadow register and OTP fuse word are blocked. Once this bit is set, it is always high unless a POR is issued. |
| 0<br>- | This field is reserved.<br>Reserved. |

## 46.5.7 Software Controllable Signals Register (OCOTP_SCS*n*)

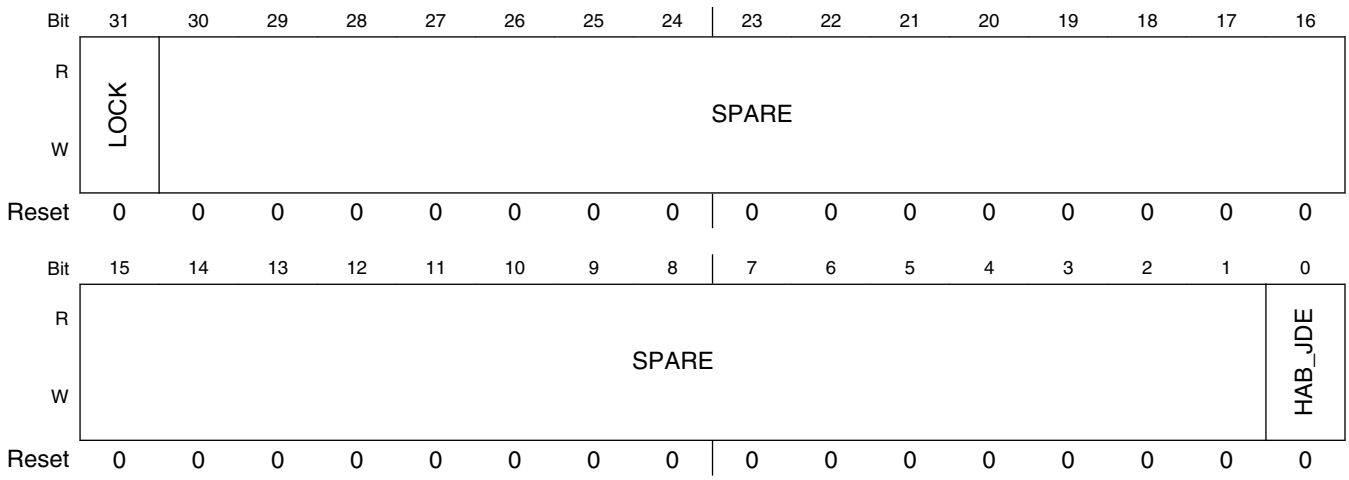
HW_OCOTP_SCS: 0x060

This register holds volatile configuration values that can be set and locked by trusted software. All values are returned to their defualt values after POR.

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 60h offset + (4d × i), where i=0d to 3d




**OCOTP_SCS*n* field descriptions**

| Field | Description |
|---|---|
| 31<br>LOCK | When set, all of the bits in this register are locked and can not be changed through SW programming. This bit is only reset after a POR is issued. |
| 30–1<br>SPARE | Unallocated read/write bits for implementation specific software use. |
| 0<br>HAB_JDE | HAB JTAG Debug Enable. This bit is used by the HAB to enable JTAG debugging, assuming that a properly signed command to do so is found and validated by the HAB.<br>The HAB must lock the register before passing control to the OS whether or not JTAG debugging has been enabled.<br>Once JTAG is enabled by this bit, it can not be disabled unless the system is reset by POR. 0: JTAG debugging is not enabled by the HAB (it may still be enabled by other mechanisms). 1: JTAG debugging is enabled by the HAB (though this signal may be gated off).<br>1 JTAG debugging is enabled by the HAB (though this signal may be gated off) |

## 46.5.8 OTP Controller Version Register (OCOTP_VERSION)

This register always returns a known read value for debug purposes it indicates the version of the block.

This register indicates the RTL version in use.

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 90h offset = 21B_C090h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | MAJOR | | | | | | | | MINOR | | | | | | | | STEP | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_VERSION field descriptions**

| Field | Description |
|---|---|
| 31–24<br>MAJOR | Fixed read-only value reflecting the MAJOR field of the RTL version. |
| 23–16<br>MINOR | Fixed read-only value reflecting the MINOR field of the RTL version. |
| STEP | Fixed read-only value reflecting the stepping of the RTL version. |

## 46.5.9 Value of OTP Bank0 Word0 (Lock controls) (OCOTP_LOCK)

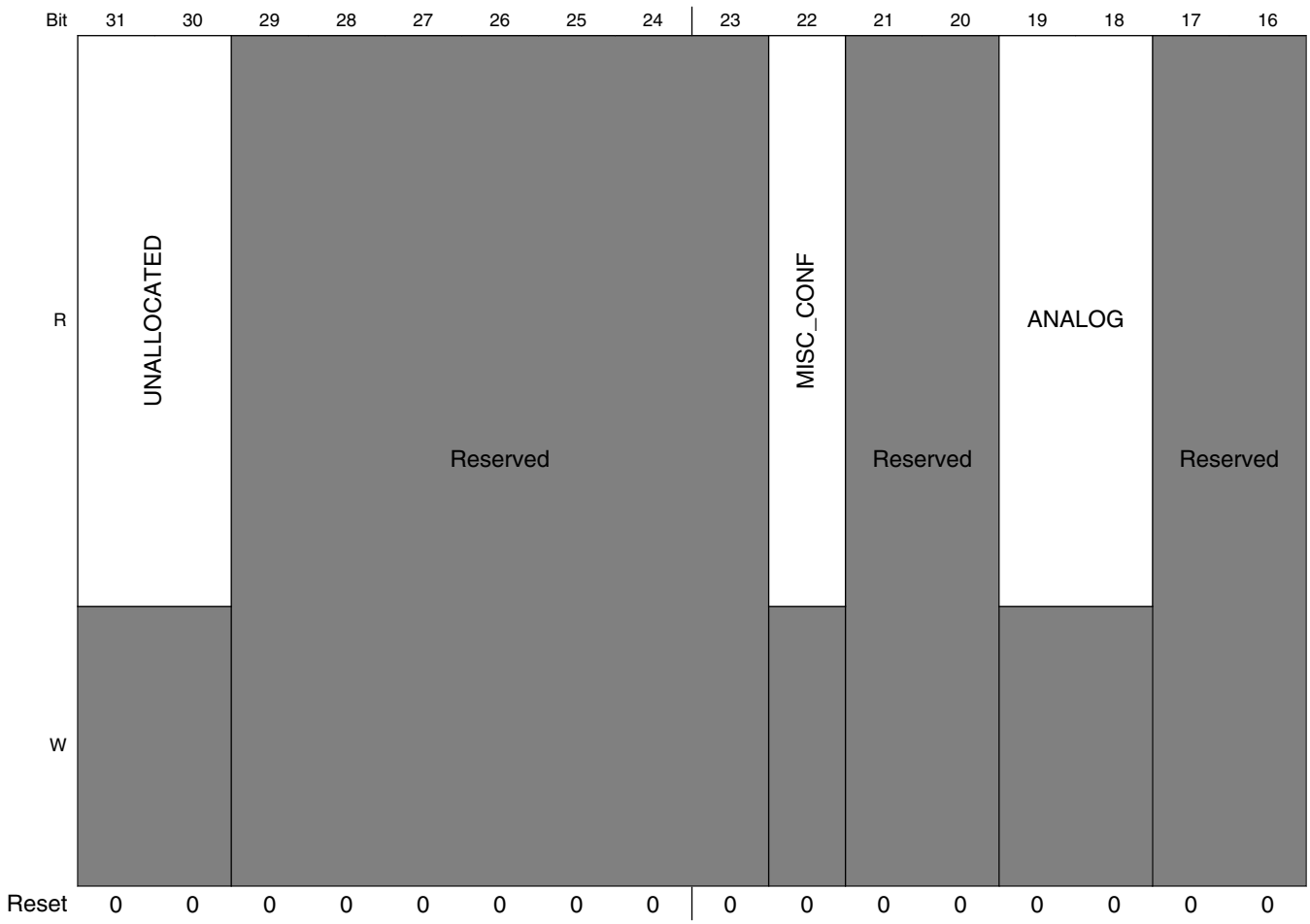
Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

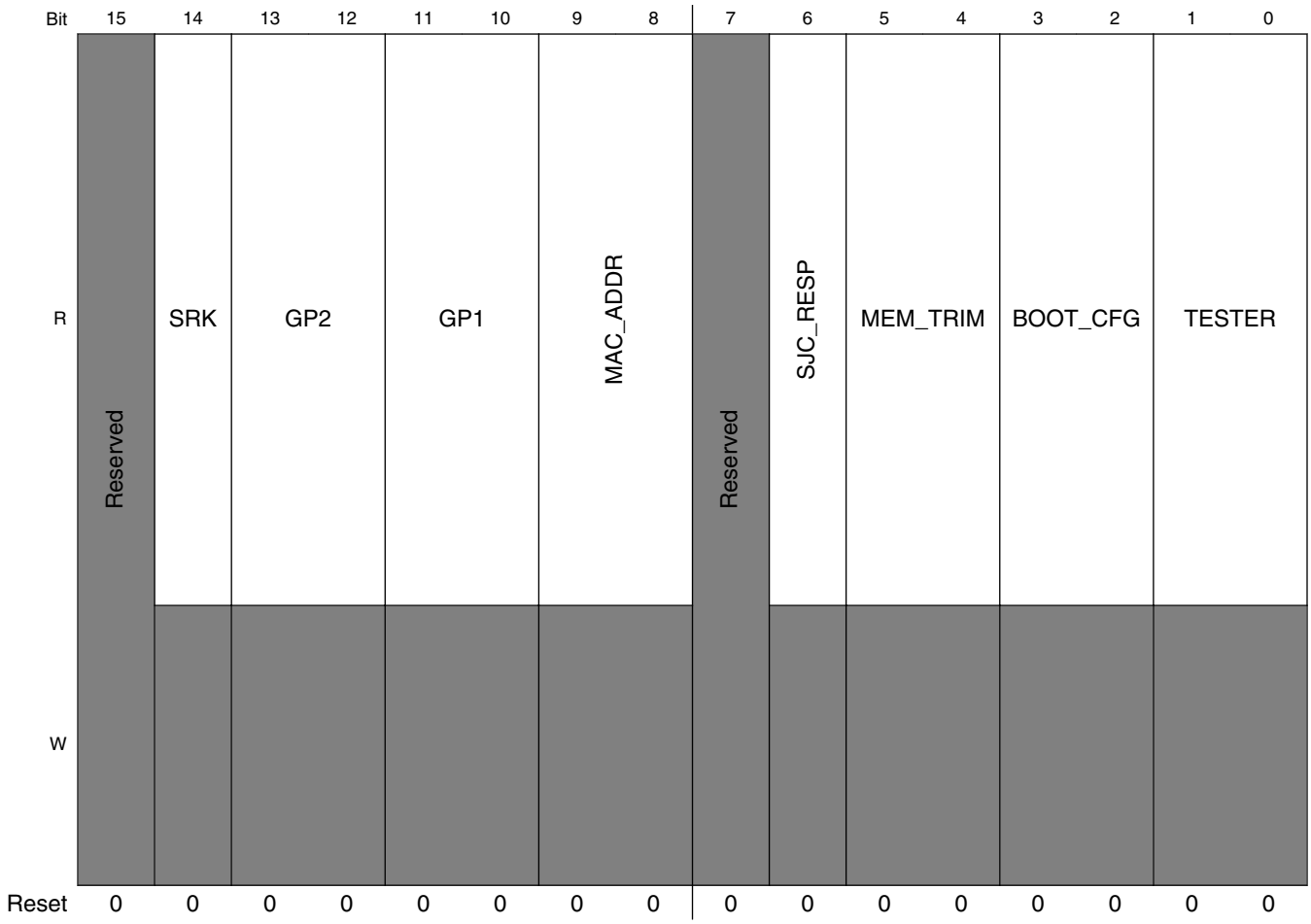
Shadowed memory mapped access to OTP Bank 0, word 0 (ADDR = 0x00).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 400h offset = 21B_C400h






## OCOTP_LOCK field descriptions

| Field | Description |
|---|---|
| 31–30<br>UNALLOCATED | Value of un-used portion of LOCK word |
| 29–23<br>- | This field is reserved.<br>Reserved |
| 22<br>MISC_CONF | Status of shadow register and OTP write lock for misc_conf region. When set, the writing of this region's shadow register and OTP fuse word are blocked. |
| 21–20<br>- | This field is reserved.<br>Reserved |
| 19–18<br>ANALOG | Status of shadow register and OTP write lock for analog region. When bit 1 is set, the writing of this region's shadow register is blocked. When bit 0 is set, the writing of this region's OTP fuse word is blocked. |
| 17–16<br>- | This field is reserved. |
| 15<br>- | This field is reserved.<br>Reserved |
| 14<br>SRK | Status of shadow register and OTP write lock for srk region. When set, the writing of this region's shadow register and OTP fuse word are blocked. |

*Table continues on the next page...*

**OCOTP_LOCK field descriptions (continued)**

| Field | Description |
|---|---|
| 13–12<br>GP2 | Status of shadow register and OTP write lock for gp2 region. When bit 1 is set, the writing of this region's shadow register is blocked. When bit 0 is set, the writing of this region's OTP fuse word is blocked. |
| 11–10<br>GP1 | Status of shadow register and OTP write lock for gp2 region. When bit 1 is set, the writing of this region's shadow register is blocked. When bit 0 is set, the writing of this region's OTP fuse word is blocked. |
| 9–8<br>MAC_ADDR | Status of shadow register and OTP write lock for mac_addr region. When bit 1 is set, the writing of this region's shadow register is blocked. When bit 0 is set, the writing of this region's OTP fuse word is blocked. |
| 7<br>- | This field is reserved.<br>Reserved |
| 6<br>SJC_RESP | Status of shadow register read and write, OTP read and write lock for sjc_resp region. When set, the writing of this region's shadow register and OTP fuse word are blocked. The read of this region's shadow register and OTP fuse word are also blocked. |
| 5–4<br>MEM_TRIM | Status of shadow register and OTP write lock for mem_trim region. When bit 1 is set, the writing of this region's shadow register is blocked. When bit 0 is set, the writing of this region's OTP fuse word is blocked. |
| 3–2<br>BOOT_CFG | Status of shadow register and OTP write lock for boot_cfg region. When bit 1 is set, the writing of this region's shadow register is blocked. When bit 0 is set, the writing of this region's OTP fuse word is blocked. |
| TESTER | Status of shadow register and OTP write lock for tester region. When bit 1 is set, the writing of this region's shadow register is blocked. When bit 0 is set, the writing of this region's OTP fuse word is blocked. |

## 46.5.10 Value of OTP Bank0 Word1 (Configuration and Manufacturing Info.) (OCOTP_CFG0)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 0, word 1 (ADDR = 0x01).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 410h offset = 21B_C410h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_CFG0 field descriptions**

| Field | Description |
|---|---|
| BITS | This register contains 32 bits of the Unique ID and SJC_CHALLENGE field. Reflects value of OTP Bank 0, word 1 (ADDR = 0x01). These bits become read-only after the HW_OCOTP_LOCK_TESTER[1] bit is set. |

## 46.5.11 Value of OTP Bank0 Word2 (Configuration and Manufacturing Info.) (OCOTP_CFG1)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

shadowed memory mapped access to OTP Bank 0, word 2 (ADDR = 0x02).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 420h offset = 21B_C420h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_CFG1 field descriptions**

| Field | Description |
|---|---|
| BITS | This register contains 32 bits of the Unique ID and SJC_CHALLENGE field. Reflects value of OTP Bank 0, word 2 (ADDR = 0x02). These bits become read-only after the HW_OCOTP_LOCK_TESTER[1] bit is set. |

## 46.5.12 Value of OTP Bank0 Word3 (Configuration and Manufacturing Info.) (OCOTP_CFG2)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 0, word 3 (ADDR = 0x03).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 430h offset = 21B_C430h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_CFG2 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 0, word 3 (ADDR = 0x03). These bits become read-only after the HW_OCOTP_LOCK_TESTER[1] bit is set. |

## 46.5.13 Value of OTP Bank0 Word4 (Configuration and Manufacturing Info.) (OCOTP_CFG3)

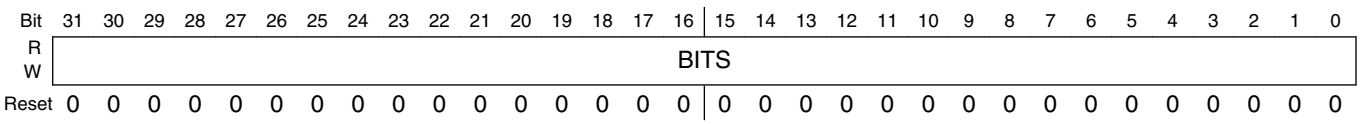
Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Non-shadowed memory mapped access to OTP Bank 0, word 4 (ADDR = 0x04).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 440h offset = 21B_C440h




**OCOTP_CFG3 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 0, word 4 (ADDR = 0x04). These bits become read-only after the HW_OCOTP_LOCK_TESTER[1] bit is set. |

## 46.5.14 Value of OTP Bank0 Word5 (Configuration and Manufacturing Info.) (OCOTP_CFG4)

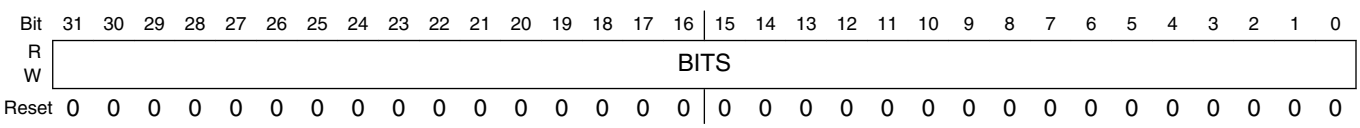
Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 0, word 5 (ADDR = 0x05).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 450h offset = 21B_C450h




**OCOTP_CFG4 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 0, word 5 (ADDR = 0x05). These bits become read-only after the HW_OCOTP_LOCK_BOOT_CFG[1] bit is set. |

## 46.5.15 Value of OTP Bank0 Word6 (Configuration and Manufacturing Info.) (OCOTP_CFG5)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 0, word 6 (ADDR = 0x06).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 460h offset = 21B_C460h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_CFG5 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 0, word 6 (ADDR = 0x06). These bits become read-only after the HW_OCOTP_LOCK_BOOT_CFG[1] bit is set. |

## 46.5.16 Value of OTP Bank0 Word7 (Configuration and Manufacturing Info.) (OCOTP_CFG6)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 0, word 7 (ADDR = 0x07).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 470h offset = 21B_C470h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_CFG6 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 0, word 7 (ADDR = 0x07). These bits become read-only after the HW_OCOTP_LOCK_BOOT_CFG[1] bit is set. |

## 46.5.17 Value of OTP Bank1 Word0 (Memory Related Info.) (OCOTP_MEM0)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP bank 1, word 0 (ADDR = 0x08).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 480h offset = 21B_C480h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_MEM0 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP bank 1, word 0 (ADDR = 0x08). These bits become read-only after the HW_OCOTP_LOCK_MEM_TRIM[1] bit is set. |

## 46.5.18 Value of OTP Bank1 Word1 (Memory Related Info.) (OCOTP_MEM1)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP bank 1, word 1 (ADDR = 0x09).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 490h offset = 21B_C490h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_MEM1 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP bank 1, word 1 (ADDR = 0x09). These bits become read-only after the HW_OCOTP_LOCK_MEM_TRIM[1] bit is set. |

## 46.5.19 Value of OTP Bank1 Word2 (Memory Related Info.) (OCOTP_MEM2)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP bank 1, word 2 (ADDR = 0x0A).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 4A0h offset = 21B_C4A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_MEM2 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP bank 1, word 2 (ADDR = 0x0A). These bits become read-only after the HW_OCOTP_LOCK_MEM_TRIM[1] bit is set. |

## 46.5.20 Value of OTP Bank1 Word3 (Memory Related Info.) (OCOTP_MEM3)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP bank 1, word 3 (ADDR = 0x0B).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 4B0h offset = 21B_C4B0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_MEM3 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP bank 1, word 3 (ADDR = 0x0B). These bits become read-only after the HW_OCOTP_LOCK_MEM_TRIM[1] bit is set. |

## 46.5.21 Value of OTP Bank1 Word4 (Memory Related Info.) (OCOTP_MEM4)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP bank 1, word 4 (ADDR = 0x0C).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 4C0h offset = 21B_C4C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_MEM4 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP bank 1, word 4 (ADDR = 0x0C). These bits become read-only after the HW_OCOTP_LOCK_MEM_TRIM[1] bit is set. |

## 46.5.22 Value of OTP Bank1 Word5 (Memory Related Info.) (OCOTP_ANA0)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP bank 1, word 5 (ADDR = 0x0D).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 4D0h offset = 21B_C4D0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_ANA0 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP bank 1, word 5 (ADDR = 0x0D). These bits become read-only after the HW_OCOTP_LOCK_ANALOG[1] bit is set. |

## 46.5.23 Value of OTP Bank1 Word6 (General Purpose Customer Defined Info.) (OCOTP_ANA1)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP bank 1, word 6 (ADDR = 0x0E).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 4E0h offset = 21B_C4E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_ANA1 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP bank 1, word 6 (ADDR = 0x0E). These bits become read-only after the HW_OCOTP_LOCK_ANALOG[1] bit is set. |

## 46.5.24 Value of OTP Bank1 Word7 (General Purpose Customer Defined Info.) (OCOTP_ANA2)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP bank 1, word 7 (ADDR = 0x0F).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 4F0h offset = 21B_C4F0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_ANA2 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP bank 1, word 7 (ADDR = 0x0F). These bits become read-only after the HW_OCOTP_LOCK_ANALOG[1] bit is set. |

## 46.5.25 Shadow Register for OTP Bank3 Word0 (SRK Hash) (OCOTP_SRK0)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS].

Shadowed memory mapped access to OTP Bank 3, word 0 (ADDR = 0x18).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 580h offset = 21B_C580h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_SRK0 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the hash of the Super Root Key word0 (Copy of OTP Bank 3, word 0 (ADDR = 0x1C)). These bits become read-only after the HW_OCOTP_LOCK_SRK bit is set. |

## 46.5.26 Shadow Register for OTP Bank3 Word1 (SRK Hash) (OCOTP_SRK1)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS].

Shadowed memory mapped access to OTP Bank 3, word 1 (ADDR = 0x19).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 590h offset = 21B_C590h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_SRK1 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the hash of the Super Root Key word1 (Copy of OTP Bank 3, word 1 (ADDR = 0x1D)). These bits become read-only after the HW_OCOTP_LOCK_SRK bit is set. |

## 46.5.27 Shadow Register for OTP Bank3 Word2 (SRK Hash) (OCOTP_SRK2)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS].

Shadowed memory mapped access to OTP Bank 3, word 2 (ADDR = 0x1A).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 5A0h offset = 21B_C5A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_SRK2 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the hash of the Super Root Key word2 (Copy of OTP Bank 3, word 2 (ADDR = 0x1E)). These bits become read-only after the HW_OCOTP_LOCK_SRK bit is set. |

## 46.5.28 Shadow Register for OTP Bank3 Word3 (SRK Hash) (OCOTP_SRK3)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS].

Shadowed memory mapped access to OTP Bank 3, word 3 (ADDR = 0x1B).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 5B0h offset = 21B_C5B0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_SRK3 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the hash of the Super Root Key word3 (Copy of OTP Bank 3, word 3 (ADDR = 0x1F)). These bits become read-only after the HW_OCOTP_LOCK_SRK bit is set. |

## 46.5.29 Shadow Register for OTP Bank3 Word4 (SRK Hash) (OCOTP_SRK4)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS].

Shadowed memory mapped access to OTP Bank 3, word 4 (ADDR = 0x1C).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 5C0h offset = 21B_C5C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_SRK4 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the hash of the Super Root Key word4 (Copy of OTP Bank 3, word 4 (ADDR = 0x20)). These bits become read-only after the HW_OCOTP_LOCK_SRK bit is set. |

## 46.5.30 Shadow Register for OTP Bank3 Word5 (SRK Hash) (OCOTP_SRK5)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS].

Shadowed memory mapped access to OTP Bank 3, word 5 (ADDR = 0x1D).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 5D0h offset = 21B_C5D0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_SRK5 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the hash of the Super Root Key word5 (Copy of OTP Bank 3, word 5 (ADDR = 0x21)). These bits become read-only after the HW_OCOTP_LOCK_SRK bit is set. |

## 46.5.31 Shadow Register for OTP Bank3 Word6 (SRK Hash) (OCOTP_SRK6)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS].

Shadowed memory mapped access to OTP Bank 3, word 6 (ADDR = 0x1E).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 5E0h offset = 21B_C5E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_SRK6 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the hash of the Super Root Key word6 (Copy of OTP Bank 3, word 6 (ADDR = 0x22)). These bits become read-only after the HW_OCOTP_LOCK_SRK bit is set. |

## 46.5.32 Shadow Register for OTP Bank3 Word7 (SRK Hash) (OCOTP_SRK7)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS].

Shadowed memory mapped access to OTP Bank 3, word 7 (ADDR = 0x1F).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 5F0h offset = 21B_C5F0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_SRK7 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the hash of the Super Root Key word7 (Copy of OTP Bank 3, word 7 (ADDR = 0x23)). These bits become read-only after the HW_OCOTP_LOCK_SRK bit is set. |

## 46.5.33 Value of OTP Bank4 Word0 (Secure JTAG Response Field) (OCOTP_RESP0)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 4, word 0 (ADDR = 0x20).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 600h offset = 21B_C600h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_RESP0 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the SJC_RESP Key word0 (Copy of OTP Bank 4, word 0 (ADDR = 0x20)). These bits can be not read and written after the HW_OCOTP_LOCK_SJC_RESP bit is set. If read, returns 0xBADA_BADA and sets HW_OCOTP_CTRL[ERROR]. |

## 46.5.34 Value of OTP Bank4 Word1 (Secure JTAG Response Field) (OCOTP_HSJC_RESP1)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 4, word 1 (ADDR = 0x21).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 610h offset = 21B_C610h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_HSJC_RESP1 field descriptions**

| Field | Description |
|---|---|
| BITS | Shadow register for the SJC_RESP Key word1 (Copy of OTP Bank 4, word 1 (ADDR = 0x21)). These bits can be not read and written after the HW_OCOTP_LOCK_SJC_RESP bit is set. If read, returns 0xBADA_BADA and sets HW_OCOTP_CTRL[ERROR]. |

## 46.5.35 Value of OTP Bank4 Word2 (MAC Address) (OCOTP_MAC0)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 4, word 2 (ADDR = 0x22).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 620h offset = 21B_C620h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_MAC0 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 4, word 2 (ADDR = 0x22). |

## 46.5.36 Value of OTP Bank4 Word3 (MAC Address) (OCOTP_MAC1)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 4, word 3 (ADDR = 0x23).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 630h offset = 21B_C630h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_MAC1 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 4, word 3 (ADDR = 0x23). |

## 46.5.37 Value of OTP Bank4 Word6 (HW Capabilities) (OCOTP_GP1)

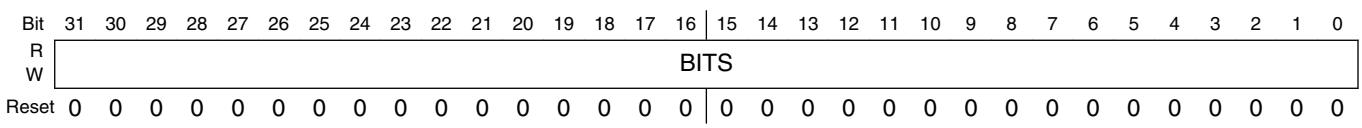
Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 4, word 6 (ADDR = 0x26).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 660h offset = 21B_C660h




**OCOTP_GP1 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 4, word 6 (ADDR = 0x26). |

## 46.5.38 Value of OTP Bank4 Word7 (HW Capabilities) (OCOTP_GP2)

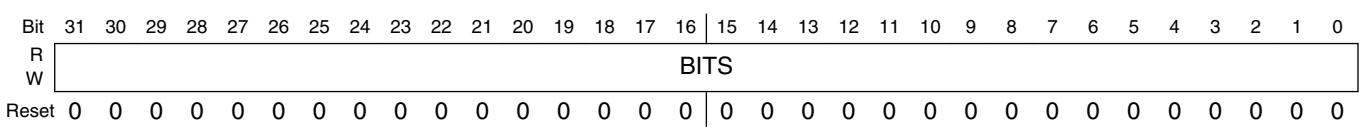
Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 4, word 7 (ADDR = 0x27).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 670h offset = 21B_C670h



**OCOTP_GP2 field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 4, word 7 (ADDR = 0x27). |

## 46.5.39 Value of OTP Bank5 Word5 (HW Capabilities) (OCOTP_MISC_CONF)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 5, word 5 (ADDR = 0x2d).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 6D0h offset = 21B_C6D0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_MISC_CONF field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 5, word 5 (ADDR = 0x2d). |

## 46.5.40 Value of OTP Bank5 Word6 (HW Capabilities) (OCOTP_FIELD_RETURN)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 5, word 6 (ADDR = 0x2e).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 6E0h offset = 21B_C6E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_FIELD_RETURN field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 5, word 6 (ADDR = 0x2e). |

## 46.5.41 Value of OTP Bank5 Word7 (HW Capabilities) (OCOTP_SRK_REVOKE)

Copied from the OTP automatically after reset. Can be re-loaded by setting HW_OCOTP_CTRL[RELOAD_SHADOWS]

Shadowed memory mapped access to OTP Bank 5, word 7 (ADDR = 0x2f).

### EXAMPLE

```
Empty Example.
```

Address: 21B_C000h base + 6F0h offset = 21B_C6F0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R<br>W | BITS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**OCOTP_SRK_REVOKE field descriptions**

| Field | Description |
|---|---|
| BITS | Reflects value of OTP Bank 5, word 7 (ADDR = 0x2f). |