

HDMI Memory Map/Register Definition

- Follower Mode
- In this mode, the CEC controller receives messages and feeds back the initiator with appropriate signals. The CEC controller always works in the follower mode whenever it is not transmitting any data.

For correct CEC controller interface operation, initial reset is required in order to set internal registers to a known state. After this reset, the interface is in an IDLE state, waiting for a read or write request coming from the register configuration.

A specific CEC API is provided that implements all necessary low-level register configuration to send and receive CEC messages. For more information, see the CEC API documentation.

The CEC engine registers base address is 0x7D00. For more information about these registers, see [HDMI Memory Map/Register Definition](#).

For more information about CEC, see *Consumer Electronics Control (CEC) Application Note*.

33.5 HDMI Memory Map/Register Definition

All registers are addressable on 32-bit boundaries; each unused bit or address location is reserved for future use and read back as 0.

HDMI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
12_0000	Design Identification Register (HDMI_DESIGN_ID)	8	R	00h	33.5.1/1593
12_0001	Revision Identification Register (HDMI_REVISION_ID)	8	R	00h	33.5.2/1594
12_0002	Product Identification Register 0 (HDMI_PRODUCT_ID0)	8	R	00h	33.5.3/1594
12_0003	Product Identification Register 1 (HDMI_PRODUCT_ID1)	8	R	00h	33.5.4/1595
12_0004	Configuration Identification Register 0 (HDMI_CONFIG0_ID)	8	R	00h	33.5.5/1595
12_0005	Configuration Identification Register 1 (HDMI_CONFIG1_ID)	8	R	00h	33.5.6/1596
12_0006	Configuration Identification Register 2 (HDMI_CONFIG2_ID)	8	R	00h	33.5.7/1597
12_0007	Configuration Identification Register 3 (HDMI_CONFIG3_ID)	8	R	00h	33.5.8/1598
12_0100	Frame Composer Interrupt Status Register 0 (HDMI_IH_FC_STAT0)	8	w1c	00h	33.5.9/1598

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_0101	Frame Composer Interrupt Status Register 1 (HDMI_IH_FC_STAT1)	8	w1c	00h	33.5.10/ 1599
12_0102	Frame Composer Interrupt Status Register 2 (HDMI_IH_FC_STAT2)	8	w1c	00h	33.5.11/ 1600
12_0103	Audio Sampler Interrupt Status Register (HDMI_IH_AS_STAT0)	8	w1c	00h	33.5.12/ 1601
12_0104	PHY Interface Interrupt Status Register (HDMI_IH_PHY_STAT0)	8	w1c	00h	33.5.13/ 1602
12_0105	E-DDC I2C Master Interrupt Status Register (HDMI_IH_I2CM_STAT0)	8	w1c	00h	33.5.14/ 1603
12_0106	CEC Interrupt Status Register (HDMI_IH_CEC_STAT0)	8	w1c	00h	33.5.15/ 1604
12_0107	Video Packetizer Interrupt Status Register (HDMI_IH_VP_STAT0)	8	w1c	00h	33.5.16/ 1605
12_0108	PHY GEN2 I2C Master Interrupt Status Register (HDMI_IH_I2CMPHY_STAT0)	8	w1c	00h	33.5.17/ 1606
12_0109	AHB Audio DMA Interrupt Status Register (HDMI_IH_AHBDMAAUD_STAT0)	8	w1c	00h	33.5.18/ 1606
12_0180	Frame Composer Interrupt Mute Control Register 0 (HDMI_IH_MUTE_FC_STAT0)	8	R/W	00h	33.5.19/ 1608
12_0181	Frame Composer Interrupt Mute Control Register 1 (HDMI_IH_MUTE_FC_STAT1)	8	R/W	00h	33.5.20/ 1609
12_0182	Frame Composer Interrupt Mute Control Register 2 (HDMI_IH_MUTE_FC_STAT2)	8	R/W	00h	33.5.21/ 1610
12_0183	Audio Sampler Interrupt Mute Control Register 0 (HDMI_IH_MUTE_AS_STAT0)	8	R/W	00h	33.5.22/ 1610
12_0184	PHY Interface Interrupt Mute Control Register (HDMI_IH_MUTE_PHY_STAT0)	8	R/W	00h	33.5.23/ 1611
12_0185	E-DDC I2C Master Interrupt Mute Control Register (HDMI_IH_MUTE_I2CM_STAT0)	8	R/W	00h	33.5.24/ 1612
12_0186	CEC Interrupt Mute Control Register (HDMI_IH_MUTE_CEC_STAT0)	8	R/W	00h	33.5.25/ 1612
12_0187	Video Packetizer Interrupt Mute Control Register (HDMI_IH_MUTE_VP_STAT0)	8	R/W	00h	33.5.26/ 1613
12_0188	PHY GEN 2 I2C Master Interrupt Mute Control Register (HDMI_IH_MUTE_I2CMPHY_STAT0)	8	R/W	00h	33.5.27/ 1614
12_0189	AHB Audio DMA Interrupt Mute Control Register (HDMI_IH_MUTE_AHBDMAAUD_STAT0)	8	R/W	00h	33.5.28/ 1615
12_01FF	Global Interrupt Mute Control Register (HDMI_IH_MUTE)	8	R/W	03h	33.5.29/ 1616
12_0200	Video Input Mapping and Internal Data Enable Configuration Register (HDMI_TX_INVID0)	8	R/W	01h	33.5.30/ 1616
12_0201	Video Input Stuffing Enable Register (HDMI_TX_INSTUFFING)	8	R/W	00h	33.5.31/ 1617

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
12_0202	Video Input GY Data Channel Stuffing Register 0 (HDMI_TX_GYDATA0)	8	R/W	00h	33.5.32/ 1618
12_0203	Video Input GY Data Channel Stuffing Register 1 (HDMI_TX_GYDATA1)	8	R/W	00h	33.5.33/ 1619
12_0204	Video Input RCR Data Channel Stuffing Register 0 (HDMI_TX_RCRDATA0)	8	R/W	00h	33.5.34/ 1619
12_0205	Video Input RCR Data Channel Stuffing Register 1 (HDMI_TX_RCRDATA1)	8	R/W	00h	33.5.35/ 1620
12_0206	Video Input RCB Data Channel Stuffing Register 0 (HDMI_TX_BCBDATA0)	8	R/W	00h	33.5.36/ 1620
12_0207	Video Input RCB Data Channel Stuffing Register 1 (HDMI_TX_BCBDATA1)	8	R/W	00h	33.5.37/ 1621
12_0800	Video Packetizer Packing Phase Status Register (HDMI_VP_STATUS)	8	R	00h	33.5.38/ 1621
12_0801	Video Packetizer Pixel Repetition and Color Depth Register (HDMI_VP_PR_CD)	8	R/W	00h	33.5.39/ 1622
12_0802	Video Packetizer Stuffing and Default Packing Phase Register (HDMI_VP_STUFF)	8	R/W	00h	33.5.40/ 1623
12_0803	Video Packetizer YCC422 Remapping Register (HDMI_VP_REMAP)	8	R/W	00h	33.5.41/ 1624
12_0804	Video Packetizer Output, Bypass, and Enable Configuration Register (HDMI_VP_CONF)	8	R/W	46h	33.5.42/ 1625
12_0805	VP_STAT (HDMI_VP_STAT)	8	R	00h	33.5.43/ 1625
12_0806	VP_INT (HDMI_VP_INT)	8	R	00h	33.5.44/ 1626
12_0807	Video Packetizer Interrupt Mask Register (HDMI_VP_MASK)	8	R/W	00h	33.5.45/ 1627
12_0808	VP_POL (HDMI_VP_POL)	8	R/W	FFh	33.5.46/ 1628
12_1000	Frame Composer Input Video Configuration and HDCP Keepout Register (HDMI_FC_INVIDCONF)	8	R/W	70h	33.5.47/ 1629
12_1001	Frame Composer Input Video HActive Pixels Register 0 (HDMI_FC_INHACTIV0)	8	R/W	00h	33.5.48/ 1630
12_1002	Frame Composer Input Video HActive Pixels Register 1 (HDMI_FC_INHACTIV1)	8	R/W	00h	33.5.49/ 1631
12_1003	Frame Composer Input Video HBlank Pixels Register 0 (HDMI_FC_INHBLANK0)	8	R/W	00h	33.5.50/ 1631
12_1004	Frame Composer Input Video HBlank Pixels Register 1 (HDMI_FC_INHBLANK1)	8	R/W	00h	33.5.51/ 1632
12_1005	Frame Composer Input Video VActive Pixels Register 0 (HDMI_FC_INVACTIV0)	8	R/W	00h	33.5.52/ 1633
12_1006	Frame Composer Input Video VActive Pixels Register 1 (HDMI_FC_INVACTIV1)	8	R/W	00h	33.5.53/ 1633

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_1007	Frame Composer Input Video VBlank Pixels Register (HDMI_FC_INVBLANK)	8	R/W	00h	33.5.54/ 1634
12_1008	Frame Composer Input Video HSync Front Porch Register 0 (HDMI_FC_HSYNCINDELAY0)	8	R/W	00h	33.5.55/ 1634
12_1009	Frame Composer Input Video HSync Front Porch Register 1 (HDMI_FC_HSYNCINDELAY1)	8	R/W	00h	33.5.56/ 1635
12_100A	Frame Composer Input Video HSync Width Register 0 (HDMI_FC_HSYNCINWIDTH0)	8	R/W	00h	33.5.57/ 1636
12_100B	Frame Composer Input Video HSync Width Register 1 (HDMI_FC_HSYNCINWIDTH1)	8	R/W	00h	33.5.58/ 1636
12_100C	Frame Composer Input Video VSync Front Porch Register (HDMI_FC_VSYNCINDELAY)	8	R/W	00h	33.5.59/ 1637
12_100D	Frame Composer Input Video VSync Width Register (HDMI_FC_VSYNCINWIDTH)	8	R/W	00h	33.5.60/ 1637
12_100E	Frame Composer Input Video Refresh Rate Register 0 (HDMI_FC_INFREQ0)	8	R/W	00h	33.5.61/ 1638
12_100F	Frame Composer Input Video Refresh Rate Register 1 (HDMI_FC_INFREQ1)	8	R/W	00h	33.5.62/ 1638
12_1010	Frame Composer Input Video Refresh Rate Register 2 (HDMI_FC_INFREQ2)	8	R/W	00h	33.5.63/ 1639
12_1011	Frame Composer Control Period Duration Register (HDMI_FC_CTRLDUR)	8	R/W	00h	33.5.64/ 1640
12_1012	Frame Composer Extended Control Period Duration Register (HDMI_FC_EXCTRLDUR)	8	R/W	00h	33.5.65/ 1640
12_1013	Frame Composer Extended Control Period Maximum Spacing Register (HDMI_FC_EXCTRLSPAC)	8	R/W	00h	33.5.66/ 1641
12_1014	Frame Composer Channel 0 Non-Preamble Data Register (HDMI_FC_CH0PREAM)	8	R/W	00h	33.5.67/ 1641
12_1015	Frame Composer Channel 1 Non-Preamble Data Register (HDMI_FC_CH1PREAM)	8	R/W	00h	33.5.68/ 1642
12_1016	Frame Composer Channel 2 Non-Preamble Data Register (HDMI_FC_CH2PREAM)	8	R/W	00h	33.5.69/ 1642
12_1017	Frame Composer AVI Configuration Register 3 (HDMI_FC_AVICONF3)	8	R/W	00h	33.5.70/ 1643
12_1018	Frame Composer GCP Packet Configuration Register (HDMI_FC_GCP)	8	R/W	00h	33.5.71/ 1643
12_1019	Frame Composer AVI Packet Configuration Register 0 (HDMI_FC_AVICONFO)	8	R/W	00h	33.5.72/ 1644
12_101A	Frame Composer AVI Packet Configuration Register 1 (HDMI_FC_AVICONF1)	8	R/W	00h	33.5.73/ 1645
12_101B	FC_AVICONFFrame Composer AVI Packet Configuration Register 2 (HDMI_FC_AVICONF2)	8	R/W	00h	33.5.74/ 1646
12_101C	Frame Composer AVI Packet VIC Register (HDMI_FC_AVIVID)	8	R/W	00h	33.5.75/ 1647

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_101D	Frame Composer AVI Packet End of Top Bar Register 0 (HDMI_FC_AVIETB0)	8	R/W	00h	33.5.76/ 1647
12_101E	Frame Composer AVI Packet End of Top Bar Register 1 (HDMI_FC_AVIETB1)	8	R/W	00h	33.5.77/ 1648
12_101F	Frame Composer AVI Packet Start of Bottom Bar Register 0 (HDMI_FC_AVISBB0)	8	R/W	00h	33.5.78/ 1648
12_1020	Frame Composer AVI Packet Start of Bottom Bar Register 1 (HDMI_FC_AVISBB1)	8	R/W	00h	33.5.79/ 1649
12_1021	Frame Composer AVI Packet End of Left Bar Register 0 (HDMI_FC_AVIELB0)	8	R/W	00h	33.5.80/ 1649
12_1022	Frame Composer AVI Packet End of Left Bar Register 1 (HDMI_FC_AVIELB1)	8	R/W	00h	33.5.81/ 1650
12_1023	Frame Composer AVI Packet Start of Right Bar Register 0 (HDMI_FC_AVISRBO)	8	R/W	00h	33.5.82/ 1650
12_1024	Frame Composer AVI Packet Start of Right Bar Register 1 (HDMI_FC_AVISRBI)	8	R/W	00h	33.5.83/ 1651
12_1025	Frame Composer AUD Packet Configuration Register 0 (HDMI_FC_AUDICONFO)	8	R/W	00h	33.5.84/ 1651
12_1026	Frame Composer AUD Packet Configuration Register 1 (HDMI_FC_AUDICONF1)	8	R/W	00h	33.5.85/ 1652
12_1027	Frame Composer AUD Packet Configuration Register 2 (HDMI_FC_AUDICONF2)	8	R/W	00h	33.5.86/ 1652
12_1028	Frame Composer AUD Packet Configuration Register 3 (HDMI_FC_AUDICONF3)	8	R/W	00h	33.5.87/ 1653
12_1029	Frame Composer VSI Packet Data IEEE Register 0 (HDMI_FC_VSDIEEEID0)	8	R/W	00h	33.5.88/ 1653
12_102A	Frame Composer VSI Packet Data Size Register (HDMI_FC_VSDSIZE)	8	R/W	1Bh	33.5.89/ 1654
12_1030	Frame Composer VSI Packet Data IEEE Register 1 (HDMI_FC_VSDIEEEID1)	8	R/W	00h	33.5.90/ 1654
12_1031	Frame Composer VSI Packet Data IEEE Register 2 (HDMI_FC_VSDIEEEID2)	8	R/W	00h	33.5.91/ 1655
12_1032	Frame Composer VSI Packet Data IEEE Register 0 (HDMI_FC_VSDPAYLOAD0)	8	R/W	00h	33.5.92/ 1655
12_1033	Frame Composer VSI Packet Data IEEE Register 1 (HDMI_FC_VSDPAYLOAD1)	8	R/W	00h	33.5.93/ 1656
12_1034	Frame Composer VSI Packet Data IEEE Register 2 (HDMI_FC_VSDPAYLOAD2)	8	R/W	00h	33.5.94/ 1656
12_1035	Frame Composer VSI Packet Data IEEE Register 3 (HDMI_FC_VSDPAYLOAD3)	8	R/W	00h	33.5.95/ 1657
12_1036	Frame Composer VSI Packet Data IEEE Register 4 (HDMI_FC_VSDPAYLOAD4)	8	R/W	00h	33.5.96/ 1657
12_1037	Frame Composer VSI Packet Data IEEE Register 5 (HDMI_FC_VSDPAYLOAD5)	8	R/W	00h	33.5.97/ 1658

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
12_1038	Frame Composer VSI Packet Data IEEE Register 6 (HDMI_FC_VSDPAYLOAD6)	8	R/W	00h	33.5.98/ 1658
12_1039	Frame Composer VSI Packet Data IEEE Register 7 (HDMI_FC_VSDPAYLOAD7)	8	R/W	00h	33.5.99/ 1659
12_103A	Frame Composer VSI Packet Data IEEE Register 8 (HDMI_FC_VSDPAYLOAD8)	8	R/W	00h	33.5.100/ 1659
12_103B	Frame Composer VSI Packet Data IEEE Register 9 (HDMI_FC_VSDPAYLOAD9)	8	R/W	00h	33.5.101/ 1660
12_103C	Frame Composer VSI Packet Data IEEE Register 10 (HDMI_FC_VSDPAYLOAD10)	8	R/W	00h	33.5.102/ 1660
12_103D	Frame Composer VSI Packet Data IEEE Register 11 (HDMI_FC_VSDPAYLOAD11)	8	R/W	00h	33.5.103/ 1661
12_103E	Frame Composer VSI Packet Data IEEE Register 12 (HDMI_FC_VSDPAYLOAD12)	8	R/W	00h	33.5.104/ 1661
12_103F	Frame Composer VSI Packet Data IEEE Register 13 (HDMI_FC_VSDPAYLOAD13)	8	R/W	00h	33.5.105/ 1662
12_1040	Frame Composer VSI Packet Data IEEE Register 14 (HDMI_FC_VSDPAYLOAD14)	8	R/W	00h	33.5.106/ 1662
12_1041	Frame Composer VSI Packet Data IEEE Register 15 (HDMI_FC_VSDPAYLOAD15)	8	R/W	00h	33.5.107/ 1663
12_1042	Frame Composer VSI Packet Data IEEE Register 16 (HDMI_FC_VSDPAYLOAD16)	8	R/W	00h	33.5.108/ 1663
12_1043	Frame Composer VSI Packet Data IEEE Register 17 (HDMI_FC_VSDPAYLOAD17)	8	R/W	00h	33.5.109/ 1664
12_1044	Frame Composer VSI Packet Data IEEE Register 18 (HDMI_FC_VSDPAYLOAD18)	8	R/W	00h	33.5.110/ 1664
12_1045	Frame Composer VSI Packet Data IEEE Register 19 (HDMI_FC_VSDPAYLOAD19)	8	R/W	00h	33.5.111/ 1665
12_1046	Frame Composer VSI Packet Data IEEE Register 20 (HDMI_FC_VSDPAYLOAD20)	8	R/W	00h	33.5.112/ 1665
12_1047	Frame Composer VSI Packet Data IEEE Register 21 (HDMI_FC_VSDPAYLOAD21)	8	R/W	00h	33.5.113/ 1666
12_1048	Frame Composer VSI Packet Data IEEE Register 22 (HDMI_FC_VSDPAYLOAD22)	8	R/W	00h	33.5.114/ 1666
12_1049	Frame Composer VSI Packet Data IEEE Register 23 (HDMI_FC_VSDPAYLOAD23)	8	R/W	00h	33.5.115/ 1667
12_104A	Frame Composer SPD Packet Data Vendor Name Register 0 (HDMI_FC_SPDVENDORNAME0)	8	R/W	00h	33.5.116/ 1667
12_1052	Frame Composer SPD Packet Data Product Name Register 0 (HDMI_FC_SPDPRODUCTNAME0)	8	R/W	00h	33.5.117/ 1668
12_1062	Frame Composer SPD Packet Data Source Product Descriptor Register (HDMI_FC_SPDDEVICEINF)	8	R/W	00h	33.5.118/ 1668
12_1063	Frame Composer Audio Sample Flat and Layout Configuration Register (HDMI_FC_AUDSCONF)	8	R/W	00h	33.5.119/ 1669

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_1064	Frame Composer Audio Packet Sample Present Status Register (HDMI_FC_AUDSSTAT)	8	R	00h	33.5.120/ 1669
12_1073	Frame Composer Number of High Priority Packets Attended Configuration Register (HDMI_FC_CTRLQHIGH)	8	R/W	0Fh	33.5.121/ 1670
12_1074	Frame Composer Number of Low Priority Packets Attended Configuration Register (HDMI_FC_CTRLQLOW)	8	R/W	03h	33.5.122/ 1671
12_1075	Frame Composer ACP Packet Type Configuration Register 0 (HDMI_FC_ACP0)	8	R/W	00h	33.5.123/ 1671
12_1091	Frame Composer ACP Packet Type Configuration Register 1 (HDMI_FC_ACP1)	8	R/W	00h	33.5.124/ 1672
12_1092	FC_ISCR1_Frame Composer Packet Status, Valid, and Continue Configuration Register (HDMI_FC_ISCR1_0)	8	R/W	00h	33.5.125/ 1672
12_1093	Frame Composer ISCR1 Packet Body Register 1 (HDMI_FC_ISCR1_1)	8	R/W	00h	33.5.126/ 1673
12_10A3	Frame Composer ISCR2 Packet Body Register 0 (HDMI_FC_ISCR2_0)	8	R/W	00h	33.5.127/ 1673
12_10B3	Frame Composer Data Island Auto Packet Scheduling Register 0 (HDMI_FC_DATAUTO0)	8	R/W	00h	33.5.128/ 1674
12_10B4	Frame Composer Data Island Auto Packet Scheduling Register 1 (HDMI_FC_DATAUTO1)	8	R/W	00h	33.5.129/ 1675
12_10B5	Frame Composer Data Island Auto Packet Scheduling Register 2 (HDMI_FC_DATAUTO2)	8	R/W	00h	33.5.130/ 1675
12_10B6	Frame Composer Data Island Manual Packet Request Register (HDMI_FC_DATMAN)	8	W	00h	33.5.131/ 1676
12_10B7	Frame Composer Data Island Auto Packet Scheduling Register 3 (HDMI_FC_DATAUTO3)	8	R/W	0Fh	33.5.132/ 1677
12_10B8	Frame Composer Round Robin ACR Packet Insertion Register 0 (HDMI_FC_RDRB0)	8	R/W	00h	33.5.133/ 1678
12_10B9	Frame Composer Round Robin ACR Packet Insertion Register 1 (HDMI_FC_RDRB1)	8	R/W	00h	33.5.134/ 1678
12_10BA	Frame Composer Round Robin ACR Packet Insertion Register 2 (HDMI_FC_RDRB2)	8	R/W	00h	33.5.135/ 1679
12_10BB	Frame Composer Round Robin ACR Packet Insertion Register 3 (HDMI_FC_RDRB3)	8	R/W	00h	33.5.136/ 1679
12_10BC	Frame Composer Round Robin ACR Packet Insertion Register 4 (HDMI_FC_RDRB4)	8	R/W	00h	33.5.137/ 1680
12_10BD	Frame Composer Round Robin ACR Packet Insertion Register 5 (HDMI_FC_RDRB5)	8	R/W	00h	33.5.138/ 1680
12_10BE	Frame Composer Round Robin ACR Packet Insertion Register 6 (HDMI_FC_RDRB6)	8	R/W	00h	33.5.139/ 1681
12_10BF	Frame Composer Round Robin ACR Packet Insertion Register 7 (HDMI_FC_RDRB7)	8	R/W	00h	33.5.140/ 1682
12_10D0	FC_STAT0 (HDMI_FC_STAT0)	8	R	00h	33.5.141/ 1682

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
12_10D1	FC_INT0 (HDMI_FC_INT0)	8	R/W	00h	33.5.142/ 1683
12_10D2	Frame Composer Packet Interrupt Mask Register 0 (HDMI_FC_MASK0)	8	R/W	25h	33.5.143/ 1684
12_10D3	FC_POL0 (HDMI_FC_POL0)	8	R/W	FFh	33.5.144/ 1685
12_10D4	FC_STAT1 (HDMI_FC_STAT1)	8	R/W	00h	33.5.145/ 1686
12_10D5	FC_INT1 (HDMI_FC_INT1)	8	R/W	00h	33.5.146/ 1686
12_10D6	Frame Composer Packet Interrupt Mask Register 1 (HDMI_FC_MASK1)	8	R/W	00h	33.5.147/ 1687
12_10D7	FC_POL1 (HDMI_FC_POL1)	8	R/W	FFh	33.5.148/ 1688
12_10D8	FC_STAT2 (HDMI_FC_STAT2)	8	R/W	00h	33.5.149/ 1689
12_10D9	FC_INT2 (HDMI_FC_INT2)	8	R/W	00h	33.5.150/ 1690
12_10DA	Frame Composer High/Low Priority Overflow Interrupt Mask Register 2 (HDMI_FC_MASK2)	8	R/W	00h	33.5.151/ 1690
12_10DB	FC_POL2 (HDMI_FC_POL2)	8	R/W	03h	33.5.152/ 1691
12_10E0	Frame Composer Pixel Repetition Configuration Register (HDMI_FC_PRCNF)	8	R/W	10h	33.5.153/ 1692
12_1100	Frame Composer GMD Packet Status Register (HDMI_FC_GMD_STAT)	8	R	00h	33.5.154/ 1693
12_1101	Frame Composer GMD Packet Enable Register (HDMI_FC_GMD_EN)	8	R/W	00h	33.5.155/ 1694
12_1102	Frame Composer GMD Packet Update Register (HDMI_FC_GMD_UP)	8	W	00h	33.5.156/ 1694
12_1103	Frame Composer GMD Packet Schedule Configuration Register (HDMI_FC_GMD_CONF)	8	R/W	10h	33.5.157/ 1695
12_1104	Frame Composer GMD Packet Profile and Gamut Sequence Configuration Register (HDMI_FC_GMD_HB)	8	R/W	00h	33.5.158/ 1696
12_1105	Frame Composer GMD Packet Body Register 0 (HDMI_FC_GMD_PB0)	8	R/W	00h	33.5.159/ 1696
12_1106	Frame Composer GMD Packet Body Register 1 (HDMI_FC_GMD_PB1)	8	R/W	00h	33.5.160/ 1697
12_1107	Frame Composer GMD Packet Body Register 2 (HDMI_FC_GMD_PB2)	8	R/W	00h	33.5.161/ 1697
12_1108	Frame Composer GMD Packet Body Register 3 (HDMI_FC_GMD_PB3)	8	R/W	00h	33.5.162/ 1698
12_1109	Frame Composer GMD Packet Body Register 4 (HDMI_FC_GMD_PB4)	8	R/W	00h	33.5.163/ 1698

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
12_110A	Frame Composer GMD Packet Body Register 5 (HDMI_FC_GMD_PB5)	8	R/W	00h	33.5.164/ 1699
12_110B	Frame Composer GMD Packet Body Register 6 (HDMI_FC_GMD_PB6)	8	R/W	00h	33.5.165/ 1699
12_110C	Frame Composer GMD Packet Body Register 7 (HDMI_FC_GMD_PB7)	8	R/W	00h	33.5.166/ 1700
12_110D	Frame Composer GMD Packet Body Register 8 (HDMI_FC_GMD_PB8)	8	R/W	00h	33.5.167/ 1700
12_110E	Frame Composer GMD Packet Body Register 9 (HDMI_FC_GMD_PB9)	8	R/W	00h	33.5.168/ 1701
12_110F	Frame Composer GMD Packet Body Register 10 (HDMI_FC_GMD_PB10)	8	R/W	00h	33.5.169/ 1701
12_1110	Frame Composer GMD Packet Body Register 11 (HDMI_FC_GMD_PB11)	8	R/W	00h	33.5.170/ 1702
12_1111	Frame Composer GMD Packet Body Register 12 (HDMI_FC_GMD_PB12)	8	R/W	00h	33.5.171/ 1702
12_1112	Frame Composer GMD Packet Body Register 13 (HDMI_FC_GMD_PB13)	8	R/W	00h	33.5.172/ 1703
12_1113	Frame Composer GMD Packet Body Register 14 (HDMI_FC_GMD_PB14)	8	R/W	00h	33.5.173/ 1703
12_1114	Frame Composer GMD Packet Body Register 15 (HDMI_FC_GMD_PB15)	8	R/W	00h	33.5.174/ 1704
12_1115	Frame Composer GMD Packet Body Register 16 (HDMI_FC_GMD_PB16)	8	R/W	00h	33.5.175/ 1704
12_1116	Frame Composer GMD Packet Body Register 17 (HDMI_FC_GMD_PB17)	8	R/W	00h	33.5.176/ 1705
12_1117	Frame Composer GMD Packet Body Register 18 (HDMI_FC_GMD_PB18)	8	R/W	00h	33.5.177/ 1705
12_1118	Frame Composer GMD Packet Body Register 19 (HDMI_FC_GMD_PB19)	8	R/W	00h	33.5.178/ 1706
12_1119	Frame Composer GMD Packet Body Register 20 (HDMI_FC_GMD_PB20)	8	R/W	00h	33.5.179/ 1706
12_111A	Frame Composer GMD Packet Body Register 21 (HDMI_FC_GMD_PB21)	8	R/W	00h	33.5.180/ 1707
12_111B	Frame Composer GMD Packet Body Register 22 (HDMI_FC_GMD_PB22)	8	R/W	00h	33.5.181/ 1707
12_111C	Frame Composer GMD Packet Body Register 23 (HDMI_FC_GMD_PB23)	8	R/W	00h	33.5.182/ 1708
12_111D	Frame Composer GMD Packet Body Register 24 (HDMI_FC_GMD_PB24)	8	R/W	00h	33.5.183/ 1708
12_111E	Frame Composer GMD Packet Body Register 25 (HDMI_FC_GMD_PB25)	8	R/W	00h	33.5.184/ 1709
12_111F	Frame Composer GMD Packet Body Register 26 (HDMI_FC_GMD_PB26)	8	R/W	00h	33.5.185/ 1709

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_1120	Frame Composer GMD Packet Body Register 27 (HDMI_FC_GMD_PB27)	8	R/W	00h	33.5.186/ 1710
12_1200	Frame Composer Video/Audio Force Enable Register (HDMI_FC_DBGFORCE)	8	R/W	00h	33.5.187/ 1710
12_1201	Frame Composer Audio Channel 0 Register 0 (HDMI_FC_DBGAUD0CH0)	8	R/W	00h	33.5.188/ 1711
12_1202	Frame Composer Audio Channel 0 Register 1 (HDMI_FC_DBGAUD1CH0)	8	R/W	00h	33.5.189/ 1712
12_1203	Frame Composer Audio Channel 0 Register 2 (HDMI_FC_DBGAUD2CH0)	8	R/W	00h	33.5.190/ 1712
12_1204	Frame Composer Audio Channel 1 Register 0 (HDMI_FC_DBGAUD0CH1)	8	R/W	00h	33.5.191/ 1713
12_1205	Frame Composer Audio Channel 1 Register 1 (HDMI_FC_DBGAUD1CH1)	8	R/W	00h	33.5.192/ 1713
12_1206	Frame Composer Audio Channel 1 Register 2 (HDMI_FC_DBGAUD2CH1)	8	R/W	00h	33.5.193/ 1714
12_1207	Frame Composer Debug Audio Channel 2 Register 0 (HDMI_FC_DBGAUD0CH2)	8	R/W	00h	33.5.194/ 1714
12_1208	Frame Composer Debug Audio Channel 2 Register 1 (HDMI_FC_DBGAUD1CH2)	8	R/W	00h	33.5.195/ 1715
12_1209	Frame Composer Audio Channel 2 Register 2 (HDMI_FC_DBGAUD2CH2)	8	R/W	00h	33.5.196/ 1715
12_120A	Frame Composer Audio Channel 3 Register 0 (HDMI_FC_DBGAUD0CH3)	8	R/W	00h	33.5.197/ 1716
12_120B	Frame Composer Audio Channel 3 Register 1 (HDMI_FC_DBGAUD1CH3)	8	R/W	00h	33.5.198/ 1716
12_120C	Frame Composer Audio Channel 3 Register 2 (HDMI_FC_DBGAUD2CH3)	8	R/W	00h	33.5.199/ 1717
12_120D	Frame Composer Audio Channel 4 Register 0 (HDMI_FC_DBGAUD0CH4)	8	R/W	00h	33.5.200/ 1717
12_120E	Frame Composer Audio Channel 4 Register 1 (HDMI_FC_DBGAUD1CH4)	8	R/W	00h	33.5.201/ 1718
12_120F	Frame Composer Audio Channel 4 Register 2 (HDMI_FC_DBGAUD2CH4)	8	R/W	00h	33.5.202/ 1718
12_1210	Frame Composer Audio Channel 5 Register 0 (HDMI_FC_DBGAUD0CH5)	8	R/W	00h	33.5.203/ 1719
12_1211	Frame Composer Audio Channel 5 Register 1 (HDMI_FC_DBGAUD1CH5)	8	R/W	00h	33.5.204/ 1719
12_1212	Frame Composer Audio Channel 5 Register 2 (HDMI_FC_DBGAUD2CH5)	8	R/W	00h	33.5.205/ 1720
12_1213	Frame Composer Audio Channel 6 Register 0 (HDMI_FC_DBGAUD0CH6)	8	R/W	00h	33.5.206/ 1720
12_1214	Frame Composer Audio Channel 6 Register 1 (HDMI_FC_DBGAUD1CH6)	8	R/W	00h	33.5.207/ 1721

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_1215	Frame Composer Audio Channel 6 Register 2 (HDMI_FC_DBGAUD2CH6)	8	R/W	00h	33.5.208/1721
12_1216	Frame Composer Audio Channel 7 Register 1 (HDMI_FC_DBGAUD0CH7)	8	R/W	00h	33.5.209/1722
12_1217	Frame Composer Audio Channel 7 Register 0 (HDMI_FC_DBGAUD1CH7)	8	R/W	00h	33.5.210/1722
12_1218	Frame Composer Audio Channel 7 Register 2 (HDMI_FC_DBGAUD2CH7)	8	R/W	00h	33.5.211/1723
12_1219	Frame Composer TMDS Channel 0 Register (HDMI_FC_DBGTMDS0)	8	R/W	00h	33.5.212/1723
12_121A	Frame Composer TMDS Channel 1 Register (HDMI_FC_DBGTMDS1)	8	R/W	00h	33.5.213/1724
12_121B	Frame Composer TMDS Channel 2 Register (HDMI_FC_DBGTMDS2)	8	R/W	00h	33.5.214/1724
12_3000	PHY Configuration Register (HDMI_PHY_CONF0)	8	R/W	06h	33.5.215/1725
12_3001	PHY Test Interface Register 0 (HDMI_PHY_TST0)	8	R/W	00h	33.5.216/1726
12_3002	PHY Test Interface Register 1 (HDMI_PHY_TST1)	8	R/W	00h	33.5.217/1726
12_3003	PHY Test Interface Register 2 (HDMI_PHY_TST2)	8	R	00h	33.5.218/1727
12_3004	PHY RXSENSE, PLL lock, and HPD Status Register (HDMI_PHY_STAT0)	8	R	00h	33.5.219/1727
12_3005	PHY RXSENSE, PLL lock, and HPD Interrupt Register (HDMI_PHY_INT0)	8	R	00h	33.5.220/1728
12_3006	PHY RXSENSE, PLL lock, and HPD Mask Register (HDMI_PHY_MASK0)	8	R/W	00h	33.5.221/1729
12_3007	PHY RXSENSE, PLL lock and HPD Polarity Register (HDMI_PHY_POL0)	8	R/W	F3h	33.5.222/1730
12_3020	PHY I2C Slave Address Configuration Register (HDMI_PHY_I2CM_SLAVE_ADDR)	8	R/W	00h	33.5.223/1731
12_3021	PHY I2C Address Configuration Register (HDMI_PHY_I2CM_ADDRESS_ADDR)	8	R/W	00h	33.5.224/1731
12_3022	PHY I2C Data Write Register 1 (HDMI_PHY_I2CM_DATAO_1_ADDR)	8	R/W	00h	33.5.225/1732
12_3023	PHY I2C Data Write Register 0 (HDMI_PHY_I2CM_DATAO_0_ADDR)	8	R/W	00h	33.5.226/1733
12_3024	PHY I2C Data Read Register 1 (HDMI_PHY_I2CM_DATAI_1_ADDR)	8	R	00h	33.5.227/1733
12_3025	PHY I2C Data Read Register 0 (HDMI_PHY_I2CM_DATAI_0_ADDR)	8	R/W	00h	33.5.228/1734
12_3026	PHY I2C Read/Write Operation (HDMI_PHY_I2CM_OPERATION_ADDR)	8	W	00h	33.5.229/1734

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_3027	PHY I2C Done Interrupt Register (HDMI_PHY_I2CM_INT_ADDR)	8	R/W	08h	33.5.230/ 1735
12_3028	PHY I2C Done Interrupt Register (HDMI_PHY_I2CM_CTLINT_ADDR)	8	R/W	88h	33.5.231/ 1736
12_3029	PHY I2C Speed Control Register (HDMI_PHY_I2CM_DIV_ADDR)	8	R/W	0Bh	33.5.232/ 1737
12_302A	PHY I2C Software Reset Register (HDMI_PHY_I2CM_SOFTRSTZ_ADDR)	8	R/W	01h	33.5.233/ 1737
12_302B	PHY I2C Slow Speed SCL High Level Control Register 1 (HDMI_PHY_I2CM_SS_SCL_HCNT_1_ADDR)	8	R/W	00h	33.5.234/ 1738
12_302C	PHY I2C Slow Speed SCL High Level Control Register 0 (HDMI_PHY_I2CM_SS_SCL_HCNT_0_ADDR)	8	R/W	6Ch	33.5.235/ 1739
12_302D	PHY I2C Slow Speed SCL Low Level Control Register 1 (HDMI_PHY_I2CM_SS_SCL_LCNT_1_ADDR)	8	R/W	00h	33.5.236/ 1739
12_302E	PHY I2C Slow Speed SCL Low Level Control Register 0 (HDMI_PHY_I2CM_SS_SCL_LCNT_0_ADDR)	8	R/W	7Fh	33.5.237/ 1740
12_302F	PHY I2C Fast Speed SCL High Level Control Register 1 (HDMI_PHY_I2CM_FS_SCL_HCNT_1_ADDR)	8	R/W	00h	33.5.238/ 1740
12_3030	PHY I2C Fast Speed SCL High Level Control Register 0 (HDMI_PHY_I2CM_FS_SCL_HCNT_0_ADDR)	8	R/W	11h	33.5.239/ 1741
12_3031	PHY I2C Fast Speed SCL Low Level Control Register 1 (HDMI_PHY_I2CM_FS_SCL_LCNT_1_ADDR)	8	R/W	00h	33.5.240/ 1741
12_3032	PHY I2C Fast Speed SCL Low Level Control Register 0 (HDMI_PHY_I2CM_FS_SCL_LCNT_0_ADDR)	8	R/W	24h	33.5.241/ 1742
12_3200	Audio Clock Regenerator N Value Register 1 (HDMI_AUD_N1)	8	R/W	00h	33.5.242/ 1742
12_3201	Audio Clock Regenerator N Value Register 2 (HDMI_AUD_N2)	8	R/W	00h	33.5.243/ 1743
12_3202	Audio Clock Regenerator N Value Register 3 (HDMI_AUD_N3)	8	R/W	00h	33.5.244/ 1743
12_3203	AUD_CTS1 (HDMI_AUD_CTS1)	8	R/W	00h	33.5.245/ 1744
12_3204	AUD_CTS2 (HDMI_AUD_CTS2)	8	R/W	00h	33.5.246/ 1744
12_3205	AUD_CTS3 (HDMI_AUD_CTS3)	8	R/W	00h	33.5.247/ 1745
12_3600	Audio DMA Start Register (HDMI_AHB_DMA_CONF0)	8	R/W	00h	33.5.248/ 1745
12_3601	AHB_DMA_START (HDMI_AHB_DMA_START)	8	R/W	00h	33.5.249/ 1746
12_3602	Audio DMA Stop Register (HDMI_AHB_DMA_STOP)	8	R/W	00h	33.5.250/ 1747
12_3603	Audio DMA FIFO Threshold Register (HDMI_AHB_DMA_THRSLD)	8	R/W	00h	33.5.251/ 1748

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_3604	Audio DMA Start Address Register 0 (HDMI_AHB_DMA_STRADDR0)	8	R/W	00h	33.5.252/ 1748
12_3605	Audio DMA Start Address Register 1 (HDMI_AHB_DMA_STRADDR1)	8	R/W	00h	33.5.253/ 1749
12_3606	Audio DMA Start Address Register 2 (HDMI_AHB_DMA_STRADDR2)	8	R/W	00h	33.5.254/ 1749
12_3607	Audio DMA Start Address Register 3 (HDMI_AHB_DMA_STRADDR3)	8	R/W	00h	33.5.255/ 1750
12_3608	Audio DMA Stop Address Register 0 (HDMI_AHB_DMA_STPADDR0)	8	R/W	00h	33.5.256/ 1750
12_3609	Audio DMA Stop Address Register 1 (HDMI_AHB_DMA_STPADDR1)	8	R/W	00h	33.5.257/ 1751
12_360A	Audio DMA Stop Address Register 2 (HDMI_AHB_DMA_STPADDR2)	8	R/W	00h	33.5.258/ 1751
12_360B	Audio DMA Stop Address Register 3 (HDMI_AHB_DMA_STPADDR3)	8	R/W	00h	33.5.259/ 1752
12_360C	Audio DMA Burst Start Address Register 0 (HDMI_AHB_DMA_BSTADDR0)	8	R	00h	33.5.260/ 1752
12_360D	Audio DMA Burst Start Address Register 1 (HDMI_AHB_DMA_BSTADDR1)	8	R	00h	33.5.261/ 1753
12_360E	Audio DMA Burst Start Address Register 2 (HDMI_AHB_DMA_BSTADDR2)	8	R	00h	33.5.262/ 1753
12_360F	Audio DMA Burst Start Address Register 3 (HDMI_AHB_DMA_BSTADDR3)	8	R	00h	33.5.263/ 1753
12_3610	Audio DMA Burst Length Register 0 (HDMI_AHB_DMA_MBLENGTH0)	8	R	00h	33.5.264/ 1754
12_3611	Audio DMA Burst Length Register 1 (HDMI_AHB_DMA_MBLENGTH1)	8	R	00h	33.5.265/ 1755
12_3612	Audio DMA Interrupt Status Register (HDMI_AHB_DMA_STAT)	8	R	00h	33.5.266/ 1755
12_3613	Audio DMA Interrupt Register (HDMI_AHB_DMA_INT)	8	R	00h	33.5.267/ 1756
12_3614	Audio DMA Mask Interrupt Register (HDMI_AHB_DMA_MASK)	8	R/W	00h	33.5.268/ 1757
12_3615	Audio DMA Polarity Interrupt Register (HDMI_AHB_DMA_POL)	8	R/W	00h	33.5.269/ 1758
12_3616	Audio DMA Channel Enable Configuration Register 1 (HDMI_AHB_DMA_CONF1)	8	R/W	00h	33.5.270/ 1759
12_3617	Audio DMA Buffer Interrupt Status Register (HDMI_AHB_DMA_BUFFSTAT)	8	R	00h	33.5.271/ 1760
12_3618	Audio DMA Buffer Interrupt Register (HDMI_AHB_DMA_BUFFINT)	8	R	00h	33.5.272/ 1761
12_3619	Audio DMA Buffer Mask Interrupt Register (HDMI_AHB_DMA_BUFFMASK)	8	R/W	00h	33.5.273/ 1762

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_361A	Audio DMA Buffer Polarity Interrupt Register (HDMI_AHB_DMA_BUFFPOL)	8	R/W	00h	33.5.274/ 1762
12_4001	Main Controller Synchronous Clock Domain Disable Register (HDMI_MC_CLKDIS)	8	R/W	00h	33.5.275/ 1763
12_4002	Main Controller Software Reset Register (HDMI_MC_SWRSTZREQ)	8	R/W	FFh	33.5.276/ 1764
12_4004	Main Controller Feed Through Control Register (HDMI_MC_FLOWCTRL)	8	R/W	00h	33.5.277/ 1765
12_4005	Main Controller PHY Reset Register (HDMI_MC_PHYRSTZ)	8	R/W	00h	33.5.278/ 1765
12_4006	Main Controller Clock Present Register (HDMI_MC_LOCKONCLOCK)	8	w1c	00h	33.5.279/ 1766
12_4007	Main Controller HEAC PHY Reset Register (HDMI_MC_HEACPHY_RST)	8	R/W	00h	33.5.280/ 1767
12_4100	Color Space Converter Interpolation and Decimation Configuration Register (HDMI_CSC_CFG)	8	R/W	00h	33.5.281/ 1767
12_4101	Color Space Converter Scale and Deep Color Configuration Register (HDMI_CSC_SCALE)	8	R/W	01h	33.5.282/ 1768
12_4102	CSC_COEF_A1_MSB (HDMI_CSC_COEF_A1_MSB)	8	R/W	20h	33.5.283/ 1769
12_4103	CSC_COEF_A1_LSB (HDMI_CSC_COEF_A1_LSB)	8	R/W	00h	33.5.284/ 1769
12_4104	CSC_COEF_A2_MSB (HDMI_CSC_COEF_A2_MSB)	8	R/W	00h	33.5.285/ 1770
12_4105	CSC_COEF_A2_LSB (HDMI_CSC_COEF_A2_LSB)	8	R/W	00h	33.5.286/ 1770
12_4106	CSC_COEF_A3_MSB (HDMI_CSC_COEF_A3_MSB)	8	R/W	00h	33.5.287/ 1771
12_4107	CSC_COEF_A3_LSB (HDMI_CSC_COEF_A3_LSB)	8	R/W	00h	33.5.288/ 1771
12_4108	CSC_COEF_A4_MSB (HDMI_CSC_COEF_A4_MSB)	8	R/W	00h	33.5.289/ 1772
12_4109	CSC_COEF_A4_LSB (HDMI_CSC_COEF_A4_LSB)	8	R/W	00h	33.5.290/ 1772
12_410A	CSC_COEF_B1_MSB (HDMI_CSC_COEF_B1_MSB)	8	R/W	00h	33.5.291/ 1773
12_410B	CSC_COEF_B1_LSB (HDMI_CSC_COEF_B1_LSB)	8	R/W	00h	33.5.292/ 1773
12_410C	CSC_COEF_B2_MSB (HDMI_CSC_COEF_B2_MSB)	8	R/W	20h	33.5.293/ 1774
12_410D	CSC_COEF_B2_LSB (HDMI_CSC_COEF_B2_LSB)	8	R/W	00h	33.5.294/ 1774
12_410E	CSC_COEF_B3_MSB (HDMI_CSC_COEF_B3_MSB)	8	R/W	00h	33.5.295/ 1775

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_410F	CSC_COEF_B3_LSB (HDMI_CSC_COEF_B3_LSB)	8	R/W	00h	33.5.296/1775
12_4110	CSC_COEF_B4_MSB (HDMI_CSC_COEF_B4_MSB)	8	R/W	00h	33.5.297/1776
12_4111	CSC_COEF_B4_LSB (HDMI_CSC_COEF_B4_LSB)	8	R/W	00h	33.5.298/1776
12_4112	CSC_COEF_C1_MSB (HDMI_CSC_COEF_C1_MSB)	8	R/W	00h	33.5.299/1777
12_4113	CSC_COEF_C1_LSB (HDMI_CSC_COEF_C1_LSB)	8	R/W	00h	33.5.300/1777
12_4114	CSC_COEF_C2_MSB (HDMI_CSC_COEF_C2_MSB)	8	R/W	00h	33.5.301/1778
12_4115	CSC_COEF_C2_LSB (HDMI_CSC_COEF_C2_LSB)	8	R/W	00h	33.5.302/1778
12_4116	CSC_COEF_C3_MSB (HDMI_CSC_COEF_C3_MSB)	8	R/W	20h	33.5.303/1779
12_4117	CSC_COEF_C3_LSB (HDMI_CSC_COEF_C3_LSB)	8	R/W	00h	33.5.304/1779
12_4118	CSC_COEFC4_MSB (HDMI_CSC_COEFC4_MSB)	8	R/W	00h	33.5.305/1780
12_4119	CSC_COEFC4_LSB (HDMI_CSC_COEFC4_LSB)	8	R/W	00h	33.5.306/1780
12_7D00	CEC_CTRL (HDMI_CEC_CTRL)	8	R/W	02h	33.5.307/1781
12_7D01	CEC_STAT (HDMI_CEC_STAT)	8	R	00h	33.5.308/1782
12_7D02	CEC_MASK (HDMI_CEC_MASK)	8	R/W	00h	33.5.309/1783
12_7D03	CEC_POLARITY (HDMI_CEC_POLARITY)	8	R/W	7Fh	33.5.310/1784
12_7D04	CEC_INT (HDMI_CEC_INT)	8	R	00h	33.5.311/1785
12_7D05	CEC_ADDR_L (HDMI_CEC_ADDR_L)	8	R/W	00h	33.5.312/1786
12_7D06	CEC_ADDR_H (HDMI_CEC_ADDR_H)	8	R/W	80h	33.5.313/1787
12_7D07	CEC_TX_CNT (HDMI_CEC_TX_CNT)	8	R/W	00h	33.5.314/1788
12_7D08	CEC_RX_CNT (HDMI_CEC_RX_CNT)	8	R	00h	33.5.315/1789
12_7D10	CEC_TX_DATA (HDMI_CEC_TX_DATA0)	8	R/W	00h	33.5.316/1790
12_7D11	CEC_TX_DATA (HDMI_CEC_TX_DATA1)	8	R/W	00h	33.5.316/1790

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HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_7D12	CEC_TX_DATA (HDMI_CEC_TX_DATA2)	8	R/W	00h	33.5.316/1790
12_7D13	CEC_TX_DATA (HDMI_CEC_TX_DATA3)	8	R/W	00h	33.5.316/1790
12_7D14	CEC_TX_DATA (HDMI_CEC_TX_DATA4)	8	R/W	00h	33.5.316/1790
12_7D15	CEC_TX_DATA (HDMI_CEC_TX_DATA5)	8	R/W	00h	33.5.316/1790
12_7D16	CEC_TX_DATA (HDMI_CEC_TX_DATA6)	8	R/W	00h	33.5.316/1790
12_7D17	CEC_TX_DATA (HDMI_CEC_TX_DATA7)	8	R/W	00h	33.5.316/1790
12_7D18	CEC_TX_DATA (HDMI_CEC_TX_DATA8)	8	R/W	00h	33.5.316/1790
12_7D19	CEC_TX_DATA (HDMI_CEC_TX_DATA9)	8	R/W	00h	33.5.316/1790
12_7D1A	CEC_TX_DATA (HDMI_CEC_TX_DATA10)	8	R/W	00h	33.5.316/1790
12_7D1B	CEC_TX_DATA (HDMI_CEC_TX_DATA11)	8	R/W	00h	33.5.316/1790
12_7D1C	CEC_TX_DATA (HDMI_CEC_TX_DATA12)	8	R/W	00h	33.5.316/1790
12_7D1D	CEC_TX_DATA (HDMI_CEC_TX_DATA13)	8	R/W	00h	33.5.316/1790
12_7D1E	CEC_TX_DATA (HDMI_CEC_TX_DATA14)	8	R/W	00h	33.5.316/1790
12_7D1F	CEC_TX_DATA (HDMI_CEC_TX_DATA15)	8	R/W	00h	33.5.316/1790
12_7D20	CEC_RX_DATA (HDMI_CEC_RX_DATA0)	8	R	00h	33.5.317/1790
12_7D21	CEC_RX_DATA (HDMI_CEC_RX_DATA1)	8	R	00h	33.5.317/1790
12_7D22	CEC_RX_DATA (HDMI_CEC_RX_DATA2)	8	R	00h	33.5.317/1790
12_7D23	CEC_RX_DATA (HDMI_CEC_RX_DATA3)	8	R	00h	33.5.317/1790
12_7D24	CEC_RX_DATA (HDMI_CEC_RX_DATA4)	8	R	00h	33.5.317/1790
12_7D25	CEC_RX_DATA (HDMI_CEC_RX_DATA5)	8	R	00h	33.5.317/1790
12_7D26	CEC_RX_DATA (HDMI_CEC_RX_DATA6)	8	R	00h	33.5.317/1790
12_7D27	CEC_RX_DATA (HDMI_CEC_RX_DATA7)	8	R	00h	33.5.317/1790

Table continues on the next page...

HDMI memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_7D28	CEC_RX_DATA (HDMI_CEC_RX_DATA8)	8	R	00h	33.5.317/ 1790
12_7D29	CEC_RX_DATA (HDMI_CEC_RX_DATA9)	8	R	00h	33.5.317/ 1790
12_7D2A	CEC_RX_DATA (HDMI_CEC_RX_DATA10)	8	R	00h	33.5.317/ 1790
12_7D2B	CEC_RX_DATA (HDMI_CEC_RX_DATA11)	8	R	00h	33.5.317/ 1790
12_7D2C	CEC_RX_DATA (HDMI_CEC_RX_DATA12)	8	R	00h	33.5.317/ 1790
12_7D2D	CEC_RX_DATA (HDMI_CEC_RX_DATA13)	8	R	00h	33.5.317/ 1790
12_7D2E	CEC_RX_DATA (HDMI_CEC_RX_DATA14)	8	R	00h	33.5.317/ 1790
12_7D2F	CEC_RX_DATA (HDMI_CEC_RX_DATA15)	8	R	00h	33.5.317/ 1790
12_7D30	CEC_LOCK (HDMI_CEC_LOCK)	8	R/W	00h	33.5.318/ 1791
12_7D31	CEC_WKUPCTRL (HDMI_CEC_WKUPCTRL)	8	R/W	FFh	33.5.319/ 1791
12_7E00	I2CM_SLAVE (HDMI_I2CM_SLAVE)	8	R/W	00h	33.5.320/ 1792
12_7E01	I2CM_ADDRESS (HDMI_I2CM_ADDRESS)	8	R/W	00h	33.5.321/ 1793
12_7E02	I2CM_DATAO (HDMI_I2CM_DATAO)	8	R/W	00h	33.5.322/ 1793
12_7E03	I2CM_DATAI (HDMI_I2CM_DATAI)	8	R	00h	33.5.323/ 1794
12_7E04	I2CM_OPERATION (HDMI_I2CM_OPERATION)	8	W	00h	33.5.324/ 1794
12_7E05	I2CM_INT (HDMI_I2CM_INT)	8	R/W	08h	33.5.325/ 1795
12_7E06	I2CM_CTLINT (HDMI_I2CM_CTLINT)	8	R/W	88h	33.5.326/ 1796
12_7E07	I2CM_DIV (HDMI_I2CM_DIV)	8	R/W	0Bh	33.5.327/ 1796
12_7E08	I2CM_SEGADDR (HDMI_I2CM_SEGADDR)	8	R/W	00h	33.5.328/ 1797
12_7E09	I2CM_SOFRSTZ (HDMI_I2CM_SOFRSTZ)	8	R/W	01h	33.5.329/ 1798
12_7E0A	I2CM_SEGPTR (HDMI_I2CM_SEGPTR)	8	R/W	00h	33.5.330/ 1798
12_7E0B	I2CM_SS_SCL_HCNT_1_ADDR (HDMI_I2CM_SS_SCL_HCNT_1_ADDR)	8	R/W	00h	33.5.331/ 1799

Table continues on the next page...

HDMI memory map (continued)

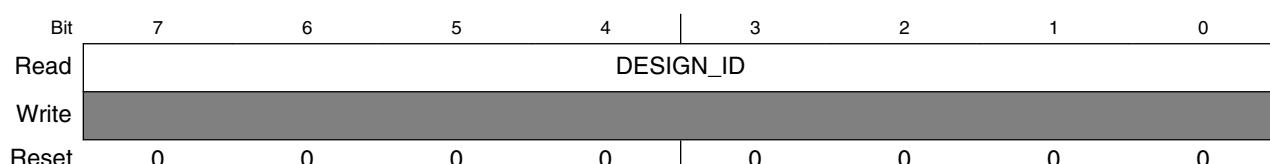
Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
12_7E0C	I2CM_SS_SCL_HCNT_0_ADDR (HDMI_I2CM_SS_SCL_HCNT_0_ADDR)	8	R/W	6Ch	33.5.332/1799
12_7E0D	I2CM_SS_SCL_LCNT_1_ADDR (HDMI_I2CM_SS_SCL_LCNT_1_ADDR)	8	R/W	00h	33.5.333/1800
12_7E0E	I2CM_SS_SCL_LCNT_0_ADDR (HDMI_I2CM_SS_SCL_LCNT_0_ADDR)	8	R/W	7Fh	33.5.334/1800
12_7E0F	I2CM_FS_SCL_HCNT_1_ADDR (HDMI_I2CM_FS_SCL_HCNT_1_ADDR)	8	R/W	00h	33.5.335/1801
12_7E10	I2CM_FS_SCL_HCNT_0_ADDR (HDMI_I2CM_FS_SCL_HCNT_0_ADDR)	8	R/W	11h	33.5.336/1801
12_7E11	I2CM_FS_SCL_LCNT_1_ADDR (HDMI_I2CM_FS_SCL_LCNT_1_ADDR)	8	R/W	00h	33.5.337/1802
12_7E12	I2CM_FS_SCL_LCNT_0_ADDR (HDMI_I2CM_FS_SCL_LCNT_0_ADDR)	8	R/W	24h	33.5.338/1802
12_7F00	BASE_POINTER_ADDR (HDMI_BASE_POINTER_ADDR)	8	R/W	00h	33.5.339/1803

33.5.1 Design Identification Register (HDMI_DESIGN_ID)

The following are the registers used to identify the HDMI TX controller.

- Name: Design Identification Register
- Address Offset: 0x0000
- Size: 8 bits
- Value after Reset: Implementation Dependent
- Access: Read

Address: 12_0000h base + 0h offset = 12_0000h

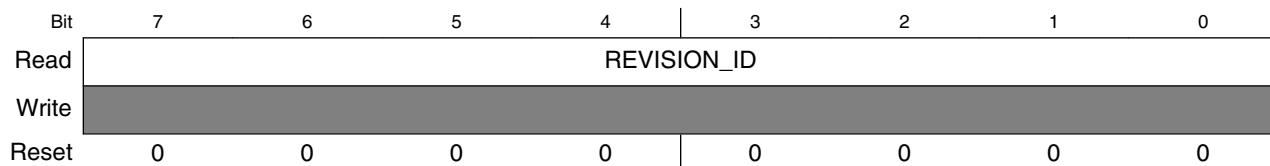
**HDMI_DESIGN_ID field descriptions**

Field	Description
DESIGN_ID	This is a 1 byte design ID code fixed by Freescale that Identifies the main revision of the HDMI TX controller. For example, HDMI TX 1.30a, DESIGN_ID = 11h; REVISION_ID = 0Ah

33.5.2 Revision Identification Register (HDMI_REVISON_ID)

- Name: Revision Identification Register
- Address Offset: 0x0001
- Size: 8 bits
- Value after Reset: Implementation Dependent
- Access: Read

Address: 12_0000h base + 1h offset = 12_0001h



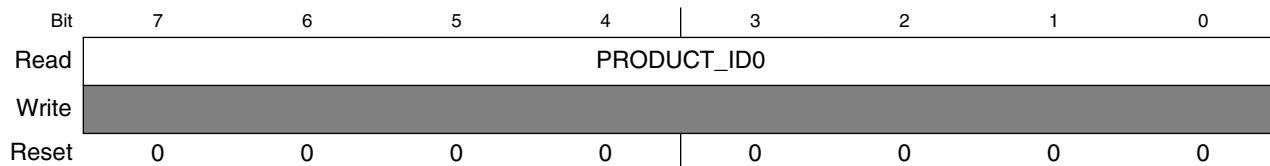
HDMI_REVISON_ID field descriptions

Field	Description
REVISION_ID	This is a one byte revision ID code fixed by Freescale that Identifies the main revision of the HDMI TX controller. For example, HDMI TX 1.30a, DESIGN_ID = 12h; REVISION_ID = 0Ah

33.5.3 Product Identification Register 0 (HDMI_PRODUCT_ID0)

- Name: Product Identification Register 0
- Address Offset: 0x0002
- Size: 8 bits
- Value after Reset: Implementation Dependent
- Access: Read

Address: 12_0000h base + 2h offset = 12_0002h



HDMI_PRODUCT_ID0 field descriptions

Field	Description
PRODUCT_ID0	This one byte fixed code Identifies Freescale's product line ("A0h" for HDMI TX products).

33.5.4 Product Identification Register 1 (HDMI_PRODUCT_ID1)

- Name: Product Identification Register 1
- Address Offset: 0x0003
- Size: 8 bits
- Value after Reset: Implementation Dependent
- Access: Read

Address: 12_0000h base + 3h offset = 12_0003h

Bit	7	6	5	4	3	2	1	0
Read	PRODUCT_ID1							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_PRODUCT_ID1 field descriptions

Field	Description
PRODUCT_ID1	This one byte fixed code identifies Freescale's product line according to: 01h HDMI TX Controller C1h HDMI TX Controller with HDCP encryption engine

33.5.5 Configuration Identification Register 0 (HDMI_CONFIG0_ID)

- Name: Configuration Identification Register 0
- Address Offset: 0x0004
- Size: 8 bits
- Value after Reset: Implementation Dependent
- Access: Read

Address: 12_0000h base + 4h offset = 12_0004h

Bit	7	6	5	4	3	2	1	0
Read	prepen	audhbr	audspdif	audi2s	hdmi14	csc	cec	hdcp
Write								
Reset	0	0	0	0	0	0	0	0

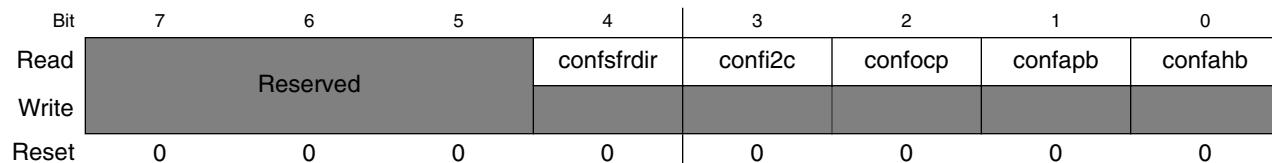
HDMI_CONFIG0_ID field descriptions

Field	Description
7 prepen	Indicates if it is possible to use internal pixel repetition
6 audhbr	Indicates if HBR interface is present
5 audspdif	Indicates if SPDIF interface is present
4 audi2s	Indicates if I2S interface is present
3 hdmi14	Indicates if HDMI 1.4 features are present
2 csc	Indicates if Color Space Conversion block is present
1 cec	Indicates if CEC is present
0 hdcp	Indicates if HDCP is present

33.5.6 Configuration Identification Register 1 (HDMI_CONFIG1_ID)

- Name: Configuration Identification Register 1
- Address Offset: 0x0005
- Size: 8 bits
- Value after Reset: Implementation Dependent
- Access: Read

Address: 12_0000h base + 5h offset = 12_0005h

**HDMI_CONFIG1_ID field descriptions**

Field	Description
7–5 -	This field is reserved.
4 confsfrdir	Indicates that configuration interface is SFR interface
3 confi2c	Indicates that configuration interface is I2C interface

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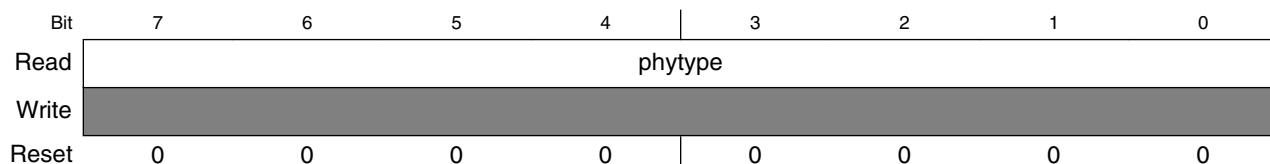
HDMI_CONFIG1_ID field descriptions (continued)

Field	Description
2 confocp	Indicates that configuration interface is OCP interface
1 confapb	Indicates that configuration interface is APB interface
0 confahb	Indicates that configuration interface is AHB interface

33.5.7 Configuration Identification Register 2 (HDMI_CONFIG2_ID)

- Name: Configuration Identification Register 2
- Address Offset: 0x0006
- Size: 8 bits
- Value after Reset: Implementation Dependent
- Access: Read

Address: 12_0000h base + 6h offset = 12_0006h

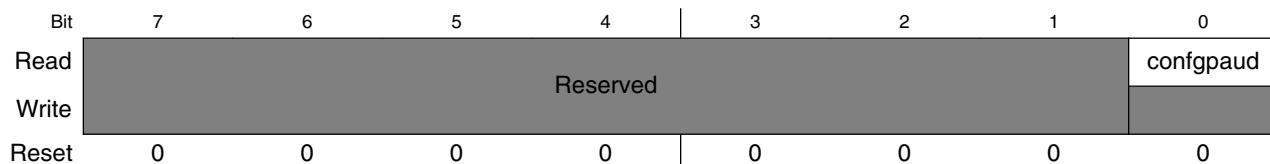
**HDMI_CONFIG2_ID field descriptions**

Field	Description
phytype	Indicates the type of PHY interface selected: 00h Legacy PHY (HDMI TX PHY) F2h PHY_Gen2 (HDMI 3D TX PHY) E2h PHY_Gen2 (HDMI 3D TX PHY) + HEAC PHY

33.5.8 Configuration Identification Register 3 (HDMI_CONFIG3_ID)

- Name: Configuration Identification Register 3
- Address Offset: 0x0007
- Size: 8 bits
- Value after Reset: Implementation Dependent
- Access: Read

Address: 12_0000h base + 7h offset = 12_0007h



HDMI_CONFIG3_ID field descriptions

Field	Description
7–1 -	This field is reserved.
0 cfgpaud	Indicates that configuration interface is Generic Parallel Audio (GPAUD) interface

33.5.9 Frame Composer Interrupt Status Register 0 (HDMI_IH_FC_STAT0)

This section describes clear on write (1 to corresponding bit) status registers, which contain the following active-high, sticky bit interrupts.

HDMI TX introduces a new set of sticky bit mute control registers (IH_MUTE_FC_STAT0 to IH_MUTE_AHBDMAAUD_STAT0) that correspond to the interrupt registers. You can ignore a sticky bit interrupt by setting the corresponding mute control register bit to 1. This puts the global interrupt line on a higher priority than the sticky bit interrupt.

- Address Offset: 0x0100
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Clear on Write

Address: 12_0000h base + 100h offset = 12_0100h

Bit	7	6	5	4	3	2	1	0
Read	AUDI	ACP	HBR	DST	OBA	AUDS	ACR	NULL
Write	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

HDMI_IH_FC_STAT0 field descriptions

Field	Description
7 AUDI	Active after successful transmission of an Audio InfoFrame packet.
6 ACP	Active after successful transmission of an Audio Content Protection packet.
5 HBR	Active after successful transmission of an Audio HBR packet.
4 DST	Reserved
3 OBA	Reserved
2 AUDS	Active after successful transmission of an Audio Sample packet. Due to high number of audio sample packets transmitted, this interrupt is by default masked at frame composer.
1 ACR	Active after successful transmission of an Audio Clock Regeneration (N/CTS transmission) packet.
0 NULL	Active after successful transmission of an Null packet. Due to high number of audio sample packets transmitted, this interrupt is by default masked at frame composer.

33.5.10 Frame Composer Interrupt Status Register 1 (HDMI_IH_FC_STAT1)

- Address Offset: 0x0101
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Clear on Write

Address: 12_0000h base + 101h offset = 12_0101h

Bit	7	6	5	4	3	2	1	0
Read	GMD	ISCR1	ISCR2	VSD	SPD	MPEG	AVI	GCP
Write	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

HDMI_IH_FC_STAT1 field descriptions

Field	Description
7 GMD	Active after successful transmission of an Gamut metadata packet.
6 ISCR1	Active after successful transmission of an International Standard Recording Code 1 packet.
5 ISCR2	Active after successful transmission of an International Standard Recording Code 2 packet.
4 VSD	Active after successful transmission of an Vendor Specific Data infoFrame packet.
3 SPD	Active after successful transmission of an Source Product Descriptor infoFrame packet.
2 MPEG	Reserved
1 AVI	Active after successful transmission of an AVI infoFrame packet.
0 GCP	Active after successful transmission of an General Control Packet.

33.5.11 Frame Composer Interrupt Status Register 2 (HDMI_IH_FC_STAT2)

- Address Offset: 0x0102
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Clear on Write

Address: 12_0000h base + 102h offset = 12_0102h

Bit	7	6	5	4	3	2	1	0
Read	Reserved						LowPriority_overflow	HighPriority_overflow
Write							w1c	w1c
Reset	0	0	0	0	0	0	0	0

HDMI_IH_FC_STAT2 field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 LowPriority_overflow	Frame Composer low priority packet queue descriptor overflow indication.

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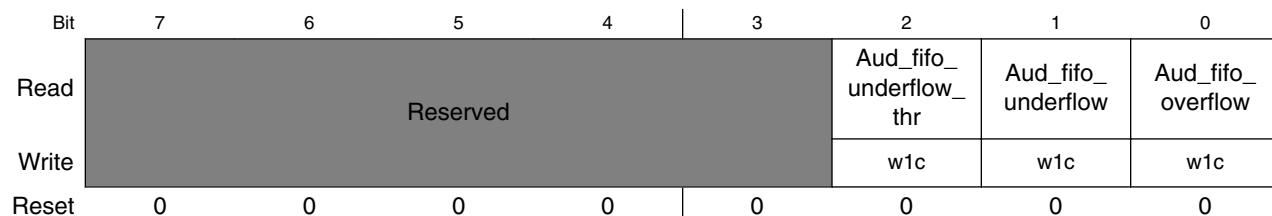
HDMI_IH_FC_STAT2 field descriptions (continued)

Field	Description
0 HighPriority_overflow	Frame Composer high priority packet queue descriptor overflow indication.

33.5.12 Audio Sampler Interrupt Status Register (HDMI_IH_AS_STAT0)

- Address Offset: 0x0103
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Clear on Write

Address: 12_0000h base + 103h offset = 12_0103h

**HDMI_IH_AS_STAT0 field descriptions**

Field	Description
7–3 -	This field is reserved. Reserved
2 Aud_fifo_underflow_thr	Audio Sampler audio FIFO empty threshold (four samples) indication. Only valid in HBR audio.
1 Aud_fifo_underflow	Audio Sampler audio FIFO empty indication.
0 Aud_fifo_overflow	Audio Sampler audio FIFO full indication.

33.5.13 PHY Interface Interrupt Status Register (HDMI_IH_PHY_STAT0)

- Address Offset: 0x0104
- Size: 8 bits
- Value after Reset: 0x00
- Access: Clear on Write/Read

Address: 12_0000h base + 104h offset = 12_0104h

Bit	7	6	5	4
Read	Reserved		RX_SENSE3	RX_SENSE2
Write			w1c	w1c
Reset	0	0	0	0
Bit	3	2	1	0
Read	RX_SENSE1	RX_SENSE0	TX_PHY_LOCK	HDP
Write	w1c	w1c	w1c	w1c
Reset	0	0	0	0

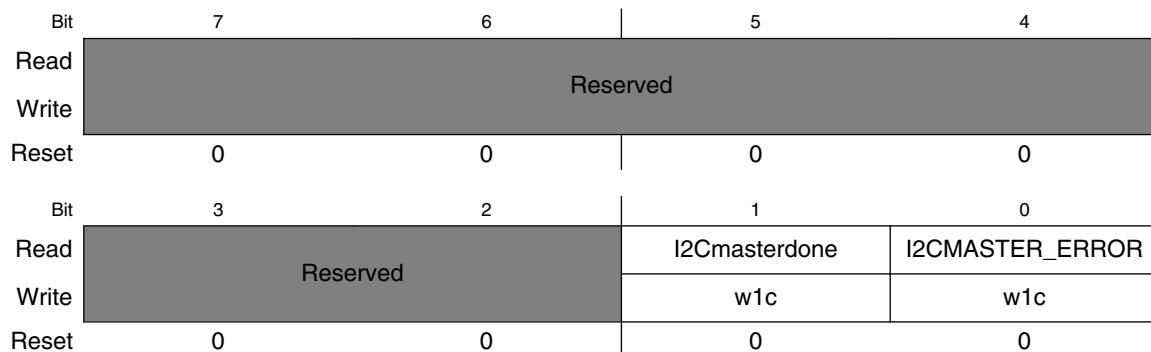
HDMI_IH_PHY_STAT0 field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5 RX_SENSE3	TX PHY RX_SENSE indication for driver 3. You may need to mask or change polarity of this interrupt after it has become active.
4 RX_SENSE2	TX PHY RX_SENSE indication for driver 2. You may need to mask or change polarity of this interrupt after it has become active.
3 RX_SENSE1	TX PHY RX_SENSE indication for driver 1. You may need to mask or change polarity of this interrupt after it has become active.
2 RX_SENSE0	TX PHY RX_SENSE indication for driver 0. You may need to mask or change polarity of this interrupt after it has become active.
1 TX_PHY_LOCK	TX PHY PLL lock indication. Please refer to PHY datasheet for more information. You may need to mask or change polarity of this interrupt after it has become active.
0 HDP	HDMI Hot Plug Detect indication. You may need to mask or change polarity of this interrupt after it has become active.

33.5.14 E-DDC I2C Master Interrupt Status Register (HDMI_IH_I2CM_STAT0)

- Address Offset: 0x0105
- Size: 8 bits
- Value after Reset: 0x00
- Access: Clear on Write/Read

Address: 12_0000h base + 105h offset = 12_0105h



HDMI_IH_I2CM_STAT0 field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 I2Cmasterdone	I2C Master done indication
0 I2CMASTER_ERROR	I2C Master error indication

33.5.15 CEC Interrupt Status Register (HDMI_IH_CEC_STAT0)

- Address Offset: 0x0106
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Clear on Write

Address: 12_0000h base + 106h offset = 12_0106h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	WAKEUP	ERROR_FOLLOW	ERROR_INITIATOR	ARB_LOST	NACK	EOM	DONE
Write		w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

HDMI_IH_CEC_STAT0 field descriptions

Field	Description
7 -	This field is reserved. Reserved
6 WAKEUP	CEC Wake-up indication
5 ERROR_FOLLOW	CEC Error_follow indication
4 ERROR_INITIATOR	CEC Error_follow indication
3 ARB_LOST	CEC Arb_Lost indication
2 NACK	CEC Nack indication
1 EOM	CEC End of Message Indication
0 DONE	CEC Done Indication

33.5.16 Video Packetizer Interrupt Status Register (HDMI_IH_VP_STAT0)

- Address Offset: 0x0107
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Clear on Write

Address: 12_0000h base + 107h offset = 12_0107h

Bit	7	6	5	4
Read	fifofullrepet	fifoemptyrepet	fifofullpp	fifoemptypp
Write	w1c	w1c	w1c	w1c
Reset	0	0	0	0
Bit	3	2	1	0
Read	fifofullremap	fifoemptyremap	fifofullbyp	fifoemptybyp
Write	w1c	w1c	w1c	w1c
Reset	0	0	0	0

HDMI_IH_VP_STAT0 field descriptions

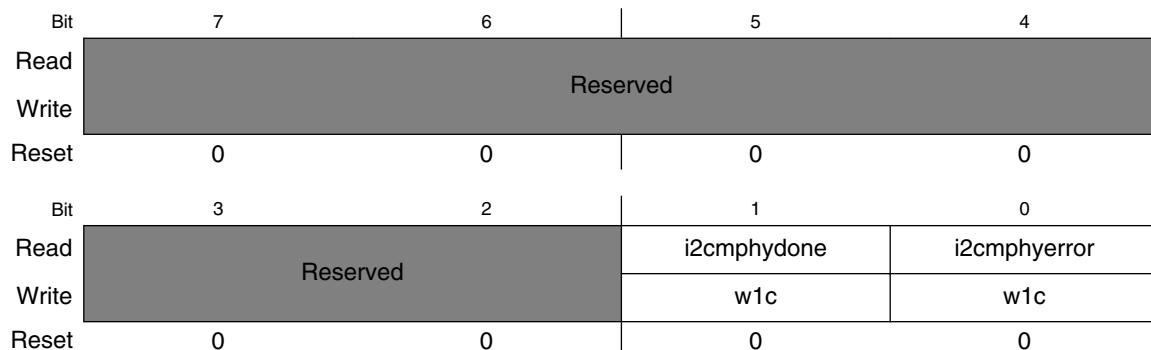
Field	Description
7 fifofullrepet	Video packetizer pixel repeater FIFO full interrupt
6 fifoemptyrepet	Video packetizer pixel repeater FIFO empty interrupt
5 fifofullpp	Video packetizer pixel packing FIFO full interrupt
4 fifoemptypp	Video packetizer pixel packing FIFO empty interrupt
3 fifofullremap	Video packetizer pixel YCC 422 re-mapper FIFO full interrupt
2 fifoemptyremap	Video packetizer pixel YCC 422 re-mapper FIFO empty interrupt
1 fifofullbyp	Video packetizer 8-bit bypass fifo full interrupt
0 fifoemptybyp	Video packetizer 8-bit bypass fifo empty interrupt

33.5.17 PHY GEN2 I2C Master Interrupt Status Register (HDMI_IH_I2CMPHY_STAT0)

This clear on write (1 to corresponding bit) register contains the following active high sticky bit interrupts. That I2C Master PHY is the I2C Master block used to access the PHY I2C Slave.

- Address Offset: 0x0108
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Clear on Write

Address: 12_0000h base + 108h offset = 12_0108h



HDMI_IH_I2CMPHY_STAT0 field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 i2cmphydone	I2C Master PHY done indication
0 i2cmphyerror	I2C Master PHY error indication

33.5.18 AHB Audio DMA Interrupt Status Register (HDMI_IH_AHBDMAAUD_STAT0)

Address Offset: 0x0109

Size: 8 bits

Value after Reset: 0x00

Access: Read/Clear on Write

Address: 12_0000h base + 109h offset = 12_0109h

Bit	7	6	5	4
Read	Reserved		ahbdmaaud_interror	ahbdmaaud_intlostownership
Write			w1c	w1c
Reset	0	0	0	0
Bit	3	2	1	0
Read	ahbdmaaud_intretrysplit	ahbdmaaud_intdone	ahbdmaaud_intbufffull	ahbdmaaud_intbuffempty
Write	w1c	w1c	w1c	w1c
Reset	0	0	0	0

HDMI_IH_AHBDMAAUD_STAT0 field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5 ahbdmaaud_interror	AHB audio DMA error interrupt
4 ahbdmaaud_intlostownership	AHB audio DMA lost ownership interrupt
3 ahbdmaaud_intretrysplit	AHB audio DMA RETRY/SPLIT interrupt
2 ahbdmaaud_intdone	AHB audio DMA done interrupt
1 ahbdmaaud_intbufffull	AHB audio DMA Buffer full interrupt
0 ahbdmaaud_intbuffempty	AHB audio DMA Buffer empty interrupt

33.5.19 Frame Composer Interrupt Mute Control Register 0 (HDMI_IH_MUTE_FC_STAT0)

- Address Offset: 0x0180
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 180h offset = 12_0180h

Bit	7	6	5	4	3	2	1	0
Read	AUDI	ACP	HBR	DST	OBA	AUDS	ACR	NULL
Reset	0	0	0	0	0	0	0	0

HDMI_IH_MUTE_FC_STAT0 field descriptions

Field	Description
7 AUDI	When set to 1, mutes IH_FC_STAT0[7]
6 ACP	When set to 1, mutes IH_FC_STAT0[6]
5 HBR	When set to 1, mutes IH_FC_STAT0[5]
4 DST	When set to 1, mutes IH_FC_STAT0[4]
3 OBA	When set to 1, mutes IH_FC_STAT0[3]
2 AUDS	When set to 1, mutes IH_FC_STAT0[2]
1 ACR	When set to 1, mutes IH_FC_STAT0[1]
0 NULL	When set to 1, mutes IH_FC_STAT0[0]

33.5.20 Frame Composer Interrupt Mute Control Register 1 (HDMI_IH_MUTE_FC_STAT1)

- Address Offset: 0x0181
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 181h offset = 12_0181h

Bit	7	6	5	4	3	2	1	0
Read Write	GMD	ISCR1	ISCR2	VSD	SPD	MPEG	AVI	GCP
Reset	0	0	0	0	0	0	0	0

HDMI_IH_MUTE_FC_STAT1 field descriptions

Field	Description
7 GMD	When set to 1, mutes IH_FC_STAT1[7]
6 ISCR1	When set to 1, mutes IH_FC_STAT1[6]
5 ISCR2	When set to 1, mutes IH_FC_STAT1[5]
4 VSD	When set to 1, mutes IH_FC_STAT1[4]
3 SPD	When set to 1, mutes IH_FC_STAT1[3]
2 MPEG	When set to 1, mutes IH_FC_STAT1[2]
1 AVI	When set to 1, mutes IH_FC_STAT1[1]
0 GCP	When set to 1, mutes IH_FC_STAT1[0]

33.5.21 Frame Composer Interrupt Mute Control Register 2 (HDMI_IH_MUTE_FC_STAT2)

- Address Offset: 0x0182
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 182h offset = 12_0182h

Bit	7	6	5	4	3	2	1	0
Read	Reserved						LowPriority_overflow	HighPriority_overflow
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_IH_MUTE_FC_STAT2 field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 LowPriority_overflow	When set to 1, mutes IH_FC_STAT2[1]
0 HighPriority_overflow	When set to 1, mutes IH_FC_STAT2[0]

33.5.22 Audio Sampler Interrupt Mute Control Register 0 (HDMI_IH_MUTE_AS_STAT0)

- Address Offset: 0x0183
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 183h offset = 12_0183h

Bit	7	6	5	4	3	2	1	0
Read	Reserved						Aud_fifo_underflow_thr	Aud_fifo_underflow
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_IH_MUTE_AS_STAT0 field descriptions

Field	Description
7–3 -	This field is reserved. Reserved
2 Aud_fifo_ underflow_thr	When set to 1, mutes IH_AS_STAT0[2]
1 Aud_fifo_ underflow	When set to 1, mutes IH_AS_STAT0[1]
0 Aud_fifo_ overflow	When set to 1, mutes IH_AS_STAT0[0]

33.5.23 PHY Interface Interrupt Mute Control Register (HDMI_IH_MUTE_PHY_STAT0)

- Address Offset: 0x0184
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 184h offset = 12_0184h

Bit	7	6	5	4	3	2	1	0
Read	Reserved		RX_SENSE3	RX_SENSE2	RX_SENSE1	RX_SENSE0	TX_PHY_LOCK	HDP
Write	0	0	0	0	0	0	0	0

HDMI_IH_MUTE_PHY_STAT0 field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5 RX_SENSE3	When set to 1, mutes IH_PHY_STAT0[5]
4 RX_SENSE2	When set to 1, mutes IH_PHY_STAT0[4]
3 RX_SENSE1	When set to 1, mutes IH_PHY_STAT0[3]
2 RX_SENSE0	When set to 1, mutes IH_PHY_STAT0[2]
1 TX_PHY_LOCK	When set to 1, mutes IH_PHY_STAT0[1]
0 HDP	When set to 1, mutes IH_PHY_STAT0[0]

33.5.24 E-DDC I2C Master Interrupt Mute Control Register (HDMI_IH_MUTE_I2CM_STAT0)

- Address Offset: 0x0185
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 185h offset = 12_0185h

Bit	7	6	5	4
Read Write	Reserved			
Reset	0	0	0	0
Bit	3	2	1	0
Read Write	Reserved		I2Cmasterdone	I2CMASTER_ERROR
Reset	0	0	0	0

HDMI_IH_MUTE_I2CM_STAT0 field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 I2Cmasterdone	When set to 1, mutes IH_I2CM_STAT0[1]
0 I2CMASTER_ERROR	When set to 1, mutes IH_I2CM_STAT0[0]

33.5.25 CEC Interrupt Mute Control Register (HDMI_IH_MUTE_CEC_STAT0)

- Address Offset: 0x0186
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 186h offset = 12_0186h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved	WAKEUP	ERROR_FOLLOW	ERROR_INITIATOR	ARB_LOST	NACK	EOM	DONE
Reset	0	0	0	0	0	0	0	0

HDMI_IH_MUTE_CEC_STAT0 field descriptions

Field	Description
7 -	This field is reserved. Reserved
6 WAKEUP	When set to 1, mutes IH_CEC_STAT0[6]
5 ERROR_FOLLOW	When set to 1, mutes IH_CEC_STAT0[5]
4 ERROR_INITIATOR	When set to 1, mutes IH_CEC_STAT0[4]
3 ARB_LOST	When set to 1, mutes IH_CEC_STAT0[3]
2 NACK	When set to 1, mutes IH_CEC_STAT0[2]
1 EOM	When set to 1, mutes IH_CEC_STAT0[1]
0 DONE	When set to 1, mutes IH_CEC_STAT0[0]

33.5.26 Video Packetizer Interrupt Mute Control Register (HDMI_IH_MUTE_VP_STAT0)

- Address Offset: 0x0187
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 187h offset = 12_0187h

Bit	7	6	5	4
Read Write	fifofullrepet	fifoemptyrepet	fifofullpp	fifoemptypp
Reset	0	0	0	0
Bit	3	2	1	0
Read Write	fifofullremap	fifoemptyremap	fifofullbyp	fifoemptybyp
Reset	0	0	0	0

HDMI_IH_MUTE_VP_STAT0 field descriptions

Field	Description
7 fifofullrepet	When set to 1, mutes IH_VP_STAT0[7]

Table continues on the next page...

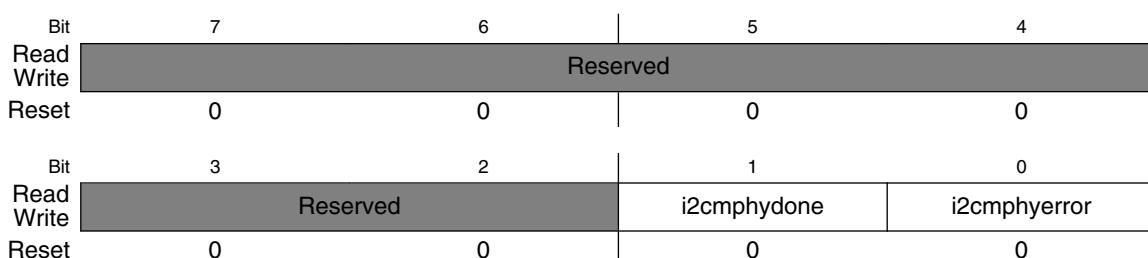
HDMI_IH_MUTE_VP_STAT0 field descriptions (continued)

Field	Description
6 fifoemptyrepel	When set to 1, mutes IH_VP_STAT0[6]
5 fifofullpp	When set to 1, mutes IH_VP_STAT0[5]
4 fifoemptypp	When set to 1, mutes IH_VP_STAT0[4]
3 fifofullremap	When set to 1, mutes IH_VP_STAT0[3]
2 fifoemptyremap	When set to 1, mutes IH_VP_STAT0[2]
1 fifofullbyp	When set to 1, mutes IH_VP_STAT0[1]
0 fifoemptybyp	When set to 1, mutes IH_VP_STAT0[0]

33.5.27 PHY GEN 2 I2C Master Interrupt Mute Control Register (HDMI_IH_MUTE_I2CMPHY_STAT0)

- Address Offset: 0x0188
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 188h offset = 12_0188h

**HDMI_IH_MUTE_I2CMPHY_STAT0 field descriptions**

Field	Description
7–2 -	This field is reserved. Reserved
1 i2cmphydone	When set to 1, mutes IH_I2CMPHY_STAT0[1]
0 i2cmphyerror	When set to 1, mutes IH_I2CMPHY_STAT0[0]

33.5.28 AHB Audio DMA Interrupt Mute Control Register (HDMI_IH_MUTE_AHBDMAAUD_STAT0)

- Address Offset: 0x0189
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 189h offset = 12_0189h

Bit	7	6	5	4
Read	Reserved		ahbdmaaud_interror	ahbdmaaud_intlostownership
Write	0	0	0	0
Bit	3	2	1	0
Read	ahbdmaaud_inttrysplit	ahbdmaaud_intdone	ahbdmaaud_intbufffull	ahbdmaaud_intbuffempty
Write	0	0	0	0

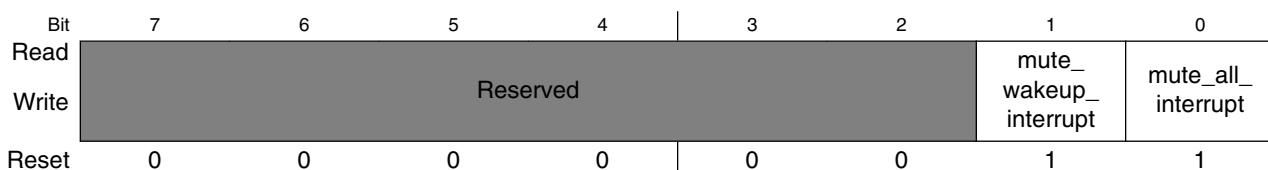
HDMI_IH_MUTE_AHBDMAAUD_STAT0 field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5 ahbdmaaud_interror	When set to 1, mutes IH_AHBDMAAUD_STAT0[5]
4 ahbdmaaud_intlostownership	When set to 1, mutes IH_AHBDMAAUD_STAT0[4]
3 ahbdmaaud_inttrysplit	When set to 1, mutes IH_AHBDMAAUD_STAT0[3]
2 ahbdmaaud_intdone	When set to 1, mutes IH_AHBDMAAUD_STAT0[2]
1 ahbdmaaud_intbufffull	When set to 1, mutes IH_AHBDMAAUD_STAT0[1]
0 ahbdmaaud_intbuffempty	When set to 1, mutes IH_AHBDMAAUD_STAT0[0]

33.5.29 Global Interrupt Mute Control Register (HDMI_IH_MUTE)

- Address Offset: 0x01FF
- Size: 8 bits
- Value after Reset: 0x03
- Access: Read/Write

Address: 12_0000h base + 1FFh offset = 12_01FFh



HDMI_IH_MUTE field descriptions

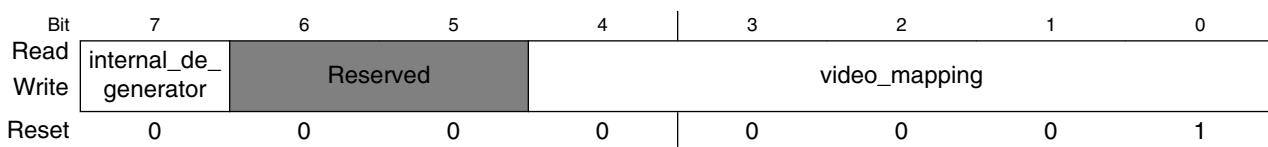
Field	Description
7–2 rsvd	This field is reserved.
1 mute_wakeup_interrupt	When set to 1, mutes the wake-up interrupt line. The sticky bit interrupt continues with its state; only the wake up interrupt line is muted.
0 mute_all_interrupt	When set to 1, mutes the main interrupt line (where all interrupts are ORed). The sticky bit interrupts continue with their state; only the main interrupt line will be muted.

33.5.30 Video Input Mapping and Internal Data Enable Configuration Register (HDMI_TX_INVID0)

This register contains the input video mapping code as defined in Table 2-1.

- Address Offset: 0x0200
- Size: 8 bits
- Value after Reset: 0x01
- Access: Read/Write

Address: 12_0000h base + 200h offset = 12_0200h



HDMI_TX_INVID0 field descriptions

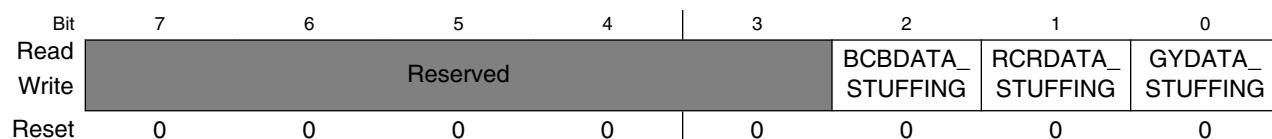
Field	Description
7 internal_de_generator	Internal data enable (DE) generator enable. If data enable is not available for the input video the user may set this bit to one to activate the internal data enable generator. NOTE: This feature only works for input video modes that have native repetition (such as, all CEA videos). No desired pixel repetition can be used with this feature because these configurations only affect the Frame Composer and not this block.
6–5 -	This field is reserved. Reserved
video_mapping	video_mapping

33.5.31 Video Input Stuffing Enable Register (HDMI_TX_INSTUFFING)

This register enables the stuffing mechanism of the Video Sampler module in order to correctly perform Color Space Conversion of the ITU.601 standard YCC video. In this case, when "de" is low, the output video components gydata[15:0], rcrdata[15:0], and bcbdata[15:0] can be configured.

- Address Offset: 0x0201
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 201h offset = 12_0201h

**HDMI_TX_INSTUFFING field descriptions**

Field	Description
7–3 -	This field is reserved. Reserved
2 BCBDATA_STUFFING	BCBDATA stuffing bit 0 When the dataen signal is low, the value in the bcbdata[15:0] output is the one sampled from the corresponding input data. 1 When the dataen signal is low, the value in the bcbdata[15:0] output is given by the values in register TX_BCBDA0 and TX_BCBDA1.
1 RCRDATA_STUFFING	RCRDATA stuffing bit

Table continues on the next page...

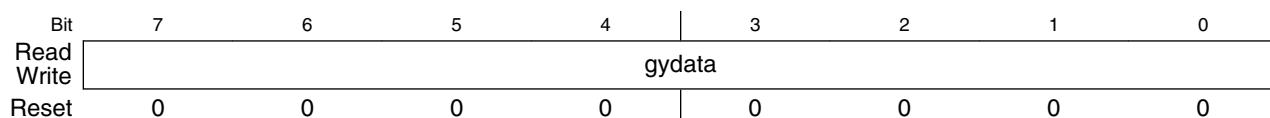
HDMI_TX_INSTUFFING field descriptions (continued)

Field	Description
	<p>0 When the dataen signal is low, the value in the rcrdata[15:0] output is the one sampled from the corresponding input data.</p> <p>1 When the dataen signal is low, the value in the rcrdata[15:0] output is given by the values in TX_RCRDTA0 and TX_RCRDATA1 registers.</p>
0 GYDATA_STUFFING	<p>GYDATA stuffing bit</p> <p>0 when the dataen signal is low, the value in the gydata[15:0] output is the one sampled from the corresponding input data.</p> <p>1 When the dataen signal is low, the value in the gydata[15:0] output is given by the values in TX_GYDTA0 and TX_GYDATA1 registers.</p>

33.5.32 Video Input GY Data Channel Stuffing Register 0 (HDMI_TX_GYDATA0)

- Address Offset: 0x0202
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 202h offset = 12_0202h

**HDMI_TX_GYDATA0 field descriptions**

Field	Description
gydata	gydata[7:0].This register defines the value of gydata[7:0] when TX_INSTUFFING[0] (gydata_stuffing) is set to 1b.

33.5.33 Video Input GY Data Channel Stuffing Register 1 (HDMI_TX_GYDATA1)

- Address Offset: 0x0203
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 203h offset = 12_0203h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	gydata	0	0	0	0
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_TX_GYDATA1 field descriptions

Field	Description
gydata	gydata[15:8]. This register defines the value of gydata[15:8] when TXINSTUFFING[0] (gydata_stuffing) is set to 1b.

33.5.34 Video Input RCR Data Channel Stuffing Register 0 (HDMI_TX_RCRDATA0)

- Address Offset: 0x0204
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 204h offset = 12_0204h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	rcrdata	0	0	0	0
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_TX_RCRDATA0 field descriptions

Field	Description
rcrdata	rcrdata[7:0]. This register defines the value of rcrdata[7:0] when TXINSTUFFING[1] (rcrdata_stuffing) is set to 1b.

33.5.35 Video Input RCR Data Channel Stuffing Register 1 (HDMI_TX_RCRDATA1)

- Address Offset: 0x0205
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 205h offset = 12_0205h

Bit	7	6	5	4		3	2	1	0
Read	rcrdata								Write
Reset	0	0	0	0		0	0	0	0

HDMI_TX_RCRDATA1 field descriptions

Field	Description
rcrdata	rcrdata[15:8]. This register defines the value of rcrydata[15:8] when TX_INSTUFFING[1] (rcrdata_stuffing) is set to 1b.

33.5.36 Video Input RCB Data Channel Stuffing Register 0 (HDMI_TX_BCBDATA0)

- Address Offset: 0x0206
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 206h offset = 12_0206h

Bit	7	6	5	4		3	2	1	0
Read	bcbdata								Write
Reset	0	0	0	0		0	0	0	0

HDMI_TX_BCBDATA0 field descriptions

Field	Description
bcbdata	bcbdata[7:0]. This register defines the value of bcbdata[7:0] when TX_INSTUFFING[2] (bcbdata_stuffing) is set to 1b.

33.5.37 Video Input RCB Data Channel Stuffing Register 1 (HDMI_TX_BCBDATA1)

- Address Offset: 0x0207
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 207h offset = 12_0207h

Bit	7	6	5	4		3	2	1	0
Read					bcbdata				
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_TX_BCBDATA1 field descriptions

Field	Description
bcbdata	bcbdata[15:8]. This register defines the value of bcbdata[15:8] when TX_INSTUFFING[2] (bcbdata_stuffing) is set to 1b.

33.5.38 Video Packetizer Packing Phase Status Register (HDMI_VP_STATUS)

- Address Offset: 0x0800
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 800h offset = 12_0800h

Bit	7	6	5	4		3	2	1	0
Read					packing_phase				
Write	Reserved								
Reset	0	0	0	0		0	0	0	0

HDMI_VP_STATUS field descriptions

Field	Description
7-4 - Reserved	This field is reserved.

Table continues on the next page...

HDMI_VP_STATUS field descriptions (continued)

Field	Description
packing_phase	Read only register that holds the "packing phase" output by the Video packetizer block. For more information about "packing" video data, refer to the HDMI1.4a specification. The register is updated at tmds clock rate.

33.5.39 Video Packetizer Pixel Repetition and Color Depth Register (HDMI_VP_PR_CD)

This register configures the Color Depth of the input video and Pixel repetition to apply to video.

- Address Offset: 0x0801
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 801h offset = 12_0801h

Bit	7	6	5	4	3	2	1	0
Read								
Write								
Reset	0	0	0	0	0	0	0	0

color_depth[3:0]	desired_pr_factor[3:0]
------------------	------------------------

HDMI_VP_PR_CD field descriptions

Field	Description
7–4 color_depth[3:0]	Color depth configuration: other Reserved. Not used. 0000 24 bits per pixel video (8 bit per component). 8-bit packing mode. 0100 24 bits per pixel video (8 bit per component). 8-bit packing mode. 0101 30 bits per pixel video (10 bit per component). 10-bit packing mode. 0110 36 bits per pixel video (12 bit per component). 12-bit packing mode. 0111 48 bits per pixel video (16 bit per component). 16-bit packing mode.
desired_pr_factor[3:0]	Desired pixel repetition factor configuration. The configured value sets H13T PHY PLL to multiply pixel clock by the factor in order to obtain the desired repetition clock. For the CEA modes some are already defined with pixel repetition in the input video. So for CEA modes this shall be always 0. Shall only be used if the user wants to do pixel repetition using H13TCTRL core. other Reserved. Not used. 0000 No pixel repetition (pixel sent only once) 0001 Pixel sent 2 times (pixel repeated once) 0010 Pixel sent 3 times 0011 Pixel sent 4 times 0100 Pixel sent 5 times 0101 Pixel sent 6 times

Table continues on the next page...

HDMI_VP_PR_CD field descriptions (continued)

Field	Description			
	0110	Pixel sent 7 times		
	0111	Pixel sent 8 times		
	1000	Pixel sent 9 times		
	1001	Pixel sent 10 times		

33.5.40 Video Packetizer Stuffing and Default Packing Phase Register (HDMI_VP_STUFF)

This register controls the Pixel repetition, pixel packing and YCC422 stuffing.

- Address Offset: 0x0802
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 802h offset = 12_0802h

Bit	7	6	5	4
Read Write	Reserved		idefault_phase	ifix_pp_to_last
Reset	0	0	0	0
Bit	3	2	1	0
Read Write	icx_goto_p0_st	ycc422_stuffing	pp_stuffing	pr_stuffing
Reset	0	0	0	0

HDMI_VP_STUFF field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5 idefault_phase	Controls the default phase packing machine used according to: "If the transmitted video format has timing such that the phase of the first pixel of every Video Data Period corresponds to pixel packing phase 0 (for example, 10P0, 12P0, 16P0), the Source may set the Default_Phase bit in the GCP. The Sink may use this bit to optimize its filtering or handling of the PP field." (HDMI specification version 1.4a) This means that for 10 bit mode the Htotal must be dividable by 4 and for 12 bit mode the Htotal must be dividable by 2.
4 ifix_pp_to_last	Reserved. Controls packing machine strategy.
3 icx_goto_p0_st	Reserved. Controls packing machine strategy.
2 ycc422_stuffing	YCC 422 remap stuffing control. For horizontal blanking: 0 YCC 422 remap block in direct mode (input blanking data goes directly to output). 1 YCC 422 remap block in stuffing mode. When "de" goes to low the outputs are fixed to 0x00.

Table continues on the next page...

HDMI_VP_STUFF field descriptions (continued)

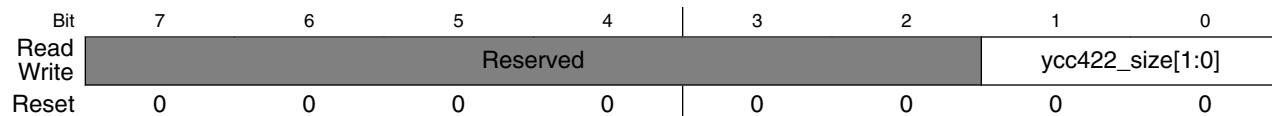
Field	Description
1 pp_stuffing	Pixel packing stuffing control 0 Pixel packing block in direct mode (input blanking data goes directly to output). 1 Pixel packing block in stuffing mode. When "de_rep" goes to low the outputs are fixed to 0x00.
0 pr_stuffing	Pixel repeater stuffing control 0 Pixel repeater block in direct mode (input blanking data goes directly to output). 1 Pixel repeater block in stuffing mode. When "de" goes to low the outputs are fixed to 0x00.

33.5.41 Video Packetizer YCC422 Remapping Register (HDMI_VP_REMAP)

This register controls YCC422 remap of the Video Packetizer. For more information about YCC422 remap refer to HDMI 1.4a specification.

- Address Offset: 0x0803
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 803h offset = 12_0803h

**HDMI_VP_REMAP field descriptions**

Field	Description
7–2 -	This field is reserved. Reserved
ycc422_size[1:0]	YCC 422 remap input video size: 00 YCC 422 16-bit input video (8 bits per component). 01 YCC 422 20-bit input video (10 bits per component). 10 YCC 422 24-bit input video (12 bits per component). 11 Reserved. Not used.

33.5.42 Video Packetizer Output, Bypass, and Enable Configuration Register (HDMI_VP_CONF)

This register controls the Video Packetizer output selection, bypass select, YCC422 enable, Pixel repeater, and pixel packing enabling.

- Address Offset: 0x0804
- Size: 8 bits
- Value after Reset: 0x46
- Access: Read/Write

Address: 12_0000h base + 804h offset = 12_0804h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	bypass_en	pp_en	pr_en	ycc422_en	BYPASS_SELECT	output_selector[1:0]	
Write	0	1	0	0	0	1	1	0

HDMI_VP_CONF field descriptions

Field	Description
7 -	This field is reserved. Reserved
6 bypass_en	Bypass enable. Disabling forces bypass module to output always zeros.
5 pp_en	Pixel packing enable. Disabling forces bypass module to output always zeros.
4 pr_en	Pixel repeater enable. Disabling forces bypass module to output always zeros.
3 ycc422_en	YCC 422 select enable. Disabling forces bypass module to output always zeros.
2 BYPASS_SELECT	Bypass select bit 0 Data from pixel repeater block. 1 Data from input of video packetizer block.
output_selector[1:0]	Video packetizer output selection. 00 Data from pixel packing block. 01 Data from YCC 422 remap block. 10 Data from 8-bit bypass block. 11 Data from 8-bit bypass block.

33.5.43 VP_STAT (HDMI_VP_STAT)

This register contains the following active high FIFO status indications:

HDMI Memory Map/Register Definition

- Address Offset: 0x0805
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 805h offset = 12_0805h

Bit	7	6	5	4
Read	ostfullrepet	ostemptyrepet	ostfullpp	ostemptypp
Write				
Reset	0	0	0	0
Bit	3	2	1	0
Read	ostfullremap	ostemptyremap	ostfullbyp	ostemptybyp
Write				
Reset	0	0	0	0

HDMI_VP_STAT field descriptions

Field	Description
7 ostfullrepet	Video packetizer pixel repeater FIFO full status.
6 ostemptyrepet	Video packetizer pixel repeater FIFO empty status.
5 ostfullpp	Video packetizer pixel packing FIFO full status.
4 ostemptypp	Video packetizer pixel packing FIFO empty status.
3 ostfullremap	Video packetizer pixel YCC 422 re-mapper FIFO full status.
2 ostemptyremap	Video packetizer pixel YCC 422 re-mapper FIFO empty status.
1 ostfullbyp	Video packetizer 8-bit bypass FIFO full status.
0 ostemptybyp	Video packetizer 8-bit bypass FIFO empty status.

33.5.44 VP_INT (HDMI_VP_INT)

This register contains the interrupt indication of the VP_STAT status interrupts. Interrupt generation is accomplished in the following way:

interrupt = (mask == 1'b0) && (polarity == status);

All this interrupts are forwarded to the Interrupt Handler sticky bit registers and after ORed to a single main interrupt line to micro controller. Assertion of this interrupt implies that data related with the corresponding packet has been sent through the HDMI interface.

- Address Offset: 0x0806
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 806h offset = 12_0806h

Bit	7	6	5	4
Read	ointfullrepet	ointemptyrepet	ointfullpp	ointemptypp
Write				
Reset	0	0	0	0
Bit	3	2	1	0
Read	ointfullremap	ointemptyremap	ointfullbyp	ointemptybyp
Write				
Reset	0	0	0	0

HDMI_VP_INT field descriptions

Field	Description
7 ointfullrepet	Video packetizer pixel repeater FIFO full status
6 ointemptyrepet	Video packetizer pixel repeater FIFO empty status
5 ointfullpp	Video packetizer pixel packing FIFO full status
4 ointemptypp	Video packetizer pixel packing FIFO empty status
3 ointfullremap	Video packetizer pixel YCC 422 re-mapper FIFO full status.
2 ointemptyremap	Video packetizer pixel YCC 422 re-mapper FIFO empty status.
1 ointfullbyp	Video packetizer 8-bit bypass FIFO full status.
0 ointemptybyp	Video packetizer 8-bit bypass FIFO empty status.

33.5.45 Video Packetizer Interrupt Mask Register (HDMI_VP_MASK)

Mask register for generation of VP_INT interrupts.

HDMI Memory Map/Register Definition

- Address Offset: 0x0807
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 807h offset = 12_0807h

Bit	7	6	5	4	3	2	1	0
Read Write	VPMASK7	VPMASK6	VPMASK5	VPMASK4	VPMASK3	VPMASK2	VPMASK1	VPMASK0
Reset	0	0	0	0	0	0	0	0

HDMI_VP_MASK field descriptions

Field	Description
7 VPMASK7	Mask bit for VP_INT[7] interrupt bit.
6 VPMASK6	Mask bit for VP_INT[6] interrupt bit.
5 VPMASK5	Mask bit for VP_INT[5] interrupt bit.
4 VPMASK4	Mask bit for VP_INT[4] interrupt bit.
3 VPMASK3	Mask bit for VP_INT[3] interrupt bit.
2 VPMASK2	Mask bit for VP_INT[2] interrupt bit.
1 VPMASK1	Mask bit for VP_INT[1] interrupt bit.
0 VPMASK0	Mask bit for VP_INT[0] interrupt bit.

33.5.46 VP_POL (HDMI_VP_POL)

Polarity register for generation of VP_INT interrupts.

- Address Offset: 0x0808
- Size: 8 bits
- Value after Reset: 0xFF
- Access: Read/Write

Address: 12_0000h base + 808h offset = 12_0808h

Bit	7	6	5	4	3	2	1	0
Read Write	VPPOL7	VPPOL6	VPPOL5	VPPOL4	VPPOL3	VPPOL2	VPPOL1	VPPOL0
Reset	1	1	1	1	1	1	1	1

HDMI_VP_POL field descriptions

Field	Description
7 VPPOL7	Polarity bit for VP_INT[7] interrupt bit.
6 VPPOL6	Polarity bit for VP_INT[6] interrupt bit.
5 VPPOL5	Polarity bit for VP_INT[5] interrupt bit.
4 VPPOL4	Polarity bit for VP_INT[4] interrupt bit.
3 VPPOL3	Polarity bit for VP_INT[3] interrupt bit.
2 VPPOL2	Polarity bit for VP_INT[2] interrupt bit.
1 VPPOL1	Polarity bit for VP_INT[1] interrupt bit.
0 VPPOL0	Polarity bit for VP_INT[0] interrupt bit.

33.5.47 Frame Composer Input Video Configuration and HDCP Keepout Register (HDMI_FC_INVIDCONF)

This register configures the Interlaced/progressive, Vblank variation and polarity of all video synchronism of the input video signal.

- Address Offset: 0x1000
- Size: 8 bits
- Value after Reset: 0x70
- Access: Read/Write

Address: 12_0000h base + 1000h offset = 12_1000h

Bit	7	6	5	4
Read Write	Reserved	vsync_in_polarity	hsync_in_polarity	de_in_polarity
Reset	0	1	1	1
Bit	3	2	1	0
Read Write	DVI_mode	Reserved	r_v_blank_in_osc	in_I_P
Reset	0	0	0	0

HDMI_FC_INVIDCONF field descriptions

Field	Description
7 -	This field is reserved. Reserved

Table continues on the next page...

HDMI_FC_INVIDCONF field descriptions (continued)

Field	Description
6 vsync_in_polarity	Vsync input polarity 1 Active high 0 Active low
5 hsync_in_polarity	Hsync input polarity 1 Active high 0 Active low
4 de_in_polarity	Data enable input polarity 1 Active high 0 Active low
3 DVI_mode	Active low 0 DVI mode selected 1 HDMI mode selected
2 -	This field is reserved. Reserved
1 r_v_blank_in_osc	Used for CEA861-D modes with fractional Vblank (for example, modes 5, 6, 7, 10, 11, 20, 21, and 22. For more modes, refer to CEA861-D specification.) 1 Active high
0 in_I_P	Input video mode: 1 Interlaced 0 Progressive

33.5.48 Frame Composer Input Video HActive Pixels Register 0 (HDMI_FC_INHACTIV0)

- Address Offset: 0x1001
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1001h offset = 12_1001h

Bit	7	6	5	4	3	2	1	0
Read					H_in_activ[7:0]			
Write								

Reset	0	0	0	0	0	0	0	0
-------	---	---	---	---	---	---	---	---

HDMI_FC_INHACTIV0 field descriptions

Field	Description
H_in_activ[7:0]	Input video Horizontal active pixel region width. Number of Horizontal active pixels [0...8191].

33.5.49 Frame Composer Input Video HActive Pixels Register 1 (HDMI_FC_INHACTIV1)

- Address Offset: 0x1002
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1002h offset = 12_1002h

Bit	7	6	5	4		3	2	1	0
Read	Reserved				H_in_activ[12:8]				
Write	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0

HDMI_FC_INHACTIV1 field descriptions

Field	Description
7–5 -	This field is reserved. Reserved
H_in_activ[12:8]	Input video Horizontal active pixel region width. Dependencies: Value after Reset: 0000b <ul style="list-style-type: none"> the higher bit of Horizontal active pixels; Number of Horizontal active pixels [0...8191].

33.5.50 Frame Composer Input Video HBlank Pixels Register 0 (HDMI_FC_INHBLANK0)

- Address Offset: 0x1003
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1003h offset = 12_1003h

Bit	7	6	5	4		3	2	1	0
Read					H_in_blank[7:0]				
Write	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0

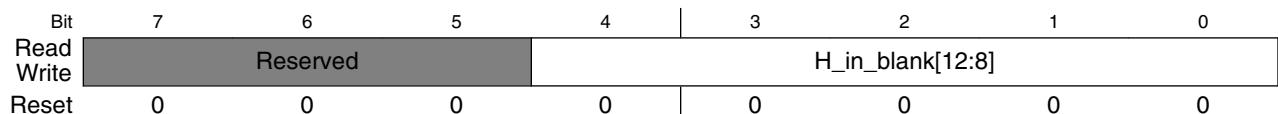
HDMI_FC_INHBLANK0 field descriptions

Field	Description
H_in_blank[7:0]	Input video Horizontal blanking pixel region width. Number of Horizontal blanking pixels [0...4095].

33.5.51 Frame Composer Input Video HBlank Pixels Register 1 (HDMI_FC_INHBLANK1)

- Address Offset: 0x1004
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1004h offset = 12_1004h

**HDMI_FC_INHBLANK1 field descriptions**

Field	Description
7–5 -	This field is reserved. Reserved
H_in_blank[12:8]	Input video Horizontal blanking pixel region width. Dependencies: Value after Reset: 0000b <ul style="list-style-type: none"> the higher bits of Horizontal blanking pixels; Number of Horizontal blanking pixels [0...8191].

33.5.52 Frame Composer Input Video VActive Pixels Register 0 (HDMI_FC_INVACTIV0)

- Address Offset: 0x1005
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1005h offset = 12_1005h

Bit	7	6	5	4	3	2	1	0
Read	V_in_activ[7:0]							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_INVACTIV0 field descriptions

Field	Description
V_in_activ[7:0]	Input video Vertical active pixel region width. Number of Vertical active lines [0...4095].

33.5.53 Frame Composer Input Video VActive Pixels Register 1 (HDMI_FC_INVACTIV1)

- Address Offset: 0x1006
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1006h offset = 12_1006h

Bit	7	6	5	4	3	2	1	0
Read	Reserved			V_in_activ[12:8]				
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_INVACTIV1 field descriptions

Field	Description
7–5 -	This field is reserved. Reserved
V_in_activ[12:8]	Input video Vertical active pixel region width. Dependencies: Value after Reset: 0000b

Table continues on the next page...

HDMI_FC_INVACTIV1 field descriptions (continued)

Field	Description
	<ul style="list-style-type: none"> the higher 5 bits of Vertical active line; Number of Vertical active lines [0...8191].

33.5.54 Frame Composer Input Video VBlank Pixels Register (HDMI_FC_INVBLANK)

- Address Offset: 0x1007
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1007h offset = 12_1007h

Bit	7	6	5	4	3	2	1	0
Read					V_in_blank[7:0]			
Write								

Reset	0	0	0	0	0	0	0	0
-------	---	---	---	---	---	---	---	---

HDMI_FC_INVBLANK field descriptions

Field	Description
V_in_blank[7:0]	Input video Vertical blanking pixel region width. Number of Vertical blanking lines [0...255]. Value after Reset: 0x00

33.5.55 Frame Composer Input Video HSync Front Porch Register 0 (HDMI_FC_HSYNCINDELAY0)

- Address Offset: 0x1008
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1008h offset = 12_1008h

Bit	7	6	5	4	3	2	1	0
Read					H_in_delay[7:0]			
Write								

Reset	0	0	0	0	0	0	0	0
-------	---	---	---	---	---	---	---	---

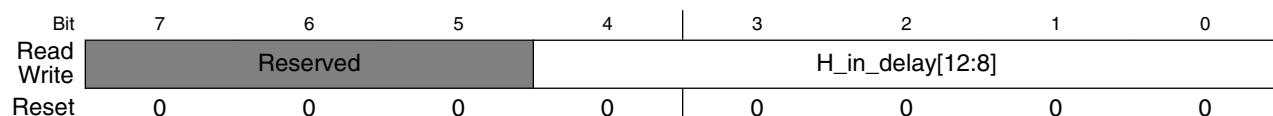
HDMI_FC_HSYNCINDELAY0 field descriptions

Field	Description
H_in_delay[7:0]	Input video Hsync active edge delay. Integer number of pixel clock cycles from "de" non active edge of the last "de" valid period [0...4095].

33.5.56 Frame Composer Input Video HSync Front Porch Register 1 (HDMI_FC_HSYNCINDELAY1)

- Address Offset: 0x1009
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1009h offset = 12_1009h

**HDMI_FC_HSYNCINDELAY1 field descriptions**

Field	Description
7–5 -	This field is reserved. Reserved
H_in_delay[12:8]	Input video Hsync active edge delay. Dependencies: Value after Reset: 0000b <ul style="list-style-type: none"> the higher 5 bits of delay; Integer number of pixel clock cycles from "de" non active edge of the last "de" valid period [0...8191].

33.5.57 Frame Composer Input Video HSync Width Register 0 (HDMI_FC_HSYNCINWIDTH0)

- Address Offset: 0x100A
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 100Ah offset = 12_100Ah

Bit	7	6	5	4		3	2	1	0
Read					H_in_width[7:0]				
Write					0	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_HSYNCINWIDTH0 field descriptions

Field	Description
H_in_width[7:0]	Input video Hsync active pulse width. Integer number of pixel clock cycles [0...511].

33.5.58 Frame Composer Input Video HSync Width Register 1 (HDMI_FC_HSYNCINWIDTH1)

- Address Offset: 0x100B
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 100Bh offset = 12_100Bh

Bit	7	6	5	4		3	2	1	0
Read					Reserved				
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_HSYNCINWIDTH1 field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
H_in_width[9:8]	Input video Hsync active pulse width. Dependencies: Value after Reset after Reset: 0b

Table continues on the next page...

HDMI_FC_HSYNCINWIDTH1 field descriptions (continued)

Field	Description
	<ul style="list-style-type: none"> • Integer number of pixel clock cycles [0...1024].

33.5.59 Frame Composer Input Video VSync Front Porch Register (HDMI_FC_VSYNCINDELAY)

- Address Offset: 0x100C
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 100Ch offset = 12_100Ch

Bit	7	6	5	4	3	2	1	0
Read					V_in_delay[7..0]			
Write	0	0	0	0	0	0	0	0

Reset	0	0	0	0	0	0	0	0
-------	---	---	---	---	---	---	---	---

HDMI_FC_VSYNCINDELAY field descriptions

Field	Description
V_in_delay[7..0]	Input video Vsync active edge delay. Integer number of Hsync pulses from "de" non active edge of the last "de" valid period. [0...255].

33.5.60 Frame Composer Input Video VSync Width Register (HDMI_FC_VSYNCINWIDTH)

- Address Offset: 0x100D
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 100Dh offset = 12_100Dh

Bit	7	6	5	4	3	2	1	0
Read					V_in_width[5..0]			
Write	Reserved	0	0	0	0	0	0	0

Reset	0	0	0	0	0	0	0	0
-------	---	---	---	---	---	---	---	---

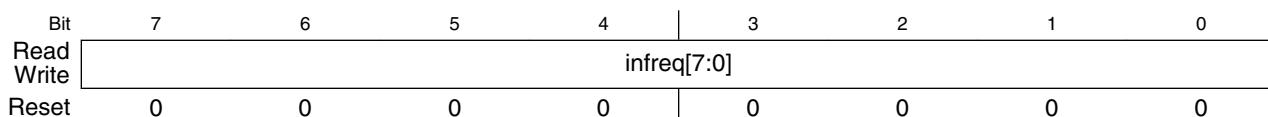
HDMI_FC_VSYNCINWIDTH field descriptions

Field	Description
7–6 - Reserved	This field is reserved.
V_in_width[5..0]	Value after Reset: 000000b Input video Vsync active pulse width: Integer number of pixel clock cycles [0...63].

33.5.61 Frame Composer Input Video Refresh Rate Register 0 (HDMI_FC_INFREQ0)

- Address Offset: 0x100E
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 100Eh offset = 12_100Eh

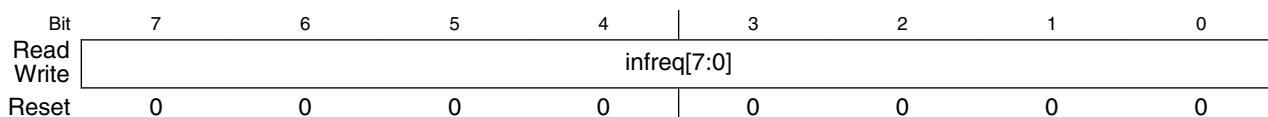
**HDMI_FC_INFREQ0 field descriptions**

Field	Description
infreq[7:0]	Video refresh rate in Hz*1E3 format. This registers are provided for debug and informative purposes. No data is written to this registers by the H13TCTRL and the data here written by software is not used in any way by the H13TCTRL.

33.5.62 Frame Composer Input Video Refresh Rate Register 1 (HDMI_FC_INFREQ1)

- Address Offset: 0x100F
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 100Fh offset = 12_100Fh



HDMI_FC_INFREQ1 field descriptions

Field	Description
infreq[7:0]	Video refresh rate in Hz*1E3 format. This registers are provided for debug and informative purposes. No data is written to this registers by the H13TCTRL and the data here written by software is not used in any way by the H13TCTRL.

33.5.63 Frame Composer Input Video Refresh Rate Register 2 (HDMI_FC_INFREQ2)

- Address Offset: 0x1010
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1010h offset = 12_1010h

Bit	7	6	5	4	3	2	1	0
Read								
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_INFREQ2 field descriptions

Field	Description
7–4 - Reserved	This field is reserved.
infreq[19:16]	Video refresh rate in Hz*1E3 format. This registers are provided for debug and informative purposes. No data is written to this registers by the H13TCTRL and the data here written by software is not used in any way by the H13TCTRL. Value after Reset: 0000b

33.5.64 Frame Composer Control Period Duration Register (HDMI_FC_CTRLDUR)

- Address Offset: 0x1011
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1011h offset = 12_1011h

Bit	7	6	5	4	3	2	1	0
Read	ctrlperiodduration							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_CTRLDUR field descriptions

Field	Description
ctrlperiodduration	Configuration of the control period minimum duration (min. of 12 pixel clock cycles, refer to HDMI 1.4a specification). Integer number of pixel clocks cycles [0..255].

33.5.65 Frame Composer Extended Control Period Duration Register (HDMI_FC_EXCTRLDUR)

- Address Offset: 0x1012
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1012h offset = 12_1012h

Bit	7	6	5	4	3	2	1	0
Read	exctrlperiodduration							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_EXCTRLDUR field descriptions

Field	Description
exctrlperiodduration	Configuration of the extended control period minimum duration (min. of 32 pixel clock cycles, see HDMI 1.4a specification). Integer number of pixel clocks cycles [0..255].

33.5.66 Frame Composer Extended Control Period Maximum Spacing Register (HDMI_FC_EXCTRLSPAC)

- Address Offset: 0x1013
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1013h offset = 12_1013h

Bit	7	6	5	4	3	2	1	0
Read	exctrlperiodspacing							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_EXCTRLSPAC field descriptions

Field	Description
exctrlperiodspacing	Configuration of the maximum spacing between consecutive extended control periods (max of 50msec, see HDMI 1.4a specification): generated spacing = (1/freq tmds clock)*256*256*extctrlperiodspacing

33.5.67 Frame Composer Channel 0 Non-Preamble Data Register (HDMI_FC_CH0PREAM)

- Address Offset: 0x1014
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1014h offset = 12_1014h

Bit	7	6	5	4	3	2	1	0
Read	ch0_preamble_filter							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_CH0PREAM field descriptions

Field	Description
ch0_preamble_filter	When in control mode, configures 8-bits that are going to fill the channel 0 data lines not used to transmit the preamble (for more clarifications refer to HDMI 1.4a specification).

33.5.68 Frame Composer Channel 1 Non-Preamble Data Register (HDMI_FC_CH1PREAM)

- Address Offset: 0x1015
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1015h offset = 12_1015h

Bit	7	6	5	4	3	2	1	0
Read	Reserved				ch1_preamble_filter			
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_CH1PREAM field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
ch1_preamble_filter	When in control mode, configures 6-bits that are going to fill the channel 1 data lines not used to transmit the preamble (for more clarifications refer to HDMI 1.4a specification).

33.5.69 Frame Composer Channel 2 Non-Preamble Data Register (HDMI_FC_CH2PREAM)

- Address Offset: 0x1016
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1016h offset = 12_1016h

Bit	7	6	5	4	3	2	1	0
Read	Reserved				ch2_preamble_filter			
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_CH2PREAM field descriptions

Field	Description
7–6 -	This field is reserved. Reserved

Table continues on the next page...

HDMI_FC_CH2PREAM field descriptions (continued)

Field	Description
ch2_preamble_filter	When in control mode, configures 6-bits that are going to fill the channel 2 data lines not used to transmit the preamble (for more clarifications, see HDMI 1.4a specification).

33.5.70 Frame Composer AVI Configuration Register 3 (HDMI_FC_AVICONF3)

- Address Offset: 0x1017
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

configuration of Quantization range and IT content type.

Address: 12_0000h base + 1017h offset = 12_1017h

Bit	7	6	5	4	3	2	1	0
Read					YQ1_YQ0_YCC		CN1_CN0	
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AVICONF3 field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
3–2 YQ1_YQ0_YCC	Quantization range according to CEA specification.
CN1_CN0	IT content type according to CEA specification

33.5.71 Frame Composer GCP Packet Configuration Register (HDMI_FC_GCP)

Configures the General Control Packet A/V mute indicators and the default phase.

- Address Offset: 0x1018
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

Address: 12_0000h base + 1018h offset = 12_1018h

Bit	7	6	5	4	3	2	1	0
Read						default_phase	set_avmute	clear_avmute
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_GCP field descriptions

Field	Description
7–3 -	This field is reserved. Reserved
2 default_phase	Value of "default_phase" in the GCP packet. This data should be equal to the default phase used at Video packetizer packing machine. Value after Reset: 0b
1 set_avmute	Value of "set_avmute" in the GCP packet. Value after Reset: 0b
0 clear_avmute	Value of "clear_avmute" in the GCP packet. Value after Reset: 0b

33.5.72 Frame Composer AVI Packet Configuration Register 0 (HDMI_FC_AVICONF0)

Configures the following contents of the AVI infoFrame:

- RGB/YCC indication
- Bar information
- Scan information
- Active format present
- Progressive/Interlaced indicator
- Active aspect ratio
- Picture aspect ratio
- Colorimetry
- IT content
- Extended colorimetry
- Quantization range
- Non-uniform picture scaling

For more information, refer to HDMI 1.4a and CEA - 861D specifications.

- Address Offset: 0x1019
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1019h offset = 12_1019h

Bit	7	6	5	4	3	2	1	0
Read	FC_AVICONF0_MISC	FC_AVICONF0_ACTIVE_FORMAT	FC_AVICONF0_SCAN		FC_AVICONF0_BAR		FC_AVICONF0_RGB_YCC	
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AVICONF0 field descriptions

Field	Description
7 FC_AVICONF0_MISC	Frame composer AVI packet configuration bit
6 FC_AVICONF0_ACTIVE_FORMAT	Active format present
5–4 FC_AVICONF0_SCAN	Scan information
3–2 FC_AVICONF0_BAR	Bar information
FC_AVICONF0_RGB_YCC	RGB/YCC indication Value after Reset: 0b

33.5.73 Frame Composer AVI Packet Configuration Register 1 (HDMI_FC_AVICONF1)

- Address Offset: 0x101A
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 101Ah offset = 12_101Ah

Bit	7	6	5	4	3	2	1	0
Read	FC_AVICONF0_COLOR	FC_AVICONF1_PICTURE_AR			FC_AVICONF1_ACTIVE_AR			
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AVICONF1 field descriptions

Field	Description
7–6 FC_AVICONF0_COLOR	Colorimetry
5–4 FC_AVICONF1_PICTURE_AR	Picture aspect ratio
FC_AVICONF1_ACTIVE_AR	Active aspect ratio Value after Reset: 0b

33.5.74 FC_AVICONFFrame Composer AVI Packet Configuration Register 2 (HDMI_FC_AVICONF2)

- Address Offset: 0x101B
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 101Bh offset = 12_101Bh

Bit	7	6	5	4	3	2	1	0
Read	FC_AVICONF2_IT							
Write		FC_AVICONF2_EXT_COLOR			-		FC_AVICONF2_SCALE	
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AVICONF2 field descriptions

Field	Description
7 FC_AVICONF2_IT	IT content
6–4 FC_AVICONF2_EXT_COLOR	Extended colorimetry
3–2 -	Quantization range
FC_AVICONF2_SCALE	Non-uniform picture scaling Value after Reset: 0b

33.5.75 Frame Composer AVI Packet VIC Register (HDMI_FC_AVIVID)

Configures the AVI infoFrame Video Identification code. For more information, refer to the CEA-861-E specification.

- Address Offset: 0x101C
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 101Ch offset = 12_101Ch

Bit	7	6	5	4	3	2	1	0
Read					FC_AVIVID			
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AVIVID field descriptions

Field	Description
FC_AVIVID	the AVI infoFrame Video Identification code.

33.5.76 Frame Composer AVI Packet End of Top Bar Register 0 (HDMI_FC_AVIETB0)

These registers define the AVI infoFrame End of Top Bar value. For more information, refer to CEA-861-E specification.

- Address Offset: 0x101D
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 101Dh offset = 12_101Dh

Bit	7	6	5	4	3	2	1	0
Read				-				
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AVIETB0 field descriptions

Field	Description
-	Line number of end of top bar (lower 8 bits)

33.5.77 Frame Composer AVI Packet End of Top Bar Register 1 (HDMI_FC_AVIETB1)

- Address Offset: 0x101E
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 101Eh offset = 12_101Eh

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_AVIETB1 field descriptions

Field	Description
-	Line number of end of top bar (upper 8 bits)

33.5.78 Frame Composer AVI Packet Start of Bottom Bar Register 0 (HDMI_FC_AVISBB0)

These registers define the AVI infoFrame Start of Bottom Bar value. For more information, refer to CEA-861D specification.

- Address Offset: 0x101F
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 101Fh offset = 12_101Fh

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_AVISBB0 field descriptions

Field	Description
FC_AVISBB0	Line number of Start of Bottom Bar (lower 8 bits)

33.5.79 Frame Composer AVI Packet Start of Bottom Bar Register 1 (HDMI_FC_AVISBB1)

- Address Offset: 0x1020
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1020h offset = 12_1020h

Bit	7	6	5	4	3	2	1	0
Read								
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AVISBB1 field descriptions

Field	Description
FC_AVISBB1	Line number of Start of Bottom Bar (upper 8 bits)

33.5.80 Frame Composer AVI Packet End of Left Bar Register 0 (HDMI_FC_AVIELB0)

These registers define the AVI infoFrame End of Left Bar value. For more information, refer to CEA-861D specification.

- Address Offset: 0x1021
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1021h offset = 12_1021h

Bit	7	6	5	4	3	2	1	0
Read								
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AVIELB0 field descriptions

Field	Description
FC_AVIELB0	Pixel number of end of left Bar (lower 8 bits)

33.5.81 Frame Composer AVI Packet End of Left Bar Register 1 (HDMI_FC_AVIELB1)

- Address Offset: 0x1022
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1022h offset = 12_1022h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0		0	0	0	0
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_AVIELB1 field descriptions

Field	Description
FC_AVIELB1	Pixel number of end of left Bar (lower 8 bits)

33.5.82 Frame Composer AVI Packet Start of Right Bar Register 0 (HDMI_FC_AVISRB0)

These registers define the AVI infoFrame Start of Right Bar value. For more information, refer to CEA-861D specification.

- Address Offset: 0x1023
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1023h offset = 12_1023h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0		0	0	0	0
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_AVISRB0 field descriptions

Field	Description
FC_AVISRB0	Pixel number of start of right Bar (lower 8 bits)

33.5.83 Frame Composer AVI Packet Start of Right Bar Register 1 (HDMI_FC_AVISRB1)

- Address Offset: 0x1024
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1024h offset = 12_1024h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	FC_AVISRB1	0	0	0	0
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_FC_AVISRB1 field descriptions

Field	Description
FC_AVISRB1	Pixel number of start of right Bar (upper 8 bits)

33.5.84 Frame Composer AUD Packet Configuration Register 0 (HDMI_FC_AUDICONF0)

These registers configure the following contents of the AUDIO infoFrame:

- Coding type
- Channel count
- Sampling frequency
- Sampling size
- Channel allocation
- Audio level shift value
- Down mix enable

For more information, refer to CEA-861D specification.

- Address Offset: 0x1025 to 0x1028
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For the FC_AUDICONF0 register, bits [6:5] correspond to LFEPBL1, LFEPBL0 LFE playback level as compared to the other channels (from HDMI 1.4a specification).

HDMI Memory Map/Register Definition

Address: 12_0000h base + 1025h offset = 12_1025h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved		CC[2:0]			CT[3:0]		
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AUDICONF0 field descriptions

Field	Description
7 -	This field is reserved. Reserved
6–4 CC[2:0]	Channel count
CT[3:0]	Coding Type

33.5.85 Frame Composer AUD Packet Configuration Register 1 (HDMI_FC_AUDICONF1)

Address: 12_0000h base + 1026h offset = 12_1026h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved		SS[1:0]	Reserved		SF[2:0]		
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AUDICONF1 field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5–4 SS[1:0]	Sampling size
3 -	This field is reserved. Reserved
SF[2:0]	Sampling frequency

33.5.86 Frame Composer AUD Packet Configuration Register 2 (HDMI_FC_AUDICONF2)

Address: 12_0000h base + 1027h offset = 12_1027h

Bit	7	6	5	4	3	2	1	0
Read Write				CA[7:0]				
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AUDICONF2 field descriptions

Field	Description
CA[7:0]	Channel allocation

33.5.87 Frame Composer AUD Packet Configuration Register 3 (HDMI_FC_AUDICONF3)

Address: 12_0000h base + 1028h offset = 12_1028h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	LFE PBL[1:0]	DM_INH		LSV[3:0]			
Write	0	0	0	0	0	0	0	0

HDMI_FC_AUDICONF3 field descriptions

Field	Description
7 -	This field is reserved. Reserved
6–5 LFE PBL[1:0]	LFE playback information
4 DM_INH	Down mix enable
LSV[3:0]	Level shift value (for down mixing)

33.5.88 Frame Composer VSI Packet Data IEEE Register 0 (HDMI_FC_VSDIEEEID0)

These registers configure the Vendor Specific infoFrame IEEE registration identifier. For more information, refer to CEA-861D specification.

- Address Offset: 0x1029
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1029h offset = 12_1029h

Bit	7	6	5	4	3	2	1	0
Read				-				
Write	0	0	0	0	0	0	0	0

HDMI_FC_VSDIEEEID0 field descriptions

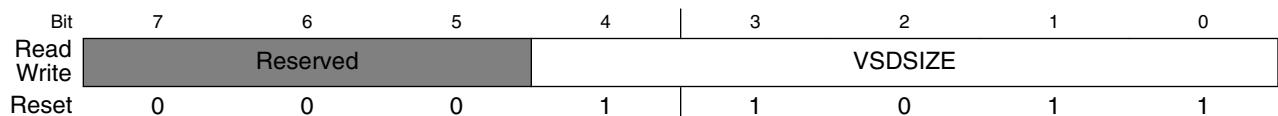
Field	Description
-	the Vendor Specific infoFrame IEEE registration identifier byte 0

33.5.89 Frame Composer VSI Packet Data Size Register (HDMI_FC_VSDSIZE)

- Address Offset: 0x102A
- Size: 8 bits
- Value after Reset: 0x1B
- Access: Read/Write

configuration of Packet size.

Address: 12_0000h base + 102Ah offset = 12_102Ah

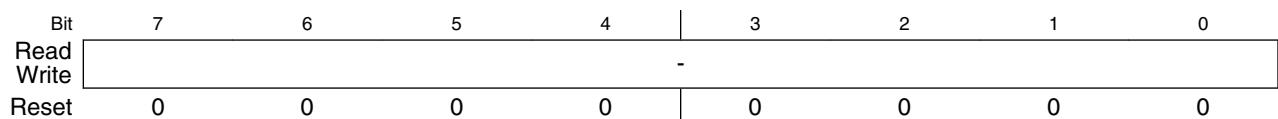
**HDMI_FC_VSDSIZE field descriptions**

Field	Description
7–5 -	This field is reserved. Reserved
VSDSIZE	Packet size as described in HDMI Vendor Specific InfoFrame (from HDMI specification).

33.5.90 Frame Composer VSI Packet Data IEEE Register 1 (HDMI_FC_VSDIEEEID1)

- Address Offset: 0x102a
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1030h offset = 12_1030h



HDMI_FC_VSDIEEEID1 field descriptions

Field	Description
-	the Vendor Specific infoFrame IEEE registration identifier byte 1

**33.5.91 Frame Composer VSI Packet Data IEEE Register 2
(HDMI_FC_VSDIEEEID2)**

- Address Offset: 0x102b
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1031h offset = 12_1031h

Bit	7	6	5	4	-	3	2	1	0
Read					-				
Write	0	0	0	0	-	0	0	0	0

HDMI_FC_VSDIEEEID2 field descriptions

Field	Description
-	the Vendor Specific infoFrame IEEE registration identifier byte 2

**33.5.92 Frame Composer VSI Packet Data IEEE Register 0
(HDMI_FC_VSDPAYLOAD0)**

These registers configure the Vendor Specific infoFrame 24 bytes specific payload. For more information, refer to CEA-861D specification.

- Address Offset: 0x1032
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1032h offset = 12_1032h

Bit	7	6	5	4	-	3	2	1	0
Read					-				
Write	0	0	0	0	-	0	0	0	0

HDMI_FC_VSDPAYLOAD0 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte0

**33.5.93 Frame Composer VSI Packet Data IEEE Register 1
(HDMI_FC_VSDPAYLOAD1)**

- Address Offset: 0x1033
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1033h offset = 12_1033h

Bit	7	6	5	4		3	2	1	0
Read					-				
Write	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD1 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte1

**33.5.94 Frame Composer VSI Packet Data IEEE Register 2
(HDMI_FC_VSDPAYLOAD2)**

- Address Offset: 0x1034
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1034h offset = 12_1034h

Bit	7	6	5	4		3	2	1	0
Read					-				
Write	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD2 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte2

33.5.95 Frame Composer VSI Packet Data IEEE Register 3 (HDMI_FC_VSDPAYLOAD3)

- Address Offset: 0x1035
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1035h offset = 12_1035h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	-	0	0	0	0
Write									
Reset	0	0	0	0	-	0	0	0	0

HDMI_FC_VSDPAYLOAD3 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte3

33.5.96 Frame Composer VSI Packet Data IEEE Register 4 (HDMI_FC_VSDPAYLOAD4)

- Address Offset: 0x1036
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1036h offset = 12_1036h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	-	0	0	0	0
Write									
Reset	0	0	0	0	-	0	0	0	0

HDMI_FC_VSDPAYLOAD4 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte4

33.5.97 Frame Composer VSI Packet Data IEEE Register 5 (HDMI_FC_VSDPAYLOAD5)

- Address Offset: 0x1037
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1037h offset = 12_1037h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD5 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte5

33.5.98 Frame Composer VSI Packet Data IEEE Register 6 (HDMI_FC_VSDPAYLOAD6)

- Address Offset: 0x1038
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1038h offset = 12_1038h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD6 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte6

33.5.99 Frame Composer VSI Packet Data IEEE Register 7 (HDMI_FC_VSDPAYLOAD7)

- Address Offset: 0x1039
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1039h offset = 12_1039h

Bit	7	6	5	4		3	2	1	0
Read					-				
Write					-				
Reset	0	0	0	0	-	0	0	0	0

HDMI_FC_VSDPAYLOAD7 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte7

33.5.100 Frame Composer VSI Packet Data IEEE Register 8 (HDMI_FC_VSDPAYLOAD8)

- Address Offset: 0x103a
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 103Ah offset = 12_103Ah

Bit	7	6	5	4		3	2	1	0
Read					-				
Write					-				
Reset	0	0	0	0	-	0	0	0	0

HDMI_FC_VSDPAYLOAD8 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte8

33.5.101 Frame Composer VSI Packet Data IEEE Register 9 (HDMI_FC_VSDPAYLOAD9)

- Address Offset: 0x103b
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 103Bh offset = 12_103Bh

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	-	0	0	0	0
Write									
Reset	0	0	0	0	-	0	0	0	0

HDMI_FC_VSDPAYLOAD9 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte9

33.5.102 Frame Composer VSI Packet Data IEEE Register 10 (HDMI_FC_VSDPAYLOAD10)

- Address Offset: 0x103c
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 103Ch offset = 12_103Ch

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	-	0	0	0	0
Write									
Reset	0	0	0	0	-	0	0	0	0

HDMI_FC_VSDPAYLOAD10 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte10

33.5.103 Frame Composer VSI Packet Data IEEE Register 11 (HDMI_FC_VSDPAYLOAD11)

- Address Offset: 0x103d
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 103Dh offset = 12_103Dh

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD11 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte11

33.5.104 Frame Composer VSI Packet Data IEEE Register 12 (HDMI_FC_VSDPAYLOAD12)

- Address Offset: 0x103e
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 103Eh offset = 12_103Eh

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD12 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte12

33.5.105 Frame Composer VSI Packet Data IEEE Register 13 (HDMI_FC_VSDPAYLOAD13)

- Address Offset: 0x103f
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 103fh offset = 12_103fh

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD13 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte13

33.5.106 Frame Composer VSI Packet Data IEEE Register 14 (HDMI_FC_VSDPAYLOAD14)

- Address Offset: 0x1040
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1040h offset = 12_1040h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD14 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte14

33.5.107 Frame Composer VSI Packet Data IEEE Register 15 (HDMI_FC_VSDPAYLOAD15)

- Address Offset: 0x1041
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1041h offset = 12_1041h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD15 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte15

33.5.108 Frame Composer VSI Packet Data IEEE Register 16 (HDMI_FC_VSDPAYLOAD16)

- Address Offset: 0x1042
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1042h offset = 12_1042h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD16 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte16

33.5.109 Frame Composer VSI Packet Data IEEE Register 17 (HDMI_FC_VSDPAYLOAD17)

- Address Offset: 0x1043
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1043h offset = 12_1043h

Bit	7	6	5	4		3	2	1	0
Read	[]				-				
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD17 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte17

33.5.110 Frame Composer VSI Packet Data IEEE Register 18 (HDMI_FC_VSDPAYLOAD18)

- Address Offset: 0x1044
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1044h offset = 12_1044h

Bit	7	6	5	4		3	2	1	0
Read	[]				-				
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD18 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte18

33.5.111 Frame Composer VSI Packet Data IEEE Register 19 (HDMI_FC_VSDPAYLOAD19)

- Address Offset: 0x1045
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1045h offset = 12_1045h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD19 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte19

33.5.112 Frame Composer VSI Packet Data IEEE Register 20 (HDMI_FC_VSDPAYLOAD20)

- Address Offset: 0x1046
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1046h offset = 12_1046h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD20 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte20

33.5.113 Frame Composer VSI Packet Data IEEE Register 21 (HDMI_FC_VSDPAYLOAD21)

- Address Offset: 0x1047
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1047h offset = 12_1047h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD21 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte21

33.5.114 Frame Composer VSI Packet Data IEEE Register 22 (HDMI_FC_VSDPAYLOAD22)

- Address Offset: 0x1048
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1048h offset = 12_1048h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD22 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte22

33.5.115 Frame Composer VSI Packet Data IEEE Register 23 (HDMI_FC_VSDPAYLOAD23)

- Address Offset: 0x1049
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1049h offset = 12_1049h

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_VSDPAYLOAD23 field descriptions

Field	Description
-	the Vendor Specific infoFrame 24 bytes specific payload byte23

33.5.116 Frame Composer SPD Packet Data Vendor Name Register 0 (HDMI_FC_SPDVENDORNAME0)

These registers configure the Source Product Descriptor infoFrame 8 bytes Vendor name. For more information, refer to CEA-861D specification.

- Address Offset: 0x104A to 0x1051
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 104Ah offset = 12_104Ah

Bit	7	6	5	4		3	2	1	0
Read	-	-	-	-	-	-	-	-	-
Write	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0		0	0	0	0

HDMI_FC_SPDVENDORNAME0 field descriptions

Field	Description
vendor_name	Vendor name

33.5.117 Frame Composer SPD Packet Data Product Name Register 0 (HDMI_FC_SPDPNAME0)

These registers configure the Source Product Descriptor infoFrame 16 bytes Product name. For more information, refer to CEA-861D specification.

- Address Offset: 0x1052 to 0x1061
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1052h offset = 12_1052h

Bit	7	6	5	4	3	2	1	0
Read					product_name			
Write								

Reset	0	0	0	0	0	0	0	0
-------	---	---	---	---	---	---	---	---

HDMI_FC_SPDPNAME0 field descriptions

Field	Description
product_name	Product name

33.5.118 Frame Composer SPD Packet Data Source Product Descriptor Register (HDMI_FC_SPDDEVICEINF)

This register configures Source Product Descriptor infoFrame description device field. For more information, refer to CEA-861D specification.

- Address Offset: 0x1062
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1062h offset = 12_1062h

Bit	7	6	5	4	3	2	1	0
Read					product_descriptor			
Write								

Reset	0	0	0	0	0	0	0	0
-------	---	---	---	---	---	---	---	---

HDMI_FC_SPDDEVICEINF field descriptions

Field	Description
product_descriptor	Product descriptor

33.5.119 Frame Composer Audio Sample Flat and Layout Configuration Register (HDMI_FC_AUDSCONF)

Configures the Audio sample packet sample flat and layout configuration. For more information, refer to HDMI 1.4a specification.

- Address Offset: 0x1063
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1063h offset = 12_1063h



HDMI_FC_AUDSCONF field descriptions

Field	Description
7–4 aud_packet_sampfit[3:0]	Set the audio packet sample flat value to be sent on the packet.
3–1 -	This field is reserved. Reserved
0 aud_packet_layout	Set the audio packet layout to be sent in the packet: 1 layout 1 0 layout 0

33.5.120 Frame Composer Audio Packet Sample Present Status Register (HDMI_FC_AUDSSTAT)

Shows the data sample present indication of the last Audio sample packet sent by the HDMI TX Controller. For more information, refer to HDMI 1.4a specification.

- Address Offset: 0x1064
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

HDMI Memory Map/Register Definition

Address: 12_0000h base + 1064h offset = 12_1064h

Bit	7	6	5	4	3	2	1	0
Read							packet_sampprs[3:0]	
Write			Reserved					
Reset	0	0	0	0	0	0	0	0

HDMI_FC_AUDSSTAT field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
packet_sampprs[3:0]	Shows the data sample present indication of the last Audio sample packet sent by the HDMI TX Controller. This register information is at tmds clock rate.

33.5.121 Frame Composer Number of High Priority Packets Attended Configuration Register (HDMI_FC_CTRLQHIGH)

- Address Offset: 0x1073
- Size: 8 bits
- Value after Reset: 0x0F
- Access: Read/Write

Address: 12_0000h base + 1073h offset = 12_1073h

Bit	7	6	5	4	3	2	1	0
Read			Reserved			onhighattended[4:0]		
Write								
Reset	0	0	0	0	1	1	1	1

HDMI_FC_CTRLQHIGH field descriptions

Field	Description
7–5 -	This field is reserved. Reserved
onhighattended[4:0]	Configures the number of high priority packets or audio sample packets consecutively attended before checking low priority queue status. Integer number [0..31]

33.5.122 Frame Composer Number of Low Priority Packets Attended Configuration Register (HDMI_FC_CTRLQLOW)

- Address Offset: 0x1074
- Size: 8 bits
- Value after Reset: 0x03
- Access: Read/Write

Address: 12_0000h base + 1074h offset = 12_1074h

Bit	7	6	5	4		3	2	1	0
Read Write	Reserved				onlowattended[4:0]				
Reset	0	0	0	0		0	0	1	1

HDMI_FC_CTRLQLOW field descriptions

Field	Description
7–5 -	This field is reserved. Reserved
onlowattended[4:0]	Configures the number of low priority packets or null packets consecutively attended before checking high priority queue status or audio sample availability. Integer number [0..31]

33.5.123 Frame Composer ACP Packet Type Configuration Register 0 (HDMI_FC_ACP0)

Configures the following contents of the ACP packet. For more information, refer to the HDMI 1.4 specification.

- Address Offset: 0x1075
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1075h offset = 12_1075h

Bit	7	6	5	4		3	2	1	0
Read Write	acctype[7:0]								
Reset	0	0	0	0		0	0	0	0

HDMI_FC_ACP0 field descriptions

Field	Description
acptype[7:0]	Configures the ACP packet type.

33.5.124 Frame Composer ACP Packet Type Configuration Register 1 (HDMI_FC_ACP1)

Configures the following contents of the Audio Content Packet (ACP) body:

- Address Offset: 0x1091 to 0x1082
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1091h offset = 12_1091h

Bit	7	6	5	4	3	2	1	0
Read Write	Audio_contentpacket							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_ACP1 field descriptions

Field	Description
Audio_contentpacket	Audio content packet

33.5.125 FC_ISCR1_Frame Composer Packet Status, Valid, and Continue Configuration Register (HDMI_FC_ISCR1_0)

Configures the following contents of the ISRC1 packet:

- Address Offset: 0x1092
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, see the HDMI 1.4 specification.

Address: 12_0000h base + 1092h offset = 12_1092h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_ISCR1_0 field descriptions

Field	Description
7–5 -	This field is reserved. Reserved
4–2 isrc_status[2:0]	Status of ISRC1.
1 isrc_valid	Valid of ISRC1.
0 isrc_cont	Indication of ISRC2.

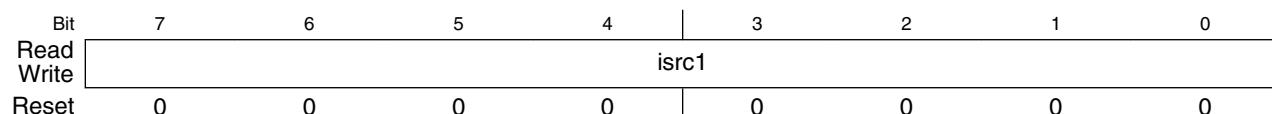
33.5.126 Frame Composer ISCR1 Packet Body Register 1 (HDMI_FC_ISCR1_1)

Configures the following contents of the ISRC1 packet:

- ISRC1 packet body
- Address Offset: 0x10A2 to 0x1093
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, see the HDMI 1.4 specification.

Address: 12_0000h base + 1093h offset = 12_1093h

**HDMI_FC_ISCR1_1 field descriptions**

Field	Description
isrc1	Configures the contents of the ISRC1 packet:

33.5.127 Frame Composer ISCR2 Packet Body Register 0 (HDMI_FC_ISCR2_0)

Configures the following contents of the ISRC2 packet:

- ISRC2 packet body
- Address Offset: 0x10B2 to 0x10A3
- Size: 8 bits

HDMI Memory Map/Register Definition

- Value after Reset: 0x00
- Access: Read/Write

For more information, see the HDMI 1.4 specification.

Address: 12_0000h base + 10A3h offset = 12_10A3h

Bit	7	6	5	4	3	2	1	0
Read Write					isrc2			
Reset	0	0	0	0	0	0	0	0

HDMI_FC_ISCR2_0 field descriptions

Field	Description
isrc2	Configures the contents of the ISRC1 packet:

33.5.128 Frame Composer Data Island Auto Packet Scheduling Register 0 (HDMI_FC_DATAUTO0)

Configures the Frame Composer RDRB(1)/Manual(0) data island packet insertion for SPD, VSD, ISRC2, ISRC1 and ACP packets. On RDRB mode the described packet scheduling is controlled by registers FC_DATAUTO1 and FC_DATAUTO2, while in Manual mode register FC_DATMAN requests to FC the insertion of the requested packet.

- Address Offset: 0x10B3
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10B3h offset = 12_10B3h

Bit	7	6	5	4	3	2	1	0
Read Write		Reserved		spd_auto	vsd_auto	isrc2_auto	isrc1_auto	acp_auto
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DATAUTO0 field descriptions

Field	Description
7–5 -	This field is reserved. Reserved
4 spd_auto	Enables SPD automatic packet scheduling
3 vsd_auto	Enables VSD automatic packet scheduling

Table continues on the next page...

HDMI_FC_DATAUTO0 field descriptions (continued)

Field	Description
2 iscr2_auto	Enables ISRC2 automatic packet scheduling
1 iscr1_auto	Enables ISRC1 automatic packet scheduling
0 acp_auto	Enables ACP automatic packet scheduling

33.5.129 Frame Composer Data Island Auto Packet Scheduling Register 1 (HDMI_FC_DATAUTO1)

Configures the Frame Composer (FC) RDRB frame interpolation for SPD, VSD, ISRC2, ISRC1 and ACP packet insertion on data island when FC is on RDRB mode for the listed packets.

- Address Offset: 0x10B4
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10B4h offset = 12_10B4h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				AUTO_FRAME_INTERPOLATION			
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DATAUTO1 field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
AUTO_FRAME_INTERPOLATION	Packet frame interpolation, for automatic packet scheduling

33.5.130 Frame Composer Data Island Auto Packet Scheduling Register 2 (HDMI_FC_DATAUTO2)

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for SPD, VSD, ISRC2, ISRC1 and ACP packet insertion on data island when FC is on RDRB mode for the listed packets.

- Address Offset: 0x10B5

HDMI Memory Map/Register Definition

- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10B5h offset = 12_10B5h

Bit	7	6	5	4	3	2	1	0
Read	AUTO_FRAME_PACKETS				AUTO_LINE_SPACING			
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DATAUTO2 field descriptions

Field	Description
7–4 AUTO_FRAME_PACKETS	Packets per frame, for automatic packet scheduling
AUTO_LINE_SPACING	Packets line spacing, for automatic packet scheduling

33.5.131 Frame Composer Data Island Manual Packet Request Register (HDMI_FC_DATMAN)

Requests to the Frame Composer the data island packet insertion for NULL, SPD, VSD, ISRC2, ISRC1 and ACP packets when FC_DATAUTO0 bit is in manual mode for the packet requested.

- Address Offset: 0x10B6
- Size: 8 bits
- Value after Reset: 0x00
- Access: Write

Address: 12_0000h base + 10B6h offset = 12_10B6h

Bit	7	6	5	4	3	2	1	0
Read	Reserved							
Write	null_tx		spd_tx	vsd_tx	isrc2_tx	isrc1_tx	acp_tx	
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DATMAN field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5 null_tx	Null packet

Table continues on the next page...

HDMI_FC_DATMAN field descriptions (continued)

Field	Description
4 spd_tx	SPD packet
3 vsd_tx	VSD packet
2 isrc2_tx	ISRC2 packet
1 isrc1_tx	ISRC1 packet
0 acp_tx	ACP packet

33.5.132 Frame Composer Data Island Auto Packet Scheduling Register 3 (HDMI_FC_DATAUTO3)

Configures the Frame Composer Automatic(1)/RDRB(0) data island packet insertion for AVI, GCP, AUDI and ACR packets. In Automatic mode, the packet will be inserted on Vblanking when first line with active Vsync appears.

- Address Offset: 0x10B7
- Size: 8 bits
- Value after Reset: 0x0F
- Access: Read/Write

Address: 12_0000h base + 10B7h offset = 12_10B7h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				avi_auto	gcp_auto	audi_auto	acr_auto
Reset	0	0	0	0	1	1	1	1

HDMI_FC_DATAUTO3 field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
3 avi_auto	Enable AVI packet insertion
2 gcp_auto	Enable GCP packet insertion
1 audi_auto	Enable AUDI packet insertion
0 acr_auto	Enable ACR packet insertion

33.5.133 Frame Composer Round Robin ACR Packet Insertion Register 0 (HDMI_FC_RDRB0)

Configures the Frame Composer (FC) RDRB frame interpolation for ACR packet insertion on data island when FC is on RDRB mode for this packet.

- Address Offset: 0x10B8
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10B8h offset = 12_10B8h

Bit	7	6	5	4	3	2	1	0
Read	Reserved				ACRframeinterpolation			
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_RDRB0 field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
ACRframeinterpolation	ACR frame interpolation

33.5.134 Frame Composer Round Robin ACR Packet Insertion Register 1 (HDMI_FC_RDRB1)

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the ACR packet insertion on data island when FC is on RDRB mode this packet.

- Address Offset: 0x10B9
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10B9h offset = 12_10B9h

Bit	7	6	5	4	3	2	1	0
Read	ACRpacketsinframe				ACRpacketlinespacing			
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_RDRB1 field descriptions

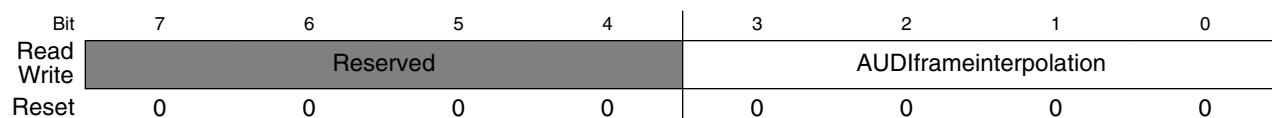
Field	Description
7–4 ACRpacketsinframe	ACR packets in frame
ACRpacketlinespacing	ACR packet line spacing

33.5.135 Frame Composer Round Robin ACR Packet Insertion Register 2 (HDMI_FC_RDRB2)

Configures the Frame Composer (FC) RDRB frame interpolation for AUDI packet insertion on data island when FC is on RDRB mode for this packet.

- Address Offset: 0x10BA
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10BAh offset = 12_10BAh

**HDMI_FC_RDRB2 field descriptions**

Field	Description
7–4 -	This field is reserved. Reserved
AUDIframeinterpolation	Audio frame interpolation

33.5.136 Frame Composer Round Robin ACR Packet Insertion Register 3 (HDMI_FC_RDRB3)

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the AUDI packet insertion on data island when FC is on RDRB mode this packet.

- Address Offset: 0x10BB
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

Address: 12_0000h base + 10BBh offset = 12_10BBh

Bit	7	6	5	4	3	2	1	0
Read	AUDIpacketsinframe				AUDIpacketlinespacing			
Write	0	0	0	0	0	0	0	0

HDMI_FC_RDRB3 field descriptions

Field	Description
7–4 AUDIpacketsinframe	Audio packets per frame
AUDIpacketlinespacing	Audio packets line spacing

33.5.137 Frame Composer Round Robin ACR Packet Insertion Register 4 (HDMI_FC_RDRB4)

Configures the Frame Composer (FC) RDRB frame interpolation for GCP packet insertion on data island when FC is on RDRB mode for this packet.

- Address Offset: 0x10BC
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10BCh offset = 12_10BCh

Bit	7	6	5	4	3	2	1	0
Read	Reserved				GCPframeinterpolation			
Write	0	0	0	0	0	0	0	0

HDMI_FC_RDRB4 field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
GCPframeinterpolation	GCP packets line spacing

33.5.138 Frame Composer Round Robin ACR Packet Insertion Register 5 (HDMI_FC_RDRB5)

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the GCP packet insertion on data island when FC is on RDRB mode this packet.

- Address Offset: 0x10BD

- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10BDh offset = 12_10BDh

Bit	7	6	5	4	3	2	1	0
Read Write	GCPacketsinframe				GCPacketlinespacing			
Reset	0	0	0	0	0	0	0	0

HDMI_FC_RDRB5 field descriptions

Field	Description
7–4 GCPacketsinframe	GCP packets per frame
GCPacketlinespacing	GCP packets line spacing

33.5.139 Frame Composer Round Robin ACR Packet Insertion Register 6 (HDMI_FC_RDRB6)

Configures the Frame Composer (FC) RDRB frame interpolation for AVI packet insertion on data island when FC is on RDRB mode for this packet.

- Address Offset: 0x10BE
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10BEh offset = 12_10BEh

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				AVIframeinterpolation			
Reset	0	0	0	0	0	0	0	0

HDMI_FC_RDRB6 field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
AVIframeinterpolation	GCP packets line spacing

33.5.140 Frame Composer Round Robin ACR Packet Insertion Register 7 (HDMI_FC_RDRB7)

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the AVI packet insertion on data island when FC is on RDRB mode this packet.

- Address Offset: 0x10BF
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10BFh offset = 12_10BFh

Bit	7	6	5	4	3	2	1	0
Read	AVIpacketsinframe				AVIpacketlinespacing			
Reset	0	0	0	0	0	0	0	0

HDMI_FC_RDRB7 field descriptions

Field	Description
7–4 AVIpacketsinframe	AVI packets per frame
AVIpacketlinespacing	AVI packets line spacing

33.5.141 FC_STAT0 (HDMI_FC_STAT0)

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the AVI packet insertion on data island when FC is on RDRB mode this packet.

- Address Offset: 0x10D0
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 10D0h offset = 12_10D0h

Bit	7	6	5	4	3	2	1	0
Read	AUDI	ACP	HBR	Reserved		AUDS	ACR	NULL
Write				0	0	0	0	0

HDMI_FC_STAT0 field descriptions

Field	Description
7 AUDI	Status bit Active after successful transmission of an Audio InfoFrame packet.
6 ACP	Status bit. Active after successful transmission of an Audio Content Protection Packet.
5 HBR	Status bit. Active after successful transmission of an Audio HBR packet
4–3 -	This field is reserved. Reserved
2 AUDS	Status bit Active after successful transmission of an Audio Sample packet.
1 ACR	Status bit Active after successful transmission of an Audio Clock Regeneration (N/CTS transmission) packet.
0 NULL	Status bit Active after successful transmission of an Null packet.

33.5.142 FC_INT0 (HDMI_FC_INT0)

This register contains the interrupt indication of the FC_STAT0 status interrupts. Interrupt generation is accomplished in the following way:

interrupt = (mask == 1'b0) && (polarity == status);

All this interrupts are forwarded to the Interrupt Handler sticky bit registers and after ORed to a single main interrupt line to micro controller. Assertion of this interrupt implies that data related with the corresponding packet has been sent through the HDMI interface.

- Address Offset: 0x10D1
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10D1h offset = 12_10D1h

Bit	7	6	5	4	3	2	1	0
Read Write	AUDI	ACP	HBR	Reserved		AUDS	ACR	NULL
Reset	0	0	0	0	0	0	0	0

HDMI_FC_INT0 field descriptions

Field	Description
7 AUDI	Interrupt indication bit

Table continues on the next page...

HDMI_FC_INT0 field descriptions (continued)

Field	Description
	Active after successful transmission of an Audio InfoFrame packet interrupt.
6 ACP	Interrupt indication bit Active after successful transmission of an Audio Content Protection packet interrupt.
5 HBR	Interrupt indication bit Active after successful transmission of a Audio HBR packet interrupt.
4–3 -	This field is reserved. Reserved
2 AUDS	Interrupt indication bit Active after successful transmission of an Audio Sample packet interrupt.
1 ACR	Interrupt indication bit Active after successful transmission of an Audio Clock Regeneration (N/CTS transmission) packet interrupt.
0 NULL	Interrupt indication bit Active after successful transmission of an Null packet interrupt.

33.5.143 Frame Composer Packet Interrupt Mask Register 0 (HDMI_FC_MASK0)

Mask register for generation of FC_INT0 interrupts.

- Address Offset: 0x10D2
- Size: 8 bits
- Value after Reset: 0x25
- Access: Read/Write

Address: 12_0000h base + 10D2h offset = 12_10D2h

Bit	7	6	5	4	3	2	1	0
Read Write	AUDI	ACP	HBR	Reserved	AUDS	ACR	NUL	
Reset	0	0	1	0	0	1	0	1

HDMI_FC_MASK0 field descriptions

Field	Description
7 AUDI	Mask bit for FC_INT0.AUDI interrupt bit Value after Reset: 0b
6 ACP	Mask bit for FC_INT0.ACPI interrupt bit Value after Reset: 0b
5 HBR	Mask bit for FC_INT0.HBR interrupt bit Value after Reset: 0b

Table continues on the next page...

HDMI_FC_MASK0 field descriptions (continued)

Field	Description
4–3 -	This field is reserved. Reserved
2 AUDS	Mask bit for FC_INT0.AUDS interrupt bit Value after Reset: 0b
1 ACR	Mask bit for FC_INT0.ACR interrupt bit Value after Reset: 0b
0 NULL	Mask bit for FC_INT0.NULL interrupt bit Value after Reset: 0b

33.5.144 FC_POL0 (HDMI_FC_POL0)

Polarity register for generation of FC_INT0 interrupts.

- Address Offset: 0x10D3
- Size: 8 bits
- Value after Reset: 0xFF
- Access: Read/Write

Address: 12_0000h base + 10D3h offset = 12_10D3h

Bit	7	6	5	4	3	2	1	0
Read	AUDI	ACP	HBR	Reserved		AUDS	ACR	NULL
Write	1	1	1	1	1	1	1	1

HDMI_FC_POL0 field descriptions

Field	Description
7 AUDI	Polarity bit for FC_INT0.AUDI interrupt bit Value after Reset: 0b
6 ACP	Polarity bit for FC_INT0.ACPI interrupt bit Value after Reset: 0b
5 HBR	Polarity bit for FC_INT0.HBR interrupt bit Value after Reset: 0b
4–3 -	This field is reserved. Reserved
2 AUDS	Polarity bit for FC_INT0.AUDS interrupt bit Value after Reset: 0b
1 ACR	Polarity bit for FC_INT0.ACR interrupt bit Value after Reset: 0b
0 NULL	Polarity bit for FC_INT0.NULL interrupt bit Value after Reset: 0b

33.5.145 FC_STAT1 (HDMI_FC_STAT1)

This register contains the following active high packet sent status indications:

- Address Offset: 0x10D4
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10D4h offset = 12_10D4h

Bit	7	6	5	4	3	2	1	0
Read Write	GMD	ISCR1	ISCR2	VSD	SPD	Reserved	AVI	GCP
Reset	0	0	0	0	0	0	0	0

HDMI_FC_STAT1 field descriptions

Field	Description
7 GMD	Status bit Active after successful transmission of an Gamut metadata packet.
6 ISCR1	Status bit Active after successful transmission of an International Standard Recording Code 1 packet.
5 ISCR2	Active after successful transmission of an International Standard Recording Code 2 packet.
4 VSD	Active after successful transmission of an Vendor Specific Data infoFrame packet.
3 SPD	Active after successful transmission of an Source Product Descriptor infoFrame packet.
2 -	This field is reserved. Reserved
1 AVI	Status bit Active after successful transmission of an AVI infoFrame packet.
0 GCP	Status bit Active after successful transmission of an General Content Packet.

33.5.146 FC_INT1 (HDMI_FC_INT1)

This register contains the interrupt indication of the FC_STAT1 status interrupts. Interrupt generation is accomplished in the following way:

interrupt = (mask == 1'b0) && (polarity == status);

All this interrupts are forwarded to the Interrupt Handler sticky bit registers and after ORed to a single main interrupt line to micro controller. Assertion of this interrupt implies that data related with the corresponding packet has been sent through the HDMI interface.

- Address Offset: 0x10D5
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10D5h offset = 12_10D5h

Bit	7	6	5	4	3	2	1	0
Read Write	GMD	ISCR1	ISCR2	VSD	SPD	Reserved	AVI	GCP
Reset	0	0	0	0	0	0	0	0

HDMI_FC_INT1 field descriptions

Field	Description
7 GMD	Interrupt indication bit Active after successful transmission of an Gamut metadata packet interrupt.
6 ISCR1	Interrupt indication bit Active after successful transmission of an International Standard Recording Code 1 packet interrupt.
5 ISCR2	Interrupt indication bit Active after successful transmission of an International Standard Recording Code 2 packet interrupt.
4 VSD	Interrupt indication bit Active after successful transmission of an Vendor Specific Data infoFrame packet interrupt.
3 SPD	Interrupt indication bit Active after successful transmission of an Source Product Descriptor infoFrame packet interrupt.
2 -	This field is reserved. Reserved
1 AVI	Interrupt indication bit Active after successful transmission of an AVI infoFrame packet interrupt.
0 GCP	Interrupt indication bit Active after successful transmission of an General Content Packet interrupt.

33.5.147 Frame Composer Packet Interrupt Mask Register 1 (HDMI_FC_MASK1)

Mask register for generation of FC_INT1 interrupts.

- Address Offset: 0x10D6

HDMI Memory Map/Register Definition

- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10D6h offset = 12_10D6h

Bit	7	6	5	4	3	2	1	0
Read Write	GMD	ISCR1	ISCR2	VSD	SPD	Reserved	AVI	GCP
Reset	0	0	0	0	0	0	0	0

HDMI_FC_MASK1 field descriptions

Field	Description
7 GMD	Mask bit for FC_INT1.GMD interrupt bit
6 ISCR1	Mask bit for FC_INT1.ISRC1 interrupt bit
5 ISCR2	Mask bit for FC_INT1.ISRC2 interrupt bit
4 VSD	Mask bit for FC_INT1.VSD interrupt bit
3 SPD	Mask bit for FC_INT1.SPD interrupt bit
2 -	This field is reserved. Reserved
1 AVI	Mask bit for FC_INT1.AVI interrupt bit
0 GCP	Mask bit for FC_INT1.GCP interrupt bit

33.5.148 FC_POL1 (HDMI_FC_POL1)

Polarity register for generation of FC_INT1 interrupts.

- Address Offset: 0x10D7
- Size: 8 bits
- Value after Reset: 0xFF
- Access: Read/Write

Address: 12_0000h base + 10D7h offset = 12_10D7h

Bit	7	6	5	4	3	2	1	0
Read Write	GMD	ISCR1	ISCR2	VSD	SPD	Reserved	AVI	GCP
Reset	1	1	1	1	1	1	1	1

HDMI_FC_POL1 field descriptions

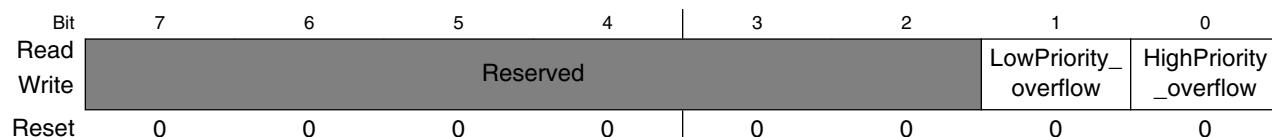
Field	Description
7 GMD	Polarity bit for FC_INT1.GMD interrupt bit
6 ISCR1	Polarity bit for FC_INT1.ISRC1 interrupt bit
5 ISCR2	Polarity bit for FC_INT1.ISRC2 interrupt bit
4 VSD	Polarity bit for FC_INT1.VSD interrupt bit
3 SPD	Polarity bit for FC_INT1.SPD interrupt bit
2 -	This field is reserved. Reserved
1 AVI	Polarity bit for FC_INT1.AVI interrupt bit
0 GCP	Polarity bit for FC_INT1.GCP interrupt bit

33.5.149 FC_STAT2 (HDMI_FC_STAT2)

This register contains the following active high packet sent status indications:

- Address Offset: 0x10D8
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10D8h offset = 12_10D8h

**HDMI_FC_STAT2 field descriptions**

Field	Description
7-2 -	This field is reserved. Reserved
1 LowPriority_overflow	Status bit Frame Composer low priority packet queue descriptor overflow indication.
0 HighPriority_overflow	Status bit Frame Composer high priority packet queue descriptor overflow indication.

33.5.150 FC_INT2 (HDMI_FC_INT2)

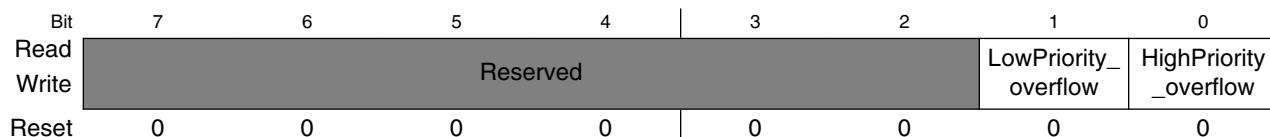
This register contains the interrupt indication of the FC_STAT2 status interrupts. Interrupt generation is accomplished in the following way:

```
interrupt = (mask == 1'b0) && (polarity == status);
```

All this interrupts are forwarded to the Interrupt Handler sticky bit registers and after ORed to a single main interrupt line to micro controller. Assertion of this interrupt implies that data related with the corresponding packet has been sent through the HDMI interface.

- Address Offset: 0x10D9
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10D9h offset = 12_10D9h



HDMI_FC_INT2 field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 LowPriority_overflow	Interrupt indication bit Frame Composer low priority packet queue descriptor overflow indication interrupt.
0 HighPriority_overflow	Interrupt indication bit Frame Composer high priority packet queue descriptor overflow indication interrupt.

33.5.151 Frame Composer High/Low Priority Overflow Interrupt Mask Register 2 (HDMI_FC_MASK2)

Mask register for generation of FC_INT2 interrupts.

- Address Offset: 0x10DA
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 10DAh offset = 12_10DAh

Bit	7	6	5	4	3	2	1	0
Read				Reserved			LowPriority_overflow	HighPriority_overflow
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_MASK2 field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 LowPriority_overflow	Mask bit for FC_INT1.LowPriority_overflow interrupt bit Value after Reset: 0b
0 HighPriority_overflow	Mask bit for FC_INT1.HighPriority_overflow interrupt bit Value after Reset: 0b

33.5.152 FC_POL2 (HDMI_FC_POL2)

Polarity register for generation of FC_INT2 interrupts.

- Address Offset: 0x10DB
- Size: 8 bits
- Value after Reset: 0x03
- Access: Read/Write

Address: 12_0000h base + 10DBh offset = 12_10DBh

Bit	7	6	5	4	3	2	1	0
Read				Reserved			LowPriority_overflow	HighPriority_overflow
Write	0	0	0	0	0	0	1	1
Reset	0	0	0	0	0	0	1	1

HDMI_FC_POL2 field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 LowPriority_overflow	Polarity bit for FC_INT1.LowPriority_overflow interrupt bit Value after Reset: 1b
0 HighPriority_overflow	Polarity bit for FC_INT1.HighPriority_overflow interrupt bit Value after Reset: 1b

33.5.153 Frame Composer Pixel Repetition Configuration Register (HDMI_FC_PRCNF)

Defines the Pixel Repetition ratio factor of the input and output video signal.

- Address Offset: 0x10E0
- Size: 8 bits
- Value after Reset: 0x10
- Access: Read/Write

Address: 12_0000h base + 10E0h offset = 12_10E0h

Bit	7	6	5	4	3	2	1	0
Read Write	incoming_pr_factor[3:0]				output_pr_factor[3:0]			
Reset	0	0	0	1	0	0	0	0

HDMI_FC_PRCNF field descriptions

Field	Description
7–4 incoming_pr_factor[3:0]	<p>Configures the input video pixel repetition. A plus 1 factor should be added in this register configuration. For CEA modes this value should be extracted from the CEA spec for the video mode being inputted.</p> <p>NOTE: When working in YCC422 video the actual repetition of the stream will be Incoming_pr_factor * (desired_pr_factor + 1). This calculation is done internally in the H13TCTRL and no HW overflow protection is available. Care must be taken to avoid this result passes the maximum number of 10 pixels repeated since no HDMI support is available for this in the spec and the H13TPHY does not support this higher repetition values.</p> <p>other: Reserved. Not used.</p> <p>0000 No action. Shall not be used. 0001 No pixel repetition (pixel sent only once). 0010 Pixel sent twice (pixel repeated once). 0011 Pixel sent 3 times. 0100 Pixel sent 4 times. 0101 Pixel sent 5 times. 0110 Pixel sent 6 times. 0111 Pixel sent 7 times. 1000 Pixel sent 8 times. 1001 Pixel sent 9 times. 1010 Pixel sent 10 times.</p>
output_pr_factor[3:0]	<p>Configures the video pixel repetition ratio to be sent on the AVI infoFrame. This value must be valid according to HDMI spec. The output_pr_factor = incoming_pr_factor(without the + 1 factor) * desired_pr_factor.</p> <p>other: Reserved. Not used.</p> <p>0000 No action. Shall not be used. 0001 Pixel sent twice (pixel repeated once). 0010 Pixel sent 3 times. 0011 Pixel sent 4 times.</p>

Table continues on the next page...

HDMI_FC_PRCNF field descriptions (continued)

Field	Description
	0100 Pixel sent 5 times.
	0101 Pixel sent 6 times.
	0110 Pixel sent 7 times.
	0111 Pixel sent 8 times.
	1000 Pixel sent 9 times.
	1001 Pixel sent 10 times.

33.5.154 Frame Composer GMD Packet Status Register (HDMI_FC_GMD_STAT)

Gamut metadata packet status bit information for no_current_gmd, next_gmd_field, gmd_packet_sequence and current_gamut_seq_num. For more information, refer to the HDMI 1.4a specification.

- Address Offset: 0x1100
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 1100h offset = 12_1100h

Bit	7	6	5	4
Read	igmdno_crnt_gbd	igmddnext_field	igmddpacket_seq[1:0]	
Write				
Reset	0	0	0	0
Bit	3	2	1	0
Read	igmddcurrent_gamut_seq_num[3:0]			
Write				
Reset	0	0	0	0

HDMI_FC_GMD_STAT field descriptions

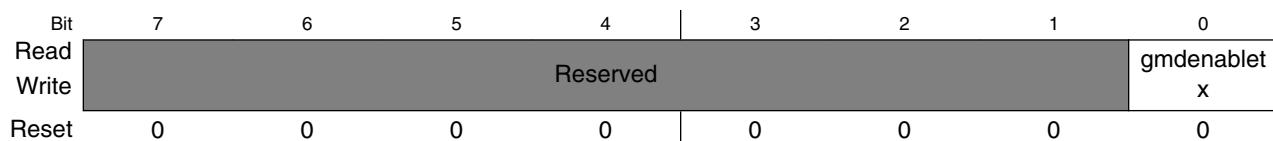
Field	Description
7 igmdno_crnt_gbd	Gamut scheduling: No current gamut data
6 igmddnext_field	Gamut scheduling: Gamut Next field
5–4 igmddpacket_seq[1:0]	Gamut scheduling: Gamut packet sequence
igmdcurrent_gamut_seq_num[3:0]	Gamut scheduling: Current Gamut packet sequence number

33.5.155 Frame Composer GMD Packet Enable Register (HDMI_FC_GMD_EN)

This register enables Gamut metadata (GMD) packet transmission. Packets are inserted in the incoming frame, starting in the line where active Vsync indication starts. After enable of GMD packets the outgoing packet is sent with no_current_gmd active indication until update GMD request is performed in the controller.

- Address Offset: 0x1101
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1101h offset = 12_1101h



HDMI_FC_GMD_EN field descriptions

Field	Description
7–1 - Reserved	This field is reserved.
0 gmdenabletx	Gamut Metadata packet transmission enable (1b).

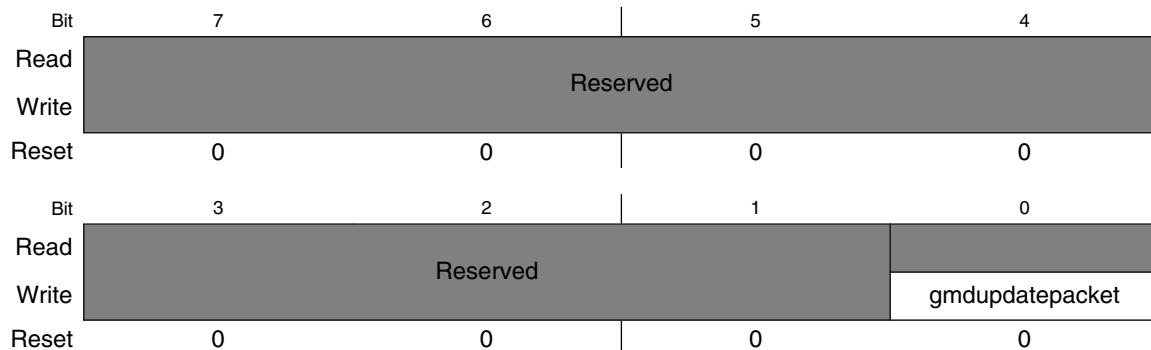
33.5.156 Frame Composer GMD Packet Update Register (HDMI_FC_GMD_UP)

This register performs an GMD packet content update according to the configured packet body (FC_GMD_PB0 to FC_GMD_PB27) and packet header (FC_GMD_HB). This active high auto clear register reflects the body and header configurations on the GMD packets sent arbitrating the current_gamut_seq_num, gmd_packet_sequence and next_gmd_field bits on packet to correctly indicate to source the Gamut change to be performed. After enable GMD packets the first update request is also responsible for deactivating the no_current_gmd indication bit. Attention packet update request must only be done after correct configuration of GMD packet body and header registers. Correct affected_gamut_seq_num and gmd_profile configuration is user responsibility and must convey with HDMI 1.4a standard gamut rules.

- Address Offset: 0x1102

- Size: 8 bits
- Value after Reset: 0x00
- Access: Write

Address: 12_0000h base + 1102h offset = 12_1102h



HDMI_FC_GMD_UP field descriptions

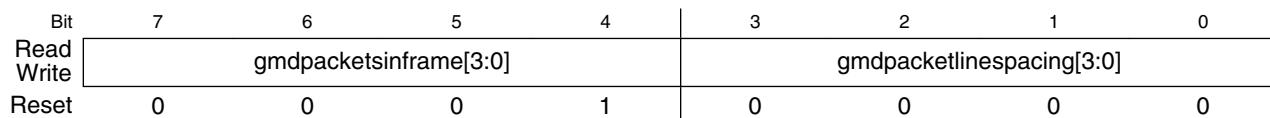
Field	Description
7–1 -	This field is reserved. Reserved
0 gmdupdatepacket	Gamut Metadata packet update.

33.5.157 Frame Composer GMD Packet Schedule Configuration Register (HDMI_FC_GMD_CONF)

This register configures the number of GMD packets to be inserted per frame (starting always in the line where the active Vsync appears) and the line spacing between the transmitted GMD packets. Note that for profile P0 (refer to HDMI 1.4a spec) this register should only indicate one GMD packet to be inserted per video field.

- Address Offset: 0x1103
- Size: 8 bits
- Value after Reset: 0x10
- Access: Read/Write

Address: 12_0000h base + 1103h offset = 12_1103h



HDMI_FC_GMD_CONF field descriptions

Field	Description
7–4 gmdpacketsinframe[3:0]	Number of GMD packets per frame or video field (profile P0)
gmdpacketlinespacing[3:0]	Number of line spacing between the transmitted GMD packets

33.5.158 Frame Composer GMD Packet Profile and Gamut Sequence Configuration Register (HDMI_FC_GMD_HB)

This register configures the GMD packet header affected_gamut_seq_num and gmd_profile bits. For more information, refer to the HDMI 1.4a specification.

- Address Offset: 0x1104
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1104h offset = 12_1104h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved		gmdgbd_profile		gmdaffected_gamut_seq_num			
Reset	0	0	0	0	0	0	0	0

HDMI_FC_GMD_HB field descriptions

Field	Description
7 -	This field is reserved. Reserved
6–4 gmdgbd_profile	GMD profile bits
gmdaffected_gamut_seq_num	Affected gamut sequence number

33.5.159 Frame Composer GMD Packet Body Register 0 (HDMI_FC_GMD_PB0)

Configures the following contents of the GMD packet:

- GMD packet body byte0
- Address Offset: 0x1105
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1105h offset = 12_1105h

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB0	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB0 field descriptions

Field	Description
FC_GMD_PB0	Gamut Metadata packet byte0

33.5.160 Frame Composer GMD Packet Body Register 1 (HDMI_FC_GMD_PB1)

- GMD packet body byte1
- Address Offset: 0x1106
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1106h offset = 12_1106h

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB1	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB1 field descriptions

Field	Description
FC_GMD_PB1	Gamut Metadata packet byte1

33.5.161 Frame Composer GMD Packet Body Register 2 (HDMI_FC_GMD_PB2)

- GMD packet body byte2
- Address Offset: 0x1107
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1107h offset = 12_1107h

Bit	7	6	5	4		3	2	1	0
Read					FC_GMD_PB2				
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB2 field descriptions

Field	Description
FC_GMD_PB2	Gamut Metadata packet byte2

33.5.162 Frame Composer GMD Packet Body Register 3 (HDMI_FC_GMD_PB3)

- GMD packet body byte3
- Address Offset: 0x1108
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1108h offset = 12_1108h

Bit	7	6	5	4		3	2	1	0
Read					FC_GMD_PB3				
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB3 field descriptions

Field	Description
FC_GMD_PB3	Gamut Metadata packet byte3

33.5.163 Frame Composer GMD Packet Body Register 4 (HDMI_FC_GMD_PB4)

- GMD packet body byte4
- Address Offset: 0x1109
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1109h offset = 12_1109h

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB4	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB4 field descriptions

Field	Description
FC_GMD_PB4	Gamut Metadata packet byte4

33.5.164 Frame Composer GMD Packet Body Register 5 (HDMI_FC_GMD_PB5)

- GMD packet body byte5
- Address Offset: 0x110a
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 110Ah offset = 12_110Ah

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB5	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB5 field descriptions

Field	Description
FC_GMD_PB5	Gamut Metadata packet byte5

33.5.165 Frame Composer GMD Packet Body Register 6 (HDMI_FC_GMD_PB6)

- GMD packet body byte6
- Address Offset: 0x110b
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 110Bh offset = 12_110Bh

Bit	7	6	5	4		3	2	1	0
Read					FC_GMD_PB6				
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB6 field descriptions

Field	Description
FC_GMD_PB6	Gamut Metadata packet byte6

33.5.166 Frame Composer GMD Packet Body Register 7 (HDMI_FC_GMD_PB7)

- GMD packet body byte7
- Address Offset: 0x110c
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 110Ch offset = 12_110Ch

Bit	7	6	5	4		3	2	1	0
Read					FC_GMD_PB2				
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB7 field descriptions

Field	Description
FC_GMD_PB2	Gamut Metadata packet byte7

33.5.167 Frame Composer GMD Packet Body Register 8 (HDMI_FC_GMD_PB8)

- GMD packet body byte8
- Address Offset: 0x110d
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 110Dh offset = 12_110Dh

Bit	7	6	5	4		3	2	1	0
Read Write	FC_GMD_PB8								
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB8 field descriptions

Field	Description
FC_GMD_PB8	Gamut Metadata packet byte8

33.5.168 Frame Composer GMD Packet Body Register 9 (HDMI_FC_GMD_PB9)

- GMD packet body byte9
- Address Offset: 0x110e
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 110Eh offset = 12_110Eh

Bit	7	6	5	4		3	2	1	0
Read Write	FC_GMD_PB9								
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB9 field descriptions

Field	Description
FC_GMD_PB9	Gamut Metadata packet byte9

33.5.169 Frame Composer GMD Packet Body Register 10 (HDMI_FC_GMD_PB10)

- GMD packet body byte10
- Address Offset: 0x110f
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 110Fh offset = 12_110Fh

Bit	7	6	5	4		3	2	1	0
Read						FC_GMD_PB10			
Write	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB10 field descriptions

Field	Description
FC_GMD_PB10	Gamut Metadata packet byte10

33.5.170 Frame Composer GMD Packet Body Register 11 (HDMI_FC_GMD_PB11)

- GMD packet body byte11
- Address Offset: 0x1110
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1110h offset = 12_1110h

Bit	7	6	5	4		3	2	1	0
Read						FC_GMD_PB11			
Write	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB11 field descriptions

Field	Description
FC_GMD_PB11	Gamut Metadata packet byte11

33.5.171 Frame Composer GMD Packet Body Register 12 (HDMI_FC_GMD_PB12)

- GMD packet body byte12
- Address Offset: 0x1111
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1111h offset = 12_1111h

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB12	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB12 field descriptions

Field	Description
FC_GMD_PB12	Gamut Metadata packet byte12

33.5.172 Frame Composer GMD Packet Body Register 13 (HDMI_FC_GMD_PB13)

- GMD packet body byte13
- Address Offset: 0x1112
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1112h offset = 12_1112h

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB13	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB13 field descriptions

Field	Description
FC_GMD_PB13	Gamut Metadata packet byte13

33.5.173 Frame Composer GMD Packet Body Register 14 (HDMI_FC_GMD_PB14)

- GMD packet body byte14
- Address Offset: 0x1113
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1113h offset = 12_1113h

Bit	7	6	5	4		3	2	1	0
Read						FC_GMD_PB14			
Write	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB14 field descriptions

Field	Description
FC_GMD_PB14	Gamut Metadata packet byte14

33.5.174 Frame Composer GMD Packet Body Register 15 (HDMI_FC_GMD_PB15)

- GMD packet body byte15
- Address Offset: 0x1114
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1114h offset = 12_1114h

Bit	7	6	5	4		3	2	1	0
Read						FC_GMD_PB15			
Write	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB15 field descriptions

Field	Description
FC_GMD_PB15	Gamut Metadata packet byte15

33.5.175 Frame Composer GMD Packet Body Register 16 (HDMI_FC_GMD_PB16)

- GMD packet body byte16
- Address Offset: 0x1115
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1115h offset = 12_1115h

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB16	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB16 field descriptions

Field	Description
FC_GMD_PB16	Gamut Metadata packet byte16

33.5.176 Frame Composer GMD Packet Body Register 17 (HDMI_FC_GMD_PB17)

- GMD packet body byte17
- Address Offset: 0x1116
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1116h offset = 12_1116h

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB17	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB17 field descriptions

Field	Description
FC_GMD_PB17	Gamut Metadata packet byte17

33.5.177 Frame Composer GMD Packet Body Register 18 (HDMI_FC_GMD_PB18)

- GMD packet body byte18
- Address Offset: 0x1117
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1117h offset = 12_1117h

Bit	7	6	5	4		3	2	1	0
Read						FC_GMD_PB18			
Write	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB18 field descriptions

Field	Description
FC_GMD_PB18	Gamut Metadata packet byte18

33.5.178 Frame Composer GMD Packet Body Register 19 (HDMI_FC_GMD_PB19)

- GMD packet body byte19
- Address Offset: 0x1118
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1118h offset = 12_1118h

Bit	7	6	5	4		3	2	1	0
Read						FC_GMD_PB18			
Write	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB19 field descriptions

Field	Description
FC_GMD_PB18	Gamut Metadata packet byte18

33.5.179 Frame Composer GMD Packet Body Register 20 (HDMI_FC_GMD_PB20)

- GMD packet body byte20
- Address Offset: 0x1119
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1119h offset = 12_1119h

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB20	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB20 field descriptions

Field	Description
FC_GMD_PB20	Gamut Metadata packet byte20

33.5.180 Frame Composer GMD Packet Body Register 21 (HDMI_FC_GMD_PB21)

- GMD packet body byte21
- Address Offset: 0x111a
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 111Ah offset = 12_111Ah

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB21	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB21 field descriptions

Field	Description
FC_GMD_PB21	Gamut Metadata packet byte21

33.5.181 Frame Composer GMD Packet Body Register 22 (HDMI_FC_GMD_PB22)

- GMD packet body byte22
- Address Offset: 0x111b
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 111Bh offset = 12_111Bh

Bit	7	6	5	4		3	2	1	0
Read						FC_GMD_PB22			
Write	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB22 field descriptions

Field	Description
FC_GMD_PB22	Gamut Metadata packet byte22

33.5.182 Frame Composer GMD Packet Body Register 23 (HDMI_FC_GMD_PB23)

- GMD packet body byte23
- Address Offset: 0x111c
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 111Ch offset = 12_111Ch

Bit	7	6	5	4		3	2	1	0
Read						FC_GMD_PB23			
Write	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB23 field descriptions

Field	Description
FC_GMD_PB23	Gamut Metadata packet byte23

33.5.183 Frame Composer GMD Packet Body Register 24 (HDMI_FC_GMD_PB24)

- GMD packet body byte24
- Address Offset: 0x111d
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 111Dh offset = 12_111Dh

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB24	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB24 field descriptions

Field	Description
FC_GMD_PB24	Gamut Metadata packet byte24

33.5.184 Frame Composer GMD Packet Body Register 25 (HDMI_FC_GMD_PB25)

- GMD packet body byte25
- Address Offset: 0x111e
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 111Eh offset = 12_111Eh

Bit	7	6	5	4		3	2	1	0
Read Write	0	0	0	0	FC_GMD_PB25	0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB25 field descriptions

Field	Description
FC_GMD_PB25	Gamut Metadata packet byte25

33.5.185 Frame Composer GMD Packet Body Register 26 (HDMI_FC_GMD_PB26)

- GMD packet body byte26
- Address Offset: 0x111f
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 111Fh offset = 12_111Fh

Bit	7	6	5	4		3	2	1	0
Read Write					FC_GMD_PB26				
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB26 field descriptions

Field	Description
FC_GMD_PB26	Gamut Metadata packet byte26

33.5.186 Frame Composer GMD Packet Body Register 27 (HDMI_FC_GMD_PB27)

- GMD packet body byte27
- Address Offset: 0x1120
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

For more information, refer to the HDMI 1.4a specification.

Address: 12_0000h base + 1120h offset = 12_1120h

Bit	7	6	5	4		3	2	1	0
Read Write					FC_GMD_PB27				
Reset	0	0	0	0		0	0	0	0

HDMI_FC_GMD_PB27 field descriptions

Field	Description
FC_GMD_PB27	Gamut Metadata packet byte27

33.5.187 Frame Composer Video/Audio Force Enable Register (HDMI_FC_DBGFORCE)

This register allows to force the controller to output audio and video data the values configured in the FC_DBGAUD and FC_DBGTMDS registers.

- Address Offset: 0x1200
- Size: 8 bits

- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1200h offset = 12_1200h

Bit	7	6	5	4		3	2	1	0	
Read Write	Reserved				forceaudio	Reserved				forcevideo
Reset	0	0	0	0		0	0	0	0	

HDMI_FC_DBGFORCE field descriptions

Field	Description
7–5 -	This field is reserved. Reserved
4 forceaudio	Force fixed audio output with FC_DBGAUDxCHx registers contain.
3–1 -	This field is reserved. Reserved
0 forcevideo	Force fixed video output with FC_DBGTMDSx registers contain.

33.5.188 Frame Composer Audio Channel 0 Register 0 (HDMI_FC_DBGAUD0CH0)

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

- Address Offset: 0x1201
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1201h offset = 12_1201h

Bit	7	6	5	4		3	2	1	0
Read Write	FC_DBGAUD0CH0					0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_DBGAUD0CH0 field descriptions

Field	Description
FC_DBGAUD0CH0	the audio fixed data byte0 to be used in channel 0 when in fixed audio selection

33.5.189 Frame Composer Audio Channel 0 Register 1 (HDMI_FC_DBGAUD1CH0)

- Address Offset: 0x1202
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1202h offset = 12_1202h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0		0	0	0	0
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_DBGAUD1CH0 field descriptions

Field	Description
FC_DBGAUD1CH0	the audio fixed data byte1 to be used in channel 0 when in fixed audio selection

33.5.190 Frame Composer Audio Channel 0 Register 2 (HDMI_FC_DBGAUD2CH0)

- Address Offset: 0x1203
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1203h offset = 12_1203h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0		0	0	0	0
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_DBGAUD2CH0 field descriptions

Field	Description
FC_DBGAUD2CH0	the audio fixed data byte2 to be used in channel 0 when in fixed audio selection

33.5.191 Frame Composer Audio Channel 1 Register 0 (HDMI_FC_DBGAUD0CH1)

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

- Address Offset: 0x1204
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1204h offset = 12_1204h

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGAUD0CH1							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD0CH1 field descriptions

Field	Description
FC_DBGAUD0CH1	the audio fixed data byte2 to be used in channel 0 when in fixed audio selection

33.5.192 Frame Composer Audio Channel 1 Register 1 (HDMI_FC_DBGAUD1CH1)

- Address Offset: 0x1205
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1205h offset = 12_1205h

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGAUD1CH1							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD1CH1 field descriptions

Field	Description
FC_DBGAUD1CH1	the audio fixed data byte1 to be used in channel 1 when in fixed audio selection

33.5.193 Frame Composer Audio Channel 1 Register 2 (HDMI_FC_DBGAUD2CH1)

- Address Offset: 0x1206
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1206h offset = 12_1206h

Bit	7	6	5	4		3	2	1	0
Read	FC_DBGAUD2CH1								
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_FC_DBGAUD2CH1 field descriptions

Field	Description
FC_DBGAUD2CH1	the audio fixed data byte2 to be used in channel 1 when in fixed audio selection

33.5.194 Frame Composer Debug Audio Channel 2 Register 0 (HDMI_FC_DBGAUD0CH2)

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

- Address Offset: 0x1207
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1207h offset = 12_1207h

Bit	7	6	5	4		3	2	1	0
Read	FC_DBGAUD0CH2								
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_FC_DBGAUD0CH2 field descriptions

Field	Description
FC_DBGAUD0CH2	the audio fixed data byte0 to be used in channel 2 when in fixed audio selection

33.5.195 Frame Composer Debug Audio Channel 2 Register 1 (HDMI_FC_DBGAUD1CH2)

- Address Offset: 0x1208
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1208h offset = 12_1208h

Bit	7	6	5	4	3	2	1	0
Read	FC_DBGAUD1CH2							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD1CH2 field descriptions

Field	Description
FC_DBGAUD1CH2	the audio fixed data byte1 to be used in channel 2 when in fixed audio selection

33.5.196 Frame Composer Audio Channel 2 Register 2 (HDMI_FC_DBGAUD2CH2)

- Address Offset: 0x1209
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1209h offset = 12_1209h

Bit	7	6	5	4	3	2	1	0
Read	FC_DBGAUD2CH2							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD2CH2 field descriptions

Field	Description
FC_DBGAUD2CH2	the audio fixed data byte2 to be used in channel 2 when in fixed audio selection

33.5.197 Frame Composer Audio Channel 3 Register 0 (HDMI_FC_DBGAUD0CH3)

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

- Address Offset: 0x120A
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 120Ah offset = 12_120Ah

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGAUD0CH3							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD0CH3 field descriptions

Field	Description
FC_DBGAUD0CH3	the audio fixed data byte0 to be used in channel 3 when in fixed audio selection

33.5.198 Frame Composer Audio Channel 3 Register 1 (HDMI_FC_DBGAUD1CH3)

- Address Offset: 0x120B
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 120Bh offset = 12_120Bh

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGAUD1CH3							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD1CH3 field descriptions

Field	Description
FC_DBGAUD1CH3	the audio fixed data byte1 to be used in channel 3 when in fixed audio selection

33.5.199 Frame Composer Audio Channel 3 Register 2 (HDMI_FC_DBGAUD2CH3)

- Address Offset: 0x120C
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 120Ch offset = 12_120Ch

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD2CH3 field descriptions

Field	Description
FC_DBGAUD2CH3	the audio fixed data byte2 to be used in channel 3 when in fixed audio selection

33.5.200 Frame Composer Audio Channel 4 Register 0 (HDMI_FC_DBGAUD0CH4)

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

- Address Offset: 0x120D
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 120Dh offset = 12_120Dh

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD0CH4 field descriptions

Field	Description
FC_DBGAUD0CH4	the audio fixed data byte0 to be used in channel 4 when in fixed audio selection

33.5.201 Frame Composer Audio Channel 4 Register 1 (HDMI_FC_DBGAUD1CH4)

- Address Offset: 0x120E
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 120Eh offset = 12_120Eh

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	FC_DBGAUD1CH4	0	0	0	0
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_DBGAUD1CH4 field descriptions

Field	Description
FC_DBGAUD1CH4	the audio fixed data byte1 to be used in channel 4 when in fixed audio selection

33.5.202 Frame Composer Audio Channel 4 Register 2 (HDMI_FC_DBGAUD2CH4)

- Address Offset: 0x120F
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 120Fh offset = 12_120Fh

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	FC_DBGAUD2CH4	0	0	0	0
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_FC_DBGAUD2CH4 field descriptions

Field	Description
FC_DBGAUD2CH4	the audio fixed data byte2 to be used in channel 4 when in fixed audio selection

33.5.203 Frame Composer Audio Channel 5 Register 0 (HDMI_FC_DBGAUD0CH5)

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

- Address Offset: 0x1210
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1210h offset = 12_1210h

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGAUD0CH5							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD0CH5 field descriptions

Field	Description
FC_DBGAUD0CH5	the audio fixed data byte0 to be used in channel 5 when in fixed audio selection

33.5.204 Frame Composer Audio Channel 5 Register 1 (HDMI_FC_DBGAUD1CH5)

- Address Offset: 0x1211
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1211h offset = 12_1211h

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGAUD1CH5							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD1CH5 field descriptions

Field	Description
FC_DBGAUD1CH5	the audio fixed data byte1 to be used in channel 5 when in fixed audio selection

33.5.205 Frame Composer Audio Channel 5 Register 2 (HDMI_FC_DBGAUD2CH5)

- Address Offset: 0x1212
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1212h offset = 12_1212h

Bit	7	6	5	4		3	2	1	0
Read	FC_DBGAUD2CH5								
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_FC_DBGAUD2CH5 field descriptions

Field	Description
FC_DBGAUD2CH5	the audio fixed data byte2 to be used in channel 5 when in fixed audio selection

33.5.206 Frame Composer Audio Channel 6 Register 0 (HDMI_FC_DBGAUD0CH6)

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

- Address Offset: 0x1213
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1213h offset = 12_1213h

Bit	7	6	5	4		3	2	1	0
Read	FC_DBGAUD0CH6								
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_FC_DBGAUD0CH6 field descriptions

Field	Description
FC_DBGAUD0CH6	The audio fixed data byte0 to be used in channel 6 when in fixed audio selection

33.5.207 Frame Composer Audio Channel 6 Register 1 (HDMI_FC_DBGAUD1CH6)

- Address Offset: 0x1214
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1214h offset = 12_1214h

Bit	7	6	5	4	3	2	1	0
Read	FC_DBGAUD1CH6							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD1CH6 field descriptions

Field	Description
FC_DBGAUD1CH6	the audio fixed data byte1 to be used in channel 6 when in fixed audio selection

33.5.208 Frame Composer Audio Channel 6 Register 2 (HDMI_FC_DBGAUD2CH6)

- Address Offset: 0x1215
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1215h offset = 12_1215h

Bit	7	6	5	4	3	2	1	0
Read	FC_DBGAUD2CH6							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD2CH6 field descriptions

Field	Description
FC_DBGAUD2CH6	the audio fixed data byte2 to be used in channel 6 when in fixed audio selection

33.5.209 Frame Composer Audio Channel 7 Register 1 (HDMI_FC_DBGAUD0CH7)

Configures the audio fixed data to be used in channel 7 when in fixed audio selection.

- Address Offset: 0x1216
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1216h offset = 12_1216h

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGAUD0CH7							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD0CH7 field descriptions

Field	Description
FC_DBGAUD0CH7	the audio fixed data byte0 to be used in channel 7 when in fixed audio selection

33.5.210 Frame Composer Audio Channel 7 Register 0 (HDMI_FC_DBGAUD1CH7)

- Address Offset: 0x1217
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1217h offset = 12_1217h

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGAUD1CH7							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD1CH7 field descriptions

Field	Description
FC_DBGAUD1CH7	the audio fixed data byte1 to be used in channel 0 when in fixed audio selection

33.5.211 Frame Composer Audio Channel 7 Register 2 (HDMI_FC_DBGAUD2CH7)

- Address Offset: 0x1218
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1218h offset = 12_1218h

Bit	7	6	5	4	3	2	1	0
Read	FC_DBGAUD2CH7							
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGAUD2CH7 field descriptions

Field	Description
FC_DBGAUD2CH7	the audio fixed data byte2 to be used in channel 0 when in fixed audio selection

33.5.212 Frame Composer TMDS Channel 0 Register (HDMI_FC_DBGTMDS0)

Configures the video fixed data to be used in tmds channel 0 when in fixed video selection. This equals to set B pixel component value in RGB video or Cb pixel component value in YCbCr.

- Address Offset: 0x1219
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 1219h offset = 12_1219h

Bit	7	6	5	4	3	2	1	0
Read	FC_DBGTMDS0							
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGTMDS0 field descriptions

Field	Description
FC_DBGTMDS0	set B pixel component value in RGB video or Cb pixel component value in YCbCr

33.5.213 Frame Composer TMDS Channel 1 Register (HDMI_FC_DBGTMDS1)

Configures the video fixed data to be used in tmds channel 1 when in fixed video selection. This equals to set G pixel component value in RGB video or Y pixel component value in YCbCr.

- Address Offset: 0x121A
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 121Ah offset = 12_121Ah

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGTMDS1							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGTMDS1 field descriptions

Field	Description
FC_DBGTMDS1	set G pixel component value in RGB video or Y pixel component value in YCbCr

33.5.214 Frame Composer TMDS Channel 2 Register (HDMI_FC_DBGTMDS2)

Configures the video fixed data to be used in tmds channel 2 when in fixed video selection. This equals to set R pixel component value in RGB video or Cr pixel component value in YCbCr.

- Address Offset: 0x121B
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 121Bh offset = 12_121Bh

Bit	7	6	5	4	3	2	1	0
Read Write	FC_DBGTMDS2							
Reset	0	0	0	0	0	0	0	0

HDMI_FC_DBGTMDS2 field descriptions

Field	Description
FC_DBGTMDS2	set R pixel component value in RGB video or Cr pixel component value in YCbCr

33.5.215 PHY Configuration Register (HDMI_PHY_CONF0)

This register holds the power down, data enable polarity and interface control of the HDMI Source PHY control. For more information, refer to the DesignWare Cores HDMI TX PHY Databook.

- Address Offset: 0x3000
- Size: 8 bits
- Value after Reset: 0x06
- Access: Read/Write

Address: 12_0000h base + 3000h offset = 12_3000h

Bit	7	6	5	4
Read	PDZ	ENTMDS	sparectrl	gen2_pddq
Write				
Reset	0	0	0	0
Bit	3	2	1	0
Read	gen2_txpwron	gen2_enhpdrxsense	seldataenpol	seldipif
Write				
Reset	0	1	1	0

HDMI_PHY_CONF0 field descriptions

Field	Description
7 PDZ	Power-down enable (active low 0b). Value after Reset: 0b
6 ENTMDS	Enable TMDS drivers, bias, and TMDS digital logic. Value after Reset: 0b
5 sparectrl	Reserved. Spare pin control. Value after Reset: 0b
4 gen2_pddq	PHY_Gen2 PDDQ signal Value after Reset: 0b
3 gen2_txpwron	PHY_Gen2 TXPWRON signal Value after Reset: 0b
2 gen2_enhpdrxsense	PHY_Gen2 ENHPDRXSENSE signal Value after Reset: 1b
1 seldataenpol	Select data enable polarity. Value after Reset: 1b

Table continues on the next page...

HDMI_PHY_CONF0 field descriptions (continued)

Field	Description
0 seldipif	Select interface control. Value after Reset: 0b

33.5.216 PHY Test Interface Register 0 (HDMI_PHY_TST0)

PHY TX mapped text interface (control). For more information, refer to the DesignWare Cores HDMI TX PHY Databook.

- Address Offset: 0x3001
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3001h offset = 12_3001h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved		testclr	testen	Reserved		testclk	
Reset	0	0	0	0	0	0	0	0

HDMI_PHY_TST0 field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5 testclr	Enable TMDS drivers, bias and tmds digital logic. Value after Reset: 0b
4 testen	Reserved. Spare control pins. Value after Reset: 0b
3–1 -	This field is reserved. Reserved
0 testclk	Test clock signal. Value after Reset: 0b

33.5.217 PHY Test Interface Register 1 (HDMI_PHY_TST1)

PHY TX mapped text interface (data in). For more information, refer to the DesignWare Cores HDMI TX PHY Databook.

- Address Offset: 0x3002
- Size: 8 bits

- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3002h offset = 12_3002h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0		testdin[7:0]	0	0	0
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_PHY_TST1 field descriptions

Field	Description
testdin[7:0]	Test data input.

33.5.218 PHY Test Interface Register 2 (HDMI_PHY_TST2)

PHY TX mapped text interface (data out). For more information, refer to the DesignWare Cores HDMI TX PHY Databook.

- Address Offset: 0x3003
- Size: 8 bits
- Value after Reset: N/A
- Access: Read

Address: 12_0000h base + 3003h offset = 12_3003h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0		testdout[7:0]	0	0	0
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_PHY_TST2 field descriptions

Field	Description
testdout[7:0]	Test data output.

33.5.219 PHY RXSENSE, PLL lock, and HPD Status Register (HDMI_PHY_STAT0)

This register contains the following active high packet sent status indications. For more information, see [Overview](#)

- Address Offset: 0x3004
- Size: 8 bits

HDMI Memory Map/Register Definition

- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 3004h offset = 12_3004h

Bit	7	6	5	4
Read	RX_SENSE3	RX_SENSE2	RX_SENSE1	RX_SENSE0
Write				
Reset	0	0	0	0
Bit	3	2	1	0
Read	Reserved		HPD	TX_PHY_LOCK
Write				
Reset	0	0	0	0

HDMI_PHY_STAT0 field descriptions

Field	Description
7 RX_SENSE3	Status bit. TX PHY RX_SENSE indication for TMDS CLK driver. User may need to mask or change polarity of this interrupt after it has became active.
6 RX_SENSE2	Status bit. TX PHY RX_SENSE indication for TMDS channel 2 driver. User may need to mask or change polarity of this interrupt after it has became active.
5 RX_SENSE1	Status bit. TX PHY RX_SENSE indication for TMDS channel 1 driver. User may need to mask or change polarity of this interrupt after it has became active.
4 RX_SENSE0	Status bit. TX PHY RX_SENSE indication for TMDS channel 0 driver. User may need to mask or change polarity of this interrupt after it has became active.
3–2 -	This field is reserved. Reserved
1 HPD	Status bit. HDMI Hot Plug Detect indication. User may need to mask or change polarity of this interrupt after it has became active.
0 TX_PHY_LOCK	Status bit. TX PHY PLL lock indication. Please refer to PHY datasheet for more information. User may need to mask or change polarity of this interrupt after it has became active.

33.5.220 PHY RXSENSE, PLL lock, and HPD Interrupt Register (HDMI_PHY_INTO)

This register contains the interrupt indication of the PHY_STAT0 status interrupts. Interrupt generation is accomplished in the following way:

interrupt = (mask == 1'b0) && (polarity == status);

All this interrupts are forwarded to the Interrupt Handler sticky bit registers and after ORed to a single main interrupt line to micro controller. Assertion of this interrupt implies that data related with the corresponding packet has been sent through the HDMI interface.

- Address Offset: 0x3005

- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 3005h offset = 12_3005h

Bit	7	6	5	4
Read	RX_SENSE3	RX_SENSE2	RX_SENSE1	RX_SENSE0
Write				
Reset	0	0	0	0
Bit	3	2	1	0
Read	Reserved		HPD	TX_PHY_LOCK
Write				
Reset	0	0	0	0

HDMI_PHY_INT0 field descriptions

Field	Description
7 RX_SENSE3	Interrupt indication bit TX PHY RX_SENSE indication interrupt for TMDS CLK driver.
6 RX_SENSE2	Interrupt indication bit TX PHY RX_SENSE indication interrupt for TMDS channel 2 driver.
5 RX_SENSE1	Interrupt indication bit TX PHY RX_SENSE indication interrupt for TMDS channel 1 driver.
4 RX_SENSE0	Interrupt indication bit TX PHY RX_SENSE indication interrupt for TMDS channel 0 driver.
3–2 -	This field is reserved. Reserved
1 HPD	Interrupt indication bit HDMI Hot Plug Detect indication interrupt.
0 TX_PHY_LOCK	Interrupt indication bit TX PHY PLL lock indication interrupt.

33.5.221 PHY RXSENSE, PLL lock, and HPD Mask Register (HDMI_PHY_MASK0)

Mask register for generation of PHY_INT0 interrupts.

- Address Offset: 0x3006
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

Address: 12_0000h base + 3006h offset = 12_3006h

Bit	7	6	5	4	3	2	1	0
Read	RX_SENSE3	RX_SENSE2	RX_SENSE1	RX_SENSE0	Reserved	HPD	TX_PHY_LOCK	
Write	0	0	0	0	0	0	0	0
Reset								

HDMI_PHY_MASK0 field descriptions

Field	Description
7 RX_SENSE3	Mask bit for PHY_INT0.RX_SENSE3 interrupt bit
6 RX_SENSE2	Mask bit for PHY_INT0.RX_SENSE2 interrupt bit
5 RX_SENSE1	Mask bit for PHY_INT0.RX_SENSE1 interrupt bit
4 RX_SENSE0	Mask bit for PHY_INT0.RX_SENSE0 interrupt bit
3–2 -	This field is reserved. Reserved
1 HPD	Mask bit for PHY_INT0.HPD interrupt bit
0 TX_PHY_LOCK	Mask bit for PHY_INT0.TX_PHY_LOCK interrupt bit

33.5.222 PHY RXSENSE, PLL lock and HPD Polarity Register (HDMI_PHY_POL0)

Polarity register for generation of PHY_INT0 interrupts.

- Address Offset: 0x3007
- Size: 8 bits
- Value after Reset: 0xF3
- Access: Read/Write

Address: 12_0000h base + 3007h offset = 12_3007h

Bit	7	6	5	4	3	2	1	0
Read	RX_SENSE3	RX_SENSE2	RX_SENSE1	RX_SENSE0	Reserved	HPD	TX_PHY_LOCK	
Write	1	1	1	1	0	0	1	1
Reset								

HDMI_PHY_POL0 field descriptions

Field	Description
7 RX_SENSE3	Polarity bit for PHY_INT0.RX_SENSE3 interrupt bit

Table continues on the next page...

HDMI_PHY_POL0 field descriptions (continued)

Field	Description
6 RX_SENSE2	Polarity bit for PHY_INT0.RX_SENSE2 interrupt bit
5 RX_SENSE1	Polarity bit for PHY_INT0.RX_SENSE1 interrupt bit
4 RX_SENSE0	Polarity bit for PHY_INT0.RX_SENSE0 interrupt bit
3–2 -	This field is reserved. Reserved
1 HPD	Polarity bit for PHY_INT0.HPD interrupt bit
0 TX_PHY_LOCK	Polarity bit for PHY_INT0.TX_PHY_LOCK interrupt bit

33.5.223 PHY I2C Slave Address Configuration Register (HDMI_PHY_I2CM_SLAVE_ADDR)

This register writes the slave address of the I2C Master PHY.

- Address Offset: 0x3020
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3020h offset = 12_3020h

Bit	7	6	5	4		3	2	1	0
Read Write	Reserved				-				
Reset	0	0	0	0		0	0	0	0

HDMI_PHY_I2CM_SLAVE_ADDR field descriptions

Field	Description
7 -	This field is reserved. Reserved
-	Slave address to be sent during read and write operations. The PHY Gen2 slave address is: 7'h69 The HEAC PHY slave address is: 7'h49

33.5.224 PHY I2C Address Configuration Register (HDMI_PHY_I2CM_ADDRESS_ADDR)

This register writes the address for read and writer operations.

HDMI Memory Map/Register Definition

- Address Offset: 0x3021
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3021h offset = 12_3021h

Bit	7	6	5	4	3	2	1	0
Read					address			
Write								

HDMI_PHY_I2CM_ADDRESS_ADDR field descriptions

Field	Description
address	Register address for read and write operations.

33.5.225 PHY I2C Data Write Register 1 (HDMI_PHY_I2CM_DATAO_1_ADDR)

- Address Offset: 0x3022
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3022h offset = 12_3022h

Bit	7	6	5	4	3	2	1	0
Read					datao[15:8]			
Write								

HDMI_PHY_I2CM_DATAO_1_ADDR field descriptions

Field	Description
datao[15:8]	MSB's of data to be written on register pointed by address [7:0].

33.5.226 PHY I2C Data Write Register 0 (HDMI_PHY_I2CM_DATAO_0_ADDR)

- Address Offset: 0x3023
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3023h offset = 12_3023h

Bit	7	6	5	4		3	2	1	0
Read	datao[7:0]								
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_PHY_I2CM_DATAO_0_ADDR field descriptions

Field	Description
datao[7:0]	LSB's of data to be written on register pointed by address [7:0].

33.5.227 PHY I2C Data Read Register 1 (HDMI_PHY_I2CM_DATAI_1_ADDR)

- Address Offset: 0x3024
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 3024h offset = 12_3024h

Bit	7	6	5	4		3	2	1	0
Read	datai[15:8]								
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_PHY_I2CM_DATAI_1_ADDR field descriptions

Field	Description
datai[15:8]	MSB's of data read from the register pointed by address [7:0].

33.5.228 PHY I2C Data Read Register 0 (HDMI_PHY_I2CM_DATAI_0_ADDR)

- Address Offset: 0x3025
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 3025h offset = 12_3025h

Bit	7	6	5	4	3	2	1	0
Read	datai[7:0]							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_PHY_I2CM_DATAI_0_ADDR field descriptions

Field	Description
datai[7:0]	LSB's of data read from the register pointed by address [7:0].

33.5.229 PHY I2C Read/Write Operation (HDMI_PHY_I2CM_OPERATION_ADDR)

This register requests read and write operations from the I2C Master PHY. This register can only be written; reading this register always results in 00h. Writing 1'b1 simultaneously to read and write requests is considered a read request.

- Address Offset: 0x3026
- Size: 8 bits
- Value after Reset: 0x00
- Access: Write

Address: 12_0000h base + 3026h offset = 12_3026h

Bit	7	6	5	4	3	2	1	0
Read	Reserved				Reserved			
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_PHY_I2CM_OPERATION_ADDR field descriptions

Field	Description
7–5 -	This field is reserved. Reserved
4 write	Write operation request
3–1 -	This field is reserved. Reserved
0 read	Read operation request.

**33.5.230 PHY I2C Done Interrupt Register
(HDMI_PHY_I2CM_INT_ADDR)**

This register contains and configures I2C master PHY done interrupt.

- Address Offset: 0x3027
- Size: 8 bits
- Value after Reset: 0x08
- Access: Read/Write

Address: 12_0000h base + 3027h offset = 12_3027h

Bit	7	6	5	4	3	2	1	0
Read					done_pol	done_mask	done_interrupt	done_status
Write					1	0	0	0

HDMI_PHY_I2CM_INT_ADDR field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
3 done_pol	Done interrupt polarity configuration Value after Reset: 1b
2 done_mask	Done interrupt mask signal Value after Reset: 0b
1 done_interrupt	Operation done interrupt bit.{done_interrupt =(done_mask==0b)&& (done_status==done_pol)}. Value after Reset: 0b
0 done_status	Operation done status bit.Marks the end of a rd or write operation. Value after Reset: 0b

33.5.231 PHY I2C Done Interrupt Register (HDMI_PHY_I2CM_CTLINT_ADDR)

This register contains and configures the I2C master PHY error interrupts.

- Address Offset: 0x3028
- Size: 8 bits
- Value after Reset: 0x88
- Access: Read/Write

Address: 12_0000h base + 3028h offset = 12_3028h

Bit	7	6	5	4
Read	nack_pol	nack_mask	nack_interrupt	nack_status
Write				
Reset	1	0	0	0
Bit	3	2	1	0
Read	arbitration_pol	arbitration_mask	arbitration_interrupt	arbitration_status
Write				
Reset	1	0	0	0

HDMI_PHY_I2CM_CTLINT_ADDR field descriptions

Field	Description
7 nack_pol	Not acknowledge error interrupt polarity configuration. Value after Reset: 1b
6 nack_mask	Not acknowledge error interrupt mask signal Value after Reset: 0b
5 nack_interrupt	Not acknowledge error interrupt bit.{nack_interrupt = nack_mask==0b) && (nack_status==nack_pol)}. Value after Reset: 0b
4 nack_status	Not acknowledge error status bit.Error on I2C not acknowledge. Value after Reset: 0b
3 arbitration_pol	Arbitration error interrupt polarity configuration. Value after Reset: 1b
2 arbitration_mask	Arbitration error interrupt mask signal. Value after Reset: 0b
1 arbitration_interrupt	Arbitration error interrupt bit.{arbitration_interrupt = (arbitration_mask==0b)&& (arbitration_status==arbitration_pol)}. Value after Reset: 0b
0 arbitration_status	Arbitration error status bit. Error on master I2C protocol arbitration. Value after Reset: 0b

33.5.232 PHY I2C Speed Control Register (HDMI_PHY_I2CM_DIV_ADDR)

This register sets the I2C Master PHY to work in either Fast or Standard mode.

- Address Offset: 0x3029
- Size: 8 bits
- Value after Reset: 0x0B
- Access: Read/Write

Address: 12_0000h base + 3029h offset = 12_3029h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				fast_mode			
Reset	0	0	0	0	1	0	1	1

HDMI_PHY_I2CM_DIV_ADDR field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
fast_mode	Sets the I2C Master to work in Fast Mode or Standard Mode (x implies that it can take any value) Value after Reset: 1011b 1xxxb Fast Mode 0xxxb Standard Mode

33.5.233 PHY I2C Software Reset Register (HDMI_PHY_I2CM_SOFTRSTZ_ADDR)

This register sets the I2C Master PHY software reset.

- Address Offset: 0x302A
- Size: 8 bits
- Value after Reset: 0x01
- Access: Read/Write

The following *CNT registers must be set before any I2C bus transaction can take place to ensure proper I/O timing.

The following are the I2C Master SCL clock settings:

- SS: Standard Speed

HDMI Memory Map/Register Definition

- FS: Fast Speed
- HCNT: SCL High Level counter
- LCNT: SCL Low Level counter

Address: 12_0000h base + 302Ah offset = 12_302Ah

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	i2c_softrst
Write	0	0	0	0	0	0	0	1

HDMI_PHY_I2CM_SOFRSTZ_ADDR field descriptions

Field	Description
7–1 -	This field is reserved. Reserved
0 i2c_softrst	I2C Master PHY Software Reset. Active by writing a zero and auto cleared to one in the following cycle. Value after Reset: 1b

33.5.234 PHY I2C Slow Speed SCL High Level Control Register 1 (HDMI_PHY_I2CM_SS_SCL_HCNT_1_ADDR)

- Address Offset: 0x302B
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 302Bh offset = 12_302Bh

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	i2cmp_ss_scl_hcnt[15:8]
Write	0	0	0	0	0	0	0	0

HDMI_PHY_I2CM_SS_SCL_HCNT_1_ADDR field descriptions

Field	Description
i2cmp_ss_scl_hcnt[15:8]	Value after Reset: 8'h00

33.5.235 PHY I2C Slow Speed SCL High Level Control Register 0 (HDMI_PHY_I2CM_SS_SCL_HCNT_0_ADDR)

- Address Offset: 0x302C
- Size: 8 bits
- Value after Reset: 0x6C
- Access: Read/Write

Address: 12_0000h base + 302Ch offset = 12_302Ch

Bit	7	6	5	4		3	2	1	0
Read	i2cmp_ss_scl_hcnt[7:0]							Write	
Reset	0	1	1	0		1	1	0	0

HDMI_PHY_I2CM_SS_SCL_HCNT_0_ADDR field descriptions

Field	Description
i2cmp_ss_scl_hcnt[7:0]	Value after Reset: 8'h6C

33.5.236 PHY I2C Slow Speed SCL Low Level Control Register 1 (HDMI_PHY_I2CM_SS_SCL_LCNT_1_ADDR)

- Address Offset: 0x302D
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 302Dh offset = 12_302Dh

Bit	7	6	5	4		3	2	1	0
Read	i2cmp_ss_scl_lcnt[15:8]							Write	
Reset	0	0	0	0		0	0	0	0

HDMI_PHY_I2CM_SS_SCL_LCNT_1_ADDR field descriptions

Field	Description
i2cmp_ss_scl_lcnt[15:8]	Value after Reset: 8'h00

33.5.237 PHY I2C Slow Speed SCL Low Level Control Register 0 (HDMI_PHY_I2CM_SS_SCL_LCNT_0_ADDR)

- Address Offset: 0x302E
- Size: 8 bits
- Value after Reset: 0x7F
- Access: Read/Write

Address: 12_0000h base + 302Eh offset = 12_302Eh

Bit	7	6	5	4		3	2	1	0
Read	i2cmp_ss_scl_lcnt[7:0]							Write	
Reset	0	1	1	1		1	1	1	1

HDMI_PHY_I2CM_SS_SCL_LCNT_0_ADDR field descriptions

Field	Description
i2cmp_ss_scl_lcnt[7:0]	Value after Reset: 8'h7F

33.5.238 PHY I2C Fast Speed SCL High Level Control Register 1 (HDMI_PHY_I2CM_FS_SCL_HCNT_1_ADDR)

- Address Offset: 0x302F
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 302Fh offset = 12_302Fh

Bit	7	6	5	4		3	2	1	0
Read	i2cmp_fs_scl_hcnt[15:8]							Write	
Reset	0	0	0	0		0	0	0	0

HDMI_PHY_I2CM_FS_SCL_HCNT_1_ADDR field descriptions

Field	Description
i2cmp_fs_scl_hcnt[15:8]	Value after Reset: 8'h00

33.5.239 PHY I2C Fast Speed SCL High Level Control Register 0 (HDMI_PHY_I2CM_FS_SCL_HCNT_0_ADDR)

- Address Offset: 0x3030
- Size: 8 bits
- Value after Reset: 0x11
- Access: Read/Write

Address: 12_0000h base + 3030h offset = 12_3030h

Bit	7	6	5	4	3	2	1	0
Read	i2cmp_fs_scl_hcnt[7:0]							
Write	0	0	0	1	0	0	0	1
Reset	i2cmp_fs_scl_hcnt[7:0]							

HDMI_PHY_I2CM_FS_SCL_HCNT_0_ADDR field descriptions

Field	Description
i2cmp_fs_scl_hcnt[7:0]	Value after Reset: 8'h11

33.5.240 PHY I2C Fast Speed SCL Low Level Control Register 1 (HDMI_PHY_I2CM_FS_SCL_LCNT_1_ADDR)

- Address Offset: 0x3031
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3031h offset = 12_3031h

Bit	7	6	5	4	3	2	1	0
Read	i2cmp_fs_scl_lcnt[15:8]							
Write	0	0	0	0	0	0	0	0
Reset	i2cmp_fs_scl_lcnt[15:8]							

HDMI_PHY_I2CM_FS_SCL_LCNT_1_ADDR field descriptions

Field	Description
i2cmp_fs_scl_lcnt[15:8]	Value after Reset: 8'h00

33.5.241 PHY I2C Fast Speed SCL Low Level Control Register 0 (HDMI_PHY_I2CM_FS_SCL_LCNT_0_ADDR)

- Address Offset: 0x3032
- Size: 8 bits
- Value after Reset: 0x24
- Access: Read/Write

Address: 12_0000h base + 3032h offset = 12_3032h

Bit	7	6	5	4		3	2	1	0
Read	i2cmp_fs_scl_lcnt[7:0]								
Write									
Reset	0	0	1	0		0	1	0	0

HDMI_PHY_I2CM_FS_SCL_LCNT_0_ADDR field descriptions

Field	Description
i2cmp_fs_scl_lcnt[7:0]	Value after Reset: 8'h24

33.5.242 Audio Clock Regenerator N Value Register 1 (HDMI_AUD_N1)

For N expected values, refer to the HDMI 1.4a specification.

- Address Offset: 0x3200
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3200h offset = 12_3200h

Bit	7	6	5	4		3	2	1	0
Read	AudN[7:0]								
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_AUD_N1 field descriptions

Field	Description
AudN[7:0]	HDMI Audio Clock Regenerator N value

33.5.243 Audio Clock Regenerator N Value Register 2 (HDMI_AUD_N2)

For N expected values, refer to the HDMI 1.4a specification.

- Address Offset: 0x3201
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3201h offset = 12_3201h

Bit	7	6	5	4	3	2	1	0
Read Write	AudN[15:8]							
Reset	0	0	0	0	0	0	0	0

HDMI_AUD_N2 field descriptions

Field	Description
AudN[15:8]	HDMI Audio Clock Regenerator N value

33.5.244 Audio Clock Regenerator N Value Register 3 (HDMI_AUD_N3)

For N expected values, refer to the HDMI 1.4a specification.

- Address Offset: 0x3202
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3202h offset = 12_3202h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				AudN[19:16]			
Reset	0	0	0	0	0	0	0	0

HDMI_AUD_N3 field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
AudN[19:16]	HDMI Audio Clock Regenerator N value

33.5.245 AUD_CTS1 (HDMI_AUD_CTS1)

For CTS expected values, refer to the HDMI 1.4a specification.

- Address Offset: 0x3203
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3203h offset = 12_3203h

Bit	7	6	5	4		3	2	1	0
Read Write	audCTS[7:0]								
Reset	0	0	0	0		0	0	0	0

HDMI_AUD_CTS1 field descriptions

Field	Description
audCTS[7:0]	HDMI Audio Clock Regenerator CTS calculated value. This value can be manually set using the CTS_manual (AUD_CTS3) mechanism.

33.5.246 AUD_CTS2 (HDMI_AUD_CTS2)

For CTS expected values, refer to the HDMI 1.4a specification.

- Address Offset: 0x3204
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3204h offset = 12_3204h

Bit	7	6	5	4		3	2	1	0
Read Write	audCTS[15:8]								
Reset	0	0	0	0		0	0	0	0

HDMI_AUD_CTS2 field descriptions

Field	Description
audCTS[15:8]	HDMI Audio Clock Regenerator CTS calculated value. This value can be manually set using the CTS_manual (AUD_CTS3) mechanism.

33.5.247 AUD_CTS3 (HDMI_AUD_CTS3)

For CTS expected values, refer to the HDMI 1.4a specification.

- Address Offset: 0x3205
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3205h offset = 12_3205h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				audCTS[19:16]			
Reset	0	0	0	0	0	0	0	0

HDMI_AUD_CTS3 field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
audCTS[19:16]	HDMI Audio Clock Regenerator CTS calculated value. This value can be manually set using the CTS_manual (AUD_CTS3) mechanism.

33.5.248 Audio DMA Start Register (HDMI_AHB_DMA_CONF0)

This register contains the software reset bit for the audio FIFOs. It also configures operating modes of the AHB master.

- Address Offset: 0x3600
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3600h offset = 12_3600h

Bit	7	6	5	4	3	2	1	0
Read Write	sw_fifo_RST	Reserved		hbr	enable_hlock	incr_type[1:0]		burst_mode
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_CONF0 field descriptions

Field	Description
7 sw_fifo_RST	This is the software reset bit for the audio and FIFOs clear. Writing 0'b does not result in any action.

Table continues on the next page...

HDMI_AHB_DMA_CONF0 field descriptions (continued)

Field	Description
	Writing 1'b to this register resets all audio FIFOs. Reading from this register always returns 0'b.
6–5 -	This field is reserved. Reserved
4 hbr	HBR packets enable. The HDMI TX sends the HBR packets. This bit is enabled when the audio frequency is higher than 192 KHz. If this bit is enabled, the number of channels configured in AHB_DMA_CONF1 is always 8.
3 enable_hlock	Enable request of locked burst AHB mechanism. 1 Enables the usage of ohlock for master request to arbiter of a locked complete burst.\n0 Disables request of locked burst AHB mechanism
2–1 incr_type[1:0]	Forced size burst mode. 00 Corresponds to INCR4 fixed four beat incremental AHB burst mode. Only valid when burst_mode is high. 01 Corresponds to INCR8 fixed eight beat incremental AHB burst mode. Only valid when burst_mode is high. 10 Corresponds to INCR16 fixed 16 beat incremental AHB burst mode. Only valid when burst_mode is high. 11 Corresponds to INCR16 fixed 16 beat incremental AHB burst mode. Only valid when burst_mode is high.
0 burst_mode	Burst mode bit 1 Forces the burst mode to be fixed beat incremental burst mode designated by the incr_type[1:0] signal. 0 Normal operation is unspecified length incremental burst. It corresponds to INCR AHB burst mode.

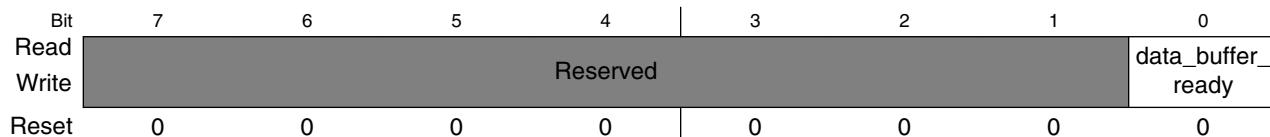
33.5.249 AHB_DMA_START (HDMI_AHB_DMA_START)

The data_buffer_ready bit field signals the AHB audio DMA to start accessing system memory in order to fetch data samples to store in the FIFO. After the operation starts, a new request for a DMA start is ignored until the DMA is stopped or it reaches the end address. Only in one of these situations will a new start request be acknowledged.

The first DMA burst request after data_buffer_ready configuration uses the initial_addr[31:0] as the ohaddr[31:0] and the MBURSTLENGTH[10:0] = AUDIO_FIFO_DEPTH if AUDIO_FIFO_DEPTH < 1024 or MBURSTLENGTH[10:0] = 1024 if AUDIO_FIFO_DEPTH >= 1024.

- Address Offset: 0x3601
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3601h offset = 12_3601h



HDMI_AHB_DMA_START field descriptions

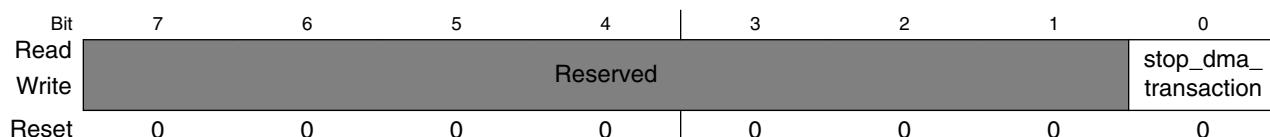
Field	Description
7–1 -	This field is reserved. Reserved
0 data_buffer_ready	Data buffer ready

33.5.250 Audio DMA Stop Register (HDMI_AHB_DMA_STOP)

The stop_dma_transaction bit field signals the AHB audio DMA to stop current memory access. After it stops, if a new start DMA operation is requested, the DMA engine restarts the memory access assuming the initial_addr[31:0] is programmed at AHB_DMA_STRADDR0 to AHB_DMA_STRADDR3.

- Address Offset: 0x3602
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3602h offset = 12_3602h



HDMI_AHB_DMA_STOP field descriptions

Field	Description
7–1 -	This field is reserved. Reserved
0 stop_dma_transaction	Stop DMA transaction

33.5.251 Audio DMA FIFO Threshold Register (HDMI_AHB_DMA_THRSLD)

This register defines the FIFO medium threshold occupation value.

After the AHB master successfully completes a burst transaction, the FIFO may stay remain full until the data fetch interface requests samples. The sample request from the FIFO using the data fetch mechanism drops the number of samples stored in the audio FIFO.

As soon as the number of samples in the FIFO drops lower than the fifo_threshold[7:0], the DMA engine requests a new burst of samples to the AHB master with a size (MBURSTLENGTH[10:0]) equal to AUDIO_FIFO_DEPTH minus fifo_threshold[7:0].

Therefore, the fifo_threshold[7:0] is the medium number of samples that should be available in the audio FIFO across the DMA operation.

- Address Offset: 0x3603
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3603h offset = 12_3603h

Bit	7	6	5	4	3	2	1	0
Read Write	fifo_threshold[7]							
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_THRSLD field descriptions

Field	Description
fifo_threshold[7]	FIFO medium threshold occupation value

33.5.252 Audio DMA Start Address Register 0 (HDMI_AHB_DMA_STRADDR0)

These registers define the initial_addr[31:0] used to initiate the DMA burst read transactions upon data_buffer_ready configuration.

- Address Offset: 0x3604 to 0x3607
- Size: 8 bits per register
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3604h offset = 12_3604h

Bit	7	6	5	4		3	2	1	0
Read					initial_addr[7]				
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_AHB_DMA_STRADDR0 field descriptions

Field	Description
initial_addr[7]	Defines init_addr[7:0] for bits 7-0 to initiate DMA burst transactions

33.5.253 Audio DMA Start Address Register 1 (HDMI_AHB_DMA_STRADDR1)

Address: 12_0000h base + 3605h offset = 12_3605h

Bit	7	6	5	4		3	2	1	0
Read					initial_addr[15]				
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_AHB_DMA_STRADDR1 field descriptions

Field	Description
initial_addr[15]	Defines init_addr[15:8] for bits 7-0 to initiate DMA burst transactions

33.5.254 Audio DMA Start Address Register 2 (HDMI_AHB_DMA_STRADDR2)

Address: 12_0000h base + 3606h offset = 12_3606h

Bit	7	6	5	4		3	2	1	0
Read					initial_addr[23]				
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_AHB_DMA_STRADDR2 field descriptions

Field	Description
initial_addr[23]	Defines init_addr[23:16] for bits 7-0 to initiate DMA burst transactions

33.5.255 Audio DMA Start Address Register 3 (HDMI_AHB_DMA_STRADDR3)

Address: 12_0000h base + 3607h offset = 12_3607h

Bit	7	6	5	4	3	2	1	0
Read								
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_STRADDR3 field descriptions

Field	Description
initial_addr[31]	Defines init_addr[31:24] for bits 7-0 to initiate DMA burst transactions

33.5.256 Audio DMA Stop Address Register 0 (HDMI_AHB_DMA_STPADDR0)

This registers define the final_addr[31:0] used as the final point to the DMA burst read transactions.

Upon data_buffer_ready configuration, the DMA engine starts requesting burst reads from the external system memory. Each burst read can have a maximum theoretical length of 1024 words (due to the AMBA AHB specification restriction). As an example, if the first burst transaction of the AHB audio DMA has a length of 16, then the second burst starts at address ohaddr[31:0] = initial_addr[31:0] + 16 and has a length of MBURSTLENGTH[10:0] = AUDIO_FIFO_DEPTH - fifo_threshold[7:0].

The DMA engine is responsible for incrementing the burst starting address and defining its corresponding burst length to reach the final_addr[31:0] address. The last burst request issued by the DMA engine takes into account that it should only request data until the final_addr[31:0] address (included) and for that should calculate the correct burst length.

After reaching the final_addr[31:0] address, the done interrupt is active to signal completion of DMA operation.

- Address Offset: 0x3608 to 0x360B
- Size: 8 bits per register
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3608h offset = 12_3608h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	final_addr[7]	0	0	0	0
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_AHB_DMA_STPADDR0 field descriptions

Field	Description
final_addr[7]	Defines final_addr[7:0] for bits 7-0 to initiate DMA burst transactions

33.5.257 Audio DMA Stop Address Register 1 (HDMI_AHB_DMA_STPADDR1)

Address: 12_0000h base + 3609h offset = 12_3609h

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	final_addr[15]	0	0	0	0
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_AHB_DMA_STPADDR1 field descriptions

Field	Description
final_addr[15]	Defines final_addr[15:8] for bits 7-0 to initiate DMA burst transactions

33.5.258 Audio DMA Stop Address Register 2 (HDMI_AHB_DMA_STPADDR2)

Address: 12_0000h base + 360Ah offset = 12_360Ah

Bit	7	6	5	4		3	2	1	0
Read	0	0	0	0	final_addr[23]	0	0	0	0
Write	0	0	0	0		0	0	0	0
Reset	0	0	0	0		0	0	0	0

HDMI_AHB_DMA_STPADDR2 field descriptions

Field	Description
final_addr[23]	Defines final_addr[23:16] for bits 7-0 to initiate DMA burst transactions

33.5.259 Audio DMA Stop Address Register 3 (HDMI_AHB_DMA_STPADDR3)

Address: 12_0000h base + 360Bh offset = 12_360Bh

Bit	7	6	5	4	3	2	1	0
Read								
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_STPADDR3 field descriptions

Field	Description
final_addr[31]	Defines final_addr[31:24] for bits 7-0 to initiate DMA burst transactions

33.5.260 Audio DMA Burst Start Address Register 0 (HDMI_AHB_DMA_BSTADDR0)

This read-only register composes the start address of the current burst operation. As an example, if the first burst transaction of the AHB audio DMA as a length of 16, then the second burst should start at address ohaddr[31:0] = initial_addr[31:0] + 16. While this burst is being executed, burst_start_addr[31:0] = haddr[31:0] = initial_addr[31:0] + 16.

- Address Offset: 0x360C to 0x360F
- Size: 8 bits per register
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 360Ch offset = 12_360Ch

Bit	7	6	5	4	3	2	1	0
Read								
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_BSTADDR0 field descriptions

Field	Description
burst_start[7]	Start address for the current burst operation

33.5.261 Audio DMA Burst Start Address Register 1 (HDMI_AHB_DMA_BSTADDR1)

Address: 12_0000h base + 360Dh offset = 12_360Dh

Bit	7	6	5	4	3	2	1	0
Read					burst_start[15]			
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_BSTADDR1 field descriptions

Field	Description
burst_start[15]	Start address for the current burst operation

33.5.262 Audio DMA Burst Start Address Register 2 (HDMI_AHB_DMA_BSTADDR2)

Address: 12_0000h base + 360Eh offset = 12_360Eh

Bit	7	6	5	4	3	2	1	0
Read					burst_start[23]			
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_BSTADDR2 field descriptions

Field	Description
burst_start[23]	Start address for the current burst operation

33.5.263 Audio DMA Burst Start Address Register 3 (HDMI_AHB_DMA_BSTADDR3)

Address: 12_0000h base + 360Fh offset = 12_360Fh

Bit	7	6	5	4	3	2	1	0
Read					burst_start[31]			
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_BSTADDR3 field descriptions

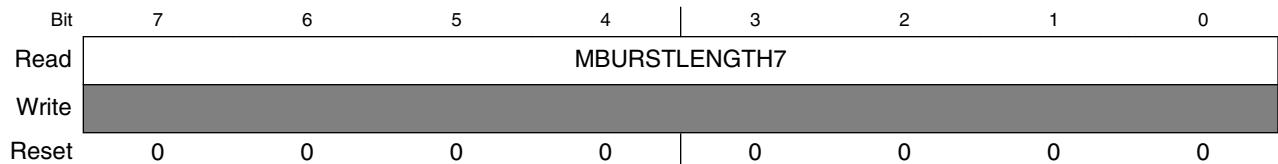
Field	Description
burst_start[31]	Start address for the current burst operation

33.5.264 Audio DMA Burst Length Register 0 (HDMI_AHB_DMA_MBLENGTH0)

These registers hold the length of the current burst operation. As an example, if the first burst transaction of the AHB audio DMA is a length of 8, then the second burst should start at address ohaddr[31:0] = initial_addr[31:0] + 8. It will also have length MBURSTLENGTH[10:0] = AUDIO_FIFO_DEPTH - fifo_threshold[7:0] while this burst is being executed, MBURSTLENGTH[10:0] = AUDIO_FIFO_DEPTH - fifo_threshold[7:0].

- Address Offset: 0x3610 to 0x3611
- Size: 8 bits per register
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 3610h offset = 12_3610h

**HDMI_AHB_DMA_MBLENGTH0 field descriptions**

Field	Description
MBURSTLENGTH7	Requested burst length

33.5.265 Audio DMA Burst Length Register 1 (HDMI_AHB_DMA_MBLENGTH1)

Address: 12_0000h base + 3611h offset = 12_3611h

Bit	7	6		5	4
Read			Reserved		
Write					
Reset	0	0		0	0
Bit	3	2		1	0
Read	Reserved	MBURSTLENGTH10	MBURSTLENGTH9	MBURSTLENGTH8	
Write					
Reset	0	0		0	0

HDMI_AHB_DMA_MBLENGTH1 field descriptions

Field	Description
7–3 -	This field is reserved. Reserved
2 MBURSTLENGTH10	Requested burst length
1 MBURSTLENGTH9	Requested burst length
0 MBURSTLENGTH8	Requested burst length

33.5.266 Audio DMA Interrupt Status Register (HDMI_AHB_DMA_STAT)

This register contains the status bits of the following interrupts:

- Address Offset: 0x3612
- Size: 8 bits per register
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 3612h offset = 12_3612h

Bit	7	6		5	4
Read	statdone	statretrysplit	statlostownership	staterror	
Write					
Reset	0	0		0	0

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Bit	3	2	1	0
Read	Reserved	statthrfifoempty	statfifofull	statfifoempty
Write				
Reset	0	0	0	0

HDMI_AHB_DMA_STAT field descriptions

Field	Description
7 statdone	Status of DMA end of operation interrupt. Active when DMA engine reaches final_addr[15:0] or when stop DMA operation is activated.
6 statretrysplit	Status of retry/split interrupt. Active when AHB master receives a RETRY or SPLIT response from slave.
5 statlostownership	Status of master lost ownership when in burst transfer. Active when AHB master loses BUS ownership within the course of a burst transfer.
4 staterror	Status of error interrupt. Active when slave indicates error through the isresp[1:0].
3 -	This field is reserved. Reserved
2 statthrfifoempty	Status of audio FIFO empty when audio FIFO has less than four samples.
1 statfifofull	Status of audio FIFO full interrupt.
0 statfifoempty	Status of audio FIFO empty interrupt.

33.5.267 Audio DMA Interrupt Register (HDMI_AHB_DMA_INT)

This register contains the interrupt bits of the following interrupts:

- Address Offset: 0x3613
- Size: 8 bits per register
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 3613h offset = 12_3613h

Bit	7	6	5	4
Read	intdone	intretrysplit	intlostownership	interror
Write				
Reset	0	0	0	0
Bit	3	2	1	0
Read	Reserved	intthrfifoempty	intfifofull	intfifoempty
Write				
Reset	0	0	0	0

HDMI_AHB_DMA_INT field descriptions

Field	Description
7 intdone	DMA end of operation interrupt. Active when DMA engine reaches final_addr[15:0] or when stop DMA operation is activated.
6 intretrysplit	Retry/split interrupt. Active when AHB master receives a RETRY or SPLIT response from slave.
5 intlostownership	Master lost ownership interrupt when in burst transfer. Active when AHB master loses BUS ownership within the course of a burst transfer.
4 interror	Error interrupt. Active when slave indicates error through the isresp[1:0].
3 -	This field is reserved. Reserved
2 intthrfifoempty	Audio FIFO empty interrupt when audio FIFO has less than four samples.
1 intfifofull	Audio FIFO full interrupt.
0 intfifoempty	Audio FIFO empty interrupt.

33.5.268 Audio DMA Mask Interrupt Register (HDMI_AHB_DMA_MASK)

Mask for each of the interrupts present in the AHB audio DMA module. For usage information, see [Audio DMA Interrupt Register \(HDMI_AHB_DMA_INT\)](#) ."

- Address Offset: 0x3614
- Size: 8 bits per register
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3614h offset = 12_3614h

Bit	7	6	5	4
Read	done_mask	retrysplit_mask	lostownership_mask	error_mask
Write	0	0	0	0
Reset	0	0	0	0
Bit	3	2	1	0
Read	Reserved	fifo_thrempy_mask	fifo_full_mask	fifo_empty_mask
Write	0	0	0	0
Reset	0	0	0	0

HDMI_AHB_DMA_MASK field descriptions

Field	Description
7 done_mask	DMA end of operation interrupt mask. Active when DMA engine reaches final_addr[15:0] or when stop DMA operation is activated.

Table continues on the next page...

HDMI_AHB_DMA_MASK field descriptions (continued)

Field	Description
6 retrysplit_mask	Retry/split interrupt mask. Active when AHB master receives a RETRY or SPLIT response from slave.
5 lostownership_mask	Master lost ownership interrupt mask when in burst transfer. Active when AHB master loses BUS ownership within the course of a burst transfer.
4 error_mask	Error interrupt mask. Active when slave indicates error through the isresp[1:0].
3 -	This field is reserved. Reserved
2 fifo_thrempty_mask	Audio FIFO empty interrupt mask when audio FIFO has less than four samples.
1 fifo_full_mask	Audio FIFO full interrupt mask.
0 fifo_empty_mask	Audio FIFO empty interrupt mask.

33.5.269 Audio DMA Polarity Interrupt Register (HDMI_AHB_DMA_POL)

Polarity for each of the interrupts present in the AHB audio DMA module. For usage information, see [Audio DMA Interrupt Register \(HDMI_AHB_DMA_INT\)](#) ."

- Address Offset: 0x3615
- Size: 8 bits per register
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3615h offset = 12_3615h

Bit	7	6	5	4
Read Write	done_polarity	retrysplit_polarity	lostownership_polarity	error_polarity
Reset	0	0	0	0
Bit	3	2	1	0
Read	Reserved		fifo_full_polarity	fifo_empty_polarity
Write				
Reset	0	0	0	0

HDMI_AHB_DMA_POL field descriptions

Field	Description
7 done_polarity	DMA end of operation interrupt mask. Active when DMA engine reaches final_addr[15:0] or when stop DMA operation is activated.

Table continues on the next page...

HDMI_AHB_DMA_POL field descriptions (continued)

Field	Description
6 retrysplit_polarity	Retry/split interrupt mask. Active when AHB master receives a RETRY or SPLIT response from slave.
5 lostownership_polarity	Master lost ownership interrupt mask when in burst transfer. Active when AHB master loses BUS ownership within the course of a burst transfer.
4 error_polarity	Error interrupt mask. Active when slave indicates error through the isresp[1:0].
3 -	This field is reserved. Reserved
2 fifo_thrfifoempty_polarity	Audio FIFO empty interrupt mask when audio FIFO has less than four samples.
1 fifo_full_polarity	Audio FIFO full interrupt mask.
0 fifo_empty_polarity	Audio FIFO empty interrupt mask.

33.5.270 Audio DMA Channel Enable Configuration Register 1 (HDMI_AHB_DMA_CONF1)

- Address Offset: 0x3616
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3616h offset = 12_3616h

Bit	7	6	5	4	3	2	1	0
Read Write	CH_IN_EN7	CH_IN_EN6	CH_IN_EN5	CH_IN_EN4	CH_IN_EN3	CH_IN_EN2	CH_IN_EN1	CH_IN_EN0
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_CONF1 field descriptions

Field	Description
7 CH_IN_EN7	Channel 7 enable bit 1 Channel enabled 0 Channel disabled
6 CH_IN_EN6	Channel 6 enable bit 1 Channel enabled 0 Channel disabled

Table continues on the next page...

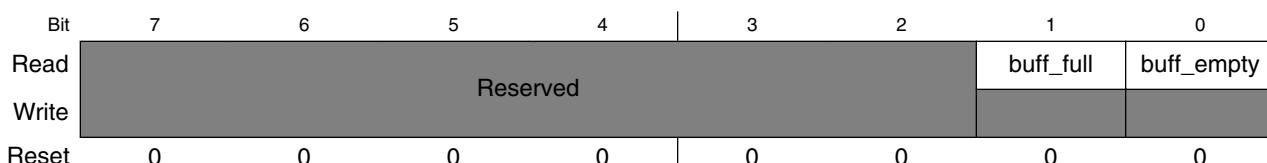
HDMI_AHB_DMA_CONF1 field descriptions (continued)

Field	Description
5 CH_IN_EN5	Channel 5 enable bit 1 Channel enabled 0 Channel disabled
4 CH_IN_EN4	Channel 4 enable bit 1 Channel enabled 0 Channel disabled
3 CH_IN_EN3	Channel 3 enable bit 1 Channel enabled 0 Channel disabled
2 CH_IN_EN2	Channel 2 enable bit 1 Channel enabled 0 Channel disabled
1 CH_IN_EN1	Channel 1 is always enabled.
0 CH_IN_EN0	Channel 0 is always enabled.

33.5.271 Audio DMA Buffer Interrupt Status Register (HDMI_AHB_DMA_BUFFSTAT)

- Address Offset: 0x3617
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 3617h offset = 12_3617h

**HDMI_AHB_DMA_BUFFSTAT field descriptions**

Field	Description
7–2 -	This field is reserved. Reserved
1 buff_full	Buffer full flag status

Table continues on the next page...

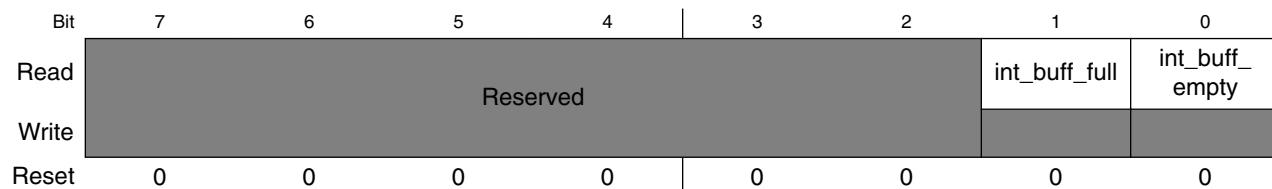
HDMI_AHB_DMA_BUFFSTAT field descriptions (continued)

Field	Description
0 buff_empty	Buffer empty flag status

33.5.272 Audio DMA Buffer Interrupt Register (HDMI_AHB_DMA_BUFFINT)

- Address Offset: 0x3618
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 3618h offset = 12_3618h

**HDMI_AHB_DMA_BUFFINT field descriptions**

Field	Description
7–2 -	This field is reserved. Reserved
1 int_buff_full	Buffer full flag interrupt
0 int_buff_empty	Buffer empty flag interrupt

33.5.273 Audio DMA Buffer Mask Interrupt Register (HDMI_AHB_DMA_BUFFMASK)

- Address Offset: 0x3619
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3619h offset = 12_3619h

Bit	7	6	5	4	3	2	1	0
Read							int_buff_full	int_buff_empty
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_BUFFMASK field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 int_buff_full	Buffer full flag mask
0 int_buff_empty	Buffer empty flag mask

33.5.274 Audio DMA Buffer Polarity Interrupt Register (HDMI_AHB_DMA_BUFFPOL)

- Address Offset: 0x361A
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 361Ah offset = 12_361Ah

Bit	7	6	5	4	3	2	1	0
Read							int_buff_full	int_buff_empty
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_AHB_DMA_BUFFPOL field descriptions

Field	Description
7–2 -	This field is reserved. Reserved
1 int_buff_full	Buffer full flag polarity
0 int_buff_empty	Buffer empty flag polarity

33.5.275 Main Controller Synchronous Clock Domain Disable Register (HDMI_MC_CLKDIS)

Main controller synchronous disable control per clock domain. Upon release of synchronous disable the corresponding sw reset NRZ request signal, to that domain, is toggled asking to the output for a synchronized active low reset to be generated to that domain.

- Address Offset: 0x4001
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4001h offset = 12_4001h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	Reserved	cecclk_disable	cscclk_disable	audclk_disable	prepclk_disable	tmdsclk_disable	pixelclk_disable
Write	0	0	0	0	0	0	0	0

HDMI_MC_CLKDIS field descriptions

Field	Description
7 -	This field is reserved. Reserved
6 hdcpclk_disable	This field is reserved. Reserved
5 cecclk_disable	CEC Engine clock synchronous disable signal.
4 cscclk_disable	Color Space Converter clock synchronous disable signal.
3 audclk_disable	Audio Sampler clock synchronous disable signal.
2 prepclk_disable	Pixel Repetition clock synchronous disable signal.

Table continues on the next page...

HDMI_MC_CLKDIS field descriptions (continued)

Field	Description
1 tmdsclk_disable	TMDS clock synchronous disable signal.
0 pixelclk_disable	Pixel clock synchronous disable signal.

33.5.276 Main Controller Software Reset Register (HDMI_MC_SWRSTZREQ)

Main controller software reset request per clock domain. Writing zero to a bit of this register results in an NRZ signal toggle at sfrclk rate to an output signal that indicates a software reset request. This toggle must be used to generate a synchronized reset to de corresponding domain, with at least 1 clock cycle. Register defaults back to 0xFF.

- Address Offset: 0x4002
- Size: 8 bits
- Value after Reset: 0xFF
- Access: Read/Write

Address: 12_0000h base + 4002h offset = 12_4002h

Bit	7	6	5	4
Read Write	Reserved	cecswrst_req	Reserved	
Reset	1	1	1	1
Bit	3	2	1	0
Read Write	Reserved	prepswrst_req	tmdsswrst_req	pixelswrst_req
Reset	1	1	1	1

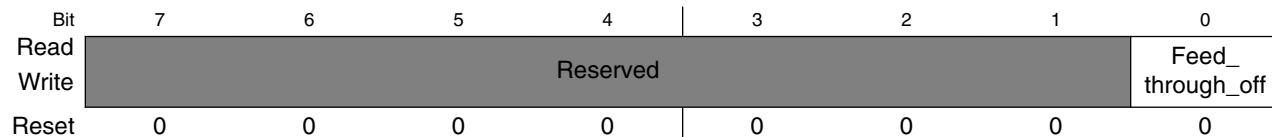
HDMI_MC_SWRSTZREQ field descriptions

Field	Description
7 -	This field is reserved. Reserved
6 cecswrst_req	CEC software reset request. Defaults back to 1b after reset request.
5–3 -	This field is reserved. Reserved
2 prepswrst_req	Pixel Repetition clock synchronous disable signal.
1 tmdsswrst_req	TMDS software reset request. Defaults back to 1b after reset request.
0 pixelswrst_req	Pixel software reset request. Defaults back to 1b after reset request.

33.5.277 Main Controller Feed Through Control Register (HDMI_MC_FLOWCTRL)

- Address Offset: 0x4004
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4004h offset = 12_4004h



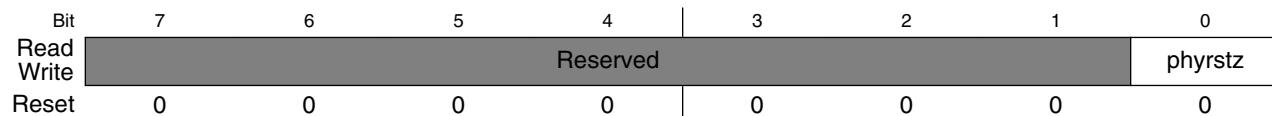
HDMI_MC_FLOWCTRL field descriptions

Field	Description
7–1 -	This field is reserved. Reserved
0 Feed_through_off	Video path Feed Through enable bit: 1 Color Space Converter is in the video data path. 0 Color Space Converter is bypassed (not in the video data path).

33.5.278 Main Controller PHY Reset Register (HDMI_MC_PHYRSTZ)

- Address Offset: 0x4005
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4005h offset = 12_4005h



HDMI_MC_PHYRSTZ field descriptions

Field	Description
7–1 -	This field is reserved. Reserved
0 phyrstz	HDMI Source PHY active low reset control.

33.5.279 Main Controller Clock Present Register (HDMI_MC_LOCKONCLOCK)

- Address Offset: 0x4006
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Clear on Write

Address: 12_0000h base + 4006h offset = 12_4006h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	pclk	tclkclk	prepclk	Reserved			cecclk
Write	w1c	w1c	w1c		Reserved			w1c
Reset	0	0	0	0	0	0	0	0

HDMI_MC_LOCKONCLOCK field descriptions

Field	Description
7 -	This field is reserved. Reserved.
6 pclk	Pixel clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position.
5 tclkclk	TMDS clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position
4 prepclk	Pixel repetition clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position.
3–1 -	This field is reserved. Reserved.
0 cecclk	CEC clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position.

33.5.280 Main Controller HEAC PHY Reset Register (HDMI_MC_HEACPHY_RST)

- Address Offset: 0x4007
- Size: 8 bits
- Value after Reset: N/A
- Access: Read/Write

Address: 12_0000h base + 4007h offset = 12_4007h

Bit	7	6	5	4	3	2	1	0	
Read Write	Reserved							heacphyrst	
Reset	0	0	0	0	0	0	0	0	

HDMI_MC_HEACPHY_RST field descriptions

Field	Description
7–1 -	This field is reserved. Reserved
0 heacphyrst	HEAC PHY reset (active high)

33.5.281 Color Space Converter Interpolation and Decimation Configuration Register (HDMI_CSC_CFG)

Color Space Conversion configuration register. Configures YCC422 to YCC444 interpolation mode and YCC444 to YCC422 decimation mode.

- Address Offset: 0x4100
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4100h offset = 12_4100h

Bit	7	6	5	4	3	2	1	0	
Read Write	Reserved		INTMODE		Reserved		DECMODE		
Reset	0	0	0	0	0	0	0	0	

HDMI_CSC_CFG field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5–4 INTMODE	Chroma interpolation configuration: 00 interpolation disabled 01 $H_u(z) = 1 + z^{-1}$ 10 $H_u(z) = 1/2 + Z^{-1} + 1/2 Z^{-2}$ 11 interpolation disabled.
3–2 -	This field is reserved. Reserved
DEC MODE	Chroma decimation configuration: DECMODE[1:0] Chroma decimation 00 decimation disabled 01 $H_d(z) = 1$ 10 $H_d(z) = 1/4 + 1/2z^{-1} + 1/4z^{-2}$ $11 H_d(z) \times 2^{11} = -5 + 12z^{-2} + 22z^{-4} + 39z^{-8} + 109z^{-10} - 204z^{-12} + 648z^{-14} + 1024z^{-15} + 648z^{-16} - 204z^{-18} + 109z^{-20} - 65z^{-22} + 39z^{-24} - 22z^{-26} + 12z^{-28} - 5z^{-30}$

33.5.282 Color Space Converter Scale and Deep Color Configuration Register (HDMI_CSC_SCALE)

- Address Offset: 0x4101
- Size: 8 bits
- Value after Reset: 0x01
- Access: Read/Write

$$\begin{bmatrix} G \\ R \\ B \end{bmatrix} = 2^{\text{csc scale} - 12} \times \begin{bmatrix} A_1 & A_2 & A_3 \\ B_1 & B_2 & B_3 \\ C_1 & C_2 & C_3 \end{bmatrix} + 2^{\text{csc scale}} \times \begin{bmatrix} A_4 \\ B_4 \\ C_4 \end{bmatrix}$$

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = 2^{\text{cscscale} - 12} \times \begin{bmatrix} A_1 & A_2 & A_3 \\ B_1 & B_2 & B_3 \\ C_1 & C_2 & C_3 \end{bmatrix} + 2^{\text{cscscale}} \times \begin{bmatrix} A_4 \\ B_4 \\ C_4 \end{bmatrix}$$

Figure 33-299. CSC Conversion Functions

Address: 12_0000h base + 4101h offset = 12_4101h

Bit	7	6	5	4	3	2	1	0
Read	csc_colorde_pth[3:0]				Reserved		-	
Write	0	0	0	0	0	0	0	1
Reset								

HDMI_CSC_SCALE field descriptions

Field	Description
7–4 csc_colorde_pth[3:0]	Color space converter color depth configuration: Other: Reserved. 0000 24 bit per pixel video (8 bit per component). 0100 24 bit per pixel video (8 bit per component). 0101 30 bit per pixel video (10 bit per component). 0110 36 bit per pixel video (12 bit per component). 0111 48 bit per pixel video (16 bit per component).
3–2 -	This field is reserved. Reserved
-	Defines the cscscale[1:0] scale factor to apply to all coefficients in Color Space Conversion. This scale factor is expressed in the number of left shifts to apply to each of the coefficients, ranging from 0 to 2.

33.5.283 CSC_COEF_A1_MSB (HDMI_CSC_COEF_A1_MSB)

Color Space Conversion A1 coefficient.

- Address Offset: 0x4102
- Size: 8 bits
- Value after Reset: 0x20
- Access: Read/Write

Address: 12_0000h base + 4102h offset = 12_4102h

Bit	7	6	5	4	3	2	1	0
Read	CSC_COEF_A1_MSB							
Write	0	0	1	0	0	0	0	0
Reset								

HDMI_CSC_COEF_A1_MSB field descriptions

Field	Description
CSC_COEF_A1_MSB	Color Space Conversion A1 MSB coefficient.

33.5.284 CSC_COEF_A1_LSB (HDMI_CSC_COEF_A1_LSB)

Color Space Conversion A1 coefficient.

HDMI Memory Map/Register Definition

- Address Offset: 0x4103
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4103h offset = 12_4103h

Bit	7	6	5	4	3	2	1	0
Read					CSC_COEF_A1_LSB			
Write								

HDMI_CSC_COEF_A1_LSB field descriptions

Field	Description
CSC_COEF_A1_LSB	Color Space Conversion A1 LSB coefficient

33.5.285 CSC_COEF_A2_MSB (HDMI_CSC_COEF_A2_MSB)

Color Space Conversion A2 coefficient.

- Address Offset: 0x4104
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4104h offset = 12_4104h

Bit	7	6	5	4	3	2	1	0
Read					CSC_COEF_A2_MSB			
Write								

HDMI_CSC_COEF_A2_MSB field descriptions

Field	Description
CSC_COEF_A2_MSB	Color Space Conversion A2 MSB coefficient.

33.5.286 CSC_COEF_A2_LSB (HDMI_CSC_COEF_A2_LSB)

Color Space Conversion A2 coefficient.

- Address Offset: 0x4105
- Size: 8 bits

- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4105h offset = 12_4105h

Bit	7	6	5	4	3	2	1	0
Read				CSC_COEF_A2_LSB				
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_CSC_COEF_A2_LSB field descriptions

Field	Description
CSC_COEF_A2_LSB	Color Space Conversion A2 LSB coefficient.

33.5.287 CSC_COEF_A3_MSB (HDMI_CSC_COEF_A3_MSB)

Color Space Conversion A3 coefficient.

- Address Offset: 0x4106
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4106h offset = 12_4106h

Bit	7	6	5	4	3	2	1	0
Read				CSC_COEF_A3_MSB				
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_CSC_COEF_A3_MSB field descriptions

Field	Description
CSC_COEF_A3_MSB	Color Space Conversion A3 MSB coefficient.

33.5.288 CSC_COEF_A3_LSB (HDMI_CSC_COEF_A3_LSB)

Color Space Conversion A3 coefficient.

- Address Offset: 0x4107
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

Address: 12_0000h base + 4107h offset = 12_4107h

Bit	7	6	5	4	3	2	1	0
Read					CSC_COEF_A3_LSB			
Write								

Reset

HDMI_CSC_COEF_A3_LSB field descriptions

Field	Description
CSC_COEF_A3_LSB	Color Space Conversion A3 LSB coefficient.

33.5.289 CSC_COEF_A4_MSB (HDMI_CSC_COEF_A4_MSB)

Color Space Conversion A4 coefficient.

- Address Offset: 0x4108
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4108h offset = 12_4108h

Bit	7	6	5	4	3	2	1	0
Read					CSC_COEF_A4_MSB			
Write								

Reset

HDMI_CSC_COEF_A4_MSB field descriptions

Field	Description
CSC_COEF_A4_MSB	Color Space Conversion A4 MSB coefficient.

33.5.290 CSC_COEF_A4_LSB (HDMI_CSC_COEF_A4_LSB)

Color Space Conversion A4 coefficient.

- Address Offset: 0x4109
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4109h offset = 12_4109h

Bit	7	6	5	4		3	2	1	0
Read Write	CSC_COEF_A4_LSB								
Reset	0	0	0	0		0	0	0	0

HDMI_CSC_COEF_A4_LSB field descriptions

Field	Description
CSC_COEF_A4_LSB	Color Space Conversion A4 LSB coefficient.

33.5.291 CSC_COEF_B1_MSB (HDMI_CSC_COEF_B1_MSB)

Color Space Conversion B1 coefficient.

- Address Offset: 0x410A
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 410Ah offset = 12_410Ah

Bit	7	6	5	4		3	2	1	0
Read Write	CSC_COEF_B1_MSB								
Reset	0	0	0	0		0	0	0	0

HDMI_CSC_COEF_B1_MSB field descriptions

Field	Description
CSC_COEF_B1_MSB	Color Space Conversion B1 MSB coefficient.

33.5.292 CSC_COEF_B1_LSB (HDMI_CSC_COEF_B1_LSB)

Color Space Conversion B1 coefficient.

- Address Offset: 0x410B
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

Address: 12_0000h base + 410Bh offset = 12_410Bh

Bit	7	6	5	4	3	2	1	0
Read				CSC_COEF_B1_LSB				
Reset	0	0	0	0	0	0	0	0

HDMI_CSC_COEF_B1_LSB field descriptions

Field	Description
CSC_COEF_B1_LSB	Color Space Conversion B1 LSB coefficient.

33.5.293 CSC_COEF_B2_MSB (HDMI_CSC_COEF_B2_MSB)

Color Space Conversion B2 coefficient.

- Address Offset: 0x410C
- Size: 8 bits
- Value after Reset: 0x20
- Access: Read/Write

Address: 12_0000h base + 410Ch offset = 12_410Ch

Bit	7	6	5	4	3	2	1	0
Read				CSC_COEF_B2_MSB				
Reset	0	0	1	0	0	0	0	0

HDMI_CSC_COEF_B2_MSB field descriptions

Field	Description
CSC_COEF_B2_MSB	Color Space Conversion B2 MSB coefficient.

33.5.294 CSC_COEF_B2_LSB (HDMI_CSC_COEF_B2_LSB)

Color Space Conversion B2 coefficient.

- Address Offset: 0x410D
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 410Dh offset = 12_410Dh

Bit	7	6	5	4		3	2	1	0
Read					CSC_COEF_B2_LSB				
Write									

Reset 0 0 0 0 | 0 0 0 0 0

HDMI_CSC_COEF_B2_LSB field descriptions

Field	Description
CSC_COEF_B2_LSB	Color Space Conversion B2 LSB coefficient.

33.5.295 CSC_COEF_B3_MSB (HDMI_CSC_COEF_B3_MSB)

Color Space Conversion B3 coefficient.

- Address Offset: 0x410E
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 410Eh offset = 12_410Eh

Bit	7	6	5	4		3	2	1	0
Read					CSC_COEF_B3_MSB				
Write									

Reset 0 0 0 0 | 0 0 0 0 0

HDMI_CSC_COEF_B3_MSB field descriptions

Field	Description
CSC_COEF_B3_MSB	Color Space Conversion B3 MSB coefficient.

33.5.296 CSC_COEF_B3_LSB (HDMI_CSC_COEF_B3_LSB)

Color Space Conversion B3 coefficient.

- Address Offset: 0x410F
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

Address: 12_0000h base + 410Fh offset = 12_410Fh

Bit	7	6	5	4	3	2	1	0
Read					CSC_COEF_B3_LSB			
Write								

Reset

HDMI_CSC_COEF_B3_LSB field descriptions

Field	Description
CSC_COEF_B3_LSB	Color Space Conversion B3 LSB coefficient.

33.5.297 CSC_COEF_B4_MSB (HDMI_CSC_COEF_B4_MSB)

Color Space Conversion B4 coefficient.

- Address Offset: 0x4110
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4110h offset = 12_4110h

Bit	7	6	5	4	3	2	1	0
Read					CSC_COEF_B4_MSB			
Write								

Reset

HDMI_CSC_COEF_B4_MSB field descriptions

Field	Description
CSC_COEF_B4_MSB	Color Space Conversion B4 MSB coefficient.

33.5.298 CSC_COEF_B4_LSB (HDMI_CSC_COEF_B4_LSB)

Color Space Conversion B4 coefficient.

- Address Offset: 0x4111
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4111h offset = 12_4111h

Bit	7	6	5	4		3	2	1	0
Read					CSC_COEF_B4_LSB				
Write									

Reset 0 0 0 0 | 0 0 0 0 0

HDMI_CSC_COEF_B4_LSB field descriptions

Field	Description
CSC_COEF_B4_LSB	Color Space Conversion B4 LSB coefficient.

33.5.299 CSC_COEF_C1_MSB (HDMI_CSC_COEF_C1_MSB)

Color Space Conversion C1 coefficient.

- Address Offset: 0x4112
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4112h offset = 12_4112h

Bit	7	6	5	4		3	2	1	0
Read					CSC_COEF_C1_MSB				
Write									

Reset 0 0 0 0 | 0 0 0 0 0

HDMI_CSC_COEF_C1_MSB field descriptions

Field	Description
CSC_COEF_C1_MSB	Color Space Conversion C1 MSB coefficient.

33.5.300 CSC_COEF_C1_LSB (HDMI_CSC_COEF_C1_LSB)

Color Space Conversion C1 coefficient.

- Address Offset: 0x4113
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

Address: 12_0000h base + 4113h offset = 12_4113h

Bit	7	6	5	4	3	2	1	0
Read				CSC_COEF_C1_LSB				
Write	0	0	0	0	0	0	0	0

HDMI_CSC_COEF_C1_LSB field descriptions

Field	Description
CSC_COEF_C1_LSB	Color Space Conversion C1 LSB coefficient.

33.5.301 CSC_COEF_C2_MSB (HDMI_CSC_COEF_C2_MSB)

Color Space Conversion C2 coefficient.

- Address Offset: 0x4114
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4114h offset = 12_4114h

Bit	7	6	5	4	3	2	1	0
Read				CSC_COEF_C2_MSB				
Write	0	0	0	0	0	0	0	0

HDMI_CSC_COEF_C2_MSB field descriptions

Field	Description
CSC_COEF_C2_MSB	Color Space Conversion C2 MSB coefficient.

33.5.302 CSC_COEF_C2_LSB (HDMI_CSC_COEF_C2_LSB)

Color Space Conversion C2 coefficient.

- Address Offset: 0x4115
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4115h offset = 12_4115h

Bit	7	6	5	4		3	2	1	0
Read					CSC_COEF_C2_LSB				
Write									

Reset 0 0 0 0 | 0 0 0 0 0

HDMI_CSC_COEF_C2_LSB field descriptions

Field	Description
CSC_COEF_C2_LSB	Color Space Conversion C2 LSB coefficient.

33.5.303 CSC_COEF_C3_MSB (HDMI_CSC_COEF_C3_MSB)

Color Space Conversion C3 coefficient.

- Address Offset: 0x4116
- Size: 8 bits
- Value after Reset: 0x20
- Access: Read/Write

Address: 12_0000h base + 4116h offset = 12_4116h

Bit	7	6	5	4		3	2	1	0
Read					CSC_COEF_C3_MSB				
Write									

Reset 0 0 1 0 | 0 0 0 0 0

HDMI_CSC_COEF_C3_MSB field descriptions

Field	Description
CSC_COEF_C3_MSB	Color Space Conversion C3 MSB coefficient.

33.5.304 CSC_COEF_C3_LSB (HDMI_CSC_COEF_C3_LSB)

Color Space Conversion C3 coefficient.

- Address Offset: 0x4117
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

HDMI Memory Map/Register Definition

Address: 12_0000h base + 4117h offset = 12_4117h

Bit	7	6	5	4	3	2	1	0
Read					CSC_COEF_C3_LSB			
Write								

Reset

HDMI_CSC_COEF_C3_LSB field descriptions

Field	Description
CSC_COEF_C3_LSB	Color Space Conversion C3 LSB coefficient.

33.5.305 CSC_COEFC4_MSB (HDMI_CSC_COEFC4_MSB)

Color Space Conversion C4 coefficient.

- Address Offset: 0x4118
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4118h offset = 12_4118h

Bit	7	6	5	4	3	2	1	0
Read					CSC_COEFC4_MSB			
Write								

Reset

HDMI_CSC_COEFC4_MSB field descriptions

Field	Description
CSC_COEFC4_MSB	Color Space Conversion C4 MSB coefficient.

33.5.306 CSC_COEFC4_LSB (HDMI_CSC_COEFC4_LSB)

Color Space Conversion C4 coefficient.

- Address Offset: 0x4119
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 4119h offset = 12_4119h

Bit	7	6	5	4	3	2	1	0
Read Write					CSC_COEFC4_LSB			
Reset	0	0	0	0	0	0	0	0

HDMI_CSC_COEFC4_LSB field descriptions

Field	Description
CSC_COEFC4_LSB	Color Space Conversion C4 LSB coefficient.

33.5.307 CEC_CTRL (HDMI_CEC_CTRL)

CEC registers control the CEC feature that is implemented in HDMI TX. They perform various functions like controlling, monitoring, and buffering data for the transmitter and the receiver.

This register handles the main control of the CEC initiator.

- Address Offset: 0x7D00
- Size: 8 bits
- Value after Reset: 0x02
- Access: Read/Write

Address: 12_0000h base + 7D00h offset = 12_7D00h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				STANDBY	BC_NACK	FRAME_TYP	SEND
Reset	0	0	0	0	0	0	1	0

HDMI_CEC_CTRL field descriptions

Field	Description
7–5 -	This field is reserved. Reserved
4 STANDBY	Standby bit 0 CEC controller responds the ACK to all messages. 1 CEC controller responds with ACK to all ping messages (only when the EOM is received) and responds with NACK to all other messages, generating wake-up status for selected opcodes. Attention that the NACK will only be posted on the last block of a frame.
3 BC_NACK	Broadcast NACK bit 0 Reset by software to ACK the received broadcast message. 1 Set by software to NACK the received broadcast message. This bit holds till software resets. The broadcasts will be answered with 1'b0. It means the follower reject the message.

Table continues on the next page...

HDMI_CEC_CTRL field descriptions (continued)

Field	Description
2-1 FRAME_TYP	<p>Frame Type bit</p> <p>00 Signal Free Time = 3-bit periods. Previous attempt to send frame is unsuccessful.</p> <p>01 Signal Free Time = 5-bit periods. New initiator wants to send a frame.</p> <p>10 Signal Free Time = 7-bit periods. Present initiator wants to send another frame immediately after its previous frame. (spec CEC 9.1)</p> <p>11 Illegal value. If software write this value, hardware will set the value to the default 2'b01.</p>
0 SEND	<p>Send bit</p> <p>0 Reset to 0 by hardware when the CEC transmission is done (no matter successful or failed). It can also work as an indicator checked by software to see whether the transmission is finished.</p> <p>1 Set by software to trigger CEC sending a frame as an initiator. This bit keeps at 1 while the transmission is going on.</p>

33.5.308 CEC_STAT (HDMI_CEC_STAT)

This register indicates the status of CEC line. All bits are read only. When an event occurs, the corresponding bit will set to 1 for one SFR clock cycle only. Then, the bit automatically resets to 0. No software reset is required. Software can read the "stable" interrupts on IH_CEC_STAT0 register (this register has the same bit arrangement as CEC_STAT register).

- Address Offset: 0x7D01
- Size: 8 bits
- Value after Reset: N/A
- Access: Read

Address: 12_0000h base + 7D01h offset = 12_7D01h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	WAKEUP	ERROR_FOLL	ERROR_INIT	ARB_LOST	NACK	EOM	DONE
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_CEC_STAT field descriptions

Field	Description
7 -	This field is reserved. Reserved
6 WAKEUP	Follower received wake-up command (for follower only).
5 ERROR_FOLL	An error is notified by a follower. Abnormal logic data bit error (for follower).

Table continues on the next page...

HDMI_CEC_STAT field descriptions (continued)

Field	Description
4 ERROR_INIT	An error is detected on cec line (for initiator only).
3 ARB_LOST	The initiator losses the CEC line arbitration to a second initiator. (specification CEC 9).
2 NACK	A frame is not acknowledged in a directly addressed message. Or a frame is negatively acknowledged in a broadcast message (for initiator only).
1 EOM	EOM is detected so that the received data is ready in the receiver data buffer (for follower only).
0 DONE	The current transmission is successful (for initiator only).

33.5.309 CEC_MASK (HDMI_CEC_MASK)

This read/write register masks/unmasks the interrupt events. When the bit is set to 1 (masked), the corresponding event will not trigger an interrupt signal at the system interface. When the bit is reset to 0, the interrupt event is unmasked.

- Address Offset: 0x7D02
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7D02h offset = 12_7D02h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	WAKEUP_MASK	ERROR_FOLL_MASK	ERROR_INIT_MASK	ARB_LOST_MASK	NACK_MASK	EOM_MASK	DONE_MASK
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

HDMI_CEC_MASK field descriptions

Field	Description
7 -	This field is reserved. Reserved
6 WAKEUP_MASK	Follower wake-up signal mask
5 ERROR_FOLL_MASK	An error is notified by a follower. Abnormal logic data bit error (for follower).
4 ERROR_INIT_MASK	An error is detected on cec line (for initiator only).

Table continues on the next page...

HDMI_CEC_MASK field descriptions (continued)

Field	Description
3 ARB_LOST_MASK	The initiator losses the CEC line arbitration to a second initiator. (specification CEC 9).
2 NACK_MASK	A frame is not acknowledged in a directly addressed message. Or a frame is negatively acknowledged in a broadcast message (for initiator only).
1 EOM_MASK	EOM is detected so that the received data is ready in the receiver data buffer (for follower only).
0 DONE_MASK	The current transmission is successful (for initiator only).

33.5.310 CEC_POLARITY (HDMI_CEC_POLARITY)

This register is readable and writable, which controls the polarity of the interrupt status register as well as the polarity of the interrupt signals at system interface.

- Address Offset: 0x7D03
- Size: 8 bits
- Value after Reset: 0x7F
- Access: Read/Write

Address: 12_0000h base + 7D03h offset = 12_7D03h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	WAKEUP_POL	ERROR_FOLL_POL	ERROR_INIT_POL	ARB_LOST_POL	NACK_POL	EOM_POL	DONE_POL
Write	0	1	1	1	1	1	1	1

HDMI_CEC_POLARITY field descriptions

Field	Description
7 -	This field is reserved. Reserved
6 WAKEUP_POL	Follower wakeup signal polarity
5 ERROR_FOLL_POL	CEC line error polarity (for follower only)
4 ERROR_INIT_POL	CEC line error polarity (for initiator only)
3 ARB_LOST_POL	Initiator Arbitration lost signal polarity
2 NACK_POL	Frame NACK signal polarity

Table continues on the next page...

HDMI_CEC_POLARITY field descriptions (continued)

Field	Description
1 EOM_POL	EOM detect signal polarity (follower only)
0 DONE_POL	Current transmission success or not signal polarity

33.5.311 CEC_INT (HDMI_CEC_INT)

This register is read only. Each bit of the register is output at the system interface. The output signals hold the active interrupt state (high or low) for only one SFR clock cycle. Then the hardware resets the bit to an inactive state. Software can read the "stable" interrupts on the IH_CEC_STAT0 register at address 0x0106 (this register has the same bit arrangement as the CEC_STAT register).

The functional formula for the interrupts is:

$$\text{CEC_INT} = (\text{CEC_MASK} == 0b) \&& (\text{CEC_STATUS} == \text{CEC_POLARITY})$$

- Address Offset: 0x7D04
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 7D04h offset = 12_7D04h

Bit	7	6	5	4
Read	Reserved	WAKEUP_INT	ERROR_FOLL_INT	ERROR_INIT_INT
Write				
Reset	0	0	0	0
Bit	3	2	1	0
Read	ARB_LOST_INT	NACK_INT	EOM_INT	DONE_INT
Write				
Reset	0	0	0	0

HDMI_CEC_INT field descriptions

Field	Description
7 -	This field is reserved. Reserved
6 WAKEUP_INT	Follower wakeup signal polarity

Table continues on the next page...

HDMI_CEC_INT field descriptions (continued)

Field	Description
5 ERROR_FOLL_INT	Follower wakeup interrupt
4 ERROR_INIT_INT	CEC line error interrupt (for follower only)
3 ARB_LOST_INT	CEC line error interrupt (for initiator only)
2 NACK_INT	Initiator Arbitration lost interrupt
1 EOM_INT	Frame NACK interrupt
0 DONE_INT	EOM detect interrupt (for follower only)

33.5.312 CEC_ADDR_L (HDMI_CEC_ADDR_L)

CEC_ADDR_L and CEC_ADDR_H registers indicate the logical address(es) allocated to the CEC device. The logical address mappings are shown in [CEC_ADDR_L \(HDMI_CEC_ADDR_L\)](#) and [CEC_ADDR_H \(HDMI_CEC_ADDR_H\)](#). This register is written by software when the logical allocation is finished. Bit value 1 means the corresponding logical address is allocated to this device. Bit value 0 means the corresponding logical address is not allocated to this device.

- Address Offset: 0x7D05
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7D05h offset = 12_7D05h

Bit	7	6	5	4
Read	CEC_ADDR_L7	CEC_ADDR_L6	CEC_ADDR_L5	CEC_ADDR_L4
Write	0	0	0	0
Reset	0	0	0	0
Bit	3	2	1	0
Read	CEC_ADDR_L3	CEC_ADDR_L2	CEC_ADDR_L1	CEC_ADDR_L0
Write	0	0	0	0
Reset	0	0	0	0

HDMI_CEC_ADDR_L field descriptions

Field	Description
7 CEC_ADDR_L7	Logical address 7 - Tuner 3
6 CEC_ADDR_L6	Logical address 6 - Tuner 2
5 CEC_ADDR_L5	Logical address 5 - Audio System
4 CEC_ADDR_L4	Logical address 4 - Playback Device 1
3 CEC_ADDR_L3	Logical address 3 - Tuner 1
2 CEC_ADDR_L2	Logical address 2 - Recording Device 2
1 CEC_ADDR_L1	Logical address 1 - Recording Device 1
0 CEC_ADDR_L0	Logical address 0 - Device TV

33.5.313 CEC_ADDR_H (HDMI_CEC_ADDR_H)

CEC_ADDR_L and CEC_ADDR_H registers indicate the logical address(es) allocated to the CEC device. The logical address mappings are shown in [CEC_ADDR_L \(HDMI_CEC_ADDR_L\)](#) and [CEC_ADDR_H \(HDMI_CEC_ADDR_H\)](#). This register is written by software when the logical allocation is finished. Bit value 1 means the corresponding logical address is allocated to this device. Bit value 0 means the corresponding logical address is not allocated to this device.

- Address Offset: 0x7D06
- Size: 8 bits
- Value after Reset: 0x80
- Access: Read/Write

Address: 12_0000h base + 7D06h offset = 12_7D06h

Bit	7	6	5	4
Read Write	CEC_ADDR_H7	CEC_ADDR_H6	CEC_ADDR_H5	CEC_ADDR_H4
Reset	1	0	0	0
Bit	3	2	1	0
Read Write	CEC_ADDR_H3	CCEC_ADDR_H2	CEC_ADDR_H1	CEC_ADDR_H0
Reset	0	0	0	0

HDMI_CEC_ADDR_H field descriptions

Field	Description
7 CEC_ADDR_H7	Logical address 15 - Unregistered (as initiator address), Broadcast (as destination address)
6 CEC_ADDR_H6	Logical address 14 - Free use
5 CEC_ADDR_H5	Logical address 13 - Reserved
4 CEC_ADDR_H4	Logical address 12 - Reserved
3 CEC_ADDR_H3	Logical address 11 - Playback Device 3
2 CCEC_ADDR_H2	Logical address 10 - Tuner 4
1 CEC_ADDR_H1	Logical address 9 - Playback Device 3
0 CEC_ADDR_H0	Logical address 8 - Playback Device 2

33.5.314 CEC_TX_CNT (HDMI_CEC_TX_CNT)

This register indicates the size of the frame in bytes (including header and data blocks), which are available in the transmitter data buffer.

When the value is zero, the CEC controller ignores the send command triggered by software. When the transmission is done (no matter success or not), the current value is held until it is overwritten by software.

- Address Offset: 0x7D07
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7D07h offset = 12_7D07h

Bit	7	6	5	4		3	2	1	0
Read Write			Reserved				CEC_TX_CNT		
Reset	0	0	0	0		0	0	0	0

HDMI_CEC_TX_CNT field descriptions

Field	Description
7–5 -	This field is reserved. Reserved

Table continues on the next page...

HDMI_CEC_TX_CNT field descriptions (continued)

Field	Description
CEC_TX_CNT	CEC Transmitter Counter register: Value after Reset: 5'b00000 0 No data needs to be transmitted. 1 Frame size is 1 byte. 16 Frame size is 16 byte.

33.5.315 CEC_RX_CNT (HDMI_CEC_RX_CNT)

This register indicates the size of the frame in bytes (including header and data blocks), which are available in the receiver data buffer.

Only after the whole receiving process is finished successfully, the counter is refreshed to the value which indicates the total number of data bytes in the Receiver Data Register.

- Address Offset: 0x7d08
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 7D08h offset = 12_7D08h

**HDMI_CEC_RX_CNT field descriptions**

Field	Description
7–5 -	
CEC_RX_CNT	CEC Receiver Counter register. Value after Reset: 5'b00000 0 No data received 1 1-byte data is received. 16 16-byte data is received.

33.5.316 CEC_TX_DATA (HDMI_CEC_TX_DATA*n*)

These registers (8 bit each) are the buffers used for storing the data waiting for transmission(including header and data blocks).

- Address Offset: 0x7D10 .. 0x7D1F
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 7D10h offset + (1d × i), where i=0d to 15d

Bit	7	6	5	4	3	2	1	0
Read	CEC_TX_DATA							
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_CEC_TX_DATA*n* field descriptions

Field	Description
CEC_TX_DATA	Header block in CEC_TX_DATA0 Data block <i>n</i> in CEC_TX_DATA <i>n</i>

33.5.317 CEC_RX_DATA (HDMI_CEC_RX_DATA*n*)

These registers (8 bit each) are the buffers used for storing the received data (including header and data blocks).

- Address Offset: 0x7D20 .. 0x7D2F
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 7D20h offset + (1d × i), where i=0d to 15d

Bit	7	6	5	4	3	2	1	0
Read	CEC_RX_DATA							
Write								
Reset	0	0	0	0	0	0	0	0

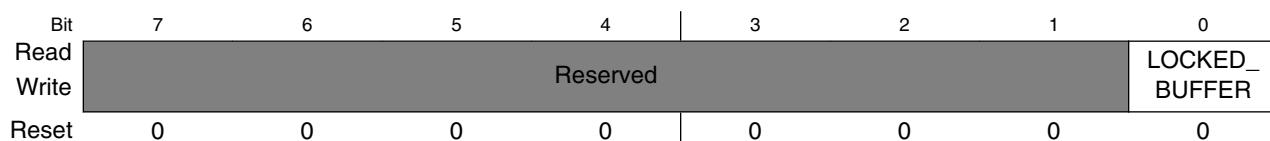
HDMI_CEC_RX_DATA*n* field descriptions

Field	Description
CEC_RX_DATA	Header block in CEC_RX_DATA0 Data block <i>n</i> in CEC_RX_DATA <i>n</i>

33.5.318 CEC_LOCK (HDMI_CEC_LOCK)

- Address Offset: 0x7D30
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7D30h offset = 12_7D30h



HDMI_CEC_LOCK field descriptions

Field	Description
7–1 - Reserved	This field is reserved.
0 LOCKED_BUFFER	When a frame is received, this bit would be active. The CEC controller answers to all the messages with NACK until the CPU writes it to '0'.

33.5.319 CEC_WKUPCTRL (HDMI_CEC_WKUPCTRL)

- Address Offset: 0x7D31
- Size: 8 bits
- Value after Reset: 0xFF
- Access: Read/Write

After receiving a message in the CEC_RX_DATA1 (OPCODE) registers, the CEC engine verifies the message opcode[7:0] against one of the previously defined values to generate the wake-up status:

Wakeupstatus is 1 when:

received opcode is 0x04 and opcode0x04en is 1 or received opcode is 0x0D and opcode0x0Den is 1 or received opcode is 0x41 and opcode0x41en is 1 or received opcode is 0x42 and opcode0x42en is 1 or received opcode is 0x44 and opcode0x44en is 1 or received opcode is 0x70 and opcode0x70en is 1 or received opcode is 0x82 and opcode0x82en is 1 or received opcode is 0x86 and opcode0x86en is 1

Wakeupstatus is 0 when none of the previous conditions are true.

HDMI Memory Map/Register Definition

This formula means that the wake-up status (on CEC_STAT[6] register) is only '1' if the opcode[7:0] received is equal to one of the defined values and the corresponding enable bit of that defined value is set to '1'.

Address: 12_0000h base + 7D31h offset = 12_7D31h

Bit	7	6	5	4
Read	OPCODE0x86en	OPCODE0x82en	OPCODE0x70en	OPCODE0x44en
Write				
Reset	1	1	1	1
Bit	3	2	1	0
Read	OPCODE0x42en	OPCODE0x41en	OPCODE0x0Den	OPCODE0x04en
Write				
Reset	1	1	1	1

HDMI_CEC_WKUPCTRL field descriptions

Field	Description
7 OPCODE0x86en	OPCODE 0x86 wake up enable
6 OPCODE0x82en	OPCODE 0x82 wake up enable
5 OPCODE0x70en	OPCODE 0x70 wake up enable
4 OPCODE0x44en	OPCODE 0x44 wake up enable
3 OPCODE0x42en	OPCODE 0x42 wake up enable
2 OPCODE0x41en	OPCODE 0x41 wake up enable
1 OPCODE0x0Den	OPCODE 0x0D wake up enable
0 OPCODE0x04en	OPCODE 0x04 wake up enable

33.5.320 I2CM_SLAVE (HDMI_I2CM_SLAVE)

I2C Master Registers (E-DDC) registers are responsible for the Master's coordination with the Slave, by coordinating the Slave address, data identification, transaction status, acknowledgement, and reset functions.

- Address Offset: 0x7E00
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7E00h offset = 12_7E00h

Bit	7	6	5	4		3	2	1	0
Read	Reserved					slaveaddr[6:0]			
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_I2CM_SLAVE field descriptions

Field	Description
7 -	This field is reserved. Reserved
slaveaddr[6:0]	Slave address to be sent during read and write normal operations.

33.5.321 I2CM_ADDRESS (HDMI_I2CM_ADDRESS)

- Address Offset: 0x7E01
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7E01h offset = 12_7E01h

Bit	7	6	5	4		3	2	1	0
Read						address[7:0]			
Write									
Reset	0	0	0	0		0	0	0	0

HDMI_I2CM_ADDRESS field descriptions

Field	Description
address[7:0]	Register address for read and write operations.

33.5.322 I2CM_DATAO (HDMI_I2CM_DATAO)

- Address Offset: 0x7E02
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7E02h offset = 12_7E02h

Bit	7	6	5	4		3	2	1	0
Read						datao[7:0]			
Write									
Reset	0	0	0	0		0	0	0	0

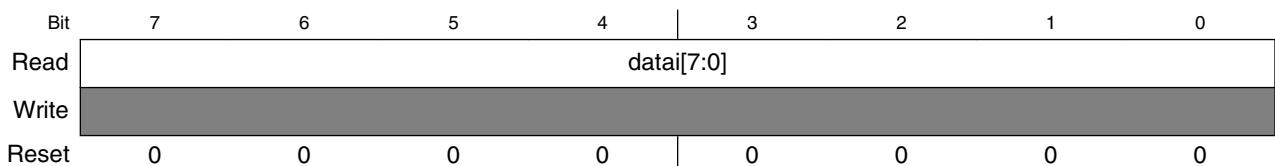
HDMI_I2CM_DATAO field descriptions

Field	Description
datao[7:0]	Data to be written on register pointed by address[7:0].

33.5.323 I2CM_DATAI (HDMI_I2CM_DATAI)

- Address Offset: 0x7E03
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read

Address: 12_0000h base + 7E03h offset = 12_7E03h

**HDMI_I2CM_DATAI field descriptions**

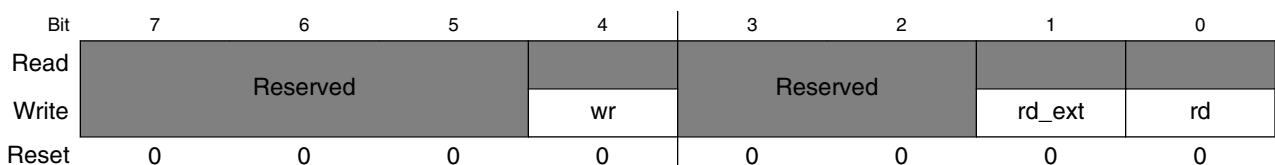
Field	Description
datai[7:0]	Data read from register pointed by address[7:0].

33.5.324 I2CM_OPERATION (HDMI_I2CM_OPERATION)

Read and write operation request. This register can only be written, reading this register will always result in 00h. Writing 1'b1 simultaneously to rd, rd_ext and wr requests is considered as a read (rd) request.

- Address Offset: 0x7E04
- Size: 8 bits
- Value after Reset: 0x00
- Access: Write

Address: 12_0000h base + 7E04h offset = 12_7E04h



HDMI_I2CM_OPERATION field descriptions

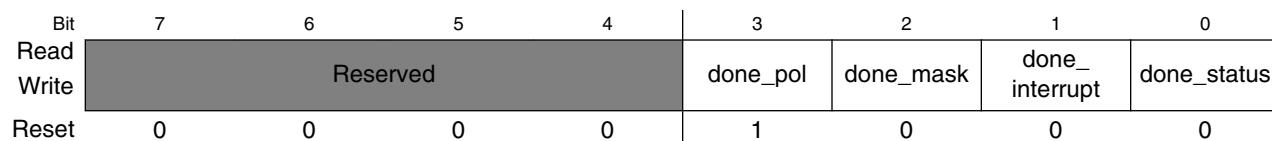
Field	Description
7–5 -	This field is reserved. Reserved
4 wr	Write operation request.
3–2 -	This field is reserved. Reserved
1 rd_ext	After writing 1'b1 to rd_ext bit a extended data read operation is started (E- DDC read operation).
0 rd	Read operation request.

33.5.325 I2CM_INT (HDMI_I2CM_INT)

This register contains and configures I2C master done interrupt.

- Address Offset: 0x7E05
- Size: 8 bits
- Value after Reset: 0x08
- Access: Read/Write

Address: 12_0000h base + 7E05h offset = 12_7E05h

**HDMI_I2CM_INT field descriptions**

Field	Description
7–4 -	This field is reserved. Reserved
3 done_pol	Done interrupt polarity configuration.
2 done_mask	Done interrupt mask signal.
1 done_interrupt	Operation done interrupt bit. Only lasts for 1 SFR clock cycle and is auto cleaned after it. {done_interrupt = (done_mask==0b) && (done_status==done_pol)}.
0 done_status	Operation done status bit. Marks the end of a rd or write operation.

33.5.326 I2CM_CTLINT (HDMI_I2CM_CTLINT)

This register contains and configures I2C master arbitration error and not acknowledge error interrupt.

- Address Offset: 0x7E06
- Size: 8 bits
- Value after Reset: 0x88
- Access: Read/Write

Address: 12_0000h base + 7E06h offset = 12_7E06h

Bit	7	6	5	4
Read Write	nack_pol	nack_mask	nack_interrupt	nack_status
Reset	1	0	0	0
Bit	3	2	1	0
Read Write	arbitration_pol	arbitration_mask	arbitration_interrupt	arbitration_status
Reset	1	0	0	0

HDMI_I2CM_CTLINT field descriptions

Field	Description
7 nack_pol	Not acknowledge error interrupt polarity configuration.
6 nack_mask	Not acknowledge error interrupt mask signal.
5 nack_interrupt	Not acknowledge error interrupt bit. Only lasts for 1 SFR clock cycle and is auto cleaned after it. {nack_interrupt = (nack_mask==0b) && (nack_status==nack_pol)}.
4 nack_status	Not acknowledge error status bit. Error on I2C not acknowledge.
3 arbitration_pol	Arbitration error interrupt polarity configuration.
2 arbitration_mask	Arbitration error interrupt mask signal.
1 arbitration_interrupt	Arbitration error interrupt bit. Only lasts for 1 SFR clock cycle and is auto cleaned after it. {arbitration_interrupt = (arbitration_mask==0b) && (arbitration_status==arbitration_pol)}.
0 arbitration_status	Arbitration error status bit. Error on master I2C protocol arbitration.

33.5.327 I2CM_DIV (HDMI_I2CM_DIV)

This register configures the division relation between master and scl clock.

- Address Offset: 0x7E07
- Size: 8 bits
- Value after Reset: 0x0B
- Access: Read/Write

Address: 12_0000h base + 7E07h offset = 12_7E07h

Bit	7	6	5	4	3	2	1	0
Read					fast_std_mode			
Write								
Reset	0	0	0	0	1	0	1	1

HDMI_I2CM_DIV field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
3 fast_std_mode	Sets the I2C Master to work in Fast Mode or Standard Mode: 1 Fast Mode 0 Standard Mode
-	This field is reserved. Reserved

33.5.328 I2CM_SEGADDR (HDMI_I2CM_SEGADDR)

This register configures the segment address for extended RD/WR destination.

- Address Offset: 0x7E08
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7E08h offset = 12_7E08h

Bit	7	6	5	4	3	2	1	0
Read					SEGADDR			
Write								
Reset	0	0	0	0	0	0	0	0

HDMI_I2CM_SEGADDR field descriptions

Field	Description
7 -	This field is reserved. Reserved
SEGADDR	E-DDC Extended read segment address

33.5.329 I2CM_SOFRSTZ (HDMI_I2CM_SOFRSTZ)

This register resets the I2C master.

- Address Offset: 0x7E09
- Size: 8 bits
- Value after Reset: 0x01
- Access: Read/Write

Address: 12_0000h base + 7E09h offset = 12_7E09h

Bit	7	6	5	4		3	2	1	0
Read Write	Reserved					i2c_softrst			
Reset	0	0	0	0		0	0	0	1

HDMI_I2CM_SOFRSTZ field descriptions

Field	Description
7–1 -	This field is reserved. Reserved
0 i2c_softrst	I2C Master Software Reset. Active by writing a zero and auto cleared to one in the following cycle. Value after Reset: 1b

33.5.330 I2CM_SEGPTR (HDMI_I2CM_SEGPTR)

This register configures the segment pointer for extended RD/WR request.

- Address Offset: 0x7E0A
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

The following *CNT registers must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Address: 12_0000h base + 7E0Ah offset = 12_7E0Ah

Bit	7	6	5	4		3	2	1	0
Read Write	I2CM_SEGPTR								
Reset	0	0	0	0		0	0	0	0

HDMI_I2CM_SEGPTR field descriptions

Field	Description
I2CM_SEGPTR	I2CM_SEGPTR is used for EDID reading operations, particularly for the Extended Data Read Operation (See I²C Master Interface Extended Read Mode ") which is used for Enhanced DDC. This is all described in the VESA Enhanced Display Data Channel Standard v1.1 spec. (addresses A0h/A1h pairs and a segment pointer - 60h).

**33.5.331 I2CM_SS_SCL_HCNT_1_ADDR
(HDMI_I2CM_SS_SCL_HCNT_1_ADDR)**

- Address Offset: 0x7E0B
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7E0Bh offset = 12_7E0Bh

Bit	7	6	5	4	3	2	1	0
Read Write				i2cmp_ss_scl_hcnt[15:8]				
Reset	0	0	0	0	0	0	0	0

HDMI_I2CM_SS_SCL_HCNT_1_ADDR field descriptions

Field	Description
i2cmp_ss_scl_hcnt[15:8]	Value after Reset: 8'h00

**33.5.332 I2CM_SS_SCL_HCNT_0_ADDR
(HDMI_I2CM_SS_SCL_HCNT_0_ADDR)**

- Address Offset: 0x7E0C
- Size: 8 bits
- Value after Reset: 0x6C
- Access: Read/Write

Address: 12_0000h base + 7E0Ch offset = 12_7E0Ch

Bit	7	6	5	4	3	2	1	0
Read Write				i2cmp_ss_scl_hcnt[7:0]				
Reset	0	1	1	0	1	1	0	0

HDMI_I2CM_SS_SCL_HCNT_0_ADDR field descriptions

Field	Description
i2cmp_ss_scl_hcnt[7:0]	Value after Reset: 8'h6C

33.5.333 I2CM_SS_SCL_LCNT_1_ADDR (HDMI_I2CM_SS_SCL_LCNT_1_ADDR)

- Address Offset: 0x7E0D
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7E0Dh offset = 12_7E0Dh

Bit	7	6	5	4	3	2	1	0
Read					i2cmp_ss_scl_lcnt[15:8]			
Write	0	0	0	0	0	0	0	0

HDMI_I2CM_SS_SCL_LCNT_1_ADDR field descriptions

Field	Description
i2cmp_ss_scl_lcnt[15:8]	Value after Reset: 8'h00

33.5.334 I2CM_SS_SCL_LCNT_0_ADDR (HDMI_I2CM_SS_SCL_LCNT_0_ADDR)

- Address Offset: 0x7E0E
- Size: 8 bits
- Value after Reset: 0x7F
- Access: Read/Write

Address: 12_0000h base + 7E0Eh offset = 12_7E0Eh

Bit	7	6	5	4	3	2	1	0
Read					i2cmp_ss_scl_lcnt[7:0]			
Write	0	1	1	1	1	1	1	1

HDMI_I2CM_SS_SCL_LCNT_0_ADDR field descriptions

Field	Description
i2cmp_ss_scl_lcnt[7:0]	Value after Reset: 8'h7F

**33.5.335 I2CM_FS_SCL_HCNT_1_ADDR
(HDMI_I2CM_FS_SCL_HCNT_1_ADDR)**

- Address Offset: 0x7E0F
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7E0Fh offset = 12_7E0Fh

Bit	7	6	5	4	3	2	1	0
Read					i2cmp_fs_scl_hcnt[15:8]			
Write	0	0	0	0	0	0	0	0

HDMI_I2CM_FS_SCL_HCNT_1_ADDR field descriptions

Field	Description
i2cmp_fs_scl_hcnt[15:8]	Value after Reset: 8'h00

**33.5.336 I2CM_FS_SCL_HCNT_0_ADDR
(HDMI_I2CM_FS_SCL_HCNT_0_ADDR)**

- Address Offset: 0x7E10
- Size: 8 bits
- Value after Reset: 0x11
- Access: Read/Write

Address: 12_0000h base + 7E10h offset = 12_7E10h

Bit	7	6	5	4	3	2	1	0
Read					i2cmp_fs_scl_hcnt[7:0]			
Write	0	0	0	1	0	0	0	1

HDMI_I2CM_FS_SCL_HCNT_0_ADDR field descriptions

Field	Description
i2cmp_fs_scl_hcnt[7:0]	Value after Reset: 8'h11

**33.5.337 I2CM_FS_SCL_LCNT_1_ADDR
(HDMI_I2CM_FS_SCL_LCNT_1_ADDR)**

- Address Offset: 0x7E11
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7E11h offset = 12_7E11h

Bit	7	6	5	4	3	2	1	0
Read					i2cmp_fs_scl_lcnt[15:8]			
Write	0	0	0	0	0	0	0	0

HDMI_I2CM_FS_SCL_LCNT_1_ADDR field descriptions

Field	Description
i2cmp_fs_scl_lcnt[15:8]	Value after Reset: 8'h00

**33.5.338 I2CM_FS_SCL_LCNT_0_ADDR
(HDMI_I2CM_FS_SCL_LCNT_0_ADDR)**

- Address Offset: 0x7E12
- Size: 8 bits
- Value after Reset: 0x24
- Access: Read/Write

Address: 12_0000h base + 7E12h offset = 12_7E12h

Bit	7	6	5	4	3	2	1	0
Read					i2cmp_fs_scl_lcnt[7:0]			
Write	0	0	1	0	0	1	0	0

HDMI_I2CM_FS_SCL_LCNT_0_ADDR field descriptions

Field	Description
i2cmp_fs_scl_Lcnt[7:0]	Value after Reset: 8'h24

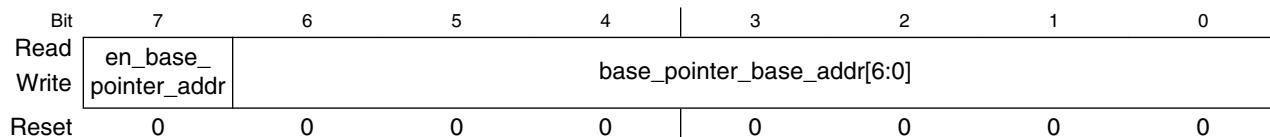
33.5.339 BASE_POINTER_ADDR (HDMI_BASE_POINTER_ADDR)

The I2C Slave Registers allow register memory pagination, and function in the incremental burst operation mode that increases the data throughput when consecutive addressed registers need to be read or write.

The I2C base pointer operation mode is aimed to allow register memory pagination. As long as this operational mode is enabled the value written to this register will be used as the seven most significant bits of the internal Special Function Register address interface (sfraddr[14:8]) for all read or write operations. I2C data transfer protocol used shall be the 7-bit addressed as defined in the section 9 of the I2C-bus Specification, version 2.1.

- Address Offset: 0x7F00
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 7F00h offset = 12_7F00h

**HDMI_BASE_POINTER_ADDR field descriptions**

Field	Description
7 en_base_pointer_addr	Enables the base pointer operation mode.
base_pointer_base_addr[6:0]	Defines the base address for base pointer operation mode. They represent the address bits [14:8]

