

1. Configure the desired settings for the PWM Control Register (PWMx\_PWMCR) while keeping the PWM disabled (PWMx\_PWMCR[0]=0).
2. Enable the desired interrupts in the PWM Interrupt Register (PWMx\_PWMIR).
3. One to three initial samples may be written to the PWM Sample Register (PWMx\_PWMSAR). The initial sample values will be loaded into the PWM FIFO even if the PWM is not yet enabled. Do not write a 4th sample because the FIFO will become full and trigger a FIFO Write Error (FWE). This error will prevent the PWM from starting once it is enabled.
4. Check the FIFO Write Error status bit (FWE), the Compare status bit (CMP) and the Roll-over status bit (ROV) in the PWM Status Register (PWMx\_PWMSR) to make sure they are all zero. Any non-zero status bits should be cleared by writing a 1 to them.
5. Write the desired period to the PWM Period Register (PWMx\_PWMPR).
6. Enable the PWM by writing a 1 to the PWM Enable bit, PWMx\_PWMCR[0], while maintaining the other register bits in their previously configured state.

## 51.6 Disable Sequence for the PWM

The PWM can be disabled at any time by clearing the PWM enable bit, PWMx\_PWMCR[0] to 0.

Any data remaining in the FIFO will not be produced at the PWM output after the PWM has been disabled and will remain in the FIFO until the PWM is enabled again. A software reset (setting PWMx\_PWMCR[3] to 1) or a hardware reset will clear the FIFO and any remaining data will be lost.

## 51.7 PWM Memory Map/Register Definition

The PWM includes six user-accessible 32-bit registers.

**PWM memory map**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
208_0000	PWM Control Register (PWM1_PWMCR)	32	R/W	0000_0000h	<a href="#">51.7.1/4467</a>
208_0004	PWM Status Register (PWM1_PWMSR)	32	w1c	0000_0008h	<a href="#">51.7.2/4469</a>
208_0008	PWM Interrupt Register (PWM1_PWMIR)	32	R/W	0000_0000h	<a href="#">51.7.3/4470</a>

*Table continues on the next page...*

## PWM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
208_000C	PWM Sample Register (PWM1_PWMSAR)	32	R/W	0000_0000h	<a href="#">51.7.4/4471</a>
208_0010	PWM Period Register (PWM1_PWMPR)	32	R/W	0000_FFFEh	<a href="#">51.7.5/4472</a>
208_0014	PWM Counter Register (PWM1_PWMCNR)	32	R	0000_0000h	<a href="#">51.7.6/4473</a>
208_4000	PWM Control Register (PWM2_PWMCR)	32	R/W	0000_0000h	<a href="#">51.7.1/4467</a>
208_4004	PWM Status Register (PWM2_PWMSR)	32	w1c	0000_0008h	<a href="#">51.7.2/4469</a>
208_4008	PWM Interrupt Register (PWM2_PWMIR)	32	R/W	0000_0000h	<a href="#">51.7.3/4470</a>
208_400C	PWM Sample Register (PWM2_PWMSAR)	32	R/W	0000_0000h	<a href="#">51.7.4/4471</a>
208_4010	PWM Period Register (PWM2_PWMPR)	32	R/W	0000_FFFEh	<a href="#">51.7.5/4472</a>
208_4014	PWM Counter Register (PWM2_PWMCNR)	32	R	0000_0000h	<a href="#">51.7.6/4473</a>
208_8000	PWM Control Register (PWM3_PWMCR)	32	R/W	0000_0000h	<a href="#">51.7.1/4467</a>
208_8004	PWM Status Register (PWM3_PWMSR)	32	w1c	0000_0008h	<a href="#">51.7.2/4469</a>
208_8008	PWM Interrupt Register (PWM3_PWMIR)	32	R/W	0000_0000h	<a href="#">51.7.3/4470</a>
208_800C	PWM Sample Register (PWM3_PWMSAR)	32	R/W	0000_0000h	<a href="#">51.7.4/4471</a>
208_8010	PWM Period Register (PWM3_PWMPR)	32	R/W	0000_FFFEh	<a href="#">51.7.5/4472</a>
208_8014	PWM Counter Register (PWM3_PWMCNR)	32	R	0000_0000h	<a href="#">51.7.6/4473</a>
208_C000	PWM Control Register (PWM4_PWMCR)	32	R/W	0000_0000h	<a href="#">51.7.1/4467</a>
208_C004	PWM Status Register (PWM4_PWMSR)	32	w1c	0000_0008h	<a href="#">51.7.2/4469</a>
208_C008	PWM Interrupt Register (PWM4_PWMIR)	32	R/W	0000_0000h	<a href="#">51.7.3/4470</a>
208_C00C	PWM Sample Register (PWM4_PWMSAR)	32	R/W	0000_0000h	<a href="#">51.7.4/4471</a>
208_C010	PWM Period Register (PWM4_PWMPR)	32	R/W	0000_FFFEh	<a href="#">51.7.5/4472</a>
208_C014	PWM Counter Register (PWM4_PWMCNR)	32	R	0000_0000h	<a href="#">51.7.6/4473</a>

### 51.7.1 PWM Control Register (PWMx\_PWMCR)

The PWM control register (PWM\_PWMCR) is used to configure the operating settings of the PWM. It contains the prescaler for the clock division.

Address: Base address + 0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0				FWM	STOPEN	DOZEN	WAITEN	DBGEN	BCTR	HCTR	POUTC	CLKSRC			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PRESCALER												SWR	REPEAT	EN	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PWMx\_PWMCR field descriptions**

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27–26 FWM	FIFO Water Mark. These bits are used to set the data level at which the FIFO empty flag will be set and the corresponding interrupt generated  00 FIFO empty flag is set when there are more than or equal to 1 empty slots in FIFO 01 FIFO empty flag is set when there are more than or equal to 2 empty slots in FIFO 10 FIFO empty flag is set when there are more than or equal to 3 empty slots in FIFO 11 FIFO empty flag is set when there are more than or equal to 4 empty slots in FIFO
25 STOPEN	Stop Mode Enable. This bit keeps the PWM functional while in stop mode. When this bit is cleared, the input clock is gated off in stop mode. This bit is not affected by software reset. It is cleared by hardware reset.  0 Inactive in stop mode 1 Active in stop mode
24 DOZEN	Doze Mode Enable. This bit keeps the PWM functional in doze mode. When this bit is cleared, the input clock is gated off in doze mode. This bit is not affected by software reset. It is cleared by hardware reset.  0 Inactive in doze mode 1 Active in doze mode
23 WAITEN	Wait Mode Enable. This bit keeps the PWM functional in wait mode. When this bit is cleared, the input clock is gated off in wait mode. This bit is not affected by software reset. It is cleared by hardware reset.

*Table continues on the next page...*

**PWMx\_PWMCR field descriptions (continued)**

Field	Description
	0 Inactive in wait mode 1 Active in wait mode
22 DBGEN	Debug Mode Enable. This bit keeps the PWM functional in debug mode. When this bit is cleared, the input clock is gated off in debug mode. This bit is not affected by software reset. It is cleared by hardware reset.  0 Inactive in debug mode 1 Active in debug mode
21 BCTR	Byte Data Swap Control. This bit determines the byte ordering of the 16-bit data when it goes into the FIFO from the sample register.  0 byte ordering remains the same 1 byte ordering is reversed
20 HCTR	Half-word Data Swap Control. This bit determines which half word data from the 32-bit IP Bus interface is written into the lower 16 bits of the sample register.  0 Half word swapping does not take place 1 Half words from write data bus are swapped
19–18 POUTC	PWM Output Configuration. This bit field determines the mode of PWM output on the output pin.  00 Output pin is set at rollover and cleared at comparison 01 Output pin is cleared at rollover and set at comparison 10 PWM output is disconnected 11 PWM output is disconnected
17–16 CLKSRC	Select Clock Source. These bits determine which clock input will be selected for running the counter. After reset the system functional clock is selected. The input clock can also be turned off if these bits are set to 00. This field value should only be changed when the PWM is disabled  00 Clock is off 01 ipg_clk 10 ipg_clk_highfreq 11 ipg_clk_32k
15–4 PRESCALER	Counter Clock Prescaler Value. This bit field determines the value by which the clock will be divided before it goes to the counter.  0x000 Divide by 1 0x001 Divide by 2 0xff Divide by 4096
3 SWR	Software Reset. PWM is reset when this bit is set to 1. It is a self clearing bit. A write 1 to this bit is a single wait state write cycle. When the block is in reset state this bit is set and is cleared when the reset procedure is over. Setting this bit resets all the registers to their reset values except for the STOPEN, DOZEN, WAITEN, and DBGEN bits in this control register.  0 PWM is out of reset 1 PWM is undergoing reset
2–1 REPEAT	Sample Repeat. This bit field determines the number of times each sample from the FIFO is to be used.  00 Use each sample once 01 Use each sample twice 10 Use each sample four times 11 Use each sample eight times

*Table continues on the next page...*

**PWMx\_PWMCR field descriptions (continued)**

Field	Description
0 EN	<p>PWM Enable. This bit enables the PWM. If this bit is not enabled, the clock prescaler and the counter is reset. When the PWM is enabled, it begins a new period, the output pin is set to start a new period while the prescaler and counter are released and counting begins.</p> <p>To make the PWM work with softreset and disable/enable, users can do software reset by setting the SWR bit, wait software reset done, configure the registers, and then enable the PWM by setting this bit to "1"</p> <p>Users can also disable/enable the PWM if PWM would like to be stopped and resumed with same registers configurations .</p> <p>0 PWM disabled 1 PWM enabled</p>

**51.7.2 PWM Status Register (PWMx\_PWMSR)**

The PWM status register (PWM\_PWMSR) contains seven bits which display the state of the FIFO and the occurrence of rollover and compare events. The FIFOAV bit is read-only but the other four bits can be cleared by writing 1 to them. The FE, ROV, and CMP bits are associated with FIFO-Empty, Roll-over, and Compare interrupts, respectively.

Address: Base address + 4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0									FWE	CMP	ROV	FE	FIFOAV		
W										w1c	w1c	w1c	w1c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

**PWMx\_PWMSR field descriptions**

Field	Description
31–7 Reserved	<p>This field is reserved.</p> <p>This read-only field is reserved and always has the value 0.</p>
6 FWE	<p>FIFO Write Error Status. This bit shows that an attempt has been made to write FIFO when it is full.</p> <p>0 FIFO write error not occurred 1 FIFO write error occurred</p>
5 CMP	<p>Compare Status. This bit shows that a compare event has occurred.</p> <p>0 Compare event not occurred 1 Compare event occurred</p>

Table continues on the next page...

**PWMx\_PWMSR field descriptions (continued)**

Field	Description
4 ROV	Roll-over Status. This bit shows that a roll-over event has occurred.  0 Roll-over event not occurred 1 Roll-over event occurred
3 FE	FIFO Empty Status Bit. This bit indicates the FIFO data level in comparison to the water level set by FWM field in the control register.  0 Data level is above water mark 1 When the data level falls below the mark set by FWM field
FIFOAV	FIFO Available. These read-only bits indicate the data level remaining in the FIFO. An attempted write to these bits will not affect their value and no transfer error is generated.  000 No data available 001 1 word of data in FIFO 010 2 words of data in FIFO 011 3 words of data in FIFO 100 4 words of data in FIFO 101 unused 110 unused 111 unused

**51.7.3 PWM Interrupt Register (PWMx\_PWMIR)**

The PWM Interrupt register (PWM\_PWMIR) contains three bits which control the generation of the compare, rollover and FIFO empty interrupts.

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0													CIE	RIE	FIE
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PWMx\_PWMIR field descriptions**

Field	Description
31–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 CIE	Compare Interrupt Enable. This bit controls the generation of the Compare interrupt.

*Table continues on the next page...*

**PWMx\_PWMIR field descriptions (continued)**

Field	Description
	0 Compare Interrupt not enabled 1 Compare Interrupt enabled
1 RIE	Roll-over Interrupt Enable. This bit controls the generation of the Rollover interrupt.  0 Roll-over interrupt not enabled 1 Roll-over Interrupt enabled
0 FIE	FIFO Empty Interrupt Enable. This bit controls the generation of the FIFO Empty interrupt.  0 FIFO Empty interrupt disabled 1 FIFO Empty interrupt enabled

**51.7.4 PWM Sample Register (PWMx\_PWMSAR)**

The PWM sample register (PWM\_PWMSAR) is the input to the FIFO. 16-bit words are loaded into the FIFO. The FIFO can be written at any time, but can be read only when the PWM is enabled. The PWM will run at the last set duty-cycle setting if all the values of the FIFO has been utilized, until the FIFO is reloaded or the PWM is disabled. When a new value is written, the duty cycle changes after the current period is over.

A value of zero in the sample register will result in the PWMO output signal always being low/high (POUTC = 00 it will be low and POUTC = 01 it will be high), and no output waveform will be produced. If the value in this register is higher than the PERIOD + 1, the output will never be set/reset depending on POUTC value.

Address: Base address + Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																SAMPLE															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PWMx\_PWMSAR field descriptions**

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
SAMPLE	Sample Value. This is the input to the 4x16 FIFO. The value in this register denotes the value of the sample being currently used.

### 51.7.5 PWM Period Register (PWMx\_PWMPR)

The PWM period register (PWM\_PWMPR) determines the period of the PWM output signal. After the counter value matches PERIOD + 1, the counter is reset to start another period.

$$PWMO\ (Hz) = PCLK(Hz) / (period + 2)$$

A value of zero in the PWM\_PWMPR will result in a period of two clock cycles for the output signal. Writing 0xFFFF to this register will achieve the same result as writing 0xFFFE.

A change in the period value due to a write in PWM\_PWMPR results in the counter being reset to zero and the start of a new count period.

**NOTE**

Settings PWM\_PWMPR to 0xFFFF when PWMx\_PWMCR REPEAT bits are set to non-zero values is not allowed.

Address: Base address + 10h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																PERIOD															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

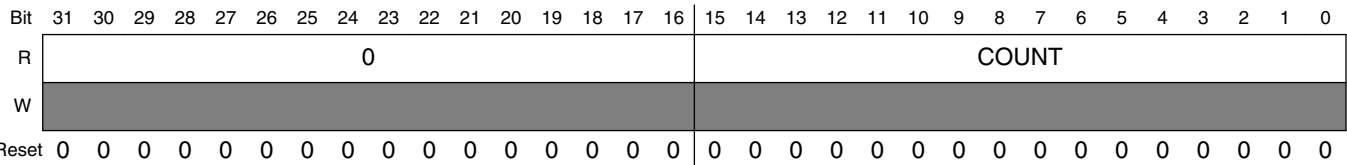
PWMx\_PWMPR field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PERIOD	Period Value. These bits determine the Period of the count cycle. The counter counts up to [Period Value] +1 and is then reset to 0x0000.

### 51.7.6 PWM Counter Register (PWMx\_PWMCNR)

The read-only pulse-width modulator counter register (PWM\_PWMCNR) contains the current count value and can be read at any time without disturbing the counter.

Address: Base address + 14h offset



PWMx\_PWMCNR field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
COUNT	Counter Value. These bits are the counter register value and denotes the current count state the counter register is in.

