PGC_CPU_PDNSCR field descriptions

Field	Description
31–14 Reserved	This read-only field is reserved and always has the value 0.
13–8 ISO2SW	After asserting isolation, the PGC waits a number of 32k clocks equal to the value of ISO2SW before negating . **NOTE:** ISO2SW must not be programmed to zero.
7–6 Reserved	This read-only field is reserved and always has the value 0.
ISO	After a power-down request (pdn_req assertion), the PGC waits a number of 32k clocks equal to the value of ISO before asserting isolation. **NOTE:** ISO must not be programmed to zero.

27.9.8 Power Gating Controller Status Register (PGC_CPU_SR)

The PDNSCR contains the power-down timing parameters.

Address: 20D_C000h base + 2ACh offset = 20D_C2ACh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R								0								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R								0								PSR
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PGC_CPU_SR field descriptions

Field	Description
31–1 Reserved	This read-only field is reserved and always has the value 0.
0 PSR	Power status. When in functional (or software-controlled debug) mode, PGC hardware sets PSR as soon as any of the power control output changes its state to one. Write one to clear this bit. Software should clear this bit after power up; otherwise, PSR continues to reflect the power status of the initial power down. 0 The target subsystem was not powered down for the previous power-down request. 1 The target subsystem was powered down for the previous power-down request.

27.10 DVFSC Memory Map/Register Definition

DVFSC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
20D_C180	DVFS Thresholds (DVFSC_THRS)	32	R/W	0FAF_003Eh	27.10.1/ 1392
20D_C184	DVFS Counters thresholds (DVFSC_COUN)	32	R/W	0007_0020h	27.10.2/ 1393
20D_C188	DVFS general purpose bits weight (DVFSC_SIG1)	32	R/W	0000_0000h	27.10.3/ 1393
20D_C18C	DVFS general purpose bits weight (DVFSC_DVFSSIG0)	32	R/W	0000_0000h	27.10.4/ 1394
20D_C190	DVFS general purpose bit 0 weight counter (DVFSC_DVFSGPC0)	32	R/W	0000_0000h	27.10.5/ 1395
20D_C194	DVFS general purpose bit 1 weight counter (DVFSC_DVFSGPC1)	32	R/W	0000_0000h	27.10.6/ 1397
20D_C198	DVFS general purpose bits enables (DVFSC_DVFSGPBT)	32	R/W	0000_0000h	27.10.7/ 1398
20D_C19C	DVFS EMAC settings (DVFSC_DVFSEMAC)	32	R/W	0000_0004h	27.10.8/ 1400
20D_C1A0	DVFS Control (DVFSC_CNTR)	32	R/W	0900_000Eh	27.10.9/ 1402
20D_C1A4	DVFS Load Tracking Register 0, portion 0 (DVFSC_DVFSLTR0_0)	32	R	0000_0000h	27.10.10/ 1405
20D_C1A8	DVFS Load Tracking Register 0, portion 1 (DVFSC_DVFSLTR0_1)	32	R	0000_0000h	27.10.11/ 1406
20D_C1AC	DVFS Load Tracking Register 1, portion 0 (DVFSC_DVFSLTR1_0)	32	R	0000_0000h	27.10.12/ 1406
20D_C1B0	DVFS Load Tracking Register 3, portion 1 (DVFSC_DVFSLTR1_1)	32	R	0000_0000h	27.10.13/ 1407
20D_C1B4	DVFS pattern 0 length (DVFSC_DVFSPT0)	32	R/W	0000_0010h	27.10.14/ 1408
20D_C1B8	DVFS pattern 1 length (DVFSC_DVFSPT1)	32	R/W	0000_0010h	27.10.15/ 1408
20D_C1BC	DVFS pattern 2 length (DVFSC_DVFSPT2)	32	R/W	0000_0010h	27.10.16/ 1409
20D_C1C0	DVFS pattern 3 length (DVFSC_DVFSPT3)	32	R/W	0000_0010h	27.10.17/ 1410

27.10.1 DVFS Thresholds (DVFSC_THRS)

Address: 20D_C180h base + 0h offset = 20D_C180h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				UPTHR						DWTHR						0										PNCTHR					
W																																
Reset	0	0	0	0	1	1	1	1	1	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0

DVFSC_THRS field descriptions

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–22 UPTHR	Upper threshold for load tracking
21–16 DWTHR	Down threshold for load tracking
15–6 Reserved	This read-only field is reserved and always has the value 0.
PNCTHR	Panic threshold for load tracking

27.10.2 DVFS Counters thresholds (DVFSC_COUN)

Address: 20D_C180h base + 4h offset = 20D_C184h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0								DN_CNT								0								UPCNT				
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

DVFSC_COUN field descriptions

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23–16 DN_CNT	Down counter threshold value
15–8 Reserved	This read-only field is reserved and always has the value 0.
UPCNT	UP counter threshold value

27.10.3 DVFS general purpose bits weight (DVFSC_SIG1)

Address: 20D_C180h base + 8h offset = 20D_C188h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	WSW15			WSW14			WSW13			WSW12			WSW11			WSW10			WSW9			WSW8			WSW7			WSW6			0	
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DVFSC_SIG1 field descriptions

Field	Description
31–29 WSW15	General purpose load tracking signal weight dvfs_w_sig[15]
28–26 WSW14	General purpose load tracking signal weight dvfs_w_sig[14]
25–23 WSW13	General purpose load tracking signal weight dvfs_w_sig[13]
22–20 WSW12	General purpose load tracking signal weight dvfs_w_sig[12]
19–17 WSW11	General purpose load tracking signal weight dvfs_w_sig[11]
16–14 WSW10	General purpose load tracking signal weight dvfs_w_sig[10]
13–11 WSW9	General purpose load tracking signal weight dvfs_w_sig[9]
10–8 WSW8	General purpose load tracking signal weight dvfs_w_sig[8]
7–5 WSW7	General purpose load tracking signal weight dvfs_w_sig[7]
4–2 WSW6	General purpose load tracking signal weight dvfs_w_sig[6]
Reserved	This read-only field is reserved and always has the value 0.

27.10.4 DVFS general purpose bits weight (DVFSC_DVFSSIG0)

Address: 20D_C180h base + Ch offset = 20D_C18Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	WSW5			WSW4			WSW3			WSW2			Reserved								WSW1						WSW0					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DVFSC_DVFSSIG0 field descriptions

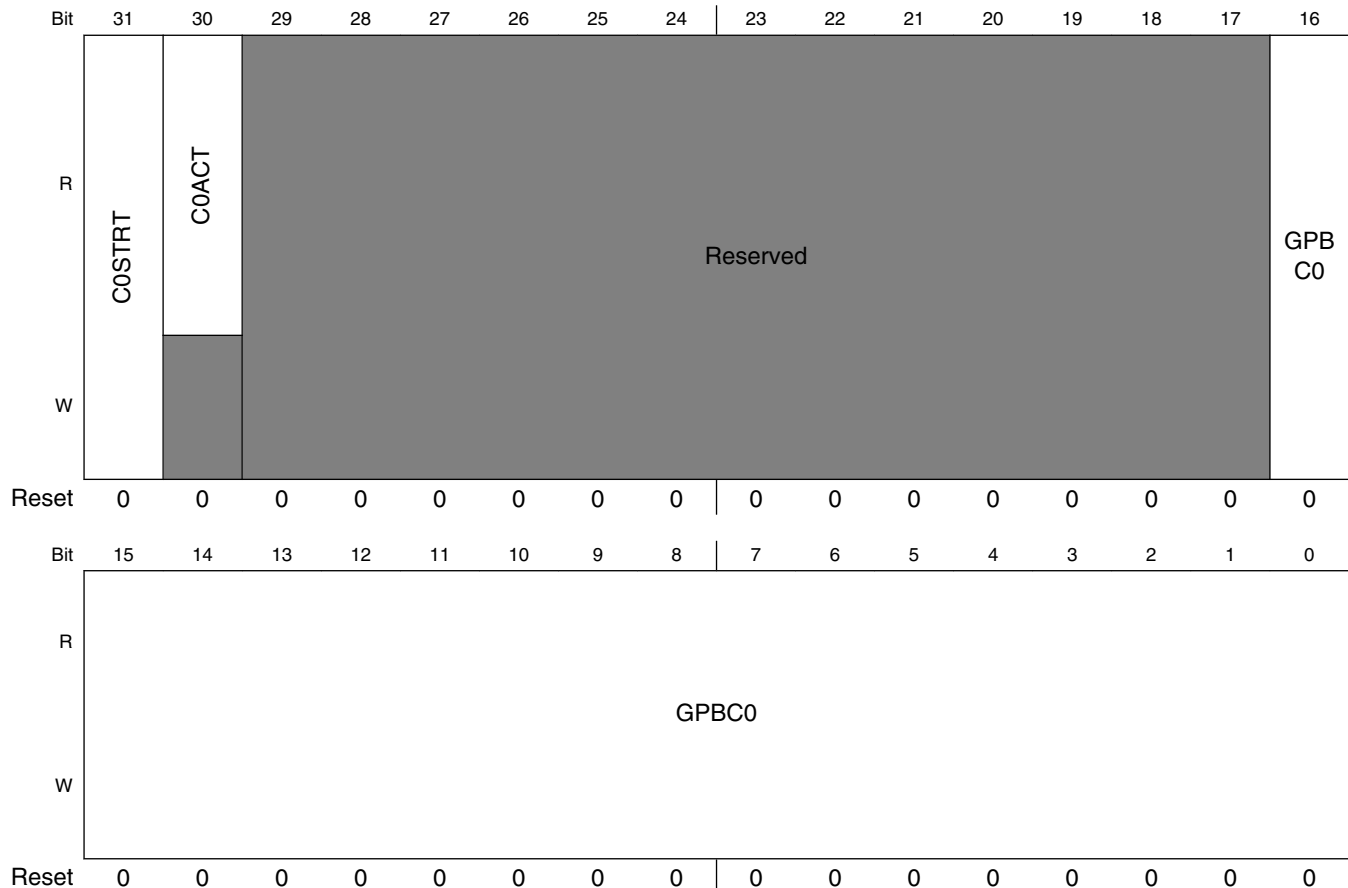| Field	Description
31–29 WSW5	General purpose load tracking signal weight dvfs_w_sig[5]
28–26 WSW4	General purpose load tracking signal weight dvfs_w_sig[4]
25–23 WSW3	General purpose load tracking signal weight dvfs_w_sig[3]
22–20 WSW2	General purpose load tracking signal weight dvfs_w_sig[2]
19–12 -	This field is reserved. Reserved

Table continues on the next page...

DVFSC_DVFSSIG0 field descriptions (continued)

Field	Description
11–6 WSW1	General purpose load tracking signal weight dvfs_w_sig[1]. This value is relevant during GPC1 counting period or when GPB1 is set.
WSW0	General purpose load tracking signal weight dvfs_w_sig[0]. This value is relevant during GPC0 counting period or when GPB0 is set.

27.10.5 DVFS general purpose bit 0 weight counter (DVFSC_DVFSGPC0)

DVFS general purpose bits weight counter.

Address: 20D_C180h base + 10h offset = 20D_C190h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	C0STRT	C0ACT	Reserved													GPB C0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	GPBC0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DVFSC_DVFSGPC0 field descriptions

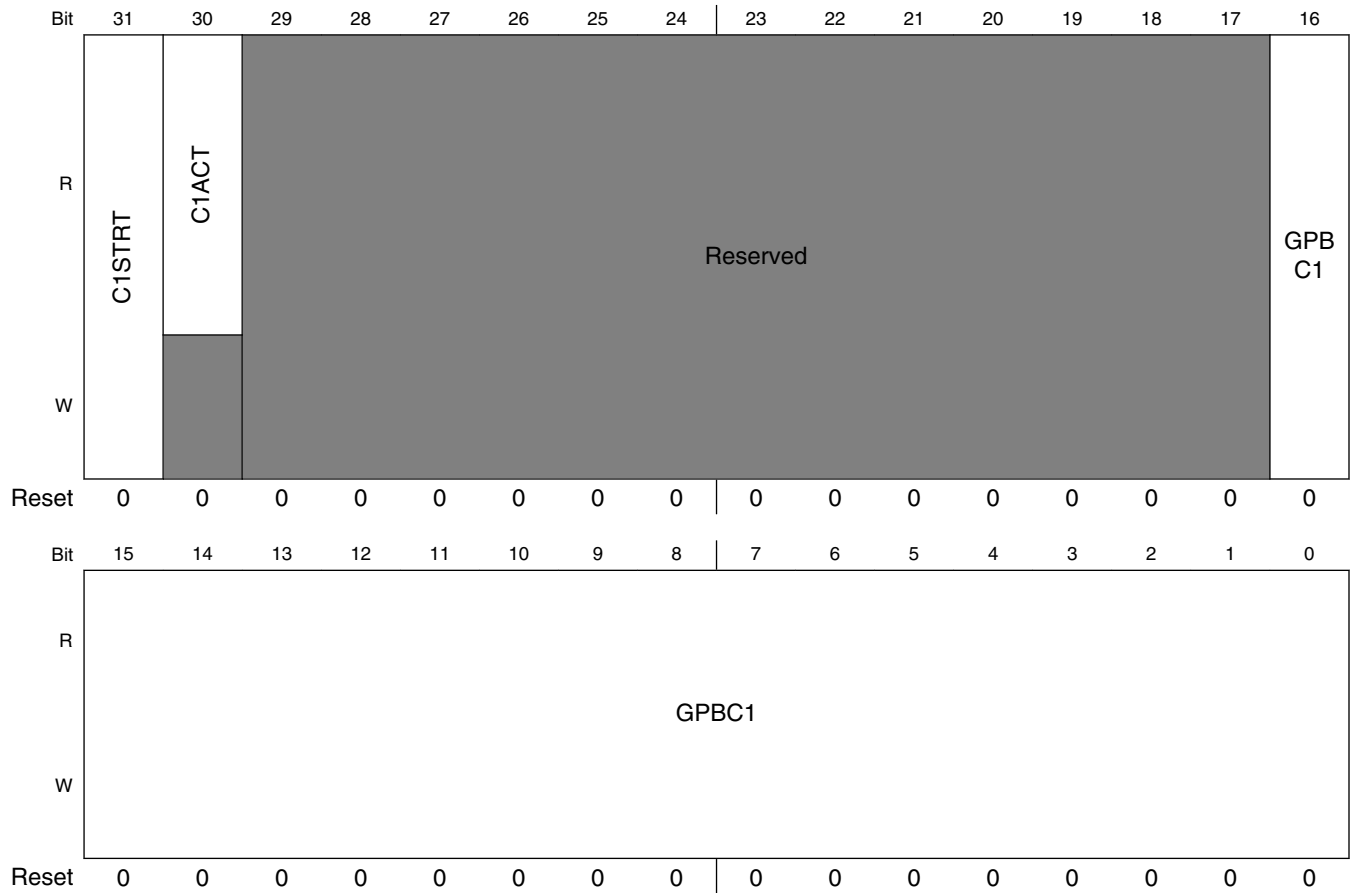| Field	Description
31 C0STRT	C0STRT - Counter 0 start Setting of this bit will initialize down counting of the GPC0 value.

Table continues on the next page...

i.MX 6Dual/6Quad Applications Processor Reference Manual, Rev. 2, 06/2014

DVFSC_DVFSGPC0 field descriptions (continued)

Field	Description
	Bit is self-cleared next cycle after setting.
	Any setting of this bit will re-start GPC0 counter to the GPC0 value.
	GPB0 bit disables (overrides) GPC0 counter - WSW0 weight is applicable continuously
30 C0ACT	C0ACT - Counter 0 active indicator 1 General Purpose bit0 counter didn't reach value of "0" - the WSW0 is provided to DVFS calculation 0 General Purpose bit0 counter reached value of "0" - the instead of WSW0, "0" (zero) is provided to DVFS calculation
29–17 -	This field is reserved. reserved
GPBC0	GPBC0 - General Purpose bits Counter 0 During period of this counter the GeP bit 0 will be set and WSW0 will be added to the calculations.

27.10.6 DVFS general purpose bit 1 weight counter (DVFSC_DVFSGPC1)

DVFS general purpose bits weight counter1.

Address: 20D_C180h base + 14h offset = 20D_C194h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	C1STRT	C1ACT	Reserved													GPB C1
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	GPBC1															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DVFSC_DVFSGPC1 field descriptions

Field	Description
31 C1STRT	C1STRT - Counter 1start Setting of this bit will initialize down counting of the GPC1 value. Bit is self-cleared next cycle after setting. Any setting of this bit will re-start GPC1 counter to the GPC1 value. GPB1 bit disables (overrides) GPC1 counter - WSW1 weight is applicable continuously
30 C1ACT	C1ACT - Counter 1 active indicator

Table continues on the next page...

DVFSC_DVFSGPC1 field descriptions (continued)

Field	Description
	1 General Purpose bit1 counter didn't reach value of "0" - the WSW1 is provided to DVFS calculation 0 General Purpose bit1 counter reached value of "0" - the instead of WSW1, "0" (zero) is provided to DVFS calculation
29–17 -	This field is reserved. reserved
GPBC1	GPBC1 - General Purpose bits Counter 1 During period of this counter the GeP bit 1 will be set and WSW1 will be added to the calculations.

27.10.7 DVFS general purpose bits enables (DVFSC_DVFSGPBT)

Address: 20D_C180h base + 18h offset = 20D_C198h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R								Reserved								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	GPB15	GPB14	GPB13	GPB12	GPB11	GPB10	GPB9	GPB8	GPB7	GPB6	GPB5	GPB4	GPB3	GPB2	GPB1	GPB0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DVFSC_DVFSGPBT field descriptions

Field	Description
31–16 -	This field is reserved. reserved
15 GPB15	General purpose bit 15. Its weight is set by WSW15 value.
14 GPB14	General purpose bit 14. Its weight is set by WSW14 value.
13 GPB13	General purpose bit 13. Its weight is set by WSW13 value.
12 GPB12	General purpose bit 12. Its weight is set by WSW12 value.
11 GPB11	General purpose bit 11. Its weight is set by WSW11 value.
10 GPB10	General purpose bit 10. Its weight is set by WSW10 value.

Table continues on the next page...

DVFSC_DVFSGPBT field descriptions (continued)

Field	Description
9 GPB9	General purpose bit 9. Its weight is set by WSW9 value.
8 GPB8	General purpose bit 8. Its weight is set by WSW8 value.
7 GPB7	General purpose bit 7. Its weight is set by WSW7 value.
6 GPB6	General purpose bit 6. Its weight is set by WSW6 value.
5 GPB5	General purpose bit 5. Its weight is set by WSW5 value.
4 GPB4	General purpose bit 4. Its weight is set by WSW4 value.
3 GPB3	General purpose bit 3. Its weight is set by WSW3 value.
2 GPB2	General purpose bit 2. Its weight is set by WSW2 value.
1 GPB1	General purpose bit 1. Its weight is set by WSW1 value. IF set (1), the GPBC1 operation is disregarded, WSW1 value is applied continuously.
0 GPB0	General purpose bit 0. Its weight is set by WSW0 value. IF set (1), the GPBC0 operation is disregarded, WSW0 value is applied continuously.

27.10.8 DVFS EMAC settings (DVFSC_DVFSEMAC)

Address: 20D_C180h base + 1Ch offset = 20D_C19Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R					WFIM3	WFIM2	WFIM1	WFIM0	FSVAI3[1:0]		FSVAI2[1:0]		FSVAI1[1:0]		FSVAI0[1:0]	
W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved			DVFEN3	DVFEN2	DVFEN1	DVFEN0	EMAC								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

DVFSC_DVFSEMAC field descriptions

Field	Description
31–28 -	This field is reserved. Reserved
27 WFIM3	DVFS Wait for Interrupt of core 3 mask bit 0 Wait for interrupt of core 3 isn't masked 1 Wait for interrupt of core 3 is masked.
26 WFIM2	DVFS Wait for Interrupt of core 2mask bit 0 Wait for interrupt of core 2 isn't masked 1 Wait for interrupt of core 2 is masked.
25 WFIM1	DVFS Wait for Interrupt of core 1 mask bit 0 Wait for interrupt of core 1 isn't masked 1 Wait for interrupt of core 1 is masked.
24 WFIM0	DVFS Wait for Interrupt of core 0 mask bit 0 Wait for interrupt of core 0 isn't masked 1 Wait for interrupt of core 0 is masked.

Table continues on the next page...

i.MX 6Dual/6Quad Applications Processor Reference Manual, Rev. 2, 06/2014

DVFSC_DVFSEMAC field descriptions (continued)

Field	Description
23–22 FSVAI3[1:0]	DVFS Frequency adjustment status of core 3. These status bits indicate that frequency should be changed, following load of core 3. 00 no change 01 frequency should be increased. Low priority source for interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency). 10 frequency should be decreased. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MINF= 1 (lowest frequency). 11 frequency should be increased immediately. High priority source of interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency).
21–20 FSVAI2[1:0]	DVFS Frequency adjustment status of core 2. These status bits indicate that frequency should be changed, following load of core 2. 00 no change 01 frequency should be increased. Low priority source for interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency). 10 frequency should be decreased. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MINF= 1 (lowest frequency). 11 frequency should be increased immediately. High priority source of interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency).
19–18 FSVAI1[1:0]	DVFS Frequency adjustment status of core 1. These status bits indicate that frequency should be changed, following load of core 1. 00 no change 01 frequency should be increased. Low priority source for interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency). 10 frequency should be decreased. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MINF= 1 (lowest frequency). 11 frequency should be increased immediately. High priority source of interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency).
17–16 FSVAI0[1:0]	DVFS Frequency adjustment status of core 0. These status bits indicate that frequency should be changed, following load of core 0. 00 no change 01 frequency should be increased. Low priority source for interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency). 10 frequency should be decreased. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MINF= 1 (lowest frequency). 11 frequency should be increased immediately. High priority source of interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency).
15–13 -	This field is reserved. Reserved
12 DVFEN3	DVFS tracking for core3 enable. 1 DVFS enabled. 0 DVFS disabled.
11 DVFEN2	DVFS tracking for core2 enable. 1 DVFS enabled. 0 DVFS disabled.

Table continues on the next page...

i.MX 6Dual/6Quad Applications Processor Reference Manual, Rev. 2, 06/2014

DVFSC_DVFSEMAC field descriptions (continued)

Field	Description
10 DVFEN1	DVFS tracking for core1 enable. 1 DVFS enabled. 0 DVFS disabled.
9 DVFEN0	DVFS tracking for core0 enable. 1 DVFS enabled. 0 DVFS disabled.
EMAC	EMAC - EMA control value

27.10.9 DVFS Control (DVFSC_CNTR)

Table 27-35.   DIV3CK division

DIV3CK setting	dividing ratio	sum_3 passing bits	div_1_clk cumulative divider
00	1	4-0	1*512=512
001	4	6-2	4*512=2048
010	16	8-4	16*512=8192
011	64	10-6	64*512=32768
100	256	12-8	256*512=131072
101	1024	16-10	1024*512=524288

Table 27-36.   Preliminary Divider definition

DIV_RATIO value	ARM clk division ratio
000000	1
000001	2
000010	3
...	...

Address: 20D_C180h base + 20h offset = 20D_C1A0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DIV3CK			DVFEV	LBMI	LBFL1	LBFL0	DVFIS	PIRQS	FSVAIM	FSVAI[1:0]		0	MAXF	MINF	DIV_RATIO
W																
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DIV_RATIO					0	PFUE	PFUS			LTBRSH	LTBRSR		0		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

DVFSC_CNTR field descriptions

Field	Description
31–29 DIV3CK	DIV3CK - div_3_clk division ratio inside the DVFS module. According to the Table 27-35
28 DVFEV	Always give a DVFS event. 0 Do not give an event always. 1 Always give event.
27 LBMI	Load buffer full mask interrupt. This bit masks the generation of this interrupt. Load buffer full interrupt is masked (LBFL0 and LBFL1 bits still will be updated, but interrupt won't be generated) Load buffer full interrupt is enabled.
26 LBFL1	Load buffer 1 - full status bit. This bit indicates that log buffer registers are full. The bit is set to 1 automatically. An interrupt will be generated if LBMI bit is set to "0" Write '1' to clear. (write '0' leaves bit unchanged) 1 Load buffer0 is full. 0 Load buffer0 is not full.
25 LBFL0	Load buffer 0 - full status bit. This bit indicates that log buffer registers are full. The bit is set to 1 automatically. An interrupt will be generated if LBMI bit is set to "0" Write '1' to clear. (write '0' leaves bit unchanged)

Table continues on the next page...

DVFSC_CNTR field descriptions (continued)

Field	Description
	1 Load buffer1 is full. 0 Load buffer1 is not full.
24 DVFIS	DVFS Interrupt select. These bits define destination of DVFS interrupts. 1 MCU interrupt will be generated for DVFS events. 0 SDMA interrupt will be generated for DVFS events.
23 PIRQS	PIRQS - Pattern IRQ Source * write '1' to clear. Writing '1' will clear interrupt if interrupt was from pattern 1 DVFS IRQ source was from pattern 0 DVFS IRQ source was not from pattern
22 FSVAIM	DVFS Frequency adjustment interrupt mask. This bit masks the DVFS frequency adjustment interrupt. FSVAI status bits will be still asserted in relevant cases. 1 interrupt is masked. 0 interrupt is enabled.
21–20 FSVAI[1:0]	FSVAI DVFS Frequency adjustment interrupt. These status bits indicate that the system frequency should be changed. 00 no interrupt 01 frequency should be increased. Low priority interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency). 10 frequency should be decreased. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MINF= 1 (lowest frequency). 11 frequency should be increased immediately. High priority interrupt. Interrupt is asserted, if FSVAIM=0. Interrupt is masked if MAXF = 1 (highest frequency).
19 Reserved	This read-only field is reserved and always has the value 0.
18 MAXF	Maximum frequency reached. Interrupt will not be created in maximum frequency reached and frequency increase required. 1 max frequency reached 0 max frequency not reached
17 MINF	Minimum frequency reached. Interrupt will not be created in minimum frequency reached and frequency decrease required. 1 min frequency reached 0 min frequency not reached
16–11 DIV_RATIO	DIV_RATIO - Divider value. Divider divides the input ARM clock, following the table Table 27-36
10 Reserved	This read-only field is reserved and always has the value 0.
9 PFUE	PFUE - Period Frequency Update Enable 1 enabled 0 disabled
8–6 PFUS	PFUS - Periodic Frequency Update Status

Table continues on the next page...

DVFSC_CNTR field descriptions (continued)

Field	Description
	000 no update 100 DVFSPT0 period, previous finished(can be performance level decrease) 101 DVFSPT1 period, previous finished(can be EMA-detected performance level) 110 DVFSPT2 period, previous finished(can be performance level increase) 111 DVFSPT3 period, previous finished (can be EMA-detected performance level)
5 LTBRSH	LTBRSH - Load Tracking Buffer Register Shift: 0 values of [5:2] of the selected input are saving in Load Tracking Buffer 1 values of [4:1] of the selected input are saving in Load Tracking Buffer
4–3 LTBRSR	LTBRSR - Load Tracking Buffer Register Source: 00 pre_ld_add 01 ld_add 10 ema_ld 11 reserved
Reserved	This read-only field is reserved and always has the value 0.

27.10.10 DVFS Load Tracking Register 0, portion 0 (DVFSC_DVFSLTR0_0)

Address: 20D_C180h base + 24h offset = 20D_C1A4h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	LTS0_7				LTS0_6				LTS0_5				LTS0_4				LTS0_3				LTS0_2				LTS0_1				LTS0_0			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DVFSC_DVFSLTR0_0 field descriptions

Field	Description
31–28 LTS0_7	core 0 Load Tracking Sample 7
27–24 LTS0_6	core 0 Load Tracking Sample 6
23–20 LTS0_5	core 0 Load Tracking Sample 5
19–16 LTS0_4	core 0 Load Tracking Sample 4
15–12 LTS0_3	core 0 Load Tracking Sample 3
11–8 LTS0_2	core 0 Load Tracking Sample 2
7–4 LTS0_1	core 0 Load Tracking Sample 1
LTS0_0	core 0 Load Tracking Sample 0

27.10.11 DVFS Load Tracking Register 0, portion 1 (DVFSC_DVFSLTR0_1)

Address: 20D_C180h base + 28h offset = 20D_C1A8h

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
R	LTS0_15	LTS0_14	LTS0_13	LTS0_12	LTS0_11	LTS0_10	LTS0_9	LTS0_8
W								
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

DVFSC_DVFSLTR0_1 field descriptions

Field	Description
31–28 LTS0_15	core 0 Load Tracking Sample 15
27–24 LTS0_14	core 0 Load Tracking Sample 14
23–20 LTS0_13	core 0 Load Tracking Sample 13
19–16 LTS0_12	core 0 Load Tracking Sample 12
15–12 LTS0_11	core 0 Load Tracking Sample 11
11–8 LTS0_10	core 0 Load Tracking Sample 10
7–4 LTS0_9	core 0 Load Tracking Sample 9
LTS0_8	core 0 Load Tracking Sample 8

27.10.12 DVFS Load Tracking Register 1, portion 0 (DVFSC_DVFSLTR1_0)

Address: 20D_C180h base + 2Ch offset = 20D_C1ACh

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
R	LTS1_7	LTS1_6	LTS1_5	LTS1_4	LTS1_3	LTS1_2	LTS1_1	LTS1_0
W								
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

DVFSC_DVFSLTR1_0 field descriptions

Field	Description
31–28 LTS1_7	core 0 Load Tracking Sample 7

Table continues on the next page...

DVFSC_DVFSLTR1_0 field descriptions (continued)

Field	Description
27–24 LTS1_6	core 0 Load Tracking Sample 6
23–20 LTS1_5	core 0 Load Tracking Sample 5
19–16 LTS1_4	core 0 Load Tracking Sample 4
15–12 LTS1_3	core 0 Load Tracking Sample 3
11–8 LTS1_2	core 0 Load Tracking Sample 2
7–4 LTS1_1	core 0 Load Tracking Sample 1
LTS1_0	core 0 Load Tracking Sample 0

27.10.13 DVFS Load Tracking Register 3, portion 1 (DVFSC_DVFSLTR1_1)

Address: 20D_C180h base + 30h offset = 20D_C1B0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	LTS1_15				LTS1_14				LTS1_13				LTS1_12				LTS1_11				LTS1_10				LTS1_9				LTS1_8			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DVFSC_DVFSLTR1_1 field descriptions

Field	Description
31–28 LTS1_15	core 0 Load Tracking Sample 15
27–24 LTS1_14	core 0 Load Tracking Sample 14
23–20 LTS1_13	core 0 Load Tracking Sample 13
19–16 LTS1_12	core 0 Load Tracking Sample 12
15–12 LTS1_11	core 0 Load Tracking Sample 11
11–8 LTS1_10	core 0 Load Tracking Sample 10
7–4 LTS1_9	core 0 Load Tracking Sample 9
LTS1_8	core 0 Load Tracking Sample 8

27.10.14   DVFS pattern 0 length (DVFSC_DVFSPT0)

Address: 20D_C180h base + 34h offset = 20D_C1B4h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R															PT0A	FPTN 0
W							Reserved									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W							FPTN0									
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

DVFSC_DVFSPT0 field descriptions

Field	Description
31–18 -	This field is reserved. reserved
17 PT0A	PT0A - Pattern 0 currently active (read-only) 1 active 0 non-active
FPTN0	FPTN0 - Frequency pattern 0 counter During period of this counter the frequency will be reduced from the EMA-detected level.

27.10.15   DVFS pattern 1 length (DVFSC_DVFSPT1)

Address: 20D_C180h base + 38h offset = 20D_C1B8h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R															PT1A	FPTN 1
W							Reserved									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W							FPTN1									
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

DVFSC_DVFSPT1 field descriptions

Field	Description
31–18 -	This field is reserved. reserved
17 PT1A	PT1A - Pattern 1 currently active (read-only) 1 active 0 non-active
FPTN1	FPTN1 - Frequency pattern 1 counter During period of this counter the frequency will be set to the EMA-detected level.

27.10.16 DVFS pattern 2 length (DVFSC_DVFSPT2)

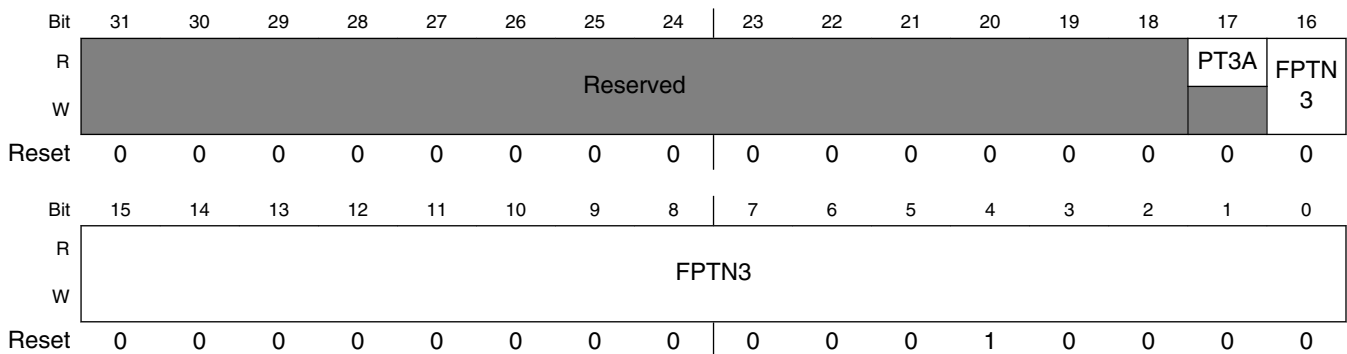Address: 20D_C180h base + 3Ch offset = 20D_C1BCh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R				P2THR							Reserved				PT2A	FPTN 2
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R								FPTN2								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

DVFSC_DVFSPT2 field descriptions

Field	Description
31–26 P2THR	P2THR - Pattern 2 Threshold Threshold of current DVFS load (after EMA), for generating interrupts with PFUS indicators 110, 111. If the current performance is greater than the P2THR value, the interrupts will be generated. Otherwise, pattern delay will be counted, but without interrupt generation.
25–18 -	This field is reserved. reserved
17 PT2A	PT2A - Pattern 2 currently active (read-only) 1 active 0 non-active
FPTN2	FPTN2 - Frequency pattern 2 counter During period of this counter the frequency will be increased to higher, than detected by the EMA-detected level.

27.10.17   DVFS pattern 3 length (DVFSC_DVFSPT3)

Address: 20D_C180h base + 40h offset = 20D_C1C0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R															PT3A	FPTN3
W							Reserved									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W							FPTN3									
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

DVFSC_DVFSPT3 field descriptions

Field	Description
31–18 -	This field is reserved. reserved
17 PT3A	PT3A - Pattern 3 currently active (read-only) 1 active 0 non-active
FPTN3	FPTN3 - Frequency pattern 3 counter During period of this counter the frequency will be set to the EMA-detected level.