

### 44.11.7 Write fine tuning

Write fine tuning is an additional circuit that provides the ability to fine tune the timing of each dq/dm bits (relative to dqs) by up to +/-100 ps.

This is done by reducing the delay between the wl\_dqs by 100 ps and adding a configurable delay of up to 200 ps (6 delay units of around 30-35 ps each) for each DQ/DM output. The delay can be configured independently for each DQ/DM. The calibration of this mechanism can be done only by writing & reading data from the memory. Controlled by register MPWRDQBY#DL.

### 44.11.8 Read fine tuning

Read fine tuning is an additional circuit that provides the ability to fine tune the timing of each coming dq bits (relative to coming dqs) by up to +/-100 ps.

This is done by reducing the delay between the incoming rd\_dqs by 100 ps and adding a configurable delay of up to 200 ps (6 delay units of around 30-35 ps each) for each DQ input. The delay can be configured independently for each DQ. The calibration of this mechanism can be done only by writing & reading data from the memory. Controlled by register MPRDDQBY#DL.

## 44.12 MMDC Memory Map/Register Definition

MMDC may be configured to several modes of operation. See [Table 44-12](#).

**Table 44-12. MMDC - Modes of Operation**

Mode of Operation	Abbreviation
DDR3 x16	DDR3_x16
DDR3 x32	DDR3_x32
DDR3 x64	DDR3_x64
LPDDR2 2-channels x16	LP2_2ch_x16
LPDDR2 2-channels x32	LP2_2ch_x32

### NOTE

In case of LPDDR2 2-channels mode while the external memory devices are exactly the same for both channels then it is recommended to configure the registers located at

0x021B\_0000 - 0x021B\_0440 and 0x021B\_4000 - 0x021B\_4440 to the same values

In case of DDR3\_x64 then IP port1 is used only to configure the parameters related to the calibration process of Byte4 - Byte7 at addresses 0x021B\_4808 - 0x021B\_48C0 as shown in [Table 44-13](#).

**Table 44-13. MMDC - Modes of Operation**

Mode of Operation	Associated Memory Map
DDR3 x16, x32	0x021B_0000 - 0x021B_08C4
DDR3 x64	0x021B_0000 - 0x021B_08C4 0x021B_4808 - 0x021B_48C0
LPDDR2 2-channels x16, x32	0x021B_0000 - 0x021B_08C4 0x021B_4808 - 0x021B_48C0

[Table 44-14](#) shows the register mode of operations.

**Table 44-14. Register Mode of Operations**

Registers	1-Channel Mode of Operations	2-Channel Mode of Operations
MMDC Core Control Register	all	LP2_2ch_x16, LP2_2ch_x32
MMDC Core Power Down Control Register		all
MMDC Core ODT Timing Control Register		LP2_2ch_x16, LP2_2ch_x32
MMDC Core Timing Configuration Register 0		
MMDC Core Timing Configuration Register 1		
MMDC Core Timing Configuration Register 2		
MMDC Core Miscellaneous Register		
MMDC Core Special Command Register		
MMDC Core Refresh Control Register		
Reserved		all
Reserved		
MMDC Core Read/Write Command Delay Register		LP2_2ch_x16, LP2_2ch_x32
MMDC Core Out of Reset Delays Register		
MMDC Core MRR Data Register	LP2_2ch_x16, LP2_2ch_x32	LP2_2ch_x16, LP2_2ch_x32
MMDC Core Timing Configuration Register 3		LP2_2ch_x16, LP2_2ch_x32
MMDC Core MR4 Derating Register		
MMDC Core Address Space Partition Register	all	
MMDC Core AXI Reordering Control Register		
MMDC Core Power Saving Control and Status Register		
MMDC Core Exclusive ID Monitor Register0		
MMDC Core Exclusive ID Monitor Register1		

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**Table 44-14. Register Mode of Operations (continued)**

Registers	1-Channel Mode of Operations	2-Channel Mode of Operations
MMDC Core Debug and Profiling Control Register 0		
MMDC Core Debug and Profiling Control Register 1		
MMDC Core Debug and Profiling Status Register 0		
MMDC Core Debug and Profiling Status Register 1		
MMDC Core Debug and Profiling Status Register 2		
MMDC Core Debug and Profiling Status Register 3		
MMDC Core Debug and Profiling Status Register 4		
MMDC Core Debug and Profiling Status Register 5		
MMDC Core Step By Step Address Register		
MMDC Core Step By Step Address Attributes Register		
Reserved	all	
MMDC Core General Purpose Register	LP2_2ch_x16, LP2_2ch_x32	
MMDC PHY ZQ HW control register	all	
MMDC PHY ZQ SW control register		
MMDC PHY Write Leveling Configuration and Error Status Register	DDR3_x64, LP2_2ch_x16, LP2_2ch_x32	
MMDC PHY Write Leveling Delay Control Register 0		
MMDC PHY Write Leveling Delay Control Register 1	DDR3_x64, LP2_2ch_x32	
MMDC PHY Write Leveling delay-line Status Register	DDR3_x64, LP2_2ch_x16, LP2_2ch_x32	
MMDC PHY ODT control register	DDR3_x16, DDR3_x32, DDR3_x64	DDR3_x64
MMDC PHY Read DQ Byte0 Delay Register	all	DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Read DQ Byte1 Delay Register		DDR3_x64, LP2_2ch_x32
MMDC PHY Read DQ Byte2 Delay Register		DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Read DQ Byte3 Delay Register		DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Write DQ Byte0 Delay Register		DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Write DQ Byte1 Delay Register		DDR3_x64, LP2_2ch_x32
MMDC PHY Write DQ Byte2 Delay Register		DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Write DQ Byte3 Delay Register		
MMDC PHY Read DQS Gating Control Register 0	DDR3_x16, DDR3_x32, DDR3_x64	DDR3_x64
MMDC PHY Read DQS Gating Control Register 1		
MMDC PHY Read DQS Gating delay-line Status Register		
MMDC PHY Read delay-lines Configuration Register	all	DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Read delay-lines Status Register		
MMDC PHY Write delay-lines Configuration Register		
MMDC PHY Write delay-lines Status Register		
MMDC PHY CK Control Register		LP2_2ch_x16, LP2_2ch_x32
MMDC ZQ LPDDR2 HW Control Register		

Table continues on the next page...

**Table 44-14. Register Mode of Operations (continued)**

Registers	1-Channel Mode of Operations	2-Channel Mode of Operations
MMDC PHY Read Delay HW Calibration Control Register	all	DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Write Delay HW Calibration Control Register		DDR3_x64, LP2_2ch_x32
MMDC PHY Read Delay HW Calibration Status Register 0		DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Read Delay HW Calibration Status Register 1		DDR3_x64, LP2_2ch_x32
MMDC PHY Write Delay HW Calibration Status Register 0		DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Write Delay HW Calibration Status Register 1		DDR3_x64, LP2_2ch_x32
MMDC PHY Write Leveling HW Error Register		DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Read DQS Gating HW Status Register 0	DDR3_x16, DDR3_x32, DDR3_x64	DDR3_x64
MMDC PHY Read DQS Gating HW Status Register 1		
MMDC PHY Read DQS Gating HW Status Register 2		
MMDC PHY Read DQS Gating HW Status Register 3		
MMDC PHY Pre-defined Compare Register 1	all	LP2_2ch_x16, LP2_2ch_x32
MMDC PHY Pre-defined Compare and CA delay-line Configuration Register		
MMDC PHY SW Dummy Access Register		DDR3_x64, LP2_2ch_x16, LP2_2ch_x32
MMDC PHY SW Dummy Read Data Register 0		
MMDC PHY SW Dummy Read Data Register 1		
MMDC PHY SW Dummy Read Data Register 2		
MMDC PHY SW Dummy Read Data Register 3		
MMDC PHY SW Dummy Read Data Register 4		
MMDC PHY SW Dummy Read Data Register 5		
MMDC PHY SW Dummy Read Data Register 6		
MMDC PHY SW Dummy Read Data Register 7		
MMDC PHY Measure Unit Register	LP2_2ch_x16, LP2_2ch_x32	LP2_2ch_x16, LP2_2ch_x32
MMDC Write CA delay-line controller		
MMDC Duty Cycle Control Register	all	DDR3_x64, LP2_2ch_x16, LP2_2ch_x32

Table 44-15 shows the maximum AXI address space for the main modes of operation.

**Table 44-15. MMDC - Maximum AXI Address Space Per Operation Mode**

Mode of Operation	Maximum AXI Address Space	Comment
LP2_2ch_x32	AXI port0: 0x8000_0000 - 0xFFFF_FFFF	Up to 2GB for LPDDR2 Channel 0
	AXI port1: 0x1000_0000 - 0x7FFF_FFFF	Up to 1.75GB for LPDDR2 Channel 1
DDR3_x64	AXI port0: 0x1000_0000 - 0xFFFF_FFFF	All address space is associated with AXI port0

The [Memory Map](#) is shown below.

**MMDC memory map**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
21B_0000	MMDC Core Control Register (MMDC1_MDCTL)	32	R/W	0311_0000h	<a href="#">44.12.1/3897</a>
21B_0004	MMDC Core Power Down Control Register (MMDC1_MDPDC)	32	R/W	0003_0012h	<a href="#">44.12.2/3899</a>
21B_0008	MMDC Core ODT Timing Control Register (MMDC1_MDOTC)	32	R/W	1227_2000h	<a href="#">44.12.3/3901</a>
21B_000C	MMDC Core Timing Configuration Register 0 (MMDC1_MDCFG0)	32	R/W	3236_22D3h	<a href="#">44.12.4/3903</a>
21B_0010	MMDC Core Timing Configuration Register 1 (MMDC1_MDCFG1)	32	R/W	B6B1_8A23h	<a href="#">44.12.5/3905</a>
21B_0014	MMDC Core Timing Configuration Register 2 (MMDC1_MDCFG2)	32	R/W	00C7_0092h	<a href="#">44.12.6/3907</a>
21B_0018	MMDC Core Miscellaneous Register (MMDC1_MDMISC)	32	R/W	0000_1600h	<a href="#">44.12.7/3909</a>
21B_001C	MMDC Core Special Command Register (MMDC1_MDSCR)	32	R/W	0000_0000h	<a href="#">44.12.8/3912</a>
21B_0020	MMDC Core Refresh Control Register (MMDC1_MDREF)	32	R/W	0000_C000h	<a href="#">44.12.9/3915</a>
21B_002C	MMDC Core Read/Write Command Delay Register (MMDC1_MDRWD)	32	R/W	0F9F_26D2h	<a href="#">44.12.10/3918</a>
21B_0030	MMDC Core Out of Reset Delays Register (MMDC1_MDOR)	32	R/W	009F_0E0Eh	<a href="#">44.12.11/3920</a>
21B_0034	MMDC Core MRR Data Register (MMDC1_MDMRR)	32	R	0000_0000h	<a href="#">44.12.12/3921</a>
21B_0038	MMDC Core Timing Configuration Register 3 (MMDC1_MDCFG3LP)	32	R/W	0000_0000h	<a href="#">44.12.13/3922</a>
21B_003C	MMDC Core MR4 Derating Register (MMDC1_MDMR4)	32	R/W	0000_0000h	<a href="#">44.12.14/3923</a>
21B_0040	MMDC Core Address Space Partition Register (MMDC1_MDASP)	32	R/W	0000_003Fh	<a href="#">44.12.15/3925</a>
21B_0400	MMDC Core AXI Reordering Control Register (MMDC1_MAARCR)	32	R/W	5142_01F0h	<a href="#">44.12.16/3926</a>
21B_0404	MMDC Core Power Saving Control and Status Register (MMDC1_MAPSR)	32	R/W	0000_1007h	<a href="#">44.12.17/3928</a>
21B_0408	MMDC Core Exclusive ID Monitor Register0 (MMDC1_MAEXIDR0)	32	R/W	0020_0000h	<a href="#">44.12.18/3931</a>
21B_040C	MMDC Core Exclusive ID Monitor Register1 (MMDC1_MAEXIDR1)	32	R/W	0060_0040h	<a href="#">44.12.19/3931</a>
21B_0410	MMDC Core Debug and Profiling Control Register 0 (MMDC1_MADPCR0)	32	R/W	0000_0000h	<a href="#">44.12.20/3932</a>

Table continues on the next page...

**MMDC memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
21B_0414	MMDC Core Debug and Profiling Control Register 1 (MMDC1_MADPCR1)	32	R/W	0000_0000h	<a href="#">44.12.21/3933</a>
21B_0418	MMDC Core Debug and Profiling Status Register 0 (MMDC1_MADPSR0)	32	R	0000_0000h	<a href="#">44.12.22/3934</a>
21B_041C	MMDC Core Debug and Profiling Status Register 1 (MMDC1_MADPSR1)	32	R	0000_0000h	<a href="#">44.12.23/3934</a>
21B_0420	MMDC Core Debug and Profiling Status Register 2 (MMDC1_MADPSR2)	32	R	0000_0000h	<a href="#">44.12.24/3935</a>
21B_0424	MMDC Core Debug and Profiling Status Register 3 (MMDC1_MADPSR3)	32	R	0000_0000h	<a href="#">44.12.25/3935</a>
21B_0428	MMDC Core Debug and Profiling Status Register 4 (MMDC1_MADPSR4)	32	R	0000_0000h	<a href="#">44.12.26/3936</a>
21B_042C	MMDC Core Debug and Profiling Status Register 5 (MMDC1_MADPSR5)	32	R	0000_0000h	<a href="#">44.12.27/3937</a>
21B_0430	MMDC Core Step By Step Address Register (MMDC1_MASBS0)	32	R	0000_0000h	<a href="#">44.12.28/3937</a>
21B_0434	MMDC Core Step By Step Address Attributes Register (MMDC1_MASBS1)	32	R	0000_0000h	<a href="#">44.12.29/3938</a>
21B_0440	MMDC Core General Purpose Register (MMDC1_MAGENP)	32	R/W	0000_0000h	<a href="#">44.12.30/3939</a>
21B_0800	MMDC PHY ZQ HW control register (MMDC1_MPZQHWCTRL)	32	R/W	A138_0000h	<a href="#">44.12.31/3939</a>
21B_0804	MMDC PHY ZQ SW control register (MMDC1_MPZQSWCTRL)	32	R/W	0000_0000h	<a href="#">44.12.32/3942</a>
21B_0808	MMDC PHY Write Leveling Configuration and Error Status Register (MMDC1_MPWLGCR)	32	R/W	0000_0000h	<a href="#">44.12.33/3944</a>
21B_080C	MMDC PHY Write Leveling Delay Control Register 0 (MMDC1_MPWLDECTRL0)	32	R/W	0000_0000h	<a href="#">44.12.34/3947</a>
21B_0810	MMDC PHY Write Leveling Delay Control Register 1 (MMDC1_MPWLDECTRL1)	32	R/W	0000_0000h	<a href="#">44.12.35/3949</a>
21B_0814	MMDC PHY Write Leveling delay-line Status Register (MMDC1_MPWLDSLST)	32	R	0000_0000h	<a href="#">44.12.36/3951</a>
21B_0818	MMDC PHY ODT control register (MMDC1_MPODTCTRL)	32	R/W	0000_0000h	<a href="#">44.12.37/3953</a>
21B_081C	MMDC PHY Read DQ Byte0 Delay Register (MMDC1_MPRDDQBY0DL)	32	R/W	0000_0000h	<a href="#">44.12.38/3955</a>
21B_0820	MMDC PHY Read DQ Byte1 Delay Register (MMDC1_MPRDDQBY1DL)	32	R/W	0000_0000h	<a href="#">44.12.39/3958</a>
21B_0824	MMDC PHY Read DQ Byte2 Delay Register (MMDC1_MPRDDQBY2DL)	32	R/W	0000_0000h	<a href="#">44.12.40/3961</a>
21B_0828	MMDC PHY Read DQ Byte3 Delay Register (MMDC1_MPRDDQBY3DL)	32	R/W	0000_0000h	<a href="#">44.12.41/3964</a>
21B_082C	MMDC PHY Write DQ Byte0 Delay Register (MMDC1_MPWRDQBY0DL)	32	R/W	0000_0000h	<a href="#">44.12.42/3966</a>

*Table continues on the next page...*

## MMDC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
21B_0830	MMDC PHY Write DQ Byte1 Delay Register (MMDC1_MPWRDQBY1DL)	32	R/W	0000_0000h	<a href="#">44.12.43/3968</a>
21B_0834	MMDC PHY Write DQ Byte2 Delay Register (MMDC1_MPWRDQBY2DL)	32	R/W	0000_0000h	<a href="#">44.12.44/3971</a>
21B_0838	MMDC PHY Write DQ Byte3 Delay Register (MMDC1_MPWRDQBY3DL)	32	R/W	0000_0000h	<a href="#">44.12.45/3973</a>
21B_083C	MMDC PHY Read DQS Gating Control Register 0 (MMDC1_MPDGCTRL0)	32	R/W	0000_0000h	<a href="#">44.12.46/3975</a>
21B_0840	MMDC PHY Read DQS Gating Control Register 1 (MMDC1_MPDGCTRL1)	32	R/W	0000_0000h	<a href="#">44.12.47/3978</a>
21B_0844	MMDC PHY Read DQS Gating delay-line Status Register (MMDC1_MPDDGLST0)	32	R	0000_0000h	<a href="#">44.12.48/3979</a>
21B_0848	MMDC PHY Read delay-lines Configuration Register (MMDC1_MPRDDLCTL)	32	R/W	4040_4040h	<a href="#">44.12.49/3981</a>
21B_084C	MMDC PHY Read delay-lines Status Register (MMDC1_MPRDDLST)	32	R	0000_0000h	<a href="#">44.12.50/3982</a>
21B_0850	MMDC PHY Write delay-lines Configuration Register (MMDC1_MPWRDLCTL)	32	R/W	4040_4040h	<a href="#">44.12.51/3983</a>
21B_0854	MMDC PHY Write delay-lines Status Register (MMDC1_MPWRDLST)	32	R	0000_0000h	<a href="#">44.12.52/3985</a>
21B_0858	MMDC PHY CK Control Register (MMDC1_MPSDCTRL)	32	R/W	0000_0000h	<a href="#">44.12.53/3986</a>
21B_085C	MMDC ZQ LPDDR2 HW Control Register (MMDC1_MPZQLP2CTL)	32	R/W	1B5F_0109h	<a href="#">44.12.54/3987</a>
21B_0860	MMDC PHY Read Delay HW Calibration Control Register (MMDC1_MPRDDLHWCTL)	32	R/W	0000_0000h	<a href="#">44.12.55/3988</a>
21B_0864	MMDC PHY Write Delay HW Calibration Control Register (MMDC1_MPWRDLHWCTL)	32	R/W	0000_0000h	<a href="#">44.12.56/3990</a>
21B_0868	MMDC PHY Read Delay HW Calibration Status Register 0 (MMDC1_MPRDDLHWST0)	32	R	0000_0000h	<a href="#">44.12.57/3992</a>
21B_086C	MMDC PHY Read Delay HW Calibration Status Register 1 (MMDC1_MPRDDLHWST1)	32	R	0000_0000h	<a href="#">44.12.58/3993</a>
21B_0870	MMDC PHY Write Delay HW Calibration Status Register 0 (MMDC1_MPWRDLHWST0)	32	R	0000_0000h	<a href="#">44.12.59/3994</a>
21B_0874	MMDC PHY Write Delay HW Calibration Status Register 1 (MMDC1_MPWRDLHWST1)	32	R	0000_0000h	<a href="#">44.12.60/3995</a>
21B_0878	MMDC PHY Write Leveling HW Error Register (MMDC1_MPWLHWERR)	32	R/W	0000_0000h	<a href="#">44.12.61/3996</a>
21B_087C	MMDC PHY Read DQS Gating HW Status Register 0 (MMDC1_MPDGHWST0)	32	R	0000_0000h	<a href="#">44.12.62/3996</a>
21B_0880	MMDC PHY Read DQS Gating HW Status Register 1 (MMDC1_MPDGHWST1)	32	R	0000_0000h	<a href="#">44.12.63/3997</a>
21B_0884	MMDC PHY Read DQS Gating HW Status Register 2 (MMDC1_MPDGHWST2)	32	R	0000_0000h	<a href="#">44.12.64/3998</a>

Table continues on the next page...

**MMDC memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
21B_0888	MMDC PHY Read DQS Gating HW Status Register 3 (MMDC1_MPDGHWST3)	32	R	0000_0000h	<a href="#">44.12.65/3998</a>
21B_088C	MMDC PHY Pre-defined Compare Register 1 (MMDC1_MPPDCMPR1)	32	R/W	0000_0000h	<a href="#">44.12.66/3999</a>
21B_0890	MMDC PHY Pre-defined Compare and CA delay-line Configuration Register (MMDC1_MPPDCMPR2)	32	R/W	0040_0000h	<a href="#">44.12.67/4000</a>
21B_0894	MMDC PHY SW Dummy Access Register (MMDC1_MPSWDAR0)	32	R/W	0000_0000h	<a href="#">44.12.68/4001</a>
21B_0898	MMDC PHY SW Dummy Read Data Register 0 (MMDC1_MPSWDRDR0)	32	R	FFFF_FFFFh	<a href="#">44.12.69/4003</a>
21B_089C	MMDC PHY SW Dummy Read Data Register 1 (MMDC1_MPSWDRDR1)	32	R	FFFF_FFFFh	<a href="#">44.12.70/4004</a>
21B_08A0	MMDC PHY SW Dummy Read Data Register 2 (MMDC1_MPSWDRDR2)	32	R	FFFF_FFFFh	<a href="#">44.12.71/4004</a>
21B_08A4	MMDC PHY SW Dummy Read Data Register 3 (MMDC1_MPSWDRDR3)	32	R	FFFF_FFFFh	<a href="#">44.12.72/4005</a>
21B_08A8	MMDC PHY SW Dummy Read Data Register 4 (MMDC1_MPSWDRDR4)	32	R	FFFF_FFFFh	<a href="#">44.12.73/4005</a>
21B_08AC	MMDC PHY SW Dummy Read Data Register 5 (MMDC1_MPSWDRDR5)	32	R	FFFF_FFFFh	<a href="#">44.12.74/4006</a>
21B_08B0	MMDC PHY SW Dummy Read Data Register 6 (MMDC1_MPSWDRDR6)	32	R	FFFF_FFFFh	<a href="#">44.12.75/4006</a>
21B_08B4	MMDC PHY SW Dummy Read Data Register 7 (MMDC1_MPSWDRDR7)	32	R	FFFF_FFFFh	<a href="#">44.12.76/4007</a>
21B_08B8	MMDC PHY Measure Unit Register (MMDC1_MPMURO)	32	R/W	0000_0000h	<a href="#">44.12.77/4007</a>
21B_08BC	MMDC Write CA delay-line controller (MMDC1_MPWRCAVL)	32	R/W	0000_0000h	<a href="#">44.12.78/4008</a>
21B_08C0	MMDC Duty Cycle Control Register (MMDC1_MPDCCR)	32	R	2492_2492h	<a href="#">44.12.79/4010</a>
21B_4000	MMDC Core Control Register (MMDC2_MDCTL)	32	R/W	0311_0000h	<a href="#">44.12.1/3897</a>
21B_4004	MMDC Core Power Down Control Register (MMDC2_MDPDC)	32	R/W	0003_0012h	<a href="#">44.12.2/3899</a>
21B_4008	MMDC Core ODT Timing Control Register (MMDC2_MDOTC)	32	R/W	1227_2000h	<a href="#">44.12.3/3901</a>
21B_400C	MMDC Core Timing Configuration Register 0 (MMDC2_MDCFG0)	32	R/W	3236_22D3h	<a href="#">44.12.4/3903</a>
21B_4010	MMDC Core Timing Configuration Register 1 (MMDC2_MDCFG1)	32	R/W	B6B1_8A23h	<a href="#">44.12.5/3905</a>
21B_4014	MMDC Core Timing Configuration Register 2 (MMDC2_MDCFG2)	32	R/W	00C7_0092h	<a href="#">44.12.6/3907</a>
21B_4018	MMDC Core Miscellaneous Register (MMDC2_MDMISC)	32	R/W	0000_1600h	<a href="#">44.12.7/3909</a>

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## MMDC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
21B_401C	MMDC Core Special Command Register (MMDC2_MDSCR)	32	R/W	0000_0000h	<a href="#">44.12.8/3912</a>
21B_4020	MMDC Core Refresh Control Register (MMDC2_MDREF)	32	R/W	0000_C000h	<a href="#">44.12.9/3915</a>
21B_402C	MMDC Core Read/Write Command Delay Register (MMDC2_MDRWD)	32	R/W	0F9F_26D2h	<a href="#">44.12.10/3918</a>
21B_4030	MMDC Core Out of Reset Delays Register (MMDC2_MDOR)	32	R/W	009F_0E0Eh	<a href="#">44.12.11/3920</a>
21B_4034	MMDC Core MRR Data Register (MMDC2_MDMRR)	32	R	0000_0000h	<a href="#">44.12.12/3921</a>
21B_4038	MMDC Core Timing Configuration Register 3 (MMDC2_MDCFG3LP)	32	R/W	0000_0000h	<a href="#">44.12.13/3922</a>
21B_403C	MMDC Core MR4 Derating Register (MMDC2_MDMR4)	32	R/W	0000_0000h	<a href="#">44.12.14/3923</a>
21B_4040	MMDC Core Address Space Partition Register (MMDC2_MDASP)	32	R/W	0000_003Fh	<a href="#">44.12.15/3925</a>
21B_4400	MMDC Core AXI Reordering Control Registers (MMDC2_MAARCR)	32	R/W	5142_01F0h	<a href="#">44.12.16/3926</a>
21B_4404	MMDC Core Power Saving Control and Status Register (MMDC2_MAPSR)	32	R/W	0000_1007h	<a href="#">44.12.17/3928</a>
21B_4408	MMDC Core Exclusive ID Monitor Register0 (MMDC2_MAEXIDR0)	32	R/W	0020_0000h	<a href="#">44.12.18/3931</a>
21B_440C	MMDC Core Exclusive ID Monitor Register1 (MMDC2_MAEXIDR1)	32	R/W	0060_0040h	<a href="#">44.12.19/3931</a>
21B_4410	MMDC Core Debug and Profiling Control Register 0 (MMDC2_MADPCR0)	32	R/W	0000_0000h	<a href="#">44.12.20/3932</a>
21B_4414	MMDC Core Debug and Profiling Control Register 1 (MMDC2_MADPCR1)	32	R/W	0000_0000h	<a href="#">44.12.21/3933</a>
21B_4418	MMDC Core Debug and Profiling Status Register 0 (MMDC2_MADPSR0)	32	R	0000_0000h	<a href="#">44.12.22/3934</a>
21B_441C	MMDC Core Debug and Profiling Status Register 1 (MMDC2_MADPSR1)	32	R	0000_0000h	<a href="#">44.12.23/3934</a>
21B_4420	MMDC Core Debug and Profiling Status Register 2 (MMDC2_MADPSR2)	32	R	0000_0000h	<a href="#">44.12.24/3935</a>
21B_4424	MMDC Core Debug and Profiling Status Register 3 (MMDC2_MADPSR3)	32	R	0000_0000h	<a href="#">44.12.25/3935</a>
21B_4428	MMDC Core Debug and Profiling Status Register 4 (MMDC2_MADPSR4)	32	R	0000_0000h	<a href="#">44.12.26/3936</a>
21B_442C	MMDC Core Debug and Profiling Status Register 5 (MMDC2_MADPSR5)	32	R	0000_0000h	<a href="#">44.12.27/3937</a>
21B_4430	MMDC Core Step By Step Address Register (MMDC2_MASBS0)	32	R	0000_0000h	<a href="#">44.12.28/3937</a>
21B_4434	MMDC Core Step By Step Address Attributes Register (MMDC2_MASBS1)	32	R	0000_0000h	<a href="#">44.12.29/3938</a>

Table continues on the next page...

**MMDC memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
21B_4440	MMDC Core General Purpose Register (MMDC2_MAGENP)	32	R/W	0000_0000h	<a href="#">44.12.30/3939</a>
21B_4800	MMDC PHY ZQ HW control register (MMDC2_MPZQHWCTRL)	32	R/W	A138_0000h	<a href="#">44.12.31/3939</a>
21B_4804	MMDC PHY ZQ SW control register (MMDC2_MPZQSWCTRL)	32	R/W	0000_0000h	<a href="#">44.12.32/3942</a>
21B_4808	MMDC PHY Write Leveling Configuration and Error Status Register (MMDC2_MPWLGCR)	32	R/W	0000_0000h	<a href="#">44.12.33/3944</a>
21B_480C	MMDC PHY Write Leveling Delay Control Register 0 (MMDC2_MPWLDECTRL0)	32	R/W	0000_0000h	<a href="#">44.12.34/3947</a>
21B_4810	MMDC PHY Write Leveling Delay Control Register 1 (MMDC2_MPWLDECTRL1)	32	R/W	0000_0000h	<a href="#">44.12.35/3949</a>
21B_4814	MMDC PHY Write Leveling delay-line Status Register (MMDC2_MPWLDSLST)	32	R	0000_0000h	<a href="#">44.12.36/3951</a>
21B_4818	MMDC PHY ODT control register (MMDC2_MPODTCTRL)	32	R/W	0000_0000h	<a href="#">44.12.37/3953</a>
21B_481C	MMDC PHY Read DQ Byte0 Delay Register (MMDC2_MPRDDQBY0DL)	32	R/W	0000_0000h	<a href="#">44.12.38/3955</a>
21B_4820	MMDC PHY Read DQ Byte1 Delay Register (MMDC2_MPRDDQBY1DL)	32	R/W	0000_0000h	<a href="#">44.12.39/3958</a>
21B_4824	MMDC PHY Read DQ Byte2 Delay Register (MMDC2_MPRDDQBY2DL)	32	R/W	0000_0000h	<a href="#">44.12.40/3961</a>
21B_4828	MMDC PHY Read DQ Byte3 Delay Register (MMDC2_MPRDDQBY3DL)	32	R/W	0000_0000h	<a href="#">44.12.41/3964</a>
21B_482C	MMDC PHY Write DQ Byte0 Delay Register (MMDC2_MPWRDQBY0DL)	32	R/W	0000_0000h	<a href="#">44.12.42/3966</a>
21B_4830	MMDC PHY Write DQ Byte1 Delay Register (MMDC2_MPWRDQBY1DL)	32	R/W	0000_0000h	<a href="#">44.12.43/3968</a>
21B_4834	MMDC PHY Write DQ Byte2 Delay Register (MMDC2_MPWRDQBY2DL)	32	R/W	0000_0000h	<a href="#">44.12.44/3971</a>
21B_4838	MMDC PHY Write DQ Byte3 Delay Register (MMDC2_MPWRDQBY3DL)	32	R/W	0000_0000h	<a href="#">44.12.45/3973</a>
21B_483C	MMDC PHY Read DQS Gating Control Register 0 (MMDC2_MPDGCTRL0)	32	R/W	0000_0000h	<a href="#">44.12.46/3975</a>
21B_4840	MMDC PHY Read DQS Gating Control Register 1 (MMDC2_MPDGCTRL1)	32	R/W	0000_0000h	<a href="#">44.12.47/3978</a>
21B_4844	MMDC PHY Read DQS Gating delay-line Status Register (MMDC2_MPDGDSLST0)	32	R	0000_0000h	<a href="#">44.12.48/3979</a>
21B_4848	MMDC PHY Read delay-lines Configuration Register (MMDC2_MPRDDLCTL)	32	R/W	4040_4040h	<a href="#">44.12.49/3981</a>
21B_484C	MMDC PHY Read delay-lines Status Register (MMDC2_MPRDDLST)	32	R	0000_0000h	<a href="#">44.12.50/3982</a>
21B_4850	MMDC PHY Write delay-lines Configuration Register (MMDC2_MPWRDLCTL)	32	R/W	4040_4040h	<a href="#">44.12.51/3983</a>

*Table continues on the next page...*

## MMDC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
21B_4854	MMDC PHY Write delay-lines Status Register (MMDC2_MPWRDLST)	32	R	0000_0000h	<a href="#">44.12.52/3985</a>
21B_4858	MMDC PHY CK Control Register (MMDC2_MPSDCTRL)	32	R/W	0000_0000h	<a href="#">44.12.53/3986</a>
21B_485C	MMDC ZQ LPDDR2 HW Control Register (MMDC2_MPZQLP2CTL)	32	R/W	1B5F_0109h	<a href="#">44.12.54/3987</a>
21B_4860	MMDC PHY Read Delay HW Calibration Control Register (MMDC2_MPRDDLHWCTL)	32	R/W	0000_0000h	<a href="#">44.12.55/3988</a>
21B_4864	MMDC PHY Write Delay HW Calibration Control Register (MMDC2_MPWRDLHWCTL)	32	R/W	0000_0000h	<a href="#">44.12.56/3990</a>
21B_4868	MMDC PHY Read Delay HW Calibration Status Register 0 (MMDC2_MPRDDLHWST0)	32	R	0000_0000h	<a href="#">44.12.57/3992</a>
21B_486C	MMDC PHY Read Delay HW Calibration Status Register 1 (MMDC2_MPRDDLHWST1)	32	R	0000_0000h	<a href="#">44.12.58/3993</a>
21B_4870	MMDC PHY Write Delay HW Calibration Status Register 0 (MMDC2_MPWRDLHWST0)	32	R	0000_0000h	<a href="#">44.12.59/3994</a>
21B_4874	MMDC PHY Write Delay HW Calibration Status Register 1 (MMDC2_MPWRDLHWST1)	32	R	0000_0000h	<a href="#">44.12.60/3995</a>
21B_4878	MMDC PHY Write Leveling HW Error Register (MMDC2_MPWLHWERR)	32	R/W	0000_0000h	<a href="#">44.12.61/3996</a>
21B_487C	MMDC PHY Read DQS Gating HW Status Register 0 (MMDC2_MPDGHWST0)	32	R	0000_0000h	<a href="#">44.12.62/3996</a>
21B_4880	MMDC PHY Read DQS Gating HW Status Register 1 (MMDC2_MPDGHWST1)	32	R	0000_0000h	<a href="#">44.12.63/3997</a>
21B_4884	MMDC PHY Read DQS Gating HW Status Register 2 (MMDC2_MPDGHWST2)	32	R	0000_0000h	<a href="#">44.12.64/3998</a>
21B_4888	MMDC PHY Read DQS Gating HW Status Register 3 (MMDC2_MPDGHWST3)	32	R	0000_0000h	<a href="#">44.12.65/3998</a>
21B_488C	MMDC PHY Pre-defined Compare Register 1 (MMDC2_MPPDCMPR1)	32	R/W	0000_0000h	<a href="#">44.12.66/3999</a>
21B_4890	MMDC PHY Pre-defined Compare and CA delay-line Configuration Register (MMDC2_MPPDCMPR2)	32	R/W	0040_0000h	<a href="#">44.12.67/4000</a>
21B_4894	MMDC PHY SW Dummy Access Register (MMDC2_MPSWDAR0)	32	R/W	0000_0000h	<a href="#">44.12.68/4001</a>
21B_4898	MMDC PHY SW Dummy Read Data Register 0 (MMDC2_MPSWDRDR0)	32	R	FFFF_FFFFh	<a href="#">44.12.69/4003</a>
21B_489C	MMDC PHY SW Dummy Read Data Register 1 (MMDC2_MPSWDRDR1)	32	R	FFFF_FFFFh	<a href="#">44.12.70/4004</a>
21B_48A0	MMDC PHY SW Dummy Read Data Register 2 (MMDC2_MPSWDRDR2)	32	R	FFFF_FFFFh	<a href="#">44.12.71/4004</a>
21B_48A4	MMDC PHY SW Dummy Read Data Register 3 (MMDC2_MPSWDRDR3)	32	R	FFFF_FFFFh	<a href="#">44.12.72/4005</a>
21B_48A8	MMDC PHY SW Dummy Read Data Register 4 (MMDC2_MPSWDRDR4)	32	R	FFFF_FFFFh	<a href="#">44.12.73/4005</a>

Table continues on the next page...

**MMDC memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
21B_48AC	MMDC PHY SW Dummy Read Data Register 5 (MMDC2_MPSWDRDR5)	32	R	FFFF_FFFFh	<a href="#">44.12.74/4006</a>
21B_48B0	MMDC PHY SW Dummy Read Data Register 6 (MMDC2_MPSWDRDR6)	32	R	FFFF_FFFFh	<a href="#">44.12.75/4006</a>
21B_48B4	MMDC PHY SW Dummy Read Data Register 7 (MMDC2_MPSWDRDR7)	32	R	FFFF_FFFFh	<a href="#">44.12.76/4007</a>
21B_48B8	MMDC PHY Measure Unit Register (MMDC2_MPMURO)	32	R/W	0000_0000h	<a href="#">44.12.77/4007</a>
21B_48BC	MMDC Write CA delay-line controller (MMDC2_MPWRCAVL)	32	R/W	0000_0000h	<a href="#">44.12.78/4008</a>
21B_48C0	MMDC Duty Cycle Control Register (MMDC2_MPDCCR)	32	R	2492_2492h	<a href="#">44.12.79/4010</a>

**44.12.1 MMDC Core Control Register (MMDCx\_MDCTL)**

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SDE_0	-	0						0					0		
W	SDE_0	SDE_1							ROW		COL		BL	0		DSIZ
Reset	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MDCTL field descriptions**

Field	Description
31 SDE_0	MMDC Enable CS0. This bit enables/disables accesses from the MMDC toward Chip Select 0. The reset value of this bit is "0" (i.e No clocks and clock enable will be driven to the memory). At the enabling point the MMDC will perform an initialization process (including a delay on RESET and/or CKE) for both chip selects. The initialization length depends on the configured memory type.

Table continues on the next page...

**MMDCx\_MDCTL field descriptions (continued)**

Field	Description
	0 Disabled 1 Enabled
30 SDE_1	<p>MMDC Enable CS1. This bit enables/disables accesses from the MMDC toward Chip Select 1. The reset value of this bit is "0" (i.e No clocks and clock enable will be driven to the memory).</p> <p>At the enabling point the MMDC will perform an initialization process (including a delay on RESET and/or CKE) for both chip selects. The initialization length depends on the configured memory type.</p> 0 Disabled 1 Enabled
29–27 Reserved	This read-only field is reserved and always has the value 0.
26–24 ROW	<p>Row Address Width. This field specifies the number of row addresses used by the memory array. It will affect the way an incoming address will be decoded.</p> <p>Settings 110-111 are reserved</p> <ul style="list-style-type: none"> <li>000 11 bits Row</li> <li>001 12 bits Row</li> <li>010 13 bits Row</li> <li>011 14 bits Row</li> <li>100 15 bits Row</li> <li>101 16 bits Row</li> </ul>
23 Reserved	This read-only field is reserved and always has the value 0.
22–20 COL	<p>Column Address Width. This field specifies the number of column addresses used by the memory array. It will determine how an incoming address will be decoded.</p> <ul style="list-style-type: none"> <li>0x0 9 bits column</li> <li>0x1 10 bits column</li> <li>0x2 11 bits column</li> <li>0x3 8 bits column</li> <li>0x4 12 bits column</li> <li>0x5-0xF Reserved</li> </ul>
19 BL	<p>Burst Length. This field determines the burst length of the DDR device.</p> <p>In LPDDR2 mode the MMDC supports burst length 4.</p> <p>In DDR3 mode the MMDC supports burst length 8.</p> <ul style="list-style-type: none"> <li>0 Burst Length 4 is used</li> <li>1 Burst Length 8 is used</li> </ul>
18 Reserved	This read-only field is reserved and always has the value 0.
17–16 DSIZ	<p>DDR data bus size. This field determines the size of the data bus of the DDR memory</p> <ul style="list-style-type: none"> <li>0 16-bit data bus</li> <li>1 32-bit data bus</li> <li>2 64-bit data bus</li> <li>3 Reserved</li> <li>—</li> </ul>

*Table continues on the next page...*

**MMDCx\_MDCTL field descriptions (continued)**

Field	Description
Reserved	This read-only field is reserved and always has the value 0.

## 44.12.2 MMDC Core Power Down Control Register (MMDCx\_MDPDC)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

**Table 44-107. PRCT field encoding**

PRCT[2:0]	Precharge Timer
000	Disabled (Bit field reset value)
001	2 clocks
010	4 clocks
011	8 clocks
100	16 clocks
101	32 clocks
110	64 clocks
111	128 clocks

**Table 44-108. PWDT field encoding**

PWDT[3:0]	Power Down Time-out
0000	Disabled (bit field reset value)
0001	16 cycles
0010	32 cycles
0011	64 cycles
0100	128 cycles
0101	256 cycles
0110	512 cycles
0111	1024 cycles
1000	2048 cycles
1001	4096 cycles
1010	8196 cycles
1011	16384 cycles
1100	32768 cycles
1101-1111	Reserved

## MMDC Memory Map/Register Definition

Address: Base address + 4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0				0				0							
W					PRCT_1				PRCT_0						tCKE	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R					PWDT_1				SLOW_PD	BOTH_CS_PD		tCKSRX		tCKSRE		
W									0	0	0	1	0	0	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

### MMDCx\_MDPDC field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–28 PRCT_1	Precharge Timer - Chip Select 1.  This field determines the amount of idle cycle for which chip select 1 will be automatically precharged. The amount of cycles are determined according to the PRCT Field Encoding table above.
27 Reserved	This read-only field is reserved and always has the value 0.
26–24 PRCT_0	Precharge Timer - Chip Select 0.  This field determines the amount of idle cycle for which chip select 0 will be automatically precharged. The amount of cycles are determined according to the table below.
23–19 Reserved	This read-only field is reserved and always has the value 0.
18–16 tCKE	CKE minimum pulse width. This field determines the minimum pulse width of CKE.  0x0 1 cycle 0x1 2 cycles 0x6 7 cycles 0x7 8 cycles
15–12 PWDT_1	Power Down Timer - Chip Select 1.  This field determines the amount of idle cycle for which chip select 1 will be automatically get into precharge/active power down. The amount of cycles are determined according to the PWDT Field Encoding table above.
11–8 PWDT_0	Power Down Timer - Chip Select 0.  This field determines the amount of idle cycle for which chip select 0 will be automatically get into precharge/active power down. The amount of cycles are determined according to the PWDT Field Encoding table above.
7 SLOW_PD	Slow/fast power down.  In DDR3 mode this field is referred to slow precharge power-down.

Table continues on the next page...

**MMDCx\_MDPDC field descriptions (continued)**

Field	Description
	In LPDDR2 mode this field is not relevant.  <b>NOTE:</b> Memory should be configured the same.  0 Fast mode. 1 Slow mode.
6 BOTH_CS_PD	Parallel power down entry to both chip selects.  When power down timer is used for both chip-selects (i.e PWDT_0 and PWDT1 don't equal "0") , then if this bit is enabled, the MMDC will enter power down only if the amount of idle cycles of both chip selects was obtained.  0 Each chip select can enter power down independently according to its configuration. 1 Chip selects can enter power down only if the amount of idle cycles of both chip selects was obtained.
5–3 tCKSRX	Valid clock cycles before self-refresh exit. This field determines the amount of clock cycles before self-refresh exit  0x0 0 cycle 0x1 1 cycles 0x6 6 cycles 0x7 7 cycles
tCKSRE	Valid clock cycles after self-refresh entry.  This field determines the amount of clock cycles after self-refresh entry  0x0 0 cycle 0x1 1 cycles 0x6 6cycles 0x7 7cycles

### 44.12.3 MMDC Core ODT Timing Control Register (MMDCx\_MDOTC)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

For further information see [ODT Configuration](#).

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0				tAOFPD		tAONPD			tANPD			tAXPD			
W																

Reset

0 0 0 1 0 0 1 0 0 0 1 0 0 1 1 1

## MMDC Memory Map/Register Definition

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	tODTLon				0	tODT_idle_off				0					
W																
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MDOTC field descriptions

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.
29–27 tAOFPD	Asynchronous RTT turn-off delay (power down with DLL frozen). This field determines the time between termination circuit starts to turn off the ODT resistance till termination has reached high impedance.  This field is not relevant in LPDDR2 mode.  0x0 1 cycle 0x1 2 cycles 0x6 7 cycles 0x7 8 cycles
26–24 tAONPD	Asynchronous RTT turn-on delay (power down with DLL frozen). This field determines the time between termination circuit gets out of high impedance and begins to turn on till ODT resistance are fully on.  This field is not relevant in LPDDR2 mode.  0x0 1 cycle 0x1 2 cycles 0x6 7 cycles 0x7 8 cycles
23–20 tANPD	Asynchronous ODT to power down entry delay. In DDR3 should be set to tCWL-1  This field is not relevant in LPDDR2 mode.  0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0xE 15 clocks 0xF 16 clocks
19–16 tAXPD	Asynchronous ODT to power down exit delay. In DDR3 should be set to tCWL-1  This field is not relevant in LPDDR2 mode.  0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0xE 15 clocks 0xF 16 clocks
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 tODTLon	ODT turn on latency. This field determines the delay between ODT signal and the associated RTT, where according to JEDEC standard it equals WL(write latency) - 2. Therefore, the value that is configured to tODTLon field should correspond the value that is configured to MDCGFG1[tCWL]  In LPDDR2 this field is not relevant.  0x0 - 0x1 Reserved

Table continues on the next page...

**MMDCx\_MDOTC field descriptions (continued)**

Field	Description
	0x2 2 cycles 0x3 3 cycles 0x4 4 cycles 0x5 5 cycles 0x6 6 cycles 0x7 Reserved
11–9 Reserved	This read-only field is reserved and always has the value 0.
8–4 tODT_idle_off	ODT turn off latency. This field determines the Idle period before turning memory ODT off. This field is not relevant in LPDDR2 mode.  0x0 0 cycle (turned off at the earliest possible time) 0x1 1 cycle 0x2 2 cycles 0x1E 30 cycles 0x1F 31 cycles
Reserved	This read-only field is reserved and always has the value 0.

**44.12.4 MMDC Core Timing Configuration Register 0  
(MMDCx\_MDCFG0)**

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																tRFC			tXS		tXP		tXPDLL		tFAW		tCL					
W	0	0	1	1	0	0	1	0	0	0	1	1	0	1	1	0	0	0	1	0	0	0	1	0	1	1	0	0	1	1		

**MMDCx\_MDCFG0 field descriptions**

Field	Description
31–24 tRFC	Refresh command to Active or Refresh command time.  See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.  0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0xFE 255 clocks 0xFF 256 clocks

*Table continues on the next page...*

**MMDCx\_MDCFG0 field descriptions (continued)**

Field	Description										
23–16 tXS	<p>Exit self refresh to non READ command. In LPDDR2 it is called tXSR, self-refresh exit to next valid command delay.</p> <p>See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.</p> <table> <tr><td>0x0</td><td>- 0x15 reserved</td></tr> <tr><td>0x16</td><td>23 clocks</td></tr> <tr><td>0x17</td><td>24 clocks</td></tr> <tr><td>0xFE</td><td>255 clocks</td></tr> <tr><td>0xFF</td><td>256 clocks</td></tr> </table>	0x0	- 0x15 reserved	0x16	23 clocks	0x17	24 clocks	0xFE	255 clocks	0xFF	256 clocks
0x0	- 0x15 reserved										
0x16	23 clocks										
0x17	24 clocks										
0xFE	255 clocks										
0xFF	256 clocks										
15–13 tXP	<p>Exit power down with DLL-on to any valid command. Exit power down with DLL-frozen to commands not requiring a locked DLL.</p> <p>In LPDDR2 mode this field is referred to Exit power-down to next valid command delay.</p> <p>See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.</p> <table> <tr><td>0x0</td><td>1 cycle</td></tr> <tr><td>0x1</td><td>2 cycles</td></tr> <tr><td>0x6</td><td>7 cycles</td></tr> <tr><td>0x7</td><td>8 cycles</td></tr> </table>	0x0	1 cycle	0x1	2 cycles	0x6	7 cycles	0x7	8 cycles		
0x0	1 cycle										
0x1	2 cycles										
0x6	7 cycles										
0x7	8 cycles										
12–9 tXPDLL	<p>Exit precharge power down with DLL frozen to commands requiring DLL.</p> <p>This field is not relevant in LPDDR2 mode.</p> <p>See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.</p> <table> <tr><td>0x0</td><td>1 clock</td></tr> <tr><td>0x1</td><td>2 clocks</td></tr> <tr><td>0x2</td><td>3 clocks</td></tr> <tr><td>0xE</td><td>15 clocks</td></tr> <tr><td>0xF</td><td>16 clocks</td></tr> </table>	0x0	1 clock	0x1	2 clocks	0x2	3 clocks	0xE	15 clocks	0xF	16 clocks
0x0	1 clock										
0x1	2 clocks										
0x2	3 clocks										
0xE	15 clocks										
0xF	16 clocks										
8–4 tFAW	<p>Four Active Window (all banks).</p> <p>See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.</p> <table> <tr><td>0x0</td><td>1 clock</td></tr> <tr><td>0x1</td><td>2 clocks</td></tr> <tr><td>0x2</td><td>3 clocks</td></tr> <tr><td>0x1E</td><td>31 clocks</td></tr> <tr><td>0x1F</td><td>32 clocks</td></tr> </table>	0x0	1 clock	0x1	2 clocks	0x2	3 clocks	0x1E	31 clocks	0x1F	32 clocks
0x0	1 clock										
0x1	2 clocks										
0x2	3 clocks										
0x1E	31 clocks										
0x1F	32 clocks										
tCL	<p>CAS Read Latency.</p> <p>In DDR3 mode this field is referred to CL.</p> <p>In LPDDR2 mode this field is referred to RL.</p> <p><b>NOTE:</b> In LPDDR2 mode only the RL/WL pairs are allowed as specified in MR2 register</p> <p>See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.</p>										

*Table continues on the next page...*

**MMDCx\_MDCFG0 field descriptions (continued)**

Field	Description
0x0	3 cycles
0x1	4 cycles
0x2	5 cycles
0x3	6 cycles
0x4	7 cycles
0x5	8 cycles
0x6	9 cycles
0x7	10 cycles
0x8	11 cycles
0x9	- 0xF Reserved

**44.12.5 MMDC Core Timing Configuration Register 1 (MMDCx\_MDCFG1)**

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 10h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	tRCD			tRP				tRC				tRAS				
W																
Reset	1	0	1	1	0	1	1	0	1	0	1	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	tRPA		0		tWR			tMRD			0		tCWL			
W																
Reset	1	0	0	0	1	0	1	0	0	0	1	0	0	0	1	1

**MMDCx\_MDCFG1 field descriptions**

Field	Description
31–29 tRCD	Active command to internal read or write delay time (same bank). (This field is valid only for DDR3 memories)  In LPDDR2 mode this parameter should be configured at tRCD_LP.  See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.  0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0x3 4 clocks 0x4 5 clocks 0x5 6 clocks

*Table continues on the next page...*

**MMDCx\_MDCFG1 field descriptions (continued)**

Field	Description
	<p>0x6 7 clocks 0x7 8 clocks</p>
28–26 tRP	<p>Precharge command period (same bank). (This field is valid only for DDR3 memories) In LPDDR2 mode this parameter should be configured at tRPpb_LP. See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.</p> <p>0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0x3 4 clocks 0x4 5 clocks 0x5 6 clocks 0x6 7 clocks 0x7 8 clocks</p>
25–21 tRC	<p>Active to Active or Refresh command period (same bank). (This field is valid only for DDR3 memories) In LPDDR2 mode this parameter should be configured at tRC_LP. See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.</p> <p>0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0x1E 31 clocks 0x1F 32 clocks</p>
20–16 tRAS	<p>Active to Precharge command period (same bank). See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.</p> <p>0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0x1E 31 clocks 0x1F Reserved</p>
15 tRPA	<p>Precharge-all command period. (This field is valid only for DDR3 memories) In LPDDR2 mode this parameter should be configured at tRPab_LP. See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.</p> <p>0 Will be equal to: tRP. 1 Will be equal to: tRP+1.</p>

*Table continues on the next page...*

**MMDCx\_MDCFG1 field descriptions (continued)**

Field	Description
14–12 Reserved	This read-only field is reserved and always has the value 0.
11–9 tWR	WRITE recovery time (same bank). See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.  0x0 1cycle 0x1 2cycles 0x2 3cycles 0x3 4cycles 0x4 5cycles 0x5 6cycles 0x6 7cycles 0x7 8 cycles
8–5 tMRD	Mode Register Set command cycle (all banks). In DDR3 mode this field shoud be set to max (tMRD,tMOD). In LPDDR2 mode this field should be set to max(tMRR,tMRW) See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.  0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0xE 15 clocks 0xF 16 clocks
4–3 Reserved	This read-only field is reserved and always has the value 0.
tCWL	CAS Write Latency. In DDR3 mode this field is referred to CWL. In LPDDR2 mode this field is referred to WL.  0x0 2cycles ( DDR3 ) , 1 cycle (LPDDR2) 0x1 3cycles ( DDR3 ) , 2 cycles (LPDDR2) 0x2 4cycles ( DDR3 ) , 3 cycles (LPDDR2) 0x3 5cycles ( DDR3 ) , 4 cycles (LPDDR2) 0x4 6cycles ( DDR3 ) , 5 cycles (LPDDR2) 0x5 7cycles ( DDR3 ) , 6 cycles (LPDDR2) 0x6 8cycles ( DDR3 ) , 7 cycles (LPDDR2) 0x7 Reserved

## 44.12.6 MMDC Core Timing Configuration Register 2 (MMDCx\_MDCFG2)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 14h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0 0 0 0 0 0 0 1 1 0 0 0 1 1 1 0 0 0 0 0 0 0 0 1 0 0 1 0 0 1 0 0

**MMDCx\_MDCFG2 field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 tDLLK	DLL locking time. This field is not relevant in LPDDR2 mode. See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.  0x0 1 cycle. 0x1 2 cycles. 0x2 3 cycles. 0xC7 200 cycles 0x1FE 511 cycles. 0x1FF 512 cycles (JEDEC value for DDR3).
15–9 Reserved	This read-only field is reserved and always has the value 0.
8–6 tRTP	Internal READ command to Precharge command delay (same bank). See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.  0x0 1cycle 0x1 2cycles 0x2 3cycles 0x3 4cycles 0x4 5cycles 0x5 6cycles 0x6 7cycles 0x7 8 cycles
5–3 tWTR	Internal WRITE to READ command delay (same bank). See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.  0x0 1cycle 0x1 2cycles 0x2 3cycles 0x3 4cycles 0x4 5cycles 0x5 6cycles

*Table continues on the next page...*

**MMDCx\_MDCFG2 field descriptions (continued)**

Field	Description
	0x6 7cycles 0x7 8 cycles
tRRD	Active to Active command period (all banks). See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter.  0x0 1cycle 0x1 2cycles 0x2 3cycles 0x3 4cycles 0x4 5cycles 0x5 6cycles 0x6 7cycles 0x7 Reserved

**44.12.7 MMDC Core Miscellaneous Register (MMDCx\_MDMISC)**

Supported Mode Of Operations:

For Channel 0: All

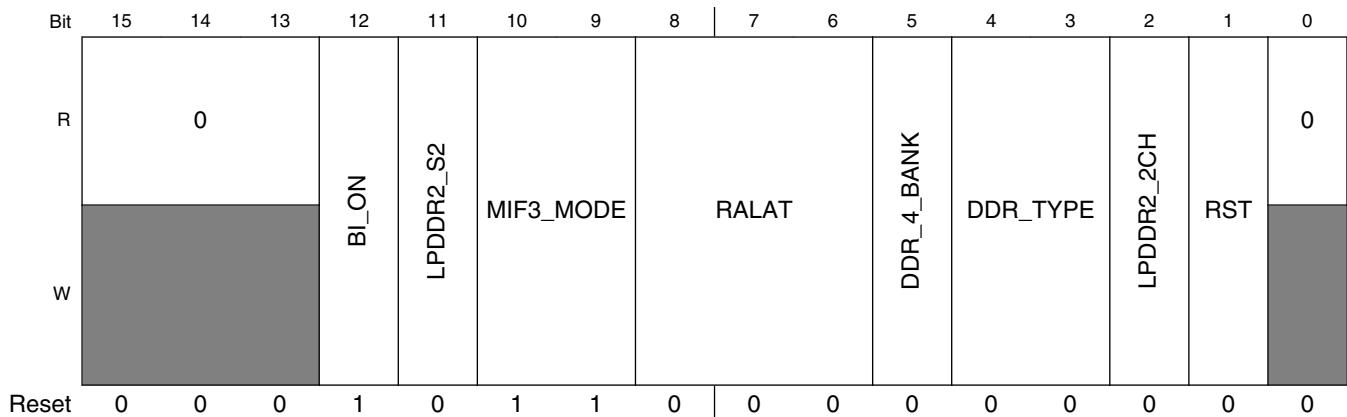
For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 18h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	CS0_RDY	CS1_RDY							0			CALIB_PER_CS	ADDR_MIRROR	LHD	WALAT	
W																

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

## MMDC Memory Map/Register Definition



### MMDCx\_MDMISC field descriptions

Field	Description
31 CS0_RDY	External status device on CS0. This is a read-only status bit, that indicates whether the external memory is in wake-up period.  0 Device in wake-up period. 1 Device is ready for initialization.
30 CS1_RDY	External status device on CS1. This is a read-only status bit, that indicates whether the external memory is in wake-up period.  0 Device in wake-up period. 1 Device is ready for initialization.
29–21 Reserved	This read-only field is reserved and always has the value 0.
20 CALIB_PER_CS	Number of chip-select for calibration process. This bit determines the chip-select index that the associated calibration is targetted to. Relevant for read, write, write leveling and read DQS gating calibrations  0 Calibration is targetted to CS0 1 Calibration is targetted to CS1
19 ADDR_MIRROR	Address mirroring.  <b>NOTE:</b> This feature is not supported for LPDDR2 memories. But only for DDR3 memories. For further information see <a href="#">Address mirroring</a> .  0 Address mirroring disabled. 1 Address mirroring enabled.
18 LHD	Latency hiding disable.  This is a debug feature. When set to "1" the MMDC will handle one read/write access at a time. Meaning that the MMDC pipe-line will be limited to 1 open access (next AXI address phase will be acknowledged if the current AXI data phase had finished)  0 Latency hiding on. 1 Latency hiding disable.
17–16 WALAT	Write Additional latency.  In case the write-leveling calibration process indicates a delay of greater than one-eighth a clock cycle (between CK and any of the DQS strobe lines), then this field must be configured accordingly.

Table continues on the next page...

**MMDCx\_MDMISC field descriptions (continued)**

Field	Description
	<p>This field will add delay on the obe I/O control, which will compensate on the additional write leveling delay on DQS and prevent the DQS from being cropped.</p> <p><b>NOTE:</b> The purpose of WALAT is to add time delay at the end of a burst write operation to ensure that the JEDEC time specification for Write Post Amble Delay (tWPST) is met (DQS strobe is held low at the end of a write burst for &gt; 30% a clock cycle before it is released). If the value of any of the WL_DL_ABS_OFFSETn register fields are greater than '1F', WALAT should be set to '1' (cycle additional delay). WALAT should be further increased for any full cycle delays added by the WL_CYC_DELn register fields.</p> <ul style="list-style-type: none"> <li>0x0 No additional latency required.</li> <li>0x1 1 cycle additional delay</li> <li>0x2 2 cycles additional delay</li> <li>0x3 3 cycles additional delay</li> </ul>
15–13 Reserved	This read-only field is reserved and always has the value 0.
12 BI_ON	<p>Bank Interleaving On. This bit controls the organization of the bank, row and column address bits.</p> <p>For further information see <a href="#">Address decoding</a>.</p> <ul style="list-style-type: none"> <li>0 Banks are not interleaved, and address will be decoded as bank-row-column</li> <li>1 Banks are interleaved, and address will be decoded as row-bank-column</li> </ul>
11 LPDDR2_S2	<p>LPDDR2 S2 device type indication.</p> <p>In case LPDDR2 device is used (DDR_TYPE = 0x1), this bit will indicate whether S2 or S4 device is used.</p> <p>This bit should be cleared in DDR3 mode</p> <ul style="list-style-type: none"> <li>0x0 LPDDR2-S4 device is used.</li> <li>0x1 LPDDR2-S2 device is used.</li> </ul>
10–9 MIF3_MODE	<p>Command prediction working mode. This field determines the level of command prediction that will be used by the MMDC</p> <ul style="list-style-type: none"> <li>00 Disable prediction.</li> <li>01 Enable prediction based on : Valid access on first pipe line stage.</li> <li>10 Enable prediction based on: Valid access on first pipe line stage, Valid access on axi bus.</li> <li>11 Enable prediction based on: Valid access on first pipe line stage, Valid access on axi bus, Next miss access from access queue.</li> </ul>
8–6 RALAT	<p>Read Additional Latency. This field determines the additional read latency which is added to CAS latency and internal delays for which the MMDC will retrieve the read data from the internal FIFO. This field is used to compensate on board/chip delays.</p> <p><b>NOTE:</b> In LPDDR2 mode 2 extra cycles will be added internally in order to compensate tDQSCK delay.</p> <ul style="list-style-type: none"> <li>0x0 no additional latency.</li> <li>0x1 1 cycle additional latency.</li> <li>0x2 2 cycles additional latency.</li> <li>0x3 3 cycles additional latency.</li> <li>0x4 4 cycles additional latency.</li> <li>0x5 5 cycles additional latency.</li> <li>0x6 6 cycles additional latency.</li> <li>0x7 7 cycles additional latency.</li> </ul>

Table continues on the next page...

**MMDCx\_MDMISC field descriptions (continued)**

Field	Description
5 DDR_4_BANK	Number of banks per DDR device. When this bit is set to "1" then the MMDC will work with DDR device of 4 banks.  0 8 banks device is being used. (Default) 1 4 banks device is being used
4–3 DDR_TYPE	DDR TYPE. This field determines the type of the external DDR device.  0x0 DDR3 device is used. (Default) 0x1 LPDDR2 device is used. — — 0x2 Reserved. 0x3 Reserved.
2 LPDDR2_2CH	LPDDR2 2-channels mode. When this bit is set to "1" then dual channel mode is activated.  This field should be cleared for DDR3 mode.  0 1-channel mode (DDR3) 1 2-channels mode (LPDDR2)
1 RST	Software Reset. When this bit is asserted then the internal FSMs and registers of the MMDC will be initialized.  <b>NOTE:</b> This bit once asserted gets deasserted automatically.  0 Do nothing. 1 Assert reset to the MMDC.
0 Reserved	This read-only field is reserved and always has the value 0.

#### **44.12.8 MMDC Core Special Command Register (MMDCx\_MDSCR)**

This register is used to issue special commands manually toward the external DDR device (such as load mode register, manual self refresh, manual precharge and so on). Every write to this register will be interpreted as a command, and a read from this register will show the last command that was executed.

Every write to this register will result in one special command, and the IP bus will assert ips\_xfr\_wait as long as the special command is being carried out.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 1Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
						CMD_ADDR_MSB_MR_OP						CMD_ADDR_LSB_MR_ADDR				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
		CON_REQ			0		MRR_READ_DATA_VALID		0			CMD		CMD_CS		CMD_BA
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MDSCR field descriptions**

Field	Description
31–24 CMD_ADDR_MSB_MR_OP	Command/Address MSB. This field indicates the MSB of the command/Address. In LPDDR2 this field indicates the MRW operand
23–16 CMD_ADDR_LSB_MR_ADDR	Command/Address LSB. This field indicates the LSB of the command/Address In LPDDR2 this field indicates the MRR/MRW address
15 CON_REQ	Configuration request. When this bit is set then the MMDC will clean the pending AXI accesses and will prevent further AXI accesses to be acknowledged. This field guarantees safe configuration (or change configuration) of the MMDC while no access is in process and prevents an unexpected behaviour. After setting this bit, it is needed to poll on CON_ACK until it is set to "1". When CON_ACK is asserted then configuration is permitted. After configuration is completed then this bit must be deasserted in order to process further AXI accesses.  <b>NOTE:</b> This bit is asserted at the end of the reset sequence, meaning that the MMDC is waiting to configure and initialize the external memory before accepting any AXI accesses. Configuration request/acknowledge mechanism should be used for the following procedures: changing of timing parameters, during calibration process or driving commands via MDSCR[CMD]  0 No request to configure MMDC. 1 A request to configure MMDC is valid
14 CON_ACK	Configuration acknowledge. Whenever this bit is set, it is permitted to configure MMDC IP registers.  0 Configuration of MMDC registers is forbidden. 1 Configuration of MMDC registers is permitted.
13–11 Reserved	This read-only field is reserved and always has the value 0.
10 MRR_READ_DATA_VALID	MRR read data valid. This field indicates that read data is valid at MDMRR register This field is relevant only for LPDDR2 mode  0 Cleared upon the assertion of MRR command 1 Set after MRR data is valid and stored at MDMRR register.
9 WL_EN	DQS pads direction. This bit controls the DQS pads direction during write-leveling calibration process. Before starting the write-leveling calibration process this bit should be set to "1". It should be set to "0" when sending write leveling exit command.  For further information see <a href="#">Write leveling Calibration</a> .  0 Exit write leveling mode or stay in normal mode. 1 Write leveling entry command was sent.
8–7 Reserved	This read-only field is reserved and always has the value 0.
6–4 CMD	Command. This field contains the command to be executed. This field will be automatically cleared after the command will be sent to the DDR memory.  0x0 Normal operation 0x1 Precharge all, command is sent independently of bank status (set correct CMD_CS). Will be issued even if banks are closed. Mainly used for init sequence purpose.

*Table continues on the next page...*

**MMDCx\_MDSCR field descriptions (continued)**

Field	Description
	0x2 Auto-Refresh Command (set correct CMD_CS). 0x3 Load Mode Register Command ( DDR3, set correct CMD_CS, CMD_BA, CMD_ADDR_LSB, CMD_ADDR_MSB), MRW Command (LPDDR2, set correct CMD_CS, MR_OP, MR_ADDR) 0x4 ZQ calibration ( DDR3, set correct CMD_CS, {CMD_ADDR_MSB,CMD_ADDR_LSB} = 0x400 or 0x0 ) 0x5 Precharge all, only if banks open (set correct CMD_CS). 0x6 MRR command (LPDDR2, set correct CMD_CS, MR_ADDR) 0x7 Reserved
3 CMD_CS	Chip Select. This field determines which chip select the command is targeted to  0 to Chip-select 0 1 to Chip-select 1
CMD_BA	Bank Address. This field determines the address of the bank within the selected chip-select where the command is targeted to.  0x0 bank address 0 0x1 bank address 1 0x2 bank address 2 0x7 bank address 7

**44.12.9 MMDC Core Refresh Control Register (MMDCx\_MDREF)**

This register determines the refresh scheme that will be executed toward the DDR device. It specifies how often a refresh cycle occurs and how many refresh commands will be executed every refresh cycle.

For further information see [Refresh Scheme](#).

The following tables show examples of possible refresh schemes.

**Table 44-116. Refresh rate example for REF\_SEL = 0**

REFR[2:0]	Number of refresh commands every 64KHz	Average periodic refresh rate (tREFI)	System Refresh period
0x0	1	15.6 µs	tRFC
0x1	2	7.8 µs	2*tRFC
0x3	4	3.9µs	4*tRFC
0x7	8	1.95 µs	8*tRFC

**Table 44-117. Refresh rate example for REF\_SEL = 1**

REFR[2:0]	Number of refresh commands every 32KHz	Average periodic refresh rate (tREFI)	System Refresh period
0x1	2	15.6 $\mu$ s	2*tRFC
0x3	4	7.8 $\mu$ s	4*tRFC
0x7	8	3.9 $\mu$ s	8*tRFC

**Table 44-118. Refresh rate example for REF\_SEL = 2@ 400MHz**

REFR[2:0]	Number of refresh commands every refresh cycle	REF_CNT	Average periodic refresh rate (tREFI)	System Refresh period
0x0	1	0x618	3.9 $\mu$ s	tRFC
0x1	2	0xC30	3.9 $\mu$ s	2*tRFC
0x2	3	0x1248	3.9 $\mu$ s	3*tRFC
0x3	4	0x1860	3.9 $\mu$ s	4*tRFC

Other refresh configurations are also allowed; the configuration values in the tables above are only examples for obtaining the desired average periodic refresh rate.

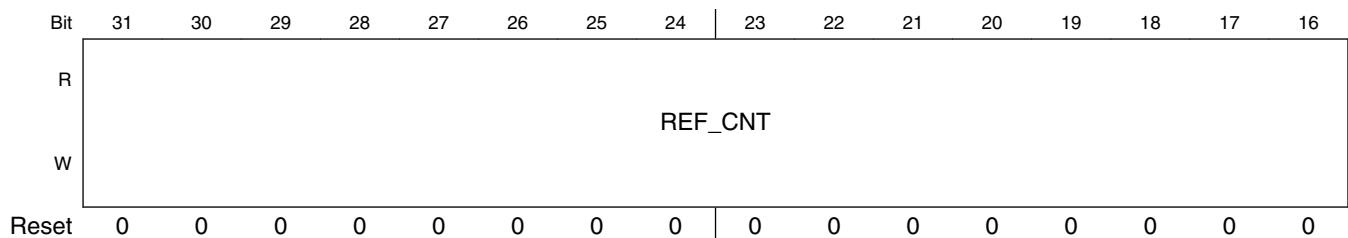
If the required average periodic refresh rate (tREFI) is kept, all of the rows will be refreshed in every refresh window. Because the memory device issues additional refresh commands for every refresh it receives, the tREFI remains the same across the device, regardless of its number of rows. This is particularly relevant in the tRFC parameter, which becomes bigger as the density increases.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 20h offset



Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	REF_SEL		REFR		0								START_REF				
W																	
Reset	1	1	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**MMDCx\_MDREF field descriptions**

Field	Description
31–16 REF_CNT	Refresh Counter at DDR clock period  If REF_SEL equals '2' a refresh cycle will begin every amount of DDR cycles configured in this field.  0x0 Reserved. 0x1 1 cycle. 0xFFFFE 65534 cycles. 0xFFFF 65535 cycles.
15–14 REF_SEL	Refresh Selector.  This bit selects the source of the clock that will trigger each refresh cycle:  0 Periodic refresh cycles will be triggered in frequency of 64KHz. 1 Periodic refresh cycles will be triggered in frequency of 32KHz. 2 Periodic refresh cycles will be triggered every amount of cycles that are configured in REF_CNT field. 3 No refresh cycles will be triggered.
13–11 REFR	Refresh Rate.  This field determines how many refresh commands will be issued every refresh cycle.  After every refresh command the MMDC won't drive any command to the DDR device until satisfying tRFC period  0x0 1 refresh 0x1 2 refreshes 0x2 3 refreshes 0x3 4 refreshes 0x4 5 refreshes 0x5 6 refreshes 0x6 7 refreshes 0x7 8 refreshes
10–1 Reserved	This read-only field is reserved and always has the value 0.
0 START_REF	Manual start of refresh cycle. When this field is set to '1' the MMDC will start a refresh cycle immediately according to number of refresh commands that are configured in 'REFR' field.  This bit returns to zero automatically.  0 Do nothing. 1 Start a refresh cycle.

#### 44.12.10 MMDC Core Read/Write Command Delay Register (MMDCx\_MDRWD)

This register determines the delay between back to back read and write accesses. The register reset values are set to the minimum required value. As the default values are set to achieve optimal results, changing them is discouraged.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 2Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			0													
W																
Reset	0	0	0	0	1	1	1	1	1	0	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		RTW_SAME		WTR_DIFF		WTW_DIFF		RTW_DIFF		RTR_DIFF					
W																
Reset	0	0	1	0	0	1	1	0	1	1	0	1	0	0	1	0

##### MMDCx\_MDRWD field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–16 tDAI	Device auto initialization period.(maximum) This field is relevant only to LPDDR2 mode  0x0 1 cycle 0xF9F 4000 cycles (Default, JEDEC value for LPDDR2, gives 10us at 400MHz clock). 0xFFFF 8192 cycles
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 RTW_SAME	Read to write delay for the same chip-select. This field controls the delay between read to write commands toward the same chip select.  The total delay is calculated according to: BL/2 + RTW_SAME + (tCL-tCWL) + RALAT  0x0 0 cycle 0x1 1 cycle 0x2 2 cycles (Default) 0x3 3 cycles 0x4 4 cycles 0x5 5 cycles

Table continues on the next page...

**MMDCx\_MDRWD field descriptions (continued)**

Field	Description
	0x6 6 cycles 0x7 7 cycles
11–9 WTR_DIFF	<p>Write to read delay for different chip-select. This field controls the delay between write to read commands toward different chip select.</p> <p>The total delay is calculated according to: <math>BL/2 + WTR\_DIFF + (tCL-tCWL) + RALAT</math></p> <ul style="list-style-type: none"> <li>0x0 0 cycle</li> <li>0x1 1 cycle</li> <li>0x2 2 cycles</li> <li>0x3 3 cycles (Default)</li> <li>0x4 4 cycles</li> <li>0x5 5 cycles</li> <li>0x6 6 cycles</li> <li>0x7 7 cycles</li> </ul>
8–6 WTW_DIFF	<p>Write to write delay for different chip-select. This field controls the delay between write to write commands toward different chip select.</p> <p>The total delay is calculated according to: <math>BL/2 + WTW\_DIFF</math></p> <ul style="list-style-type: none"> <li>0x0 0 cycle</li> <li>0x1 1 cycle</li> <li>0x2 2 cycles</li> <li>0x3 3 cycles (Default)</li> <li>0x4 4 cycles</li> <li>0x5 5 cycles</li> <li>0x6 6 cycles</li> <li>0x7 7 cycles</li> </ul>
5–3 RTW_DIFF	<p>Read to write delay for different chip-select. This field controls the delay between read to write commands toward different chip select.</p> <p>The total delay is calculated according to: <math>BL/2 + RTW\_DIFF + (tCL - tCWL) + RALAT</math></p> <ul style="list-style-type: none"> <li>0x0 0 cycle</li> <li>0x1 1 cycle</li> <li>0x2 2 cycles (Default)</li> <li>0x3 3 cycles</li> <li>0x4 4 cycles</li> <li>0x5 5 cycles</li> <li>0x6 6 cycles</li> <li>0x7 7 cycles</li> </ul>
RTR_DIFF	<p>Read to read delay for different chip-select. This field controls the delay between read to read commands toward different chip select.</p> <p>The total delay is calculated according to: <math>BL/2 + RTR\_DIFF</math></p> <ul style="list-style-type: none"> <li>0x0 0 cycle</li> <li>0x1 1 cycle</li> <li>0x2 2 cycles (Default)</li> <li>0x3 3 cycles</li> <li>0x4 4 cycles</li> </ul>

*Table continues on the next page...*

**MMDCx\_MDRWD field descriptions (continued)**

Field	Description
	0x5 5 cycles 0x6 6 cycles 0x7 7 cycles

### 44.12.11 MMDC Core Out of Reset Delays Register (MMDCx\_MDOR)

This register defines delays that must be kept when MMDC exits reset.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 30h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0								0								
W																																	
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1	1	0	

**MMDCx\_MDOR field descriptions**

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23–16 txPR	DDR3: CKE HIGH to a valid command. This field is not relevant in LPDDR2 mode.  DDR3: As defined in timing parameter table.  0x0 Reserved 0x1 2 cycles 0x2 3 cycles 0xFE 255 cycles 0xFF 256 cycles
15–14 Reserved	This read-only field is reserved and always has the value 0.
13–8 SDE_to_RST	DDR3: Time from SDE enable until DDR reset# is high. In LPDDR2 mode this field is not relevant .  <b>NOTE:</b> Each cycle in this field is 15.258 us.  0x0 Reserved 0x1 Reserved

Table continues on the next page...

**MMDCx\_MDOR field descriptions (continued)**

Field	Description
	0x2 Reserved 0x3 1 cycles 0x4 2 cycles 0x10 14 cycles (Jedec value for DDR3) - total of 200 us 0x3E 60 cycles 0x3F 61 cycles
7–6 Reserved	This read-only field is reserved and always has the value 0.
RST_to_CKE	DDR3: Time from SDE enable to CKE rise. In case that DDR reset# is low, will wait until it's high and thenwait this period until rising CKE. (JEDEC value is 500 us) LPDDR2: Idle time after first CKE assertion. (JEDEC value is 200 us) <b>NOTE:</b> Each cycle in this field is 15.258 us. 0x0 Reserved 0x1 Reserved 0x2 Reserved 0x3 1 cycles 0x10 14 cycles (JEDEC value for LPDDR2) - total of 200 us 0x23 33 cycles (JEDEC value for DDR3) - total of 500 us 0x3E 60 cycles 0x3F 61 cycles

**44.12.12 MMDC Core MRR Data Register (MMDCx\_MDMRR)**

This register contains data that was collected after issuing MRR command. The data in this register is valid only when MDSCR[MRR\_READ\_DATA\_VALID] is set to "1".

This register is relevant only in LPDDR2 mode. For further information see [LPDDR2 Refresh Rate Update and Timing Derating](#).

Supported Mode Of Operations:

For Channel 0: LP2\_2ch\_x16, LP2\_2ch\_x32

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 34h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MRR_READ_DATA3		MRR_READ_DATA2														MRR_READ_DATA1										MRR_READ_DATA0					
W																																

Reset 0

**MMDCx\_MDMRR field descriptions**

Field	Description
31–24 MRR_READ_ DATA3	MRR DATA that arrived on DQ[31:24]
23–16 MRR_READ_ DATA2	MRR DATA that arrived on DQ[23:16]
15–8 MRR_READ_ DATA1	MRR DATA that arrived on DQ[15:8]
MRR_READ_ DATA0	MRR DATA that arrived on DQ[7:0]

**44.12.13 MMDC Core Timing Configuration Register 3  
(MMDCx\_MDCFG3LP)**

This register is relevant only for LPDDR2 mode.

Supported Mode Of Operations:

For Channel 0: LP2\_2ch\_x16, LP2\_2ch\_x32

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 38h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0																
W																																	

Reset 0

**MMDCx\_MDCFG3LP field descriptions**

Field	Description
31–22 Reserved	This read-only field is reserved and always has the value 0.
21–16 RC_LP	Active to Active or Refresh command period (same bank). (This field is valid only for LPDDR2 memories)  0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0x3E 63 clocks 0x3F Reserved
15–12 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**MMDCx\_MDCFG3LP field descriptions (continued)**

Field	Description
11–8 tRCD_LP	Active command to internal read or write delay time (same bank).  (This field is valid only for LPDDR2 memories)  0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0xE 15 clocks 0xF Reserved
7–4 tRPpb_LP	Precharge (per bank) command period (same bank).  (This field is valid only for LPDDR2 memories)  0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0xE 15 clocks 0xF Reserved
tRPab_LP	Precharge (all banks) command period.  (This field is valid only for LPDDR2 memories)  0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0xE 15 clocks 0xF Reserved

**44.12.14 MMDC Core MR4 Derating Register (MMDCx\_MDMR4)**

This register is relevant only for LPDDR2 mode. It is used to dynamically change certain values depending on MR4 read result, which is based on memory temperature sensor result.

Supported Mode of Operations:

For Channel 0: LP2\_2ch\_x16, LP2\_2ch\_x32

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

## MMDC Memory Map/Register Definition

Address: Base address + 3Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R									0								
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R								0	tRRD_DE	tRP_DE	tRAS_DE	tRC_DE	tRCD_DE	0	UPDATE_DE_ACK	UPDATE_DE_REQ	
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MDMR4 field descriptions

Field	Description
31–9 Reserved	This read-only field is reserved and always has the value 0.
8 tRRD_DE	tRRD derating value. 0 Original tRRD is used. 1 tRRD is derated in 1 cycle.
7 tRP_DE	tRP derating value.

Table continues on the next page...

**MMDCx\_MDMR4 field descriptions (continued)**

Field	Description
	0 Original tRP is used. 1 tRP is derated in 1 cycle.
6 tRAS_DE	tRAS derating value. 0 Original tRAS is used. 1 tRAS is derated in 1 cycle.
5 tRC_DE	tRC derating value. 0 Original tRC is used. 1 tRC is derated in 1 cycle.
4 tRCD_DE	tRCD derating value. 0 Original tRCD is used. 1 tRCD is derated in 1 cycle.
3–2 Reserved	This read-only field is reserved and always has the value 0.
1 UPDATE_DE_ACK	Update Derated Values Acknowledge. This read only bit will be cleared upon UPDATE_DE_REQ assertion and will be set after the new values are taken.
0 UPDATE_DE_REQ	Update Derated Values Request. This read modify write field is automatically cleared after the request is issued. 0 Do nothing. 1 Request to update the following values: tRRD, tRCD, tRP, tRC, tRAS and refresh related fields(MDREF register): REF_CNT, REF_SEL, REFR

#### 44.12.15 MMDC Core Address Space Partition Register (MMDCx\_MDASP)

This register defines the partitioning between chip select 0 and chip select 1. For further information see [Chip select settings](#).

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 40h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
R																0																			
W																																			

Reset 0 1 1 1 1 1 1

**MMDCx\_MDASP field descriptions**

Field	Description
31–7 Reserved	This read-only field is reserved and always has the value 0.
CS0_END	<p>CS0_END. Defines the absolute last address associated with CS0 with increments of 256Mb. CS0_END=AXI_ADDRESS[31:25] bits.</p> <p>In DDR3 and 1-channel LPDDR2 mode: MMDCx_MDASP[CS0_END] should be set to DDR_CS_SIZE/32MB + 0x7 (DDR base address begins at 0x10000000)</p> <p>In 2-channel LPDDR2 mode: MMDC0_MDASP[CS0_END] should be set to DDR_CS_SIZE/32M + 0x3f (channel 0 base address begins at 0x80000000) MMDC1_MDASP[CS0_END] should be set to DDR_CS_SIZE/32M + 0x7 (channel 1 base address begins at 0x10000000)</p> <p>In 2-channel LPDDR2 with 4k-interleave mode: MMDC0_MDASP[CS0_END] should be set to DDR_CS_SIZE/32M + 0x43 MMDC1_MDASP[CS0_END] should be set to DDR_CS_SIZE/32M + 0x3</p>

#### 44.12.16 MMDC Core AXI Reordering Control Register (MMDCx\_MAARCR)

This register determines the values of the weights used for the re-ordering arbitration engine. For further information see [Performance](#).

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 400h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	ARCR_SEC_ERR_LOCK	ARCR_SEC_ERR_EN	Reserved	ARCR_EXC_ERR_EN	Reserved	Reserved	Reserved	ARCR_RCH_EN	Reserved	ARCR_PAG_HIT	0	0	0	0	0	0
W	0	1	0	1	0	0	0	1	0	1	0	0	0	1	0	0

Reset

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
	Reserved				ARCR_DYN_JMP				ARCR_DYN_MAX				ARCR_GUARD			
W																
Reset	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0

**MMDCx\_MAARCR field descriptions**

Field	Description
31 ARCR_SEC_ERR_LOCK	Once set, this bit locks ARCR_SEC_ERR_EN and prevents from its updating. This bit can be only cleared by reset  Default value is 0x0 - encoding 0 (unlocked)  0 ARCR_SEC_ERR_EN is unlocked, so can be updated any moment 1 ARCR_SEC_ERR_EN is locked, so it can't be updated
30 ARCR_SEC_ERR_EN	This bit defines whether security read/write access violation result in SLV Error response or in OKAY response  Default value is 0x1 - encoding 1(response is SLV Error, rresp/bresp=2'b10)  0 security violation results in OKAY response (rresp/bresp=2'b00) 1 security violation results in SLAVE Error response (rresp/bresp=2'b10)
29 -	This field is reserved. Reserved
28 ARCR_EXC_ERR_EN	This bit defines whether exclusive read/write access violation of AXI 6.2.4 rule result in SLV Error response or in OKAY response  Default value is 0x1 - encoding 1(response is SLV Error)  0 violation of AXI exclusive rules (6.2.4) result in OKAY response (rresp/bresp=2'b00) 1 violation of AXI exclusive rules (6.2.4) result in SLAVE Error response (rresp/bresp=2'b10)
27–25 -	This field is reserved. Reserved
24 ARCR_RCH_EN	This bit defines whether Real time channel is activated and bypassed all other pending accesses, So accesses with QoS=='F' will be granted the highest prioritiy in the optimization/reordering mechanism  Default value is 0x1 - encoding 1 (Enabled)  0 normal prioritization, no bypassing 1 accesses with QoS=='F' bypass the arbitration
23 -	This field is reserved. Reserved
22–20 ARCR_PAG_HIT	ARCR Page Hit Rate. This value will be added by the optimization/reordering mechanism to any pending access that is targeted to an open DDR row.  Default value of ARCR_PAG_HIT is 0x00100 - encoding 4.
19 -	This field is reserved. Reserved

Table continues on the next page...

**MMDCx\_MAARCR field descriptions (continued)**

Field	Description
18–16 ARCR_ACC_HIT	ARCR Access Hit Rate. This value will be added by the optimization/reordering mechanism to any pending access that has the same access type (read/write) as the previous access.  Default value of is ARCR_ACC_HIT 0x0010 - encoding 2.
15–12 -	This field is reserved. Reserved
11–8 ARCR_DYN_JMP	ARCR Dynamic Jump. Each time an access wan't chosen by the optimization/reordering mechanism then its dynamic score will be incremented by ARCR_DYN_JMP value.  <b>NOTE:</b> Setting ARCR_DYN_JMP may cause starvation of low priority accesses  <b>NOTE:</b> ARCR_DYN_JMP must be smaller than ARCR_DYN_MAX  Default ARCR_DYN_JMP value is 0x0001 - encoding 1
7–4 ARCR_DYN_MAX	ARCR Dynamic Maximum. ARCR_DYN_MAX is the maximum dynamic score value that each access inside the optimization/reordering mechanism can get.  0000 0 0001 1 1111 15 (default)
ARCR_GUARD	ARCR Guard. After an access reached the maximum dynamic score value, it will wait additional ARCR_GUARD arbitration cycles and then will gain the highest priority in the optimization/reordering mechanism.  0000 15 (default) 0001 16 1111 30

#### **44.12.17 MMDC Core Power Saving Control and Status Register (MMDCx\_MAPSR)**

The MAPSR determines the power saving features of MMDC. For further information see [Power Saving and Clock Frequency Change modes](#).

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 404h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R							DVACK	LPACK								
W							Reserved		Reserved		DVFS		LPMD		Reserved	

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									WIS	RIS	PSS					
W							PST		Reserved	0	0	0	0	0	0	PSD

Reset 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 1 1

**MMDCx\_MAPSR field descriptions**

Field	Description
31–26 -	This field is reserved. Reserved
25 DVACK	General DVFS acknowledge. This read only bit indicates whether a dvfs acknowledge was asserted and that MMDC is in self-refresh mode
24 LPACK	General low-power acknowledge. This read only bit indicates whether a low-power acknowledge was asserted and that MMDC is in self-refresh mode
23–22 -	This field is reserved. Reserved
21 DVFS	General DVFS request. SW request for DVFS. Assertion of this bit will yield in self-refresh entry sequence  0 no dvfs request 1 dvfs request
20 LPMD	General LPMD request. SW request for LPMD. Assertion of this bit will yield in self-refresh entry sequence  0 no lpmd request 1 lpmd request
19–16 -	This field is reserved. Reserved
15–8 PST	Automatic Power saving timer.  Valid only when PSD is set to "0". When the MMDC is idle for amount of cycles specified in that field then the DDR device will be entered automatically into self-refresh mode.  The real value which is used is register-value multiplied by 64.  00000000 Reserved - this value is forbidden. 00000001 timer is configured to 64 clock cycles. 00000010 timer is configured to 128 clock cycles. 00010000 (Default)- 1024 clock cycles. 11111111 timer clock is configured to 16320 clock cycles.
7 -	This field is reserved. Reserved.
6 WIS	Write Idle Status.This read only bit indicates whether write request buffer is idle (empty) or not.  0 idle 1 not idle
5 RIS	Read Idle Status.This read only bit indicates whether read request buffer is idle (empty) or not.  0 idle 1 not idle
4 PSS	Power Saving Status. This read only bit indicates whether the MMDC is in automatic power saving mode.  0 not in power saving 1 power saving
3–1 -	This field is reserved. Reserved.
0 PSD	Automatic Power Saving Disable. When the value of PSD is "0" (i.e automatic power saving is enabled) then the PST is activated and MMDC will enter automatically to self-refresh while the number of idle cycle reached.

*Table continues on the next page...*

**MMDCx\_MAPSR field descriptions (continued)**

Field	Description
	<b>NOTE:</b> This bit must be disabled (i.e set to "1") during calibration process 0 power saving enabled 1 power saving disabled (default)

**44.12.18 MMDC Core Exclusive ID Monitor Register0 (MMDCx\_MAEXIDR0)**

This register defines the ID to be monitored for exclusive accesses of monitor0 and monitor1. For further information see [Exclusive accesses handling](#).

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 408h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0 0 0 0 0 0 0 0 0 0 1 0

**MMDCx\_MAEXIDR0 field descriptions**

Field	Description
31–16 EXC_ID_MONITOR1	This field defines ID for Exclusive monitor#1. Default value is 0x0020
EXC_ID_MONITOR0	This field defines ID for Exclusive monitor#0. Default value is 0x0000

**44.12.19 MMDC Core Exclusive ID Monitor Register1 (MMDCx\_MAEXIDR1)**

This register defines the ID to be monitored for exclusive accesses of monitor2 and monitor3. For further information see [Exclusive accesses handling](#).

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

## MMDC Memory Map/Register Definition

Address: Base address + 40Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0 0 0 0 0 0 0 0 0 1 1 0

### MMDCx\_MAEXIDR1 field descriptions

Field	Description
31–16 EXC_ID_MONITOR3	This feild defines ID for Exclusive monitor#3. Default value is 0x0060
EXC_ID_MONITOR2	This feild defines ID for Exclusive monitor#2. Default value is 0x0040

## 44.12.20 MMDC Core Debug and Profiling Control Register 0 (MMDCx\_MADPCR0)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 410h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																

**MMDCx\_MADPCR0 field descriptions**

Field	Description
31–10 Reserved	This read-only field is reserved and always has the value 0.
9 SBS	Step By Step trigger. If SBS_EN is set to "1" then dispatching AXI pending access toward the DDR will done only if this bit is set to "1", otherwise no access will be dispatched toward the DDR. This bit is cleared when the pending access has been issued toward the DDR device.  1 Launch AXI pending access toward the DDR 0 No access will be launched toward the DDR
8 SBS_EN	Step By Step debug Enable. Enable step by step mode. Every time this mechanism is enabled then setting SBS to "1" will dispatch one pending AXI access to the DDR and in parallel its attributes will be observed in the status registres (MASBS0 and MASBS1). For further information see <a href="#">Step By Step (SBS software monitor</a> .  0 disable 1 enable
7–4 Reserved	This read-only field is reserved and always has the value 0.
3 CYC_OVF	Total Profiling Cycles Count Overflow. When profiling mechanism is enabled (DBG_EN is set to "1") then this bit is asserted when overflow of CYC_COUNT occurred. Cleared by writing 1 to it.  0 no overflow 1 overflow
2 PRF_FRZ	Profiling freeze. When this bit is asserted then the profiling mechanism will be freezed and the associated status registers ( MADPSR0-MADPSR5) will hold the current profiling values.  0 profiling counters are not frozen 1 profiling counters are frozen
1 DBG_RST	Debug and Profiling Reset. Reset all debug and profiling counters and components.  0 no reset 1 reset
0 DBG_EN	Debug and Profiling Enable. Enable debug and profiling mechanism. When this bit is asserted then the MMDC will perform a profiling based on the ID that is configured to MADPCR1. Upon assertion of PRF_FRZ the profiling will be freezed and the profiling results will be sampled to the status registers (MADPSR0-MADPSR5). For further information see <a href="#">MMDC Profiling</a> .  default is "disable"  0 disable 1 enable

**44.12.21 MMDC Core Debug and Profiling Control Register 1 (MMDCx\_MADPCR1)**

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

## MMDC Memory Map/Register Definition

Address: Base address + 414h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

### MMDCx\_MADPCR1 field descriptions

Field	Description
31–16 PRF_AXI_ID_ MASK	Profiling AXI ID Mask. AXI ID bits which masked by this value are chosen for profiling. 1 AXI ID specific bit is chosen for profiling 0 AXI ID specific bit is ignored (don't care)
PRF_AXI_ID	Profiling AXI ID. AXI IDs that matches a bit-wise AND logic operation between PRF_AXI_ID and PRF_AXI_ID_MASK are chosen for profiling. Default value is 0x0, to choose any ID-s for profiling

## 44.12.22 MMDC Core Debug and Profiling Status Register 0 (MMDCx\_MADPSR0)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 418h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

### MMDCx\_MADPSR0 field descriptions

Field	Description
CYC_COUNT	Total Profiling cycle Count. This field reflects the total cycle count in case the profiling mechanism is enabled from assertion of DBG_EN and until PRF_FRZ is asserted

## 44.12.23 MMDC Core Debug and Profiling Status Register 1 (MMDCx\_MADPSR1)

The register reflects the total cycles during which the MMDC state machines were busy (both writes and reads). This information can be used for DDR Utilization calculation.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 41Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BUSY_COUNT																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### MMDCx\_MADPSR1 field descriptions

Field	Description
BUSY_COUNT	Profiling Busy Cycles Count. This field reflects the total number of cycles where the MMDC read and write state machines were busy during the profiling period. Can be used for DDR utilization calculations. Busy cycles are any MMDC clock cycles where the internal state machine is not idle. If any read or write requests are pending in the FIFOs, the MMDC is not idle.

### 44.12.24 MMDC Core Debug and Profiling Status Register 2 (MMDCx\_MADPSR2)

This register reflects the total number of read accesses (per AXI ID) toward MMDC.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 420h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RD_ACC_COUNT																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### MMDCx\_MADPSR2 field descriptions

Field	Description
RD_ACC_COUNT	Profiling Read Access Count. This register reflects the total number of read accesses (per AXI ID) toward MMDC.

### 44.12.25 MMDC Core Debug and Profiling Status Register 3 (MMDCx\_MADPSR3)

This register reflects the total number of write accesses (per AXI ID) toward MMDC.

## MMDC Memory Map/Register Definition

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 424h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	WR_ACC_COUNT																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

### MMDCx\_MADPSR3 field descriptions

Field	Description
WR_ACC_COUNT	Profiling Write Access Count. This register reflects the total number of write accesses (per AXI ID) toward MMDC.

## 44.12.26 MMDC Core Debug and Profiling Status Register 4 (MMDCx\_MADPSR4)

This register reflects the total number of bytes that were transferred during read access (per AXI ID) toward MMDC.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 428h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RD_BYTES_COUNT																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

### MMDCx\_MADPSR4 field descriptions

Field	Description
RD_BYTES_COUNT	Profiling Read Bytes Count. This register reflects the total number of bytes that were transferred during read access (per AXI ID) toward MMDC.

### 44.12.27 MMDC Core Debug and Profiling Status Register 5 (MMDCx\_MADPSR5)

This register reflects the total number of bytes that were transferred during write access (per AXI ID) toward MMDC.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 42Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	WR_BYTES_COUNT																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### MMDCx\_MADPSR5 field descriptions

Field	Description
WR_BYTES_COUNT	Profiling Write Bytes Count. This register reflects the total number of bytes that were transferred during write access (per AXI ID) toward MMDC.

### 44.12.28 MMDC Core Step By Step Address Register (MMDCx\_MASBS0)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 430h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SBS_ADDR																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### MMDCx\_MASBS0 field descriptions

Field	Description
SBS_ADDR	Step By Step Address. These bits reflect the address of the pending request in case of step by step mode.

## 44.12.29 MMDC Core Step By Step Address Attributes Register (MMDCx\_MASBS1)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 434h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SBS_AXI_ID															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SBS_LEN		SBS_BUFF		SBS_BURST		SBS_SIZE		SBS_PROT		SBS_LOCK		SBS_TYPE		SBS_VLD	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MASBS1 field descriptions

Field	Description
31–16 SBS_AXI_ID	Step By Step AXI ID. These bits reflect the AXI ID of the pending request in case of step by step mode.
15–13 SBS_LEN	Step By Step Length. These bits reflect the AXI LENGTH of the pending request in case of step by step mode.  000 burst of length 1 001 burst of length 2 111 burst of length 8
12 SBS_BUFF	Step By Step Buffered. This bit reflect the AXI CACHE[0] of the pending request in case of step by step mode. Relevant only for write requests
11–10 SBS_BURST	Step By Step Burst. These bits reflect the AXI BURST of the pending request in case of step by step mode.  00 FIXED 01 INCR burst 10 WRAP burst 11 reserved
9–7 SBS_SIZE	Step By Step Size. These bits reflect the AXI SIZE of the pending request in case of step by step mode.  000 8 bits 001 16 bits 010 32 bits 011 64 bits

Table continues on the next page...

**MMDCx\_MASBS1 field descriptions (continued)**

Field	Description
	100 128bits 101-111 Reserved
6-4 SBS_PROT	Step By Step Protection. These bits reflect the AXI PROT of the pending request in case of step by step mode.
3-2 SBS_LOCK	Step By Step Lock. These bits reflect the AXI LOCK of the pending request in case of step by step mode.
1 SBS_TYPE	Step By Step Request Type. These bits reflect the type (read/write) of the pending request in case of step by step mode. 0 write 1 read
0 SBS_VLD	Step By Step Valid. This bit reflects whether there is a pending request in case of step by step mode. 0 not valid 1 valid

**44.12.30 MMDC Core General Purpose Register (MMDCx\_MAGENP)**

This register is a general 32 bit read/write register.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 440h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

**MMDCx\_MAGENP field descriptions**

Field	Description
GP31_GP0	General purpose read/write bits.

**44.12.31 MMDC PHY ZQ HW control register (MMDCx\_MPZQHWCTRL)**

Supported Mode Of Operations:

For Channel 0: All

## MMDC Memory Map/Register Definition

For Channel 1: This register is reserved for channel 1. Channel 1 ZQ is also controlled by MMDC0\_MPZQHWCTRL.

Address: Base address + 800h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	ZQ_EARLY_COMPARATOR_EN_TIMER					0			TZQ_CS		TZQ_OPER		TZQ_INIT		ZQ_HW_FOR	
W																
Reset	1	0	1	0	0	0	0	0	1	0	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ZQ_HW_PD_RES						ZQ_HW_PU_RES				ZQ_HW_PER		ZQ_MODE			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MPZQHWCTRL field descriptions

Field	Description
31–27 ZQ_EARLY_COMPARATOR_EN_TIMER	ZQ early comparator enable timer. This timer defines the interval between the warming up of the comparator of the i.MX ZQ calibration pad and the begining of the ZQ calibration process with the pad  0x0 - 0x6 Reserved 0x7 8 cycles 0x14 21 cycles (Default) 0x1E 31 cycles 0x1F 32 cycles
26 Reserved	This read-only field is reserved and always has the value 0.
25–23 TZQ_CS	Device ZQ short time. This field holds the number of cycles that are required by the external DDR device to perform ZQ short calibration. Upon driving the command to the DDR device then no further accesses will be issued to the DDR device till satisfying that time.  <b>NOTE:</b> In LPDDR2 the ZQ short time is taken from MPZQLP2CTL[ZQ_LP2_HW_ZQCS]  <b>NOTE:</b> This field should not be update during ZQ calibration.  000 Reserved 001 Reserved 010 128 cycles (Default) 011 256 cycles 100 512 cycles 101 1024 cycles 110- 111 Resreveed
22–20 TZQ_OPER	Device ZQ long/oper time. This field holds the number of cycles that are required by the external DDR device to perform ZQ long calibration except the first ZQ long command that is issued after reset. Upon driving the command to the DDR device then no further accesses will be issued to the DDR device till satisfying that time.  <b>NOTE:</b> In LPDDR2 the ZQ oper time is taken from MPZQLP2CTL[ZQ_LP2_HW_ZQCL]  <b>NOTE:</b> This field should not be update during ZQ calibration.  000 Reserved

Table continues on the next page...

**MMDCx\_MPZQHWCTRL field descriptions (continued)**

Field	Description
	<p>001 Reserved      010 128 cycles      011 256 cycles - Default (JEDEC value for DDR3)      100 512 cycles      101 1024 cycles      110- 111 Reserved</p>
19–17 TZQ_INIT	<p>Device ZQ long/init time. This field holds the number of cycles that are required by the external DDR device to perform ZQ long calibration right after reset. Upon driving the command to the DDR device then no further accesses will be issued to the DDR device till satisfying that time.</p> <p><b>NOTE:</b> In LPDDR2 the ZQ init time is taken from MPZQLP2CTL[ZQ_LP2_HW_ZQINIT]</p> <p><b>NOTE:</b> This field should not be update during ZQ calibration.</p> <p>000 Reserved      001 Reserved      010 128 cycles      011 256 cycles      100 512 cycles - Default (JEDEC value for DDR3)      101 1024 cycles      110- 111 Reserved</p>
16 ZQ_HW_FOR	<p>Force ZQ automatic calibration process with the i.MX ZQ calibration pad. When this bit is asserted then the MMDC will issue one ZQ automatic calibration process with the i.MX ZQ calibration pad. It is the user responsibility to make sure that all the accesses to DDR will be finished before asserting this bit using CON_REQ/CON_ACK mechanism. HW will negate this bit upon completion of the ZQ calibration process. Upon negation of this bit the ZQ HW calibration pull-up and pull-down results (ZQ_HW_PU_RES and ZQ_HW_PD_RES respectively) are valid</p> <p><b>NOTE:</b> In order to enable this bit ZQ_MODE must be set to either "1" or "3"</p>
15–11 ZQ_HW_PD_RES	<p>ZQ HW calibration pull-down result. This field holds the pull-down resistor value calculated at the end of the ZQ automatic calibration process with the i.MX ZQ calibration pad.</p> <p>00000 Max. resistance.      11111 Min. resistance.</p>
10–6 ZQ_HW_PU_RES	<p>ZQ automatic calibration pull-up result. This field holds the pull-up resistor value calculated at the end of the ZQ automatic calibration process with the i.MX ZQ calibration pad.</p> <p>00000 Min. resistance.      11111 Max. resistance.</p>
5–2 ZQ_HW_PER	<p>ZQ periodic calibration time. This field determines how often the periodic ZQ calibration is performed. This field is applied for both ZQ short calibration and ZQ automatic calibration process with i.MX ZQ calibration pad. Whenever this timer is expired then according to ZQ_MODE the ZQ automatic calibration process with the i.MX ZQ calibration pad will be issued and/or short/long command will be issued to the external DDR device.</p> <p>This field is ignored if ZQ_MODE equals "00"</p> <p>0000 ZQ calibration is performed every 1 ms.      0001 ZQ calibration is performed every 2 ms.      0010 ZQ calibration is performed every 4 ms.      1010 ZQ calibration is performed every 1 sec.</p>

*Table continues on the next page...*

**MMDCx\_MPZQHWCTRL field descriptions (continued)**

Field	Description
	1110 ZQ calibration is performed every 16 sec. 1111 ZQ calibration is performed every 32 sec.
ZQ_MODE	ZQ calibration mode:  0x0 No ZQ calibration is issued. (Default) 0x1 ZQ calibration is issued to i.MX ZQ calibration pad together with ZQ long command to the external DDR device only when exiting self refresh. 0x2 ZQ calibration command long/short is issued only to the external DDR device periodically and when exiting self refresh 0x3 ZQ calibration is issued to i.MX ZQ calibration pad together with ZQ calibration command long/short to the external DDR device periodically and when exiting self refresh

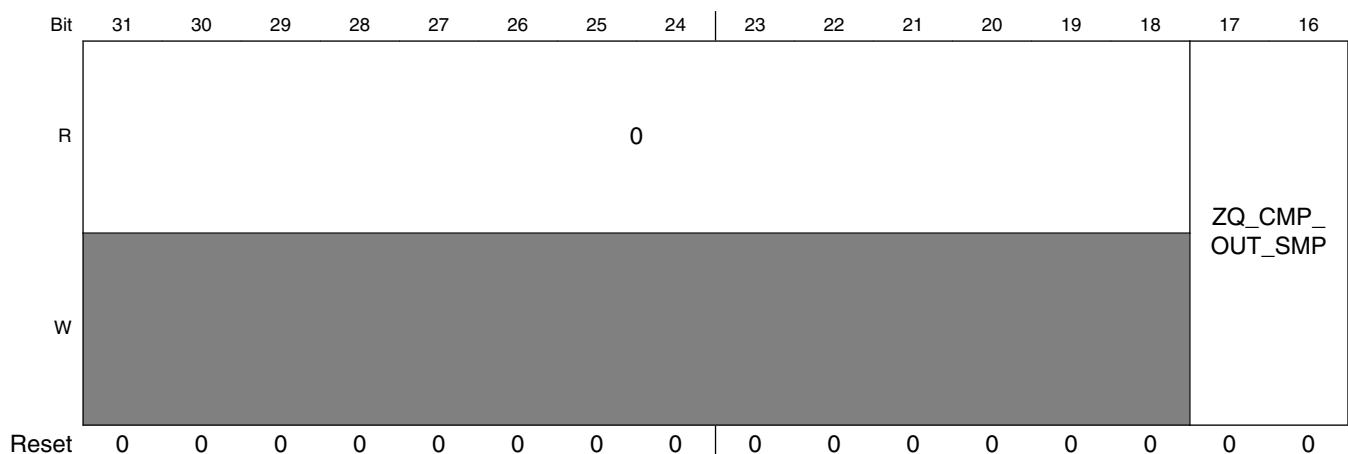
### 44.12.32 MMDC PHY ZQ SW control register (MMDCx\_MPZQSWCTRL)

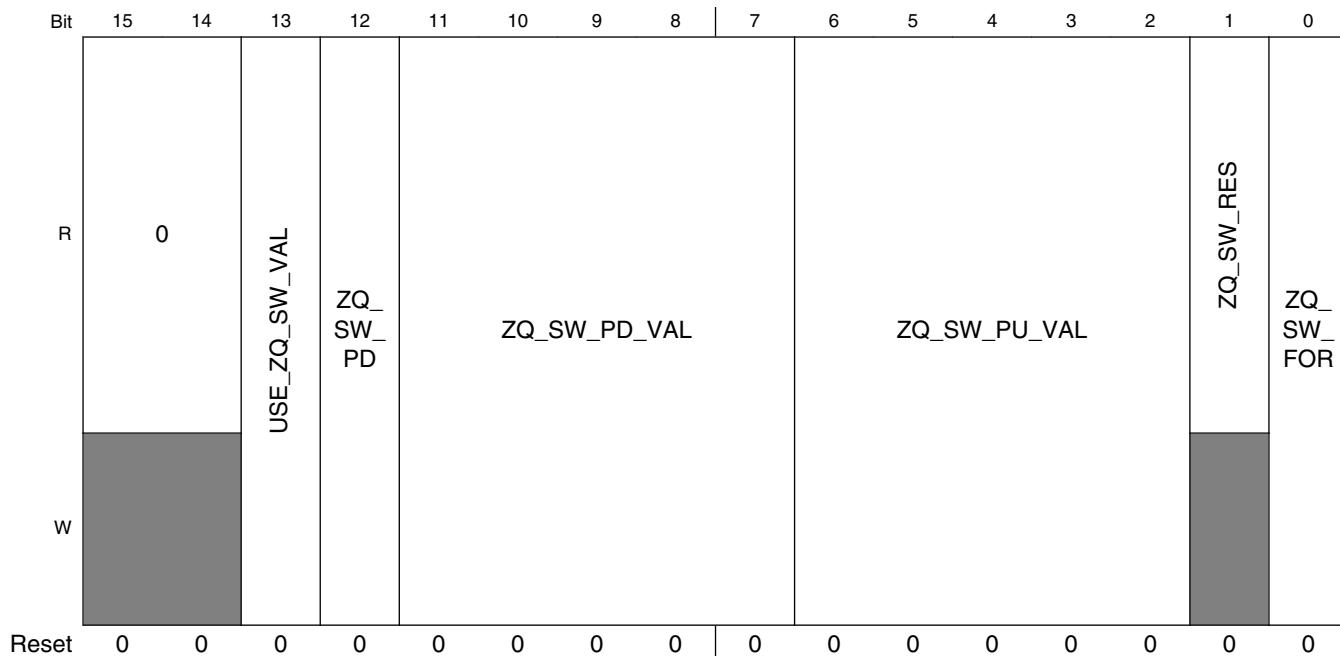
Supported Mode Of Operations:

For Channel 0: All

For Channel 1: This register is reserved.

Address: Base address + 804h offset



**MMDCx\_MPZQSWCTRL field descriptions**

Field	Description
31–18 Reserved	This read-only field is reserved and always has the value 0.
17–16 ZQ_CMP_OUT_SMP	Defines the amount of cycles between driving the ZQ signals to the ZQ pad and till sampling the comparator enable output while performing ZQ calibration process with the i.MX ZQ calibration pad 00 7 cycles 01 15 cycles 10 23 cycles 11 31 cycles
15–14 Reserved	This read-only field is reserved and always has the value 0.
13 USE_ZQ_SW_VAL	Use SW ZQ configured value for I/O pads resistor controls. This bit selects whether ZQ SW value or ZQ HW value will be driven to the I/O pads resistor controls. By default this bit is cleared and MMDC drives the HW ZQ status bits on the resistor controls of the I/O pads. <b>NOTE:</b> This bit should not be updated during ZQ calibration. 0 Fields ZQ_HW_PD_VAL & ZQ_HW_PU_VAL will be driven to I/O pads resistor controls. 1 Fields ZQ_SW_PD_VAL & ZQ_SW_PU_VAL will be driven to I/O pads resistor controls.
12 ZQ_SW_PD	ZQ software PU/PD calibration. This bit determines the calibration stage (PU or PD). 0 PU resistor calibration 1 PD resistor calibration
11–7 ZQ_SW_PD_VAL	ZQ software pull-down resistance. This field determines the value of the PD resistor during SW ZQ calibration. 00000 Max. resistance. 11111 Min. resistance.

*Table continues on the next page...*

**MMDCx\_MPZQSWCTRL field descriptions (continued)**

Field	Description
6–2 ZQ_SW_PU_VAL	ZQ software pull-up resistance. This field determines the value of the PU resistor during SW ZQ calibration.  00000 Min. resistance. 11111 Max. resistance.
1 ZQ_SW_RES	ZQ software calibration result. This bit reflects the ZQ calibration voltage comparator value.  0 Current ZQ calibration voltage is less than VDD/2. 1 Current ZQ calibration voltage is more than VDD/2
0 ZQ_SW_FOR	ZQ SW calibration enable. This bit when asserted enables ZQ SW calibration. HW negates this bit upon completion of the ZQ SW calibration. Upon negation of this bit the ZQ SW calibration result (i.e ZQ_SW_RES) is valid

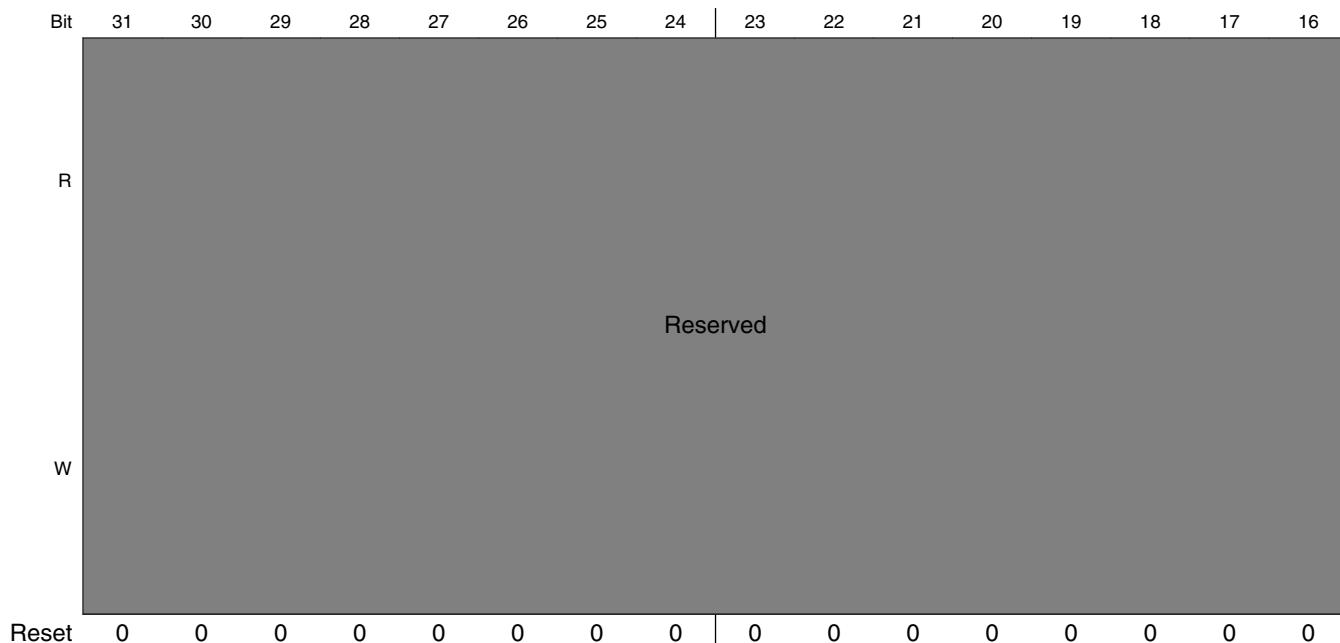
### 44.12.33 MMDC PHY Write Leveling Configuration and Error Status Register (MMDCx\_MPWLGCR)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 808h offset



Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R					WL_HW_ERR3	WL_HW_ERR2	WL_HW_ERR1	WL_HW_ERR0	WL_SW_RES3	WL_SW_RES2	WL_SW_RES1	WL_SW_RES0				
	Reserved												Reserved			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWLGCR field descriptions**

Field	Description
31–12 -	This field is reserved. Reserved
11 WL_HW_ERR3	Byte3 write-leveling HW calibration error. This bit is asserted when an error was found on byte3 during write-leveling HW calibration.  This bit is valid only upon completion of the write-leveling HW calibration (i.e HW_WL_EN bit is de-asserted)  0 No error was found on byte3 during write-leveling HW calibration. 1 An error was found on byte3 during write-leveling HW calibration.
10 WL_HW_ERR2	Byte2 write-leveling HW calibration error. This bit is asserted when an error was found on byte2 during write-leveling HW calibration.  This bit is valid only upon completion of the write-leveling HW calibration (i.e HW_WL_EN bit is de-asserted)  0 No error was found on byte2 during write-leveling HW calibration. 1 An error was found on byte2 during write-leveling HW calibration.
9 WL_HW_ERR1	Byte1 write-leveling HW calibration error. This bit is asserted when an error was found on byte1 during write-leveling HW calibration.

*Table continues on the next page...*

**MMDCx\_MPWLGCR field descriptions (continued)**

Field	Description
	<p>This bit is valid only upon completion of the write-leveling HW calibration (i.e HW_WL_EN bit is de-asserted)</p> <p>0 No error was found on byte1 during write-leveling HW calibration. 1 An error was found on byte1 during write-leveling HW calibration.</p>
8 WL_HW_ERR0	<p>Byte0 write-leveling HW calibration error. This bit is asserted when an error was found on byte0 during write-leveling HW calibration.</p> <p>This bit is valid only upon completion of the write-leveling HW calibration (i.e HW_WL_EN bit is de-asserted)</p> <p>0 No error was found on byte0 during write-leveling HW calibration. 1 An error was found on byte0 during write-leveling HW calibration.</p>
7 WL_SW_RES3	<p>Byte3 write-leveling software result. This bit reflects the value that is driven by the DDR device on DQ24 during SW write-leveling.</p> <p>0 DQS3 sampled low CK during SW write-leveling. 1 DQS3 sampled high CK during SW write-leveling.</p>
6 WL_SW_RES2	<p>Byte2 write-leveling software result. This bit reflects the value that is driven by the DDR device on DQ16 during SW write-leveling.</p> <p>0 DQS2 sampled low CK during SW write-leveling. 1 DQS2 sampled high CK during SW write-leveling.</p>
5 WL_SW_RES1	<p>Byte1 write-leveling software result. This bit reflects the value that is driven by the DDR device on DQ8 during SW write-leveling.</p> <p>0 DQS1 sampled low CK during SW write-leveling. 1 DQS1 sampled high CK during SW write-leveling.</p>
4 WL_SW_RES0	<p>Byte0 write-leveling software result. This bit reflects the value that is driven by the DDR device on DQ0 during SW write-leveling.</p> <p>0 DQS0 sampled low CK during SW write-leveling. 1 DQS0 sampled high CK during SW write-leveling.</p>
3 -	<p>This field is reserved. Reserved</p>
2 SW_WL_CNT_EN	<p>SW write-leveling count down enable. This bit when asserted set a certain delay of (25+15) cycles from the setting of SW_WL_EN and before driving the DQS to the DDR device. This bit should be asserted before the first SW write-leveling request and after issuing the write leveling MRS command</p> <p>0 MMDC doesn't count 25+15 cycles before issuing write-leveling DQS. 1 MMDC counts 25+15 cycles before issuing write-leveling DQS.</p>
1 SW_WL_EN	<p>Write-Leveling SW enable. If this bit is asserted then the MMDC will perform one write-leveling iteration with the DDR device (assuming that Write-Leveling procedure is already enabled in the DDR device through MRS command). HW negate this bit upon completion of the SW write-leveling. Negation of this bit also points that the write-leveling SW calibration result is valid</p> <p><b>NOTE:</b> If this bit and the SW_WL_CNT_EN are enabled the MMDC counts 25 + 15 cycles before issuing the SW write-leveling DQS.</p>
0 HW_WL_EN	<p>Write-Leveling HW (automatic) enable. If this bit is asserted then the MMDC will perform the whole Write-Leveling sequence with the DDR device (assuming that Write-Leveling procedure is already enabled in the DDR device through MRS command). HW negates this bit upon completion of the HW write-leveling. Negation of this bit also points that the write-leveling HW calibration results are valid</p>

*Table continues on the next page...*

**MMDCx\_MPWLGCR field descriptions (continued)**

Field	Description
	<b>NOTE:</b> Before issuing the first DQS the MMDC counts 25 + 15 cycles automatically as required by the standard.

### 44.12.34 MMDC PHY Write Leveling Delay Control Register 0 (MMDCx\_MPWLDECTRL0)

Supported Mode OF Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 80Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R				0				WL_CYC_DEL1	0							
W										WL_HC_DEL1						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0				WL_CYC_DEL0	0							
W										WL_HC_DEL0						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWLDECTRL0 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–25 WL_CYC_DEL1	<p>Write leveling cycle delay for Byte 1. This field indicates whether a delay of 1 or 2 cycles between CK and write DQS is added to the delay that is indicated in the associated WR_DL_ABS_OFFSET and WL_HC_DEL. So the total delay is the sum of (WL_DL_ABS_OFFSET/256*cycle) + (WL_HC_DEL*half cycle) + (WL_CYC_DEL*cycle).</p> <p>When both SW write-leveling is enabled (i.e SW_WL_EN = 1) or HW write-leveling is enabled (i.e HW_WL_EN = 1) then this value will be taken as is and will be added to the associated delay that is configured in WL_DL_OFFSET and WL_HC_DEL.</p> <p>Note that in HW write-leveling this field is not used for indication, as in WL_DL_OFFSET and WL_HC_DEL, but for configuration.</p> <p>0 No delay is added.</p>

*Table continues on the next page...*

**MMDCx\_MPWLDECTRL0 field descriptions (continued)**

Field	Description
	<p>1 1 cycle delay is added.      2 2 cycles delay is added.      3 Reserved.</p>
24 WL_HC_DEL1	<p>Write leveling half cycle delay for Byte 1. This field indicates whether a delay of half cycle between CK and write DQS is added to the delay that is indicated in the associated WR_DL_ABS_OFFSET and WL_CYC_DEL. So the total delay is the sum of (WL_DL_ABS_OFFSET/256*cycle) + (WL_HC_DEL*half cycle) + (WL_CYC_DEL*cycle).</p> <p>When SW write-leveling is enabled (i.e SW_WL_EN = 1) then this value will be taken as is and will be added to the associated delay that is configured in WL_DL_OFFSET and WL_CYC_DEL. When HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will indicate (status) whether a delay of half cycle was added or not to the associated WL_DL_OFFSET and WL_CYC_DEL.</p> <p>0 No delay is added.      1 Half cycle delay is added.</p>
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 WL_DL_ABS_OFFSET1	<p>Absolute write-leveling delay offset for Byte 1. This field indicates the absolute delay between CK and write DQS of Byte1 with fractions of a clock period and up to half cycle. This value is process and frequency independent. The value of the delay can be calculated using the following equation  <math>(WR_DL_ABS_OFFSET1 / 256) * \text{clock period}</math></p> <p>When SW write-leveling is enabled (i.e SW_WL_EN = 1) then this value will be taken as is to the associated delay-line. When HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will indicate (status) the value that is taken to the associated delay-line at the end of the write-leveling calibration.</p> <p><b>NOTE:</b> The delay-line has a resolution that may vary between device to device, therefore in some cases an increment of the delay by 1 step may be smaller than the delay-line resolution.</p>
15–11 Reserved	This read-only field is reserved and always has the value 0.
10–9 WL_CYC_DEL0	<p>Write leveling cycle delay for Byte 0. This field indicates whether a delay of 1 or 2 cycles between CK and write DQS is added to the delay that is indicated in the associated WR_DL_ABS_OFFSET and WL_HC_DEL. So the total delay is the sum of (WL_DL_ABS_OFFSET/256*cycle) + (WL_HC_DEL*half cycle) + (WL_CYC_DEL*cycle).</p> <p>When both SW write-leveling is enabled (i.e SW_WL_EN = 1) or HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will be taken as is and will be added to the associated delay that is configured in WL_DL_OFFSET and WL_HC_DEL.</p> <p>Note that in HW write-leveling this field is not used for indication, as in WL_DL_OFFSET and WL_HC_DEL, but for configuration.</p> <p>0 No delay is added.      1 1 cycle delay is added.      2 2 cycles delay is added.      3 Reserved.</p>
8 WL_HC_DEL0	Write leveling half cycle delay for Byte 0. This field indicates whether a delay of half cycle between CK and write DQS is added to the delay that is indicated in the associated WR_DL_ABS_OFFSET and WL_CYC_DEL. So the total delay is the sum of (WL_DL_ABS_OFFSET/256*cycle) + (WL_HC_DEL*half cycle) + (WL_CYC_DEL*cycle).

*Table continues on the next page...*

**MMDCx\_MPWLDECTRL0 field descriptions (continued)**

Field	Description
	When SW write-leveling is enabled (i.e SW_WL_EN = 1) then this value will be taken as is and will be added to the associated delay that is configured in WL_DL_OFFSET and WL_CYC_DEL. When HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will indicate (status) whether a delay of half cycle was added or not to the associated WL_DL_OFFSET and WL_CYC_DEL.  0 No delay is added. 1 Half cycle delay is added.
7 Reserved	This read-only field is reserved and always has the value 0.
WL_DL_ABS_OFFSET0	Absolute write-leveling delay offset for Byte 0. This field indicates the absolute delay between CK and write DQS of Byte0 with fractions of a clock period and up to half cycle. This value is process and frequency independent. The value of the delay can be calculated using the following equation (WR_DL_ABS_OFFSET1 / 256) * clock period  When SW write-leveling is enabled (i.e SW_WL_EN = 1) then this value will be taken as is to the associated delay-line. When HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will indicate (status) the value that is taken to the associated delay-line at the end of the write-leveling calibration.  <b>NOTE:</b> The delay-line has a resolution that may vary between device to device, therefore in some cases an increment of the delay by 1 step may be smaller than the delay-line resolution.

### 44.12.35 MMDC PHY Write Leveling Delay Control Register 1 (MMDCx\_MPWLDECTRL1)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x32

Address: Base address + 810h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R					0		WL_CYC_DEL3		0							
W								WL_HC_DEL3								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R					0		WL_CYC_DEL2		0							
W								WL_HC_DEL2								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWLDECTRL1 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–25 WL_CYC_DEL3	<p>Write leveling cycle delay for Byte 3. This field indicates whether a delay of 1 or 2 cycles between CK and write DQS is added to the delay that is indicated in the associated WL_DL_ABS_OFFSET and WL_HC_DEL. So the total delay is the sum of (WL_DL_ABS_OFFSET/256*cycle) + (WL_HC_DEL*half cycle) + (WL_CYC_DEL*cycle).</p> <p>When both SW write-leveling is enabled (i.e SW_WL_EN = 1) or HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will be taken as is and will be added to the associated delay that is configured in WL_DL_OFFSET and WL_HC_DEL.</p> <p>Note that in HW write-leveling this field is not used for indication, as in WL_DL_OFFSET and WL_HC_DEL, but for configuration.</p> <ul style="list-style-type: none"> <li>0 No delay is added.</li> <li>1 1 cycle delay is added.</li> <li>2 2 cycles delay is added.</li> <li>3 Reserved.</li> </ul>
24 WL_HC_DEL3	<p>Write leveling half cycle delay for Byte 3. This field indicates whether a delay of half cycle between CK and write DQS is added to the delay that is indicated in the associated WL_DL_ABS_OFFSET and WL_CYC_DEL. So the total delay is the sum of (WL_DL_ABS_OFFSET/256*cycle) + (WL_HC_DEL*half cycle) + (WL_CYC_DEL*cycle).</p> <p>When SW write-leveling is enabled (i.e SW_WL_EN = 1) then this value will be taken as is and will be added to the associated delay that is configured in WL_DL_OFFSET and WL_CYC_DEL. When HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will indicate (status) whether a delay of half cycle was added or not to the associated WL_DL_OFFSET and WL_CYC_DEL.</p> <ul style="list-style-type: none"> <li>0 No delay is added.</li> <li>1 Half cycle delay is added.</li> </ul>
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 WL_DL_ABS_OFFSET3	<p>Absolute write-leveling delay offset for Byte 3. This field indicates the absolute delay between CK and write DQS of Byte3 with fractions of a clock period and up to half cycle. This value is process and frequency independent. The value of the delay can be calculated using the following equation  <math>(WL_DL_ABS_OFFSET3 / 256) * \text{clock period}</math></p> <p>When SW write-leveling is enabled (i.e SW_WL_EN = 1) then this value will be taken as is to the associated delay-line. When HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will indicate (status) the value that is taken to the associated delay-line at the end of the write-leveling calibration.</p> <p><b>NOTE:</b> The delay-line has a resolution that may vary between device to device, therefore in some cases an increment of the delay by 1 step may be smaller than the delay-line resolution.</p>
15–11 Reserved	This read-only field is reserved and always has the value 0.
10–9 WL_CYC_DEL2	<p>Write leveling cycle delay for Byte 2. This field indicates whether a delay of 1 or 2 cycles between CK and write DQS is added to the delay that is indicated in the associated WR_DL_ABS_OFFSET and WL_HC_DEL. So the total delay is the sum of (WL_DL_ABS_OFFSET/256*cycle) + (WL_HC_DEL*half cycle) + (WL_CYC_DEL*cycle).</p> <p>When both SW write-leveling is enabled (i.e SW_WL_EN = 1) or HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will be taken as is and will be added to the associated delay that is configured in WL_DL_OFFSET and WL_HC_DEL.</p>

*Table continues on the next page...*

**MMDCx\_MPWLDECTRL1 field descriptions (continued)**

Field	Description
	Note that in HW write-leveling this field is not used for indication, as in WL_DL_OFFSET and WL_HC_DEL, but for configuration.  0 No delay is added. 1 1 cycle delay is added. 2 2 cycles delay is added. 3 Reserved.
8 WL_HC_DEL2	Write leveling half cycle delay for Byte 2. This field indicates whether a delay of half cycle between CK and write DQS is added to the delay that is indicated in the associated WR_DL_ABS_OFFSET and WL_CYC_DEL. So the total delay is the sum of (WL_DL_ABS_OFFSET/256*cycle) + (WL_HC_DEL*half cycle) + (WL_CYC_DEL*cycle).  When SW write-leveling is enabled (i.e SW_WL_EN = 1) then this value will be taken as is and will be added to the associated delay that is configured in WL_DL_OFFSET and WL_CYC_DEL. When HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will indicate (status) whether a delay of half cycle was added or not to the associated WL_DL_OFFSET and WL_CYC_DEL.  0 No delay is added. 1 Half cycle delay is added.
7 Reserved	This read-only field is reserved and always has the value 0.
WL_DL_ABS_OFFSET2	Absolute write-leveling delay offset for Byte 2. This field indicates the absolute delay between CK and write DQS of Byte1 with fractions of a clock period and up to half cycle. This value is process and frequency independent. The value of the delay can be calculated using the following equation (WR_DL_ABS_OFFSET2 / 256) * clock period  When SW write-leveling is enabled (i.e SW_WL_EN = 1) then this value will be taken as is to the associated delay-line. When HW write-leveling is enabled (i.e HW_WL_EN = 1 ) then this value will indicate (status) the value that is taken to the associated delay-line at the end of the write-leveling calibration.  <b>NOTE:</b> The delay-line has a resolution that may vary between device to device, therefore in some cases an increment of the delay by 1 step may be smaller than the delay-line resolution.

**44.12.36 MMDC PHY Write Leveling delay-line Status Register (MMDCx\_MPWLDSL)**

This register holds the status of the four write leveling delay-lines.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

## MMDC Memory Map/Register Definition

Address: Base address + 814h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									WL_DL_UNIT_NUM3					WL_DL_UNIT_NUM2		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									WL_DL_UNIT_NUM1				WL_DL_UNIT_NUM0			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MPWLDLST field descriptions

Field	Description
31 -	This field is reserved. Reserved
30–24 WL_DL_UNIT_NUM3	This field reflects the number of delay units that are actually used by write leveling delay-line 3.
23 -	This field is reserved. Reserved

Table continues on the next page...

**MMDCx\_MPWLDLST field descriptions (continued)**

Field	Description
22–16 WL_DL_UNIT_NUM2	This field reflects the number of delay units that are actually used by write leveling delay-line 2.
15 -	This field is reserved. Reserved
14–8 WL_DL_UNIT_NUM1	This field reflects the number of delay units that are actually used by write leveling delay-line 1.
7 -	This field is reserved. Reserved
WL_DL_UNIT_NUM0	This field reflects the number of delay units that are actually used by write leveling delay-line 0.

### 44.12.37 MMDC PHY ODT control register (MMDCx\_MPODTCTRL)

#### NOTE

In LPDDR2 mode this register should be cleared, so no termination will be activated

Supported Mode Of Operations:

For Channel 0: DDR3\_x16, DDR3\_x32, DDR3\_x64

For Channel 1: DDR3\_x64

Address: Base address + 818h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																ODT3_INT_RES
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				0				0					ODT_RD_ACT_EN	ODT_WR_ACT_EN	ODT_WR_PAS_EN
W														0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPODTCTRL field descriptions**

<b>Field</b>	<b>Description</b>
31–19 Reserved	This read-only field is reserved and always has the value 0.
18–16 ODT3_INT_RES	On chip ODT byte3 resistor - This field determines the Rtt_Nom of the on chip ODT byte3 resistor during read accesses.  000 Rtt_Nom Disabled. 001 Rtt_Nom 120 Ohm 010 Rtt_Nom 60 Ohm 011 Rtt_Nom 40 Ohm 100 Rtt_Nom 30 Ohm 101 Rtt_Nom 24 Ohm 110 Rtt_Nom 20 Ohm 111 Rtt_Nom 17 Ohm
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 ODT2_INT_RES	On chip ODT byte2 resistor - This field determines the Rtt_Nom of the on chip ODT byte2 resistor during read accesses.  000 Rtt_Nom Disabled. 001 Rtt_Nom 120 Ohm 010 Rtt_Nom 60 Ohm 011 Rtt_Nom 40 Ohm 100 Rtt_Nom 30 Ohm 101 Rtt_Nom 24 Ohm 110 Rtt_Nom 20 Ohm 111 Rtt_Nom 17 Ohm
11 Reserved	This read-only field is reserved and always has the value 0.
10–8 ODT1_INT_RES	On chip ODT byte1 resistor - This field determines the Rtt_Nom of the on chip ODT byte1 resistor during read accesses.  0000 Rtt_Nom Disabled. 001 Rtt_Nom 120 Ohm 010 Rtt_Nom 60 Ohm 011 Rtt_Nom 40 Ohm 100 Rtt_Nom 30 Ohm 101 Rtt_Nom 24 Ohm 110 Rtt_Nom 20 Ohm 111 Rtt_Nom 17 Ohm
7 Reserved	This read-only field is reserved and always has the value 0.
6–4 ODT0_INT_RES	On chip ODT byte0 resistor - This field determines the Rtt_Nom of the on chip ODT byte0 resistor during read accesses.  000 Rtt_Nom Disabled. 001 Rtt_Nom 120 Ohm 010 Rtt_Nom 60 Ohm 011 Rtt_Nom 40 Ohm

*Table continues on the next page...*

**MMDCx\_MPODTCTRL field descriptions (continued)**

Field	Description
	100 Rtt_Nom 30 Ohm 101 Rtt_Nom 24 Ohm 110 Rtt_Nom 20 Ohm 111 Rtt_Nom 17 Ohm
3 ODT_RD_ACT_EN	Active read CS ODT enable. The bit determines if ODT pin of the active CS will be asserted during read accesses. 0 Active CS ODT pin is disabled during read access. 1 Active CS ODT pin is enabled during read access.
2 ODT_RD_PAS_EN	Inactive read CS ODT enable. The bit determines if ODT pin of the inactive CS will be asserted during read accesses. 0 Inactive CS ODT pin is disabled during read accesses to other CS. 1 Inactive CS ODT pin is enabled during read accesses to other CS.
1 ODT_WR_ACT_EN	Active write CS ODT enable. The bit determines if ODT pin of the active CS will be asserted during write accesses. 0 Active CS ODT pin is disabled during write access. 1 Active CS ODT pin is enabled during write access.
0 ODT_WR_PAS_EN	Inactive write CS ODT enable. The bit determines if ODT pin of the inactive CS will be asserted during write accesses. 0 Inactive CS ODT pin is disabled during write accesses to other CS. 1 Inactive CS ODT pin is enabled during write accesses to other CS.

### 44.12.38 MMDC PHY Read DQ Byte0 Delay Register (MMDCx\_MPRDDQBY0DL)

This register is used to add fine-tuning adjustment to every bit in the read DQ byte0 relative to the read DQS. This delay is in addition to the read data calibration. If operating in 64-bit mode, there is an identical register that is mapped at the second base address.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 81Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0			rd_dq7_del	0			rd_dq6_del	0		rd_dq5_del	0		rd_dq4_del		
W																

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

## MMDC Memory Map/Register Definition

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				0				0			rd_dq1_del	0			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

## MMDCx\_MPRDDQBY0DL field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–28 rd_dq7_del	Read dqs0 to dq7 delay fine-tuning. This field holds the number of delay units that are added to dq7 relative to dqs0.  000 No change in dq7 delay 001 Add dq7 delay of 1 delay unit 010 Add dq7 delay of 2 delay units. 011 Add dq7 delay of 3 delay units. 100 Add dq7 delay of 4 delay units. 101 Add dq7 delay of 5 delay units. 110 Add dq7 delay of 6 delay units. 111 Add dq7 delay of 7 delay units.
27 Reserved	This read-only field is reserved and always has the value 0.
26–24 rd_dq6_del	Read dqs0 to dq6 delay fine-tuning. This field holds the number of delay units that are added to dq6 relative to dqs0.  000 No change in dq6 delay 001 Add dq6 delay of 1 delay unit 010 Add dq6 delay of 2 delay units. 011 Add dq6 delay of 3 delay units. 100 Add dq6 delay of 4 delay units. 101 Add dq6 delay of 5 delay units. 110 Add dq6 delay of 6 delay units. 111 Add dq6 delay of 7 delay units.
23 Reserved	This read-only field is reserved and always has the value 0.
22–20 rd_dq5_del	Read dqs0 to dq5 delay fine-tuning. This field holds the number of delay units that are added to dq5 relative to dqs0.  000 No change in dq5 delay 001 Add dq5 delay of 1 delay unit 010 Add dq5 delay of 2 delay units. 011 Add dq5 delay of 3 delay units. 100 Add dq5 delay of 4 delay units. 101 Add dq5 delay of 5 delay units. 110 Add dq5 delay of 6 delay units. 111 Add dq5 delay of 7 delay units.
19 Reserved	This read-only field is reserved and always has the value 0.

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**MMDCx\_MPRDDQBY0DL field descriptions (continued)**

Field	Description
18–16 rd_dq4_del	Read dqs0 to dq4 delay fine-tuning. This field holds the number of delay units that are added to dq4 relative to dqs0.  000 No change in dq4 delay 001 Add dq4 delay of 1 delay unit 010 Add dq4 delay of 2 delay units. 011 Add dq4 delay of 3 delay units. 100 Add dq4 delay of 4 delay units. 101 Add dq4 delay of 5 delay units. 110 Add dq4 delay of 6 delay units. 111 Add dq4 delay of 7 delay units.
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 rd_dq3_del	Read dqs0 to dq3 delay fine-tuning. This field holds the number of delay units that are added to dq3 relative to dqs0.  000 No change in dq3 delay 001 Add dq3 delay of 1 delay unit 010 Add dq3 delay of 2 delay units. 011 Add dq3 delay of 3 delay units. 100 Add dq3 delay of 4 delay units. 101 Add dq3 delay of 5 delay units. 110 Add dq3 delay of 6 delay units. 111 Add dq3 delay of 7 delay units.
11 Reserved	This read-only field is reserved and always has the value 0.
10–8 rd_dq2_del	Read dqs0 to dq2 delay fine-tuning. This field holds the number of delay units that are added to dq2 relative to dqs0.  000 No change in dq2 delay 001 Add dq2 delay of 1 delay unit 010 Add dq2 delay of 2 delay units. 011 Add dq2 delay of 3 delay units. 100 Add dq2 delay of 4 delay units. 101 Add dq2 delay of 5 delay units. 110 Add dq2 delay of 6 delay units. 111 Add dq2 delay of 7 delay units.
7 Reserved	This read-only field is reserved and always has the value 0.
6–4 rd_dq1_del	Read dqs0 to dq1 delay fine-tuning. This field holds the number of delay units that are added to dq1 relative to dqs0.  000 No change in dq1 delay 001 Add dq1 delay of 1 delay unit 010 Add dq1 delay of 2 delay units. 011 Add dq1 delay of 3 delay units. 100 Add dq1 delay of 4 delay units. 101 Add dq1 delay of 5 delay units.

*Table continues on the next page...*

**MMDCx\_MPRDDQBY0DL field descriptions (continued)**

Field	Description
	110 Add dq1 delay of 6 delay units. 111 Add dq1 delay of 7 delay units.
3 Reserved	This read-only field is reserved and always has the value 0.
rd_dq0_del	Read dqs0 to dq0 delay fine-tuning. This field holds the number of delay units that are added to dq0 relative to dqs0.  000 No change in dq0 delay 001 Add dq0 delay of 1 delay unit 010 Add dq0 delay of 2 delay units. 011 Add dq0 delay of 3 delay units. 100 Add dq0 delay of 4 delay units. 101 Add dq0 delay of 5 delay units. 110 Add dq0 delay of 6 delay units. 111 Add dq0 delay of 7 delay units.

### 44.12.39 MMDC PHY Read DQ Byte1 Delay Register (MMDCx\_MPRDDQBY1DL)

This register is used to add fine-tuning adjustment to every bit in the read DQ byte1 relative to the read DQS

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 820h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0				rd_dq15_del	0			0			rd_dq13_del	0		rd_dq12_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				rd_dq11_del	0			0			rd_dq9_del	0		rd_dq8_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPRDDQBY1DL field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**MMDCx\_MPRDDQBY1DL field descriptions (continued)**

Field	Description
30–28 rd_dq15_del	Read dqs1 to dq15 delay fine-tuning. This field holds the number of delay units that are added to dq15 relative to dqs1.  000 No change in dq15 delay 001 Add dq15 delay of 1 delay unit 010 Add dq15 delay of 2 delay units. 011 Add dq15 delay of 3 delay units. 100 Add dq15 delay of 4 delay units. 101 Add dq15 delay of 5 delay units. 110 Add dq15 delay of 6 delay units. 111 Add dq15 delay of 7 delay units.
27 Reserved	This read-only field is reserved and always has the value 0.
26–24 rd_dq14_del	Read dqs1 to dq14 delay fine-tuning. This field holds the number of delay units that are added to dq14 relative to dqs1.  000 No change in dq14 delay 001 Add dq14 delay of 1 delay unit 010 Add dq14 delay of 2 delay units. 011 Add dq14 delay of 3 delay units. 100 Add dq14 delay of 4 delay units. 101 Add dq14 delay of 5 delay units. 110 Add dq14 delay of 6 delay units. 111 Add dq14 delay of 7 delay units.
23 Reserved	This read-only field is reserved and always has the value 0.
22–20 rd_dq13_del	Read dqs1 to dq13 delay fine-tuning. This field holds the number of delay units that are added to dq13 relative to dqs1.  000 No change in dq13 delay 001 Add dq13 delay of 1 delay unit 010 Add dq13 delay of 2 delay units. 011 Add dq13 delay of 3 delay units. 100 Add dq13 delay of 4 delay units. 101 Add dq13 delay of 5 delay units. 110 Add dq13 delay of 6 delay units. 111 Add dq13 delay of 7 delay units.
19 Reserved	This read-only field is reserved and always has the value 0.
18–16 rd_dq12_del	Read dqs1 to dq12 delay fine-tuning. This field holds the number of delay units that are added to dq12 relative to dqs1.  000 No change in dq12 delay 001 Add dq12 delay of 1 delay unit 010 Add dq12 delay of 2 delay units. 011 Add dq12 delay of 3 delay units. 100 Add dq12 delay of 4 delay units. 101 Add dq12 delay of 5 delay units.

*Table continues on the next page...*

**MMDCx\_MPRDDQBY1DL field descriptions (continued)**

Field	Description
	110 Add dq12 delay of 6 delay units. 111 Add dq12 delay of 7 delay units.
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 rd_dq11_del	Read dqs1 to dq11 delay fine-tuning. This field holds the number of delay units that are added to dq11 relative to dqs1.  000 No change in dq11 delay 001 Add dq11 delay of 1 delay unit 010 Add dq11 delay of 2 delay units. 011 Add dq11 delay of 3 delay units. 100 Add dq11 delay of 4 delay units. 101 Add dq11 delay of 5 delay units. 110 Add dq11 delay of 6 delay units. 111 Add dq11 delay of 7 delay units.
11 Reserved	This read-only field is reserved and always has the value 0.
10–8 rd_dq10_del	Read dqs1 to dq10 delay fine-tuning. This field holds the number of delay units that are added to dq10 relative to dqs1.  000 No change in dq10 delay 001 Add dq10 delay of 1 delay unit 010 Add dq10 delay of 2 delay units. 011 Add dq10 delay of 3 delay units. 100 Add dq10 delay of 4 delay units. 101 Add dq10 delay of 5 delay unit 110 Add dq10 delay of 6 delay units. 111 Add dq10 delay of 7 delay units.
7 Reserved	This read-only field is reserved and always has the value 0.
6–4 rd_dq9_del	Read dqs1 to dq9 delay fine-tuning. This field holds the number of delay units that are added to dq9 relative to dqs1.  000 No change in dq9 delay 001 Add dq9 delay of 1 delay unit 010 Add dq9 delay of 2 delay units. 011 Add dq9 delay of 3 delay units. 100 Add dq9 delay of 4 delay units. 101 Add dq9 delay of 5 delay units. 110 Add dq9 delay of 6 delay units. 111 Add dq9 delay of 7 delay units.
3 Reserved	This read-only field is reserved and always has the value 0.
rd_dq8_del	Read dqs1 to dq8 delay fine-tuning. This field holds the number of delay units that are added to dq8 relative to dqs1.  000 No change in dq8 delay 001 Add dq8 delay of 1 delay unit

*Table continues on the next page...*

**MMDCx\_MPRDDQBY1DL field descriptions (continued)**

Field	Description
	010 Add dq8 delay of 2 delay units. 011 Add dq8 delay of 3 delay units. 100 Add dq8 delay of 4 delay units. 101 Add dq8 delay of 5 delay units. 110 Add dq8 delay of 6 delay units. 111 Add dq8 delay of 7 delay units.

#### 44.12.40 MMDC PHY Read DQ Byte2 Delay Register (MMDCx\_MPRDDQBY2DL)

This register is used to add fine-tuning adjustment to every bit in the read DQ byte2 relative to the read DQS

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x32

Address: Base address + 824h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0				rd_dq23_del	0			0		rd_dq21_del	0		rd_dq20_del		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				rd_dq19_del	0			0		rd_dq17_del	0		rd_dq16_del		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPRDDQBY2DL field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–28 rd_dq23_del	Read dqs2 to dq23 delay fine-tuning. This field holds the number of delay units that are added to dq23 relative to dqs2.  000 No change in dq23 delay 001 Add dq23 delay of 1 delay unit 010 Add dq23 delay of 2 delay units. 011 Add dq23 delay of 3 delay units. 100 Add dq23 delay of 4 delay units. 101 Add dq23 delay of 5 delay units.

Table continues on the next page...

**MMDCx\_MPRDDQBY2DL field descriptions (continued)**

Field	Description
	110 Add dq23 delay of 6 delay units. 111 Add dq23 delay of 7 delay units.
27 Reserved	This read-only field is reserved and always has the value 0.
26–24 rd_dq22_del	Read dqs2 to dq22 delay fine-tuning. This field holds the number of delay units that are added to dq22 relative to dqs2.  000 No change in dq22 delay 001 Add dq22 delay of 1 delay unit 010 Add dq22 delay of 2 delay units. 011 Add dq22 delay of 3 delay units. 100 Add dq22 delay of 4 delay units. 101 Add dq22 delay of 5 delay units. 110 Add dq22 delay of 6 delay units. 111 Add dq22 delay of 7 delay units.
23 Reserved	This read-only field is reserved and always has the value 0.
22–20 rd_dq21_del	Read dqs2 to dq21 delay fine-tuning. This field holds the number of delay units that are added to dq21 relative to dqs2.  000 No change in dq21 delay 001 Add dq21 delay of 1 delay unit 010 Add dq21 delay of 2 delay units. 011 Add dq21 delay of 3 delay units. 100 Add dq21 delay of 4 delay units. 101 Add dq21 delay of 5 delay units. 110 Add dq21 delay of 6 delay units. 111 Add dq21 delay of 7 delay units.
19 Reserved	This read-only field is reserved and always has the value 0.
18–16 rd_dq20_del	Read dqs2 to dq20 delay fine-tuning. This field holds the number of delay units that are added to dq20 relative to dqs2.  000 No change in dq20 delay 001 Add dq20 delay of 1 delay unit 010 Add dq20 delay of 2 delay units. 011 Add dq20 delay of 3 delay units. 100 Add dq20 delay of 4 delay units. 101 Add dq20 delay of 5 delay units. 110 Add dq20 delay of 6 delay units. 111 Add dq20 delay of 7 delay units.
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 rd_dq19_del	Read dqs2 to dq19 delay fine-tuning. This field holds the number of delay units that are added to dq19 relative to dqs2.  000 No change in dq19 delay 001 Add dq19 delay of 1 delay unit

*Table continues on the next page...*

**MMDCx\_MPRDDQBY2DL field descriptions (continued)**

Field	Description
	010 Add dq19 delay of 2 delay units. 011 Add dq19 delay of 3 delay units. 100 Add dq19 delay of 4 delay units. 101 Add dq19 delay of 5 delay units. 110 Add dq19 delay of 6 delay units. 111 Add dq19 delay of 7 delay units.
11 Reserved	This read-only field is reserved and always has the value 0.
10–8 rd_dq18_del	Read dqs2 to dq18 delay fine-tuning. This field holds the number of delay units that are added to dq18 relative to dqs2.  000 No change in dq18 delay 001 Add dq18 delay of 1 delay unit 010 Add dq18 delay of 2 delay units. 011 Add dq18 delay of 3 delay units. 100 Add dq18 delay of 4 delay units. 101 Add dq18 delay of 5 delay units. 110 Add dq18 delay of 6 delay units. 111 Add dq18 delay of 7 delay units.
7 Reserved	This read-only field is reserved and always has the value 0.
6–4 rd_dq17_del	Read dqs2 to dq17 delay fine-tuning. This field holds the number of delay units that are added to dq17 relative to dqs2.  000 No change in dq17 delay 001 Add dq17 delay of 1 delay unit 010 Add dq17 delay of 2 delay units. 011 Add dq17 delay of 3 delay units. 100 Add dq17 delay of 4 delay units. 101 Add dq17 delay of 5 delay units. 110 Add dq17 delay of 6 delay units. 111 Add dq17 delay of 7 delay units.
3 Reserved	This read-only field is reserved and always has the value 0.
rd_dq16_del	Read dqs2 to dq16 delay fine-tuning. This field holds the number of delay units that are added to dq16 relative to dqs2.  000 No change in dq16 delay 001 Add dq16 delay of 1 delay unit 010 Add dq16 delay of 2 delay units. 011 Add dq16 delay of 3 delay units. 100 Add dq16 delay of 4 delay units. 101 Add dq16 delay of 5 delay units. 110 Add dq16 delay of 6 delay units. 111 Add dq16 delay of 7 delay units.

#### 44.12.41 MMDC PHY Read DQ Byte3 Delay Register (MMDCx\_MPRDDQBY3DL)

This register is used to add fine-tuning adjustment to every bit in the read DQ byte3 relative to the read DQS.

The bit assignments and the bit field descriptions for the register are shown below.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x32

Address: Base address + 828h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0				0				0				0			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				0				0				0			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### MMDCx\_MPRDDQBY3DL field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–28 rd_dq31_del	Read dqs3 to dq31 delay fine-tuning. This field holds the number of delay units that are added to dq31 relative to dqs3.  000 No change in dq31 delay 001 Add dq31 delay of 1 delay unit 010 Add dq31 delay of 2 delay units. 011 Add dq31 delay of 3 delay units. 100 Add dq31 delay of 4 delay units. 101 Add dq31 delay of 5 delay units. 110 Add dq31 delay of 6 delay units. 111 Add dq31 delay of 7 delay units.
27 Reserved	This read-only field is reserved and always has the value 0.
26–24 rd_dq30_del	Read dqs3 to dq30 delay fine-tuning. This field holds the number of delay units that are added to dq30 relative to dqs3.  000 No change in dq30 delay 001 Add dq30 delay of 1 delay unit 010 Add dq30 delay of 2 delay units.

Table continues on the next page...

**MMDCx\_MPRDDQBY3DL field descriptions (continued)**

Field	Description
	011 Add dq30 delay of 3 delay units. 100 Add dq30 delay of 4 delay units. 101 Add dq30 delay of 5 delay units. 110 Add dq30 delay of 6 delay units. 111 Add dq30 delay of 7 delay units.
23 Reserved	This read-only field is reserved and always has the value 0.
22–20 rd_dq29_del	Read dqs3 to dq29 delay fine-tuning. This field holds the number of delay units that are added to dq29 relative to dqs3.  000 No change in dq29 delay 001 Add dq29 delay of 1 delay unit 010 Add dq29 delay of 2 delay units. 011 Add dq29 delay of 3 delay units. 100 Add dq29 delay of 4 delay units. 101 Add dq29 delay of 5 delay units. 110 Add dq29 delay of 6 delay units. 111 Add dq29 delay of 7 delay units.
19 Reserved	This read-only field is reserved and always has the value 0.
18–16 rd_dq28_del	Read dqs3 to dq28 delay fine-tuning. This field holds the number of delay units that are added to dq28 relative to dqs3.  000 No change in dq28 delay 001 Add dq28 delay of 1 delay unit 010 Add dq28 delay of 2 delay units. 011 Add dq28 delay of 3 delay units. 100 Add dq28 delay of 4 delay units. 101 Add dq28 delay of 5 delay units. 110 Add dq28 delay of 6 delay units. 111 Add dq28 delay of 7 delay units.
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 rd_dq27_del	Read dqs3 to dq27 delay fine-tuning. This field holds the number of delay units that are added to dq27 relative to dqs3.  000 No change in dq27 delay 001 Add dq27 delay of 1 delay unit 010 Add dq27 delay of 2 delay units. 011 Add dq27 delay of 3 delay units. 100 Add dq27 delay of 4 delay units. 101 Add dq27 delay of 5 delay units. 110 Add dq27 delay of 6 delay units. 111 Add dq27 delay of 7 delay units.
11 Reserved	This read-only field is reserved and always has the value 0.
10–8 rd_dq26_del	Read dqs3 to dq26 delay fine-tuning. This field holds the number of delay units that are added to dq26 relative to dqs3.

*Table continues on the next page...*

**MMDCx\_MPRDDQBY3DL field descriptions (continued)**

Field	Description
	000 No change in dq26 delay 001 Add dq26 delay of 1 delay unit 010 Add dq26 delay of 2 delay units. 011 Add dq26 delay of 3 delay units. 100 Add dq26 delay of 4 delay units. 101 Add dq26 delay of 5 delay units. 110 Add dq26 delay of 6 delay units. 111 Add dq26 delay of 7 delay units.
7 Reserved	This read-only field is reserved and always has the value 0.
6–4 rd_dq25_del	Read dqs3 to dq25 delay fine-tuning. This field holds the number of delay units that are added to dq25 relative to dqs3.  000 No change in dq25 delay 001 Add dq25 delay of 1 delay unit 010 Add dq25 delay of 2 delay units. 011 Add dq25 delay of 3 delay units. 100 Add dq25 delay of 4 delay units. 101 Add dq25 delay of 5 delay units. 110 Add dq25 delay of 6 delay units. 111 Add dq25 delay of 7 delay units.
3 Reserved	This read-only field is reserved and always has the value 0.
rd_dq24_del	Read dqs3 to dq24 delay fine-tuning. This field holds the number of delay units that are added to dq24 relative to dqs3.  000 No change in dq24 delay 001 Add dq24 delay of 1 delay unit 010 Add dq24 delay of 2 delay units. 011 Add dq24 delay of 3 delay units. 100 Add dq24 delay of 4 delay units. 101 Add dq24 delay of 5 delay units. 110 Add dq24 delay of 6 delay units. 111 Add dq24 delay of 7 delay units.

#### **44.12.42 MMDC PHY Write DQ Byte0 Delay Register (MMDCx\_MPWRDQBY0DL)**

This register is used to add fine-tuning adjustment to every bit in the write DQ byte0 relative to the write DQS

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 82Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			wr_dm0_del		wr_dq7_del	0		wr_dq6_del	0		wr_dq5_del	0		0	wr_dq4_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		0		wr_dq3_del	0		wr_dq2_del		0		wr_dq1_del	0		0	wr_dq0_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWRDQBY0DL field descriptions**

Field	Description
31–30 wr_dm0_del	Write dm0 delay fine-tuning. This field holds the number of delay units that are added to dm0 relative to dqs0.  00 No change in dm0 delay 01 Add dm0 delay of 1 delay unit. 10 Add dm0 delay of 2 delay units. 11 Add dm0 delay of 3 delay units.
29–28 wr_dq7_del	Write dq7 delay fine-tuning. This field holds the number of delay units that are added to dq7 relative to dqs0.  00 No change in dq7 delay 01 Add dq7 delay of 1 delay unit. 10 Add dq7 delay of 2 delay units. 11 Add dq7 delay of 3 delay units.
27–26 Reserved	This read-only field is reserved and always has the value 0.
25–24 wr_dq6_del	Write dq6 delay fine-tuning. This field holds the number of delay units that are added to dq6 relative to dqs0.  00 No change in dq6 delay 01 Add dq6 delay of 1 delay unit. 10 Add dq6 delay of 2 delay units. 11 Add dq6 delay of 3 delay units.
23–22 Reserved	This read-only field is reserved and always has the value 0.
21–20 wr_dq5_del	Write dq5 delay fine-tuning. This field holds the number of delay units that are added to dq5 relative to dqs0.  00 No change in dq5 delay 01 Add dq5 delay of 1 delay unit. 10 Add dq5 delay of 2 delay units. 11 Add dq5 delay of 3 delay units.
19–18 Reserved	This read-only field is reserved and always has the value 0.
17–16 wr_dq4_del	Write dq4 delay fine-tuning. This field holds the number of delay units that are added to dq4 relative to dqs0.  00 No change in dq4 delay

*Table continues on the next page...*

**MMDCx\_MPWRDQBY0DL field descriptions (continued)**

Field	Description
	01 Add dq4 delay of 1 delay unit.. 10 Add dq4 delay of 2 delay units. 11 Add dq4 delay of 3 delay units.
15–14 Reserved	This read-only field is reserved and always has the value 0.
13–12 wr_dq3_del	Write dq3 delay fine-tuning. This field holds the number of delay units that are added to dq3 relative to dqs0.  00 No change in dq3 delay 01 Add dq3 delay of 1 delay unit. 10 Add dq3 delay of 2 delay units. 11 Add dq3 delay of 3 delay units.
11–10 Reserved	This read-only field is reserved and always has the value 0.
9–8 wr_dq2_del	Write dq2 delay fine-tuning. This field holds the number of delay units that are added to dq2 relative to dqs0.  00 No change in dq2 delay 01 Add dq2 delay of 1 delay unit. 10 Add dq2 delay of 2 delay units. 11 Add dq2 delay of 3 delay units.
7–6 Reserved	This read-only field is reserved and always has the value 0.
5–4 wr_dq1_del	Write dq1 delay fine-tuning. This field holds the number of delay units that are added to dq1 relative to dqs0.  00 No change in dq1 delay 01 Add dq1 delay of 1 delay unit. 10 Add dq1 delay of 2 delay units. 11 Add dq1 delay of 3 delay units.
3–2 Reserved	This read-only field is reserved and always has the value 0.
wr_dq0_del	Write dq0 delay fine-tuning. This field holds the number of delay units that are added to dq0 relative to dqs0.  00 No change in dq0 delay 01 Add dq0 delay of 1 delay unit. 10 Add dq0 delay of 2 delay units. 11 Add dq0 delay of 3 delay units.

#### **44.12.43 MMDC PHY Write DQ Byte1 Delay Register (MMDCx\_MPWRDQBY1DL)**

This register is used to add fine-tuning adjustment to every bit in the write DQ byte1 relative to the write DQS

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 830h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	wr_dm1_del		wr_dq15_del		0		wr_dq14_del		0		wr_dq13_del		0		wr_dq12_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		wr_dq11_del		0		wr_dq10_del		0		wr_dq9_del		0		wr_dq8_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MPWRDQBY1DL field descriptions

Field	Description
31–30 wr_dm1_del	Write dm1 delay fine-tuning. This field holds the number of delay units that are added to dm1 relative to dqs1.  00 No change in dm1 delay 01 Add dm1 delay of 1 delay unit. 10 Add dm1 delay of 2 delay units. 11 Add dm1 delay of 3 delay units.
29–28 wr_dq15_del	Write dq15 delay fine-tuning. This field holds the number of delay units that are added to dq15 relative to dqs1.  00 No change in dq15 delay 01 Add dq15 delay of 1 delay unit. 10 Add dq15 delay of 2 delay units. 11 Add dq15 delay of 3 delay units.
27–26 Reserved	This read-only field is reserved and always has the value 0.
25–24 wr_dq14_del	Write dq14 delay fine-tuning. This field holds the number of delay units that are added to dq14 relative to dqs1.  00 No change in dq14 delay 01 Add dq14 delay of 1 delay unit. 10 Add dq14 delay of 2 delay units. 11 Add dq14 delay of 3 delay units.
23–22 Reserved	This read-only field is reserved and always has the value 0.
21–20 wr_dq13_del	Write dq13 delay fine-tuning. This field holds the number of delay units that are added to dq13 relative to dqs1.  00 No change in dq13 delay 01 Add dq13 delay of 1 delay unit. 10 Add dq13 delay of 2 delay units. 11 Add dq13 delay of 3 delay units.

Table continues on the next page...

**MMDCx\_MPWRDQBY1DL field descriptions (continued)**

Field	Description
19–18 Reserved	This read-only field is reserved and always has the value 0.
17–16 wr_dq12_del	Write dq12 delay fine-tuning. This field holds the number of delay units that are added to dq12 relative to dqs1.  00 No change in dq12 delay 01 Add dq12 delay of 1 delay unit. 10 Add dq12 delay of 2 delay units. 11 Add dq12 delay of 3 delay units.
15–14 Reserved	This read-only field is reserved and always has the value 0.
13–12 wr_dq11_del	Write dq11 delay fine-tuning. This field holds the number of delay units that are added to dq11 relative to dqs1.  00 No change in dq11 delay 01 Add dq11 delay of 1 delay unit. 10 Add dq11 delay of 2 delay units. 11 Add dq11 delay of 3 delay units.
11–10 Reserved	This read-only field is reserved and always has the value 0.
9–8 wr_dq10_del	Write dq10 delay fine-tuning. This field holds the number of delay units that are added to dq10 relative to dqs1.  00 No change in dq10 delay 01 Add dq10 delay of 1 delay unit. 10 Add dq10 delay of 2 delay units. 11 Add dq10 delay of 3 delay units.
7–6 Reserved	This read-only field is reserved and always has the value 0.
5–4 wr_dq9_del	Write dq9 delay fine-tuning. This field holds the number of delay units that are added to dq9 relative to dqs1.  00 No change in dq9 delay 01 Add dq9 delay of 1 delay unit. 10 Add dq9 delay of 2 delay units. 11 Add dq9 delay of 3 delay units.
3–2 Reserved	This read-only field is reserved and always has the value 0.
wr_dq8_del	Write dq8 delay fine-tuning. This field holds the number of delay units that are added to dq8 relative to dqs1.  00 No change in dq8 delay 01 Add dq8 delay of 1 delay unit. 10 Add dq8 delay of 2 delay units. 11 Add dq8 delay of 3 delay units.

#### 44.12.44 MMDC PHY Write DQ Byte2 Delay Register (MMDCx\_MPWRDQBY2DL)

This register is used to add fine-tuning adjustment to every bit in the write DQ byte2 relative to the write DQS

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x32

Address: Base address + 834h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	wr_dm2_del		wr_dq23_del		0		wr_dq22_del		0		wr_dq21_del		0		wr_dq20_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		wr_dq19_del		0		wr_dq18_del		0		wr_dq17_del		0		wr_dq16_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### MMDCx\_MPWRDQBY2DL field descriptions

Field	Description
31–30 wr_dm2_del	Write dm2 delay fine-tuning. This field holds the number of delay units that are added to dm2 relative to dqs2.  00 No change in dm2 delay 01 Add dm2 delay of 1 delay unit. 10 Add dm2 delay of 2 delay units. 11 Add dm2 delay of 3 delay units.
29–28 wr_dq23_del	Write dq23 delay fine tuning. This field holds the number of delay units that are added to dq23 relative to dqs2.  00 No change in dq23 delay 01 Add dq23 delay of 1 delay unit. 10 Add dq23 delay of 2 delay units. 11 Add dq23 delay of 3 delay units.
27–26 Reserved	This read-only field is reserved and always has the value 0.
25–24 wr_dq22_del	Write dq22 delay fine tuning. This field holds the number of delay units that are added to dq22 relative to dqs2.  00 No change in dq22 delay 01 Add dq22 delay of 1 delay unit. 10 Add dq22 delay of 2 delay units. 11 Add dq22 delay of 3 delay units.

Table continues on the next page...

**MMDCx\_MPWRDQBY2DL field descriptions (continued)**

Field	Description
23–22 Reserved	This read-only field is reserved and always has the value 0.
21–20 wr_dq21_del	Write dq21 delay fine tuning. This field holds the number of delay units that are added to dq21 relative to dqs2.  00 No change in dq21 delay 01 Add dq21 delay of 1 delay unit. 10 Add dq21 delay of 2 delay units. 11 Add dq21 delay of 3 delay units.
19–18 Reserved	This read-only field is reserved and always has the value 0.
17–16 wr_dq20_del	Write dq20 delay fine tuning. This field holds the number of delay units that are added to dq20 relative to dqs2.  00 No change in dq20 delay 01 Add dq20 delay of 1 delay unit. 10 Add dq20 delay of 2 delay units. 11 Add dq20 delay of 3 delay units.
15–14 Reserved	This read-only field is reserved and always has the value 0.
13–12 wr_dq19_del	Write dq19 delay fine tuning. This field holds the number of delay units that are added to dq19 relative to dqs2.  00 No change in dq19 delay 01 Add dq19 delay of 1 delay unit. 10 Add dq19 delay of 2 delay units. 11 Add dq19 delay of 3 delay units.
11–10 Reserved	This read-only field is reserved and always has the value 0.
9–8 wr_dq18_del	Write dq18 delay fine tuning. This field holds the number of delay units that are added to dq18 relative to dqs2.  00 No change in dq18 delay 01 Add dq18 delay of 1 delay unit. 10 Add dq18 delay of 2 delay units. 11 Add dq18 delay of 3 delay units.
7–6 Reserved	This read-only field is reserved and always has the value 0.
5–4 wr_dq17_del	Write dq17 delay fine tuning. This field holds the number of delay units that are added to dq17 relative to dqs2.  00 No change in dq17 delay 01 Add dq17 delay of 1 delay unit. 10 Add dq17 delay of 2 delay units. 11 Add dq17 delay of 3 delay units.
3–2 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**MMDCx\_MPWRDQBY2DL field descriptions (continued)**

Field	Description
wr_dq16_del	<p>Write dq16 delay fine tuning. This field holds the number of delay units that are added to dq16 relative to dqs2.</p> <p>00 No change in dq16 delay      01 Add dq16 delay of 1 delay unit.      10 Add dq16 delay of 2 delay units.      11 Add dq16 delay of 3 delay units.</p>

**44.12.45 MMDC PHY Write DQ Byte3 Delay Register (MMDCx\_MPWRDQBY3DL)**

This register is used to add fine-tuning adjustment to every bit in the write DQ byte3 relative to the write DQS

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x32

Address: Base address + 838h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	wr_dm3_del		wr_dq31_del		0		wr_dq30_del		0		wr_dq29_del		0		wr_dq28_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		wr_dq27_del		0		wr_dq26_del		0		wr_dq25_del		0		wr_dq24_del	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWRDQBY3DL field descriptions**

Field	Description
31–30 wr_dm3_del	<p>Write dm3 delay fine tuning. This field holds the number of delay units that are added to dm3 relative to dqs3.</p> <p>00 No change in dm3 delay      01 Add dm3 delay of 1 delay unit.      10 Add dm3 delay of 2 delay units.      11 Add dm3 delay of 3 delay units.</p>
29–28 wr_dq31_del	<p>Write dq31 delay fine tuning. This field holds the number of delay units that are added to dq31 relative to dqs3.</p> <p>00 No change in dq31 delay      01 Add dq31 delay of 1 delay unit.</p>

*Table continues on the next page...*

**MMDCx\_MPWRDQBY3DL field descriptions (continued)**

Field	Description
	10 Add dq31 delay of 2 delay units. 11 Add dq31 delay of 3 delay units.
27–26 Reserved	This read-only field is reserved and always has the value 0.
25–24 wr_dq30_del	Write dq30 delay fine tuning. This field holds the number of delay units that are added to dq30 relative to dqs3.  00 No change in dq30 delay 01 Add dq30 delay of 1 delay unit. 10 Add dq30 delay of 2 delay units. 11 Add dq30 delay of 3 delay units.
23–22 Reserved	This read-only field is reserved and always has the value 0.
21–20 wr_dq29_del	Write dq29 delay fine tuning. This field holds the number of delay units that are added to dq29 relative to dqs3.  00 No change in dq29 delay 01 Add dq29 delay of 1 delay unit. 10 Add dq29 delay of 2 delay units. 11 Add dq29 delay of 3 delay units.
19–18 Reserved	This read-only field is reserved and always has the value 0.
17–16 wr_dq28_del	Write dq28 delay fine tuning. This field holds the number of delay units that are added to dq28 relative to dqs3.  00 No change in dq28 delay 01 Add dq28 delay of 1 delay unit. 10 Add dq28 delay of 2 delay units. 11 Add dq28 delay of 3 delay units.
15–14 Reserved	This read-only field is reserved and always has the value 0.
13–12 wr_dq27_del	Write dq27 delay fine tuning. This field holds the number of delay units that are added to dq27 relative to dqs3.  00 No change in dq27 delay 01 Add dq27 delay of 1 delay unit. 10 Add dq27 delay of 2 delay units. 11 Add dq27 delay of 3 delay units.
11–10 Reserved	This read-only field is reserved and always has the value 0.
9–8 wr_dq26_del	Write dq26 delay fine tuning. This field holds the number of delay units that are added to dq26 relative to dqs3.  00 No change in dq26 delay 01 Add dq26 delay of 1 delay unit. 10 Add dq26 delay of 2 delay units. 11 Add dq26 delay of 3 delay units.

*Table continues on the next page...*

**MMDCx\_MPWRDQBY3DL field descriptions (continued)**

Field	Description
7–6 Reserved	This read-only field is reserved and always has the value 0.
5–4 wr_dq25_del	Write dq25 delay fine tuning. This field holds the number of delay units that are added to dq25 relative to dqs3.  00 No change in dq25 delay 01 Add dq25 delay of 1 delay unit. 10 Add dq25 delay of 2 delay units. 11 Add dq25 delay of 3 delay units.
3–2 Reserved	This read-only field is reserved and always has the value 0.
wr_dq24_del	Write dq24 delay fine tuning. This field holds the number of delay units that are added to dq24 relative to dqs3.  00 No change in dq24 delay 01 Add dq24 delay of 1 delay unit. 10 Add dq24 delay of 2 delay units. 11 Add dq24 delay of 3 delay units.

#### 44.12.46 MMDC PHY Read DQS Gating Control Register 0 (MMDCx\_MPDGCTRL0)

Supported Mode Of Operations:

For Channel 0: DDR3\_x16, DDR3\_x32, DDR3\_x64

For Channel 1: DDR3\_x64

Address: Base address + 83Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	RST_RD_FIFO	DG_CMP_CYC	DG_DIS	HW_DG_EN	DG_HC_DEL1	DG_EXT_UP	DG_DL_ABS_OFFSET1									
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

## MMDC Memory Map/Register Definition

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				HW_DG_ERR					0							
	0				DG_HC_DEL0							DG_DL_ABS_OFFSET0				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MPDGCTRL0 field descriptions

Field	Description
31 RST_RD_FIFO	Reset Read Data FIFO and associated pointers. If this bit is asserted then the MMDC resets the read data FIFO and the associated pointers. This bit is self cleared after the FIFO reset is done.
30 DG_CMP_CYC	Read DQS gating sample cycle. If this bit is asserted then the MMDC waits 32 cycles before comparing the read data, Otherwise it waits 16 DDR cycles. 0 MMDC waits 16 DDR cycles 1 MMDC waits 32 DDR cycles
29 DG_DIS	Read DQS gating disable. If this bit is asserted then the MMDC disables the read DQS gating mechanism. If this bits is asserted (read DQS gating is disabled) then pull-up and pull-down resistors suppose to be used on DQS and DQS# respectively 0 Read DQS gating mechanism is enabled 1 Read DQS gating mechanism is disabled
28 HW_DG_EN	Enable automatic read DQS gating calibration. If this bit is asserted then the MMDC performs automatic read DQS gating calibration. HW negates this bit upon completion of the automatic read DQS gating. Note: Before issuing the first read command the MMDC counts 12 cycles. In LPDDR2 mode automatic (HW) read DQS gating should be disabled and Pull-up/pull-down resistors on DQS/DQS# should be enabled while ODT resistors must be disconnected. 0 Disable automatic read DQS gating calibration 1 Start automatic read DQS gating calibration
27–24 DG_HC_DEL1	Read DQS gating half cycles delay for Byte1 (channel 0 register) and Byte5 in 64-bit mode (channel 1 register) . This field indicates the delay in half cycles between read DQS gate and the middle of the read DQS preamble of Byte1. This delay is added to the delay that is genearted by the read DQS1 gating delay-line, So the total read DQS gating delay is $(DG\_HC\_DEL\#)*0.5*\text{cycle} + (DG\_DL\_ABS\_OFFSET\#)*1/256*\text{cycle}$ Upon completion of the automatic read DQS gating calibration this field gets the value of the 4 MSB of $((HW\_DG\_LOW1 + HW\_DG\_UP1) / 2)$ . 0000 0 cycles delay. 0001 Half cycle delay. 0010 1 cycle delay 1101 6.5 cycles delay

Table continues on the next page...

**MMDCx\_MPDGCTRL0 field descriptions (continued)**

Field	Description
	1110 Reserved 1111 Reserved
23 DG_EXT_UP	DG extend upper boundary. By default the upper boundary of DQS gating HW calibration is set according to first failing comparison after at least one passing comparison. If this bit is asserted then the upper boundary is set according to the last passing comparison.
22–16 DG_DL_ABS_OFFSET1	Absolute read DQS gating delay offset for Byte1. This field indicates the absolute delay between read DQS gate and the middle of the read DQS preamble of Byte1 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be $(DG\_DL\_ABS\_OFFSET1 / 256) * MMDC\_CH0 AXI clock (fast clock)$ .  This field can also be written by HW. Upon completion of the automatic read DQS gating calibration this field gets the value of the 7 LSB of $((HW\_DG\_LOW1 + HW\_DG\_UP1) / 2)$ .  Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12 HW_DG_ERR	HW DQS gating error. This bit valid is asserted when an error was found during the read DQS gating HW calibration process. Error can occur when no valid value was found during HW calibration.  This bit is valid only after HW_DG_EN is de-asserted.  0 No error was found during the DQS gating HW calibration process. 1 An error was found during the DQS gating HW calibration process.
11–8 DG_HC_DEL0	Read DQS gating half cycles delay for Byte0 (Channel 0 register) and Byte4 in 64-bit mode (Channel 1 register)  . This field indicates the delay in half cycles between read DQS gate and the middle of the read DQS preamble of Byte0/4. This delay is added to the delay that is generated by the read DQS1 gating delay-line, So the total read DQS gating delay is $(DG\_HC\_DEL\#) * 0.5 * \text{cycle} + (DG\_DL\_ABS\_OFFSET\#) * 1/256 * \text{cycle}$  Upon completion of the automatic read DQS gating calibration this field gets the value of the 4 MSB of $((HW\_DG\_LOW1 + HW\_DG\_UP1) / 2)$ .  0000 0 cycles delay. 0001 Half cycle delay. 0010 1 cycle delay 1101 6.5 cycles delay 1110 Reserved 1111 Reserved
7 Reserved	This read-only field is reserved and always has the value 0.
DG_DL_ABS_OFFSET0	Absolute read DQS gating delay offset for Byte0. This field indicates the absolute delay between read DQS gate and the middle of the read DQS preamble of Byte0 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be $(DG\_DL\_ABS\_OFFSET0 / 256) * MMDC\_CH0 AXI clock (fast clock)$ .  This field can also be written by HW. Upon completion of the automatic read DQS gating calibration this field gets the value of the 7 LSB of $((HW\_DG\_LOW0 + HW\_DG\_UP0) / 2)$ .  Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.

#### 44.12.47 MMDC PHY Read DQS Gating Control Register 1 (MMDCx\_MPDGCTRL1)

Supported Mode Of Operations:

For Channel 0: DDR3\_x16, DDR3\_x32, DDR3\_x64

For Channel 1: DDR3\_x64

Address: Base address + 840h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	0				DG_HC_DEL3				0	DG_DL_ABS_OFFSET3							
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	0				DG_HC_DEL2				0	DG_DL_ABS_OFFSET2							
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### MMDCx\_MPDGCTRL1 field descriptions

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–24 DG_HC_DEL3	<p>Read DQS gating half cycles delay for Byte3 (Channel 0 register) and Byte7 for 64-bit data (Channel 1 register).</p> <p>. This field indicates the delay in half cycles between read DQS gate and the middle of the read DQS preamble of Byte3/7. This delay is added to the delay that is generated by the read DQS1 gating delay-line. So the total read DQS gating delay is <math>(DG\_HC\_DEL\#)*0.5*\text{cycle} + (DG\_DL\_ABS\_OFFSET\#)*1/256*\text{cycle}</math></p> <p>Upon completion of the automatic read DQS gating calibration this field gets the value of the 4 MSB of <math>((HW\_DG\_LOW3 + HW\_DG\_UP3) / 2)</math>.</p> <ul style="list-style-type: none"> <li>0000 0 cycles delay.</li> <li>0001 Half cycle delay.</li> <li>0010 1 cycle delay</li> <li>1101 6.5 cycles delay</li> <li>1110 Reserved</li> <li>1111 Reserved</li> </ul>
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 DG_DL_ABS_OFFSET3	<p>Absolute read DQS gating delay offset for Byte3. This field indicates the absolute delay between read DQS gate and the middle of the read DQS preamble of Byte3 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be <math>(DG\_DL\_ABS\_OFFSET3 / 256) * \text{MMDC\_CH0 AXI clock (fast clock)}</math>.</p> <p>This field can also be written by HW. Upon completion of the automatic read DQS gating calibration this field gets the value of the 7 LSB of <math>((HW\_DG\_LOW3 + HW\_DG\_UP3) / 2)</math>.</p>

Table continues on the next page...

**MMDCx\_MPDGCTRL1 field descriptions (continued)**

Field	Description
	Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.
15–12 Reserved	This read-only field is reserved and always has the value 0.
11–8 DG_HC_DEL2	<p>Read DQS gating half cycles delay for Byte2 (Channel 0 register) and Byte6 for 64-bit mode(channel 1 register)</p> <p>. This field indicates the delay in half cycles between read DQS gate and the middle of the read DQS preamble of Byte2/5. This delay is added to the delay that is generated by the read DQS1 gating delay-line, So the total read DQS gating delay is <math>(DG\_HC\_DEL\#)*0.5*\text{cycle} + (DG\_DL\_ABS\_OFFSET\#)*1/256*\text{cycle}</math></p> <p>Upon completion of the automatic read DQS gating calibration this field gets the value of the 4 MSB of <math>((HW\_DG\_LOW2 + HW\_DG\_UP2) / 2)</math>.</p> <p>0000 0 cycles delay. 0001 Half cycle delay. 0010 1 cycle delay 1101 6.5 cycles delay 1110 Reserved 1111 Reserved</p>
7 Reserved	This read-only field is reserved and always has the value 0.
DG_DL_ABS_OFFSET2	<p>Absolute read DQS gating delay offset for Byte2. This field indicates the absolute delay between read DQS gate and the middle of the read DQS preamble of Byte2 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be <math>(DG\_DL\_ABS\_OFFSET2 / 256) * MMDC\_CH0 AXI clock (fast clock)</math>.</p> <p>This field can also be written by HW. Upon completion of the automatic read DQS gating calibration this field gets the value of the 7 LSB of <math>((HW\_DG\_LOW2 + HW\_DG\_UP2) / 2)</math>.</p> <p>Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.</p>

#### 44.12.48 MMDC PHY Read DQS Gating delay-line Status Register (MMDCx\_MPDGDLST0)

This register holds the status of the 4 dqs gating delay-lines.

Supported Mode Of Operations:

For Channel 0: DDR3\_x16, DDR3\_x32, DDR3\_x64

For Channel 1: DDR3\_x64

## MMDC Memory Map/Register Definition

Address: Base address + 844h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									DG_DL_UNIT_NUM3							
	Reserved															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									DG_DL_UNIT_NUM1							
	Reserved															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MPDLST0 field descriptions

Field	Description
31 -	This field is reserved. Reserved
30–24 DG_DL_UNIT_NUM3	This field reflects the number of delay units that are actually used by read DQS gating delay-line 3.
23 -	This field is reserved. Reserved

Table continues on the next page...

**MMDCx\_MPDLST0 field descriptions (continued)**

Field	Description
22–16 DG_DL_UNIT_NUM2	This field reflects the number of delay units that are actually used by read DQS gating delay-line 2.
15 -	This field is reserved. Reserved
14–8 DG_DL_UNIT_NUM1	This field reflects the number of delay units that are actually used by read DQS gating delay-line 1.
7 -	This field is reserved. Reserved
DG_DL_UNIT_NUM0	This field reflects the number of delay units that are actually used by read DQS gating delay-line 0.

**44.12.49 MMDC PHY Read delay-lines Configuration Register (MMDCx\_MPRDDLCTL)**

This register controls read delay-lines functionality; it determines DQS delay relative to the associated DQ read access. The delay-line compensates for process variations and produces a constant delay regardless of the process, temperature and voltage.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 848h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								0							
W																
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0							
W																
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0

**MMDCx\_MPRDDLCTL field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 RD_DL_ABS_OFFSET3	Absolute read delay offset for Byte3. This field indicates the absolute delay between read DQS strobe and the read data of Byte3 with fractions of a clock period and up to half cycle. The fraction is process and

*Table continues on the next page...*

**MMDCx\_MPRDDLCTL field descriptions (continued)**

Field	Description
	<p>frequency independent. The delay of the delay-line would be <math>(RD\_DL\_ABS\_OFFSET3 / 256) * MMDC\_CH0 AXI clock (fast clock)</math>. So for the default value of 64 we get a quarter cycle delay.</p> <p>This field can also be written by HW. Upon completion of the read delay-line HW calibration this field gets the value of <math>(HW\_RD\_DL\_LOW3 + HW\_RD\_DL\_UP3) / 2</math></p> <p>Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.</p>
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 RD_DL_ABS_OFFSET2	<p>Absolute read delay offset for Byte2. This field indicates the absolute delay between read DQS strobe and the read data of Byte2 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be <math>(RD\_DL\_ABS\_OFFSET2 / 256) * MMDC\_CH0 AXI clock (fast clock)</math>. So for the default value of 64 we get a quarter cycle delay.</p> <p>This field can also be written by HW. Upon completion of the read delay-line HW calibration this field gets the value of <math>(HW\_RD\_DL\_LOW2 + HW\_RD\_DL\_UP2) / 2</math></p> <p>Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–8 RD_DL_ABS_OFFSET1	<p>Absolute read delay offset for Byte1. This field indicates the absolute delay between read DQS strobe and the read data of Byte1 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be <math>(RD\_DL\_ABS\_OFFSET1 / 256) * MMDC\_CH0 AXI clock (fast clock)</math>. So for the default value of 64 we get a quarter cycle delay.</p> <p>This field can also be written by HW. Upon completion of the read delay-line HW calibration this field gets the value of <math>(HW\_RD\_DL\_LOW1 + HW\_RD\_DL\_UP1) / 2</math></p> <p>Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.</p>
7 Reserved	This read-only field is reserved and always has the value 0.
RD_DL_ABS_OFFSET0	<p>Absolute read delay offset for Byte0. This field indicates the absolute delay between read DQS strobe and the read data of Byte0 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be <math>(RD\_DL\_ABS\_OFFSET0 / 256) * MMDC\_CH0 AXI clock (fast clock)</math>. So for the default value of 64 we get a quarter cycle delay.</p> <p>This field can also be written by HW. Upon completion of the read delay-line HW calibration this field gets the value of <math>(HW\_RD\_DL\_LOW0 + HW\_RD\_DL\_UP0) / 2</math></p> <p>Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.</p>

#### 44.12.50 MMDC PHY Read delay-lines Status Register (MMDCx\_MPRDDLST)

This register holds the status of the 4 read delay-lines.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 84Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MPDDLST field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 RD_DL_UNIT_NUM3	This field reflects the number of delay units that are actually used by read delay-line 3.
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 RD_DL_UNIT_NUM2	This field reflects the number of delay units that are actually used by read delay-line 2.
15 Reserved	This read-only field is reserved and always has the value 0.
14–8 RD_DL_UNIT_NUM1	This field reflects the number of delay units that are actually used by read delay-line 1.
7 Reserved	This read-only field is reserved and always has the value 0.
RD_DL_UNIT_NUM0	This field reflects the number of delay units that are actually used by read delay-line 0.

## 44.12.51 MMDC PHY Write delay-lines Configuration Register (MMDCx\_MPWRDLCTL)

This register controls write delay-lines functionality, it determines DQ/DM delay relative to the associated DQS in write access. The delay-line compensates for process variations, and produces a constant delay regardless of the process, temperature and voltage.

Supported Mode Of Operations:

For Channel 0: All

## MMDC Memory Map/Register Definition

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 850h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								0							
W																
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0							
W																
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0

### MMDCx\_MPWRDLCTL field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 WR_DL_ABS_OFFSET3	Absolute write delay offset for Byte3. This field indicates the absolute delay between write DQS strobe and the write data of Byte3 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be $(WR\_DL\_ABS\_OFFSET3 / 256) * MMDC\_CH0 AXI clock (fast clock)$ . So for the default value of 64 we get a quarter cycle delay.  This field can also be written by HW. Upon completion of the write delay-line HW calibration this field gets the value of $(HW\_WR\_DL\_LOW3 + HW\_WR\_DL\_UP3) / 2$  Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 WR_DL_ABS_OFFSET2	Absolute write delay offset for Byte2. This field indicates the absolute delay between write DQS strobe and the write data of Byte2 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be $(WR\_DL\_ABS\_OFFSET2 / 256) * MMDC\_CH0 AXI clock (fast clock)$ . So for the default value of 64 we get a quarter cycle delay.  This field can also be written by HW. Upon completion of the write delay-line HW calibration this field gets the value of $(HW\_WR\_DL\_LOW2 + HW\_WR\_DL\_UP2) / 2$  Note that not all changes will have effect on the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.
15 Reserved	This read-only field is reserved and always has the value 0.
14–8 WR_DL_ABS_OFFSET1	Absolute write delay offset for Byte1. This field indicates the absolute delay between write DQS strobe and the write data of Byte1 with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be $(WR\_DL\_ABS\_OFFSET1 / 256) * MMDC\_CH0 AXI clock (fast clock)$ . So for the default value of 64 we get a quarter cycle delay.  This field can also be written by HW. Upon completion of the write delay-line HW calibration this field gets the value of $(HW\_WR\_DL\_LOW1 + HW\_WR\_DL\_UP1) / 2$  Note that not all changes of this value will affect the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.
7 Reserved	This read-only field is reserved and always has the value 0.
WR_DL_ABS_OFFSET0	Absolute write delay offset for Byte0. This field indicates the absolute delay between write DQS strobe and the write data of Byte0 with fractions of a clock period and up to half cycle. The fraction is process and

Table continues on the next page...

**MMDCx\_MPWRDLCTL field descriptions (continued)**

Field	Description
	<p>frequency independent. The delay of the delay-line would be <math>(\text{WR\_DL\_ABS\_OFFSET0} / 256) * \text{MMDC\_CH0 AXI clock (fast clock)}</math>. So for the default value of 64 we get a quarter cycle delay.</p> <p>This field can also be written by HW. Upon completion of the write delay-line HW calibration this field gets the value of <math>(\text{HW\_WR\_DL\_LOW0} + \text{HW\_WR\_DL\_UP0}) / 2</math></p> <p>Note that not all changes of this value will affect the actual delay. If the requested change is smaller than the delay-line resolution, then no change will occur.</p>

### 44.12.52 MMDC PHY Write delay-lines Status Register (MMDCx\_MPWRDLST)

This register holds the status of the 4 write delay-line.

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 854h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWRDLST field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 WR_DL_UNIT_NUM3	This field reflects the number of delay units that are actually used by write delay-line 3.
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 WR_DL_UNIT_NUM2	This field reflects the number of delay units that are actually used by write delay-line 2.
15 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**MMDCx\_MPWRDLST field descriptions (continued)**

Field	Description
14–8 WR_DL_UNIT_NUM1	This field reflects the number of delay units that are actually used by write delay-line 1.
7 Reserved	This read-only field is reserved and always has the value 0.
WR_DL_UNIT_NUM0	This field reflects the number of delay units that are actually used by write delay-line 0.

**44.12.53 MMDC PHY CK Control Register (MMDCx\_MPSDCTRL)**

This register controls the fine tuning of the primary clock (CK0).

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 858h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R								0									
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R				0			SDclk0_del						0				
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**MMDCx\_MPSDCTRL field descriptions**

Field	Description
31–10 Reserved	This read-only field is reserved and always has the value 0.
9–8 SDclk0_del	DDR clock0 delay fine tuning. This field holds the number of delay units that are added to DDR clock (CK0).  Note:  In case of LPDDR2 2-ch mode this register controls the fine tuning of the clock that is driven to channel0 In case of DDR3 the fine tuning of the secondary clock is controlled by 0x021B_4858[SDCLK]  00 No change in DDR clock0 delay 01 Add DDR clock0 delay of 1 delay unit. 10 Add DDR clock0 delay of 2 delay units. 11 Add DDR clock0 delay of 3 delay units.
Reserved	This read-only field is reserved and always has the value 0.

#### 44.12.54 MMDC ZQ LPDDR2 HW Control Register (MMDCx\_MPZQLP2CTL)

This register controls the idle time that takes the LPDDR2 device to perform ZQ calibration

Supported Mode Of Operations:

For Channel 0: LP2\_2ch\_x16, LP2\_2ch\_x32

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 85Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0				ZQ_LP2_HW_ZQCS					ZQ_LP2_HW_ZQCL							
W																	
Reset	0	0	0	1	1	0	1	1		0	1	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R					0					ZQ_LP2_HW_ZQINIT							
W																	
Reset	0	0	0	0	0	0	0	1		0	0	0	0	1	0	0	1

#### MMDCx\_MPZQLP2CTL field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 ZQ_LP2_HW_ZQCS	This register defines the period in cycles that it takes the memory device to perform a Short ZQ calibration. This is the period of time that the MMDC has to wait after sending a long ZQ calibration and before sending other commands. This delay will also be used if ZQ reset is sent.  0x0-0x1A Reserved 0x1B 112 cycles (default) 0x1C 116 cycles 0x7E 508 cycles 0x7F 512 cycles
23–16 ZQ_LP2_HW_ZQCL	This register defines the period in cycles that it takes the memory device to perform a long ZQ calibration. This is the period of time that the MMDC has to wait after sending a Short ZQ calibration and before sending other commands.  0x0-0x36 Reserved 0x37 112 cycles 0x38 114 cycles 0x5F 192 cycles (Default, JEDEC value, tZQCL, for LPDDR2, 360ns @ clock frequency 533MHz) 0xFE 510 cycles 0xFF 512 cycles

Table continues on the next page...

**MMDCx\_MPZQLP2CTL field descriptions (continued)**

Field	Description												
15–9 Reserved	This read-only field is reserved and always has the value 0.												
ZQ_LP2_HW_ZQINIT	<p>This register defines the period in cycles that it takes the memory device to perform a Init ZQ calibration.</p> <p>This is the period of time that the MMDC has to wait after sending a init ZQ calibration and before sending other commands.</p> <table> <tr> <td>0x0-0x36</td> <td>Reserved</td> </tr> <tr> <td>0x37</td> <td>112 cycles</td> </tr> <tr> <td>0x38</td> <td>114 cycles</td> </tr> <tr> <td>0x109</td> <td>532 cycles (Default, JEDEC value, tZQINIT, for LPDDR2, 1us @ clock frequency 533MHz)</td> </tr> <tr> <td>0x1FE</td> <td>1022 cycles</td> </tr> <tr> <td>0x1FF</td> <td>1024 cycles</td> </tr> </table>	0x0-0x36	Reserved	0x37	112 cycles	0x38	114 cycles	0x109	532 cycles (Default, JEDEC value, tZQINIT, for LPDDR2, 1us @ clock frequency 533MHz)	0x1FE	1022 cycles	0x1FF	1024 cycles
0x0-0x36	Reserved												
0x37	112 cycles												
0x38	114 cycles												
0x109	532 cycles (Default, JEDEC value, tZQINIT, for LPDDR2, 1us @ clock frequency 533MHz)												
0x1FE	1022 cycles												
0x1FF	1024 cycles												

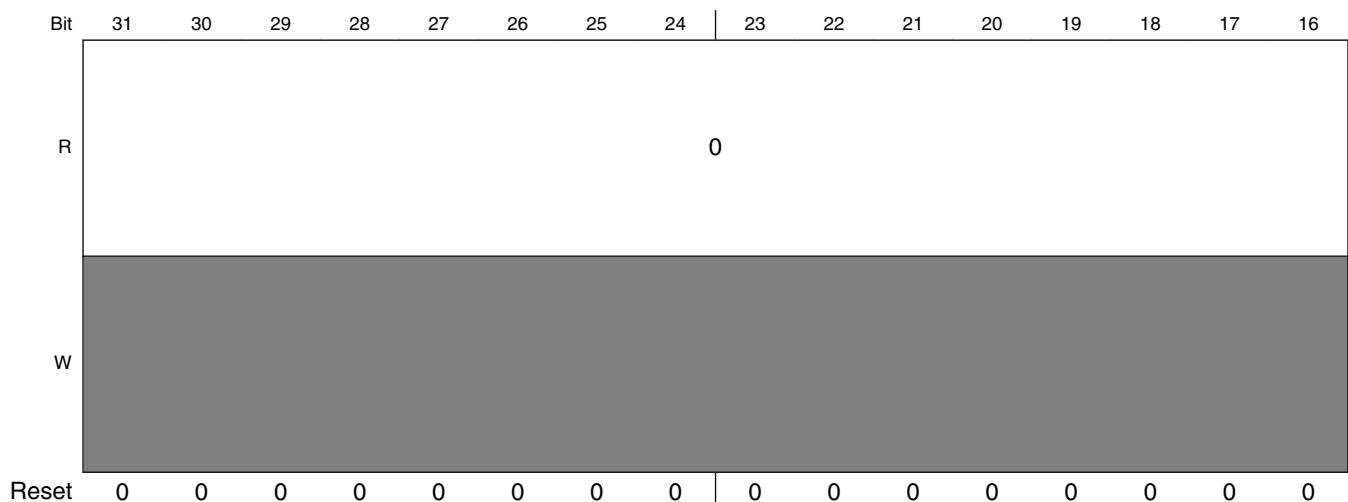
#### 44.12.55 MMDC PHY Read Delay HW Calibration Control Register (MMDCx\_MPRDDLHWCTL)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 860h offset



Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R								0								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPRDDLHWCTL field descriptions**

Field	Description
31–6 Reserved	This read-only field is reserved and always has the value 0.
5 HW_RD_DL_CMP_CYC	Automatic (HW) read sample cycle. If this bit is asserted then the MMDC will compare the read data 32 cycles after the MMDC sent the read command enable pulse else it compares the data after 16 cycles.
4 HW_RD_DL_EN	Enable automatic (HW) read calibration. If this bit is asserted then the MMDC will perform an automatic read calibration. HW should negate this bit upon completion of the calibration. Negation of this bit also points that the read calibration results are valid  Note: Before issuing the first read command MMDC counts 12 cycles.
3 HW_RD_DL_ERR3	Automatic (HW) read calibration error of Byte3. If this bit is asserted then it indicates that an error was found during the HW calibration process of read delay-line 3. In case this bit is zero at the end of the calibration process then the boundary results can be found at MPRDDLHWST1 register. This bit is valid only after HW_RD_DL_EN is de-asserted.  0 No error was found in read delay-line 3 during the automatic (HW) read calibration process of read delay-line 3. 1 An error was found in read delay-line 3 during the automatic (HW) read calibration process of read delay-line 3.
2 HW_RD_DL_ERR2	Automatic (HW) read calibration error of Byte2. If this bit is asserted then it indicates that an error was found during the HW calibration process of read delay-line 2. In case this bit is zero at the end of the calibration process then the boundary results can be found at MPRDDLHWST1 register. This bit is valid only after HW_RD_DL_EN is de-asserted.

Table continues on the next page...

**MMDCx\_MPRDDLHWCTL field descriptions (continued)**

Field	Description
	<ul style="list-style-type: none"> <li>0 No error was found in read delay-line 2 during the automatic (HW) read calibration process of read delay-line 2.</li> <li>1 An error was found in read delay-line 2 during the automatic (HW) read calibration process of read delay-line 2.</li> </ul>
1 HW_RD_DL_ERR1	<p>Automatic (HW) read calibration error of Byte1. If this bit is asserted then it indicates that an error was found during the HW calibration process of read delay-line 1. In case this bit is zero at the end of the calibration process then the boundary results can be found at MPRDDLHWST0 register. This bit is valid only after HW_RD_DL_EN is de-asserted.</p> <ul style="list-style-type: none"> <li>0 No error was found in read delay-line 1 during the automatic (HW) read calibration process of read delay-line 1.</li> <li>1 An error was found in read delay-line 1 during the automatic (HW) read calibration process of read delay-line 1.</li> </ul>
0 HW_RD_DL_ERR0	<p>Automatic (HW) read calibration error of Byte0. If this bit is asserted then it indicates that an error was found during the HW calibration process of read delay-line 0. In case this bit is zero at the end of the calibration process then the boundary results can be found at MPRDDLHWST0 register. This bit is valid only after HW_RD_DL_EN is de-asserted.</p> <ul style="list-style-type: none"> <li>0 No error was found in read delay-line 0 during the automatic (HW) read calibration process of read delay-line 0.</li> <li>1 An error was found in read delay-line 0 during the automatic (HW) read calibration process of read delay-line 0.</li> </ul>

#### 44.12.56 MMDC PHY Write Delay HW Calibration Control Register (MMDCx\_MPWRDLHWCTL)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 864h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R										0						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R								0					HW_WR_DL_CMP_CYC	HW_WR_DL_EN	HW_WR_DL_EN	HW_WR_DL_EN
W													HW_WR_DL_EN			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWRDLHWCTL field descriptions**

Field	Description
31–6 Reserved	This read-only field is reserved and always has the value 0.
5 HW_WR_DL_CMP_CYC	Write sample cycle. If this bit is asserted then the MMDC will compare the data 32 cycles after the MMDC sent the read command enable pulse else it compares the data after 16 cycles.
4 HW_WR_DL_EN	Enable automatic (HW) write calibration. If this bit is asserted then the MMDC will perform an automatic write calibration. HW should negate this bit upon completion of the calibration. Negation of this bit also indicates that the write calibration results are valid  Note: Before issuing the first read command MMDC counts 12 cycles.
3 HW_WR_DL_ERR3	Automatic (HW) write calibration error of Byte3. If this bit is asserted then it indicates that an error was found during the HW calibration process of write delay-line 3. In case this bit is zero at the end of the calibration process then the boundary results can be found at MPWRDLHWST1 register. This bit is valid only after HW_WR_DL_EN is de-asserted.  0 No error was found during the automatic (HW) write calibration process of write delay-line 3. 1 An error was found during the automatic (HW) write calibration process of write delay-line 3.
2 HW_WR_DL_ERR2	Automatic (HW) write calibration error of Byte2. If this bit is asserted then it indicates that an error was found during the HW calibration process of write delay-line 2. T In case this bit is zero at the end of the calibration process then the boundary results can be found at MPWRDLHWST1 register. This bit is valid only after HW_WR_DL_EN is de-asserted.  0 No error was found during the automatic (HW) write calibration process of write delay-line 2. 1 An error was found during the automatic (HW) write calibration process of write delay-line 2.
1 HW_WR_DL_ERR1	Automatic (HW) write calibration error of Byte1. If this bit is asserted then it indicates that an error was found during the HW calibration process of write delay-line 1. In case this bit is zero at the end of the calibration process then the boundary results can be found at MPWRDLHWST0 register. This bit is valid only after HW_WR_DL_EN is de-asserted.  0 No error was found during the automatic (HW) write calibration process of write delay-line 1. 1 An error was found during the automatic (HW) write calibration process of write delay-line 1.
0 HW_WR_DL_ERR0	Automatic (HW) write calibration error of Byte0. If this bit is asserted then it indicates that an error was found during the HW calibration process of write delay-line 0. In case this bit is zero at the end of the

*Table continues on the next page...*

**MMDCx\_MPWRDLHWCTL field descriptions (continued)**

Field	Description
	<p>calibration process then the boundary results can be found at MPWRDLHWST0 register. This bit is valid only after HW_WR_DL_EN is de-asserted.</p> <p>0 No error was found during the automatic (HW) write calibration process of write delay-line 0. 1 An error was found during the automatic (HW) write calibration process of write delay-line 0.</p>

## 44.12.57 MMDC PHY Read Delay HW Calibration Status Register 0 (MMDCx\_MPRDDLHWST0)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 868h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPRDDLHWST0 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 HW_RD_DL_UP1	Automatic (HW) read calibration result of the upper boundary of Byte1. This field holds the automatic (HW) read calibration result of the upper boundary of Byte1
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 HW_RD_DL_LOW1	Automatic (HW) read calibration result of the lower boundary of Byte1. This field holds the automatic (HW) read calibration result of the lower boundary of Byte1
15 Reserved	This read-only field is reserved and always has the value 0.
14–8 HW_RD_DL_UP0	Automatic (HW) read calibration result of the upper boundary of Byte0. This field holds the automatic (HW) read calibration result of the upper boundary of Byte0.

Table continues on the next page...

**MMDCx\_MPRDDLHWST0 field descriptions (continued)**

Field	Description
7 Reserved	This read-only field is reserved and always has the value 0.
HW_RD_DL_ LOW0	Automatic (HW) read calibration result of the lower boundary of Byte0. This field holds the automatic (HW) read calibration result of the lower boundary of Byte0.

**44.12.58 MMDC PHY Read Delay HW Calibration Status Register 1 (MMDCx\_MPRDDLHWST1)**

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 86Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPRDDLHWST1 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 HW_RD_DL_ UP3	Automatic (HW) read calibration result of the upper boundary of Byte3. This field holds the automatic (HW) read calibration result of the upper boundary of Byte3
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 HW_RD_DL_ LOW3	Automatic (HW) read calibration result of the lower boundary of Byte3. This field holds the automatic (HW) read calibration result of the lower boundary of Byte3
15 Reserved	This read-only field is reserved and always has the value 0.
14–8 HW_RD_DL_ UP2	Automatic (HW) read calibration result of the upper boundary of Byte2. This field holds the automatic (HW) read calibration result of the upper boundary of Byte2.

*Table continues on the next page...*

**MMDCx\_MPRDDLHWST1 field descriptions (continued)**

Field	Description
7 Reserved	This read-only field is reserved and always has the value 0.
HW_RD_DL_ LOW2	Automatic (HW) read calibration result of the lower boundary of Byte2. This field holds the automatic (HW) read calibration result of the lower boundary of Byte2.

**44.12.59 MMDC PHY Write Delay HW Calibration Status Register 0 (MMDCx\_MPWRDLHWST0)**

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 870h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWRDLHWST0 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 HW_WR_DL_ UP1	Aautomatic (HW) write utomatic (HW) write calibration result of the upper boundary of Byte1. This field holds the automatic (HW) write calibration result of the upper boundary of Byte1.
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 HW_WR_DL_ LOW1	Automatic (HW) write calibration result of the lower boundary of Byte1. This field holds the automatic (HW) write calibration result of the lower boundary of Byte1.
15 Reserved	This read-only field is reserved and always has the value 0.
14–8 HW_WR_DL_ UP0	Automatic (HW) write calibration result of the upper boundary of Byte0. This field holds the automatic (HW) write calibration result of the upper boundary of Byte0.

*Table continues on the next page...*

**MMDCx\_MPWRDLHWST0 field descriptions (continued)**

Field	Description
7 Reserved	This read-only field is reserved and always has the value 0.
HW_WR_DL_ LOW0	Automatic (HW) write calibration result of the lower boundary of Byte0. This field holds the automatic (HW) write calibration result of the lower boundary of Byte0.

**44.12.60 MMDC PHY Write Delay HW Calibration Status Register 1 (MMDCx\_MPWRDLHWST1)**

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x32

Address: Base address + 874h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWRDLHWST1 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 HW_WR_DL_ UP3	Automatic (HW) write calibration result of the upper boundary of Byte3. This field holds the automatic (HW) write calibration result of the upper boundary of Byte3.
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 HW_WR_DL_ LOW3	Automatic (HW) write calibration result of the lower boundary of Byte3. This field holds the automatic (HW) write calibration result of the lower boundary of Byte3.
15 Reserved	This read-only field is reserved and always has the value 0.
14–8 HW_WR_DL_ UP2	Automatic (HW) write calibration result of the upper boundary of Byte2. This field holds the automatic (HW) write calibration result of the upper boundary of Byte2.

Table continues on the next page...

**MMDCx\_MPWRDLHWST1 field descriptions (continued)**

Field	Description
7 Reserved	This read-only field is reserved and always has the value 0.
HW_WR_DL_ LOW2	Automatic (HW) write calibration result of the lower boundary of Byte2. This field holds the automatic (HW) write calibration result of the lower boundary of Byte2.

**44.12.61 MMDC PHY Write Leveling HW Error Register (MMDCx\_MPWLHWERR)**

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 878h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																																	
	HW_WL3_DQ								HW_WL2_DQ								HW_WL1_DQ								HW_WL0_DQ								
W																																	

Reset 0

**MMDCx\_MPWLHWERR field descriptions**

Field	Description
31–24 HW_WL3_DQ	HW write-leveling calibration result of Byte3. This field holds the results for all the 8 write-leveling steps of Byte3. i.e bit 0 holds the result of the write-leveling calibration of 0 delay, bit 1 holds the result of the write-leveling calibration of 1/8delay till bit 7 that holds the result of the write-leveling calibration of 7/8 delay
23–16 HW_WL2_DQ	HW write-leveling calibration result of Byte2. This field holds the results for all the 8 write-leveling steps of Byte2. i.e bit 0 holds the result of the write-leveling calibration of 0 delay, bit 1 holds the result of the write-leveling calibration of 1/8delay till bit 7 that holds the result of the write-leveling calibration of 7/8 delay
15–8 HW_WL1_DQ	HW write-leveling calibration result of Byte1. This field holds the results for all the 8 write-leveling steps of Byte1. i.e bit 0 holds the result of the write-leveling calibration of 0 delay, bit 1 holds the result of the write-leveling calibration of 1/8delay till bit 7 that holds the result of the write-leveling calibration of 7/8 delay
HW_WL0_DQ	HW write-leveling calibration result of Byte0. This field holds the results for all the 8 write-leveling steps of Byte0. i.e bit 0 holds the result of the write-leveling calibration of 0 delay, bit 1 holds the result of the write-leveling calibration of 1/8delay till bit 7 that holds the result of the write-leveling calibration of 7/8 delay

**44.12.62 MMDC PHY Read DQS Gating HW Status Register 0 (MMDCx\_MPDGHWST0)**

Supported Mode Of Operations:

For Channel 0: DDR3\_x16, DDR3\_x32, DDR3\_x64

For Channel 1: DDR3\_x64

Address: Base address + 87Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved					HW_DG_UP0						Reserved						HW_DG_LOW0														
W																																

#### MMDCx\_MPDGHWST0 field descriptions

Field	Description
31–27 -	This field is reserved. Reserved
26–16 HW_DG_UP0	HW DQS gating calibration result of the upper boundary of Byte0. This field holds the HW DQS gating calibration result of the upper boundary of Byte0.
15–11 -	This field is reserved. Reserved
HW_DG_LOW0	HW DQS gating calibration result of the lower boundary of Byte0. This field holds the HW DQS gating calibration result of the lower boundary of Byte0.

### 44.12.63 MMDC PHY Read DQS Gating HW Status Register 1 (MMDCx\_MPDGHWST1)

Supported Mode Of Operations:

For Channel 0: DDR3\_x16, DDR3\_x32, DDR3\_x64

For Channel 1: DDR3\_x64

Address: Base address + 880h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved					HW_DG_UP1						Reserved						HW_DG_LOW1														
W																																

#### MMDCx\_MPDGHWST1 field descriptions

Field	Description
31–27 -	This field is reserved. Reserved
26–16 HW_DG_UP1	HW DQS gating calibration result of the upper boundary of Byte1. This field holds the HW DQS gating calibration result of the upper boundary of Byte1.
15–11 -	This field is reserved. Reserved
HW_DG_LOW1	HW DQS gating calibration result of the lower boundary of Byte1. This field holds the HW DQS gating calibration result of the lower boundary of Byte1.

#### 44.12.64 MMDC PHY Read DQS Gating HW Status Register 2 (MMDCx\_MPDGHWST2)

Supported Mode Of Operations:

For Channel 0: DDR3\_x16, DDR3\_x32, DDR3\_x64

For Channel 1: DDR3\_x64

Address: Base address + 884h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved					HW_DG_UP2						Reserved						HW_DG_LOW2														
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

##### MMDCx\_MPDGHWST2 field descriptions

Field	Description
31–27 -	This field is reserved. Reserved
26–16 HW_DG_UP2	HW DQS gating calibration result of the upper boundary of Byte2. This field holds the HW DQS gating calibration result of the upper boundary of Byte2.
15–11 -	This field is reserved. Reserved
HW_DG_LOW2	HW DQS gating calibration result of the lower boundary of Byte2. This field holds the HW DQS gating calibration result of the lower boundary of Byte2.

#### 44.12.65 MMDC PHY Read DQS Gating HW Status Register 3 (MMDCx\_MPDGHWST3)

Supported Mode Of Operations:

For Channel 0: DDR3\_x16, DDR3\_x32, DDR3\_x64

For Channel 1: DDR3\_x64

Address: Base address + 888h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved					HW_DG_UP3						Reserved						HW_DG_LOW3														
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**MMDCx\_MPDPHWST3 field descriptions**

Field	Description
31–27 -	This field is reserved. Reserved
26–16 HW_DG_UP3	HW DQS gating calibration result of the upper boundary of Byte3. This field holds the HW DQS gating calibration result of the upper boundary of Byte3.
15–11 -	This field is reserved. Reserved
HW_DG_LOW3	HW DQS gating calibration result of the lower boundary of Byte3. This field holds the HW DQS gating calibration result of the lower boundary of Byte3.

**44.12.66 MMDC PHY Pre-defined Compare Register 1  
(MMDCx\_MPPDCMPR1)**

This register holds the MMDC pre-defined compare value that will be used during automatic read, read DQS gating and write calibration process. The compare value can be the MPR value (as defined in the JEDEC) or can be programmed by the PDV1 and PDV2 fields. In case of DDR3 (BL=8) the MMDC will duplicate PDV1,PDV2 and drive that data on Beat4-7 of the same byte

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 88Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

**MMDCx\_MPPDCMPR1 field descriptions**

Field	Description
31–16 PDV2	MMDC Pre defined compare value2. This field holds the 2 MSB of the data that will be driven to the DDR device during automatic read, read DQS gating and write calibrations in case MPR(DDR3)/ DQ calibration (LPDDR2) mode are disabled (MPR_CMP is disabled). Upon read access during the calibration the MMDC will compare the read data with the data that is stored in this field.  Note : Before issue the read access the MMDC will invert the value of this field and drive it to the associate entry in the read comparison FIFO. For further information see Section 19.14.3.1.2, "Calibration with pre-defined value , Section 19.14.4.1.2, "Calibration with pre-defined value and Section 19.14.5.1, "HW (automatic) Write Calibration
PDV1	MMDC Pre defined compare value2. This field holds the 2 LSB of the data that will be driven to the DDR device during automatic read, read DQS gating and write calibrations in case MPR(DDR3)/ DQ calibration (LPDDR2) mode are disabled (MPR_CMP is disabled). Upon read access during the calibration the MMDC will compare the read data with the data that is stored in this field.

*Table continues on the next page...*

**MMDCx\_MPPDCMPR1 field descriptions (continued)**

Field	Description
	<b>NOTE:</b> Before issuing the read access, the MMDC will invert the value of this field and drive it to the associated entry in the read comparison FIFO.

### 44.12.67 MMDC PHY Pre-defined Compare and CA delay-line Configuration Register (MMDCx\_MPPDCMPR2)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 890h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								0							
W																
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPPDCMPR2 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–24 PHY_CA_DL_UNIT	This field reflects the number of delay units that are actually used by CA (Command/Address of LPDDR2) delay-line
23 Reserved	This read-only field is reserved and always has the value 0.
22–16 CA_DL_ABS_OFFSET	Absolute CA (Command/Address of LPDDR2) offset. This field indicates the absolute delay between CA (Command/Address) bus and the DDR clock (CK) with fractions of a clock period and up to half cycle. The fraction is process and frequency independent. The delay of the delay-line would be $(CA\_DL\_ABS\_OFFSET / 256) * MMDC\_CH0 AXI clock (fast clock)$ . So for the default value of 64 we get a quarter cycle delay.
15–3 Reserved	This read-only field is reserved and always has the value 0.
2 READ_LEVEL_PATTERN	MPR(DDR3)/DQ calibration(LPDDR2) read compare pattern. In case MPR(DDR3)/DQ calibration(LPDDR2) modes are used during the calibration process (MPR_CMP is asserted) then this field indicates the read pattern for the comparison.  0 Compare with read pattern 1010 1 Compare with read pattern 0011 (Used only in LPDDR2 mode)
1 MPR_FULL_CMP	MPR(DDR3)/DQ calibration (LPDDR2) full compare enable. In case MPR(DDR3)/DQ calibration(LPDDR2) modes are used during the calibration process (MPR_CMP is asserted) then this field indicates whether the MMDC will compare all the bits of the data that is read from the DDR device to the MPR pre-defined pattern. When this bit is de-asserted only LSB of each byte is compared.
0 MPR_CMP	MPR(DDR3)/DQ calibration (LPDDR2) compare enable. This bit indicates whether the MMDC will compare the read data during automatic read and read DQS calibration processes to the pre-defined patterns that are driven by the DDR device (READ_LEVEL_PATTERN as defined by JEDEC) or general pre-defined value that are stored in PDV1 and PDV2. When this bit is disabled data is compared to the data of the pre defined compare value field  For further information see <a href="#">Read DQS Gating Calibration</a> and <a href="#">Read Calibration</a> .

**44.12.68 MMDC PHY SW Dummy Access Register (MMDCx\_MPSWDAR0)**

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

## MMDC Memory Map/Register Definition

Address: Base address + 894h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R									0								
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R									0			SW_DUM_CMP3	SW_DUM_CMP2	SW_DUM_CMP1	SW_DUM_CMP0	SW_DUMMY_RD	SW_DUMMY_WR
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### MMDCx\_MPSWDAR0 field descriptions

Field	Description
31–6 Reserved	This read-only field is reserved and always has the value 0.
5 SW_DUM_CMP3	SW dummy read byte3 compare results. This bit indicates the result of the read data comparison of Byte3 at the completion of SW_DUMMY_RD. This bit is valid only when SW_DUMMY_RD is de-asserted. 0 Dummy read fail 1 Dummy read pass
4 SW_DUM_CMP2	SW dummy read byte2 compare results. This bit indicates the result of the read data comparison of Byte2 at the completion of SW_DUMMY_RD. This bit is valid only when SW_DUMMY_RD is de-asserted.

Table continues on the next page...

**MMDCx\_MPSWDAR0 field descriptions (continued)**

Field	Description
	0 Dummy read fail 1 Dummy read pass
3 SW_DUM_CMP1	SW dummy read byte1 compare results. This bit indicates the result of the read data comparison of Byte1 at the completion of SW_DUMMY_RD. This bit is valid only when SW_DUMMY_RD is de-assrted.  0 Dummy read fail 1 Dummy read pass
2 SW_DUM_CMP0	SW dummy read byte0 compare results. This bit indicates the result of the read data comparison of Byte0 at the completion of SW_DUMMY_RD. This bit is valid only when SW_DUMMY_RD is de-assrted.  0 Dummy read fail 1 Dummy read pass
1 SW_DUMMY_RD	SW dummy read. When this bit is asserted the MMDC will generate internally read access without intervention of the system toward bank 0, row 0, column 0. If MPR_CMP = 1 then the read data will be compared to MPPDCMPR2[READ_LEVEL_PATTERN]. If MPR_CMP = 0 then the read data will be compared to MPPDCMPR1[PDV1], MPPDCMPR1[PDV2]. Upon completion of the access this bit is de-asserted automatically and the read data and comparison results are valid at MPSWDAR0[SW_DUM_CMP#] and MPSWDRDR0-MPSWDRDR7 respectively.
0 SW_DUMMY_WR	SW dummy write. When this bit is asserted the MMDC will generate internally write access without intervention of the system toward bank 0, row 0, column 0, while the data is driven from MPPDCMPR1[PDV1] and MPPDCMPR1[PDV2]. The bit is de-asserted automatically upon completion of the access.

## 44.12.69 MMDC PHY SW Dummy Read Data Register 0 (MMDCx\_MPSWDRDR0)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 898h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
R																	DUM_RD0																		
W																																			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

**MMDCx\_MPSWDRDR0 field descriptions**

Field	Description
DUM_RD0	Dummy read data0. This field holds the first data that is read from the DDR during SW dummy read access (i.e when SW_DUMMY_RD = 1). This field is valid only when SW_DUMMY_RD is de-assrted

### 44.12.70 MMDC PHY SW Dummy Read Data Register 1 (MMDCx\_MPSWDRDR1)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 89Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	DUM_RD1																
W																																	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

#### MMDCx\_MPSWDRDR1 field descriptions

Field	Description
DUM_RD1	Dummy read data1. This field holds the second data that is read from the DDR during SW dummy read access (i.e when SW_DUMMY_RD = 1). This field is valid only when SW_DUMMY_RD is de-assrted

### 44.12.71 MMDC PHY SW Dummy Read Data Register 2 (MMDCx\_MPSWDRDR2)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 8A0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																	DUM_RD2																	
W																																		
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			

#### MMDCx\_MPSWDRDR2 field descriptions

Field	Description
DUM_RD2	Dummy read data2. This field holds the third data that is read from the DDR during SW dummy read access (i.e when SW_DUMMY_RD = 1). This field is valid only when SW_DUMMY_RD is de-assrted.

### 44.12.72 MMDC PHY SW Dummy Read Data Register 3 (MMDCx\_MPSWDRDR3)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 8A4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DUM_RD3																															
W																																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

#### MMDCx\_MPSWDRDR3 field descriptions

Field	Description
DUM_RD3	Dummy read data3. This field holds the forth data that is read from the DDR during SW dummy read access (i.e when SW_DUMMY_RD = 1). This field is valid only when SW_DUMMY_RD is de-assrted.

### 44.12.73 MMDC PHY SW Dummy Read Data Register 4 (MMDCx\_MPSWDRDR4)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 8A8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DUM_RD4																															
W																																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

#### MMDCx\_MPSWDRDR4 field descriptions

Field	Description
DUM_RD4	Dummy read data4. This field holds the fifth data (only in case of burst length 8 (BL =1 )) that is read from the DDR during SW dummy read access (i.e when SW_DUMMY_RD = 1). This field is valid only when SW_DUMMY_RD is de-assrted.

#### 44.12.74 MMDC PHY SW Dummy Read Data Register 5 (MMDCx\_MPSWDRDR5)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 8ACh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	DUM_RD5																
W																																	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

##### MMDCx\_MPSWDRDR5 field descriptions

Field	Description
DUM_RD5	Dummy read data5. This field holds the sixth data (only in case of burst length 8 (BL =1 )) that is read from the DDR during SW dummy read access (i.e when SW_DUMMY_RD = 1). This field is valid only when SW_DUMMY_RD is de-assrted.

#### 44.12.75 MMDC PHY SW Dummy Read Data Register 6 (MMDCx\_MPSWDRDR6)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 8B0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																	DUM_RD6																	
W																																		
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			

##### MMDCx\_MPSWDRDR6 field descriptions

Field	Description
DUM_RD6	Dummy read data6. This field holds the seventh data (only in case of burst length 8 (BL =1 )) that is read from the DDR during SW dummy read access (i.e when SW_DUMMY_RD = 1). This field is valid only when SW_DUMMY_RD is de-assrted.

### 44.12.76 MMDC PHY SW Dummy Read Data Register 7 (MMDCx\_MPSWDRDR7)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 8B4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DUM_RD7																															
W																																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

#### MMDCx\_MPSWDRDR7 field descriptions

Field	Description
DUM_RD7	Dummy read data7. This field holds the eighth data (only in case of burst length 8 (BL =1 )) that is read from the DDR during SW dummy read access (i.e when SW_DUMMY_RD = 1). This field is valid only when SW_DUMMY_RD is de-assrted.

### 44.12.77 MMDC PHY Measure Unit Register (MMDCx\_MPMUR0)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 8B8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	0						MU_UNIT_DEL_NUM										
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	0				FRC_MSR	MU_BYP_EN	MU_BYP_VAL										
W					0	0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPMUR0 field descriptions**

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.
25–16 MU_UNIT_DEL_NUM	Number of delay units measured per cycle. This field is used in debug mode and holds the number of delay units that were measured by the measure unit per DDR clock cycle. The delay-lines that are used in every calibration process use that number for generating the desired delay.
15–12 Reserved	This read-only field is reserved and always has the value 0.
11 FRC_MSR	Force measurement on delay-lines. When this bit is asserted then a measurement process will be performed, where at the completion of the process the delay-lines will issue the desired delay. Upon completion of the measurement process the measure unit and the delay-lines will return to functional mode. This bit is self cleared.  <b>NOTE:</b> This bit should be used only during manual (SW) calibration and not while the DDR is functional (being accessed). After initial calibration is done the hardware performs periodic measurements to track any operating conditions changes. Hence, force measurements (FRC_MSR) should not be used. See <a href="#">Calibration Process</a> for more information.  <b>NOTE:</b> User should make sure that there is no active accesses to/from DDR before asserting this bit.  0 No measurement is performed 1 Perform measurement process
10 MU_BYP_EN	Measure unit bypass enable. This field is used in debug mode and when it is asserted then the delay-lines will use the number of delay units that are indicated at MU_BYP_VAL, otherwise the delay-lines will use the number of delay units that was measured by the measurement unit and are indicated at MU_UNIT_DEL_NUM  0 The delay-lines use delay units as indicated at MU_UNIT_DEL_NUM. 1 The delay-lines use delay units as indicated at MU_BYPASS_VAL.
MU_BYP_VAL	Number of delay units for measurement bypass. This field is used in debug mode and holds the number of delay units that will be used by the delay-lines when MU_BYP_EN is asserted.

### 44.12.78 MMDC Write CA delay-line controller (MMDCx\_MPWRCADL)

This register is used to add fine-tuning adjustment to the CA (command/Address of LPDDR2 bus) relative to the DDR clock

Supported Mode Of Operations:

For Channel 0: LP2\_2ch\_x16, LP2\_2ch\_x32

For Channel 1: LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 8BCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W													WR_CA9_DEL		WR_CA8_DEL	

Reset    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	WR_CA7_DEL		WR_CA6_DEL		WR_CA5_DEL		WR_CA4_DEL		WR_CA3_DEL		WR_CA2_DEL		WR_CA1_DEL		WR_CA0_DEL	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**MMDCx\_MPWRCADL field descriptions**

Field	Description	
31–20 Reserved	This read-only field is reserved and always has the value 0.	
19–18 WR_CA9_DEL	<p>CA (Command/Address LPDDR2 bus) bit 9 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 9 relative to the clock.</p> <ul style="list-style-type: none"> <li>00 No change in CA9 delay</li> <li>01 Add CA9 delay of 1 delay unit</li> <li>10 Add CA9 delay of 2 delay units.</li> <li>11 Add CA9 delay of 3 delay units.</li> </ul>	
17–16 WR_CA8_DEL	<p>CA (Command/Address LPDDR2 bus) bit 8 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 8 relative to the clock.</p> <ul style="list-style-type: none"> <li>00 No change in CA8 delay</li> <li>01 Add CA8 delay of 1 delay unit</li> <li>10 Add CA8 delay of 2 delay units.</li> <li>11 Add CA8 delay of 3 delay units.</li> </ul>	
15–14 WR_CA7_DEL	<p>CA (Command/Address LPDDR2 bus) bit 7 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 7 relative to the clock.</p> <ul style="list-style-type: none"> <li>00 No change in CA7 delay</li> <li>01 Add CA7 delay of 1 delay unit</li> <li>10 Add CA7 delay of 2 delay units.</li> <li>11 Add CA7 delay of 3 delay units.</li> </ul>	
13–12 WR_CA6_DEL	<p>CA (Command/Address LPDDR2 bus) bit 6 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 6 relative to the clock.</p> <ul style="list-style-type: none"> <li>00 No change in CA6 delay</li> <li>01 Add CA6 delay of 1 delay unit</li> <li>10 Add CA6 delay of 2 delay units.</li> <li>11 Add CA6 delay of 3 delay units.</li> </ul>	
11–10 WR_CA5_DEL	<p>CA (Command/Address LPDDR2 bus) bit 5 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 5 relative to the clock.</p> <ul style="list-style-type: none"> <li>00 No change in CA5 delay</li> <li>01 Add CA5 delay of 1 delay unit</li> <li>10 Add CA5 delay of 2 delay units.</li> <li>11 Add CA5 delay of 3 delay units.</li> </ul>	
9–8 WR_CA4_DEL	<p>CA (Command/Address LPDDR2 bus) bit 4 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 4 relative to the clock.</p> <ul style="list-style-type: none"> <li>00 No change in CA4 delay</li> <li>01 Add CA4 delay of 1 delay unit</li> <li>10 Add CA4 delay of 2 delay units.</li> <li>11 Add CA4 delay of 3 delay units.</li> </ul>	

Table continues on the next page...

**MMDCx\_MPWRCADL field descriptions (continued)**

Field	Description
7–6 WR_CA3_DEL	CA (Command/Address LPDDR2 bus) bit 3 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 3 relative to the clock.  00 No change in CA3 delay 01 Add CA3 delay of 1 delay unit 10 Add CA3 delay of 2 delay units. 11 Add CA3 delay of 3 delay units.
5–4 WR_CA2_DEL	CA (Command/Address LPDDR2 bus) bit 2 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 2 relative to the clock.  00 No change in CA2 delay 01 Add CA2 delay of 1 delay unit 10 Add CA2 delay of 2 delay units. 11 Add CA2 delay of 3 delay units.
3–2 WR_CA1_DEL	CA (Command/Address LPDDR2 bus) bit 1 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 1 relative to the clock.  00 No change in CA1 delay 01 Add CA1 delay of 1 delay unit 10 Add CA1 delay of 2 delay units. 11 Add CA1 delay of 3 delay units.
WR_CA0_DEL	CA (Command/Address LPDDR2 bus) bit 0 delay fine tuning. This field holds the number of delay units that are added to CA (Command/Address bus) bit 0 relative to the clock.  00 No change in CA0 delay 01 Add CA0 delay of 1 delay unit 10 Add CA0 delay of 2 delay units. 11 Add CA0 delay of 3 delay units.

**44.12.79 MMDC Duty Cycle Control Register (MMDCx\_MPDCCR)**

This register is used to control the duty cycle of the DQS and the primary clock (CK0). Programming of that register is permitted by entering the DDR device into self-refresh mode through LPMD/DVFS mechanism

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: DDR3\_x64, LP2\_2ch\_x16, LP2\_2ch\_x32

Address: Base address + 8C0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	RD_DQS3_FT_DCC		RD_DQS2_FT_DCC		RD_DQS1_FT_DCC		RD_DQSO_FT_DCC		CK_FT1_DCC						
W																
Reset	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		CK_FT0_DCC		WR_DQS3_FT_DCC		WR_DQS2_FT_DCC		WR_DQS1_FT_DCC		WR_DQS0_FT_DCC					
W																
Reset	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0

**MMDCx\_MPCCR field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–28 RD_DQS3_FT_DCC	Read DQS duty cycle fine tuning control of Byte3. This field controls the duty cycle of read DQS of Byte3 Note all the other options are not allowed 001 48.5% low 51.5% high 010 50% duty cycle (default) 100 51.5% low 48.5% high
27–25 RD_DQS2_FT_DCC	Read DQS duty cycle fine tuning control of Byte2. This field controls the duty cycle of read DQS of Byte2 Note all the other options are not allowed 001 48.5% low 51.5% high 010 50% duty cycle (default) 100 51.5% low 48.5% high
24–22 RD_DQS1_FT_DCC	Read DQS duty cycle fine tuning control of Byte1. This field controls the duty cycle of read DQS of Byte1 Note all the other options are not allowed 001 48.5% low 51.5% high 010 50% duty cycle (default) 100 51.5% low 48.5% high
21–19 RD_DQS0_FT_DCC	Read DQS duty cycle fine tuning control of Byte0. This field controls the duty cycle of read DQS of Byte0 Note all the other options are not allowed 001 48.5% low 51.5% high 010 50% duty cycle (default) 100 51.5% low 48.5% high
18–16 CK_FT1_DCC	Secondary duty cycle fine tuning control of DDR clock. This field controls the duty cycle of the DDR clock and is cascaded to CK_FT0_DCC Note all the other options are not allowed 001 48.5% low 51.5% high 010 50% duty cycle (default) 100 51.5% low 48.5% high
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 CK_FT0_DCC	Primary duty cycle fine tuning control of DDR clock. This field controls the duty cycle of the DDR clock Note all the other options are not allowed 001 48.5% low 51.5% high

*Table continues on the next page...*

**MMDCx\_MPCCR field descriptions (continued)**

Field	Description
	010 50% duty cycle (default) 100 51.5% low 48.5% high
11–9 WR_DQS3_FT_DCC	Write DQS duty cycle fine tuning control of Byte0. This field controls the duty cycle of write DQS of Byte0 Note all the other options are not allowed 001 48.5% low 51.5% high 010 50% duty cycle (default) 100 51.5% low 48.5% high
8–6 WR_DQS2_FT_DCC	Write DQS duty cycle fine tuning control of Byte1. This field controls the duty cycle of write DQS of Byte1 Note all the other options are not allowed 001 48.5% low 51.5% high 010 50% duty cycle (default) 100 51.5% low 48.5% high
5–3 WR_DQS1_FT_DCC	Write DQS duty cycle fine tuning control of Byte1. This field controls the duty cycle of write DQS of Byte1 Note all the other options are not allowed 001 48.5% low 51.5% high 010 50% duty cycle (default) 100 51.5% low 48.5% high
WR_DQS0_FT_DCC	Write DQS duty cycle fine tuning control of Byte0. This field controls the duty cycle of write DQS of Byte0 Note all the other options are not allowed 001 48.5% low 51.5% high 010 50% duty cycle (default) 100 51.5% low 48.5% high