**NOTE**

Several options of control usage can be available. some display devices use only DE, some others use all 3 controls, some use only HS, VS. "CTL" is an optional general purpose control which is usually unused by display.

## 39.6 LDB Memory Map/Register Definition

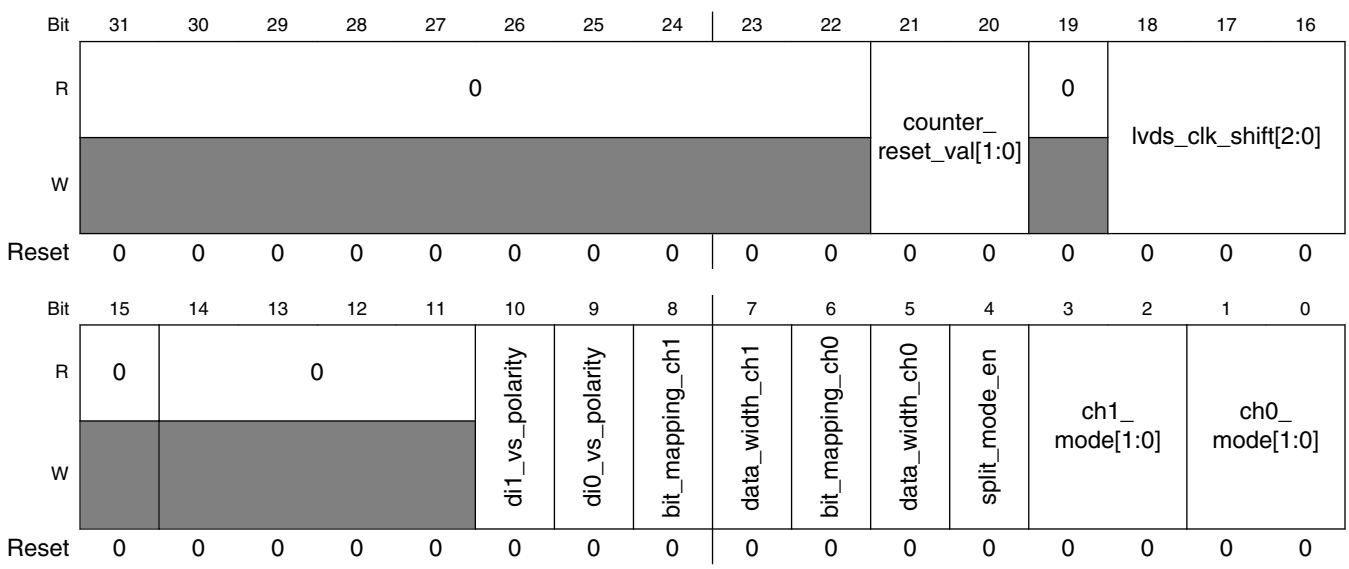
**LDB memory map**

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|---|---|---|---|---|---|
| 20E_0008 | LDB Control Register (LDB_CTRL) | 32 | R/W | 0000_0000h | 39.6.1/3565 |

### 39.6.1 LDB Control Register (LDB_CTRL)

The register is implemented in the IOMUX Controller block (IOMUXC), as the register IOMUXC_GPR2.

Address: 20E_0008h base + 0h offset = 20E_0008h



## LDB_CTRL field descriptions

| Field | Description |
|---|---|
| 31–22<br>Reserved | This read-only field is reserved and always has the value 0. |
| 21–20<br>counter_reset_val[1:0] | Reset value for the LDB counter which determines when the shift registers are loaded with data.<br>**NOTE:** Used for debug purposes only. In normal functional operation must be '00'<br>00 Reset value is 5<br>01 Reset value is 3<br>10 Reset value is 4<br>11 Reset value is 6 |
| 19<br>Reserved | This read-only field is reserved and always has the value 0. |
| 18–16<br>lvds_clk_shift[2:0] | Shifts the LVDS output clock in relation to the data.<br>**NOTE:** Used for debug purposes only. In normal functional operation must be '000'<br>000 Output clock is '1100011' (normal operation)<br>001 Output clock is '1110001'<br>010 Output clock is '1111000'<br>011 Output clock is '1000111'<br>100 Output clock is '0001111'<br>101 Output clock is '0011111'<br>110 Output clock is '0111100'<br>111 Output clock is '1100011' |
| 15<br>Reserved | This read-only field is reserved and always has the value 0. |
| 14–11<br>Reserved | This read-only field is reserved and always has the value 0. |
| 10<br>di1_vs_polarity | Vsync polarity for IPU's DI1 interface.<br>0 ipu_di1_vsync is active high.<br>1 ipu_di1_vsync is active low. |
| 9<br>di0_vs_polarity | Vsync polarity for IPU's DI0 interface.<br>0 ipu_di0_vsync is active high.<br>1 ipu_di0_vsync is active low. |
| 8<br>bit_mapping_ch1 | Data mapping for LVDS channel 1.<br>0 Use SPWG standard.<br>1 Use JEIDA standard. |
| 7<br>data_width_ch1 | Data width for LVDS channel 1.<br>**NOTE:** This bit must be set when using JEIDA standard (bit_mapping_ch1 is set)<br>0 Data width is 18 bits wide (lvds1_tx3 is not used)<br>1 Data width is 24 bits wide. |
| 6<br>bit_mapping_ch0 | Data mapping for LVDS channel 0.<br>0 Use SPWG standard.<br>1 Use JEIDA standard. |

*Table continues on the next page...*

## LDB_CTRL field descriptions (continued)

| Field | Description |
|---|---|
| 5<br>data_width_ch0 | Data width for LVDS channel 0.<br>**NOTE:** This bit must be set when using JEIDA standard (bit_mapping_ch0 is set)<br>0 Data width is 18 bits wide (lvds0_tx3 is not used)<br>1 Data width is 24 bits wide. |
| 4<br>split_mode_en | Enable split mode.<br>**NOTE:** In this mode both channels should be enabled and working with the same DI (ch0_mode and ch1_mode should both be either '01' or '11')<br>0 Split mode is disabled.<br>1 Split mode is enabled. |
| 3–2<br>ch1_mode[1:0] | LVDS channel 1 operation mode<br>00 Channel disabled.<br>01 Channel enabled, routed to DI0<br>10 Channel disabled.<br>11 Channel enabled, routed to DI1. |
| ch0_mode[1:0] | LVDS channel 0 operation mode<br>00 Channel disabled.<br>01 Channel enabled, routed to DI0<br>10 Channel disabled.<br>11 Channel enabled, routed to DI1. |