53.7 SATA Memory Map/Register Definition

This section provides high-level summaries of the Generic and Port control regsier maps.

The register names in SATA Memory Map are cross-referenced to the detailed register descriptions in the following section (double-click on the register name to link to the detailed description).

SATA memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
220_0000	HBA Capabilites Register (SATA_CAP)	32	R	0000_0000h	53.7.1/4552
220_0004	Global HBA Control Register (SATA_GHC)	32	R/W	8000_0000h	53.7.2/4555
220_0008	Interrupt Status Register (SATA_IS)	32	R/W	0000_0000h	53.7.3/4556
220_000C	Ports Implemented Register (SATA_PI)	32	R	See section	53.7.4/4557
220_0010	AHCI Version Register (SATA_VS)	32	R	0001_0300h	53.7.5/4557
220_0014	Command Completion Coalescing Control (SATA_CCC_CTL)	32	R/W	See section	53.7.6/4558
220_0018	Command Completion Coalescing Ports (SATA_CCC_PORTS)	32	R/W	0000_0000h	53.7.7/4559
220_0024	HBA Capabilities Extended Register (SATA_CAP2)	32	R	0000_0004h	53.7.8/4560
220_00A0	BIST Activate FIS Register (SATA_BISTAFR)	32	R	0000_0000h	53.7.9/4561
220_00A4	BIST Control Register (SATA_BISTCR)	32	R/W	0000_0700h	53.7.10/ 4562
220_00A8	BIST FIS Count Register (SATA_BISTFCTR)	32	R	0000_0000h	53.7.11/ 4565
220_00AC	BIST Status Register (SATA_BISTSR)	32	R	0000_0000h	53.7.12/ 4566
220_00BC	OOB Register (SATA_OOBR)	32	R/W	See section	53.7.13/ 4566
220_00D0	General Purpose Control Register (SATA_GPCR)	32	R/W	0000_0000h	53.7.14/ 4567
220_00D4	General Purpose Status Register (SATA_GPSR)	32	R/W	0000_0000h	53.7.15/ 4568
220_00E0	Timer 1-ms Register (SATA_TIMER1MS)	32	R/W	0001_86A0h	53.7.16/ 4568
220_00F4	Test Register (SATA_TESTR)	32	R/W	0000_0000h	53.7.17/ 4569
220_00F8	Version Register (SATA_VERSIONR)	32	R	3330_302Ah	53.7.18/ 4571
220_0100	Port0 Command List Base Address Register (SATA_P0CLB)	32	R/W	0000_0000h	53.7.19/ 4571

Table continues on the next page...

SATA memory map (continued)

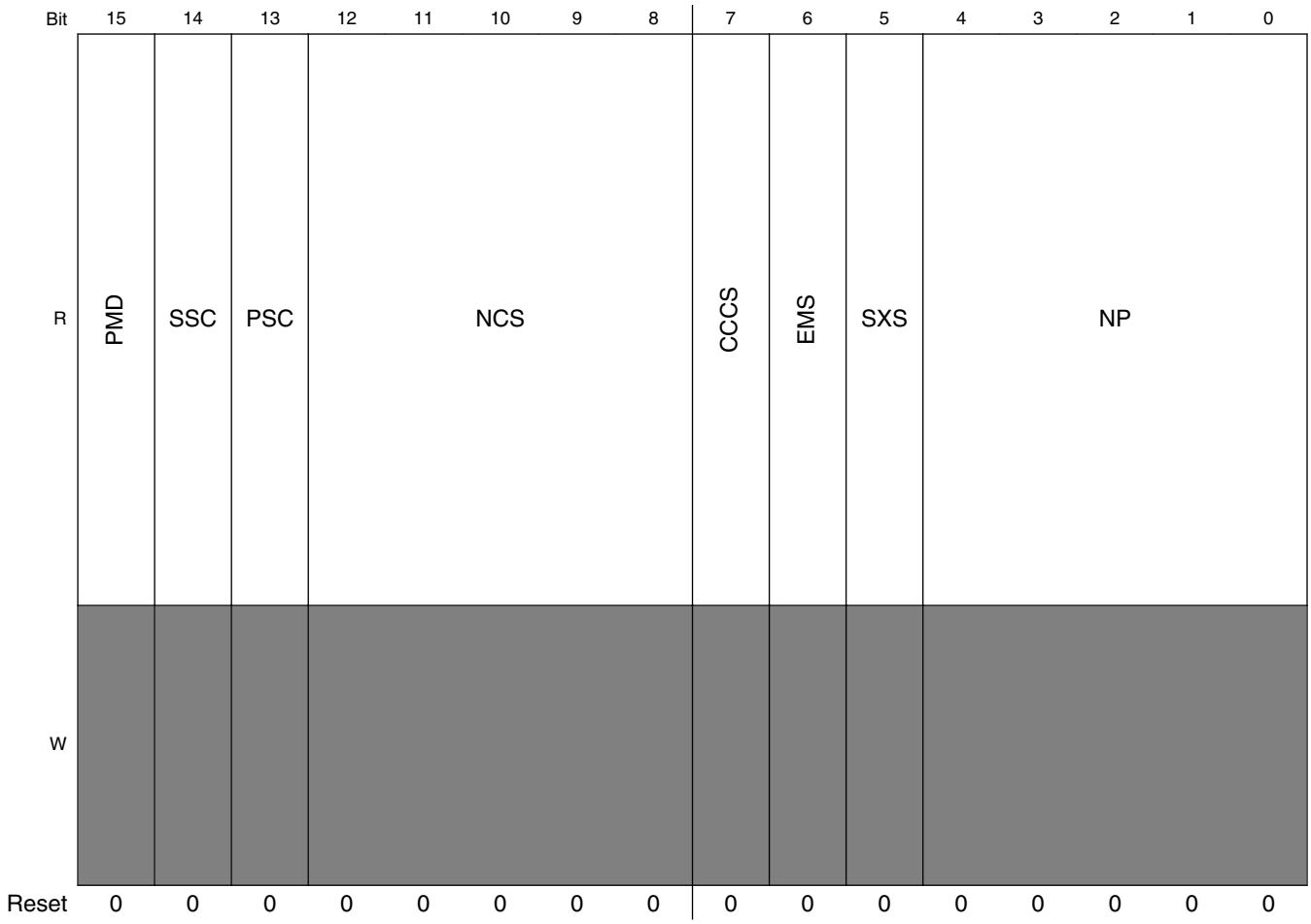
Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
220_0108	Port0 FIS Base Address Register (SATA_P0FB)	32	R/W	0000_0000h	53.7.20/ 4572
220_0110	Port0 Interrupt Status Register (SATA_P0IS)	32	R/W	0000_0000h	53.7.21/ 4573
220_0114	Port0 Interrupt Enable Register (SATA_P0IE)	32	R/W	0000_0000h	53.7.22/ 4577
220_0118	Port0 Command Register (SATA_P0CMD)	32	R/W	0000_0000h	53.7.23/ 4580
220_0120	Port0 Task File Data Register (SATA_P0TFD)	32	R	0000_007Fh	53.7.24/ 4584
220_0124	Port0 Signature Register (SATA_P0SIG)	32	R	FFFF_FFFFh	53.7.25/ 4584
220_0128	Port0 Serial ATA Status Register (SATA_P0SSTS)	32	R	0000_0000h	53.7.26/ 4585
220_012C	Port0 Serial ATA Control {SControl} Register (SATA_P0SCTL)	32	R/W	0000_0000h	53.7.27/ 4586
220_0130	Port0 Serial ATA Error Register (SATA_P0SERR)	32	R/W	0000_0000h	53.7.28/ 4588
220_0134	Port0 Serial ATA Active Register (SATA_P0SACT)	32	R/W	0000_0000h	53.7.29/ 4590
220_0138	Port0 Command Issue Register (SATA_P0CI)	32	R/W	0000_0000h	53.7.30/ 4591
220_013C	Port0 Serial ATA Notification Register (SATA_P0SNTF)	32	w1c	0000_0000h	53.7.31/ 4592
220_0170	Port0 DMA Control Register (SATA_P0DMACR)	32	R/W	0000_0044h	53.7.32/ 4592
220_0178	Port0 PHY Control Register (SATA_P0PHYCR)	32	R/W	0000_0000h	53.7.33/ 4594
220_017C	Port0 PHY Status Register (SATA_P0PHYSR)	32	R	0000_0000h	53.7.34/ 4595

53.7.1 HBA Capabilites Register (SATA_CAP)

This register indicates basic capabilities of the SATA block to the software.

Address: 220_0000h base + 0h offset = 220_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	S64A	SNCQ	SSNTF	SMPS	SSS	SALP	SAL	SCLO	Reserved				Reserved	SAM	SMP	Reserved
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



SATA_CAP field descriptions

Field	Description
31 S64A	Supports 64-bit Addressing SATA block supports 64-bit addressable data structures by utilizing PFFBU and P#CLBU registers. Reset Value: Configurable. 1 when M_HADDR_WIDTH=64 0 when M_HADDR_WIDTH=32
30 SNCQ	Supports Native Command Queuing. SATA block supports SATA native command queueing by handling DMA Setup FIS natively.
29 SSNTF	Supports SNotification Register. SATA block supports SATA_P 0 SNTF (SNotification) register and its associated functionality.
28 SMPS	Supports Mechanical Presence Switch. This bit is set by the system firmware/BIOS when the platform supports mechanical presence switch for hot plug operation. Dependencies: This field is implemented only when parameter (Macro configuration parm) DEV_MP_SWITCH==Include. When this field is not implemented, this field is reserved, and reads 1'b0.

Table continues on the next page...

SATA_CAP field descriptions (continued)

Field	Description
27 SSS	Supports Staggered Spin-up. This bit is set by the system firmware/BIOS to indicate platform support for staggered devices' spin-up. SATA block supports this feature through the SATA_P 0 CMD[SUD] bit functionality.
26 SALP	Supports Aggressive Link Power Management. SATA block supports auto-generating (Port-initiated) Link Layer requests to the PARTIAL or SLUMBER power management states when there are no commands to process.
25 SAL	Supports Activity LED. SATA block supports activity indication using signal p 0 _act_led.
24 SCLO	Supports Command List Override. SATA block supports the SATA_P 0 CMD[CLO] bit functionality for Port Multiplier devices' enumeration.
23–20 ISS	This field is reserved. Interface Speed Support. Reserved. Returns 0x2 on read.
19 -	This field is reserved. Reserved. Returns 0 on read.
18 SAM	Supports AHCI Mode Only. SATA block supports AHCI mode only and does not support legacy, task-file based register interface.
17 SMP	Supports Port Multiplier. SATA block supports command-based switching Port Multiplier on any of its Ports.
16 -	This field is reserved. Reserved.
15 PMD	PIO Multiple DRQ Block. SATA block supports multiple DRQ block data transfers for the PIO command protocol.
14 SSC	Slumber State Capable. SATA block supports transitions to the interface SLUMBER power management state.
13 PSC	Partial State Capable. SATA block supports transitions to the interface PARTIAL power management state.
12–8 NCS	Number of Command Slots. SATA block supports 32 command slots per Port.
7 CCCS	Command Completion Coalescing Support. SATA block supports command completion coalescing.
6 EMS	Enclosure Management Support. SATA block does not support enclosure management.
5 SXS	Supports External SATA. The options for this field are: 1 Indicates that the SATA block has one or more Ports that has a signal only connector (power is not part of that connector) that is externally accessible. When this bit is set to 1, the software can refer to the SATA_P 0 CMD[ESP] bit to determine whether a specific Port has its signal connector externally accessible. 0 Indicates that the SATA block has no Ports that have a signal only connector externally accessible.

Table continues on the next page...

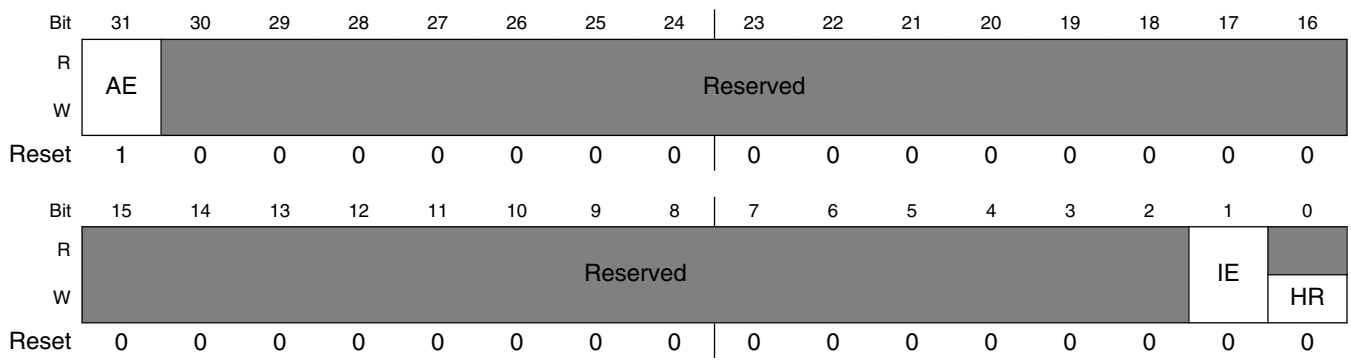
SATA_CAP field descriptions (continued)

Field	Description
	Reset Value: Configurable 1 when any of the SATA_P 0 CMD[ESP]=1 0 when all of the SATA_P 0 CMD[ESP]=0
NP	Number of Ports. 0's based value indicating the number of Ports supported by the SATA block: The options for this field are: • 0x00: 1 Port • 0x01: 2 Ports • 0x02: 3 Ports Reset Value: 0x00

53.7.2 Global HBA Control Register (SATA_GHC)

This register controls various global actions of the SATA block.

Address: 220_0000h base + 4h offset = 220_0004h



SATA_GHC field descriptions

Field	Description
31 AE	AHCI Enable. This bit is always set since SATA block supports only AHCI mode as indicated by the SATA_CAP[SAM]=1.
30–2 -	This field is reserved. Reserved
1 IE	Interrupt Enable. This global bit enables interrupts from the SATA block. When cleared, all interrupt sources from all the Ports are disabled (masked). When set, interrupts are enabled and any SATA block interrupt event causes intrq output assertion.

Table continues on the next page...

SATA_GHC field descriptions (continued)

Field	Description
	This field is reset on Global reset (SATA_GHC[HR]=1).
0 HR	HBA Reset. When set by the software, this bit causes an internal Global reset of the SATA block. All state machines that relate to data transfers and queueing return to an idle state, and all the Ports are re-initialized by sending COMRESET When staggered spin-up is not supported. When staggered spin-up is supported, then the software must spin-up each Port after this reset has completed. See Global Reset for details. The SATA block clears this bit when the reset action is done. A software write of 0 has no effect.

53.7.3 Interrupt Status Register (SATA_IS)

This register indicates which of the Ports within the SATA block have an interrupt pending and require service. This register is reset on Global reset (SATA_GHC[HR]=1).

- Size: 32 bits
- Address offset: 0x08
- Read/write access: Read/Write One to Clear
- Reset: 0x0000_00000

Address: 220_0000h base + 8h offset = 220_0008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved																														IPS	
W																															w1c	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_IS field descriptions

Field	Description
31–2 -	This field is reserved. Reserved.
IPS	Interrupt Pending Status. When bit 1is set, this indicates that Port 0 has an interrupt pending. This bit is set when the Port has an interrupt event pending and the interrupt source is enabled (see the definition of the SATA_P 0 IE register). Bit 0 of the IPS field is not used.

53.7.4 Ports Implemented Register (SATA_PI)

This register indicates which Ports are exposed by the SATA block and are available for the software to use. It is loaded by the BIOS. For example, when the SATA block supports 8 Ports as indicated in the SATA_CAP[NP], only Ports 1, 3, 5, and 7 could be available, while Ports 0, 2, 4, and 6 being unavailable.

NOTE

The contents of this register are relevant to the SATA_CCC_PORTS (Command Completion Coalescing Ports) register.

Address: 220_0000h base + Ch offset = 220_000Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved															PI
W																
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- See descriptions for reset values.

SATA_PI field descriptions

Field	Description
31–1 -	This field is reserved. Reserved.
0 PI	Ports Implemented. BIOS must set this bit to 1

53.7.5 AHCI Version Register (SATA_VS)

This register indicates the major and minor version of the AHCI specification that the SATA block implementation supports. The SATA block supports version 1.30.

NOTE

The SATA block core currently complies fully with AHCI version 1.10 , and complies with AHCI version 1.3, except with

respect to FIS-based switching. FIS-based switching is not currently supported.

Address: 220_0000h base + 10h offset = 220_0010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MJR																MNR															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

SATA_VS field descriptions

Field	Description
31–16 MJR	Major Version Number. Indicates that the major AHCI version is 1.
MNR	Minor Version Number. Indicates that the minor AHCI version is 30.

53.7.6 Command Completion Coalescing Control (SATA_CCC_CTL)

This register is used to configure the command completion coalescing (CCC) feature for the SATA block core. It is reset on Global reset.

Address: 220_0000h base + 14h offset = 220_0014h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	TV															
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CC								INT					Reserved		EN
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- See descriptions for reset values.

SATA_CCC_CTL field descriptions

Field	Description
31–16 TV	Time-out Value. This field specifies the CCC time-out value in 1ms intervals. The software loads this value prior to enabling CCC. The options for this field are:

Table continues on the next page...

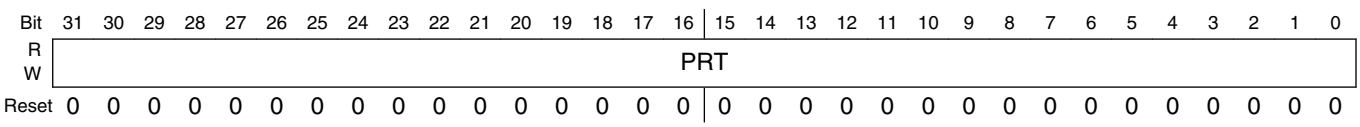
SATA_CCC_CTL field descriptions (continued)

Field	Description
	• RW when SATA_CCC_CTL[EN]==0. • RO when SATA_CCC_CTL[EN]==1. A time-out value of 0x0000 is reserved and should not be used.
15–8 CC	Command Completions. This field specifies the number of command completions that are necessary to cause a CCC interrupt. The value 0x00 for this field disables CCC interrupts being generated based on the number of commands completed. In this case, CCC interrupts are only generated based on the timer. Software loads this value prior to enabling CCC: Field access is: • RW when SATA_CCC_CTL[EN]==0 • RO when SATA_CCC_CTL[EN]==1
7–3 INT	Interrupt. Set this field to 0x01.
2–1 -	This field is reserved. Reserved.
0 EN	Enable. **NOTE:** When field SATA_CCC_CTL[EN]==1, the software can not change the fields SATA_CCC_CTL[TV] and SATA_CCC_CTL[CC]. The options for this field are: 0 CCC feature is disabled and no CCC interrupts are generated. 1 CCC feature is enabled and CCC interrupts may be generated based on the time-out or command completion conditions.

53.7.7 Command Completion Coalescing Ports (SATA_CCC_PORTS)

This register specifies the Ports that are coalesced as part of the command completion coalescing (CCC) feature when SATA_CCC_CTL[EN]==1. It is reset on Global reset.

Address: 220_0000h base + 18h offset = 220_0018h



SATA_CCC_PORTS field descriptions

Field	Description
PRT	Ports. This field is bit significant. Each bit corresponds to a particular Port, where bit 0 corresponds to Port0.

SATA_CCC_PORTS field descriptions (continued)

Field	Description
	Bits set in this register must have the corresponding bit set in the SATA_PI (Ports Implemented Register). The options for this field are: 1 the corresponding Port is part of the CCC feature. 0 the corresponding Port is not part of the CCC feature.

53.7.8 HBA Capabilities Extended Register (SATA_CAP2)

This register indicates capabilites of the SATA block core to the software.

Address: 220_0000h base + 24h offset = 220_0024h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved													APST	Reserved	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

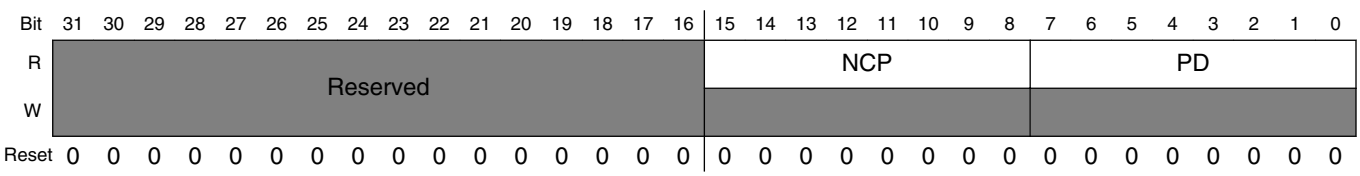
SATA_CAP2 field descriptions

Field	Description
31–3 -	This field is reserved. Reserved
2 APST	Automatic Partial to Slumber Transitions. SATA block supports automatic Partial to Slumber transitions.
-	This field is reserved. Reserved.

53.7.9 BIST Activate FIS Register (SATA_BISTAFR)

This register contains the pattern definition (bits [23:16] of the first DWORD) and data pattern (bits [7:0] of the second DWORD) fields of the received BIST Activate FIS. These fields define the SATA block loopback responder mode requested by the device. It is updated every time a new BIST Activate FIS is received from the device. Reset on Global or Port reset.

Address: 220_0000h base + A0h offset = 220_00A0h



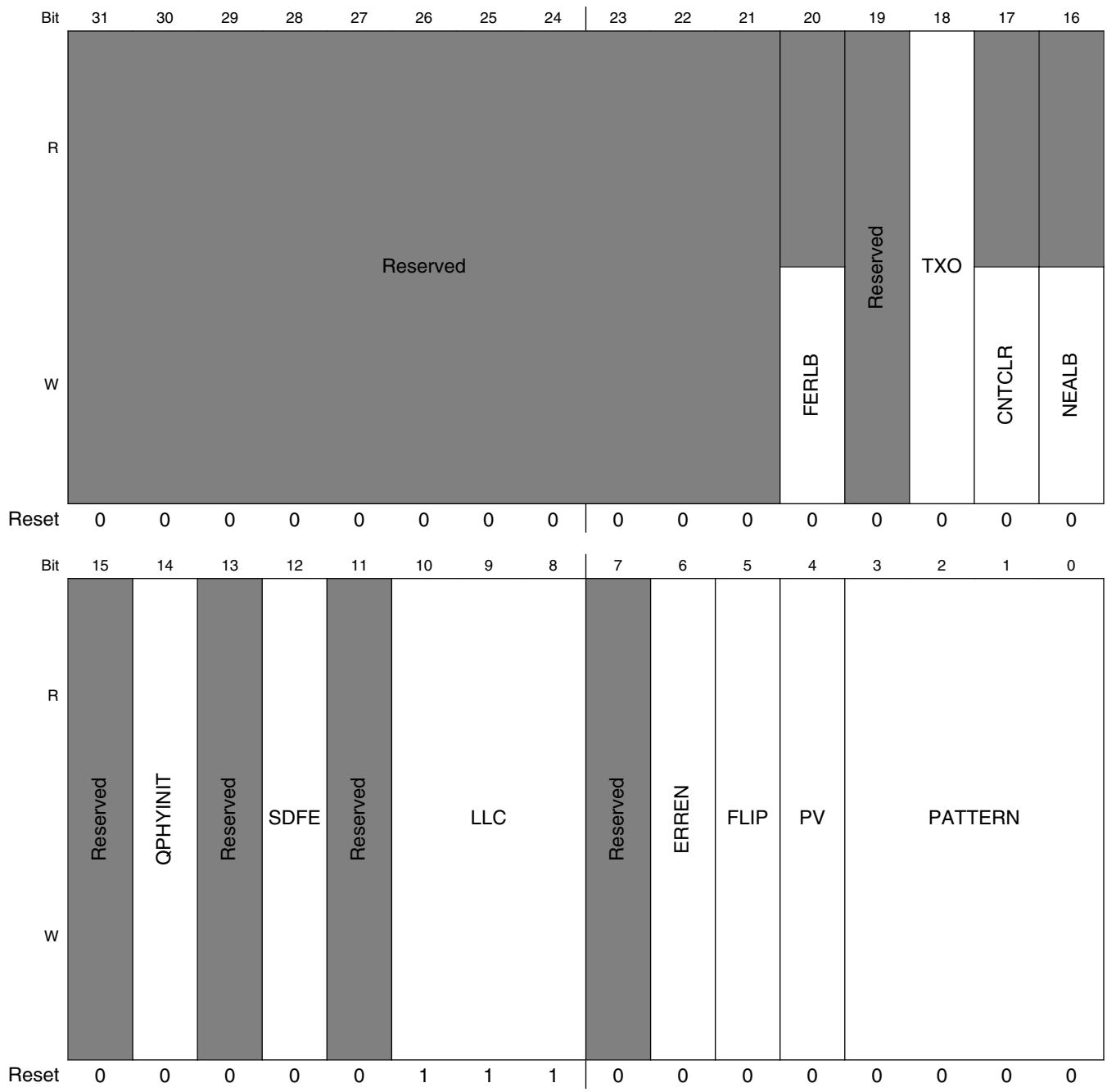
SATA_BISTAFR field descriptions

Field	Description
31–16 -	This field is reserved. Reserved.
15–8 NCP	Least significant byte of the received BIST Activate FIS second DWORD (bits [7:0]). This value defines the required pattern for far-end transmit only mode (SATA_BISTAFR[PD]=0x80 or 0xA0): When none of these values is decoded, the simultaneous switching pattern is transmitted by default. 0xF1 Low transition density pattern (LTDP) 0xB5 High transition density pattern (HTDP) 0xAB Low frequency spectral component pattern (LFSCP) 0x7F Simultaneous switching outputs pattern (SSOP) 0x8B Lone Bit pattern (LBP) 0x78 Mid frequency test pattern (MFTP) 0x4A High frequency test pattern (HFTP) 0x7E Low frequency test pattern (LFTP)
PD	Pattern Definition Indicates the pattern definition field of the received BIST Activate FIS - bits [23:16] of the first DWORD. It is used to put the SATA block in one of the following BIST modes: For far-end transmit only modes SATA_BISTAFR[NCP] field contains the required data pattern. 0x10 Far-end retimed 0x08 Far-end analog (when PHY supports this mode) 0x80 Far-end transmit only 0xA0 Far-end transmit only with scrambler bypassed All other values should not be used by the device, otherwise, the FIS is negatively acknowledged with R_ERRp.

53.7.10 BIST Control Register (SATA_BISTCR)

This register is used in BIST initiator modes. It is loaded by the host software prior to sending BIST Activate FIS to the device (via TXBISTPD write). It is reset on a Global or Port reset.

Address: 220_0000h base + A4h offset = 220_00A4h



SATA_BISTCR field descriptions

Field	Description
31–21 -	This field is reserved. Reserved.
20 FERLB	Far-end Retimed Loopback. When set, this bit is used to put the SATA block Link into Far-end Retimed mode, without the BIST Activate FIS, regardless whether the device is connected or disconnected (Link in NOCOMM state). This field is one-shot type and reads returns 0.
19 -	This field is reserved. Reserved.
18 TXO	Transmit Only. This bit is used to initiate transmission of one of the non-compliant patterns defined by the SATA_BISTCR[PATTERN] value when the device is disconnected.
17 CNTCLR	Counter Clear This bit clears BIST error count registers. This field is one-shot type and reads returns 0. 1 Clear SATA_BISTFCTR, and SATA_BISTSR registers.
16 NEALB	Near-End Analog Loopback This mode should be initiated either in the PARTIAL or SLUMBER power mode, or with the device disconnected from the Port PHY (Link NOCOMM state). BIST Activate FIS is not sent to the device in this mode. This bit places the Port PHY into near-end analog loopback mode. This field is one-shot type and reads returns 0: 1 Near-end analog loopback request. SATA_BISTCR[PATTERN] field contains the appropriate pattern.
15 -	This field is reserved. Reserved.
14 QPHYINIT	When set, this bit enables quick PHY initialization feature. The Link does not require any ALIGNs to transition from OOB to normal operation. **NOTE:** This bit is available only when TX_OOB_MODE = Exclude (0) and ALIGN_MODE = Aligned (1), otherwise it is reserved.
13 -	This field is reserved. Reserved.
12 SDFE	Signal Detect Feature Enable Reset: PHY_INTERFACE_TYPE 1: Link layer feature to handle unstable/absent phy_sig_det signal is enabled 0: Link layer feature to handle unstable/absent phy_sig_det signal is disabled. This bit is set on power-up or asynchronous reset if PHY_INTERFACE_TYPE = Synopsys_SATA_II (1) or PHY_INTERFACE_TYPE = Synopsys_SATA_6G (2), otherwise, the bit is cleared until it is set via programming. It is not affected by a Global reset or COMRESET. **NOTE:** For special handling in systems where phy_sig_det may not be present or stable after OOB signalling and during normal operation . For these systems, phy_rx_data_vld must not be tied high and must go low when no data is detected on the wires.
11 -	This field is reserved. Reserved.
10–8 LLC	Link Layer Control This field controls the Port Link Layer functions: scrambler, descrambler, and repeat primitive drop. Note the different meanings for normal and BIST modes of operation:

Table continues on the next page...

SATA_BISTCR field descriptions (continued)

Field	Description
	• Bit8-SCRAM The options for this field are: 0 Scrambler disabled in normal mode, enabled in BIST mode 1 Scrambler enabled in normal mode, disabled in BIST mode • Bit9-DESCRAM The options for this field are: 0 Descrambler disabled in normal mode, enabled in BIST mode 1 Descrambler enabled in normal mode, disabled in BIST mode • Bit10-RPD The options for this field are: 0 Repeat primitive drop function disabled in normal mode, NA in BIST mode. 1 Repeat primitive drop function enabled in normal mode, NA in BIST mode. The SCRAM bit is cleared (enabled) by the Port when the Port enters a responder far-end transmit BIST mode with scrambling enabled (SATA_BISTAFR[PD]=0x80). In normal mode, the functions scrambler, descrambler, or RPD can be changed only during Port reset (SATA_P 0 SCTL[DET]=0x1)
7 -	This field is reserved. Reserved.
6 ERREN	Error Enable. This bit is used to allow or filter (disable) [internal errors outside the FIS boundary to set corresponding SATA_P 0 SERR bits. The options for this field are: 0 Filter errors outside the FIS, allow errors inside the FIS; 1 Allow errors outside or inside the FIS.
5 FLIP	Flip Disparity This bit is used to change disparity of the current test pattern to the opposite every time its state is changed by the software.
4 PV	Pattern Version This bit is used to select either short or long version of the SSOP, HTDP, LTDP, LFSCP, COMP patterns. The options for this field are: 0 Short pattern version 1 Long pattern version
PATTERN	This field defines one of the following SATA compliant patterns for far-end retimed/ far-end analog/ near-end analog initiator modes, or non-compliant patterns for transmit-only responder mode when initiated by the software writing to the SATA_BISTCR[TXO] bit. If the value is none of the listed below, Composite pattern (COMP) is transmitted by default. 0000b Simultaneous switching outputs pattern (SSOP)

Table continues on the next page...

SATA_BISTCR field descriptions (continued)

Field	Description	
	0001b	High transition density pattern (HTDP)
	0010b	Low transition density pattern (LTDP)
	0011b	Low frequency spectral component pattern (LFSCP)
	0100b	Composite pattern (COMP)
	0101b	Lone bit pattern (LBP)
	0110b	Mid frequency test pattern (MFTP)
	0111b	High frequency test pattern (HFTP)
	1000b	Low frequency test pattern (LFTP)
	All other values	Reserved and should not be used.

53.7.11 BIST FIS Count Register (SATA_BISTFCTR)

This register contains the received BIST FIS count in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST FIS is received. It is reset by Global reset, Port reset (COMRESET) or by setting the SATA_BISTCR[CNTCLR] bit. This register does not roll over and freezes when the FFFF_FFFFh value is reached. It takes approximately 65 hours of continuous BIST operation to reach this value.

Address: 220_0000h base + A8h offset = 220_00A8h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	-																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

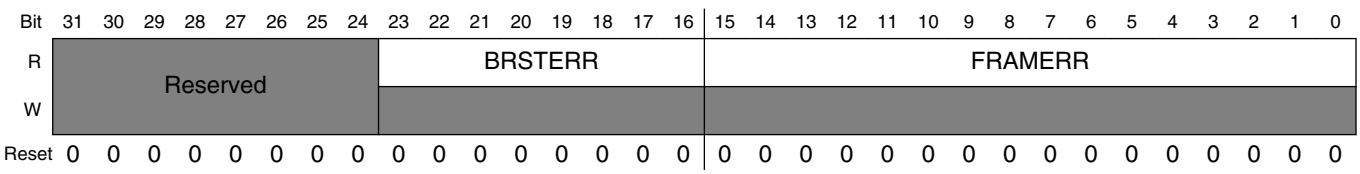
SATA_BISTFCTR field descriptions

Field	Description
-	Received BIST FIS Count

53.7.12 BIST Status Register (SATA_BISTSR)

This register contains errors detected in the received BIST FIS in the loopback initiator far-end retimed, far- end analog and near-end analog modes. It is updated each time a new BIST FIS is received. It is reset by Global reset, Port reset (COMRESET) or by setting the SATA_BISTCR[CNTCLR] bit.

Address: 220_0000h base + ACh offset = 220_00ACh



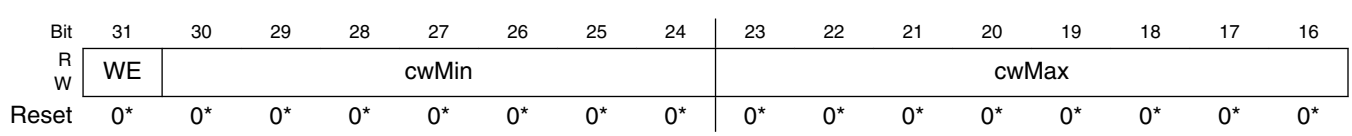
SATA_BISTSR field descriptions

Field	Description
31–24 -	This field is reserved. Reserved.
23–16 BRSTERR	Burst Error. This field contains the burst error count. It is accumulated each time a burst error condition is detected: DWORD error is detected in the received frame and 1.5 seconds (27,000 frames) passed since the previous burst error was detected. The BRSTERR value does not roll over and freezes at FFh. This field is updated when parameter BIST_MODE=DWORD.
FRAMERR	Frame Error. This field contains the frame error count. It is accumulated (new value is added to the old value) each time a new BIST frame with a CRC error is received. The FRAMERR value does not roll over and freezes at FFFFh.

53.7.13 OOB Register (SATA_OOBR)

This register controls the Link layer OOB detection counters. The default values, MIN_COMWAKE, MAX_COMWAKE, MIN_COMINIT and MAX_COMINIT are calculated based on the RXOOB_CLK parameter and loaded on power-up or asynchronous SATA block reset.

Address: 220_0000h base + BCh offset = 220_00BCh



Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	ciMin								ciMax							
Reset	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*	0*

* Notes:
- See descriptions for reset values.

SATA_OOBR field descriptions

Field	Description
31 WE	Write Enable This bit is cleared when COMRESET is detected. The options for this field are: 1 SATA_OOBR bits [30:0] can be written 0 SATA_OOBR bits [30:0] are read-only
30–24 cwMin	COMWAKE Minimum Value This field is RW when WE=1 and RO when WE=0.
23–16 cwMax	COMWAKE Maximum Value This field is RW when WE=1 and RO when WE=0.
15–8 ciMin	COMINIT Minimum Value This field is RW when WE=1 and RO when WE=0.
ciMax	COMINIT Maximum Value This field is RW when WE=1 and RO when WE=0.

53.7.14 General Purpose Control Register (SATA_GPCR)

This 32-bit register is used for general purpose control. This register only exists when GP_CTRL parameter is set to “Include” otherwise this location is reserved.

The bits of this register are connected to the corresponding bits of the gp_ctrl output. Resets on power-up (system reset) only to the GP_CTRL_DEF value.

Address: 220_0000h base + D0h offset = 220_00D0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	GP_CONTROL																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_GPCR field descriptions

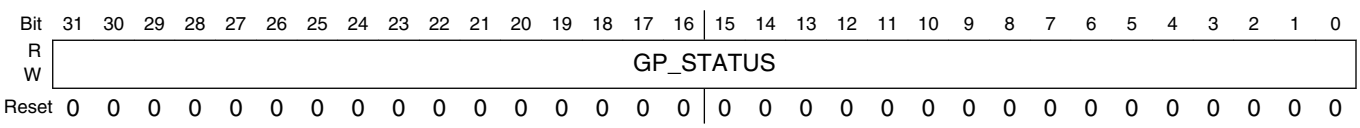
Field	Description
GP_CONTROL	General Purpose Control. Present only when GP_CTRL=Include(1). Reset Value: Configurable parameter GP_CTRL_DEF

53.7.15 General Purpose Status Register (SATA_GPSR)

This 32-bit register is used to monitor the general purpose status. This register only exists when GP_STAT parameter is set to “Include”, otherwise, this location is reserved.

The bits of this register reflect the state of the corresponding bits of the gp_status input. Signals connected to the gp_status input can be asynchronous to any of the DWC_ahsata clocks, however they must not change faster than five hclk/aclk periods, otherwise the GPSR register may never be updated with the intermediate changing values.

Address: 220_0000h base + D4h offset = 220_00D4h



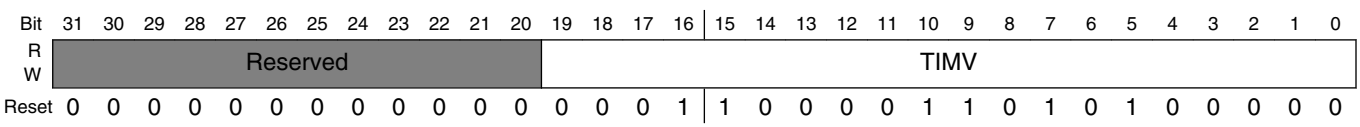
SATA_GPSR field descriptions

Field	Description
GP_STATUS	General Purpose Status. Present only when GP_STAT=Include(1)

53.7.16 Timer 1-ms Register (SATA_TIMER1MS)

This register is used to generate a 1-ms tick for the command completion coalescing (CCC) logic, based on the AHB bus clock frequency. The Software must initialize this register with the required value after power up before using the CCC feature. This register is reset to 100,000 (TIMV value for 100-MHz hclk) on power up and is not affected by Global reset.

Address: 220_0000h base + E0h offset = 220_00E0h



SATA_TIMER1MS field descriptions

Field	Description
31–20 -	This field is reserved. Reserved.
TIMV	1ms Timer Value This field contains the following value for the internal timer to generate 1-ms tick:

Table continues on the next page...

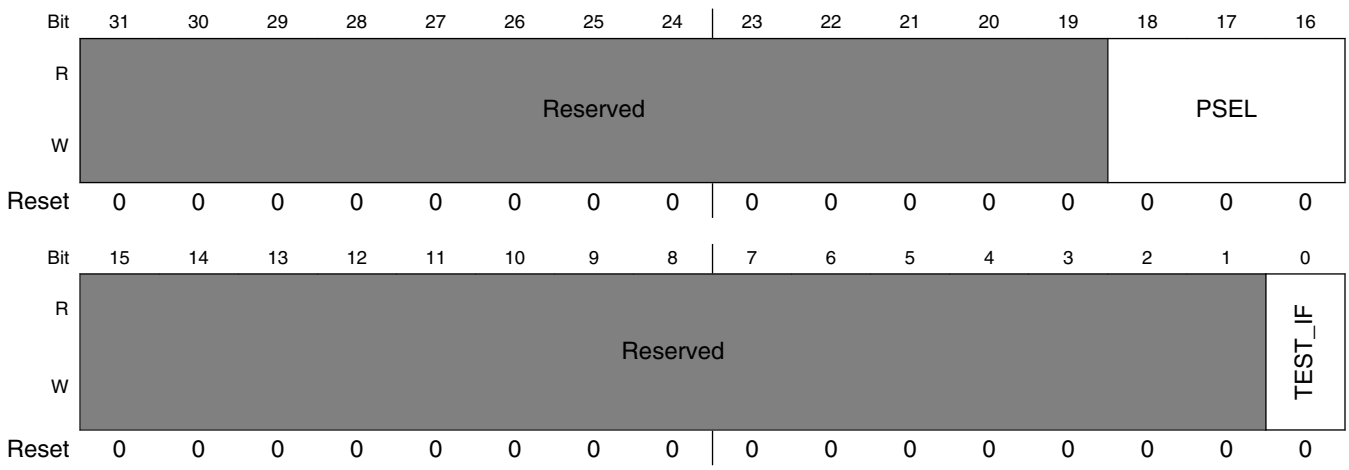
SATA_TIMER1MS field descriptions (continued)

Field	Description
	Fhclk*1000 where Fhclk = AHB clock frequency in MHz The options for this field are: • RW when SATA_CCC_CTL[EN]==0 • RO when SATA_CCC_CTL[EN]==1.

53.7.17 Test Register (SATA_TESTR)

This register is used to put the SATA block slave interface into a test mode and to select a Port for BIST operation.

Address: 220_0000h base + F4h offset = 220_00F4h



SATA_TESTR field descriptions

Field	Description
31–19 -	This field is reserved. Reserved
18–16 PSEL	Port Select This field is used to select a Port for BIST operation: The options for this field are: 0x0 Port0 is selected 0x0 Port1 is selected 0x0 Port2 is selected 0x0 Port3 is selected 0x0 Port4 is selected 0x0 Port5 is selected

Table continues on the next page...

SATA_TESTR field descriptions (continued)

Field	Description
	0x0 Port6 is selected 0x0 Port7 is selected
15–1 -	This field is reserved. Reserved
0 TEST_IF	TEST_IF: Test Interface Normal operation is disabled. The following registers can be accessed in this mode: - SATA_GHC register IE bit - SATA_BISTAFR register NCP and PD bits become read-write - SATA_BISTCR register LLC, ERREN, FLIP, PV, PATTERN - SATA_BISTFCTR, SATA_BISTSR become read-write - SATA_P 0 CLB , SATA_P 0 FB registers - SATA_P 0 IS register RW1C and UFS bits become read-write - SATA_P 0 IE register - SATA_P 0 CMD register ASP, ALPE, DLAE, ATAPI, PMA bits - SATA_P 0 TFD, SATA_P 0 SIG registers become read-write - SATA_P 0 SCTL register - SATA_P 0 SERR register RW1C bits become read-write bits - SATA_P 0 SACT, SATA_P 0 CI, SATA_P 0 SNTF registers become read-write - SATA_P 0 DMACR register - SATA_P 0 PHYCR register - SATA_P 0 PHYSR register becomes read-write Notes: • Interrupt is asserted when any of the SATA_IS register bits is set after setting the corresponding SATA_P 0 IS and SATA_P 0 IE registers and SATA_GHC[IE]=1. • SATA_CAP[SMPS], SATA_CAP[SSS], SATA_PI, SATA_P 0 CMD[ESP], SATA_P 0 CMD[CPD], SATA_P 0 CMD[MPSP], and SATA_P 0 CMD[HPCP] register bits are HwInit type and can not be used in Test mode. They are written once after power-on reset and become read-only. • Global SATA block reset must be issued (SATA_GHC[HR]=1) after TEST_WHEN bit is cleared following the Test mode operation. This bit is used to put the SATA block slave interface into the test mode: The options for this field are: 0 Normal mode: the read back value of some registers is a function of the SATA block state and does not match the value written. 1 Test mode: the read back value of the registers matches the value written.

53.7.18 Version Register (SATA_VERSIONR)

This 32-bit read-only register contains a hard-coded ASCII string that represents the version level of the SATA block. This register contains the ASCII string "300*" (hexadecimal 0x3330302A).

Address: 220_0000h base + F8h offset = 220_00F8h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	-																															
W																																
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1	0	1	0

SATA_VERSIONR field descriptions

Field	Description
-	SATA block hard-coded hexadecimal version value encoded in ASCII.

53.7.19 Port0 Command List Base Address Register (SATA_P0CLB)

Address: 220_0000h base + 100h offset = 220_0100h

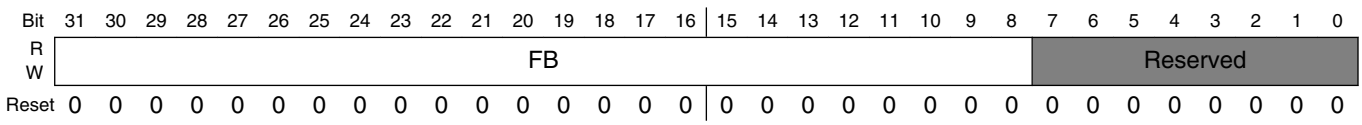
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CLB																						Reserved									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_P0CLB field descriptions

Field	Description
31–10 CLB	Command List Base Address Indicates the 32-bit base physical address for the command list for this Port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1 KB in length. This address must be 1-KB-aligned as indicated by bits [9:0] being read only.
-	This field is reserved. Reserved.

53.7.20 Port0 FIS Base Address Register (SATA_P0FB)

Address: 220_0000h base + 108h offset = 220_0108h



SATA_P0FB field descriptions

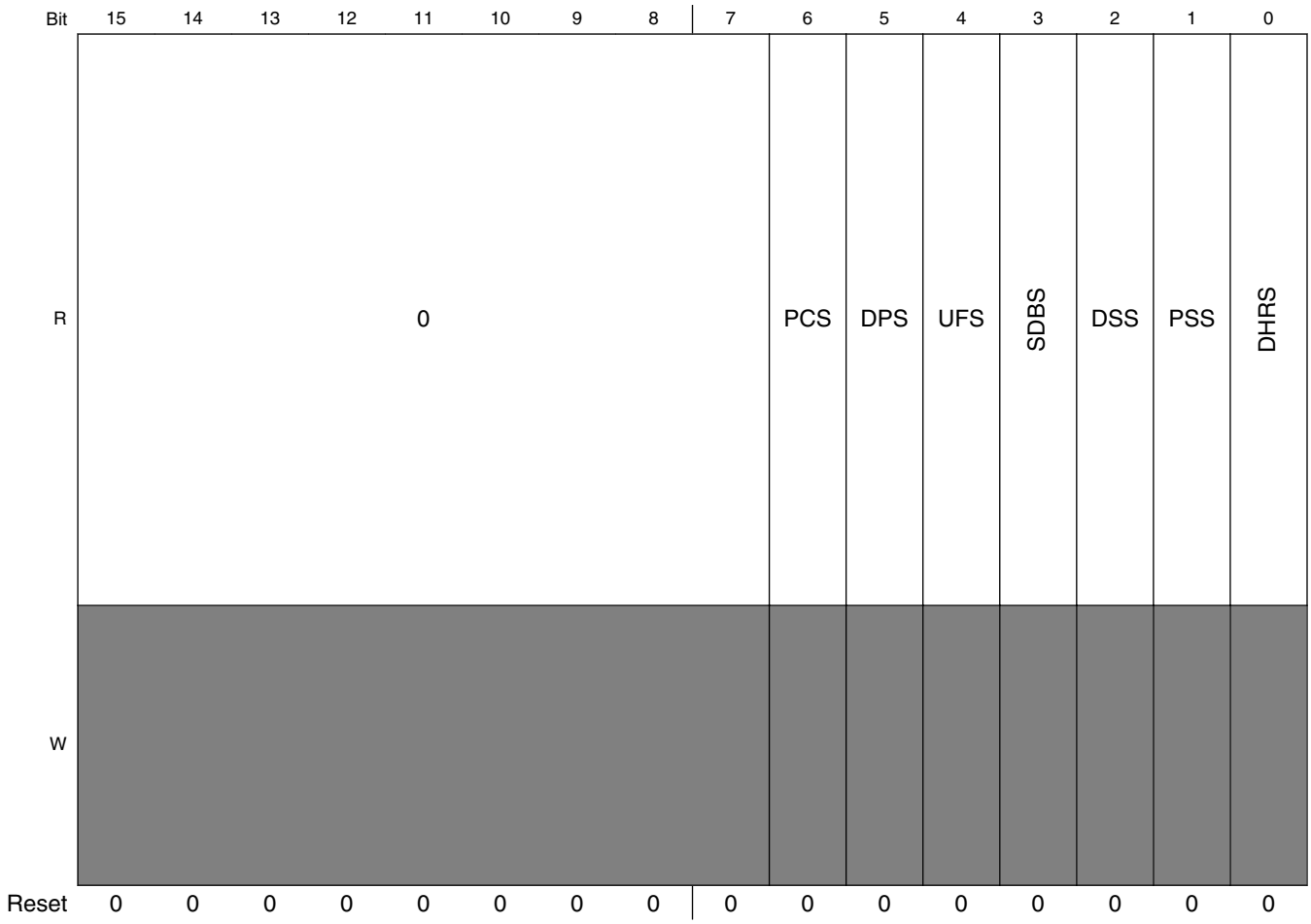
Field	Description
31–8 FB	FIS Base Address. Indicates the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256byte-aligned as indicated by bits [7:0] being read only. Reset: 0x000000
-	This field is reserved. Reserved.

53.7.21 Port0 Interrupt Status Register (SATA_P0IS)

This register is used to generate SATA block interrupt when any of the bits are set. Bits in this register are set by some internal conditions, and cleared by the software writing ones in the positions it wants to clear. This register is reset on Global SATA block reset.

Address: 220_0000h base + 110h offset = 220_0110h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	TFES	HBFS	HBDS	IFS	INFS	Reserved	OFS	IPMS	PRCS	0					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



SATA_P0IS field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30 TFES	Task File Error Status. This bit is set whenever the SATA_P 0 TFD[STS] register is updated by the device and the error bit (bit 0) is set.
29 HBFS	Host Bus Fatal Error Status. This bit is set when SATA block AHB Master detects an ERROR response from the slave.
28 HBDS	Host Bus Data Error Status. This bit is always cleared to 0.
27 IFS	Interface Fatal Error Status This bit is set when any of the following conditions is detected: • SYNC escape is received from the device during H2D Register or Data FIS transmission; • One or more of the following errors are detected during Data FIS transfer: - 10B to 8B Decode Error (SATA_P 0 SERR[DIAG_B])

Table continues on the next page...

SATA_P0IS field descriptions (continued)

Field	Description
	- Protocol (SATA_P 0 SERR[ERR_P]) - CRC (SATA_P 0 SERR[DIAG_C]) - Handshake (SATA_P 0 SERR[DIAG_H]) - PHY Not Ready (SATA_P 0 SERR[ERR_C]) • Unknown FIS is received with good CRC, but the length exceeds 64 bytes; • PRD table byte count is zero. Port DMA transitions to a fatal state until the software clears SATA_P 0 CMD[ST] bit or resets the interface by way of Port or Global reset.
26 INFS	Interface Non-fatal Error Status This bit is set when any of the following conditions is detected: • One or more of the following errors are detected during non-data FIS transfer - 10B to 8B Decode Error (SATA_P 0 SERR[DIAG_B]) - Protocol (SATA_P 0 SERR[ERR_P]) - CRC (SATA_P 0 SERR[DIAG_C]), - Handshake (SATA_P 0 SERR[DIAG_H]) - PHY Not Ready (SATA_P 0 SERR[ERR_C]); • Command list underflow during read operation (i.e. DMA read) when the software builds command table that has more total bytes than the transaction given to the device.
25 -	This field is reserved. Reserved
24 OFS	Overflow Status This bit is set when command list overflow is detected during read or write operation when the software builds command table that has fever total bytes than the transaction given to the device. Port DMA transitions to a fatal state until the software clears SATA_P 0 CMD[ST] bit or resets the interface by way of Port or Global reset.
23 IPMS	Incorrect Port Multiplier Status. Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. This bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. The software must use the IPMS bit only after enumeration is complete on the Port Multiplier.
22 PRCS	PHY Ready Change Status This bit reflects the state of the SATA_P 0 SERR[DIAG_N] bit. When set to 1, indicates the internal p 0 _phy_ready signal changed state. To clear this bit, the software must clear the SATA_P 0 SERR[DIAG_N] bit to 0.
21–7 Reserved	This read-only field is reserved and always has the value 0.
6 PCS	Port Connect Change Status

Table continues on the next page...

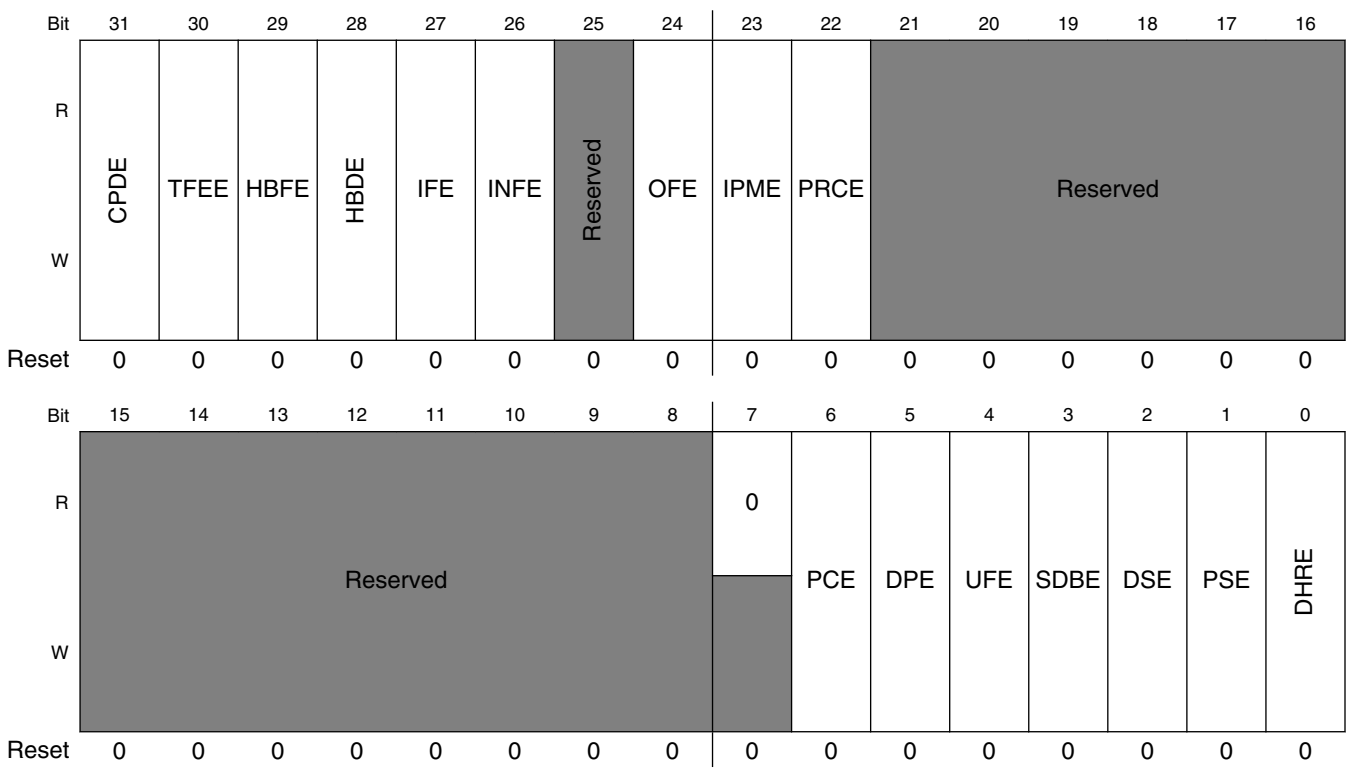
SATA_P0IS field descriptions (continued)

Field	Description
	This bit is cleared only when SATA_P 0 SERR[DIAG_X] is cleared. This bit reflects the state of the SATA_P 0 SERR[DIAG_X] bit: 1 Change in Current Connect Status; 0 No change in Current Connect Status.
5 DPS	Descriptor Processed A PRD with the I bit set has transferred all of its data. **NOTE:** This is an opportunistic interrupt and must not be used to definitively indicate the end of a transfer. Two PRD interrupts could happen close in time together such that the second interrupt is missed when the first PRD interrupt is being cleared.
4 UFS	Unknown FIS Interrupt. When set to 1, indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by the software clearing the SATA_P 0 SERR[DIAG_F] bit to 0. **NOTE:** The UFS bit does not directly reflect the SATA_P 0 SERR[DIAG_F] bit. SATA_P 0 SERR[DIAG_F] bit is set immediately when an unknown FIS is detected, whereas the UFS bit is set when that FIS is posted to memory. The software should wait to act on an unknown FIS until the UFS bit is set to 1 or the two bits may become out of sync.
3 SDBS	Set Device Bits Interrupt. A Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.
2 DSS	DMA Setup FIS Interrupt A DMA Setup FIS has been received with the 'I' bit set and has been copied into system memory.
1 PSS	PIO Setup FIS Interrupt. A PIO Setup FIS has been received with the 'I' bit set, it has been copied into system memory, and the data related to that FIS has been transferred. **NOTE:** This bit is set even when the data transfer resulted in an error.
0 DHRS	Device to Host Register FIS Interrupt A D2H Register FIS has been received with the 'I' bit set, and has been copied into system memory.

53.7.22 Port0 Interrupt Enable Register (SATA_P0IE)

This register enables and disables the reporting of the corresponding interrupt to the software. When a bit is set (1), and the corresponding interrupt condition is active, then the SATA block intrq output is asserted. Interrupt sources that are disabled (0) are still reflected in the status registers. This register is symmetrical with the SATA_P 0 IS register. This register is reset on Global SATA block reset.

Address: 220_0000h base + 114h offset = 220_0114h



SATA_P0IE field descriptions

Field	Description
31 CPDE	Cold Port Detect Enable Read-only. Returns 0.
30 TFEE	Task File Error Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[TFES]=1

Table continues on the next page...

SATA_P0IE field descriptions (continued)

Field	Description
29 HBFE	Host Bus Fatal Error Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[HBFS]=1
28 HBDE	Host Bus Data Error Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[HBDS]=1
27 IFE	Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[IFS]=1
26 INFE	Interface Non-Fatal Error Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[INFS]=1
25 -	This field is reserved. Reserved
24 OFE	Overflow Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[OFS]=1
23 IPME	Incorrect Port Multiplier Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[IPMS]=1
22 PRCE	PHY Ready Change Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[PRCS]=1
21–8 -	This field is reserved. Reserved.

Table continues on the next page...

SATA_P0IE field descriptions (continued)

Field	Description
7 Reserved	This read-only field is reserved and always has the value 0.
6 PCE	Port Change Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[PCS]=1
5 DPE	Descriptor Processed Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[DPS]=1
4 UFE	Unknown FIS Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[UFS]=1
3 SDBE	Set Device Bits FIS Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[SDBS]=1
2 DSE	DMA Setup FIS Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[DSS]=1
1 PSE	PIO Setup FIS Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[PSS]=1
0 DHRE	Device to Host Register FIS Interrupt Dependencies: when the following conditions are true, the intrq output signal is asserted: • This bit=1 • SATA_GHC[IE]=1 • SATA_P 0 IS[DHRS]=1

53.7.23 Port0 Command Register (SATA_P0CMD)

This register contains bits controlling various Port functions. All RW bits are reset on Global reset.

Address: 220_0000h base + 118h offset = 220_0118h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	ICC				ASP	ALPE	DLAE	ATAPI	APSTE	Reserved	ESP	Reserved	Reserved	HPCP	PMA	CPS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CR	FR	MPSS	CCS					Reserved			FRE	CLO	POD	SUD	ST
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_P0CMD field descriptions

Field	Description
31–28 ICC	Interface Communication Control This field is used to control power management states of the interface. When the Link layer is currently in the L_IDLE state, writes to this field cause the Port to initiate a transition to the interface power management state requested. When the Link layer is not currently in the L_IDLE state, writes to this field have no effect. • 0xF-0x7: Reserved • 0x6: Slumber. This causes the Port to request a transition of the interface to the Slumber state. The SATA device can reject the request and the interface remains in its current state. • 0x5-0x3: Reserved • 0x2: Partial. This causes the Port to request a transition of the interface to the Partial state. The SATA device can reject the request and the interface remains in its current state. • 0x1: Active. This causes the Port to request a transition of the interface into the active state.

Table continues on the next page...

SATA_P0CMD field descriptions (continued)

Field	Description
	• 0x0: No-Op/ Idle. This value indicates to the software that the Port 0 is ready to accept a new interface control command, although the transition to the previously selected state may not yet have occurred. When the software writes a non-reserved value other than No-Op (0x0), the Port performs the action and update this field back to Idle (0x0). When the software writes to this field to change the state to a state the link is already in (i.e., interface is in the active state and a request is made to go to the active state), the Port takes no action and returns this field to Idle. When the interface is in a low power state and the software wants to transition to a different low power state, the software must first bring the link to active and then initiate the transition to the desired low power state.
27 ASP	Aggressive Slumber/ Partial The options for this field are: • When set to 1, and SATA_P 0 CMD[ALPE]=1, the Port aggressively enters the SLUMBER state when one of the following conditions is true: - The Port clears the SATA_P 0 CI and the SATA_P 0 SACT register is cleared. - The Port clears the SATA_P 0 SACT register and SATA_P 0 CI is cleared. • When cleared to 0, and SATA_P 0 CMD[ALPE]=1, the Port aggressively enters the PARTIAL state when one of the following conditions is true: - The Port clears the SATA_P 0 CI register and the SATA_P 0 SACT register is cleared. - The Port clears the SATA_P 0 SACT register and SATA_P 0 CI is cleared.
26 ALPE	Aggressive Link Power Management Enable When set to 1, the Port aggressively enters a lower link power state (PARTIAL or SLUMBER) based on the setting of the SATA_P 0 CMD[ASP] bit. When cleared to 0, aggressive power management state transition is disabled.
25 DLAE	Drive LED on ATAPI Enable When set to 1, SATA_P 0 CMD[ATAPI]=1, and commands are active, the Port asserts p 0 _act_led output.
24 ATAPI	ATAPI Device is ATAPI This bit is used by the Port to control whether to assert p 0 _act_led output when commands are active. The options for this field are: 0 non-ATAPI device 1 ATAPI device
23 APSTE	Device is ATAPI This bit is used by the Port to control whether to assert p 0 _act_led output when commands are active. The options for this field are: 0 non-ATAPI device 1 ATAPI device
22 -	This field is reserved. Reserved
21 ESP	External SATA Port When set to 1, indicates that this Port's signal only connector is externally accessible. When set to 1, SATA_CAP[SXS] is also set to 1.

Table continues on the next page...

SATA_P0CMD field descriptions (continued)

Field	Description
	When cleared to 0, indicates that this Port's signal only connector is not externally accessible. Note: The ESP bit is mutually exclusive with SATA_P 0 CMD[HPCP]
20 -	This field is reserved. Reserved. Returns 0 on read.
19 -	This field is reserved. Reserved. Returns 0 on read.
18 HPCP	Hot Plug Capable Port **NOTE:** The HPCP bit is mutually exclusive with SATA_P 0 CMD[ESP]. The options for this field are: 1 Indicates that this Port's signal and power connectors are externally accessible via a joint signal-power connector for blindmate device hot plug. 0 Indicates that this Port's signal and power connectors are not externally accessible.
17 PMA	Port Multiplier Attached The software is responsible for detecting whether a Port Multiplier is present; the SATA block Port does not auto-detect the presence of a Port Multiplier. The options for this field are: 1 A Port Multiplier is attached to this Port. 0 A Port Multiplier is not attached to this Port.
16 CPS	Cold Presence State This bit reports whether a device is currently detected on this Port as indicated by the p 0 _cp_det input state (assuming SATA_P 0 CMD[CPD]=1). The options for this field are: 1 device is attached to this Port 0 no device attached to this Port
15 CR	Command List Running When this bit is set to '1', the command list DMA engine for this Port is running. See AHCI state machine in AHCI specification section 5.3.2 for details on when this bit is set and cleared by the Port.
14 FR	FIS Receive Running When set to '1', the FIS Receive DMA engine for the Port is running. See AHCI specification section 10.3.2 for details on when this bit is set and cleared by the Port.
13 MPSS	Mechanical Presence Switch State The software must use this bit only when both SATA_CAP[SMPS] and SATA_P 0 CMD[MPSP] are set. This bit reports the state of a mechanical presence switch attached to this Port as indicated by the p 0 _mp_switch input state (assuming SATA_CAP[SMPS]=1 and SATA_P 0 CMD[MPSP]=1). The options for this field are: When SATA_CAP[SMPS]=0 then this bit is cleared to 0. 0 Switch is closed 1 Switch is open
12–8 CCS	Current Command Slot This field is set to the command slot value value of the command that is currently being issued by the Port.

Table continues on the next page...

SATA_P0CMD field descriptions (continued)

Field	Description
	• When SATA_P 0 CMD[ST] transitions from 1 to 0, this field is recleared to 0x00. • After SATA_P 0 CMD[ST] transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is SATA_P 0 CMD[CCS]+1.For example, after the Port has issued its first command, when CCS=0x00 and SATA_P 0 CI is cleared to 0x3, the next command issued is from command slot 1. This field is valid only when SATA_P 0 CMD[ST] is set to 1.
7–5 -	This field is reserved. Reserved.
4 FRE	FIS Receive Enable When set to 1, the Port may post received FISes into the FIS receive area pointed to by SATA_P 0 FB . When cleared, received FISes are not accepted by the Port, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. The software must not set this bit until SATA_P 0 FB has been programmed with a valid pointer to the FIS receive area When the software wishes to move the base, this bit must first be cleared, and the software must wait for the SATA_P 0 CMD[FR] bit to be cleared.
3 CLO	Command List Override Setting this bit to 1 causes the SATA_P 0 TFD[STS] field BSY bit and the SATA_P 0 TFD[STS] field DRQ bit to be cleared. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the SATA_P 0 TFD[STS] field. This bit is cleared to 0 when SATA_P 0 TFD[STS] BSY bit and SATA_P 0 TFD[STS] DRQ bit have been cleared. A write to this register with a value of '0' has no effect. This bit should only be set to 1 immediately prior to setting SATA_P 0 CMD[ST] bit to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and results in indeterminate behavior.
2 POD	Power On Device This bit is read/write when cold presence detection is supported on this Port as indicated by SATA_P 0 CMD[CPD]=1. This bit is read-only 1 when cold presence detection is not supported and SATA_P 0 CMD[CPD]=0. When set, the Port asserts the p 0 _cp_pod output pin so that it may be used to provide power to a cold-presence detectable Port.
1 SUD	Spin-Up Device This bit is read/write when staggered spin-up is supported as indicated by the SATA_CAP[SSS]=1. This bit is read-only 1 when staggered spin-up is not supported and SATA_CAP[SSS]=0. On an edge detect from 0 to 1, the Port starts a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Note: The SUD bit is read-only 0 on power-up until SATA_CAP[SSS] bit is written with the required value.
0 ST	Start When set to 1, the Port processes the command list. When cleared, the Port does not process the command list. Whenever this bit is changed from a 0 to a 1, the Port starts processing the command list at entry'0. Whenever this bit is changed from a 1 to a 0, the SATA_P 0 CI register is cleared by the Port upon transition into an idle state. Refer to AHCI specification, section 10.3.1, for important restrictions on when this bit can be set to 1. Note: SATA_P 0 SERR register must be cleared prior to setting ST bit to 1.

53.7.24 Port0 Task File Data Register (SATA_P0TFD)

This register contains Error and Status registers updated every time a new Register FIS, PIO Setup FIS, or Set Device Bits FIS is received from the device. Reset on Global or Port reset (COMRESET).

Address: 220_0000h base + 120h offset = 220_0120h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved																ERR								STS							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

SATA_P0TFD field descriptions

Field	Description
31–16 -	This field is reserved. Reserved
15–8 ERR	Error This field contains the latest copy of the task file error register.
STS	Status This field contains the latest copy of the task file status register. The bits that affect SATA block operation are: • Bit [7] BSY - Indicates the interface is busy • Bits [6:4] cs - Command specific • Bit [3] DRQ - Indicates a data transfer is requested • Bits [2:1] cs - Command specific • Bit [0] ERR - Indicates an error during the transfer **NOTE:** The Port updates the entire 8-bit field, not just the bits noted above.

53.7.25 Port0 Signature Register (SATA_P0SIG)

Address: 220_0000h base + 124h offset = 220_0124h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SIG																															
W																																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

SATA_P0SIG field descriptions

Field	Description
SIG	Signature This field contains the signature received from a device on the first D2H Register FIS. The bit order as follows: • Bits [31:24] - LBA High (Cylinder High) Register • Bits [23:16] - LBA Mid (Cylinder Low) Register • Bits [15:8] - LBA Low (Sector Number) Register • Bits [7:0] - Sector Count Register This field is updated once after a reset sequence. Reset on Global or Port reset.

53.7.26 Port0 Serial ATA Status Register (SATA_P0SSTS)

This 32-bit register conveys the current state of the interface and host. The Port updates it continuously and asynchronously. When the Port transmits a COMRESET to the device, this register is updated to its reset values (i.e., Global reset, Port reset, or COMINIT from the device

Address: 220_0000h base + 128h offset = 220_0128h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved																				IPM				SPD				Reserved			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_P0SSTS field descriptions

Field	Description
31–12 -	This field is reserved. Reserved
11–8 IPM	Interface Power Management Indicates the current interface state. The options for this field are: 0x0 Device not present or communication not established 0x1 Interface in active state 0x2 Interface in Partial power management state 0x6 Interface in Slumber power management state All other values Reserved
7–4 SPD	Current Interface Speed Indicates the negotiated interface communication speed. The options for this field are: 0x0 Device not present or communication not established

Table continues on the next page...

SATA_P0SSTS field descriptions (continued)

Field	Description
	0x1 1.5 Gb/s communication rate negotiated 0x2 3.0 Gb/s communication rate negotiated All other values Reserved and should not be used
DET	This field is reserved. Indicates the interface device detection and PHY state. The options for this field are: • 0x0: No device detected and PHY communication not established • 0x1: Device presence detected but PHY communication not established (COMINIT is detected) • 0x3: Device presence detected and PHY communication established (“PHY Ready” is detected) • 0x4: PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved.

53.7.27 Port0 Serial ATA Control {SControl} Register (SATA_P0SCTL)

This 32-bit read-write register is used by the software to control SATA interface capabilities. Writes to this register result in an action being taken by the Port PHY interface. Reads from the register return the last value written to it. Reset on Global reset.

These bits are static and should not be changed frequently due to the clock crossing between the Transport and Link Layers. The software must wait for at least seven periods of the slower clock (clk_asic 0 or hclk) before changing this register

Address: 220_0000h base + 12Ch offset = 220_012Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved																				IPM				SPD				DET			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_P0SCTL field descriptions

Field	Description
31–12 -	This field is reserved. Reserved
11–8 IPM	Interface Power Management Transitions Allowed This field indicates which power states the Port PHY interface is allowed to transition to. When an interface power management state is disabled, the Port does not initiate that state and any request from the device to enter that state is rejected via PMNAKp The options for this field are: 0x0 No interface power management state restrictions 0x1 Transitions to the Partial state disabled 0x2 Transitions to the Slumber state disabled

Table continues on the next page...

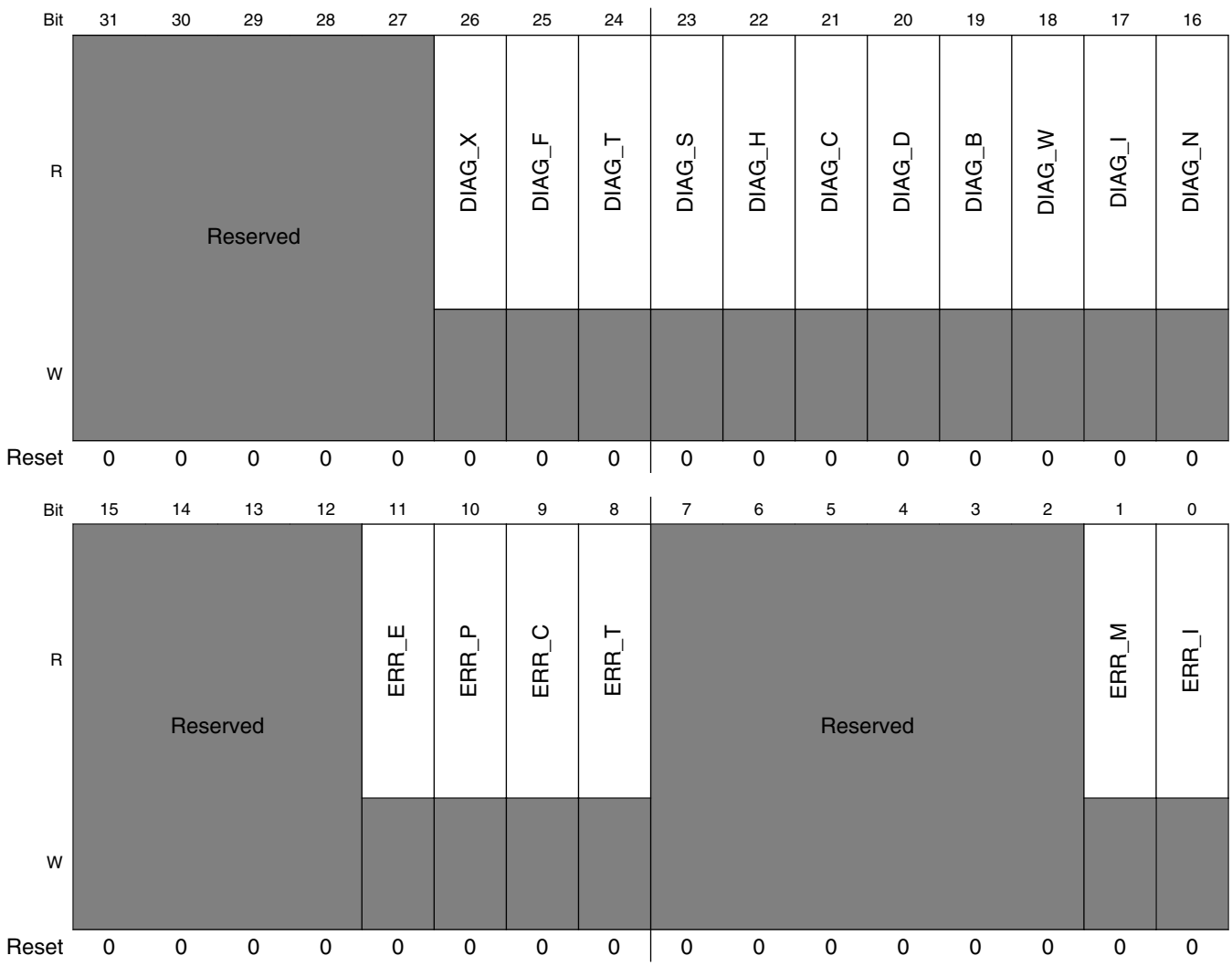
SATA_P0SCTL field descriptions (continued)

Field	Description
	0x3 Transitions to both Partial and Slumber states disabled All other values. Reserved and should not be used
7–4 SPD	Speed Allowed This field indicates the highest allowable speed of the Port PHY interface. The options for this field are: **NOTE:** When the host software must change this field value, the host must also reset the Port (SATA_P 0 SCTL[DET] = 0x1) at the same time to ensure proper speed negotiation. 0x0 No speed negotiation restrictions 0x1 Limit speed negotiation to SATA 1.5 Gb/s communication rate 0x2 Limit speed negotiation to SATA 3.0 Gb/s communication rate All other values Reserved and should not be used.
DET	Device Detection Initialization Controls the Port's device detection and interface initialization. The options for this field are: **NOTE:** This field may only be modified when SATA_P 0 CMD[ST] is 0. Changing this field while the SATA_P 0 CMD[ST]=1 results in undefined behavior. When SATA_P 0 CMD[ST] is set to 1, this field should have a value of 0x0. 0x0 No device detection or initialization action requested 0x1 Perform interface initialization sequence to establish communication. This results in the interface being reset and communication re initialized. 0x4 Disable the Serial ATA interface and put the Port PHY in offline mode. All other values reserved.

53.7.28 Port0 Serial ATA Error Register (SATA_P0SERR)

This 32-bit register represents all the detected interface errors accumulated since the last time it was cleared. The set bits in the SError register indicate that the corresponding error condition became true one or more times since the last time the bit was cleared. The set bits in this register are explicitly cleared by a write operation to the register, Global reset, or Port reset (COMRESET). The value written to clear the set error bits should have ones encoded in the bit positions corresponding to the bits that are to be cleared. All bits in the following table have a reset value of 0.

Address: 220_0000h base + 130h offset = 220_0130h



SATA_P0SERR field descriptions

Field	Description
31–27 -	This field is reserved. Reserved
26 DIAG_X	Exchanged This bit is set to 1 when PHY COMINIT signal is detected. This bit is reflected in the SATA_P 0 IS[PCS] bit.
25 DIAG_F	Unknown FIS Type This bit indicates that one or more FISes were received by the Transport layer with good CRC, but had a type field that was not recognized/known and the length was less than or equal to 64bytes. **NOTE:** When the Unknown FIS length exceeds 64 bytes, the DIAG_F bit is not set and the DIAG_T bit is set instead.
24 DIAG_T	Transport State Transition Error This bit indicates that a Transport Layer protocol violation was detected since the last time this bit was cleared. See Transport Check (TCHK) for details.
23 DIAG_S	Link Sequence Error This bit indicates that one or more Link state machine error conditions was encountered. One of the conditions that cause this bit to be set is device doing SYNC escape during FIS transmission.
22 DIAG_H	Handshake Error This bit indicates that one or more R_ERRp was received in response to frame transmission. Such errors may be the result of a CRC error detected by the device, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21 DIAG_C	CRC Error
20 DIAG_D	Disparity Error This bit is always cleared to 0 since it is not used by the AHCI specification.
19 DIAG_B	10B to 8B Decode Error This bit indicates errors were detected by 10b8b decoder. This bit indicates that one or more CRC errors were detected by the Link layer during FIS reception. **NOTE:** This bit is set only when an error is detected on the received FIS data dword. This bit is not set when an error is detected on the primitive, regardless whether it is inside or outside the FIS.
18 DIAG_W	Comm Wake This bit is set when PHY COMWAKE signal is detected.
17 DIAG_I	PHY Internal Error This bit is set when the PHY detects some internal error as indicated by the assertion of the p 0 _phy_rx_err input. **NOTE:** The setting of this bit is controlled by the SATA_BISTCR[ERREN] bit: when ERREN==0 (default), only errors occurring inside the received FIS cause DIAG_I bit to be set; when ERREN==1, any error inside or outside the FIS causes the DIAG_I bit to be set.
16 DIAG_N	PHY Ready Change This bit indicates that the PHY Ready signal changed state. This bit is reflected in the SATA_P 0 IS[PRCS] bit.
15–12 -	This field is reserved. Reserved

Table continues on the next page...

SATA_P0SERR field descriptions (continued)

Field	Description
11 ERR_E	Internal Error This bit is set to 1 when one or more AHB bus ERROR responses are detected on the master interface.
10 ERR_P	Protocol Error This bit is set to 1 when any of the following conditions are detected. • Transport state transition error (DIAG_T) • Link sequence error (DIAG_S) • RxFIFO overflow • Link bad end error (WTRM instead of EOF is received).
9 ERR_C	Non-Recovered Persistent Communication Error This bit is set to 1 when PHY Ready signal is negated due to the loss of communication with the device or problems with interface, but not after transition from active to Partial or Slumber power management state.
8 ERR_T	Non-Recovered Transient Data Integrity Error This bit is set when any of the following SATA_P 0 SERR register bits is set during Data FIS transfer: ERR_P (Protocol) • DIAG_C (CRC) • DIAG_H (Handshake) • ERR_C ("PHY Ready" negation)
7–2 -	This field is reserved. Reserved
1 ERR_M	Recovered Communication Error This bit is set to 1 when PHY Ready condition is detected after interface initialization, but not after transition from Partial or Slumber power management state to active state.
0 ERR_I	This bit is set when any of the following SATA_P 0 SERR register bits is set during non- Data FIS transfer: • DIAG_C (CRC) • DIAG_H (Handshake) • ERR_C ("PHY Ready" negation)

53.7.29 Port0 Serial ATA Active Register (SATA_P0SACT)

Address: 220_0000h base + 134h offset = 220_0134h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DS																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_P0SACT field descriptions

Field	Description
DS	Device Status

SATA_P0SACT field descriptions (continued)

Field	Description
	This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. Software sets this field prior to issuing a native queued command for a particular command slot. Prior to writing SATA_P 0 CI[TAG] to 1, the software sets DS[TAG] to 1 to indicate that a command with that TAG is outstanding. This field is cleared to 0 when: • The software writes SATA_P 0 CMD[ST from a 1 to a 0 . • The device sends a Set Device Bits FIS to the Port. The Port clears bits in this field that are set in the SActive field of the Set Device Bits FIS. The Port clears only bits that correspond to native queued commands that have completed successfully. This field is not cleared by the following: • Port reset (COMRESET). • Software reset. **NOTE:** Software must write this field only when SATA_P 0 CMD[ST] bit is set to 1.

53.7.30 Port0 Command Issue Register (SATA_P0CI)

Address: 220_0000h base + 138h offset = 220_0138h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CI																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_P0CI field descriptions

Field	Description
CI	Command Issued This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by the software to indicate to the Port that a command has been built in system memory for a command slot and may be sent to the device. When the Port receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field can only be set to 1 by the software when SATA_P 0 CMD[ST] is set to 1. **NOTE:** This field is reset when SATA_P 0 CMD[ST] is written from a 1 to a 0 by the software.

53.7.31 Port0 Serial ATA Notification Register (SATA_P0SNTF)

This register is used to determine when asynchronous notification events have occurred for directly connected devices and devices connected to a Port Multiplier.

Address: 220_0000h base + 13Ch offset = 220_013Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved																PMN															
W																	w1c															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_P0SNTF field descriptions

Field	Description
31–16 -	This field is reserved. Reserved
PMN	PM Notify This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the SATA block Port with the Notification bit set: • PM Port 0h sets bit 0, • PM Port 1h sets bit 1, ... • PM Port Fh sets bit 15. Individual bits are cleared by the software writing 1s to the corresponding bit positions. This field is reset on Global reset, but it is not reset by Port reset (COMRESET) or software reset.

53.7.32 Port0 DMA Control Register (SATA_P0DMACR)

This register contains bits for controlling the Port DMA engine. The software can change the fields of this register only when SATA_P 0 CMD[ST]=0. Power-up (system reset), Global reset, or Port reset (COMRESET) reset this register to the default value.

Address: 220_0000h base + 170h offset = 220_0170h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved																-				-				RXTS				TXTS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

SATA_P0DMACR field descriptions

Field	Description
31–16 -	This field is reserved. Reserved
15–12 -	Reserved
11–8 -	Reserved
7–4 RXTS	Receive Transaction Size This field defines the Port DMA transaction size in DWORDs for receive (system bus write, device read) operation. This field is read-write when SATA_P 0 CMD[ST]=0 and read-only when SATA_P 0 CMD[ST]=1. The maximum value of this field is determined by the RxFIFO depth parameter. When the software attempts to write a value exceeding this value, the maximum value would be set instead. 0x0 1 DWORD 0x1 2 DWORD 0x2 4 DWORD 0x3 8 DWORD 0x4 16 DWORDs (maximum value when RXFIFO_DEPTH=64) 0x5 32 DWORD 0x6 64 DWORDs (maximum value when RXFIFO_DEPTH=128) 0x7 128 DWORDs (maximum value when RXFIFO_DEPTH=256) 0x8 256 DWORDs (maximum value when RXFIFO_DEPTH=512) 0x9 12 DWORDs (maximum value when RXFIFO_DEPTH=1024) 0xA 1024 DWORDs (maximum value when RXFIFO_DEPTH=2048) All other values are reserved and should not be used.
TXTS	Transmit Transaction Size This field defines the DMA transaction size in DWORDs for transmit (system bus read, device write) operation. The options for this field are: This field is read-write when SATA_P 0 CMD[ST]=0 and read-only when SATA_P 0 CMD[ST]=1. The maximum value of this field is determined by the TxFIFO depth parameter. When the software attempts to write a value exceeding this value, the maximum value would be set instead. 0x0 1 DWORD 0x1 2 DWORD 0x2 4 DWORD 0x3 8 DWORD 0x4 16 DWORDs (maximum value when TXFIFO_DEPTH=32) 0x5 32 DWORDs (maximum value when TXFIFO_DEPTH=64) 0x6 64 DWORDs (maximum value when TXFIFO_DEPTH=128) 0x7 128 DWORDs (maximum value when TXFIFO_DEPTH=256) 0x8 256 DWORDs (maximum value when TXFIFO_DEPTH=512) 0x9 512 DWORDs (maximum value when TXFIFO_DEPTH=1024) 0xA 1024 DWORDs (maximum value when TXFIFO_DEPTH=2048) All other values are reserved and should not be used.

53.7.33 Port0 PHY Control Register (SATA_P0PHYCR)

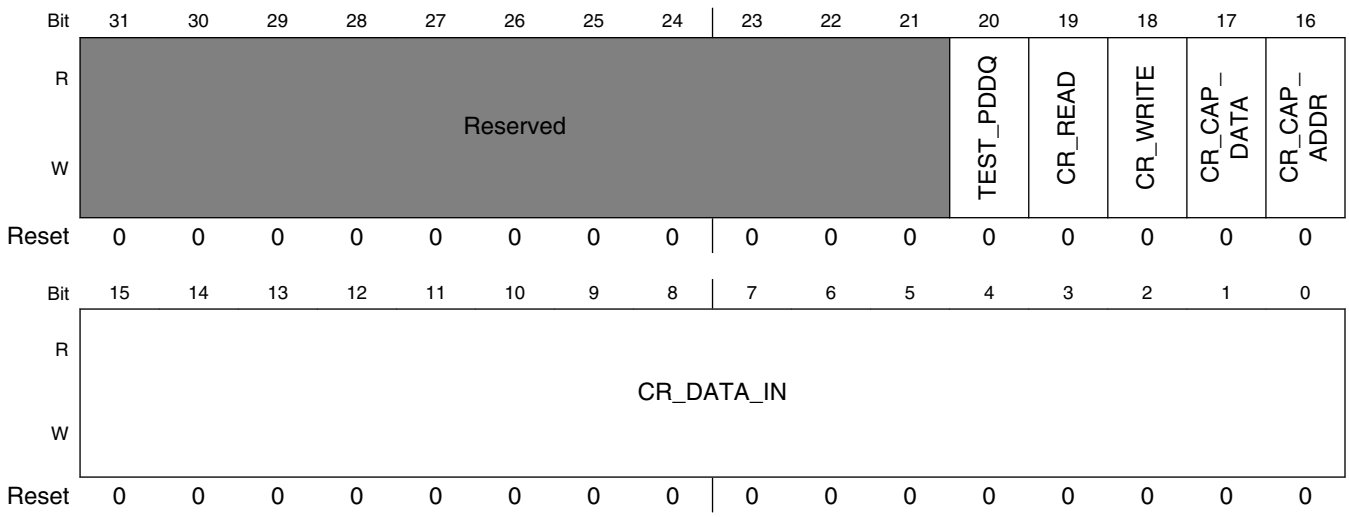
This register is used for Port PHY control.

Bits of this register are connected to the corresponding bits of the p 0 _phy_ctrl output Port.

NOTE

The SATA_P 0 PHYCR register supports only 32-bit write access

Address: 220_0000h base + 178h offset = 220_0178h



SATA_P0PHYCR field descriptions

Field	Description
31–21 -	This field is reserved. Reserved
20 TEST_PDDQ	Test IDDQ
19 CR_READ	CR Read. Reads from the referenced Address register.
18 CR_WRITE	CR Write. Writes the Write Data register to the referenced Address register.
17 CR_CAP_DATA	CR Capture Data. Captures phy_cr_data_in[15:0] into the Write Data register.
16 CR_CAP_ADDR	CR Capture Address. Captures phy_cr_data_in[15:0] into the Address register.
CR_DATA_IN	CR Address and Write Data Input Bus. Supplies and captures address and write data.

53.7.34 Port0 PHY Status Register (SATA_P0PHYSR)

This register is used to monitor PHY status.

The bits of this register reflect the state of the corresponding bits of the p 0 _phy_status input.

Signals connected to the p 0 _phy_status input can be asynchronous to any of the SATA block clocks, however they must not change faster than five hclk periods, otherwise the SATA_P 0 PHYSR register may never be updated with the intermediate changing values.

Address: 220_0000h base + 17Ch offset = 220_017Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0													CR_ ACK	0	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CR_DATA_OUT															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SATA_P0PHYSR field descriptions

Field	Description
31–19 Reserved	This read-only field is reserved and always has the value 0.
18 CR_ACK	CR Acknowledgement. Acknowledgement for the phy_cr_cap_addr, phy_cr_cap_data, phy_cr_write, and phy_cr_read control signals.
17–16 Reserved	This read-only field is reserved and always has the value 0.
CR_DATA_OUT	CR Data Output Bus. Always presents last read data.