

**Figure 37-56. Entering and Exiting LPSR mode**

## 37.5 IPU Memory Map/Register Definition

The address space for accesses through the AHB-lite slave port is 4 MB and it is split internally (with 2MB resolution) according to bit [21] of the address. Using the following notation

Address = (IPU\_ID[31:25], 1,1,1,MSB[21], LSB[20:0])

the address is used as follows :

1. MSB=0: Low-level access to an external device, with LSB[3:0] = (Lock, CS, RS[1:0])
  - LSB[5:4] = RS[1:0] (the address on the display interface)
  - LSB[6] = Choice of display's channel (0=channel 8, 1=channel 9)
  - LSB[7] = Lock (Lock=1 prevents the use of the display port until the next ARM platform access)
1. MSB=1: access to internal IPU registers, with address LSB

### NOTE

The addresses given in the table are relative to the IPU base address defined at SoC's level.

**IPU memory map**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
260_0000	Configuration Register (IPU1_CONF)	32	R/W	0000_0000h	<a href="#">37.5.1/2959</a>
260_0004	SISG Control 0 Register (IPU1_SISG_CTRL0)	32	R/W	0000_0000h	<a href="#">37.5.2/2962</a>
260_0008	SISG Control 1 Register (IPU1_SISG_CTRL1)	32	R/W	0000_0000h	<a href="#">37.5.3/2963</a>
260_000C	SISG Set<i> Register (IPU1_SISG_SET_i)	32	R/W	0000_0000h	<a href="#">37.5.4/2963</a>
260_0024	SISG Clear <i> Register (IPU1_SISG_CLR_i)	32	R/W	0000_0000h	<a href="#">37.5.5/2964</a>
260_003C	Interrupt Control Register 1 (IPU1_INT_CTRL_1)	32	R/W	0000_0000h	<a href="#">37.5.6/2964</a>
260_0040	Interrupt Control Register 2 (IPU1_INT_CTRL_2)	32	R/W	0000_0000h	<a href="#">37.5.7/2968</a>
260_0044	Interrupt Control Register 3 (IPU1_INT_CTRL_3)	32	R/W	0000_0000h	<a href="#">37.5.8/2971</a>
260_0048	Interrupt Control Register 4 (IPU1_INT_CTRL_4)	32	R/W	0000_0000h	<a href="#">37.5.9/2975</a>
260_004C	Interrupt Control Register 5 (IPU1_INT_CTRL_5)	32	R/W	0000_0000h	<a href="#">37.5.10/2978</a>
260_0050	Interrupt Control Register 6 (IPU1_INT_CTRL_6)	32	R/W	0000_0000h	<a href="#">37.5.11/2983</a>
260_0054	Interrupt Control Register 7 (IPU1_INT_CTRL_7)	32	R/W	0000_0000h	<a href="#">37.5.12/2986</a>
260_0058	Interrupt Control Register 8 (IPU1_INT_CTRL_8)	32	R/W	0000_0000h	<a href="#">37.5.13/2988</a>
260_005C	Interrupt Control Register 9 (IPU1_INT_CTRL_9)	32	R/W	0000_0000h	<a href="#">37.5.14/2990</a>
260_0060	Interrupt Control Register 10 (IPU1_INT_CTRL_10)	32	R/W	0000_0000h	<a href="#">37.5.15/2992</a>
260_0064	Interrupt Control Register 11 (IPU1_INT_CTRL_11)	32	R/W	0000_0000h	<a href="#">37.5.16/2994</a>
260_0068	Interrupt Control Register 12 (IPU1_INT_CTRL_12)	32	R/W	0000_0000h	<a href="#">37.5.17/2997</a>
260_006C	Interrupt Control Register 13 (IPU1_INT_CTRL_13)	32	R/W	0000_0000h	<a href="#">37.5.18/2999</a>
260_0070	Interrupt Control Register 14 (IPU1_INT_CTRL_14)	32	R/W	0000_0000h	<a href="#">37.5.19/3003</a>
260_0074	Interrupt Control Register 15 (IPU1_INT_CTRL_15)	32	R/W	0000_0000h	<a href="#">37.5.20/3006</a>
260_0078	SDMA Event Control Register 1 (IPU1_SDMA_EVENT_1)	32	R/W	0000_0000h	<a href="#">37.5.21/3010</a>
260_007C	SDMA Event Control Register 2 (IPU1_SDMA_EVENT_2)	32	R/W	0000_0000h	<a href="#">37.5.22/3014</a>
260_0080	SDMA Event Control Register 3 (IPU1_SDMA_EVENT_3)	32	R/W	0000_0000h	<a href="#">37.5.23/3017</a>
260_0084	SDMA Event Control Register 4 (IPU1_SDMA_EVENT_4)	32	R/W	0000_0000h	<a href="#">37.5.24/3022</a>
260_0088	SDMA Event Control Register 7 (IPU1_SDMA_EVENT_7)	32	R/W	0000_0000h	<a href="#">37.5.25/3025</a>
260_008C	SDMA Event Control Register 8 (IPU1_SDMA_EVENT_8)	32	R/W	0000_0000h	<a href="#">37.5.26/3027</a>

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**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
260_0090	SDMA Event Control Register 11 (IPU1_SDMA_EVENT_11)	32	R/W	0000_0000h	<a href="#">37.5.27/ 3028</a>
260_0094	SDMA Event Control Register 12 (IPU1_SDMA_EVENT_12)	32	R/W	0000_0000h	<a href="#">37.5.28/ 3031</a>
260_0098	SDMA Event Control Register 13 (IPU1_SDMA_EVENT_13)	32	R/W	0000_0000h	<a href="#">37.5.29/ 3033</a>
260_009C	SDMA Event Control Register 14 (IPU1_SDMA_EVENT_14)	32	R/W	0000_0000h	<a href="#">37.5.30/ 3037</a>
260_00A0	Shadow Registers Memory Priority 1 Register (IPU1_SRM_PRI1)	32	R/W	0000_0100h	<a href="#">37.5.31/ 3040</a>
260_00A4	Shadow Registers Memory Priority 2 Register (IPU1_SRM_PRI2)	32	R/W	0605_0803h	<a href="#">37.5.32/ 3041</a>
260_00A8	FSU Processing Flow 1 Register (IPU1_FS_PROC_FLOW1)	32	R/W	0000_0000h	<a href="#">37.5.33/ 3043</a>
260_00AC	FSU Processing Flow 2 Register (IPU1_FS_PROC_FLOW2)	32	R/W	0000_0000h	<a href="#">37.5.34/ 3047</a>
260_00B0	FSU Processing Flow 3 Register (IPU1_FS_PROC_FLOW3)	32	R/W	0000_0000h	<a href="#">37.5.35/ 3050</a>
260_00B4	FSU Displaying Flow 1 Register (IPU1_FS_DISP_FLOW1)	32	R/W	0000_0000h	<a href="#">37.5.36/ 3053</a>
260_00B8	FSU Displaying Flow 2 Register (IPU1_FS_DISP_FLOW2)	32	R/W	0000_0000h	<a href="#">37.5.37/ 3056</a>
260_00BC	SKIP Register (IPU1_SKIP)	32	R/W	0000_0000h	<a href="#">37.5.38/ 3058</a>
260_00C4	Display General Control Register (IPU1_DISP_GEN)	32	R/W	0040_0000h	<a href="#">37.5.39/ 3060</a>
260_00C8	Display Alternate Flow Control Register 1 (IPU1_DISP_ALT1)	32	R/W	0040_0000h	<a href="#">37.5.40/ 3063</a>
260_00CC	Display Alternate Flow Control Register 2 (IPU1_DISP_ALT2)	32	R/W	0000_0000h	<a href="#">37.5.41/ 3064</a>
260_00D0	Display Alternate Flow Control Register 3 (IPU1_DISP_ALT3)	32	R/W	0040_0000h	<a href="#">37.5.42/ 3065</a>
260_00D4	Display Alternate Flow Control Register 4 (IPU1_DISP_ALT4)	32	R/W	0000_0000h	<a href="#">37.5.43/ 3067</a>
260_00DC	Memory Reset Control Register (IPU1_MEM_RST)	32	R/W	0000_0000h	<a href="#">37.5.44/ 3068</a>
260_00E0	Power Modes Control Register (IPU1_PM)	32	R/W	0810_0810h	<a href="#">37.5.45/ 3070</a>
260_00E4	General Purpose Register (IPU1_GPR)	32	R/W	0000_0000h	<a href="#">37.5.46/ 3073</a>
260_0150	Channel Double Buffer Mode Select 0 Register (IPU1_CH_DB_MODE_SEL0)	32	R/W	0000_0000h	<a href="#">37.5.47/ 3075</a>
260_0154	Channel Double Buffer Mode Select 1 Register (IPU1_CH_DB_MODE_SEL1)	32	R/W	0000_0000h	<a href="#">37.5.48/ 3079</a>

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## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
260_0168	Alternate Channel Double Buffer Mode Select 0 Register (IPU1_ALT_CH_DB_MODE_SEL0)	32	R/W	0000_0000h	37.5.49/ 3082
260_016C	Alternate Channel Double Buffer Mode Select1 Register (IPU1_ALT_CH_DB_MODE_SEL1)	32	R/W	0000_0000h	37.5.50/ 3084
260_0178	Alternate Channel Triple Buffer Mode Select 0 Register (IPU1_ALT_CH_TRB_MODE_SEL0)	32	R/W	0000_0000h	37.5.51/ 3085
260_0200	Interrupt Status Register 1 (IPU1_INT_STAT_1)	32	w1c	0000_0000h	37.5.52/ 3088
260_0204	Interrupt Status Register2 (IPU1_INT_STAT_2)	32	w1c	0000_0000h	37.5.53/ 3093
260_0208	Interrupt Status Register 3 (IPU1_INT_STAT_3)	32	w1c	0000_0000h	37.5.54/ 3096
260_020C	Interrupt Status Register 4 (IPU1_INT_STAT_4)	32	w1c	0000_0000h	37.5.55/ 3100
260_0210	Interrupt Status Register 5 (IPU1_INT_STAT_5)	32	w1c	0000_0000h	37.5.56/ 3103
260_0214	Interrupt Status Register 6 (IPU1_INT_STAT_6)	32	w1c	0000_0000h	37.5.57/ 3108
260_0218	Interrupt Status Register7 1 (IPU1_INT_STAT_7)	32	w1c	0000_0000h	37.5.58/ 3111
260_021C	Interrupt Status Register 8 (IPU1_INT_STAT_8)	32	w1c	0000_0000h	37.5.59/ 3114
260_0220	Interrupt Status Register 9 (IPU1_INT_STAT_9)	32	w1c	0000_0000h	37.5.60/ 3117
260_0224	Interrupt Status Register 10 (IPU1_INT_STAT_10)	32	w1c	0000_0000h	37.5.61/ 3119
260_0228	Interrupt Status Register 11 (IPU1_INT_STAT_11)	32	w1c	0000_0000h	37.5.62/ 3122
260_022C	Interrupt Status Register 12 (IPU1_INT_STAT_12)	32	w1c	0000_0000h	37.5.63/ 3126
260_0230	Interrupt Status Register 13 (IPU1_INT_STAT_13)	32	w1c	0000_0000h	37.5.64/ 3128
260_0234	Interrupt Status Register 14 (IPU1_INT_STAT_14)	32	w1c	0000_0000h	37.5.65/ 3133
260_0238	Interrupt Status Register 15 (IPU1_INT_STAT_15)	32	w1c	0000_0000h	37.5.66/ 3136
260_023C	Current Buffer Register 0 (IPU1_CUR_BUF_0)	32	R	0000_0000h	37.5.67/ 3140
260_0240	Current Buffer Register 1 (IPU1_CUR_BUF_1)	32	R	0000_0000h	37.5.68/ 3145
260_0244	Alternate Current Buffer Register 0 (IPU1_ALT_CUR_0)	32	R	0000_0000h	37.5.69/ 3149
260_0248	Alternate Current Buffer Register 1 (IPU1_ALT_CUR_1)	32	R	0000_0000h	37.5.70/ 3151

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**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
260_024C	Shadow Registers Memory Status Register (IPU1_SR_M_STAT)	32	R	0000_0000h	<a href="#">37.5.71/ 3154</a>
260_0250	Processing Status Tasks Register (IPU1_PROC_TASKS_STAT)	32	R	0000_0000h	<a href="#">37.5.72/ 3156</a>
260_0254	Display Tasks Status Register (IPU1_DISP_TASKS_STAT)	32	R	0000_0000h	<a href="#">37.5.73/ 3158</a>
260_0258	Triple Current Buffer Register 0 (IPU1_TRIPLE_CUR_BUF_0)	32	R	0000_0000h	<a href="#">37.5.74/ 3160</a>
260_025C	Triple Current Buffer Register 1 (IPU1_TRIPLE_CUR_BUF_1)	32	R	0000_0000h	<a href="#">37.5.75/ 3162</a>
260_0268	IPU Channels Buffer 0 Ready 0 Register (IPU1_CH_BUF0_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.76/ 3163</a>
260_026C	IPU Channels Buffer 0 Ready 1 Register (IPU1_CH_BUF0_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.77/ 3167</a>
260_0270	IPU Channels Buffer 1 Ready 0 Register (IPU1_CH_BUF1_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.78/ 3169</a>
260_0274	IPU Channels Buffer 1 Ready 1 Register (IPU1_CH_BUF1_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.79/ 3172</a>
260_0278	IPU Alternate Channels Buffer 0 Ready 0 Register (IPU1_ALT_CH_BUF0_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.80/ 3175</a>
260_027C	IPU Alternate Channels Buffer 0 Ready 1 Register (IPU1_ALT_CH_BUF0_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.81/ 3176</a>
260_0280	IPU Alternate Channels Buffer 1 Ready 0 Register (IPU1_ALT_CH_BUF1_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.82/ 3177</a>
260_0284	IPU Alternate Channels Buffer 1 Ready 1 Register (IPU1_ALT_CH_BUF1_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.83/ 3178</a>
260_0288	IPU Channels Buffer 2 Ready 0 Register (IPU1_CH_BUF2_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.84/ 3179</a>
260_028C	IPU Channels Buffer 2 Ready 1 Register (IPU1_CH_BUF2_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.85/ 3181</a>
260_8000	IDMAC Configuration Register (IPU1_IDMAC_CONF)	32	R/W	0000_002Fh	<a href="#">37.5.86/ 3182</a>
260_8004	IDMAC Channel Enable 1 Register (IPU1_IDMAC_CH_EN_1)	32	R/W	0000_0000h	<a href="#">37.5.87/ 3184</a>
260_8008	IDMAC Channel Enable 2 Register (IPU1_IDMAC_CH_EN_2)	32	R/W	0000_0000h	<a href="#">37.5.88/ 3187</a>
260_800C	IDMAC Separate Alpha Indication Register (IPU1_IDMAC_SEP_ALPHA)	32	R/W	0000_0000h	<a href="#">37.5.89/ 3189</a>
260_8010	IDMAC Alternate Separate Alpha Indication Register (IPU1_IDMAC_ALT_SEP_ALPHA)	32	R/W	0000_0000h	<a href="#">37.5.90/ 3191</a>
260_8014	IDMAC Channel Priority 1 Register (IPU1_IDMAC_CH_PRI_1)	32	R/W	0000_0000h	<a href="#">37.5.91/ 3193</a>
260_8018	IDMAC Channel Priority 2 Register (IPU1_IDMAC_CH_PRI_2)	32	R/W	0000_0000h	<a href="#">37.5.92/ 3196</a>

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## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
260_801C	IDMAC Channel Watermark Enable 1 Register (IPU1_IDMAC_WM_EN_1)	32	R/W	0000_0000h	37.5.93/ 3198
260_8020	IDMAC Channel Watermark Enable 2 Register (IPU1_IDMAC_WM_EN_2)	32	R/W	0000_0000h	37.5.94/ 3200
260_8024	IDMAC Channel Lock Enable 1 Register (IPU1_IDMAC_LOCK_EN_1)	32	R/W	0000_0000h	37.5.95/ 3201
260_8028	IDMAC Channel Lock Enable 2 Register (IPU1_IDMAC_LOCK_EN_2)	32	R/W	0000_0000h	37.5.96/ 3203
260_802C	IDMAC Channel Alternate Address 0 Register (IPU1_IDMAC_SUB_ADDR_0)	32	R/W	0000_0000h	37.5.97/ 3204
260_8030	IDMAC Channel Alternate Address 1 Register (IPU1_IDMAC_SUB_ADDR_1)	32	R/W	0000_0000h	37.5.98/ 3205
260_8034	IDMAC Channel Alternate Address 2 Register (IPU1_IDMAC_SUB_ADDR_2)	32	R/W	0000_0000h	37.5.99/ 3206
260_8038	IDMAC Channel Alternate Address 3 Register (IPU1_IDMAC_SUB_ADDR_3)	32	R/W	0000_0000h	37.5.100/ 3207
260_803C	IDMAC Channel Alternate Address 4 Register (IPU1_IDMAC_SUB_ADDR_4)	32	R/W	0000_0000h	37.5.101/ 3209
260_8040	IDMAC Band Mode Enable 1 Register (IPU1_IDMAC_BNDM_EN_1)	32	R/W	0000_0000h	37.5.102/ 3210
260_8044	IDMAC Band Mode Enable 2 Register (IPU1_IDMAC_BNDM_EN_2)	32	R/W	0000_0000h	37.5.103/ 3213
260_8048	IDMAC Scroll Coordinations Register (IPU1_IDMAC_SC_CORD)	32	R/W	0000_0000h	37.5.104/ 3214
260_804C	IDMAC Scroll Coordinations Register 1 (IPU1_IDMAC_SC_CORD_1)	32	R/W	0000_0000h	37.5.105/ 3215
260_8100	IDMAC Channel Busy 1 Register (IPU1_IDMAC_CH_BUSY_1)	32	R	0000_0000h	37.5.106/ 3216
260_8104	IDMAC Channel Busy 2 Register (IPU1_IDMAC_CH_BUSY_2)	32	R	0000_0000h	37.5.107/ 3222
261_8000	DP Common Configuration Sync Flow Register (IPU1_DP_COM_CONF_SYNC)	32	R/W	0000_0000h	37.5.108/ 3226
261_8004	DP Graphic Window Control Sync Flow Register (IPU1_DP_Graph_Wind_CTRL_SYNC)	32	R/W	0000_0000h	37.5.109/ 3228
261_8008	DP Partial Plane Window Position Sync Flow Register (IPU1_DP_FG_POS_SYNC)	32	R/W	0000_0000h	37.5.110/ 3229
261_800C	DP Cursor Position and Size Sync Flow Register (IPU1_DP_CUR_POS_SYNC)	32	R/W	0000_0000h	37.5.111/ 3229
261_8010	DP Color Cursor Mapping Sync Flow Register (IPU1_DP_CUR_MAP_SYNC)	32	R/W	0000_0000h	37.5.112/ 3230
261_8014	DP Gamma Constants Sync Flow Register i (IPU1_DP_GAMMA_C_SYNC_i)	32	R/W	0000_0000h	37.5.113/ 3231
261_8034	DP Gamma Correction Slope Sync Flow Register i (IPU1_DP_GAMMA_S_SYNC_i)	32	R/W	0000_0000h	37.5.114/ 3231

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
261_8044	DP Color Space Conversion Control Sync Flow Registers (IPU1_DP_CSCA_SYNC_i)	32	R/W	0000_0000h	<a href="#">37.5.115/3232</a>
261_8054	DP Color Conversion Control Sync Flow Register 0 (IPU1_DP_SCS_SYNC_0)	32	R/W	0000_0000h	<a href="#">37.5.116/3233</a>
261_8058	DP Color Conversion Control Sync Flow Register 1 (IPU1_DP_SCS_SYNC_1)	32	R/W	0000_0000h	<a href="#">37.5.117/3233</a>
261_805C	DP Cursor Position and Size Alternate Register (IPU1_DP_CUR_POS_ALT)	32	R/W	0000_0000h	<a href="#">37.5.118/3234</a>
261_8060	DP Common Configuration Async 0 Flow Register (IPU1_DP_COM_CONF_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.119/3235</a>
261_8064	DP Graphic Window Control Async 0 Flow Register (IPU1_DP_GRAPH_WIND_CTRL_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.120/3237</a>
261_8068	DP Partial Plane Window Position Async 0 Flow Register (IPU1_DP_FG_POS_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.121/3238</a>
261_806C	DP Cursor Position and Size Async 0 Flow Register (IPU1_DP_CUR_POS_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.122/3239</a>
261_8070	DP Color Cursor Mapping Async 0 Flow Register (IPU1_DP_CUR_MAP_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.123/3239</a>
261_8074	DP Gamma Constant Async 0 Flow Register i (IPU1_DP_GAMMA_C_ASYNC0_i)	32	R/W	0000_0000h	<a href="#">37.5.124/3240</a>
261_8094	DP Gamma Correction Slope Async 0 Flow Register i (IPU1_DP_GAMMA_S_ASYNC0_i)	32	R/W	0000_0000h	<a href="#">37.5.125/3241</a>
261_80A4	DP Color Space Conversion Control Async 0 Flow Register i (IPU1_DP_CSCA_ASYNC0_i)	32	R/W	0000_0000h	<a href="#">37.5.126/3241</a>
261_80B4	DP Color Conversion Control Async 0 Flow Register 0 (IPU1_DP_CSC_ASYNC0_0)	32	R/W	0000_0000h	<a href="#">37.5.127/3242</a>
261_80B8	DP Color Conversion Control Async 1 Flow Register (IPU1_DP_CSC_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.128/3243</a>
261_80BC	DP Common Configuration Async 1 Flow Register (IPU1_DP_COM_CONF_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.129/3244</a>
261_80BC	DP Debug Control Register (IPU1_DP_DEBUG_CNT)	32	R/W	0000_0000h	<a href="#">37.5.130/3246</a>
261_80C0	DP Graphic Window Control Async 1 Flow Register (IPU1_DP_GRAPH_WIND_CTRL_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.131/3247</a>
261_80C0	DP Debug Status Register (IPU1_DP_DEBUG_STAT)	32	R	0000_0000h	<a href="#">37.5.132/3248</a>
261_80C4	DP Partial Plane Window Position Async 1 Flow Register (IPU1_DP_FG_POS_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.133/3250</a>
261_80C8	DP Cursor Postion and Size Async 1 Flow Register (IPU1_DP_CUR_POS_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.134/3250</a>
261_80CC	DP Color Cursor Mapping Async 1 Flow Register (IPU1_DP_CUR_MAP_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.135/3251</a>
261_80D0	DP Gamma Constants Async 1 Flow Register i (IPU1_DP_GAMMA_C_ASYNC1_i)	32	R/W	0000_0000h	<a href="#">37.5.136/3252</a>

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## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
261_80F0	DP Gamma Correction Slope Async 1 Flow Register i (IPU1_DP_GAMMA_S_ASYN1_i)	32	R/W	0000_0000h	37.5.137/ 3253
261_8100	DP Color Space Converstion Control Async 1 Flow Register i (IPU1_DP_CSCA_ASYNC1_i)	32	R/W	0000_0000h	37.5.138/ 3253
261_8110	DP Color Conversion Control Async 1 Flow Register 0 (IPU1_DP_CSC_ASYNC1_0)	32	R/W	0000_0000h	37.5.139/ 3254
261_8114	DP Color Conversion Control Async 1 Flow Register 1 (IPU1_DP_CSC_ASYNC1_1)	32	R/W	0000_0000h	37.5.140/ 3255
262_0000	IC Configuration Register (IPU1_IC_CONF)	32	R/W	0000_0000h	37.5.141/ 3256
262_0004	IC Preprocessing Encoder Resizing Coefficients Register (IPU1_IC_PRP_ENC_RSC)	32	R/W	2000_2000h	37.5.142/ 3258
262_0008	IC Preprocessing View-Finder Resizing Coefficients Register (IPU1_IC_PRP_VF_RSC)	32	R/W	2000_2000h	37.5.143/ 3259
262_000C	IC Postprocessing Encoder Resizing Coefficients Register (IPU1_IC_PP_RSC)	32	R/W	2000_2000h	37.5.144/ 3260
262_0010	IC Combining Parameters Register 1 (IPU1_IC_CMBP_1)	32	R/W	0000_0000h	37.5.145/ 3261
262_0014	IC Combining Parameters Register 2 (IPU1_IC_CMBP_2)	32	R/W	0000_0000h	37.5.146/ 3261
262_0018	IC IDMAC Parameters 1 Register (IPU1_IC_IDMAC_1)	32	R/W	0000_0000h	37.5.147/ 3262
262_001C	IC IDMAC Parameters 2 Register (IPU1_IC_IDMAC_2)	32	R/W	0000_0000h	37.5.148/ 3265
262_0020	IC IDMAC Parameters 3Register (IPU1_IC_IDMAC_3)	32	R/W	0000_0000h	37.5.149/ 3266
262_0024	IC IDMAC Parameters 4 Register (IPU1_IC_IDMAC_4)	32	R/W	0000_0000h	37.5.150/ 3266
263_0000	CSI0 Sensor Configuration Register (IPU1_CSI0_SENS_CONF)	32	R/W	0000_0000h	37.5.151/ 3267
263_0004	CSI0 Sense Frame Size Register (IPU1_CSI0_SENS_FRM_SIZE)	32	R/W	0000_0000h	37.5.152/ 3270
263_0008	CSI0 Actual Frame Size Register (IPU1_CSI0_ACT_FRM_SIZE)	32	R/W	0000_0000h	37.5.153/ 3270
263_000C	CSI0 Output Control Register (IPU1_CSI0_OUT_FRM_CTRL)	32	R/W	0000_0000h	37.5.154/ 3271
263_0010	CSIO Test Control Register (IPU1_CSI0_TST_CTRL)	32	R/W	0000_0000h	37.5.155/ 3272
263_0014	CSIO CCIR Code Register 1 (IPU1_CSI0_CCIR_CODE_1)	32	R/W	0000_0000h	37.5.156/ 3273
263_0018	CSIO CCIR Code Register 2 (IPU1_CSI0_CCIR_CODE_2)	32	R/W	0000_0000h	37.5.157/ 3274
263_001C	CSIO CCIR Code Register 3 (IPU1_CSI0_CCIR_CODE_3)	32	R/W	0000_0000h	37.5.158/ 3275

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
263_0020	CSI0 Data Identifier Register (IPU1_CSIO_DI)	32	R/W	FFFF_FFFFh	<a href="#">37.5.159/3275</a>
263_0024	CSI0 SKIP Register (IPU1_CSIO_SKIP)	32	R/W	0000_0000h	<a href="#">37.5.160/3276</a>
263_0028	CSI0 Compander Control Register (IPU1_CSIO_CPD_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.161/3277</a>
263_002C	CSI0 Red Component Compander Constants Register <i> (IPU1_CSIO_CPD_RC_i)	32	R/W	0000_0000h	<a href="#">37.5.162/3278</a>
263_004C	CSI0 Red Component Compander SLOPE Register <i> (IPU1_CSIO_CPD_RS_i)	32	R/W	0000_0000h	<a href="#">37.5.163/3279</a>
263_005C	CSI0 GR Component Compander Constants Register <i> (IPU1_CSIO_CPD_GRC_i)	32	R/W	0000_0000h	<a href="#">37.5.164/3279</a>
263_007C	CSI0 GR Component Compander SLOPE Register <i> (IPU1_CSIO_CPD_GRS_i)	32	R/W	0000_0000h	<a href="#">37.5.165/3280</a>
263_008C	CSI0 GB Component Compander Constants Register <i> (IPU1_CSIO_CPD_GBC_i)	32	R/W	0000_0000h	<a href="#">37.5.166/3281</a>
263_00AC	CSI0 GB Component Compander SLOPE Register <i> (IPU1_CSIO_CPD_GBS_i)	32	R/W	0000_0000h	<a href="#">37.5.167/3281</a>
263_00BC	CSI0 Blue Component Compander Constants Register <i> (IPU1_CSIO_CPD_BC_i)	32	R/W	0000_0000h	<a href="#">37.5.168/3282</a>
263_00DC	CSI0 Blue Component Compander SLOPE Register <i> (IPU1_CSIO_CPD_BS_i)	32	R/W	0000_0000h	<a href="#">37.5.169/3283</a>
263_00EC	CSI0 Compander Offset Register 1 (IPU1_CSIO_CPD_OFFSET1)	32	R/W	0000_0000h	<a href="#">37.5.170/3283</a>
263_00F0	CSI0 Compander Offset Register 2 (IPU1_CSIO_CPD_OFFSET2)	32	R/W	0000_0000h	<a href="#">37.5.171/3284</a>
263_8000	CSI1 Sensor Configuration Register (IPU1_CS1_SENS_CONF)	32	R/W	0000_0000h	<a href="#">37.5.172/3285</a>
263_8004	CSI1 Sense Frame Size Register (IPU1_CS1_SENS_FRM_SIZE)	32	R/W	0000_0000h	<a href="#">37.5.173/3287</a>
263_8008	CSI1 Actual Frame Size Register (IPU1_CS1_ACT_FRM_SIZE)	32	R/W	0000_0000h	<a href="#">37.5.174/3288</a>
263_800C	CSI1 Output Control Register (IPU1_CS1_OUT_FRM_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.175/3289</a>
263_8010	CSI1 Test Control Register (IPU1_CS1_TST_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.176/3290</a>
263_8014	CSI1 CCIR Code Register 1 (IPU1_CS1_CCIR_CODE_1)	32	R/W	0000_0000h	<a href="#">37.5.177/3291</a>
263_8018	CSI1 CCIR Code Register 2 (IPU1_CS1_CCIR_CODE_2)	32	R/W	0000_0000h	<a href="#">37.5.178/3292</a>
263_801C	CSI1 CCIR Code Register 3 (IPU1_CS1_CCIR_CODE_3)	32	R/W	0000_0000h	<a href="#">37.5.179/3293</a>
263_8020	CSI1 Data Identifier Register (IPU1_CS1_DI)	32	R/W	FFFF_FFFFh	<a href="#">37.5.180/3293</a>

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## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
263_8024	CSI1 SKIP Register (IPU1_CSI1_SKIP)	32	R/W	0000_0000h	<a href="#">37.5.181/3294</a>
263_8028	CSI1 Compander Control Register (IPU1_CSI1_CPD_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.182/3295</a>
263_802C	CSI1 Red Component Compander Constants Register <i> (IPU1_CSI1_CPD_RC_i)	32	R/W	0000_0000h	<a href="#">37.5.183/3296</a>
263_804C	CSI1 Red Component Compander SLOPE Register <i> (IPU1_CSI1_CPD_RS_i)	32	R/W	0000_0000h	<a href="#">37.5.184/3296</a>
263_805C	CSI1 GR Component Compander Constants Register <i> (IPU1_CSI1_CPD_GRC_i)	32	R/W	0000_0000h	<a href="#">37.5.185/3297</a>
263_807C	CSI1 GR Component Compander SLOPE Register <i> (IPU1_CSI1_CPD_GRS_i)	32	R/W	0000_0000h	<a href="#">37.5.186/3298</a>
263_808C	CSI1 GB Component Compander Constants Register <i> (IPU1_CSI1_CPD_GBC_i)	32	R/W	0000_0000h	<a href="#">37.5.187/3298</a>
263_80AC	CSI1 GB Component Compander SLOPE Register <i> (IPU1_CSI1_CPD_GBS_i)	32	R/W	0000_0000h	<a href="#">37.5.188/3299</a>
263_80BC	CSI1 Blue Component Compander Constants Register <i> (IPU1_CSI1_CPD_BC_i)	32	R/W	0000_0000h	<a href="#">37.5.189/3300</a>
263_80DC	CSI1 Blue Component Compander SLOPE Register <i> (IPU1_CSI1_CPD_BS_i)	32	R/W	0000_0000h	<a href="#">37.5.190/3300</a>
263_80EC	CSI1 Compander Offset Register 1 (IPU1_CSI1_CPD_OFFSET1)	32	R/W	0000_0000h	<a href="#">37.5.191/3301</a>
263_80F0	CSI1 Compander Offset Register 2 (IPU1_CSI1_CPD_OFFSET2)	32	R/W	0000_0000h	<a href="#">37.5.192/3302</a>
264_0000	DI0 General Register (IPU1_DI0_GENERAL)	32	R/W	0020_0000h	<a href="#">37.5.193/3303</a>
264_0004	DI0 Base Sync Clock Gen 0 Register (IPU1_DI0_BS_CLKGEN0)	32	R/W	0000_0000h	<a href="#">37.5.194/3305</a>
264_0008	DI0 Base Sync Clock Gen 1 Register (IPU1_DI0_BS_CLKGEN1)	32	R/W	0000_0000h	<a href="#">37.5.195/3306</a>
264_000C	DI0 Sync Wave Gen 1 Register 0 (IPU1_DI0_SW_GEN0_1)	32	R/W	0000_0000h	<a href="#">37.5.196/3306</a>
264_0010	DI0 Sync Wave Gen 2 Register 0 (IPU1_DI0_SW_GEN0_2)	32	R/W	0000_0000h	<a href="#">37.5.197/3308</a>
264_0014	DI0 Sync Wave Gen 3 Register 0 (IPU1_DI0_SW_GEN0_3)	32	R/W	0000_0000h	<a href="#">37.5.198/3309</a>
264_0018	DI0 Sync Wave Gen 4 Register 0 (IPU1_DI0_SW_GEN0_4)	32	R/W	0000_0000h	<a href="#">37.5.199/3310</a>
264_001C	DI0 Sync Wave Gen 5 Register 0 (IPU1_DI0_SW_GEN0_5)	32	R/W	0000_0000h	<a href="#">37.5.200/3311</a>
264_0020	DI0 Sync Wave Gen 6 Register 0 (IPU1_DI0_SW_GEN0_6)	32	R/W	0000_0000h	<a href="#">37.5.201/3313</a>
264_0024	DI0 Sync Wave Gen 7 Register 0 (IPU1_DI0_SW_GEN0_7)	32	R/W	0000_0000h	<a href="#">37.5.202/3314</a>

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**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
264_0028	DIO Sync Wave Gen 8 Register 0 (IPU1_DIO_SW_GEN0_8)	32	R/W	0000_0000h	<a href="#">37.5.203/3315</a>
264_002C	DIO Sync Wave Gen 9 Register 0 (IPU1_DIO_SW_GEN0_9)	32	R/W	0000_0000h	<a href="#">37.5.204/3316</a>
264_0030	DIO Sync Wave Gen 1 Register 1 (IPU1_DIO_SW_GEN1_1)	32	R/W	0000_0000h	<a href="#">37.5.205/3318</a>
264_0034	DIO Sync Wave Gen 2 Register 1 (IPU1_DIO_SW_GEN1_2)	32	R/W	0000_0000h	<a href="#">37.5.206/3320</a>
264_0038	DIO Sync Wave Gen 3 Register 1 (IPU1_DIO_SW_GEN1_3)	32	R/W	0000_0000h	<a href="#">37.5.207/3322</a>
264_003C	DIO Sync Wave Gen 4 Register 1 (IPU1_DIO_SW_GEN1_4)	32	R/W	0000_0000h	<a href="#">37.5.208/3324</a>
264_0040	DIO Sync Wave Gen 5 Register 1 (IPU1_DIO_SW_GEN1_5)	32	R/W	0000_0000h	<a href="#">37.5.209/3326</a>
264_0044	DIO Sync Wave Gen 6 Register 1 (IPU1_DIO_SW_GEN1_6)	32	R/W	0000_0000h	<a href="#">37.5.210/3328</a>
264_0048	DIO Sync Wave Gen 7 Register 1 (IPU1_DIO_SW_GEN1_7)	32	R/W	0000_0000h	<a href="#">37.5.211/3330</a>
264_004C	DIO Sync Wave Gen 8 Register 1 (IPU1_DIO_SW_GEN1_8)	32	R/W	0000_0000h	<a href="#">37.5.212/3332</a>
264_0050	DIO Sync Wave Gen 9 Register 1 (IPU1_DIO_SW_GEN1_9)	32	R/W	0000_0000h	<a href="#">37.5.213/3334</a>
264_0054	DIO Sync Assistance Gen Register (IPU1_DIO_SYNC_AS_GEN)	32	R/W	0000_0000h	<a href="#">37.5.214/3335</a>
264_0058	DIO Data Wave Gen <i>i</i> Register (IPU1_DIO_DW_GEN_i)	32	R/W	0000_0000h	<a href="#">37.5.215/3336</a>
264_0088	DIO Data Wave Set 0 <i>i</i> Register (IPU1_DIO_DW_SET0_i)	32	R/W	0000_0000h	<a href="#">37.5.216/3339</a>
264_00B8	DIO Data Wave Set 1 <i>i</i> Register (IPU1_DIO_DW_SET1_i)	32	R/W	0000_0000h	<a href="#">37.5.217/3339</a>
264_00E8	DIO Data Wave Set 2 <i>i</i> Register (IPU1_DIO_DW_SET2_i)	32	R/W	0000_0000h	<a href="#">37.5.218/3340</a>
264_0118	DIO Data Wave Set 3 <i>i</i> Register (IPU1_DIO_DW_SET3_i)	32	R/W	0000_0000h	<a href="#">37.5.219/3341</a>
264_0148	DIO Step Repeat <i>i</i> Registers (IPU1_DIO_STP_REP_i)	32	R/W	0000_0000h	<a href="#">37.5.220/3341</a>
264_0158	DIO Step Repeat 9 Registers (IPU1_DIO_STP_REP_9)	32	R/W	0000_0000h	<a href="#">37.5.221/3342</a>
264_015C	DIO Serial Display Control Register (IPU1_DIO_SER_CONF)	32	R/W	0000_0000h	<a href="#">37.5.222/3342</a>
264_0160	DIO Special Signals Control Register (IPU1_DIO_SSC)	32	R/W	0000_0000h	<a href="#">37.5.223/3345</a>
264_0164	DIO Polarity Register (IPU1_DIO_POL)	32	R/W	0000_0000h	<a href="#">37.5.224/3347</a>

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## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
264_0168	DIO Active Window 0 Register (IPU1_DIO_AW0)	32	R/W	0000_0000h	<a href="#">37.5.225/3348</a>
264_016C	DIO Active Window 1 Register (IPU1_DIO_AW1)	32	R/W	0000_0000h	<a href="#">37.5.226/3349</a>
264_0170	DIO Screen Configuration Register (IPU1_DIO_SCR_CONF)	32	R/W	0000_0000h	<a href="#">37.5.227/3350</a>
264_0174	DIO Status Register (IPU1_DIO_STAT)	32	R	0000_0005h	<a href="#">37.5.228/3351</a>
264_8000	DI1General Register (IPU1_DI1_GENERAL)	32	R/W	0020_0000h	<a href="#">37.5.229/3353</a>
264_8004	DI1 Base Sync Clock Gen 0 Register (IPU1_DI1_BS_CLKGEN0)	32	R/W	0000_0000h	<a href="#">37.5.230/3355</a>
264_8008	DI1 Base Sync Clock Gen 1 Register (IPU1_DI1_BS_CLKGEN1)	32	R/W	0000_0000h	<a href="#">37.5.231/3356</a>
264_800C	DI1 Sync Wave Gen 1 Register 0 (IPU1_DI1_SW_GEN0_1)	32	R/W	0000_0000h	<a href="#">37.5.232/3356</a>
264_8010	DI1 Sync Wave Gen 2 Register 0 (IPU1_DI1_SW_GEN0_2)	32	R/W	0000_0000h	<a href="#">37.5.233/3358</a>
264_8014	DI1 Sync Wave Gen 3 Register 0 (IPU1_DI1_SW_GEN0_3)	32	R/W	0000_0000h	<a href="#">37.5.234/3359</a>
264_8018	DI1 Sync Wave Gen 4 Register 0 (IPU1_DI1_SW_GEN0_4)	32	R/W	0000_0000h	<a href="#">37.5.235/3360</a>
264_801C	DI1 Sync Wave Gen 5 Register 0 (IPU1_DI1_SW_GEN0_5)	32	R/W	0000_0000h	<a href="#">37.5.236/3361</a>
264_8020	DI1 Sync Wave Gen 6 Register 0 (IPU1_DI1_SW_GEN0_6)	32	R/W	0000_0000h	<a href="#">37.5.237/3363</a>
264_8024	DI1 Sync Wave Gen 7 Register 0 (IPU1_DI1_SW_GEN0_7)	32	R/W	0000_0000h	<a href="#">37.5.238/3364</a>
264_8028	DI1 Sync Wave Gen 8 Register 0 (IPU1_DI1_SW_GEN0_8)	32	R/W	0000_0000h	<a href="#">37.5.239/3365</a>
264_802C	DI1 Sync Wave Gen 9 Register 0 (IPU1_DI1_SW_GEN0_9)	32	R/W	0000_0000h	<a href="#">37.5.240/3366</a>
264_8030	DI1 Sync Wave Gen 1 Register 1 (IPU1_DI1_SW_GEN1_1)	32	R/W	0000_0000h	<a href="#">37.5.241/3368</a>
264_8034	DI1 Sync Wave Gen 2 Register 1 (IPU1_DI1_SW_GEN1_2)	32	R/W	0000_0000h	<a href="#">37.5.242/3370</a>
264_8038	DI1 Sync Wave Gen 3 Register 1 (IPU1_DI1_SW_GEN1_3)	32	R/W	0000_0000h	<a href="#">37.5.243/3372</a>
264_803C	DI1 Sync Wave Gen 4 Register 1 (IPU1_DI1_SW_GEN1_4)	32	R/W	0000_0000h	<a href="#">37.5.244/3374</a>
264_8040	DI1 Sync Wave Gen 5 Register 1 (IPU1_DI1_SW_GEN1_5)	32	R/W	0000_0000h	<a href="#">37.5.245/3376</a>
264_8044	DI1 Sync Wave Gen 6 Register 1 (IPU1_DI1_SW_GEN1_6)	32	R/W	0000_0000h	<a href="#">37.5.246/3378</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
264_8048	DI1Sync Wave Gen 7 Register 1 (IPU1_DI1_SW_GEN1_7)	32	R/W	0000_0000h	<a href="#">37.5.247/3380</a>
264_804C	DI1 Sync Wave Gen 8 Register 1 (IPU1_DI1_SW_GEN1_8)	32	R/W	0000_0000h	<a href="#">37.5.248/3382</a>
264_8050	DI1 Sync Wave Gen 9 Register 1 (IPU1_DI1_SW_GEN1_9)	32	R/W	0000_0000h	<a href="#">37.5.249/3384</a>
264_8054	DI1 Sync Assistance Gen Register (IPU1_DI1_SYNC_AS_GEN)	32	R/W	0000_0000h	<a href="#">37.5.250/3385</a>
264_8058	DI1 Data Wave Gen <i>i</i> Register (IPU1_DI1_DW_GEN_i)	32	R/W	0000_0000h	<a href="#">37.5.251/3386</a>
264_8088	DI1 Data Wave Set 0 <i>i</i> Register (IPU1_DI1_DW_SET0_i)	32	R/W	0000_0000h	<a href="#">37.5.252/3389</a>
264_80B8	DI1 Data Wave Set 1 <i>i</i> Register (IPU1_DI1_DW_SET1_i)	32	R/W	0000_0000h	<a href="#">37.5.253/3389</a>
264_80E8	DI1 Data Wave Set 2 <i>i</i> Register (IPU1_DI1_DW_SET2_i)	32	R/W	0000_0000h	<a href="#">37.5.254/3390</a>
264_8118	DI1 Data Wave Set 3 <i>i</i> Register (IPU1_DI1_DW_SET3_i)	32	R/W	0000_0000h	<a href="#">37.5.255/3391</a>
264_8148	DI1 Step Repeat <i>i</i> Registers (IPU1_DI1_STP REP_i)	32	R/W	0000_0000h	<a href="#">37.5.256/3391</a>
264_8158	DI1Step Repeat 9 Registers (IPU1_DI1_STP REP_9)	32	R/W	0000_0000h	<a href="#">37.5.257/3392</a>
264_815C	DI1 Serial Display Control Register (IPU1_DI1_SER_CONF)	32	R/W	0000_0000h	<a href="#">37.5.258/3392</a>
264_8160	DI1 Special Signals Control Register (IPU1_DI1_SSC)	32	R/W	0000_0000h	<a href="#">37.5.259/3395</a>
264_8164	DI1 Polarity Register (IPU1_DI1_POL)	32	R/W	0000_0000h	<a href="#">37.5.260/3397</a>
264_8168	DI1Active Window 0 Register (IPU1_DI1_AW0)	32	R/W	0000_0000h	<a href="#">37.5.261/3398</a>
264_816C	DI1 Active Window 1 Register (IPU1_DI1_AW1)	32	R/W	0000_0000h	<a href="#">37.5.262/3399</a>
264_8170	DI1 Screen Configuration Register (IPU1_DI1_SCR_CONF)	32	R/W	0000_0000h	<a href="#">37.5.263/3400</a>
264_8174	DI1 Status Register (IPU1_DI1_STAT)	32	R	0000_0005h	<a href="#">37.5.264/3401</a>
265_0000	SMFC Mapping Register (IPU1_SMFC_MAP)	32	R/W	0000_0000h	<a href="#">37.5.265/3402</a>
265_0004	SMFC Watermark Control Register (IPU1_SMFC_WMC)	32	R/W	0000_09A6h	<a href="#">37.5.266/3403</a>
265_0008	SMFC Burst Size Register (IPU1_SMFC_BS)	32	R/W	0000_0000h	<a href="#">37.5.267/3405</a>
265_8000	DC Read Channel Configuration Register (IPU1_DC_READ_CH_CONF)	32	R/W	FFFF_0000h	<a href="#">37.5.268/3406</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
265_8004	DC Read Channel Start Address Register (IPU1_DC_READ_SH_ADDR)	32	R/W	0000_0000h	<a href="#">37.5.269/3407</a>
265_8008	DC Routine Link Register 0 Channel 0 (IPU1_DC_RL0_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.270/3408</a>
265_800C	DC Routine Link Register 1 Channel 0 (IPU1_DC_RL1_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.271/3409</a>
265_8010	DC Routine Link Register2 Channel 0 (IPU1_DC_RL2_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.272/3410</a>
265_8014	DC Routine Link Registe3 Channel 0 (IPU1_DC_RL3_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.273/3411</a>
265_8018	DC Routine Link Register 4 Channel 0 (IPU1_DC_RL4_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.274/3412</a>
265_801C	DC Write Channel 1 Configuration Register (IPU1_DC_WR_CH_CONF_1)	32	R/W	0000_0000h	<a href="#">37.5.275/3413</a>
265_8020	DC Write Channel 1 Address Configuration Register (IPU1_DC_WR_CH_ADDR_1)	32	R/W	0000_0000h	<a href="#">37.5.276/3414</a>
265_8024	DC Routine Link Register 0 Channel 1 (IPU1_DC_RL0_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.277/3415</a>
265_8028	DC Routine Link Register 1 Channel 1 (IPU1_DC_RL1_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.278/3416</a>
265_8030	DC Routine Link Register 2 Channel 1 (IPU1_DC_RL2_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.279/3417</a>
265_8032	DC Routine Link Register 3 Channel 1 (IPU1_DC_RL3_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.280/3418</a>
265_8034	DC Routine Link Register 4 Channel 1 (IPU1_DC_RL4_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.281/3419</a>
265_8038	DC Write Channel 2 Configuration Register (IPU1_DC_WR_CH_CONF_2)	32	R/W	0000_0000h	<a href="#">37.5.282/3420</a>
265_803C	DC Write Channel 2 Address Configuration Register (IPU1_DC_WR_CH_ADDR_2)	32	R/W	0000_0000h	<a href="#">37.5.283/3421</a>
265_8040	DC Routine Link Register 0 Channel 2 (IPU1_DC_RL0_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.284/3422</a>
265_8044	DC Routine Link Register 1 Channel 2 (IPU1_DC_RL1_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.285/3423</a>
265_8048	DC Routine Link Register 2 Channel 2 (IPU1_DC_RL2_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.286/3424</a>
265_804C	DC Routine Link Register 3 Channel 2 (IPU1_DC_RL3_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.287/3425</a>
265_8050	DC Routine Link Register 4 Channel 2 (IPU1_DC_RL4_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.288/3426</a>
265_8054	DC Command Channel 3 Configuration Register (IPU1_DC_CMD_CH_CONF_3)	32	R/W	0000_0000h	<a href="#">37.5.289/3426</a>
265_8058	DC Command Channel 4 Configuration Register (IPU1_DC_CMD_CH_CONF_4)	32	R/W	0000_0000h	<a href="#">37.5.290/3427</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
265_805C	DC Write Channel 5 Configuration Register (IPU1_DC_WR_CH_CONF_5)	32	R/W	0000_0000h	<a href="#">37.5.291/3428</a>
265_8060	DC Write Channel 5 Address Configuration Register (IPU1_DC_WR_CH_ADDR_5)	32	R/W	0000_0000h	<a href="#">37.5.292/3430</a>
265_8064	DC Routine Link Register 0 Channel 5 (IPU1_DC_RL0_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.293/3430</a>
265_8068	DC Routine Link Register 1 Channel 5 (IPU1_DC_RL1_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.294/3431</a>
265_806C	DC Routine Link Register 2 Channel 5 (IPU1_DC_RL2_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.295/3432</a>
265_8070	DC Routine Link Register 3 Channel 5 (IPU1_DC_RL3_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.296/3433</a>
265_8074	DC Routine Link Register 4 Channel 5 (IPU1_DC_RL4_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.297/3434</a>
265_8078	DC Write Channel 6 Configuration Register (IPU1_DC_WR_CH_CONF_6)	32	R/W	0000_0000h	<a href="#">37.5.298/3435</a>
265_807C	DC Write Channel 6 Address Configuration Register (IPU1_DC_WR_CH_ADDR_6)	32	R/W	0000_0000h	<a href="#">37.5.299/3436</a>
265_8080	DC Routine Link Register 0 Channel 6 (IPU1_DC_RL0_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.300/3437</a>
265_8084	DC Routine Link Register 1 Channel 6 (IPU1_DC_RL1_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.301/3438</a>
265_8088	DC Routine Link Register 2 Channel 6 (IPU1_DC_RL2_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.302/3439</a>
265_808C	DC Routine Link Register 3 Channel 6 (IPU1_DC_RL3_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.303/3440</a>
265_8090	DC Routine Link Register 4 Channel 6 (IPU1_DC_RL4_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.304/3441</a>
265_8094	DC Write Channel 8 Configuration 1 Register (IPU1_DC_WR_CH_CONF1_8)	32	R/W	0000_0000h	<a href="#">37.5.305/3442</a>
265_8098	DC Write Channel 8 Configuration 2 Register (IPU1_DC_WR_CH_CONF2_8)	32	R/W	0000_0000h	<a href="#">37.5.306/3443</a>
265_809C	DC Routine Link Register 1 Channel 8 (IPU1_DC_RL1_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.307/3443</a>
265_80A0	DC Routine Link Register 2 Channel 8 (IPU1_DC_RL2_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.308/3444</a>
265_80A4	DC Routine Link Register 3 Channel 8 (IPU1_DC_RL3_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.309/3445</a>
265_80A8	DC Routine Link Register 4 Channel 8 (IPU1_DC_RL4_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.310/3445</a>
265_80AC	DC Routine Link Register 5 Channel 8 (IPU1_DC_RL5_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.311/3446</a>
265_80B0	DC Routine Link Register 6 Channel 8 (IPU1_DC_RL6_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.312/3447</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
265_80B4	DC Write Channel 9 Configuration 1 Register (IPU1_DC_WR_CH_CONF1_9)	32	R/W	0000_0000h	<a href="#">37.5.313/3447</a>
265_80B8	DC Write Channel 9 Configuration 2 Register (IPU1_DC_WR_CH_CONF2_9)	32	R/W	0000_0000h	<a href="#">37.5.314/3448</a>
265_80BC	DC Routine Link Register 1 Channel 9 (IPU1_DC_RL1_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.315/3449</a>
265_80C0	DC Routine Link Register 2 Channel 9 (IPU1_DC_RL2_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.316/3449</a>
265_80C4	DC Routine Link Register 3 Channel 9 (IPU1_DC_RL3_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.317/3450</a>
265_80C8	DC Routine Link Register 4 Channel 9 (IPU1_DC_RL4_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.318/3451</a>
265_80CC	DC Routine Link Register 5 Channel 9 (IPU1_DC_RL5_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.319/3452</a>
265_80D0	DC Routine Link Register 6 Channel 9 (IPU1_DC_RL6_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.320/3452</a>
265_80D4	DC General Register (IPU1_DC_GEN)	32	R/W	0000_0060h	<a href="#">37.5.321/3453</a>
265_80D8	DC Display Configuration 1 Register 0 (IPU1_DC_DISP_CONF1_0)	32	R/W	0000_0042h	<a href="#">37.5.322/3455</a>
265_80DC	DC Display Configuration 1 Register 1 (IPU1_DC_DISP_CONF1_1)	32	R/W	0000_0042h	<a href="#">37.5.323/3456</a>
265_80E0	DC Display Configuration 1 Register 2 (IPU1_DC_DISP_CONF1_2)	32	R/W	0000_0042h	<a href="#">37.5.324/3458</a>
265_80E4	DC Display Configuration 1 Register 3 (IPU1_DC_DISP_CONF1_3)	32	R/W	0000_0042h	<a href="#">37.5.325/3459</a>
265_80E8	DC Display Configuration 2 Register 0 (IPU1_DC_DISP_CONF2_0)	32	R/W	0000_0000h	<a href="#">37.5.326/3460</a>
265_80EC	DC Display Configuration 2 Register 1 (IPU1_DC_DISP_CONF2_1)	32	R/W	0000_0000h	<a href="#">37.5.327/3461</a>
265_80F0	DC Display Configuration 2 Register 2 (IPU1_DC_DISP_CONF2_2)	32	R/W	0000_0000h	<a href="#">37.5.328/3461</a>
265_80F4	DC Display Configuration 2 Register 3 (IPU1_DC_DISP_CONF2_3)	32	R/W	0000_0000h	<a href="#">37.5.329/3461</a>
265_80F8	DC DI0 Configuration Register 1 (IPU1_DC_DI0_CONF_1)	32	R/W	0000_0000h	<a href="#">37.5.330/3462</a>
265_80FC	DC DI0 Configuration Register 2 (IPU1_DC_DI0_CONF_2)	32	R/W	0000_0000h	<a href="#">37.5.331/3462</a>
265_8100	DC DI1 Configuration Register 1 (IPU1_DC_DI1_CONF_1)	32	R/W	0000_0000h	<a href="#">37.5.332/3462</a>
265_8104	DC DI1 Configuration Register 2 (IPU1_DC_DI1_CONF_2)	32	R/W	0000_0000h	<a href="#">37.5.333/3463</a>
265_8108	DC Mapping Configuration Register 0 (IPU1_DC_MAP_CONF_0)	32	R/W	0000_0000h	<a href="#">37.5.334/3463</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
265_810C	DC Mapping Configuration Register 1 (IPU1_DC_MAP_CONF_1)	32	R/W	0000_0000h	<a href="#">37.5.335/3464</a>
265_8110	DC Mapping Configuration Register 2 (IPU1_DC_MAP_CONF_2)	32	R/W	0000_0000h	<a href="#">37.5.336/3465</a>
265_8114	DC Mapping Configuration Register 3 (IPU1_DC_MAP_CONF_3)	32	R/W	0000_0000h	<a href="#">37.5.337/3466</a>
265_8118	DC Mapping Configuration Register 4 (IPU1_DC_MAP_CONF_4)	32	R/W	0000_0000h	<a href="#">37.5.338/3467</a>
265_811C	DC Mapping Configuration Register 5 (IPU1_DC_MAP_CONF_5)	32	R/W	0000_0000h	<a href="#">37.5.339/3468</a>
265_8120	DC Mapping Configuration Register 6 (IPU1_DC_MAP_CONF_6)	32	R/W	0000_0000h	<a href="#">37.5.340/3469</a>
265_8124	DC Mapping Configuration Register 7 (IPU1_DC_MAP_CONF_7)	32	R/W	0000_0000h	<a href="#">37.5.341/3470</a>
265_8128	DC Mapping Configuration Register 8 (IPU1_DC_MAP_CONF_8)	32	R/W	0000_0000h	<a href="#">37.5.342/3471</a>
265_812C	DC Mapping Configuration Register 9 (IPU1_DC_MAP_CONF_9)	32	R/W	0000_0000h	<a href="#">37.5.343/3472</a>
265_8130	DC Mapping Configuration Register 10 (IPU1_DC_MAP_CONF_10)	32	R/W	0000_0000h	<a href="#">37.5.344/3473</a>
265_8134	DC Mapping Configuration Register 11 (IPU1_DC_MAP_CONF_11)	32	R/W	0000_0000h	<a href="#">37.5.345/3474</a>
265_8138	DC Mapping Configuration Register 12 (IPU1_DC_MAP_CONF_12)	32	R/W	0000_0000h	<a href="#">37.5.346/3475</a>
265_813C	DC Mapping Configuration Register 13 (IPU1_DC_MAP_CONF_13)	32	R/W	0000_0000h	<a href="#">37.5.347/3476</a>
265_8140	DC Mapping Configuration Register 14 (IPU1_DC_MAP_CONF_14)	32	R/W	0000_0000h	<a href="#">37.5.348/3477</a>
265_8144	DC Mapping Configuration Register 15 (IPU1_DC_MAP_CONF_15)	32	R/W	0000_0000h	<a href="#">37.5.349/3478</a>
265_8148	DC Mapping Configuration Register 16 (IPU1_DC_MAP_CONF_16)	32	R/W	0000_0000h	<a href="#">37.5.350/3478</a>
265_814C	DC Mapping Configuration Register 17 (IPU1_DC_MAP_CONF_17)	32	R/W	0000_0000h	<a href="#">37.5.351/3479</a>
265_8150	DC Mapping Configuration Register 18 (IPU1_DC_MAP_CONF_18)	32	R/W	0000_0000h	<a href="#">37.5.352/3480</a>
265_8154	DC Mapping Configuration Register 19 (IPU1_DC_MAP_CONF_19)	32	R/W	0000_0000h	<a href="#">37.5.353/3480</a>
265_8158	DC Mapping Configuration Register 20 (IPU1_DC_MAP_CONF_20)	32	R/W	0000_0000h	<a href="#">37.5.354/3481</a>
265_815C	DC Mapping Configuration Register 21 (IPU1_DC_MAP_CONF_21)	32	R/W	0000_0000h	<a href="#">37.5.355/3482</a>
265_8160	DC Mapping Configuration Register 22 (IPU1_DC_MAP_CONF_22)	32	R/W	0000_0000h	<a href="#">37.5.356/3482</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
265_8164	DC Mapping Configuration Register 23 (IPU1_DC_MAP_CONF_23)	32	R/W	0000_0000h	<a href="#">37.5.357/3483</a>
265_8168	DC Mapping Configuration Register 24 (IPU1_DC_MAP_CONF_24)	32	R/W	0000_0000h	<a href="#">37.5.358/3484</a>
265_816C	DC Mapping Configuration Register 25 (IPU1_DC_MAP_CONF_25)	32	R/W	0000_0000h	<a href="#">37.5.359/3484</a>
265_8170	DC Mapping Configuration Register 26 (IPU1_DC_MAP_CONF_26)	32	R/W	0000_0000h	<a href="#">37.5.360/3485</a>
265_8174	DC User General Data Event 0 Register 0 (IPU1_DC_UGDE0_0)	32	R/W	0000_0000h	<a href="#">37.5.361/3486</a>
265_8178	DC User General Data Event 0 Register 1 (IPU1_DC_UGDE0_1)	32	R/W	0000_0000h	<a href="#">37.5.362/3487</a>
265_817C	DC User General Data Event 0 Register2 (IPU1_DC_UGDE0_2)	32	R/W	0000_0000h	<a href="#">37.5.363/3488</a>
265_8180	DC User General Data Event 0 Register 3 (IPU1_DC_UGDE0_3)	32	R/W	0000_0000h	<a href="#">37.5.364/3488</a>
265_8184	DC User General Data Event 1Register0 (IPU1_DC_UGDE1_0)	32	R/W	0000_0000h	<a href="#">37.5.365/3489</a>
265_8188	DC User General Data Event 1 Register 1 (IPU1_DC_UGDE1_1)	32	R/W	0000_0000h	<a href="#">37.5.366/3490</a>
265_818C	DC User General Data Event 1Register 2 (IPU1_DC_UGDE1_2)	32	R/W	0000_0000h	<a href="#">37.5.367/3491</a>
265_8190	DC User General Data Event 1Register 3 (IPU1_DC_UGDE1_3)	32	R/W	0000_0000h	<a href="#">37.5.368/3491</a>
265_8194	DC User General Data Event 2 Register 0 (IPU1_DC_UGDE2_0)	32	R/W	0000_0000h	<a href="#">37.5.369/3492</a>
265_8198	DC User General Data Event 2 Register 1 (IPU1_DC_UGDE2_1)	32	R/W	0000_0000h	<a href="#">37.5.370/3493</a>
265_819C	DC User General Data Event 2Register 2 (IPU1_DC_UGDE2_2)	32	R/W	0000_0000h	<a href="#">37.5.371/3494</a>
265_81A0	DC User General Data Event 2Register 3 (IPU1_DC_UGDE2_3)	32	R/W	0000_0000h	<a href="#">37.5.372/3494</a>
265_81A4	DC User General Data Event 3Register 0 (IPU1_DC_UGDE3_0)	32	R/W	0000_0000h	<a href="#">37.5.373/3495</a>
265_81A8	DC User General Data Event 3Register 1 (IPU1_DC_UGDE3_1)	32	R/W	0000_0000h	<a href="#">37.5.374/3496</a>
265_81AC	DC User General Data Event 3Register 2 (IPU1_DC_UGDE3_2)	32	R/W	0000_0000h	<a href="#">37.5.375/3497</a>
265_81B0	DC User General Data Event 3Register 2 (IPU1_DC_UGDE3_3)	32	R/W	0000_0000h	<a href="#">37.5.376/3497</a>
265_81B4	DC Low Level Access Control Register 0 (IPU1_DC_LLA0)	32	R/W	0000_0000h	<a href="#">37.5.377/3497</a>
265_81B8	DC Low Level Access Control Register 1 (IPU1_DC_LLA1)	32	R/W	0000_0000h	<a href="#">37.5.378/3498</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
265_81BC	DC Read Low Level Read Access Control Register 0 (IPU1_DC_R_LLA0)	32	R/W	0000_0000h	<a href="#">37.5.379/3498</a>
265_81C0	DC Read Low Level Read Access Control Register1 (IPU1_DC_R_LLA1)	32	R/W	0000_0000h	<a href="#">37.5.380/3499</a>
265_81C4	DC Write Channel 5 Configuration Register (IPU1_DC_WR_CH_ADDR_5_ALT)	32	R/W	0000_0000h	<a href="#">37.5.381/3499</a>
265_81C8	DC Status Register (IPU1_DC_STAT)	32	R	0000_00AAh	<a href="#">37.5.382/3501</a>
266_0000	DMFC Read Channel Register (IPU1_DMFC_RD_CHAN)	32	R/W	0000_0200h	<a href="#">37.5.383/3503</a>
266_0004	DMFC Write Channel Register (IPU1_DMFC_WR_CHAN)	32	R/W	0000_0000h	<a href="#">37.5.384/3505</a>
266_0008	DMFC Write Channel Definition Register (IPU1_DMFC_WR_CHAN_DEF)	32	R/W	2020_2020h	<a href="#">37.5.385/3508</a>
266_000C	DMFC Display Processor Channel Register (IPU1_DMFC_DP_CHAN)	32	R/W	0000_0000h	<a href="#">37.5.386/3510</a>
266_0010	DMFC Display Processor Channel Definition Register (IPU1_DMFC_DP_CHAN_DEF)	32	R/W	2020_2020h	<a href="#">37.5.387/3513</a>
266_0014	DMFC General 1 Register (IPU1_DMFC_GENERAL_1)	32	R/W	0000_0003h	<a href="#">37.5.388/3515</a>
266_0018	DMFC General 2 Register (IPU1_DMFC_GENERAL_2)	32	R/W	0000_0000h	<a href="#">37.5.389/3517</a>
266_001C	DMFC IC Interface Control Register (IPU1_DMFC_IC_CTRL)	32	R/W	0000_0002h	<a href="#">37.5.390/3518</a>
266_0020	DMFC Write Channel Alternate Register (IPU1_DMFC_WR_CHAN_ALT)	32	R/W	0000_0000h	<a href="#">37.5.391/3519</a>
266_0024	DMFC Write Channel Definition Alternate Register (IPU1_DMFC_WR_CHAN_DEF_ALT)	32	R/W	0000_2000h	<a href="#">37.5.392/3520</a>
266_0028	DMFC MFC Display Processor Channel Alternate Register (IPU1_DMFC_DP_CHAN_ALT)	32	R/W	0000_0000h	<a href="#">37.5.393/3521</a>
266_002C	DMFC Display Channel Definition Alternate Register (IPU1_DMFC_DP_CHAN_DEF_ALT)	32	R/W	2020_0020h	<a href="#">37.5.394/3524</a>
266_0030	DMFC General 1 Alternate Register (IPU1_DMFC_GENERAL1_ALT)	32	R/W	0000_0000h	<a href="#">37.5.395/3526</a>
266_0034	DMFC Status Register (IPU1_DMFC_STAT)	32	R	02FF_F000h	<a href="#">37.5.396/3528</a>
266_8000	VDI Field Size Register (IPU1_VDIFSIZE)	32	R/W	0000_0000h	<a href="#">37.5.397/3529</a>
266_8004	VDI Control Register (IPU1_VDI_C)	32	R/W	0000_0000h	<a href="#">37.5.398/3530</a>
266_8008	VDI Control Register 2 (IPU1_VDI_C2_)	32	R/W	0000_0000h	<a href="#">37.5.399/3532</a>
266_800C	VDI Combining Parameters Register 1 (IPU1_VDI_CMDP_1)	32	R/W	0000_0000h	<a href="#">37.5.400/3533</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
266_8010	VDI Combining Parameters Register 2 (IPU1_VDI_CMDP_2)	32	R/W	0000_0000h	37.5.401/ 3534
266_8014	VDI Plane Size Register 1 (IPU1_VDI_PS_1)	32	R/W	0000_0000h	37.5.402/ 3534
266_8018	VDI Plane Size Register 2 (IPU1_VDI_PS_2)	32	R/W	0000_0000h	37.5.403/ 3535
266_801C	VDI Plane Size Register 3 (IPU1_VDI_PS_3)	32	R/W	0000_0000h	37.5.404/ 3536
266_8020	VDI Plane Size Register 4 (IPU1_VDI_PS_4)	32	R/W	0000_0000h	37.5.405/ 3536
2A0_0000	Configuration Register (IPU2_CONF)	32	R/W	0000_0000h	37.5.1/2959
2A0_0004	SISG Control 0 Register (IPU2_SISG_CTRL0)	32	R/W	0000_0000h	37.5.2/2962
2A0_0008	SISG Control 1 Register (IPU2_SISG_CTRL1)	32	R/W	0000_0000h	37.5.3/2963
2A0_000C	SISG Set<i> Register (IPU2_SISG_SET_i)	32	R/W	0000_0000h	37.5.4/2963
2A0_0024	SISG Clear <i> Register (IPU2_SISG_CLR_i)	32	R/W	0000_0000h	37.5.5/2964
2A0_003C	Interrupt Control Register 1 (IPU2_INT_CTRL_1)	32	R/W	0000_0000h	37.5.6/2964
2A0_0040	Interrupt Control Register 2 (IPU2_INT_CTRL_2)	32	R/W	0000_0000h	37.5.7/2968
2A0_0044	Interrupt Control Register 3 (IPU2_INT_CTRL_3)	32	R/W	0000_0000h	37.5.8/2971
2A0_0048	Interrupt Control Register 4 (IPU2_INT_CTRL_4)	32	R/W	0000_0000h	37.5.9/2975
2A0_004C	Interrupt Control Register 5 (IPU2_INT_CTRL_5)	32	R/W	0000_0000h	37.5.10/ 2978
2A0_0050	Interrupt Control Register 6 (IPU2_INT_CTRL_6)	32	R/W	0000_0000h	37.5.11/ 2983
2A0_0054	Interrupt Control Register 7 (IPU2_INT_CTRL_7)	32	R/W	0000_0000h	37.5.12/ 2986
2A0_0058	Interrupt Control Register 8 (IPU2_INT_CTRL_8)	32	R/W	0000_0000h	37.5.13/ 2988
2A0_005C	Interrupt Control Register 9 (IPU2_INT_CTRL_9)	32	R/W	0000_0000h	37.5.14/ 2990
2A0_0060	Interrupt Control Register 10 (IPU2_INT_CTRL_10)	32	R/W	0000_0000h	37.5.15/ 2992
2A0_0064	Interrupt Control Register 11 (IPU2_INT_CTRL_11)	32	R/W	0000_0000h	37.5.16/ 2994
2A0_0068	Interrupt Control Register 12 (IPU2_INT_CTRL_12)	32	R/W	0000_0000h	37.5.17/ 2997
2A0_006C	Interrupt Control Register 13 (IPU2_INT_CTRL_13)	32	R/W	0000_0000h	37.5.18/ 2999
2A0_0070	Interrupt Control Register 14 (IPU2_INT_CTRL_14)	32	R/W	0000_0000h	37.5.19/ 3003
2A0_0074	Interrupt Control Register 15 (IPU2_INT_CTRL_15)	32	R/W	0000_0000h	37.5.20/ 3006
2A0_0078	SDMA Event Control Register 1 (IPU2_SDMA_EVENT_1)	32	R/W	0000_0000h	37.5.21/ 3010

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**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A0_007C	SDMA Event Control Register 2 (IPU2_SDMA_EVENT_2)	32	R/W	0000_0000h	<a href="#">37.5.22/ 3014</a>
2A0_0080	SDMA Event Control Register 3 (IPU2_SDMA_EVENT_3)	32	R/W	0000_0000h	<a href="#">37.5.23/ 3017</a>
2A0_0084	SDMA Event Control Register 4 (IPU2_SDMA_EVENT_4)	32	R/W	0000_0000h	<a href="#">37.5.24/ 3022</a>
2A0_0088	SDMA Event Control Register 7 (IPU2_SDMA_EVENT_7)	32	R/W	0000_0000h	<a href="#">37.5.25/ 3025</a>
2A0_008C	SDMA Event Control Register 8 (IPU2_SDMA_EVENT_8)	32	R/W	0000_0000h	<a href="#">37.5.26/ 3027</a>
2A0_0090	SDMA Event Control Register 11 (IPU2_SDMA_EVENT_11)	32	R/W	0000_0000h	<a href="#">37.5.27/ 3028</a>
2A0_0094	SDMA Event Control Register 12 (IPU2_SDMA_EVENT_12)	32	R/W	0000_0000h	<a href="#">37.5.28/ 3031</a>
2A0_0098	SDMA Event Control Register 13 (IPU2_SDMA_EVENT_13)	32	R/W	0000_0000h	<a href="#">37.5.29/ 3033</a>
2A0_009C	SDMA Event Control Register 14 (IPU2_SDMA_EVENT_14)	32	R/W	0000_0000h	<a href="#">37.5.30/ 3037</a>
2A0_00A0	Shadow Registers Memory Priority 1 Register (IPU2_SRMM_PRI1)	32	R/W	0000_0100h	<a href="#">37.5.31/ 3040</a>
2A0_00A4	Shadow Registers Memory Priority 2 Register (IPU2_SRMM_PRI2)	32	R/W	0605_0803h	<a href="#">37.5.32/ 3041</a>
2A0_00A8	FSU Processing Flow 1 Register (IPU2_FS_PROC_FLOW1)	32	R/W	0000_0000h	<a href="#">37.5.33/ 3043</a>
2A0_00AC	FSU Processing Flow 2 Register (IPU2_FS_PROC_FLOW2)	32	R/W	0000_0000h	<a href="#">37.5.34/ 3047</a>
2A0_00B0	FSU Processing Flow 3 Register (IPU2_FS_PROC_FLOW3)	32	R/W	0000_0000h	<a href="#">37.5.35/ 3050</a>
2A0_00B4	FSU Displaying Flow 1 Register (IPU2_FS_DISP_FLOW1)	32	R/W	0000_0000h	<a href="#">37.5.36/ 3053</a>
2A0_00B8	FSU Displaying Flow 2 Register (IPU2_FS_DISP_FLOW2)	32	R/W	0000_0000h	<a href="#">37.5.37/ 3056</a>
2A0_00BC	SKIP Register (IPU2_SKIP)	32	R/W	0000_0000h	<a href="#">37.5.38/ 3058</a>
2A0_00C4	Display General Control Register (IPU2_DISP_GEN)	32	R/W	0040_0000h	<a href="#">37.5.39/ 3060</a>
2A0_00C8	Display Alternate Flow Control Register 1 (IPU2_DISP_ALT1)	32	R/W	0040_0000h	<a href="#">37.5.40/ 3063</a>
2A0_00CC	Display Alternate Flow Control Register 2 (IPU2_DISP_ALT2)	32	R/W	0000_0000h	<a href="#">37.5.41/ 3064</a>
2A0_00D0	Display Alternate Flow Control Register 3 (IPU2_DISP_ALT3)	32	R/W	0040_0000h	<a href="#">37.5.42/ 3065</a>
2A0_00D4	Display Alternate Flow Control Register 4 (IPU2_DISP_ALT4)	32	R/W	0000_0000h	<a href="#">37.5.43/ 3067</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A0_00DC	Memory Reset Control Register (IPU2_MEM_RST)	32	R/W	0000_0000h	<a href="#">37.5.44/3068</a>
2A0_00E0	Power Modes Control Register (IPU2_PM)	32	R/W	0810_0810h	<a href="#">37.5.45/3070</a>
2A0_00E4	General Purpose Register (IPU2_GPR)	32	R/W	0000_0000h	<a href="#">37.5.46/3073</a>
2A0_0150	Channel Double Buffer Mode Select 0 Register (IPU2_CH_DB_MODE_SEL0)	32	R/W	0000_0000h	<a href="#">37.5.47/3075</a>
2A0_0154	Channel Double Buffer Mode Select 1 Register (IPU2_CH_DB_MODE_SEL1)	32	R/W	0000_0000h	<a href="#">37.5.48/3079</a>
2A0_0168	Alternate Channel Double Buffer Mode Select 0 Register (IPU2_ALT_CH_DB_MODE_SEL0)	32	R/W	0000_0000h	<a href="#">37.5.49/3082</a>
2A0_016C	Alternate Channel Double Buffer Mode Select1 Register (IPU2_ALT_CH_DB_MODE_SEL1)	32	R/W	0000_0000h	<a href="#">37.5.50/3084</a>
2A0_0178	Alternate Channel Triple Buffer Mode Select 0 Register (IPU2_ALT_CH_TRB_MODE_SEL0)	32	R/W	0000_0000h	<a href="#">37.5.51/3085</a>
2A0_0200	Interrupt Status Register 1 (IPU2_INT_STAT_1)	32	w1c	0000_0000h	<a href="#">37.5.52/3088</a>
2A0_0204	Interrupt Status Register2 (IPU2_INT_STAT_2)	32	w1c	0000_0000h	<a href="#">37.5.53/3093</a>
2A0_0208	Interrupt Status Register 3 (IPU2_INT_STAT_3)	32	w1c	0000_0000h	<a href="#">37.5.54/3096</a>
2A0_020C	Interrupt Status Register 4 (IPU2_INT_STAT_4)	32	w1c	0000_0000h	<a href="#">37.5.55/3100</a>
2A0_0210	Interrupt Status Register 5 (IPU2_INT_STAT_5)	32	w1c	0000_0000h	<a href="#">37.5.56/3103</a>
2A0_0214	Interrupt Status Register 6 (IPU2_INT_STAT_6)	32	w1c	0000_0000h	<a href="#">37.5.57/3108</a>
2A0_0218	Interrupt Status Register7 1 (IPU2_INT_STAT_7)	32	w1c	0000_0000h	<a href="#">37.5.58/3111</a>
2A0_021C	Interrupt Status Register 8 (IPU2_INT_STAT_8)	32	w1c	0000_0000h	<a href="#">37.5.59/3114</a>
2A0_0220	Interrupt Status Register 9 (IPU2_INT_STAT_9)	32	w1c	0000_0000h	<a href="#">37.5.60/3117</a>
2A0_0224	Interrupt Status Register 10 (IPU2_INT_STAT_10)	32	w1c	0000_0000h	<a href="#">37.5.61/3119</a>
2A0_0228	Interrupt Status Register 11 (IPU2_INT_STAT_11)	32	w1c	0000_0000h	<a href="#">37.5.62/3122</a>
2A0_022C	Interrupt Status Register 12 (IPU2_INT_STAT_12)	32	w1c	0000_0000h	<a href="#">37.5.63/3126</a>
2A0_0230	Interrupt Status Register 13 (IPU2_INT_STAT_13)	32	w1c	0000_0000h	<a href="#">37.5.64/3128</a>
2A0_0234	Interrupt Status Register 14 (IPU2_INT_STAT_14)	32	w1c	0000_0000h	<a href="#">37.5.65/3133</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A0_0238	Interrupt Status Register 15 (IPU2_INT_STAT_15)	32	w1c	0000_0000h	<a href="#">37.5.66/ 3136</a>
2A0_023C	Current Buffer Register 0 (IPU2_CUR_BUF_0)	32	R	0000_0000h	<a href="#">37.5.67/ 3140</a>
2A0_0240	Current Buffer Register 1 (IPU2_CUR_BUF_1)	32	R	0000_0000h	<a href="#">37.5.68/ 3145</a>
2A0_0244	Alternate Current Buffer Register 0 (IPU2_ALT_CUR_0)	32	R	0000_0000h	<a href="#">37.5.69/ 3149</a>
2A0_0248	Alternate Current Buffer Register 1 (IPU2_ALT_CUR_1)	32	R	0000_0000h	<a href="#">37.5.70/ 3151</a>
2A0_024C	Shadow Registers Memory Status Register (IPU2_SRMM_STAT)	32	R	0000_0000h	<a href="#">37.5.71/ 3154</a>
2A0_0250	Processing Status Tasks Register (IPU2_PROC_TASKS_STAT)	32	R	0000_0000h	<a href="#">37.5.72/ 3156</a>
2A0_0254	Display Tasks Status Register (IPU2_DISP_TASKS_STAT)	32	R	0000_0000h	<a href="#">37.5.73/ 3158</a>
2A0_0258	Triple Current Buffer Register 0 (IPU2_TRIPLE_CUR_BUF_0)	32	R	0000_0000h	<a href="#">37.5.74/ 3160</a>
2A0_025C	Triple Current Buffer Register 1 (IPU2_TRIPLE_CUR_BUF_1)	32	R	0000_0000h	<a href="#">37.5.75/ 3162</a>
2A0_0268	IPU Channels Buffer 0 Ready 0 Register (IPU2_CH_BUF0_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.76/ 3163</a>
2A0_026C	IPU Channels Buffer 0 Ready 1 Register (IPU2_CH_BUF0_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.77/ 3167</a>
2A0_0270	IPU Channels Buffer 1 Ready 0 Register (IPU2_CH_BUF1_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.78/ 3169</a>
2A0_0274	IPU Channels Buffer 1 Ready 1 Register (IPU2_CH_BUF1_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.79/ 3172</a>
2A0_0278	IPU Alternate Channels Buffer 0 Ready 0 Register (IPU2_ALT_CH_BUF0_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.80/ 3175</a>
2A0_027C	IPU Alternate Channels Buffer 0 Ready 1 Register (IPU2_ALT_CH_BUF0_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.81/ 3176</a>
2A0_0280	IPU Alternate Channels Buffer1 Ready 0 Register (IPU2_ALT_CH_BUF1_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.82/ 3177</a>
2A0_0284	IPU Alternate Channels Buffer 1 Ready 1 Register (IPU2_ALT_CH_BUF1_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.83/ 3178</a>
2A0_0288	IPU Channels Buffer 2 Ready 0 Register (IPU2_CH_BUF2_RDY0)	32	R/W	0000_0000h	<a href="#">37.5.84/ 3179</a>
2A0_028C	IPU Channels Buffer 2 Ready 1 Register (IPU2_CH_BUF2_RDY1)	32	R/W	0000_0000h	<a href="#">37.5.85/ 3181</a>
2A0_8000	IDMAC Configuration Register (IPU2_IDMAC_CONF)	32	R/W	0000_002Fh	<a href="#">37.5.86/ 3182</a>
2A0_8004	IDMAC Channel Enable 1 Register (IPU2_IDMAC_CH_EN_1)	32	R/W	0000_0000h	<a href="#">37.5.87/ 3184</a>

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## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A0_8008	IDMAC Channel Enable 2 Register (IPU2_IDMAC_CH_EN_2)	32	R/W	0000_0000h	<a href="#">37.5.88/ 3187</a>
2A0_800C	IDMAC Separate Alpha Indication Register (IPU2_IDMAC_SEP_ALPHA)	32	R/W	0000_0000h	<a href="#">37.5.89/ 3189</a>
2A0_8010	IDMAC Alternate Separate Alpha Indication Register (IPU2_IDMAC_ALT_SEP_ALPHA)	32	R/W	0000_0000h	<a href="#">37.5.90/ 3191</a>
2A0_8014	IDMAC Channel Priority 1 Register (IPU2_IDMAC_CH_PRI_1)	32	R/W	0000_0000h	<a href="#">37.5.91/ 3193</a>
2A0_8018	IDMAC Channel Priority 2 Register (IPU2_IDMAC_CH_PRI_2)	32	R/W	0000_0000h	<a href="#">37.5.92/ 3196</a>
2A0_801C	IDMAC Channel Watermark Enable 1 Register (IPU2_IDMAC_WM_EN_1)	32	R/W	0000_0000h	<a href="#">37.5.93/ 3198</a>
2A0_8020	IDMAC Channel Watermark Enable 2 Register (IPU2_IDMAC_WM_EN_2)	32	R/W	0000_0000h	<a href="#">37.5.94/ 3200</a>
2A0_8024	IDMAC Channel Lock Enable 1 Register (IPU2_IDMAC_LOCK_EN_1)	32	R/W	0000_0000h	<a href="#">37.5.95/ 3201</a>
2A0_8028	IDMAC Channel Lock Enable 2 Register (IPU2_IDMAC_LOCK_EN_2)	32	R/W	0000_0000h	<a href="#">37.5.96/ 3203</a>
2A0_802C	IDMAC Channel Alternate Address 0 Register (IPU2_IDMAC_SUB_ADDR_0)	32	R/W	0000_0000h	<a href="#">37.5.97/ 3204</a>
2A0_8030	IDMAC Channel Alternate Address 1 Register (IPU2_IDMAC_SUB_ADDR_1)	32	R/W	0000_0000h	<a href="#">37.5.98/ 3205</a>
2A0_8034	IDMAC Channel Alternate Address 2 Register (IPU2_IDMAC_SUB_ADDR_2)	32	R/W	0000_0000h	<a href="#">37.5.99/ 3206</a>
2A0_8038	IDMAC Channel Alternate Address 3 Register (IPU2_IDMAC_SUB_ADDR_3)	32	R/W	0000_0000h	<a href="#">37.5.100/ 3207</a>
2A0_803C	IDMAC Channel Alternate Address 4 Register (IPU2_IDMAC_SUB_ADDR_4)	32	R/W	0000_0000h	<a href="#">37.5.101/ 3209</a>
2A0_8040	IDMAC Band Mode Enable 1 Register (IPU2_IDMAC_BNDM_EN_1)	32	R/W	0000_0000h	<a href="#">37.5.102/ 3210</a>
2A0_8044	IDMAC Band Mode Enable 2 Register (IPU2_IDMAC_BNDM_EN_2)	32	R/W	0000_0000h	<a href="#">37.5.103/ 3213</a>
2A0_8048	IDMAC Scroll Coordinations Register (IPU2_IDMAC_SC_CORD)	32	R/W	0000_0000h	<a href="#">37.5.104/ 3214</a>
2A0_804C	IDMAC Scroll Coordinations Register 1 (IPU2_IDMAC_SC_CORD_1)	32	R/W	0000_0000h	<a href="#">37.5.105/ 3215</a>
2A0_8100	IDMAC Channel Busy 1 Register (IPU2_IDMAC_CH_BUSY_1)	32	R	0000_0000h	<a href="#">37.5.106/ 3216</a>
2A0_8104	IDMAC Channel Busy 2 Register (IPU2_IDMAC_CH_BUSY_2)	32	R	0000_0000h	<a href="#">37.5.107/ 3222</a>
2A1_8000	DP Common Configuration Sync Flow Register (IPU2_DP_COM_CONF_SYNC)	32	R/W	0000_0000h	<a href="#">37.5.108/ 3226</a>
2A1_8004	DP Graphic Window Control Sync Flow Register (IPU2_DP_Graph_Wind_CTRL_SYNC)	32	R/W	0000_0000h	<a href="#">37.5.109/ 3228</a>

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**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A1_8008	DP Partial Plane Window Position Sync Flow Register (IPU2_DP_FG_POS_SYNC)	32	R/W	0000_0000h	<a href="#">37.5.110/ 3229</a>
2A1_800C	DP Cursor Position and Size Sync Flow Register (IPU2_DP_CUR_POS_SYNC)	32	R/W	0000_0000h	<a href="#">37.5.111/ 3229</a>
2A1_8010	DP Color Cursor Mapping Sync Flow Register (IPU2_DP_CUR_MAP_SYNC)	32	R/W	0000_0000h	<a href="#">37.5.112/ 3230</a>
2A1_8014	DP Gamma Constants Sync Flow Register i (IPU2_DP_GAMMA_C_SYNC_i)	32	R/W	0000_0000h	<a href="#">37.5.113/ 3231</a>
2A1_8034	DP Gamma Correction Slope Sync Flow Register i (IPU2_DP_GAMMA_S_SYNC_i)	32	R/W	0000_0000h	<a href="#">37.5.114/ 3231</a>
2A1_8044	DP Color Space Conversion Control Sync Flow Registers (IPU2_DP_CSCA_SYNC_i)	32	R/W	0000_0000h	<a href="#">37.5.115/ 3232</a>
2A1_8054	DP Color Conversion Control Sync Flow Register 0 (IPU2_DP_SCS_SYNC_0)	32	R/W	0000_0000h	<a href="#">37.5.116/ 3233</a>
2A1_8058	DP Color Conversion Control Sync Flow Register 1 (IPU2_DP_SCS_SYNC_1)	32	R/W	0000_0000h	<a href="#">37.5.117/ 3233</a>
2A1_805C	DP Cursor Position and Size Alternate Register (IPU2_DP_CUR_POS_ALT)	32	R/W	0000_0000h	<a href="#">37.5.118/ 3234</a>
2A1_8060	DP Common Configuration Async 0 Flow Register (IPU2_DP_COM_CONF_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.119/ 3235</a>
2A1_8064	DP Graphic Window Control Async 0 Flow Register (IPU2_DP_GRAPH_WIND_CTRL_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.120/ 3237</a>
2A1_8068	DP Partial Plane Window Position Async 0 Flow Register (IPU2_DP_FG_POS_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.121/ 3238</a>
2A1_806C	DP Cursor Position and Size Async 0 Flow Register (IPU2_DP_CUR_POS_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.122/ 3239</a>
2A1_8070	DP Color Cursor Mapping Async 0 Flow Register (IPU2_DP_CUR_MAP_ASYNC0)	32	R/W	0000_0000h	<a href="#">37.5.123/ 3239</a>
2A1_8074	DP Gamma Constant Async 0 Flow Register i (IPU2_DP_GAMMA_C_ASYNC0_i)	32	R/W	0000_0000h	<a href="#">37.5.124/ 3240</a>
2A1_8094	DP Gamma Correction Slope Async 0 Flow Register i (IPU2_DP_GAMMA_S_ASYNC0_i)	32	R/W	0000_0000h	<a href="#">37.5.125/ 3241</a>
2A1_80A4	DP Color Space Conversion Control Async 0 Flow Register i (IPU2_DP_CSCA_ASYNC0_i)	32	R/W	0000_0000h	<a href="#">37.5.126/ 3241</a>
2A1_80B4	DP Color Conversion Control Async 0 Flow Register 0 (IPU2_DP_CSC_ASYNC0_0)	32	R/W	0000_0000h	<a href="#">37.5.127/ 3242</a>
2A1_80B8	DP Color Conversion Control Async 1 Flow Register (IPU2_DP_CSC_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.128/ 3243</a>
2A1_80BC	DP Common Configuration Async 1 Flow Register (IPU2_DP_COM_CONF_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.129/ 3244</a>
2A1_80BC	DP Debug Control Register (IPU2_DP_DEBUG_CNT)	32	R/W	0000_0000h	<a href="#">37.5.130/ 3246</a>
2A1_80C0	DP Graphic Window Control Async 1 Flow Register (IPU2_DP_GRAPH_WIND_CTRL_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.131/ 3247</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A1_80C0	DP Debug Status Register (IPU2_DP_DEBUG_STAT)	32	R	0000_0000h	<a href="#">37.5.132/3248</a>
2A1_80C4	DP Partial Plane Window Position Async 1 Flow Register (IPU2_DP_FG_POS_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.133/3250</a>
2A1_80C8	DP Cursor Postion and Size Async 1 Flow Register (IPU2_DP_CUR_POS_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.134/3250</a>
2A1_80CC	DP Color Cursor Mapping Async 1 Flow Register (IPU2_DP_CUR_MAP_ASYNC1)	32	R/W	0000_0000h	<a href="#">37.5.135/3251</a>
2A1_80D0	DP Gamma Constants Async 1 Flow Register i (IPU2_DP_GAMMA_C_ASYNC1_i)	32	R/W	0000_0000h	<a href="#">37.5.136/3252</a>
2A1_80F0	DP Gamma Correction Slope Async 1 Flow Register i (IPU2_DP_GAMMA_S_ASYN1_i)	32	R/W	0000_0000h	<a href="#">37.5.137/3253</a>
2A1_8100	DP Color Space Converstion Control Async 1 Flow Register i (IPU2_DP_CSCA_ASYNC1_i)	32	R/W	0000_0000h	<a href="#">37.5.138/3253</a>
2A1_8110	DP Color Conversion Control Async 1 Flow Register 0 (IPU2_DP_CSC_ASYNC1_0)	32	R/W	0000_0000h	<a href="#">37.5.139/3254</a>
2A1_8114	DP Color Conversion Control Async 1 Flow Register 1 (IPU2_DP_CSC_ASYNC1_1)	32	R/W	0000_0000h	<a href="#">37.5.140/3255</a>
2A2_0000	IC Configuration Register (IPU2_IC_CONF)	32	R/W	0000_0000h	<a href="#">37.5.141/3256</a>
2A2_0004	IC Preprocessing Encoder Resizing Coefficients Register (IPU2_IC_PRP_ENC_RSC)	32	R/W	2000_2000h	<a href="#">37.5.142/3258</a>
2A2_0008	IC Preprocessing View-Finder Resizing Coefficients Register (IPU2_IC_PRP_VF_RSC)	32	R/W	2000_2000h	<a href="#">37.5.143/3259</a>
2A2_000C	IC Postprocessing Encoder Resizing Coefficients Register (IPU2_IC_PP_RSC)	32	R/W	2000_2000h	<a href="#">37.5.144/3260</a>
2A2_0010	IC Combining Parameters Register 1 (IPU2_IC_CMBP_1)	32	R/W	0000_0000h	<a href="#">37.5.145/3261</a>
2A2_0014	IC Combining Parameters Register 2 (IPU2_IC_CMBP_2)	32	R/W	0000_0000h	<a href="#">37.5.146/3261</a>
2A2_0018	IC IDMAC Parameters 1 Register (IPU2_IC_IDMAC_1)	32	R/W	0000_0000h	<a href="#">37.5.147/3262</a>
2A2_001C	IC IDMAC Parameters 2 Register (IPU2_IC_IDMAC_2)	32	R/W	0000_0000h	<a href="#">37.5.148/3265</a>
2A2_0020	IC IDMAC Parameters 3Register (IPU2_IC_IDMAC_3)	32	R/W	0000_0000h	<a href="#">37.5.149/3266</a>
2A2_0024	IC IDMAC Parameters 4 Register (IPU2_IC_IDMAC_4)	32	R/W	0000_0000h	<a href="#">37.5.150/3266</a>
2A3_0000	CSI0 Sensor Configuration Register (IPU2_CSIO_SENS_CONF)	32	R/W	0000_0000h	<a href="#">37.5.151/3267</a>
2A3_0004	CSI0 Sense Frame Size Register (IPU2_CSIO_SENS_FRM_SIZE)	32	R/W	0000_0000h	<a href="#">37.5.152/3270</a>
2A3_0008	CSI0 Actual Frame Size Register (IPU2_CSIO_ACT_FRM_SIZE)	32	R/W	0000_0000h	<a href="#">37.5.153/3270</a>

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**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A3_000C	CSI0 Output Control Register (IPU2_CSIO_OUT_FRM_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.154/3271</a>
2A3_0010	CSIO Test Control Register (IPU2_CSIO_TST_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.155/3272</a>
2A3_0014	CSIO CCIR Code Register 1 (IPU2_CSIO_CCIR_CODE_1)	32	R/W	0000_0000h	<a href="#">37.5.156/3273</a>
2A3_0018	CSIO CCIR Code Register 2 (IPU2_CSIO_CCIR_CODE_2)	32	R/W	0000_0000h	<a href="#">37.5.157/3274</a>
2A3_001C	CSIO CCIR Code Register 3 (IPU2_CSIO_CCIR_CODE_3)	32	R/W	0000_0000h	<a href="#">37.5.158/3275</a>
2A3_0020	CSIO Data Identifier Register (IPU2_CSIO_DI)	32	R/W	FFFF_FFFFh	<a href="#">37.5.159/3275</a>
2A3_0024	CSI0 SKIP Register (IPU2_CSIO_SKIP)	32	R/W	0000_0000h	<a href="#">37.5.160/3276</a>
2A3_0028	CSI0 Compander Control Register (IPU2_CSIO_CPD_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.161/3277</a>
2A3_002C	CSI0 Red Component Compander Constants Register <i> (IPU2_CSIO_CPD_RC_i)	32	R/W	0000_0000h	<a href="#">37.5.162/3278</a>
2A3_004C	CSI0 Red Component Compander SLOPE Register <i> (IPU2_CSIO_CPD_RS_i)	32	R/W	0000_0000h	<a href="#">37.5.163/3279</a>
2A3_005C	CSI0 GR Component Compander Constants Register <i> (IPU2_CSIO_CPD_GRC_i)	32	R/W	0000_0000h	<a href="#">37.5.164/3279</a>
2A3_007C	CSI0 GR Component Compander SLOPE Register <i> (IPU2_CSIO_CPD_GRS_i)	32	R/W	0000_0000h	<a href="#">37.5.165/3280</a>
2A3_008C	CSI0 GB Component Compander Constants Register <i> (IPU2_CSIO_CPD_GBC_i)	32	R/W	0000_0000h	<a href="#">37.5.166/3281</a>
2A3_00AC	CSI0 GB Component Compander SLOPE Register <i> (IPU2_CSIO_CPD_GBS_i)	32	R/W	0000_0000h	<a href="#">37.5.167/3281</a>
2A3_00BC	CSI0 Blue Component Compander Constants Register <i> (IPU2_CSIO_CPD_BC_i)	32	R/W	0000_0000h	<a href="#">37.5.168/3282</a>
2A3_00DC	CSI0 Blue Component Compander SLOPE Register <i> (IPU2_CSIO_CPD_BS_i)	32	R/W	0000_0000h	<a href="#">37.5.169/3283</a>
2A3_00EC	CSI0 Compander Offset Register 1 (IPU2_CSIO_CPD_OFFSET1)	32	R/W	0000_0000h	<a href="#">37.5.170/3283</a>
2A3_00F0	CSI0 Compander Offset Register 2 (IPU2_CSIO_CPD_OFFSET2)	32	R/W	0000_0000h	<a href="#">37.5.171/3284</a>
2A3_8000	CSI1 Sensor Configuration Register (IPU2_CS1_SENS_CONF)	32	R/W	0000_0000h	<a href="#">37.5.172/3285</a>
2A3_8004	CSI1 Sense Frame Size Register (IPU2_CS1_SENS_FRM_SIZE)	32	R/W	0000_0000h	<a href="#">37.5.173/3287</a>
2A3_8008	CSI1 Actual Frame Size Register (IPU2_CS1_ACT_FRM_SIZE)	32	R/W	0000_0000h	<a href="#">37.5.174/3288</a>
2A3_800C	CSI1 Output Control Register (IPU2_CS1_OUT_FRM_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.175/3289</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A3_8010	CSI1 Test Control Register (IPU2_CSI1_TST_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.176/3290</a>
2A3_8014	CSI1 CCIR Code Register 1 (IPU2_CSI1_CCIR_CODE_1)	32	R/W	0000_0000h	<a href="#">37.5.177/3291</a>
2A3_8018	CSI1 CCIR Code Register 2 (IPU2_CSI1_CCIR_CODE_2)	32	R/W	0000_0000h	<a href="#">37.5.178/3292</a>
2A3_801C	CSI1 CCIR Code Register 3 (IPU2_CSI1_CCIR_CODE_3)	32	R/W	0000_0000h	<a href="#">37.5.179/3293</a>
2A3_8020	CSI1 Data Identifier Register (IPU2_CSI1_DI)	32	R/W	FFFF_FFFFh	<a href="#">37.5.180/3293</a>
2A3_8024	CSI1 SKIP Register (IPU2_CSI1_SKIP)	32	R/W	0000_0000h	<a href="#">37.5.181/3294</a>
2A3_8028	CSI1 Compander Control Register (IPU2_CSI1_CPD_CTRL)	32	R/W	0000_0000h	<a href="#">37.5.182/3295</a>
2A3_802C	CSI1 Red Component Compander Constants Register <i> (IPU2_CSI1_CPD_RC_i)	32	R/W	0000_0000h	<a href="#">37.5.183/3296</a>
2A3_804C	CSI1 Red Component Compander SLOPE Register <i> (IPU2_CSI1_CPD_RS_i)	32	R/W	0000_0000h	<a href="#">37.5.184/3296</a>
2A3_805C	CSI1 GR Component Compander Constants Register <i> (IPU2_CSI1_CPD_GRC_i)	32	R/W	0000_0000h	<a href="#">37.5.185/3297</a>
2A3_807C	CSI1 GR Component Compander SLOPE Register <i> (IPU2_CSI1_CPD_GRS_i)	32	R/W	0000_0000h	<a href="#">37.5.186/3298</a>
2A3_808C	CSI1 GB Component Compander Constants Register <i> (IPU2_CSI1_CPD_GBC_i)	32	R/W	0000_0000h	<a href="#">37.5.187/3298</a>
2A3_80AC	CSI1 GB Component Compander SLOPE Register <i> (IPU2_CSI1_CPD_GBS_i)	32	R/W	0000_0000h	<a href="#">37.5.188/3299</a>
2A3_80BC	CSI1 Blue Component Compander Constants Register <i> (IPU2_CSI1_CPD_BC_i)	32	R/W	0000_0000h	<a href="#">37.5.189/3300</a>
2A3_80DC	CSI1 Blue Component Compander SLOPE Register <i> (IPU2_CSI1_CPD_BS_i)	32	R/W	0000_0000h	<a href="#">37.5.190/3300</a>
2A3_80EC	CSI1 Compander Offset Register 1 (IPU2_CSI1_CPD_OFFSET1)	32	R/W	0000_0000h	<a href="#">37.5.191/3301</a>
2A3_80F0	CSI1 Compander Offset Register 2 (IPU2_CSI1_CPD_OFFSET2)	32	R/W	0000_0000h	<a href="#">37.5.192/3302</a>
2A4_0000	DIO General Register (IPU2_DIO_GENERAL)	32	R/W	0020_0000h	<a href="#">37.5.193/3303</a>
2A4_0004	DIO Base Sync Clock Gen 0 Register (IPU2_DIO_BS_CLKGEN0)	32	R/W	0000_0000h	<a href="#">37.5.194/3305</a>
2A4_0008	DIO Base Sync Clock Gen 1 Register (IPU2_DIO_BS_CLKGEN1)	32	R/W	0000_0000h	<a href="#">37.5.195/3306</a>
2A4_000C	DIO Sync Wave Gen 1 Register 0 (IPU2_DIO_SW_GEN0_1)	32	R/W	0000_0000h	<a href="#">37.5.196/3306</a>
2A4_0010	DIO Sync Wave Gen 2 Register 0 (IPU2_DIO_SW_GEN0_2)	32	R/W	0000_0000h	<a href="#">37.5.197/3308</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A4_0014	DIO Sync Wave Gen 3 Register 0 (IPU2_DIO_SW_GEN0_3)	32	R/W	0000_0000h	<a href="#">37.5.198/3309</a>
2A4_0018	DIO Sync Wave Gen 4 Register 0 (IPU2_DIO_SW_GEN0_4)	32	R/W	0000_0000h	<a href="#">37.5.199/3310</a>
2A4_001C	DIO Sync Wave Gen 5 Register 0 (IPU2_DIO_SW_GEN0_5)	32	R/W	0000_0000h	<a href="#">37.5.200/3311</a>
2A4_0020	DIO Sync Wave Gen 6 Register 0 (IPU2_DIO_SW_GEN0_6)	32	R/W	0000_0000h	<a href="#">37.5.201/3313</a>
2A4_0024	DIO Sync Wave Gen 7 Register 0 (IPU2_DIO_SW_GEN0_7)	32	R/W	0000_0000h	<a href="#">37.5.202/3314</a>
2A4_0028	DIO Sync Wave Gen 8 Register 0 (IPU2_DIO_SW_GEN0_8)	32	R/W	0000_0000h	<a href="#">37.5.203/3315</a>
2A4_002C	DIO Sync Wave Gen 9 Register 0 (IPU2_DIO_SW_GEN0_9)	32	R/W	0000_0000h	<a href="#">37.5.204/3316</a>
2A4_0030	DIO Sync Wave Gen 1 Register 1 (IPU2_DIO_SW_GEN1_1)	32	R/W	0000_0000h	<a href="#">37.5.205/3318</a>
2A4_0034	DIO Sync Wave Gen 2 Register 1 (IPU2_DIO_SW_GEN1_2)	32	R/W	0000_0000h	<a href="#">37.5.206/3320</a>
2A4_0038	DIO Sync Wave Gen 3 Register 1 (IPU2_DIO_SW_GEN1_3)	32	R/W	0000_0000h	<a href="#">37.5.207/3322</a>
2A4_003C	DIO Sync Wave Gen 4 Register 1 (IPU2_DIO_SW_GEN1_4)	32	R/W	0000_0000h	<a href="#">37.5.208/3324</a>
2A4_0040	DIO Sync Wave Gen 5 Register 1 (IPU2_DIO_SW_GEN1_5)	32	R/W	0000_0000h	<a href="#">37.5.209/3326</a>
2A4_0044	DIO Sync Wave Gen 6 Register 1 (IPU2_DIO_SW_GEN1_6)	32	R/W	0000_0000h	<a href="#">37.5.210/3328</a>
2A4_0048	DIO Sync Wave Gen 7 Register 1 (IPU2_DIO_SW_GEN1_7)	32	R/W	0000_0000h	<a href="#">37.5.211/3330</a>
2A4_004C	DIO Sync Wave Gen 8 Register 1 (IPU2_DIO_SW_GEN1_8)	32	R/W	0000_0000h	<a href="#">37.5.212/3332</a>
2A4_0050	DIO Sync Wave Gen 9 Register 1 (IPU2_DIO_SW_GEN1_9)	32	R/W	0000_0000h	<a href="#">37.5.213/3334</a>
2A4_0054	DIO Sync Assistance Gen Register (IPU2_DIO_SYNC_AS_GEN)	32	R/W	0000_0000h	<a href="#">37.5.214/3335</a>
2A4_0058	DIO Data Wave Gen <i> Register (IPU2_DIO_DW_GEN_i)	32	R/W	0000_0000h	<a href="#">37.5.215/3336</a>
2A4_0088	DIO Data Wave Set 0 <i> Register (IPU2_DIO_DW_SET0_i)	32	R/W	0000_0000h	<a href="#">37.5.216/3339</a>
2A4_00B8	DIO Data Wave Set 1 <i> Register (IPU2_DIO_DW_SET1_i)	32	R/W	0000_0000h	<a href="#">37.5.217/3339</a>
2A4_00E8	DIO Data Wave Set 2 <i> Register (IPU2_DIO_DW_SET2_i)	32	R/W	0000_0000h	<a href="#">37.5.218/3340</a>
2A4_0118	DIO Data Wave Set 3 <i> Register (IPU2_DIO_DW_SET3_i)	32	R/W	0000_0000h	<a href="#">37.5.219/3341</a>

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## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A4_0148	DIO Step Repeat <i>i</i> Registers (IPU2_DIO_STP_REP_<i>i</i>)	32	R/W	0000_0000h	<a href="#">37.5.220/3341</a>
2A4_0158	DIO Step Repeat 9 Registers (IPU2_DIO_STP_REP_9)	32	R/W	0000_0000h	<a href="#">37.5.221/3342</a>
2A4_015C	DIO Serial Display Control Register (IPU2_DIO_SER_CONF)	32	R/W	0000_0000h	<a href="#">37.5.222/3342</a>
2A4_0160	DIO Special Signals Control Register (IPU2_DIO_SSC)	32	R/W	0000_0000h	<a href="#">37.5.223/3345</a>
2A4_0164	DIO Polarity Register (IPU2_DIO_POL)	32	R/W	0000_0000h	<a href="#">37.5.224/3347</a>
2A4_0168	DIO Active Window 0 Register (IPU2_DIO_AW0)	32	R/W	0000_0000h	<a href="#">37.5.225/3348</a>
2A4_016C	DIO Active Window 1 Register (IPU2_DIO_AW1)	32	R/W	0000_0000h	<a href="#">37.5.226/3349</a>
2A4_0170	DIO Screen Configuration Register (IPU2_DIO_SCR_CONF)	32	R/W	0000_0000h	<a href="#">37.5.227/3350</a>
2A4_0174	DIO Status Register (IPU2_DIO_STAT)	32	R	0000_0005h	<a href="#">37.5.228/3351</a>
2A4_8000	DI1General Register (IPU2_DI1_GENERAL)	32	R/W	0020_0000h	<a href="#">37.5.229/3353</a>
2A4_8004	DI1 Base Sync Clock Gen 0 Register (IPU2_DI1_BS_CLKGEN0)	32	R/W	0000_0000h	<a href="#">37.5.230/3355</a>
2A4_8008	DI1 Base Sync Clock Gen 1 Register (IPU2_DI1_BS_CLKGEN1)	32	R/W	0000_0000h	<a href="#">37.5.231/3356</a>
2A4_800C	DI1 Sync Wave Gen 1 Register 0 (IPU2_DI1_SW_GEN0_1)	32	R/W	0000_0000h	<a href="#">37.5.232/3356</a>
2A4_8010	DI1 Sync Wave Gen 2 Register 0 (IPU2_DI1_SW_GEN0_2)	32	R/W	0000_0000h	<a href="#">37.5.233/3358</a>
2A4_8014	DI1 Sync Wave Gen 3 Register 0 (IPU2_DI1_SW_GEN0_3)	32	R/W	0000_0000h	<a href="#">37.5.234/3359</a>
2A4_8018	DI1 Sync Wave Gen 4 Register 0 (IPU2_DI1_SW_GEN0_4)	32	R/W	0000_0000h	<a href="#">37.5.235/3360</a>
2A4_801C	DI1 Sync Wave Gen 5 Register 0 (IPU2_DI1_SW_GEN0_5)	32	R/W	0000_0000h	<a href="#">37.5.236/3361</a>
2A4_8020	DI1 Sync Wave Gen 6 Register 0 (IPU2_DI1_SW_GEN0_6)	32	R/W	0000_0000h	<a href="#">37.5.237/3363</a>
2A4_8024	DI1 Sync Wave Gen 7 Register 0 (IPU2_DI1_SW_GEN0_7)	32	R/W	0000_0000h	<a href="#">37.5.238/3364</a>
2A4_8028	DI1 Sync Wave Gen 8 Register 0 (IPU2_DI1_SW_GEN0_8)	32	R/W	0000_0000h	<a href="#">37.5.239/3365</a>
2A4_802C	DI1Sync Wave Gen 9 Register 0 (IPU2_DI1_SW_GEN0_9)	32	R/W	0000_0000h	<a href="#">37.5.240/3366</a>
2A4_8030	DI1 Sync Wave Gen 1 Register 1 (IPU2_DI1_SW_GEN1_1)	32	R/W	0000_0000h	<a href="#">37.5.241/3368</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A4_8034	DI1 Sync Wave Gen 2 Register 1 (IPU2_DI1_SW_GEN1_2)	32	R/W	0000_0000h	<a href="#">37.5.242/3370</a>
2A4_8038	DI1 Sync Wave Gen 3 Register 1 (IPU2_DI1_SW_GEN1_3)	32	R/W	0000_0000h	<a href="#">37.5.243/3372</a>
2A4_803C	DI1 Sync Wave Gen 4 Register 1 (IPU2_DI1_SW_GEN1_4)	32	R/W	0000_0000h	<a href="#">37.5.244/3374</a>
2A4_8040	DI1 Sync Wave Gen 5 Register 1 (IPU2_DI1_SW_GEN1_5)	32	R/W	0000_0000h	<a href="#">37.5.245/3376</a>
2A4_8044	DI1 Sync Wave Gen 6 Register 1 (IPU2_DI1_SW_GEN1_6)	32	R/W	0000_0000h	<a href="#">37.5.246/3378</a>
2A4_8048	DI1 Sync Wave Gen 7 Register 1 (IPU2_DI1_SW_GEN1_7)	32	R/W	0000_0000h	<a href="#">37.5.247/3380</a>
2A4_804C	DI1 Sync Wave Gen 8 Register 1 (IPU2_DI1_SW_GEN1_8)	32	R/W	0000_0000h	<a href="#">37.5.248/3382</a>
2A4_8050	DI1 Sync Wave Gen 9 Register 1 (IPU2_DI1_SW_GEN1_9)	32	R/W	0000_0000h	<a href="#">37.5.249/3384</a>
2A4_8054	DI1 Sync Assistance Gen Register (IPU2_DI1_SYNC_AS_GEN)	32	R/W	0000_0000h	<a href="#">37.5.250/3385</a>
2A4_8058	DI1 Data Wave Gen <i> Register (IPU2_DI1_DW_GEN_i)	32	R/W	0000_0000h	<a href="#">37.5.251/3386</a>
2A4_8088	DI1 Data Wave Set 0 <i> Register (IPU2_DI1_DW_SET0_i)	32	R/W	0000_0000h	<a href="#">37.5.252/3389</a>
2A4_80B8	DI1 Data Wave Set 1 <i> Register (IPU2_DI1_DW_SET1_i)	32	R/W	0000_0000h	<a href="#">37.5.253/3389</a>
2A4_80E8	DI1 Data Wave Set 2 <i> Register (IPU2_DI1_DW_SET2_i)	32	R/W	0000_0000h	<a href="#">37.5.254/3390</a>
2A4_8118	DI1 Data Wave Set 3 <i> Register (IPU2_DI1_DW_SET3_i)	32	R/W	0000_0000h	<a href="#">37.5.255/3391</a>
2A4_8148	DI1 Step Repeat <i> Registers (IPU2_D1_STP REP_i)	32	R/W	0000_0000h	<a href="#">37.5.256/3391</a>
2A4_8158	DI1 Step Repeat 9 Registers (IPU2_DI1_STP REP_9)	32	R/W	0000_0000h	<a href="#">37.5.257/3392</a>
2A4_815C	DI1 Serial Display Control Register (IPU2_DI1_SER_CONF)	32	R/W	0000_0000h	<a href="#">37.5.258/3392</a>
2A4_8160	DI1 Special Signals Control Register (IPU2_DI1_SSC)	32	R/W	0000_0000h	<a href="#">37.5.259/3395</a>
2A4_8164	DI1 Polarity Register (IPU2_DI1_POL)	32	R/W	0000_0000h	<a href="#">37.5.260/3397</a>
2A4_8168	DI1 Active Window 0 Register (IPU2_DI1_AW0)	32	R/W	0000_0000h	<a href="#">37.5.261/3398</a>
2A4_816C	DI1 Active Window 1 Register (IPU2_DI1_AW1)	32	R/W	0000_0000h	<a href="#">37.5.262/3399</a>
2A4_8170	DI1 Screen Configuration Register (IPU2_DI1_SCR_CONF)	32	R/W	0000_0000h	<a href="#">37.5.263/3400</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A4_8174	DI1 Status Register (IPU2_DI1_STAT)	32	R	0000_0005h	<a href="#">37.5.264/3401</a>
2A5_0000	SMFC Mapping Register (IPU2_SMFC_MAP)	32	R/W	0000_0000h	<a href="#">37.5.265/3402</a>
2A5_0004	SMFC Watermark Control Register (IPU2_SMFC_WMC)	32	R/W	0000_09A6h	<a href="#">37.5.266/3403</a>
2A5_0008	SMFC Burst Size Register (IPU2_SMFC_BS)	32	R/W	0000_0000h	<a href="#">37.5.267/3405</a>
2A5_8000	DC Read Channel Configuration Register (IPU2_DC_READ_CH_CONF)	32	R/W	FFFF_0000h	<a href="#">37.5.268/3406</a>
2A5_8004	DC Read Channel Start Address Register (IPU2_DC_READ_SH_ADDR)	32	R/W	0000_0000h	<a href="#">37.5.269/3407</a>
2A5_8008	DC Routine Link Register 0 Channel 0 (IPU2_DC_RL0_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.270/3408</a>
2A5_800C	DC Routine Link Register 1 Channel 0 (IPU2_DC_RL1_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.271/3409</a>
2A5_8010	DC Routine Link Register2 Channel 0 (IPU2_DC_RL2_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.272/3410</a>
2A5_8014	DC Routine Link Registe3 Channel 0 (IPU2_DC_RL3_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.273/3411</a>
2A5_8018	DC Routine Link Register 4 Channel 0 (IPU2_DC_RL4_CH_0)	32	R/W	0000_0000h	<a href="#">37.5.274/3412</a>
2A5_801C	DC Write Channel 1 Configuration Register (IPU2_DC_WR_CH_CONF_1)	32	R/W	0000_0000h	<a href="#">37.5.275/3413</a>
2A5_8020	DC Write Channel 1 Address Configuration Register (IPU2_DC_WR_CH_ADDR_1)	32	R/W	0000_0000h	<a href="#">37.5.276/3414</a>
2A5_8024	DC Routine Link Register 0 Channel 1 (IPU2_DC_RL0_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.277/3415</a>
2A5_8028	DC Routine Link Register 1 Channel 1 (IPU2_DC_RL1_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.278/3416</a>
2A5_8030	DC Routine Link Register 2 Channel 1 (IPU2_DC_RL2_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.279/3417</a>
2A5_8032	DC Routine Link Register 3 Channel 1 (IPU2_DC_RL3_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.280/3418</a>
2A5_8034	DC Routine Link Register 4 Channel 1 (IPU2_DC_RL4_CH_1)	32	R/W	0000_0000h	<a href="#">37.5.281/3419</a>
2A5_8038	DC Write Channel 2 Configuration Register (IPU2_DC_WR_CH_CONF_2)	32	R/W	0000_0000h	<a href="#">37.5.282/3420</a>
2A5_803C	DC Write Channel 2 Address Configuration Register (IPU2_DC_WR_CH_ADDR_2)	32	R/W	0000_0000h	<a href="#">37.5.283/3421</a>
2A5_8040	DC Routine Link Register 0 Channel 2 (IPU2_DC_RL0_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.284/3422</a>
2A5_8044	DC Routine Link Register 1 Channel 2 (IPU2_DC_RL1_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.285/3423</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A5_8048	DC Routine Link Register 2 Channel 2 (IPU2_DC_RL2_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.286/3424</a>
2A5_804C	DC Routine Link Register 3 Channel 2 (IPU2_DC_RL3_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.287/3425</a>
2A5_8050	DC Routine Link Register 4 Channel 2 (IPU2_DC_RL4_CH_2)	32	R/W	0000_0000h	<a href="#">37.5.288/3426</a>
2A5_8054	DC Command Channel 3 Configuration Register (IPU2_DC_CMD_CH_CONF_3)	32	R/W	0000_0000h	<a href="#">37.5.289/3426</a>
2A5_8058	DC Command Channel 4 Configuration Register (IPU2_DC_CMD_CH_CONF_4)	32	R/W	0000_0000h	<a href="#">37.5.290/3427</a>
2A5_805C	DC Write Channel 5 Configuration Register (IPU2_DC_WR_CH_CONF_5)	32	R/W	0000_0000h	<a href="#">37.5.291/3428</a>
2A5_8060	DC Write Channel 5 Address Configuration Register (IPU2_DC_WR_CH_ADDR_5)	32	R/W	0000_0000h	<a href="#">37.5.292/3430</a>
2A5_8064	DC Routine Link Register 0 Channel 5 (IPU2_DC_RL0_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.293/3430</a>
2A5_8068	DC Routine Link Register 1 Channel 5 (IPU2_DC_RL1_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.294/3431</a>
2A5_806C	DC Routine Link Register 2 Channel 5 (IPU2_DC_RL2_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.295/3432</a>
2A5_8070	DC Routine Link Register 3 Channel 5 (IPU2_DC_RL3_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.296/3433</a>
2A5_8074	DC Routine Link Register 4 Channel 5 (IPU2_DC_RL4_CH_5)	32	R/W	0000_0000h	<a href="#">37.5.297/3434</a>
2A5_8078	DC Write Channel 6 Configuration Register (IPU2_DC_WR_CH_CONF_6)	32	R/W	0000_0000h	<a href="#">37.5.298/3435</a>
2A5_807C	DC Write Channel 6 Address Configuration Register (IPU2_DC_WR_CH_ADDR_6)	32	R/W	0000_0000h	<a href="#">37.5.299/3436</a>
2A5_8080	DC Routine Link Register 0 Channel 6 (IPU2_DC_RL0_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.300/3437</a>
2A5_8084	DC Routine Link Register 1 Channel 6 (IPU2_DC_RL1_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.301/3438</a>
2A5_8088	DC Routine Link Register 2 Channel 6 (IPU2_DC_RL2_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.302/3439</a>
2A5_808C	DC Routine Link Register 3 Channel 6 (IPU2_DC_RL3_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.303/3440</a>
2A5_8090	DC Routine Link Register 4 Channel 6 (IPU2_DC_RL4_CH_6)	32	R/W	0000_0000h	<a href="#">37.5.304/3441</a>
2A5_8094	DC Write Channel 8 Configuration 1 Register (IPU2_DC_WR_CH_CONF1_8)	32	R/W	0000_0000h	<a href="#">37.5.305/3442</a>
2A5_8098	DC Write Channel 8 Configuration 2 Register (IPU2_DC_WR_CH_CONF2_8)	32	R/W	0000_0000h	<a href="#">37.5.306/3443</a>
2A5_809C	DC Routine Link Register 1 Channel 8 (IPU2_DC_RL1_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.307/3443</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A5_80A0	DC Routine Link Register 2 Channel 8 (IPU2_DC_RL2_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.308/3444</a>
2A5_80A4	DC Routine Link Register 3 Channel 8 (IPU2_DC_RL3_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.309/3445</a>
2A5_80A8	DC Routine Link Register 4 Channel 8 (IPU2_DC_RL4_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.310/3445</a>
2A5_80AC	DC Routine Link Register 5 Channel 8 (IPU2_DC_RL5_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.311/3446</a>
2A5_80B0	DC Routine Link Register 6 Channel 8 (IPU2_DC_RL6_CH_8)	32	R/W	0000_0000h	<a href="#">37.5.312/3447</a>
2A5_80B4	DC Write Channel 9 Configuration 1 Register (IPU2_DC_WR_CH_CONF1_9)	32	R/W	0000_0000h	<a href="#">37.5.313/3447</a>
2A5_80B8	DC Write Channel 9 Configuration 2 Register (IPU2_DC_WR_CH_CONF2_9)	32	R/W	0000_0000h	<a href="#">37.5.314/3448</a>
2A5_80BC	DC Routine Link Register 1 Channel 9 (IPU2_DC_RL1_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.315/3449</a>
2A5_80C0	DC Routine Link Register 2 Channel 9 (IPU2_DC_RL2_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.316/3449</a>
2A5_80C4	DC Routine Link Register 3 Channel 9 (IPU2_DC_RL3_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.317/3450</a>
2A5_80C8	DC Routine Link Register 4 Channel 9 (IPU2_DC_RL4_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.318/3451</a>
2A5_80CC	DC Routine Link Register 5 Channel 9 (IPU2_DC_RL5_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.319/3452</a>
2A5_80D0	DC Routine Link Register 6 Channel 9 (IPU2_DC_RL6_CH_9)	32	R/W	0000_0000h	<a href="#">37.5.320/3452</a>
2A5_80D4	DC General Register (IPU2_DC_GEN)	32	R/W	0000_0060h	<a href="#">37.5.321/3453</a>
2A5_80D8	DC Display Configuration 1 Register 0 (IPU2_DC_DISP_CONF1_0)	32	R/W	0000_0042h	<a href="#">37.5.322/3455</a>
2A5_80DC	DC Display Configuration 1 Register 1 (IPU2_DC_DISP_CONF1_1)	32	R/W	0000_0042h	<a href="#">37.5.323/3456</a>
2A5_80E0	DC Display Configuration 1 Register 2 (IPU2_DC_DISP_CONF1_2)	32	R/W	0000_0042h	<a href="#">37.5.324/3458</a>
2A5_80E4	DC Display Configuration 1 Register 3 (IPU2_DC_DISP_CONF1_3)	32	R/W	0000_0042h	<a href="#">37.5.325/3459</a>
2A5_80E8	DC Display Configuration 2 Register 0 (IPU2_DC_DISP_CONF2_0)	32	R/W	0000_0000h	<a href="#">37.5.326/3460</a>
2A5_80EC	DC Display Configuration 2 Register 1 (IPU2_DC_DISP_CONF2_1)	32	R/W	0000_0000h	<a href="#">37.5.327/3461</a>
2A5_80F0	DC Display Configuration 2 Register 2 (IPU2_DC_DISP_CONF2_2)	32	R/W	0000_0000h	<a href="#">37.5.328/3461</a>
2A5_80F4	DC Display Configuration 2 Register 3 (IPU2_DC_DISP_CONF2_3)	32	R/W	0000_0000h	<a href="#">37.5.329/3461</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A5_80F8	DC DI0Configuration Register 1 (IPU2_DC_DI0_CONF_1)	32	R/W	0000_0000h	<a href="#">37.5.330/3462</a>
2A5_80FC	DC DI0Configuration Register 2 (IPU2_DC_DI0_CONF_2)	32	R/W	0000_0000h	<a href="#">37.5.331/3462</a>
2A5_8100	DC DI1Configuration Register 1 (IPU2_DC_DI1_CONF_1)	32	R/W	0000_0000h	<a href="#">37.5.332/3462</a>
2A5_8104	DC DI1Configuration Register 2 (IPU2_DC_DI1_CONF_2)	32	R/W	0000_0000h	<a href="#">37.5.333/3463</a>
2A5_8108	DC Mapping Configuration Register 0 (IPU2_DC_MAP_CONF_0)	32	R/W	0000_0000h	<a href="#">37.5.334/3463</a>
2A5_810C	DC Mapping Configuration Register 1 (IPU2_DC_MAP_CONF_1)	32	R/W	0000_0000h	<a href="#">37.5.335/3464</a>
2A5_8110	DC Mapping Configuration Register 2 (IPU2_DC_MAP_CONF_2)	32	R/W	0000_0000h	<a href="#">37.5.336/3465</a>
2A5_8114	DC Mapping Configuration Register 3 (IPU2_DC_MAP_CONF_3)	32	R/W	0000_0000h	<a href="#">37.5.337/3466</a>
2A5_8118	DC Mapping Configuration Register 4 (IPU2_DC_MAP_CONF_4)	32	R/W	0000_0000h	<a href="#">37.5.338/3467</a>
2A5_811C	DC Mapping Configuration Register 5 (IPU2_DC_MAP_CONF_5)	32	R/W	0000_0000h	<a href="#">37.5.339/3468</a>
2A5_8120	DC Mapping Configuration Register 6 (IPU2_DC_MAP_CONF_6)	32	R/W	0000_0000h	<a href="#">37.5.340/3469</a>
2A5_8124	DC Mapping Configuration Register 7 (IPU2_DC_MAP_CONF_7)	32	R/W	0000_0000h	<a href="#">37.5.341/3470</a>
2A5_8128	DC Mapping Configuration Register 8 (IPU2_DC_MAP_CONF_8)	32	R/W	0000_0000h	<a href="#">37.5.342/3471</a>
2A5_812C	DC Mapping Configuration Register 9 (IPU2_DC_MAP_CONF_9)	32	R/W	0000_0000h	<a href="#">37.5.343/3472</a>
2A5_8130	DC Mapping Configuration Register 10 (IPU2_DC_MAP_CONF_10)	32	R/W	0000_0000h	<a href="#">37.5.344/3473</a>
2A5_8134	DC Mapping Configuration Register 11 (IPU2_DC_MAP_CONF_11)	32	R/W	0000_0000h	<a href="#">37.5.345/3474</a>
2A5_8138	DC Mapping Configuration Register 12 (IPU2_DC_MAP_CONF_12)	32	R/W	0000_0000h	<a href="#">37.5.346/3475</a>
2A5_813C	DC Mapping Configuration Register 13 (IPU2_DC_MAP_CONF_13)	32	R/W	0000_0000h	<a href="#">37.5.347/3476</a>
2A5_8140	DC Mapping Configuration Register 14 (IPU2_DC_MAP_CONF_14)	32	R/W	0000_0000h	<a href="#">37.5.348/3477</a>
2A5_8144	DC Mapping Configuration Register 15 (IPU2_DC_MAP_CONF_15)	32	R/W	0000_0000h	<a href="#">37.5.349/3478</a>
2A5_8148	DC Mapping Configuration Register 16 (IPU2_DC_MAP_CONF_16)	32	R/W	0000_0000h	<a href="#">37.5.350/3478</a>
2A5_814C	DC Mapping Configuration Register 17 (IPU2_DC_MAP_CONF_17)	32	R/W	0000_0000h	<a href="#">37.5.351/3479</a>

Table continues on the next page...

## IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A5_8150	DC Mapping Configuration Register 18 (IPU2_DC_MAP_CONF_18)	32	R/W	0000_0000h	<a href="#">37.5.352/3480</a>
2A5_8154	DC Mapping Configuration Register 19 (IPU2_DC_MAP_CONF_19)	32	R/W	0000_0000h	<a href="#">37.5.353/3480</a>
2A5_8158	DC Mapping Configuration Register 20 (IPU2_DC_MAP_CONF_20)	32	R/W	0000_0000h	<a href="#">37.5.354/3481</a>
2A5_815C	DC Mapping Configuration Register 21 (IPU2_DC_MAP_CONF_21)	32	R/W	0000_0000h	<a href="#">37.5.355/3482</a>
2A5_8160	DC Mapping Configuration Register 22 (IPU2_DC_MAP_CONF_22)	32	R/W	0000_0000h	<a href="#">37.5.356/3482</a>
2A5_8164	DC Mapping Configuration Register 23 (IPU2_DC_MAP_CONF_23)	32	R/W	0000_0000h	<a href="#">37.5.357/3483</a>
2A5_8168	DC Mapping Configuration Register 24 (IPU2_DC_MAP_CONF_24)	32	R/W	0000_0000h	<a href="#">37.5.358/3484</a>
2A5_816C	DC Mapping Configuration Register 25 (IPU2_DC_MAP_CONF_25)	32	R/W	0000_0000h	<a href="#">37.5.359/3484</a>
2A5_8170	DC Mapping Configuration Register 26 (IPU2_DC_MAP_CONF_26)	32	R/W	0000_0000h	<a href="#">37.5.360/3485</a>
2A5_8174	DC User General Data Event 0 Register 0 (IPU2_DC_UGDE0_0)	32	R/W	0000_0000h	<a href="#">37.5.361/3486</a>
2A5_8178	DC User General Data Event 0 Register 1 (IPU2_DC_UGDE0_1)	32	R/W	0000_0000h	<a href="#">37.5.362/3487</a>
2A5_817C	DC User General Data Event 0 Register2 (IPU2_DC_UGDE0_2)	32	R/W	0000_0000h	<a href="#">37.5.363/3488</a>
2A5_8180	DC User General Data Event 0 Register 3 (IPU2_DC_UGDE0_3)	32	R/W	0000_0000h	<a href="#">37.5.364/3488</a>
2A5_8184	DC User General Data Event 1Register0 (IPU2_DC_UGDE1_0)	32	R/W	0000_0000h	<a href="#">37.5.365/3489</a>
2A5_8188	DC User General Data Event 1 Register 1 (IPU2_DC_UGDE1_1)	32	R/W	0000_0000h	<a href="#">37.5.366/3490</a>
2A5_818C	DC User General Data Event 1Register 2 (IPU2_DC_UGDE1_2)	32	R/W	0000_0000h	<a href="#">37.5.367/3491</a>
2A5_8190	DC User General Data Event 1Register 3 (IPU2_DC_UGDE1_3)	32	R/W	0000_0000h	<a href="#">37.5.368/3491</a>
2A5_8194	DC User General Data Event 2 Register 0 (IPU2_DC_UGDE2_0)	32	R/W	0000_0000h	<a href="#">37.5.369/3492</a>
2A5_8198	DC User General Data Event 2 Register 1 (IPU2_DC_UGDE2_1)	32	R/W	0000_0000h	<a href="#">37.5.370/3493</a>
2A5_819C	DC User General Data Event 2Register 2 (IPU2_DC_UGDE2_2)	32	R/W	0000_0000h	<a href="#">37.5.371/3494</a>
2A5_81A0	DC User General Data Event 2Register 3 (IPU2_DC_UGDE2_3)	32	R/W	0000_0000h	<a href="#">37.5.372/3494</a>
2A5_81A4	DC User General Data Event 3Register 0 (IPU2_DC_UGDE3_0)	32	R/W	0000_0000h	<a href="#">37.5.373/3495</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A5_81A8	DC User General Data Event 3Register 1 (IPU2_DC_UGDE3_1)	32	R/W	0000_0000h	<a href="#">37.5.374/3496</a>
2A5_81AC	DC User General Data Event 3Register 2 (IPU2_DC_UGDE3_2)	32	R/W	0000_0000h	<a href="#">37.5.375/3497</a>
2A5_81B0	DC User General Data Event 3Register 2 (IPU2_DC_UGDE3_3)	32	R/W	0000_0000h	<a href="#">37.5.376/3497</a>
2A5_81B4	DC Low Level Access Control Register 0 (IPU2_DC_LLA0)	32	R/W	0000_0000h	<a href="#">37.5.377/3497</a>
2A5_81B8	DC Low Level Access Control Register 1 (IPU2_DC_LLA1)	32	R/W	0000_0000h	<a href="#">37.5.378/3498</a>
2A5_81BC	DC Read Low Level Read Access Control Register 0 (IPU2_DC_R_LLA0)	32	R/W	0000_0000h	<a href="#">37.5.379/3498</a>
2A5_81C0	DC Read Low Level Read Access Control Register1 (IPU2_DC_R_LLA1)	32	R/W	0000_0000h	<a href="#">37.5.380/3499</a>
2A5_81C4	DC Write Channel 5 Configuration Register (IPU2_DC_WR_CH_ADDR_5_ALT)	32	R/W	0000_0000h	<a href="#">37.5.381/3499</a>
2A5_81C8	DC Status Register (IPU2_DC_STAT)	32	R	0000_00AAh	<a href="#">37.5.382/3501</a>
2A6_0000	DMFC Read Channel Register (IPU2_DMFC_RD_CHAN)	32	R/W	0000_0200h	<a href="#">37.5.383/3503</a>
2A6_0004	DMFC Write Channel Register (IPU2_DMFC_WR_CHAN)	32	R/W	0000_0000h	<a href="#">37.5.384/3505</a>
2A6_0008	DMFC Write Channel Definition Register (IPU2_DMFC_WR_CHAN_DEF)	32	R/W	2020_2020h	<a href="#">37.5.385/3508</a>
2A6_000C	DMFC Display Processor Channel Register (IPU2_DMFC_DP_CHAN)	32	R/W	0000_0000h	<a href="#">37.5.386/3510</a>
2A6_0010	DMFC Display Processor Channel Definition Register (IPU2_DMFC_DP_CHAN_DEF)	32	R/W	2020_2020h	<a href="#">37.5.387/3513</a>
2A6_0014	DMFC General 1 Register (IPU2_DMFC_GENERAL_1)	32	R/W	0000_0003h	<a href="#">37.5.388/3515</a>
2A6_0018	DMFC General 2 Register (IPU2_DMFC_GENERAL_2)	32	R/W	0000_0000h	<a href="#">37.5.389/3517</a>
2A6_001C	DMFC IC Interface Control Register (IPU2_DMFC_IC_CTRL)	32	R/W	0000_0002h	<a href="#">37.5.390/3518</a>
2A6_0020	DMFC Write Channel Alternate Register (IPU2_DMFC_WR_CHAN_ALT)	32	R/W	0000_0000h	<a href="#">37.5.391/3519</a>
2A6_0024	DMFC Write Channel Definition Alternate Register (IPU2_DMFC_WR_CHAN_DEF_ALT)	32	R/W	0000_2000h	<a href="#">37.5.392/3520</a>
2A6_0028	DMFC MFC Display Processor Channel Alternate Register (IPU2_DMFC_DP_CHAN_ALT)	32	R/W	0000_0000h	<a href="#">37.5.393/3521</a>
2A6_002C	DMFC Display Channel Definition Alternate Register (IPU2_DMFC_DP_CHAN_DEF_ALT)	32	R/W	2020_0020h	<a href="#">37.5.394/3524</a>
2A6_0030	DMFC General 1 Alternate Register (IPU2_DMFC_GENERAL1_ALT)	32	R/W	0000_0000h	<a href="#">37.5.395/3526</a>

Table continues on the next page...

**IPU memory map (continued)**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
2A6_0034	DMFC Status Register (IPU2_DMFC_STAT)	32	R	02FF_F000h	<a href="#">37.5.396/3528</a>
2A6_8000	VDI Field Size Register (IPU2_VDI_FSIZE)	32	R/W	0000_0000h	<a href="#">37.5.397/3529</a>
2A6_8004	VDI Control Register (IPU2_VDI_C)	32	R/W	0000_0000h	<a href="#">37.5.398/3530</a>
2A6_8008	VDI Control Register 2 (IPU2_VDI_C2_)	32	R/W	0000_0000h	<a href="#">37.5.399/3532</a>
2A6_800C	VDI Combining Parameters Register 1 (IPU2_VDI_CMDP_1)	32	R/W	0000_0000h	<a href="#">37.5.400/3533</a>
2A6_8010	VDI Combining Parameters Register 2 (IPU2_VDI_CMDP_2)	32	R/W	0000_0000h	<a href="#">37.5.401/3534</a>
2A6_8014	VDI Plane Size Register 1 (IPU2_VDI_PS_1)	32	R/W	0000_0000h	<a href="#">37.5.402/3534</a>
2A6_8018	VDI Plane Size Register 2 (IPU2_VDI_PS_2)	32	R/W	0000_0000h	<a href="#">37.5.403/3535</a>
2A6_801C	VDI Plane Size Register 3 (IPU2_VDI_PS_3)	32	R/W	0000_0000h	<a href="#">37.5.404/3536</a>
2A6_8020	VDI Plane Size Register 4 (IPU2_VDI_PS_4)	32	R/W	0000_0000h	<a href="#">37.5.405/3536</a>

### 37.5.1 Configuration Register (IPUx\_CONF)

Address: Base address + 0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	CSI_SEL	IC_INPUT	CSI1_DATA_SOURCE	CSI0_DATA_SOURCE	VDI_DMFC_SYNC	IC_DMFC_SYNC	IC_DMFC_SEL	0	0	IDMAC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0			VDI_EN	SISG_EN	DMFC_EN	DC_EN	SMFC_EN	D11_EN	D10_EN	DP_EN	0	IRT_EN	IC_EN	CSI1_EN	CSI0_EN
W												0				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_CONF field descriptions

Field	Description
31 CSI_SEL	CSI select bit; This bit selects manually between the 2 CSIs. This bit defines which CSI is the input to the IC. This bit is effective only if IC_INPUT is bit cleared  0 CSI0 is selected 1 CSI1 is selected
30 IC_INPUT	IC Input select bit. This bit selects manually between the 2 inputs to the IC  0 CSI0/1 is selected; In order to select between the CSIs use the CSI_SEL bit. 1 VDI
29 CSI1_DATA_SOURCE	CSI1 data Source  This bit selects what is the data source for the CSI1. This is a static mux that should not be changed while CSI1 is working. Data is handles differently if the source is MCT (MIPI) or parallel interface.  0 Parallel interface is connected to CSI1 1 MCT (MIPI) is connected to CSI1
28 CSI0_DATA_SOURCE	CSI0 data Source  This bit selects what is the data source for the CSI0. This is a static mux that should not be changed while CSI0 is working. Data is handles differently if the source is MCT (MIPI) or parallel interface.

Table continues on the next page...

## IPUx\_CONF field descriptions (continued)

Field	Description
	0 Parallel interface is connected to CSI0 1 MCT (MIPI) is connected to CSI0
27 VDI_DMFC_SYNC	This bit enables the direct path VDIC -> IC_VF -> DMFC for sync flow. If this bit is set IC_DMFC_SEL must be set. 0 the flow is disabled 1 the flow is enabled
26 IC_DMFC_SYNC	IC to DMFC Sync flow This bit defines if the direct flow between IC to DMFC is synchronous or asynchronous 0 async flow 1 Sync flow
25 IC_DMFC_SEL	IC to DMFC select Selects the DMAIC_1 (channel 21) channel's connectivity between the IC and the DMFC 0 DMAIC_1 (channel 21) is routed to the IDMAC 1 DMAIC_1 (channel 21) is routed to DMFC In case DMFC was selected the IDMAC_CH_EN[21] must be clear.
24 Reserved	This read-only field is reserved and always has the value 0.
23 Reserved	This read-only field is reserved and always has the value 0.
22 IDMAC_DISABLE	Image DMA controller (IDMAC) disable bit. This bit allows the user to turn off the clock of the IDMAC if the use case permits it. By default the IDMAC is enabled. 0 IDMAC is enabled 1 IDMAC is disabled
21 -	This field is reserved. Reserved.
20–16 -	This field is reserved. Reserved
15–13 Reserved	This read-only field is reserved and always has the value 0.
12 VDI_EN	VDI enable bit. This bit must be cleared if the ISP_EN bit is set. 0 VDIC is disabled 1 VDIC is enabled
11 SISG_EN	Still Image Synchronization Generator (SISG) Enable bit 0 SISG is disabled 1 SISG is enabled
10 DMFC_EN	Display's Multi FIFO Controller sub-block (DMFC) Enable bit 0 DMFC is disabled 1 DMFC is enabled
9 DC_EN	Display Controller sub-block (DC) Enable bit

Table continues on the next page...

**IPUx\_CONF field descriptions (continued)**

Field	Description
	0 DC is disabled 1 DC is enabled
8 SMFC_EN	Sensor's Multi FIFO Controller Sub-block (SMFC) Enable bit 0 SMFC is disabled 1 SMFC is enabled
7 DI1_EN	Display Interface Sub-block 1 Enable bit 0 DI1 is disabled 1 DI1 is enabled
6 DIO_EN	Display interface Sub-block 0 Enable bit 0 DIO is disabled 1 DIO is enabled
5 DP_EN	Display processor Sub-block Enable bit 0 DP is disabled 1 DP is enabled
4 Reserved	This read-only field is reserved and always has the value 0.
3 IRT_EN	Image Rotation Sub-Block Enable bit 0 IRT is disabled 1 IRT is enabled
2 IC_EN	Image Conversion Sub-Block Enable bit 0 IC is disabled 1 IC is enabled
1 CSI1_EN	Camera Sensor Interface 1 Enable bit 0 CSI1 is disabled 1 CSI1 is enabled
0 CSI0_EN	Camera Sensor Interface 0 Enable bit 0 CSI0 is disabled 1 CSI0 is enabled

## 37.5.2 SISG Control 0 Register (IPUx\_SISG\_CTRL0)

Address: Base address + 4h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																
W		EXT_ACTV	MCU_ACTV_I_TRIG														
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R																	
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

### IPUx\_SISG\_CTRL0 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30 EXT_ACTV	External Active Define if an external active trigger will start the counters. The external active trigger is an input signal to the IPU called ext_actv_trig
29 MCU_ACTV_I_TRIG	Reserved, should be cleared.
28–4 VAL_STOP_SISG_COUNTER	SISG Stop Counters value. This is a predefined value that stops the SISG counters. The user should write to this field the N-1 value of the desired value.
3–1 NO_VSYNC_2_STRT_CNT	VSYCs to Start Counter This bits define how many VSYNCs signals will be counter before activating the SISG counters. If set to 0 starts immediately. If set to N (1..7) starts after N VSYNCs.
0 VSYNC_RST_CNT	VSYNC Resets counters Defines if the counters are stopped following VSYNC or when the counters reach a pre defined value (VAL_STOP_SISG_COUNTER) 1 The counters are stopped at VSYNC 0 The counters are stopped when the counters reach the VAL_STOP_SISG_COUNTER value.

### 37.5.3 SISG Control 1 Register (IPUx\_SISG\_CTRL1)

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

IPUx\_SISG\_CTRL1 field descriptions

Field	Description
31–14 Reserved	This read-only field is reserved and always has the value 0.
13–8 SISG_OUT_POL	SISG_OUT_POL This bits defines the polarity of the SISG output signals 1 active high 0 active low
7–5 Reserved	This read-only field is reserved and always has the value 0.
SISG_STROBE_CNT	SISG Strobe Count The SISG can repeat the sequence for up to 32 cycles; this is used for generating a train of pulses.

### 37.5.4 SISG Set*<i>* Register (IPUx\_SISG\_SET\_i)

Address: Base address + Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

IPUx\_SISG\_SET\_i field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
SISG_SET_i	SISG SET <i> value These bits define the set value of the SISG counter #<i>

### 37.5.5 SISG Clear <i> Register (IPUx\_SISG\_CLR\_i)

Address: Base address + 24h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																																	
W																																	

Reset 0

#### IPUx\_SISG\_CLR\_i field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
SISG_CLEAR_i	SISG CLR <i> value These bits define the clear value of the SISG counter #<i>

### 37.5.6 Interrupt Control Register 1 (IPUx\_INT\_CTRL\_1)

This register contains part of IPU interrupts controls. The controls of EOF (end of frame) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 3Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_EOF_EN_31	0	IDMAC_EOF_EN_29	IDMAC_EOF_EN_28	IDMAC_EOF_EN_27	IDMAC_EOF_EN_26	IDMAC_EOF_EN_25	IDMAC_EOF_EN_24	IDMAC_EOF_EN_23	IDMAC_EOF_EN_22	IDMAC_EOF_EN_21	IDMAC_EOF_EN_20	IDMAC_EOF_EN_19	IDMAC_EOF_EN_18	IDMAC_EOF_EN_17	0
W																

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_EOF_EN_15	IDMAC_EOF_EN_14	IDMAC_EOF_EN_13	IDMAC_EOF_EN_12	IDMAC_EOF_EN_11	IDMAC_EOF_EN_10	IDMAC_EOF_EN_9	IDMAC_EOF_EN_8	0	0	0	0	IDMAC_EOF_EN_3	IDMAC_EOF_EN_2	IDMAC_EOF_EN_1	IDMAC_EOF_EN_0
W																

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

**IPUx\_INT\_CTRL\_1 field descriptions**

Field	Description
31 IDMAC_EOF_EN_31	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
30 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
29 IDMAC_EOF_EN_29	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
28 IDMAC_EOF_EN_28	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
27 IDMAC_EOF_EN_27	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
26 IDMAC_EOF_EN_26	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
25 IDMAC_EOF_EN_25	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
24 IDMAC_EOF_EN_24	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
23 IDMAC_EOF_EN_23	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
22 IDMAC_EOF_EN_22	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_1 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
21 IDMAC_EOF_EN_21	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
20 IDMAC_EOF_EN_20	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_EOF_EN_19	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
18 IDMAC_EOF_EN_18	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
17 IDMAC_EOF_EN_17	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
16 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
15 IDMAC_EOF_EN_15	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
14 IDMAC_EOF_EN_14	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
13 IDMAC_EOF_EN_13	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

Table continues on the next page...

**IPUx\_INT\_CTRL\_1 field descriptions (continued)**

Field	Description
12 IDMAC_EOF_EN_12	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
11 IDMAC_EOF_EN_11	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
10 IDMAC_EOF_EN_10	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
9 IDMAC_EOF_EN_9	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
8 IDMAC_EOF_EN_8	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
7–6 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
5 IDMAC_EOF_EN_5	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
4 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
3 IDMAC_EOF_EN_3	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
2 IDMAC_EOF_EN_2	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_1 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
1 IDMAC_EOF_EN_1	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
0 IDMAC_EOF_EN_0	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

**37.5.7 Interrupt Control Register 2 (IPUx\_INT\_CTRL\_2)**

This register contains part of IPU interrupts controls. The controls of EOF (end of frame) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 40h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W												IDMAC_EOF_EN_52	IDMAC_EOF_EN_51	IDMAC_EOF_EN_50	IDMAC_EOF_EN_49	IDMAC_EOF_EN_48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_EOF_EN_47	IDMAC_EOF_EN_46	IDMAC_EOF_EN_45	IDMAC_EOF_EN_44	IDMAC_EOF_EN_43	IDMAC_EOF_EN_42	IDMAC_EOF_EN_41	IDMAC_EOF_EN_40				0				
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_CTRL\_2 field descriptions**

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_2 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
20 IDMAC_EOF_EN_52	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_EOF_EN_51	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
18 IDMAC_EOF_EN_50	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
17 IDMAC_EOF_EN_49	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
16 IDMAC_EOF_EN_48	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
15 IDMAC_EOF_EN_47	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
14 IDMAC_EOF_EN_46	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
13 IDMAC_EOF_EN_45	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
12 IDMAC_EOF_EN_44	Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_2 field descriptions (continued)**

Field	Description
	<p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
11 IDMAC_EOF_ EN_43	<p>Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
10 IDMAC_EOF_ EN_42	<p>Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
9 IDMAC_EOF_ EN_41	<p>Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
8 IDMAC_EOF_ EN_40	<p>Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
7–2 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
1 IDMAC_EOF_ EN_33	<p>Enable End of Frame of Channel interrupt. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
0 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>

### 37.5.8 Interrupt Control Register 3 (IPUx\_INT\_CTRL\_3)

This register contains part of IPU interrupts controls. The controls of NFACK (New Frame Ack) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 44h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
R	IDMAC_NFACK_EN_31	0	IDMAC_NFACK_EN_29	IDMAC_NFACK_EN_28	IDMAC_NFACK_EN_27	IDMAC_NFACK_EN_26	IDMAC_NFACK_EN_25	IDMAC_NFACK_EN_24	IDMAC_NFACK_EN_23	IDMAC_NFACK_EN_22	IDMAC_NFACK_EN_21	IDMAC_NFACK_EN_20	IDMAC_NFACK_EN_19	IDMAC_NFACK_EN_18	IDMAC_NFACK_EN_17	0		
W																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R	IDMAC_NFACK_EN_15	IDMAC_NFACK_EN_14	IDMAC_NFACK_EN_13	IDMAC_NFACK_EN_12	IDMAC_NFACK_EN_11	IDMAC_NFACK_EN_10	IDMAC_NFACK_EN_9	IDMAC_NFACK_EN_8	0	0	0	0	IDMAC_NFACK_EN_5	0	IDMAC_NFACK_EN_3	IDMAC_NFACK_EN_2	IDMAC_NFACK_EN_1	IDMAC_NFACK_EN_0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_INT\_CTRL\_3 field descriptions

Field	Description
31 IDMAC_NFACK_EN_31	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
30 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
29 IDMAC_NFACK_EN_29	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
28 IDMAC_NFACK_EN_28	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_CTRL\_3 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
27 IDMAC_NFACK_EN_27	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
26 IDMAC_NFACK_EN_26	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
25 IDMAC_NFACK_EN_25	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
24 IDMAC_NFACK_EN_24	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
23 IDMAC_NFACK_EN_23	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
22 IDMAC_NFACK_EN_22	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
21 IDMAC_NFACK_EN_21	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
20 IDMAC_NFACK_EN_20	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_NFACK_EN_19	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_3 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
18 IDMAC_NFACK_ EN_18	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
17 IDMAC_NFACK_ EN_17	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
16 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
15 IDMAC_NFACK_ EN_15	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
14 IDMAC_NFACK_ EN_14	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
13 IDMAC_NFACK_ EN_13	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
12 IDMAC_NFACK_ EN_12	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
11 IDMAC_NFACK_ EN_11	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
10 IDMAC_NFACK_ EN_10	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_3 field descriptions (continued)**

Field	Description
9 IDMAC_NFACK_EN_9	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
8 IDMAC_NFACK_EN_8	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
7–6 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
5 IDMAC_NFACK_EN_5	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
4 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
3 IDMAC_NFACK_EN_3	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
2 IDMAC_NFACK_EN_2	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
1 IDMAC_NFACK_EN_1	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
0 IDMAC_NFACK_EN_0	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

### 37.5.9 Interrupt Control Register 4 (IPUx\_INT\_CTRL\_4)

This register contains part of IPU interrupts controls. The controls of NFACK (New Frame Ack) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 48h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_NFACK_EN_47	IDMAC_NFACK_EN_46	IDMAC_NFACK_EN_45	IDMAC_NFACK_EN_44	IDMAC_NFACK_EN_43	IDMAC_NFACK_EN_42	IDMAC_NFACK_EN_41	IDMAC_NFACK_EN_40				0				
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_CTRL\_4 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
20 IDMAC_NFACK_EN_52	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_NFACK_EN_51	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
18 IDMAC_NFACK_EN_50	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_CTRL\_4 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
17 IDMAC_NFACK_ EN_49	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
16 IDMAC_NFACK_ EN_48	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
15 IDMAC_NFACK_ EN_47	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
14 IDMAC_NFACK_ EN_46	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
13 IDMAC_NFACK_ EN_45	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
12 IDMAC_NFACK_ EN_44	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
11 IDMAC_NFACK_ EN_43	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
10 IDMAC_NFACK_ EN_42	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
9 IDMAC_NFACK_ EN_41	Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_4 field descriptions (continued)**

Field	Description
	<p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
8 IDMAC_NFACK_ EN_40	<p>Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
7–2 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
1 IDMAC_NFACK_ EN_33	<p>Enable New Frame Ack of Channel interrupt. This bit is the control of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
0 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>

### 37.5.10 Interrupt Control Register 5 (IPUx\_INT\_CTRL\_5)

This register contains part of IPU interrupts controls. The controls of the New-frame before end-of-frame indication (NFB4EOF) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 4Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_NFB4EOF_EN_31	0	IDMAC_NFB4EOF_EN_29	IDMAC_NFB4EOF_EN_28	IDMAC_NFB4EOF_EN_27	IDMAC_NFB4EOF_EN_26	IDMAC_NFB4EOF_EN_25	IDMAC_NFB4EOF_EN_24	IDMAC_NFB4EOF_EN_23	IDMAC_NFB4EOF_EN_22	IDMAC_NFB4EOF_EN_21	IDMAC_NFB4EOF_EN_20	IDMAC_NFB4EOF_EN_19	IDMAC_NFB4EOF_EN_18	IDMAC_NFB4EOF_EN_17	0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_NFB4EOF_EN_15	IDMAC_NFB4EOF_EN_14	IDMAC_NFB4EOF_EN_13	IDMAC_NFB4EOF_EN_12	IDMAC_NFB4EOF_EN_11	IDMAC_NFB4EOF_EN_10	IDMAC_NFB4EOF_EN_9	IDMAC_NFB4EOF_EN_8	0	0	0	0	0	0	0	0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_CTRL\_5 field descriptions

Field	Description
31 IDMAC_NFB4EOF_EN_31	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
30 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
29 IDMAC_NFB4EOF_EN_29	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.

Table continues on the next page...

**IPUx\_INT\_CTRL\_5 field descriptions (continued)**

Field	Description
28 IDMAC_ NFB4EOF_EN_ 28	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
27 IDMAC_ NFB4EOF_EN_ 27	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
26 IDMAC_ NFB4EOF_EN_ 26	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
25 IDMAC_ NFB4EOF_EN_ 25	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
24 IDMAC_ NFB4EOF_EN_ 24	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
23 IDMAC_ NFB4EOF_EN_ 23	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
22 IDMAC_ NFB4EOF_EN_ 22	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
21 IDMAC_ NFB4EOF_EN_ 21	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

Table continues on the next page...

**IPUx\_INT\_CTRL\_5 field descriptions (continued)**

Field	Description
20 IDMAC_ NFB4EOF_EN_20	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_ NFB4EOF_EN_19	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
18 IDMAC_ NFB4EOF_EN_18	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
17 IDMAC_ NFB4EOF_EN_17	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
16 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
15 IDMAC_ NFB4EOF_EN_15	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
14 IDMAC_ NFB4EOF_EN_14	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
13 IDMAC_ NFB4EOF_EN_13	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_5 field descriptions (continued)**

Field	Description
12 IDMAC_ NFB4EOF_EN_12	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
11 IDMAC_ NFB4EOF_EN_11	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
10 IDMAC_ NFB4EOF_EN_10	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
9 IDMAC_ NFB4EOF_EN_9	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
8 IDMAC_ NFB4EOF_EN_8	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
7–6 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
5 IDMAC_ NFB4EOF_EN_5	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
4 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
3 IDMAC_ NFB4EOF_EN_3	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_5 field descriptions (continued)**

Field	Description
	<p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
2 IDMAC_ NFB4EOF_EN_2	<p>New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
1 IDMAC_ NFB4EOF_EN_1	<p>New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
0 IDMAC_ NFB4EOF_EN_0	<p>New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>

### 37.5.11 Interrupt Control Register 6 (IPUx\_INT\_CTRL\_6)

This register contains part of IPU interrupts controls. The controls of the New-frame before end-of-frame indication (NFB4EOF\_ERR) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 50h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_NFB4EOF_EN_47	IDMAC_NFB4EOF_EN_46	IDMAC_NFB4EOF_EN_45	IDMAC_NFB4EOF_EN_44	IDMAC_NFB4EOF_EN_43	IDMAC_NFB4EOF_EN_42	IDMAC_NFB4EOF_EN_41	IDMAC_NFB4EOF_EN_40			0					
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_CTRL\_6 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
20 IDMAC_NFB4EOF_EN_52	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n.  n Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_NFB4EOF_EN_51	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n.  n Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.

Table continues on the next page...

**IPUx\_INT\_CTRL\_6 field descriptions (continued)**

Field	Description
18 IDMAC_ NFB4EOF_EN_ 50	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
17 IDMAC_ NFB4EOF_EN_ 49	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
16 IDMAC_ NFB4EOF_EN_ 48	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
15 IDMAC_ NFB4EOF_EN_ 47	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
14 IDMAC_ NFB4EOF_EN_ 46	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
13 IDMAC_ NFB4EOF_EN_ 45	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
12 IDMAC_ NFB4EOF_EN_ 44	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
11 IDMAC_ NFB4EOF_EN_ 43	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_6 field descriptions (continued)**

Field	Description
10 IDMAC_ NFB4EOF_EN_ 42	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
9 IDMAC_ NFB4EOF_EN_ 41	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
8 IDMAC_ NFB4EOF_EN_ 40	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
7–2 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
1 IDMAC_ NFB4EOF_EN_ 33	New Frame before end-of-frame error indication of Channel interrupt. This bit is the control of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
0 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.

### 37.5.12 Interrupt Control Register 7 (IPUx\_INT\_CTRL\_7)

This register contains part of IPUIPU interrupts controls. The controls of the End-of-Scroll indication (EOS) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 54h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_EOS_EN_31	0	IDMAC_EOS_EN_29	IDMAC_EOS_EN_28	IDMAC_EOS_EN_27	IDMAC_EOS_EN_26	IDMAC_EOS_EN_25	IDMAC_EOS_EN_24	IDMAC_EOS_EN_23	0	0	0	IDMAC_EOS_EN_19	0	0	0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_CTRL\_7 field descriptions

Field	Description
31 IDMAC_EOS_EN_31	End of Scroll indication of Channel interrupt. This bit is the control of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
30 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
29 IDMAC_EOS_EN_29	End of Scroll indication of Channel interrupt. This bit is the control of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
28 IDMAC_EOS_EN_28	End of Scroll indication of Channel interrupt. This bit is the control of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

Table continues on the next page...

**IPUx\_INT\_CTRL\_7 field descriptions (continued)**

Field	Description
27 IDMAC_EOS_EN_27	End of Scroll indication of Channel interrupt. This bit is the control of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
26 IDMAC_EOS_EN_26	End of Scroll indication of Channel interrupt. This bit is the control of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
25 IDMAC_EOS_EN_25	End of Scroll indication of Channel interrupt. This bit is the control of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
24 IDMAC_EOS_EN_24	End of Scroll indication of Channel interrupt. This bit is the control of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
23 IDMAC_EOS_EN_23	End of Scroll indication of Channel interrupt. This bit is the control of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
22–20 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_EOS_EN_19	End of Scroll indication of Channel interrupt. This bit is the control of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.

### 37.5.13 Interrupt Control Register 8 (IPUx\_INT\_CTRL\_8)

This register contains part of IPU interrupts controls. The controls of the End of Scroll indication (EOS) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 58h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0	IDMAC_EOS_EN_44	IDMAC_EOS_EN_43	IDMAC_EOS_EN_42	IDMAC_EOS_EN_41			0					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_CTRL\_8 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
20 IDMAC_EOS_EN_52	End of Scroll of Channel interrupt. This bit is the control of End Of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_EOS_EN_51	End of Scroll of Channel interrupt. This bit is the control of End Of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
18–13 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.

Table continues on the next page...

**IPUx\_INT\_CTRL\_8 field descriptions (continued)**

Field	Description
12 IDMAC_EOS_ EN_44	End of Scroll of Channel interrupt. This bit is the control of End Of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
11 IDMAC_EOS_ EN_43	End of Scroll of Channel interrupt. This bit is the control of End Of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
10 IDMAC_EOS_ EN_42	End of Scroll of Channel interrupt. This bit is the control of End Of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
9 IDMAC_EOS_ EN_41	End of Scroll of Channel interrupt. This bit is the control of End Of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
8–2 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
1 IDMAC_EOS_ EN_33	End of Scroll of Channel interrupt. This bit is the control of End Of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
0 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.

### 37.5.14 Interrupt Control Register 9 (IPUx\_INT\_CTRL\_9)

This register contains part of IPU interrupts controls. This register controls error interrupt signals coming from different sub-blocks within

Address: Base address + 5Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	CSI1_PUPE_EN	CSI0_PUPE_EN	0	IC_VF_BUFBUF_OVF_EN	IC_ENC_BUFBUF_OVF_EN	IC_BAYER_BUFBUF_OVF_EN										
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R								0								
W																VDL_FIFO1_OVF_EN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_CTRL\_9 field descriptions

Field	Description
31 CSI1_PUPE_EN	CSI1_PUPE_EN - CSI1 parameters update error interrupt enable. This bit enables an interrupt that is a result of an error generated by the CSI1. The error is generated in case where new frame arrived from the CSI1 before the completion of the CSI1's parameters update by the SRM 0 Interrupt is disabled. 1 Interrupt is enabled.
30 CSI0_PUPE_EN	CSI0_PUPE_EN - CSI0 parameters update error interrupt enable. This bit enables an interrupt that is a result of an error generated by the CSI0. The error is generated in case where new frame arrived from the CSI0 before the completion of the CSI0's parameters update by the SRM 0 Interrupt is disabled. 1 Interrupt is enabled.
29 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_INT\_CTRL\_9 field descriptions (continued)**

Field	Description
28 IC_VF_BUF_ OVF_EN	This bit enables an interrupt that is a result of the IC Buffer overflow for view finder coming from the IC. The user needs to write 1 to this bit in order to clear it.  0 Interrupt is disabled. 1 Interrupt is enabled.
27 IC_ENC_BUF_ OVF_EN	This bit enables an interrupt that is a result of the IC Buffer overflow for encoding coming from the IC. The user needs to write 1 to this bit in order to clear it.  0 Interrupt is disabled. 1 Interrupt is enabled.
26 IC_BAYER_ BUF_OVF_EN	This bit enables an interrupt that is a result of the IC Buffer overflow for bayer coming from the IC. The user needs to write 1 to this bit in order to clear it.  0 Interrupt is disabled. 1 Interrupt is enabled.
25–1 Reserved	This read-only field is reserved and always has the value 0.
0 VDI_FIFO1_ OVF_EN	FIFO1 overflow Interrupt1 Enable  The VDIC generates FIFO1 overflow interrupt1 when the write pointer of FIFO1 overruns read pointer.  0 Interrupt is disabled. 1 Interrupt is enabled.

### 37.5.15 Interrupt Control Register 10 (IPUx\_INT\_CTRL\_10)

This register contains part of IPU interrupts controls. This register controls error interrupt signals coming from different modules within

Address: Base address + 60h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	AXIR_ERR_EN	AXIW_ERR_EN	NON_PRIVILEGED_ACC_ERR_EN	0	IC_BAYER_FRM_LOST_ERR_EN	IC_ENC_FRM_LOST_ERR_EN	IC_VF_FRM_LOST_ERR_EN	0	D1_TIME_OUT_ERR_EN	D10_TIME_OUT_ERR_EN	D1_SYNC_DISP_ERR_EN	D10_SYNC_DISP_ERR_EN	DC_TEARING_ERR_6_EN	DC_TEARING_ERR_2_EN	DC_TEARING_ERR_1_EN
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_CTRL\_10 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30 AXIR_ERR_EN	This bit enables an interrupt that is a result of AXI read access resulted with error response. 0 Interrupt is disabled. 1 Interrupt is enabled.
29 AXIW_ERR_EN	This bit enables an interrupt that is a result of AXI write access resulted with error response. 0 Interrupt is disabled. 1 Interrupt is enabled.
28 NON_PRIVILEGED_ACC_ERR_EN	Non Privileged Access Error interrupt enable. The CPMEM and the DP can be accessed by the ARM platform in privileged mode only HPROT[1] =1. An attempt to access these regions in user mode will issue an interrupt. This bit enables the interrupt. 0 Interrupt is disabled. 1 Interrupt is enabled.

Table continues on the next page...

**IPUx\_INT\_CTRL\_10 field descriptions (continued)**

Field	Description
27 Reserved	This read-only field is reserved and always has the value 0.
26 IC_BAYER_ FRM_LOST_ ERR_EN	This bit enables an interrupt that is a result of IC's Bayer frame lost. 0 Interrupt is disabled. 1 Interrupt is enabled.
25 IC_ENC_FRM_ LOST_ERR_EN	This bit enables an interrupt that is a result of IC's encoding frame lost. 0 Interrupt is disabled. 1 Interrupt is enabled.
24 IC_VF_FRM_ LOST_ERR_EN	This bit enables an interrupt that is a result of IC's view finder frame lost. 0 Interrupt is disabled. 1 Interrupt is enabled.
23 Reserved	This read-only field is reserved and always has the value 0.
22 DI1_TIME_OUT_ ERR_EN	DI1 time out error interrupt enable This bit enables the interrupt that is a result of a time out error during a read access via DI1 0 Interrupt is disabled. 1 Interrupt is enabled.
21 DI0_TIME_OUT_ ERR_EN	DI0 time out error interrupt enable This bit enables the interrupt that is a result of a time out error during a read access via DI0 0 Interrupt is disabled. 1 Interrupt is enabled.
20 DI1_SYNC_ DISP_ERR_EN	DI1 Synchronous display error enable This bit enables the interrupt that is a result of an error during access to a synchronous display via DI1 0 Interrupt is disabled. 1 Interrupt is enabled.
19 DI0_SYNC_ DISP_ERR_EN	DI0 Synchronous display error enable This bit enables the interrupt that is a result of an error during access to a synchronous display via DI0 0 Interrupt is disabled. 1 Interrupt is enabled.
18 DC_TEARING_ ERR_6_EN	Tearing Error #6 enable This bit enables the interrupt that is a result of tearing error while the anti tearing mechanism is activated for DC channel 6 0 Interrupt is disabled. 1 Interrupt is enabled.
17 DC_TEARING_ ERR_2_EN	Tearing Error #2 enable This bit enables the interrupt that is a result of tearing error while the anti tearing mechanism is activated for DC channel 2

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_10 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
16 DC_TEARING_ERR_1_EN	Tearing Error #1 enable This bit enables the interrupt that is a result of tearing error while the anti tearing mechanism is activated for DC channel 1 0 Interrupt is disabled. 1 Interrupt is enabled.
15–4 Reserved	This read-only field is reserved and always has the value 0.
3 SMFC3_FRM_LOST_EN	Frame Lost of SMFC channel 3 interrupt enable bit This bit enables an interrupt that is a result of a Frame Lost of SMFC channel 3. 0 Interrupt is disabled. 1 Interrupt is enabled.
2 SMFC2_FRM_LOST_EN	Frame Lost of SMFC channel 2 interrupt enable bit This bit enables an interrupt that is a result of a Frame Lost of SMFC channel 2. 0 Interrupt is disabled. 1 Interrupt is enabled.
1 SMFC1_FRM_LOST_EN	Frame Lost of SMFC channel 1 interrupt enable bit This bit enables an interrupt that is a result of a Frame Lost of SMFC channel 1. 0 Interrupt is disabled. 1 Interrupt is enabled.
0 SMFC0_FRM_LOST_EN	Frame Lost of SMFC channel 0 interrupt enable bit This bit enables an interrupt that is a result of a Frame Lost of SMFC channel 0. 0 Interrupt is disabled. 1 Interrupt is enabled.

**37.5.16 Interrupt Control Register 11 (IPUx\_INT\_CTRL\_11)**

This register contains part of IPU interrupts controls. The controls of the end-of-band indication (EOBND) of DMA Channels interrupts [31:0] can be found in this register.

- Hide VDOA\_SYNC for all versions
- Show VDOA\_SYNC for IPUv3H version.
- The table below tagged with other settings (like IPU3M\_only) should be hidden in IPUv3H version.

Address: Base address + 64h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R				0		IDMAC_EOBND_EN_26			0		IDMAC_EOBND_EN_22		IDMAC_EOBND_EN_21		IDMAC_EOBND_EN_20		
W						IDMAC_EOBND_EN_25											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R				0	IDMAC_EOBND_EN_12		IDMAC_EOBND_EN_11			0		0	IDMAC_EOBND_EN_5		0		
W														IDMAC_EOBND_EN_3		IDMAC_EOBND_EN_2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_INT\_CTRL\_11 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
26 IDMAC_EOBND_EN_26	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
25 IDMAC_EOBND_EN_25	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
24–23 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
22 IDMAC_EOBND_EN_22	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
21 IDMAC_EOBND_EN_21	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_CTRL\_11 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
20 IDMAC_EOBND_EN_20	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
19–13 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
12 IDMAC_EOBND_EN_12	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
11 IDMAC_EOBND_EN_11	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
10–6 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
5 IDMAC_EOBND_EN_5	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
4 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
3 IDMAC_EOBND_EN_3	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
2 IDMAC_EOBND_EN_2	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
1 IDMAC_EOBND_EN_1	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_11 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
0 IDMAC_EOBND_EN_0	end-of-band indication of Channel interrupt. This bit is the control of end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

**37.5.17 Interrupt Control Register 12 (IPUx\_INT\_CTRL\_12)**

This register contains part of IPU interrupts controls. The controls of the end-of-band indication (EOBND) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 68h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_EOBND_EN_47	IDMAC_EOBND_EN_46	IDMAC_EOBND_EN_45						0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_CTRL\_12 field descriptions**

Field	Description
31–19 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
18 IDMAC_EOBND_EN_50	end-of-band indication of Channel interrupt. This bit is the control end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_CTRL\_12 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
17 IDMAC_EOBND_EN_49	end-of-band indication of Channel interrupt. This bit is the control end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
16 IDMAC_EOBND_EN_48	end-of-band indication of Channel interrupt. This bit is the control end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
15 IDMAC_EOBND_EN_47	end-of-band indication of Channel interrupt. This bit is the control end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
14 IDMAC_EOBND_EN_46	end-of-band indication of Channel interrupt. This bit is the control end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
13 IDMAC_EOBND_EN_45	end-of-band indication of Channel interrupt. This bit is the control end-of-band interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.

### 37.5.18 Interrupt Control Register 13 (IPUx\_INT\_CTRL\_13)

This register contains part of IPU interrupts controls. The controls of the threshold crossing indication (TH) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 6Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_TH_EN_31	0	IDMAC_TH_EN_29	IDMAC_TH_EN_28	IDMAC_TH_EN_27	IDMAC_TH_EN_26	IDMAC_TH_EN_25	IDMAC_TH_EN_24	IDMAC_TH_EN_23	IDMAC_TH_EN_22	IDMAC_TH_EN_21	IDMAC_TH_EN_20	IDMAC_TH_EN_19	IDMAC_TH_EN_18	IDMAC_TH_EN_17	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_TH_EN_15	IDMAC_TH_EN_14	IDMAC_TH_EN_13	IDMAC_TH_EN_12	IDMAC_TH_EN_11	IDMAC_TH_EN_10	IDMAC_TH_EN_9	IDMAC_TH_EN_8	0	0	0	0	IDMAC_TH_EN_3	IDMAC_TH_EN_2	IDMAC_TH_EN_1	IDMAC_TH_EN_0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IPUx\_INT\_CTRL\_13 field descriptions

Field	Description
31 IDMAC_TH_EN_31	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
30 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
29 IDMAC_TH_EN_29	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
28 IDMAC_TH_EN_28	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_CTRL\_13 field descriptions (continued)**

Field	Description
	<p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
27 IDMAC_TH_EN_27	<p>Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
26 IDMAC_TH_EN_26	<p>Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
25 IDMAC_TH_EN_25	<p>Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
24 IDMAC_TH_EN_24	<p>Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
23 IDMAC_TH_EN_23	<p>Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
22 IDMAC_TH_EN_22	<p>Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
21 IDMAC_TH_EN_21	<p>Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is disabled. 1 Interrupt is enabled.</p>
20 IDMAC_TH_EN_20	<p>Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p>

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_13 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_TH_EN_19	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
18 IDMAC_TH_EN_18	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
17 IDMAC_TH_EN_17	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
16 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
15 IDMAC_TH_EN_15	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
14 IDMAC_TH_EN_14	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
13 IDMAC_TH_EN_13	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
12 IDMAC_TH_EN_12	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

Table continues on the next page...

**IPUx\_INT\_CTRL\_13 field descriptions (continued)**

Field	Description
11 IDMAC_TH_EN_11	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
10 IDMAC_TH_EN_10	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
9 IDMAC_TH_EN_9	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
8 IDMAC_TH_EN_8	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
7–6 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
5 IDMAC_TH_EN_5	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
4 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
3 IDMAC_TH_EN_3	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
2 IDMAC_TH_EN_2	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_13 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
1 IDMAC_TH_EN_1	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
0 IDMAC_TH_EN_0	Threshold crossing indication of Channel interrupt. This bit is the control of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.

**37.5.19 Interrupt Control Register 14 (IPUx\_INT\_CTRL\_14)**

This register contains part of IPU interrupts controls. The controls of the Threshold crossing indication (TH) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 70h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W												IDMAC_TH_EN_52	IDMAC_TH_EN_51	IDMAC_TH_EN_50	IDMAC_TH_EN_49	IDMAC_TH_EN_48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_TH_EN_47	IDMAC_TH_EN_46	IDMAC_TH_EN_45	IDMAC_TH_EN_44	IDMAC_TH_EN_43	IDMAC_TH_EN_42	IDMAC_TH_EN_41	IDMAC_TH_EN_40				0				
W	0	0	0	0	0	0	0	0	0	0	0				IDMAC_TH_EN_33	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_CTRL\_14 field descriptions**

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
20 IDMAC_TH_EN_ 52	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
19 IDMAC_TH_EN_ 51	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
18 IDMAC_TH_EN_ 50	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
17 IDMAC_TH_EN_ 49	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
16 IDMAC_TH_EN_ 48	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
15 IDMAC_TH_EN_ 47	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
14 IDMAC_TH_EN_ 46	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.

Table continues on the next page...

**IPUx\_INT\_CTRL\_14 field descriptions (continued)**

Field	Description
13 IDMAC_TH_EN_ 45	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
12 IDMAC_TH_EN_ 44	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
11 IDMAC_TH_EN_ 43	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
10 IDMAC_TH_EN_ 42	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
9 IDMAC_TH_EN_ 41	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
8 IDMAC_TH_EN_ 40	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
7–2 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is disabled. 1 Interrupt is enabled.
1 IDMAC_TH_EN_ 33	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is disabled. 1 Interrupt is enabled.
0 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_INT\_CTRL\_14 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.

**37.5.20 Interrupt Control Register15 (IPUx\_INT\_CTRL\_15)**

This register contains part of IPU interrupts controls. The controls of general purpose interrupts can be found in this register.

Address: Base address + 74h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DI1_CNT_EN_PRE_8_EN	DI1_CNT_EN_PRE_3_EN	DI1_DISP_CLK_EN_PRE_EN	DIO_CNT_EN_PRE_10_EN	DIO_CNT_EN_PRE_9_EN	DIO_CNT_EN_PRE_8_EN	DIO_CNT_EN_PRE_7_EN	DIO_CNT_EN_PRE_6_EN	DIO_CNT_EN_PRE_5_EN	DIO_CNT_EN_PRE_4_EN	DIO_CNT_EN_PRE_3_EN	DIO_CNT_EN_PRE_2_EN	DIO_CNT_EN_PRE_1_EN	DIO_CNT_EN_PRE_0_EN	DC_DP_START_EN	
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DL_VSYNC_PRE_1_EN	DL_VSYNC_PRE_0_EN	DC_FC_6_EN	DC_FC_4_EN	DC_FC_3_EN	DC_FC_2_EN	DC_FC_1_EN	DC_FC_0_EN	DP ASF_BRAKE_EN	DP_SF_BRAKE_EN	DP ASF_END_EN	DP ASF_START_EN	DP_SF_END_EN	DP_SF_START_EN	SNOOPING2_INT_EN	SNOOPING1_INT_EN
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_INT\_CTRL\_15 field descriptions**

Field	Description
31 DI1_CNT_EN_PRE_8_EN	This bit enables the interrupt that is a result of a trigger generated by counter #8 of DI1  0 Interrupt is disabled. 1 Interrupt is enabled.
30 DI1_CNT_EN_PRE_3_EN	This bit enables the interrupt that is a result of a trigger generated by counter #3 of DI1  0 Interrupt is disabled. 1 Interrupt is enabled.
29 DI1_DISP_CLK_EN_PRE_EN	DI1_DISP_CLK_EN_PRE_EN

Table continues on the next page...

**IPUx\_INT\_CTRL\_15 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
28 DI0_CNT_EN_ PRE_10_EN	This bit enables the interrupt that is a result of a trigger generated by counter #10 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
27 DI0_CNT_EN_ PRE_9_EN	This bit enables the interrupt that is a result of a trigger generated by counter #9 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
26 DI0_CNT_EN_ PRE_8_EN	This bit enables the interrupt that is a result of a trigger generated by counter #8 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
25 DI0_CNT_EN_ PRE_7_EN	This bit enables the interrupt that is a result of a trigger generated by counter #7 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
24 DI0_CNT_EN_ PRE_6_EN	This bit enables the interrupt that is a result of a trigger generated by counter #6 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
23 DI0_CNT_EN_ PRE_5_EN	This bit enables the interrupt that is a result of a trigger generated by counter #5 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
22 DI0_CNT_EN_ PRE_4_EN	This bit enables the interrupt that is a result of a trigger generated by counter #4 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
21 DI0_CNT_EN_ PRE_3_EN	This bit enables the interrupt that is a result of a trigger generated by counter #3 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
20 DI0_CNT_EN_ PRE_2_EN	This bit enables the interrupt that is a result of a trigger generated by counter #2 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
19 DI0_CNT_EN_ PRE_1_EN	This bit enables the interrupt that is a result of a trigger generated by counter #1 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
18 DI0_CNT_EN_ PRE_0_EN	This bit enables the interrupt that is a result of a trigger generated by counter #0 of DIO 0 Interrupt is disabled. 1 Interrupt is enabled.
17 DC_ASYNC_ STOP_EN	This bit enables the interrupt asserted anytime the DP stops an async flow and moves to a sync flow

*Table continues on the next page...*

**IPUx\_INT\_CTRL\_15 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
16 DC_DP_START_EN	This bit enables the interrupt asserted anytime the DP start a new sync or async flow or when an async flow is interrupted by a sync flow 0 Interrupt is disabled. 1 Interrupt is enabled.
15 DI_VSYNC_PRE_1_EN	This bit enables the DI1 interrupt indicating of a VSYNC signal asserted 2 rows before the VSYNC sent to the display 0 Interrupt is disabled. 1 Interrupt is enabled.
14 DI_VSYNC_PRE_0_EN	This bit enables the DI0 interrupt indicating of a VSYNC signal asserted 2 rows before the VSYNC sent to the display 0 Interrupt is disabled. 1 Interrupt is enabled.
13 DC_FC_6_EN	This bit enables the DC Frame Complete on channel #6 interrupt 0 Interrupt is disabled. 1 Interrupt is enabled.
12 DC_FC_4_EN	This bit enables the DC Frame Complete on channel #4 interrupt 0 Interrupt is disabled. 1 Interrupt is enabled.
11 DC_FC_3_EN	This bit enables the DC Frame Complete on channel #3 interrupt 0 Interrupt is disabled. 1 Interrupt is enabled.
10 DC_FC_2_EN	This bit enables the DC Frame Complete on channel #2 interrupt 0 Interrupt is disabled. 1 Interrupt is enabled.
9 DC_FC_1_EN	This bit enables they'd Frame Complete on channel #1 interrupt 0 Interrupt is disabled. 1 Interrupt is enabled.
8 DC_FC_0_EN	This bit enables they'd Frame Complete on channel #0 interrupt 0 Interrupt is disabled. 1 Interrupt is enabled.
7 DP ASF BRAKE_EN	DP Async Flow Brake enable bit. This bit enables the interrupt that is a result of the async flow brake at the DP 0 Interrupt is disabled. 1 Interrupt is enabled.
6 DP_SF_BRAKE_EN	DP Sync Flow Brake enable bit. This bit enables the interrupt that is a result of the Sync flow brake at the DP

Table continues on the next page...

**IPUx\_INT\_CTRL\_15 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
5 DP ASF-END_EN	DP Async Flow End enable bit. This bit enables the interrupt that is a result of the Async flow end at the DP 0 Interrupt is disabled. 1 Interrupt is enabled.
4 DP ASF-START_EN	DP Async Flow Start enable bit. This bit enables the interrupt that is a result of the Async flow start at the DP 0 Interrupt is disabled. 1 Interrupt is enabled.
3 DP_SF_END_EN	DP Sync Flow End enable bit. This bit enables the interrupt that is a result of the Sync flow end at the DP 0 Interrupt is disabled. 1 Interrupt is enabled.
2 DP_SF_START_EN	DP Sync Flow Start enable bit. This bit enables the interrupt that is a result of the Sync flow start at the DP 0 Interrupt is disabled. 1 Interrupt is enabled.
1 SNOOPING2_INT_EN	IPU snooping 2 interrupt enable bit. This bit enables the interrupt that is a result of the detection of a snooping 2 signal assertion coming to the IPU 0 Interrupt is disabled. 1 Interrupt is enabled.
0 SNOOPING1_INT_EN	IPU snooping 1 interrupt enable bit. This bit enables the interrupt that is a result of the detection of a snooping 1 signal assertion coming to the IPU 0 Interrupt is disabled. 1 Interrupt is enabled.

### 37.5.21 SDMA Event Control Register 1 (IPUx\_SDMA\_EVENT\_1)

This register contains part of IPU SDMA events controls. The controls of EOF (end of frame) of DMA Channels SDMA events [31:0] can be found in this register.

Address: Base address + 78h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_EOF_SDMA_EN_31	0	IDMAC_EOF_SDMA_EN_29	IDMAC_EOF_SDMA_EN_28	IDMAC_EOF_SDMA_EN_27	IDMAC_EOF_SDMA_EN_26	IDMAC_EOF_SDMA_EN_25	IDMAC_EOF_SDMA_EN_24	IDMAC_EOF_SDMA_EN_23	IDMAC_EOF_SDMA_EN_22	IDMAC_EOF_SDMA_EN_21	IDMAC_EOF_SDMA_EN_20	IDMAC_EOF_SDMA_EN_19	IDMAC_EOF_SDMA_EN_18	IDMAC_EOF_SDMA_EN_17	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_EOF_SDMA_EN_15	IDMAC_EOF_SDMA_EN_14	IDMAC_EOF_SDMA_EN_13	IDMAC_EOF_SDMA_EN_12	IDMAC_EOF_SDMA_EN_11	IDMAC_EOF_SDMA_EN_10	IDMAC_EOF_SDMA_EN_9	IDMAC_EOF_SDMA_EN_8	0		IDMAC_EOF_SDMA_EN_5	0	IDMAC_EOF_SDMA_EN_3	IDMAC_EOF_SDMA_EN_2	IDMAC_EOF_SDMA_EN_1	IDMAC_EOF_SDMA_EN_0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_SDMA\_EVENT\_1 field descriptions

Field	Description
31 IDMAC_EOF_SDMA_EN_31	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
30 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
29 IDMAC_EOF_SDMA_EN_29	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
28 IDMAC_EOF_SDMA_EN_28	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_1 field descriptions (continued)**

Field	Description
	0 SDMA event is disabled. 1 SDMA event is enabled.
27 IDMAC_EOF_SDMA_EN_27	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
26 IDMAC_EOF_SDMA_EN_26	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
25 IDMAC_EOF_SDMA_EN_25	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
24 IDMAC_EOF_SDMA_EN_24	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
23 IDMAC_EOF_SDMA_EN_23	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
22 IDMAC_EOF_SDMA_EN_22	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
21 IDMAC_EOF_SDMA_EN_21	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
20 IDMAC_EOF_SDMA_EN_20	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
19 IDMAC_EOF_SDMA_EN_19	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_SDMA\_EVENT\_1 field descriptions (continued)**

Field	Description
	0 SDMA event is disabled. 1 SDMA event is enabled.
18 IDMAC_EOF_SDMA_EN_18	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
17 IDMAC_EOF_SDMA_EN_17	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
16 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
15 IDMAC_EOF_SDMA_EN_15	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
14 IDMAC_EOF_SDMA_EN_14	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
13 IDMAC_EOF_SDMA_EN_13	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
12 IDMAC_EOF_SDMA_EN_12	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
11 IDMAC_EOF_SDMA_EN_11	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
10 IDMAC_EOF_SDMA_EN_10	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_1 field descriptions (continued)**

Field	Description
9 IDMAC_EOF_SDMA_EN_9	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
8 IDMAC_EOF_SDMA_EN_8	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
7–6 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
5 IDMAC_EOF_SDMA_EN_5	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
4 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
3 IDMAC_EOF_SDMA_EN_3	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
2 IDMAC_EOF_SDMA_EN_2	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
1 IDMAC_EOF_SDMA_EN_1	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
0 IDMAC_EOF_SDMA_EN_0	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.

### 37.5.22 SDMA Event Control Register 2 (IPUx\_SDMA\_EVENT\_2)

This register contains part of IPU SDMA events controls. The controls of EOF (end of frame) of DMA Channels SDMA events [63:32] can be found in this register.

Address: Base address + 7Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W												IDMAC_EOF_SDMA_EN_52	IDMAC_EOF_SDMA_EN_51	IDMAC_EOF_SDMA_EN_50	IDMAC_EOF_SDMA_EN_49	IDMAC_EOF_SDMA_EN_48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_EOF_SDMA_EN_47	IDMAC_EOF_SDMA_EN_46	IDMAC_EOF_SDMA_EN_45	IDMAC_EOF_SDMA_EN_44	IDMAC_EOF_SDMA_EN_43	IDMAC_EOF_SDMA_EN_42	IDMAC_EOF_SDMA_EN_41	IDMAC_EOF_SDMA_EN_40			0					
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_SDMA\_EVENT\_2 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
20 IDMAC_EOF_SDMA_EN_52	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n.  n Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
19 IDMAC_EOF_SDMA_EN_51	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n.  n Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
18 IDMAC_EOF_SDMA_EN_50	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n.  n Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_2 field descriptions (continued)**

Field	Description
	0 SDMA event is disabled. 1 SDMA event is enabled.
17 IDMAC_EOF_SDMA_EN_49	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
16 IDMAC_EOF_SDMA_EN_48	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
15 IDMAC_EOF_SDMA_EN_47	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
14 IDMAC_EOF_SDMA_EN_46	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
13 IDMAC_EOF_SDMA_EN_45	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
12 IDMAC_EOF_SDMA_EN_44	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
11 IDMAC_EOF_SDMA_EN_43	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
10 IDMAC_EOF_SDMA_EN_42	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
9 IDMAC_EOF_SDMA_EN_41	Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_SDMA\_EVENT\_2 field descriptions (continued)**

Field	Description
	<p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
8 IDMAC_EOF_ SDMA_EN_40	<p>Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
7–2 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
1 IDMAC_EOF_ SDMA_EN_33	<p>Enable End of Frame of Channel SDMA event. This bit is the control of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
0 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>

### 37.5.23 SDMA Event Control Register 3 (IPUx\_SDMA\_EVENT\_3)

This register contains part of IPU SDMA events controls. The controls of NFACK (New Frame Acknowledge) of DMA Channels SDMA events [31:0] can be found in this register.

Address: Base address + 80h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_NFACK_SDMA_EN_31	0	IDMAC_NFACK_SDMA_EN_29	IDMAC_NFACK_SDMA_EN_28	IDMAC_NFACK_SDMA_EN_27	IDMAC_NFACK_SDMA_EN_26	IDMAC_NFACK_SDMA_EN_25	IDMAC_NFACK_SDMA_EN_24	IDMAC_NFACK_SDMA_EN_23	IDMAC_NFACK_SDMA_EN_22	IDMAC_NFACK_SDMA_EN_21	IDMAC_NFACK_SDMA_EN_20	IDMAC_NFACK_SDMA_EN_19	IDMAC_NFACK_SDMA_EN_18	IDMAC_NFACK_SDMA_EN_17	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_NFACK_SDMA_EN_15	IDMAC_NFACK_SDMA_EN_14	IDMAC_NFACK_SDMA_EN_13	IDMAC_NFACK_SDMA_EN_12	IDMAC_NFACK_SDMA_EN_11	IDMAC_NFACK_SDMA_EN_10	IDMAC_NFACK_SDMA_EN_9	IDMAC_NFACK_SDMA_EN_8	0	0	5	4	3	2	1	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_SDMA\_EVENT\_3 field descriptions

Field	Description
31 IDMAC_NFACK_SDMA_EN_31	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
30 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
29 IDMAC_NFACK_SDMA_EN_29	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_3 field descriptions (continued)**

Field	Description
28 IDMAC_NFACK_SDMA_EN_28	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
27 IDMAC_NFACK_SDMA_EN_27	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
26 IDMAC_NFACK_SDMA_EN_26	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
25 IDMAC_NFACK_SDMA_EN_25	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
24 IDMAC_NFACK_SDMA_EN_24	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
23 IDMAC_NFACK_SDMA_EN_23	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
22 IDMAC_NFACK_SDMA_EN_22	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
21 IDMAC_NFACK_SDMA_EN_21	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_3 field descriptions (continued)**

Field	Description
20 IDMAC_NFACK_SDMA_EN_20	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
19 IDMAC_NFACK_SDMA_EN_19	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
18 IDMAC_NFACK_SDMA_EN_18	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
17 IDMAC_NFACK_SDMA_EN_17	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
16 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
15 IDMAC_NFACK_SDMA_EN_15	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
14 IDMAC_NFACK_SDMA_EN_14	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
13 IDMAC_NFACK_SDMA_EN_13	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.

*Table continues on the next page...*

**IPUx\_SDMA\_EVENT\_3 field descriptions (continued)**

Field	Description
12 IDMAC_NFACK_SDMA_EN_12	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
11 IDMAC_NFACK_SDMA_EN_11	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
10 IDMAC_NFACK_SDMA_EN_10	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
9 IDMAC_NFACK_SDMA_EN_9	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
8 IDMAC_NFACK_SDMA_EN_8	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
7–6 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
5 IDMAC_NFACK_SDMA_EN_5	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
4 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
3 IDMAC_NFACK_SDMA_EN_3	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_SDMA\_EVENT\_3 field descriptions (continued)**

Field	Description
	<p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
2 IDMAC_NFACK_ SDMA_EN_2	<p>Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
1 IDMAC_NFACK_ SDMA_EN_1	<p>Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
0 IDMAC_NFACK_ SDMA_EN_0	<p>Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>

### 37.5.24 SDMA Event Control Register 4 (IPUx\_SDMA\_EVENT\_4)

This register contains part of IPU SDMA events controls. The controls of NFACK (New Frame Acknowledge) of DMA Channels SDMA events [63:32] can be found in this register.

Address: Base address + 84h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_NFACK_SDMA_EN_47	IDMAC_NFACK_SDMA_EN_46	IDMAC_NFACK_SDMA_EN_45	IDMAC_NFACK_SDMA_EN_44	IDMAC_NFACK_SDMA_EN_43	IDMAC_NFACK_SDMA_EN_42	IDMAC_NFACK_SDMA_EN_41	IDMAC_NFACK_SDMA_EN_40				0				
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_SDMA\_EVENT\_4 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
20 IDMAC_NFACK_SDMA_EN_52	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
19 IDMAC_NFACK_SDMA_EN_51	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_4 field descriptions (continued)**

Field	Description
18 IDMAC_NFACK_SDMA_EN_50	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
17 IDMAC_NFACK_SDMA_EN_49	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
16 IDMAC_NFACK_SDMA_EN_48	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
15 IDMAC_NFACK_SDMA_EN_47	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
14 IDMAC_NFACK_SDMA_EN_46	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
13 IDMAC_NFACK_SDMA_EN_45	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
12 IDMAC_NFACK_SDMA_EN_44	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
11 IDMAC_NFACK_SDMA_EN_43	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_4 field descriptions (continued)**

Field	Description
10 IDMAC_NFACK_ SDMA_EN_42	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
9 IDMAC_NFACK_ SDMA_EN_41	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
8 IDMAC_NFACK_ SDMA_EN_40	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
7–2 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
1 IDMAC_NFACK_ SDMA_EN_33	Enable New Frame Acknowledge of Channel SDMA event. This bit is the control of New Frame Acknowledge of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
0 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.

### 37.5.25 SDMA Event Control Register 7 (IPUx\_SDMA\_EVENT\_7)

This register contains part of IPU SDMA events controls. The controls of EOS (End of Scroll) of DMA Channels SDMA events [31:0] can be found in this register.

Address: Base address + 88h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_EOS_SDMA_EN_31	0	IDMAC_EOS_SDMA_EN_29	IDMAC_EOS_SDMA_EN_28	IDMAC_EOS_SDMA_EN_27	IDMAC_EOS_SDMA_EN_26	IDMAC_EOS_SDMA_EN_25	IDMAC_EOS_SDMA_EN_24	IDMAC_EOS_SDMA_EN_23	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_SDMA\_EVENT\_7 field descriptions

Field	Description
31 IDMAC_EOS_SDMA_EN_31	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
30 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
29 IDMAC_EOS_SDMA_EN_29	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
28 IDMAC_EOS_SDMA_EN_28	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_7 field descriptions (continued)**

Field	Description
	0 SDMA event is disabled. 1 SDMA event is enabled.
27 IDMAC_EOS_ SDMA_EN_27	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
26 IDMAC_EOS_ SDMA_EN_26	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
25 IDMAC_EOS_ SDMA_EN_25	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
24 IDMAC_EOS_ SDMA_EN_24	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
23 IDMAC_EOS_ SDMA_EN_23	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
22–20 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
19 IDMAC_EOS_ SDMA_EN_19	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.

### 37.5.26 SDMA Event Control Register 8 (IPUx\_SDMA\_EVENT\_8)

This register contains part of IPU SDMA events controls. The controls of EOS (End of Scroll) of DMA Channels SDMA events [63:32] can be found in this register.

Address: Base address + 8Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W												IDMAC_EOS_SDMA_EN_52	IDMAC_EOS_SDMA_EN_51	0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0	IDMAC_EOS_SDMA_EN_44	IDMAC_EOS_SDMA_EN_43	IDMAC_EOS_SDMA_EN_42	IDMAC_EOS_SDMA_EN_41			0					
W														IDMAC_EOS_SDMA_EN_33	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_SDMA\_EVENT\_8 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
20 IDMAC_EOS_SDMA_EN_52	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
19 IDMAC_EOS_SDMA_EN_51	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
18–13 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_8 field descriptions (continued)**

Field	Description
12 IDMAC_EOS_SDMA_EN_44	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
11 IDMAC_EOS_SDMA_EN_43	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
10 IDMAC_EOS_SDMA_EN_42	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
9 IDMAC_EOS_SDMA_EN_41	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
8–2 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
1 IDMAC_EOS_SDMA_EN_33	Enable End of Scroll of Channel SDMA event. This bit is the control of End Of Scroll of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
0 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.

### 37.5.27 SDMA Event Control Register 11 (IPUx\_SDMA\_EVENT\_11)

This register contains part of IPU SDMA events controls. The controls of EOBND (End of Band) of DMA Channels SDMA events [31:0] can be found in this register.

- Hide VDOA\_SYNC for all versions
- Show VDOA\_SYNC for IPUv3H version.
- The table below tagged with other settings (like IPU3M\_only) should be hidden in IPUv3H version.

Address: Base address + 90h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R						IDMAC_EOBND_SDMA_EN_26			0							0
W						IDMAC_EOBND_SDMA_EN_25										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				IDMAC_EOBND_SDMA_EN_12		IDMAC_EOBND_SDMA_EN_11			0			0				
W										IDMAC_EOBND_SDMA_EN_5		0				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_SDMA\_EVENT\_11 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
26 IDMAC_EOBND_SDMA_EN_26	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
25 IDMAC_EOBND_SDMA_EN_25	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
24–23 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
22 IDMAC_EOBND_SDMA_EN_22	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
21 IDMAC_EOBND_SDMA_EN_21	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_11 field descriptions (continued)**

Field	Description
	<p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
20 IDMAC_EOBND_SDMA_EN_20	<p>Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
19–13 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
12 IDMAC_EOBND_SDMA_EN_12	<p>Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
11 IDMAC_EOBND_SDMA_EN_11	<p>Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
10–6 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
5 IDMAC_EOBND_SDMA_EN_5	<p>Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
4 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
3 IDMAC_EOBND_SDMA_EN_3	<p>Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
2 IDMAC_EOBND_SDMA_EN_2	<p>Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
1 IDMAC_EOBND_SDMA_EN_1	<p>Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p>

*Table continues on the next page...*

**IPUx\_SDMA\_EVENT\_11 field descriptions (continued)**

Field	Description
	0 SDMA event is disabled. 1 SDMA event is enabled.
0 IDMAC_EOBND_SDMA_EN_0	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.

### 37.5.28 SDMA Event Control Register 12 (IPUx\_SDMA\_EVENT\_12)

This register contains part of IPU SDMA events controls. The controls of EOBND (End of Band) of DMA Channels SDMA events [63:32] can be found in this register.

Address: Base address + 94h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_EOBND_SDMA_EN_47	IDMAC_EOBND_SDMA_EN_46	IDMAC_EOBND_SDMA_EN_45						0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_SDMA\_EVENT\_12 field descriptions**

Field	Description
31–19 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_12 field descriptions (continued)**

Field	Description
18 IDMAC_EOBND_SDMA_EN_50	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
17 IDMAC_EOBND_SDMA_EN_49	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
16 IDMAC_EOBND_SDMA_EN_48	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
15 IDMAC_EOBND_SDMA_EN_47	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
14 IDMAC_EOBND_SDMA_EN_46	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
13 IDMAC_EOBND_SDMA_EN_45	Enable End of Band of Channel SDMA event. This bit is the control of End Of Band of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.

### 37.5.29 SDMA Event Control Register 13 (IPUx\_SDMA\_EVENT\_13)

This register contains part of IPU SDMA events controls. The controls of TH (Threshold) of DMA Channels SDMA events [31:0] can be found in this register.

Address: Base address + 98h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_TH_SDMA_EN_31	0	IDMAC_TH_SDMA_EN_29	IDMAC_TH_SDMA_EN_28	IDMAC_TH_SDMA_EN_27	IDMAC_TH_SDMA_EN_26	IDMAC_TH_SDMA_EN_25	IDMAC_TH_SDMA_EN_24	IDMAC_TH_SDMA_EN_23	IDMAC_TH_SDMA_EN_22	IDMAC_TH_SDMA_EN_21	IDMAC_TH_SDMA_EN_20	IDMAC_TH_SDMA_EN_19	IDMAC_TH_SDMA_EN_18	IDMAC_TH_SDMA_EN_17	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_TH_SDMA_EN_15	IDMAC_TH_SDMA_EN_14	IDMAC_TH_SDMA_EN_13	IDMAC_TH_SDMA_EN_12	IDMAC_TH_SDMA_EN_11	IDMAC_TH_SDMA_EN_10	IDMAC_TH_SDMA_EN_9	IDMAC_TH_SDMA_EN_8	0	0	IDMAC_TH_SDMA_EN_5	0	IDMAC_TH_SDMA_EN_3	IDMAC_TH_SDMA_EN_2	IDMAC_TH_SDMA_EN_1	IDMAC_TH_SDMA_EN_0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_SDMA\_EVENT\_13 field descriptions

Field	Description
31 IDMAC_TH_SDMA_EN_31	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
30 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
29 IDMAC_TH_SDMA_EN_29	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
28 IDMAC_TH_SDMA_EN_28	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_13 field descriptions (continued)**

Field	Description
	0 SDMA event is disabled. 1 SDMA event is enabled.
27 IDMAC_TH_SDMA_EN_27	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
26 IDMAC_TH_SDMA_EN_26	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
25 IDMAC_TH_SDMA_EN_25	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
24 IDMAC_TH_SDMA_EN_24	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
23 IDMAC_TH_SDMA_EN_23	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
22 IDMAC_TH_SDMA_EN_22	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
21 IDMAC_TH_SDMA_EN_21	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
20 IDMAC_TH_SDMA_EN_20	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
19 IDMAC_TH_SDMA_EN_19	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_SDMA\_EVENT\_13 field descriptions (continued)**

Field	Description
	0 SDMA event is disabled. 1 SDMA event is enabled.
18 IDMAC_TH_ SDMA_EN_18	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
17 IDMAC_TH_ SDMA_EN_17	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
16 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
15 IDMAC_TH_ SDMA_EN_15	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
14 IDMAC_TH_ SDMA_EN_14	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
13 IDMAC_TH_ SDMA_EN_13	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
12 IDMAC_TH_ SDMA_EN_12	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
11 IDMAC_TH_ SDMA_EN_11	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
10 IDMAC_TH_ SDMA_EN_10	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.

*Table continues on the next page...*

**IPUx\_SDMA\_EVENT\_13 field descriptions (continued)**

Field	Description
9 IDMAC_TH_ SDMA_EN_9	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
8 IDMAC_TH_ SDMA_EN_8	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
7–6 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
5 IDMAC_TH_ SDMA_EN_5	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
4 Reserved	This read-only field is reserved and always has the value 0. 0 SDMA event is disabled. 1 SDMA event is enabled.
3 IDMAC_TH_ SDMA_EN_3	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
2 IDMAC_TH_ SDMA_EN_2	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
1 IDMAC_TH_ SDMA_EN_1	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.
0 IDMAC_TH_ SDMA_EN_0	Enable Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 SDMA event is disabled. 1 SDMA event is enabled.

### 37.5.30 SDMA Event Control Register 14 (IPUx\_SDMA\_EVENT\_14)

This register contains part of IPU SDMA events controls. The controls of TH (Threshold) of DMA Channels SDMA events [63:32] can be found in this register.

Address: Base address + 9Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_TH_SDMA_EN_47	IDMAC_TH_SDMA_EN_46	IDMAC_TH_SDMA_EN_45	IDMAC_TH_SDMA_EN_44	IDMAC_TH_SDMA_EN_43	IDMAC_TH_SDMA_EN_42	IDMAC_TH_SDMA_EN_41	IDMAC_TH_SDMA_EN_40			0					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_SDMA\_EVENT\_14 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 SDMA event is disabled. 1 SDMA event is enabled.
20 IDMAC_TH_SDMA_EN_52	Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.
19 IDMAC_TH_SDMA_EN_51	Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.  <i>n</i> Indicates the corresponding DMA channel number.  0 SDMA event is disabled. 1 SDMA event is enabled.

Table continues on the next page...

**IPUx\_SDMA\_EVENT\_14 field descriptions (continued)**

Field	Description
18 IDMAC_TH_SDMA_EN_50	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
17 IDMAC_TH_SDMA_EN_49	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
16 IDMAC_TH_SDMA_EN_48	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
15 IDMAC_TH_SDMA_EN_47	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
14 IDMAC_TH_SDMA_EN_46	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
13 IDMAC_TH_SDMA_EN_45	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
12 IDMAC_TH_SDMA_EN_44	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
11 IDMAC_TH_SDMA_EN_43	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>

*Table continues on the next page...*

**IPUx\_SDMA\_EVENT\_14 field descriptions (continued)**

Field	Description
10 IDMAC_TH_ SDMA_EN_42	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
9 IDMAC_TH_ SDMA_EN_41	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
8 IDMAC_TH_ SDMA_EN_40	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
7–2 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
1 IDMAC_TH_ SDMA_EN_33	<p>Threshold of Channel SDMA event. This bit is the control of Threshold of Channel #n. n Indicates the corresponding DMA channel number.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>
0 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 SDMA event is disabled. 1 SDMA event is enabled.</p>

### 37.5.31 Shadow Registers Memory Priority 1 Register (IPUx\_SRM\_PRI1)

The register controls the priority of SRM updates. The priority level for each block that has a shadow of its registers in the SRM should be unique. The priority level defines the order of SRM updates. A block with priority set to 010 will be updated before a block with priority set to 001.

Address: Base address + A0h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R									0								
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R			0	CSI0_SRM_MODE		CSI0_SRM_PRI				0		CSI1_SRM_MODE		CSI1_SRM_PRI			
W																	
Reset	0	0	0	0	0	0	0	1		0	0	0	0	0	0	0	0

#### IPUx\_SRM\_PRI1 field descriptions

Field	Description
31–13 Reserved	This read-only field is reserved and always has the value 0.
12–11 CSI0_SRM_MODE	CSI0 SRM Mode This field controls the SRM logic that handles the CSI0 registers  00 Automatic swapping is disabled; ARM platform is allowed to access the CSI1's region in the RAM 01 The SRM logic is controlled by the FSU. The update will be done of the next frame. 10 The SRM logic is controlled by the FSU. Registers are swapped continuously frame by frame 11 Update now. The SRM is controlled by the ARM Platform. The Register will be update now
10–8 CSI0_SRM_PRI	CSI0 SRM priority This bits define the priority of the CSI1 block
7–5 Reserved	This read-only field is reserved and always has the value 0.
4–3 CSI1_SRM_MODE	CSI1 SRM Mode This field controls the SRM logic that handles the CSI1 registers  00 Automatic swapping is disabled; ARM platform is allowed to access the CSI0's region in the RAM 01 The SRM logic is controlled by the FSU. The update will be done of the next frame. 10 The SRM logic is controlled by the FSU. Registers are swapped continuously frame by frame 11 Update now. The SRM is controlled by the ARM platform. The Register will be update now
CSI1_SRM_PRI	CSI1 SRM priority This bits define the priority of the CSI0 module

### 37.5.32 Shadow Registers Memory Priority 2 Register (IPUx\_SRM\_PRI2)

The register controls the priority of SRM updates. The priority level for each block that has a shadow of its registers in the SRM should be unique. The priority level defines the order of SRM updates. A block with priority set to 010 will be updated before a block with priority set to 001.

Address: Base address + A4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	0		DI1_SRM_MODE			DI1_SRM_PRI			0		DI0_SRM_MCU_USE			DI0_SRM_PRI			
W																	
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	DC_6_SRM_MODE	DC_2_SRM_MODE	DC_SRM_PRI			DP_A1_SRM_MODE			DP_A0_SRM_MODE			DP_S_SRM_MODE			DP_SRM_PRI		
W	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	

#### IPUx\_SRM\_PRI2 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–27 DI1_SRM_MODE	<p>DCI1 SRM Mode</p> <p>This field controls the SRM logic that handles the DI1 registers</p> <p>00 Automatic swapping is disabled; ARM platform is allowed to access the DI1 region in the RAM</p> <p>01 The SRM logic is controlled by the FSU. The update will be done of the next frame.</p> <p>10 The SRM logic is controlled by the FSU. Registers are swapped continuously frame by frame</p> <p>11 Update now. The SRM is controlled by the ARM platform. The Register will be update now</p>
26–24 DI1_SRM_PRI	<p>DI1 SRM priority</p> <p>This bits define the priority of the DI1 module</p>
23–21 Reserved	This read-only field is reserved and always has the value 0.
20–19 DI0_SRM_MCU_USE	<p>DI0 SRM is used by ARM platform</p> <p>This bit indicates that the registers of the DI0 are currently being updated by the ARM platform. The ARM platform should set this bit before accessing the SRM part that is relevant to the DI0. The ARM platform should clear this bit when the update procedure is finished. When this bit is set the SRM mechanism will not update the DI0's registers to avoid data coherency problems.</p> <p>1 DI0 SRM is currently updated by the ARM platform</p> <p>0 DI0 SRM s currently not updated by the ARM platform</p>
18–16 DI0_SRM_PRI	<p>DI0 SRM priority</p> <p>This bits define the priority of the DI0 module</p>

Table continues on the next page...

**IPUx\_SRM\_PRI2 field descriptions (continued)**

Field	Description
15–14 DC_6_SRM_MODE	<p>DC Group #6 SRM Mode</p> <p>This field controls the SRM logic that handles the DC Group #6 registers</p> <ul style="list-style-type: none"> <li>00 Automatic swapping is disabled; ARM platform is allowed to access the DC Group #6's region in the RAM</li> <li>01 The SRM logic is controlled by the FSU. The update will be done of the next frame.</li> <li>10 The SRM logic is controlled by the FSU. Registers are swapped continuously frame by frame</li> <li>11 Update now. The SRM is controlled by the ARM platform. The Register will be update now</li> </ul>
13–12 DC_2_SRM_MODE	<p>DC Group #2 SRM Mode</p> <p>This field controls the SRM logic that handles the DC Group #2 registers</p> <ul style="list-style-type: none"> <li>00 Automatic swapping is disabled; ARM platform is allowed to access the DC Group #2's region in the RAM</li> <li>01 The SRM logic is controlled by the FSU. The update will be done of the next frame.</li> <li>10 The SRM logic is controlled by the FSU. Registers are swapped continuously frame by frame</li> <li>11 Update now. The SRM is controlled by the ARM platform. The Register will be update now</li> </ul>
11–9 DC_SRM_PRI	<p>DC SRM priority</p> <p>This bits define the priority of the DC module</p>
8–7 DP_A1_SRM_MODE	<p>DP Async flow #1 SRM Mode</p> <p>This field controls the SRM logic that handles the DP Async flow #1 registers</p> <ul style="list-style-type: none"> <li>00 Automatic swapping is disabled; ARM platform is allowed to access the DP Async flow #1 region in the RAM</li> <li>01 The SRM logic is controlled by the FSU. The update will be done of the next frame.</li> <li>10 The SRM logic is controlled by the FSU. Registers are swapped continuously frame by frame</li> <li>11 Update now. The SRM is controlled by the ARM platform. The Register will be update now</li> </ul>
6–5 DP_A0_SRM_MODE	<p>DP Async flow #0 SRM Mode</p> <p>This field controls the SRM logic that handles the DP Async flow #0 registers</p> <ul style="list-style-type: none"> <li>00 Automatic swapping is disabled; ARM platform is allowed to access the DP Async flow #0 region in the RAM</li> <li>01 The SRM logic is controlled by the FSU. The update will be done of the next frame.</li> <li>10 The SRM logic is controlled by the FSU. Registers are swapped continuously frame by frame</li> <li>11 Update now. The SRM is controlled by the ARM platform. The Register will be update now</li> </ul>
4–3 DP_S_SRM_MODE	<p>DP sync flow SRM Mode</p> <p>This field controls the SRM logic that handles the DP sync flow registers</p> <ul style="list-style-type: none"> <li>00 Automatic swapping is disabled; ARM platform is allowed to access the DP sync flow region in the RAM</li> <li>01 The SRM logic is controlled by the FSU. The update will be done on the next frame.</li> <li>10 Reserved</li> <li>11 Update now. The SRM is controlled by the ARM platform. The Register will be update now</li> </ul>
DP_SRM_PRI	<p>DP SRM priority</p> <p>This bits define the priority of the DP module</p>

### 37.5.33 FSU Processing Flow 1 Register (IPUx\_FS\_PROC\_FLOW1)

This register contains controls for IPU's tasks.

Address: Base address + A8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	VF_IN_VALID	ENC_IN_VALID	VDI_SRC_SEL	PRP_SRC_SEL	VDI3_SRC_SEL	VDI1_SRC_SEL	PP_ROT_SRC_SEL									
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PP_SRC_SEL	PRPVF_ROT_SRC_SEL							0				PRPENC_ROT_SRC_SEL			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_FS\_PROC\_FLOW1 field descriptions

Field	Description
31 VF_IN_VALID	View-finder Input valid. Setting this bit indicates that the buffer in memory for viewfinder is validated by the ARM platform (valid only when RWS_EN is '1').  0 View-finder should skip buffer in memory. 1 View-finder should use buffer in memory.
30 ENC_IN_VALID	Encoding Input valid. Setting this bit indicates that the buffer in memory for encoding is validated by the ARM platform (valid only when RWS_EN is '1').  0 Encoding should skip buffer in memory. 1 Encoding should use buffer in memory.
29–28 VDI_SRC_SEL	Source select for the VDIC  This field is relevant if the VDIC works in de-interlacing mode (when VDI_CMB_EN bit is clear)  00 ARM platform 01 CSI direct (cb7) 10 Reserved 10 VDOA 11 Reserved
27–24 PRP_SRC_SEL	Source select for the Pre Processing Task  0000 ARM platform

Table continues on the next page...

**IPUx\_FS\_PROC\_FLOW1 field descriptions (continued)**

Field	Description
	0001 capture0 (smfc0) — — — 0011 capture2 (smfc2) — — — 0101 IC direct (cb7) — 0110 IRT Encoding 0111 IRT viewfinder 1000 Reserved 1001 Reserved 1010 Reserved 1011 autoref 1100 autoref+snoop1 1101 autoref+snoop2 1110 snoop1 1111 snoop2
23–22 VDI3_SRC_SEL	Source select for the VDIC plane #3 (IDMAC's CH 25) 00 ARM platform This field is relevant only if the VDIC works in combining mode (VDI_CMB_EN bit is set) 01 IRT viewfinder (ch 49) 10 IRT playback (ch 50) 11 post-processing (ch 22)
21–20 VDI1_SRC_SEL	Source select for the VDIC plane #1 (IDMAC's CH26) This field is relevant only if the VDIC works in combining mode (VDI_CMB_EN bit is set) 00 ARM platform 01 IRT viewfinder 10 IRT playback 11 post-processing
19–16 PP_ROT_SRC_SEL	Source select for the pre processing task of the IRT (CH 50) 0000 ARM platform 0001 capture0 (smfc0) — 0010 Reserved 0011 capture2 (smfc2) — 0100 Reserved 0101 Post-processing 0110 Reserved 0111 Reserved —

*Table continues on the next page...*

**IPUx\_FS\_PROC\_FLOW1 field descriptions (continued)**

Field	Description
	1000 Reserved — 1001 Reserved 1010 Reserved 1011 autoref 1100 autoref+snoop1 1101 autoref+snoop2 1110 snoop1 1111 snoop2
15–12 PP_SRC_SEL	Source select for the pre processing task of the IC 0000 ARM platform 0001 capture0 (smfc0) — 0010 Reserved 0011 capture2 (smfc2) — 0100 Reserved 0101 Reserved 0110 Rotation for post-processing 0111 Reserved — 1000 Reserved 1000 VDOA — 1001 Reserved 1010 Reserved 1011 autoref 1100 autoref+snoop1 1101 autoref+snoop2 1110 snoop1 1111 snoop2
11–8 PRPVF_ROT_ SRC_SEL	Source select for the view finder task of the IRT 0000 ARM platform 0001 capture0 (smfc0) — 0010 capture1 (smfc1) — 0011 capture2 (smfc2) — 0100 capture3 (smfc3) — 0101 IC direct (cb7) — 0110 Reserved 0111 Reserved

*Table continues on the next page...*

**IPUx\_FS\_PROC\_FLOW1 field descriptions (continued)**

Field	Description
	1000 View-finder 1001 Reserved 1010 Reserved 1011 autoref 1100 autoref+snoop1 1101 autoref+snoop2 1110 snoop1 1111 snoop2
7–4 Reserved	This read-only field is reserved and always has the value 0.
PRPENC_ROT_ SRC_SEL	Source select for the encoding task of the IRT 0000 ARM platform 0001 capture0 (smfc0) — 0010 capture1 (smfc1) — 0011 capture2 (smfc2) — 0100 capture3 (smfc3) — 0101 IC direct (cb7) — 0110 Reserved 0111 encoding 1000 Reserved 1001 Reserved 1010 Reserved 1011 autoref 1100 autoref+snoop1 1101 autoref+snoop2 1110 snoop1 1111 snoop2

### 37.5.34 FSU Processing Flow 2 Register (IPUx\_FS\_PROC\_FLOW2)

This register contains controls for IPU's tasks.

Address: Base address + ACh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_FS\_PROC\_FLOW2 field descriptions

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–24 PRP_DEST_SEL	<b>Pre processing destination select (for channel DMAIC_7)</b> 0000 ARM platform 0001 IC input buffer (ch12) 0010 PP (ch11) 0011 PP_ROT (ch47) 0100 DC1 (ch28) 0101 DC2 (ch41) 0110 DP_ASYNC1 (ch24) 0111 DP_ASYNC0 (ch29) 1000 DP_SYNC1 (ch27) 1001 DP_SYNC0 (ch23) 1010 Alt DC2 (ch41) 1011 Alt DP_ASYNC1 (ch24) 1100 Alt DP_ASYNC0 (ch29) 1111 Reserved
23–20 PRPENC_ROT_DEST_SEL	Destination select for Rotation task coming from the Encoding input 0000 ARM platform 0001 Reserved 0010 Reserved — 0011 Reserved — 0100 Reserved 0101 IC Pre Processing 0110 Reserved 0111 DC1 (ch28) 1000 DC2 (ch41)

Table continues on the next page...

## IPUX\_FS\_PROC\_FLOW2 field descriptions (continued)

Field	Description
	1001 <b>DP_SYNC0 (ch23)</b> 1010 <b>DP_SYNC1 (ch27)</b> 1011 <b>DP_ASYNC1 (ch24)</b> 1100 <b>DP_ASYNC0 (ch29)</b> 1101 Alt DC2 (ch41) 1110 Alt <b>DP_ASYNC1 (ch24)</b> 1111 Alt <b>DP_ASYNC0 (ch29)</b>
19–16 PP_ROT_DEST_SEL	Destination select for Rotation task coming from the Post Processing input  0000 ARM platform 0001 Reserved 0010 Reserved 0011 Reserved 0100 IC Playback (Post Processing) — — 0101 VDI_PLANE3 (Ch 25) — — 0110 VDI_PLANE1 (Ch 26) 0111 DC1 (ch28) 1000 DC2 (ch41) 1001 <b>DP_SYNC0 (ch23)</b> 1010 <b>DP_SYNC1 (ch27)</b> 1011 <b>DP_ASYNC1 (ch24)</b> 1100 <b>DP_ASYNC0 (ch29)</b> 1101 Alt DC2 (ch41) 1110 Alt <b>DP_ASYNC1 (ch24)</b> 1111 Alt <b>DP_ASYNC0 (ch29)</b>
15–12 PP_DEST_SEL	Destination select for post processing task  0000 ARM platform 0001 Reserved 0010 Reserved 0011 IRT playback — 0100 VDI_PLANE3 (Ch 25) — 0101 VDI_PLANE1 (Ch 26) 0110 Reserved 0111 DC1 (ch28) 1000 DC2 (ch41) 1001 <b>DP_SYNC0 (ch23)</b> 1010 <b>DP_SYNC1 (ch27)</b> 1011 <b>DP_ASYNC1 (ch24)</b> 1100 <b>DP_ASYNC0 (ch29)</b> 1101 Alt DC2 (ch41)

Table continues on the next page...

**IPUx\_FS\_PROC\_FLOW2 field descriptions (continued)**

Field	Description
	1110 Alt DP_ASYNC1 (ch24) 1111 Alt DP_ASYNC0 (ch29)
11–8 PRPVF_ROT_DEST_SEL	Destination select for Rotation task coming from the View finder input  0000 ARM platform 0001 Reserved 0010 Reserved — — 0011 VDI_PLANE3 (Ch 25) — — 0100 VDI_PLANE1 (Ch 26) 0101 IC Pre Processing 0110 Reserved 0111 DC1 (ch28) 1000 DC2 (ch41) 1001 <b>DP_SYNC0 (ch23)</b> 1010 <b>DP_SYNC1 (ch27)</b> 1011 <b>DP_ASYNC1 (ch24)</b> 1100 <b>DP_ASYNC0 (ch29)</b> 1101 Alt DC2 (ch41) 1110 Alt <b>DP_ASYNC1 (ch24)</b> 1111 Alt <b>DP_ASYNC0 (ch29)</b>
7–4 PRPVF_DEST_SEL	Destination select for View finder task  0000 ARM platform 0001 IRT viewfinder 0010 Reserved 0011 Reserved 0100 Reserved 0101 Reserved 0110 Reserved 0111 DC1 (ch28) 1000 DC2 (ch41) 1001 <b>DP_SYNC0 (ch23)</b> 1010 <b>DP_SYNC1 (ch27)</b> 1011 <b>DP_ASYNC1 (ch24)</b> 1100 <b>DP_ASYNC0 (ch29)</b> 1101 Alt DC2 (ch41) 1110 Alt <b>DP_ASYNC1 (ch24)</b> 1111 Alt <b>DP_ASYNC0 (ch29)</b>
PRP_ENC_DEST_SEL	Destination select for Encoding task  0000 ARM platform 0001 IRT Encoding 0010 Reserved

*Table continues on the next page...*

**IPUx\_FS\_PROC\_FLOW2 field descriptions (continued)**

Field	Description
0011	Reserved
0100	Reserved
0101	Reserved
0110	Reserved
0111	DC1 (ch28)
1000	DC2 (ch41)
1001	<b>DP_SYNC0 (ch23)</b>
1010	<b>DP_SYNC1 (ch27)</b>
1011	<b>DP_ASYNC1 (ch24)</b>
1100	<b>DP_ASYNC0 (ch29)</b>
1101	Alt DC2 (ch41)
1110	Alt <b>DP_ASYNC1 (ch24)</b>
1111	Alt <b>DP_ASYNC0 (ch29)</b>

### 37.5.35 FSU Processing Flow 3 Register (IPUx\_FS\_PROC\_FLOW3)

This register contains controls for IPU's tasks.

- Hide VPU\_SUB\_FRAME\_SYNC for all versions
- Show VPU\_SUB\_FRAME\_SYNC for IPUv3H version.
- The table below tagged with other settings (like IPU3M\_only) should be hidden in IPUv3H version.
- This requires some sophisticated conditional tag settings

Address: Base address + B0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R				0			VPU_DEST_SEL		EXT_SRC2_DEST_SEL	EXT_SRC1_DEST_SEL		0		VDOA_DEST_SEL		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		SMFC3_DEST_SEL		SMFC2_DEST_SEL		SMFC1_DEST_SEL		SMFC0_DEST_SEL							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_FS\_PROC\_FLOW3 field descriptions**

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.
25–24 VPU_DEST_SEL	This bits selects the corresponding IDMAC channel's EOL indication to be used for sub frame synchronization with the VPU. The corresponding IDMAC channel's EOLI bit at the CPMEM has to be set as well.

*Table continues on the next page...*

**IPUx\_FS\_PROC\_FLOW3 field descriptions (continued)**

Field	Description
	00 disabled 01 capture0 (smfc0) ( <b>ch0</b> ) 10 capture2 (smfc2) ( <b>ch2</b> ) 11 IC viewfinder (ch21)
23–22 EXT_SRC2_DEST_SEL	Destination select for External Source 2 00 disabled 01 <b>DP_SYNC0 (ch23)</b> 10 <b>DP_SYNC1 (ch27)</b> 11 DC1 (ch28)
21–20 EXT_SRC1_DEST_SEL	Destination select for External Source 1 00 disabled 01 <b>DP_SYNC0 (ch23)</b> 10 <b>DP_SYNC1 (ch27)</b> 11 DC1 (ch28)
19–18 Reserved	This read-only field is reserved and always has the value 0.
17–16 VDOA_DEST_SEL	<b>Destination select for VDOA</b> 00 disabled 01 IC Playback (Post Processing) 10 VDI (ch8, ch9 & ch10 or ch9 according to VDI_MOT_SEL settings) 11 Reserved
15–14 Reserved	This read-only field is reserved and always has the value 0.
13–11 SMFC3_DEST_SEL	Destination select for SMFC3 000 ARM platform 001 IRT Encoding 010 IRT viewfinder 011 IRT playback 100 IC Playback (Post Processing) 101 IC Pre Processing — 111 Reserved
10–7 SMFC2_DEST_SEL	Destination select for SMFC2 0000 ARM platform 0001 IRT Encoding 0010 IRT viewfinder 0011 IRT playback 0100 IC Playback (Post Processing) 0101 IC Pre Processing — 0111 DC1 (ch28) 1000 DC2 (ch41) 1001 <b>DP_SYNC0 (ch23)</b>

Table continues on the next page...

**IPUx\_FS\_PROC\_FLOW3 field descriptions (continued)**

Field	Description
	1010 <b>DP_SYNC1 (ch27)</b> 1011 <b>DP_ASYNC1 (ch24)</b> 1100 <b>DP_ASYNC0 (ch29)</b> 1101 Alt DC2 (ch41) 1110 Alt <b>DP_ASYNC1 (ch24)</b> 1111 Alt <b>DP_ASYNC0 (ch29)</b>
6–4 SMFC1_DEST_SEL	Destination select for SMFC1 000 ARM platform 001 IRT Encoding 010 IRT viewfinder 011 IRT playback 100 IC Playback (Post Processing) 101 IC Pre Processing — 111 Reserved
SMFC0_DEST_SEL	Destination select for SMFC0 0000 ARM platform 0001 IRT Encoding 0010 IRT viewfinder 0011 IRT playback 0100 IC Playback (Post Processing) 0101 IC Pre Processing — 0111 DC1 (ch28) 1000 DC2 (ch41) 1001 <b>DP_SYNC0 (ch23)</b> 1010 <b>DP_SYNC1 (ch27)</b> 1011 <b>DP_ASYNC1 (ch24)</b> 1100 <b>DP_ASYNC0 (ch29)</b> 1101 Alt DC2 (ch41) 1110 Alt <b>DP_ASYNC1 (ch24)</b> 1111 Alt <b>DP_ASYNC0 (ch29)</b>

### 37.5.36 FSU Displaying Flow 1 Register (IPUx\_FS\_DISP\_FLOW1)

This register contains controls for IPU's tasks.

Address: Base address + B4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_FS\_DISP\_FLOW1 field descriptions

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23–20 DC1_SRC_SEL	<p>Source select for DS1/DS2 - MG (graphics) plane (ch28)</p> <p>0000 ARM platform      0001 capture0 (smfc0)      —      0010 capture2 (smfc2)      —      0011 IC encoding      0100 IC viewfinder      0101 IC playback      0110 IRT Encoding      0111 IRT viewfinder      1000 IRT playback      —      1001 Reserved      —      1010 Reserved      1011 autoref      1100 autoref+snoop1      —      1101 External source #1 (e.g. an external block like GPU)      1110 snoop1      —      1111 External source #2 (e.g. an external block like GPU)</p>
19–16 DC2_SRC_SEL	<p>Source select for DS3 (ch41)</p> <p>0000 ARM platform      0001 capture0 (smfc0)      —      0010 capture2 (smfc2)</p>

Table continues on the next page...

**IPUx\_FS\_DISP\_FLOW1 field descriptions (continued)**

Field	Description
	<p>—</p> <p>0011 IC encoding</p> <p>0100 IC viewfinder</p> <p>0101 IC playback</p> <p>0110 IRT Encoding</p> <p>0111 IRT viewfinder</p> <p>1000 IRT playback</p> <p>—</p> <p>1001 Reserved</p> <p>—</p> <p>1010 Reserved</p> <p>1011 autoref</p> <p>1100 autoref+snoop1</p> <p>1101 autoref+snoop2</p> <p>1110 snoop1</p> <p>1111 snoop2</p>
15–12 DP_ASYNC1_SRC_SEL	<p>Source select for DS1/DS2 - Vx (video) plane (ch24)</p> <p>0000 ARM platform</p> <p>0001 capture0 (smfc0)</p> <p>—</p> <p>0010 capture2 (smfc2)</p> <p>—</p> <p>0011 IC encoding</p> <p>0100 IC viewfinder</p> <p>0101 IC playback</p> <p>0110 IRT Encoding</p> <p>0111 IRT viewfinder</p> <p>1000 IRT playback</p> <p>—</p> <p>1001 Reserved</p> <p>—</p> <p>1010 Reserved</p> <p>1011 autoref</p> <p>1100 autoref+snoop1</p> <p>1101 autoref+snoop2</p> <p>1110 snoop1</p> <p>1111 snoop2</p>
11–8 DP_ASYNC0_SRC_SEL	<p>Source select for DS2 - MG (graphics) plane (ch29)</p> <p>0000 ARM platform</p> <p>0001 capture0 (smfc0)</p> <p>—</p> <p>0010 capture2 (smfc2)</p> <p>—</p> <p>0011 IC encoding</p> <p>0100 IC viewfinder</p>

*Table continues on the next page...*

**IPUx\_FS\_DISP\_FLOW1 field descriptions (continued)**

Field	Description
	0101 IC playback 0110 IRT Encoding 0111 IRT viewfinder 1000 IRT playback — 1001 Reserved — 1010 Reserved 1011 autoref 1100 autoref+snoop1 1101 autoref+snoop2 1110 snoop1 1111 snoop2
7–4 DP_SYNC1_ SRC_SEL	Source select for DS1/DS2 - Vx (video) plane (ch27) 0000 ARM platform 0001 capture0 (smfc0) — 0010 capture2 (smfc2) — 0011 IC encoding 0100 IC viewfinder 0101 IC playback 0110 IRT Encoding 0111 IRT viewfinder 1000 IRT playback — 1001 Reserved — 1010 Reserved — — — — — 1110 snoop1 1111 snoop2
DP_SYNC0_ SRC_SEL	Source select for DS2 - MG (graphics) plane (ch23) 0000 ARM platform 0001 capture0 (smfc0) — 0010 capture2 (smfc2) — 0011 IC encoding 0100 IC viewfinder

*Table continues on the next page...*

**IPUx\_FS\_DISP\_FLOW1 field descriptions (continued)**

Field	Description	
	0101	IC playback
	0110	IRT Encoding
	0111	IRT viewfinder
	1000	IRT playback
	—	
	1001	Reserved
	—	
	1010	Reserved
	—	
	—	
	—	
	—	
	—	
	1110	snoop1
	1111	snoop2

**37.5.37 FSU Displaying Flow 2 Register (IPUx\_FS\_DISP\_FLOW2)**

This register contains controls for IPU's tasks.

Address: Base address + B8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0							0			DP_		DP_				
W																																	

Reset 0

**IPUx\_FS\_DISP\_FLOW2 field descriptions**

Field	Description	
31–20 Reserved	This read-only field is reserved and always has the value 0.	
19–16 DC2_ALT_SRC_SEL	Source select for Alternate DS3 (ch41) 0000 ARM platform 0001 capture0 (smfc0) — 0010 capture2 (smfc2) — 0011 IC encoding 0100 IC viewfinder	

*Table continues on the next page...*

**IPUx\_FS\_DISP\_FLOW2 field descriptions (continued)**

Field	Description
	0101 IC playback 0110 IRT Encoding 0111 IRT viewfinder 1000 IRT playback — 1001 Reserved — 1010 Reserved 1011 autoref 1100 autoref+snoop1 1101 autoref+snoop2 1110 snoop1 1111 snoop2
15–8 Reserved	This read-only field is reserved and always has the value 0.
7–4 DP_ASYNC1_ ALT_SRC_SEL	Source select for alternate DS1/DS2 - Vx (video) plane (ch24) 0000 ARM platform 0001 capture0 (smfc0) — 0010 capture2 (smfc2) — 0011 IC encoding 0100 IC viewfinder 0101 IC playback 0110 IRT Encoding 0111 IRT viewfinder 1000 IRT playback — 1001 Reserved — 1010 Reserved 1011 autoref 1100 autoref+snoop1 1101 autoref+snoop2 1110 snoop1 1111 snoop2
DP_ASYNC0_ ALT_SRC_SEL	Source select for alternate DS2 - MG (graphics) plane (ch29) 0000 ARM platform 0001 capture0 (smfc0) — 0010 capture2 (smfc2) — 0011 IC encoding 0100 IC viewfinder 0101 IC playback

*Table continues on the next page...*

**IPUx\_FS\_DISP\_FLOW2 field descriptions (continued)**

Field	Description
	0110 IRT Encoding 0111 IRT viewfinder 1000 IRT playback — 1001 Reserved — 1010 Reserved 1011 autoref 1100 autoref+snoop1 1101 autoref+snoop2 1110 snoop1 1111 snoop2

**37.5.38 SKIP Register (IPUx\_SKIP)**

This register controls the different frame skipping supported by the IPU.

Address: Base address + BCCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_SKIP field descriptions**

Field	Description
31–20 VDI_SKIP	<b>VDI_SKIP</b> These 12 bits define the skipping pattern of the frames send from the VDIC. The VDIC avoids reading fields from the memory if the output frame is skipped. Skipping is relevant only if the source to the VDIC is coming from the CSI. Skipping is done for a set of frames. The number of frames in a set is defined at VDI_MAX_RATIO_SKIP. when VDI_MAX_RATIO_SKIP = 1 => VDI_SKIP[1:0] is used; other bits are ignored when VDI_MAX_RATIO_SKIP = 2 => VDI_SKIP[2:0] are used; other bits are ignored .. .. when VDI_MAX_RATIO_SKIP = 11 => VDI_SKIP[11:0] are used;
19–16 VDI_MAX_RATIO_SKIP	Maximum Ratio Skip for VDIC

*Table continues on the next page...*

**IPUx\_SKIP field descriptions (continued)**

Field	Description
	<p>These bits define the number of frames in a skipping set. The maximum value of this bits is 11. When set to 0 the skipping is disabled.</p>
15–11 CSI_SKIP_IC_VF	<p>CSI SKIP IC_VF</p> <p>These 5 bits define the skipping pattern of the frames send to the IC for view finder task from one of the CSIs as defined on the CSI_SEL and IC_INPUT bits Skipping is done for a set of frames. The number of frames in a set is defined at CSI_MAX_RATIO_SKIP_IC_VF.</p> <p>when CSI_MAX_RATIO_SKIP_IC_VF = 1 =&gt; CSI_SKIP_IC_VF[1:0] are used; other bits are ignored</p> <p>when CSI_MAX_RATIO_SKIP_IC_VF = 2 =&gt; CSI_SKIP_IC_VF[2:0] are used; other bits are ignored</p> <p>when CSI_MAX_RATIO_SKIP_IC_VF = 3 =&gt; CSI_SKIP_IC_VF[3:0] are used; other bits are ignored</p> <p>when CSI_MAX_RATIO_SKIP_IC_VF = 4 =&gt; CSI_SKIP_IC_VF[4:0] are used;</p> <p>Setting bit #n of CSI_SKIP_IC_VF means that the #n frame in the set is skipped.</p> <p>For example: if CSI_MAX_RATIO_SKIP_IC_VF = 4 and CSI_SKIP_IC_VF = 11010</p> <p>Frames #0 &amp; Frame #2 will not be skipped as bit0 and bit2 are cleared</p> <p>Frames #1 &amp; Frame #3 will be skipped as bit1 and bit3 are set</p> <p>bit #4 is ignored as CSI_MAX_RATIO_SKIP_IC_VF is set to 4</p>
10–8 CSI_MAX_RATIO_SKIP_IC_VF	<p>CSI Maximum Ratio Skip for IC (view finder task)</p> <p>These bits define the number of frames in a skipping set. The maximum value of this bits is 4. When set to 0 the skipping is disabled.</p>
7–3 CSI_SKIP_IC_ENC	<p>CSI SKIP IC_ENC</p> <p>These 5 bits define the skipping pattern of the frames send to the IC for encoding task from one of the CSIs as defined on the CSI_SEL and IC_INPUT bits Skipping is done for a set of frames. The number of frames in a set is defined at CSI_MAX_RATIO_SKIP_IC_ENC.</p> <p>when CSI_MAX_RATIO_SKIP_IC_ENC = 1 =&gt; CSI_SKIP_IC_ENC[1:0] are used; other bits are ignored</p> <p>when CSI_MAX_RATIO_SKIP_IC_ENC = 2 =&gt; CSI_SKIP_IC_ENC[2:0] are used; other bits are ignored</p> <p>when CSI_MAX_RATIO_SKIP_IC_ENC = 3 =&gt; CSI_SKIP_IC_ENC[3:0] are used; other bits are ignored</p> <p>when CSI_MAX_RATIO_SKIP_IC_ENC = 4 =&gt; CSI_SKIP_IC_ENC[4:0] are used;</p> <p>Setting bit #n of CSI_SKIP_IC_ENC means that the #n frame in the set is skipped.</p> <p>For example: if CSI_MAX_RATIO_SKIP_IC_ENC = 4 and CSI_SKIP_IC_ENC = 11010</p> <p>Frames #0 &amp; Frame #2 will not be skipped as bit0 and bit2 are cleared</p> <p>Frames #1 &amp; Frame #3 will be skipped as bit1 and bit3 are set</p> <p>bit #4 is ignored as CSI_MAX_RATIO_SKIP_IC_ENC is set to 4</p>
CSI_MAX_RATIO_SKIP_IC_ENC	<p>CSI Maximum Ratio Skip for IC (encoding task)</p> <p>These bits define the number of frames in a skipping set. The maximum value of this bits is 4. When set to 0 the skipping is disabled.</p>

### 37.5.39 Display General Control Register (IPUx\_DISP\_GEN)

This register controls various aspects of the display port.

Address: Base address + C4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R							0		D11_COUNTER_RELEASE	D10_COUNTER_RELEASE						
W									CSI_VSYNC_DEST	MCU_MAX_BURST_STOP			MCU_T		MCU_DI_ID_9	MCU_DI_ID_8
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0	0	DP_FG_EN_ASYNC1	DP_FG_EN_ASYNC0	DP_ASYNC_DOUBLE_FLOW	DC2_DOUBLE_FLOW	DI1_DUAL_MODE	DI0_DUAL_MODE
W										DP_PIPE_CLR						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DISP\_GEN field descriptions

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_DISP\_GEN field descriptions (continued)**

Field	Description
25 DI1_COUNTER_RELEASE	<p>DI1 Counter release</p> <p>By default the DI0 counters responsible for waveform generation for sync flow are frozen. For the first attempt to use the DI in sync flow the user should set this bit</p> <p>1 counter is released and running 0 counter is cleared and stopped</p>
24 DI0_COUNTER_RELEASE	<p>DI1 Counter release</p> <p>By default the DI0 counters responsible for waveform generation for sync flow are frozen. For the first attempt to use the DI in sync flow the user should set this bit</p> <p>1 counter is released and running 0 counter is cleared and stopped</p>
23 CSI_VSYNC_DEST	<p>CSI_VSYNC destination</p> <p>This bit defines the destination of the VSYNC coming from the CSI's</p> <p>1 csi1_vsync is connected to DI0; csi0_vsync is connected to DI1 0 csi0_vsync is connected to DI0; csi1_vsync is connected to DI1</p>
22 MCU_MAX_BURST_STOP	<p>ARM platform Maximal burst</p> <p>This bit limit the maximal unspecified length burst.</p> <p>1 The maximum unspecified burst length is 8-beat 0 The unspecified burst length is unlimited</p>
21–18 MCU_T	<p>The address space for accesses through the AHB-lite slave port is MB and it is split internally (with 32MB resolution) according to bits [28:25] of the address. Using the following notation:</p> <p>Address = (ID[31:29], MSB[28:25], LSB[24:0])</p> <p>The address is used as follows ("T" is a configurable integer between 0 and 13):</p> <p>MSB&lt;T: access to an external device, with address = (MSB, LSB)</p> <p>T&lt;=MSB&lt;14: access to an external device, with address (MSB-T, LSB)</p>
17 MCU_DI_ID_9	<p>MCU_DI_ID_9 - DI ID via DC channel 9.</p> <p>This bit defines the DI that the ARM platform DC's access via channel #9</p> <p>1 ARM platform accesses DC's channel #9 via DI1. 0 ARM platform accesses DC's channel #9 via DI0.</p>
16 MCU_DI_ID_8	<p>MCU_DI_ID_8 - DI ID via DC channel 8.</p> <p>This bit defines the DI that the ARM platform DC's access via channel #8</p> <p>1 ARM platform accesses DC's channel #8 via DI1. 0 ARM platform accesses DC's channel #8 via DI0.</p>
15–7 Reserved	This read-only field is reserved and always has the value 0.
6 DP_PIPE_CLR	<p>DP Pipe Clear</p> <p>This bit clears the internal pipe of the DP. The user may use this bit in case of an error condition</p> <p>This is a self clear bit</p>

*Table continues on the next page...*

**IPUx\_DISP\_GEN field descriptions (continued)**

Field	Description
	<p>1 Clear the internal pipe of the DP 0 Idle - does nothing</p>
5 DP_FG_EN_ASYNC1	<p>FG_EN - partial plane Enable for async flow 1. This bit enables the partial plane channel.</p> <p>1 partial plane channel is enabled. 0 partial plane channel is disabled.</p>
4 DP_FG_EN_ASYNC0	<p>FG_EN - partial plane Enable for async flow 0. This bit enables the partial plane channel.</p> <p>1 partial plane channel is enabled. 0 partial plane channel is disabled.</p>
3 DP_ASYNC_DOUBLE_FLOW	<p>DP Async Double Flow. This bit define how many async flows are currently handles via DP channel (ch24+29)</p> <p>1 2 flows are handled via DP 0 single flow is handled via DP</p>
2 DC2_DOUBLE_FLOW	<p>DC2 Double Flow. This bit define how many flows are currently handles via DC2 channel (ch41)</p> <p>1 2 flows are handled via DC2 0 single flow is handled via DC2</p>
1 DI1_DUAL_MODE	<p>DI1 dual mode control</p> <p>1 DI1 operates in dual mode 0 DI1 is not in dual mode</p>
0 DI0_DUAL_MODE	<p>DI0 dual mode control</p> <p>1 DI0 operates in dual mode 0 DI0 is not in dual mode</p>

### 37.5.40 Display Alternate Flow Control Register 1 (IPUx\_DISP\_ALT1)

This register controls various aspects of the display port.

Address: Base address + C8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DISP\_ALT1 field descriptions

Field	Description
31–28 sel_alt_0	Select alternative parameters instead of DI Sync Wave Gen counter#. The DI is selected according to DP's synchronous channel destination 0000-disable  0001 instead of counter 1 0010 instead of counter 2 1000 instead of counter 8
27–16 step_repeat_alt_0	This fields defines the amount of repetitions that will be performed by the counter
15 cnt_auto_reload_alt_0	Counter auto reload mode  1 The counter will automatically be reloaded forever, ignoring the value of the step_repeat_alt_0 field 0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the step_repeat_alt_0 field
14–12 cnt_clr_sel_alt_0	Counter Clear select  This field defines the source of the signals that clears the counter.  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock.

Table continues on the next page...

**IPUx\_DISP\_ALT1 field descriptions (continued)**

Field	Description
	010 Reserved 011 Reserved 100 Reserved 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.
run_value_m1_alt_0	Counter pre defined value This fields defines the counter pre defines value. real value- 1

### 37.5.41 Display Alternate Flow Control Register 2 (IPUx\_DISP\_ALT2)

This register controls various aspects of the display port.

Address: Base address + CCh offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R								0									
W																	run_resolution_alt_0
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																
W																	offset_value_alt_0
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DISP\_ALT2 field descriptions**

Field	Description
31–19 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**IPUx\_DISP\_ALT2 field descriptions (continued)**

Field	Description
18–16 run_resolution_ alt_0	Counter Run Resolution This field defines the trigger causing the counter to increment. The counter run resolution should be defined in the same way as in original DI's counter#
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 offset_resolution_ alt_0	Counter offset Resolution This field defines the trigger causing the offset counter to increment The counter offset resolution should be defined in the same way as in original DI's counter#
offset_value_alt_0	Counter offset value The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by

**37.5.42 Display Alternate Flow Control Register 3  
(IPUx\_DISP\_ALT3)**

This register controls various aspects of the display port.

Address: Base address + D0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	sel_alt_1				step_repeat_alt_1											
W																
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	cnt_auto_reload_ alt_1		cnt_clr_sel_alt_1						run_value_m1_alt_1							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DISP\_ALT3 field descriptions**

Field	Description
31–28 sel_alt_1	Select alternative parameters instead of DI Sync Wave Gen counter#. The DI is selected according to DP's synchronous channel destination

*Table continues on the next page...*

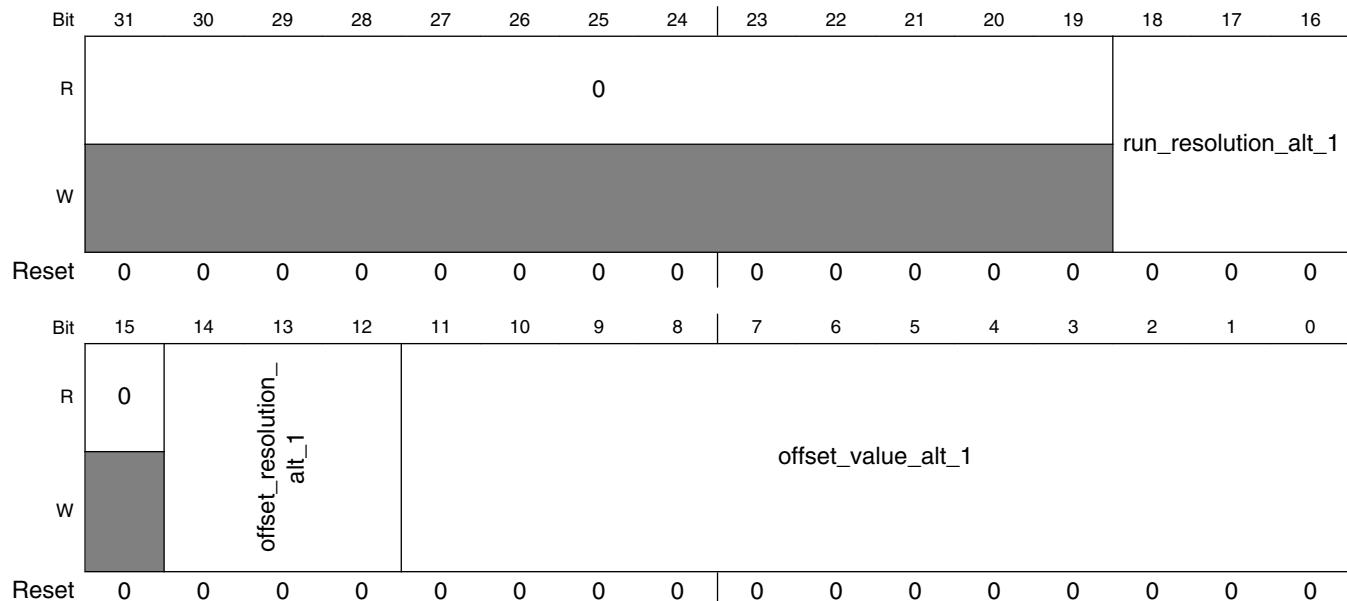
**IPUx\_DISP\_ALT3 field descriptions (continued)**

Field	Description
	0000 disable 0001 instead of counter 1 0010 instead of counter 2 1000 instead of counter 8
27–16 step_repeat_alt_1	This fields defines the amount of repetitions that will be performed by the counter
15 cnt_auto_reload_alt_1	Counter auto reload mode 1 The counter will automatically be reloaded forever, ignoring the value of the step_repeat_alt_0 field 0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the step_repeat_alt_0 field
14–12 cnt_clr_sel_alt_1	Counter Clear select This field defines the source of the signals that clears the counter. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 Reserved 011 Reserved 100 Reserved 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.
run_value_m1_alt_1	Counter pre defined value This fields defines the counter pre defines value. real value- 1

### 37.5.43 Display Alternate Flow Control Register 4 (IPUx\_DISP\_ALT4)

This register controls various aspects of the display port.

Address: Base address + D4h offset



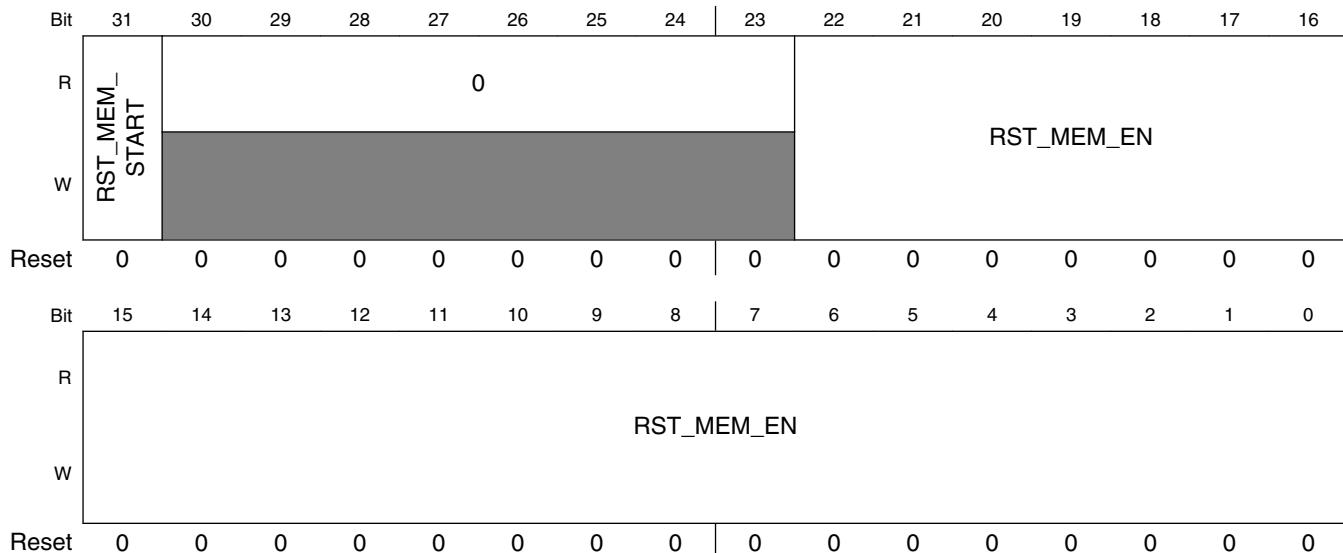
**IPUx\_DISP\_ALT4 field descriptions**

Field	Description
31–19 Reserved	This read-only field is reserved and always has the value 0.
18–16 run_resolution_	Counter Run Resolution
alt_1	This field defines the trigger causing the counter to increment. The counter run resolution should be defined in the same way as in original DI's counter#
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 offset_resolution_	Counter offset Resolution
alt_1	This field defines the trigger causing the offset counter to increment The counter offset resolution should be defined in the same way as in original DI's counter#
offset_value_alt_	Counter offset value
1	The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by

### 37.5.44 Memory Reset Control Register (IPUx\_MEM\_RST)

This register controls the memory reset mechanism. IPU has a hardware mechanism for clearing the content of the internal memories. This allows the user to clear the content of or more of the internal memories without the need to perform write accesses to the memories.

Address: Base address + DCh offset



**IPUx\_MEM\_RST field descriptions**

Field	Description
31 RST_MEM_START	Memory Reset Start Writing one to this bit activate the memory reset mechanism. The memories that their corresponding RST_MEM_EN bit is set will be cleared. When the memory reset mechanism completes the memory clearing procedure this bit will be automatically cleared.  1 The memory reset mechanism is activated and busy 0 Idle, the memory reset mechanism is not working.
30–23 Reserved	This read-only field is reserved and always has the value 0.
RST_MEM_EN	Reset Memory Enable  Each bit on this field enables the memory reset mechanism for a specific memory. The user should set the relevant bits for the memories that need to be cleared. Below is the list of memories and their corresponding bit.  srm = rst_mem_en[0] alpha = rst_mem_en[1] cpmem = rst_mem_en[2]

*Table continues on the next page...*

**IPUx\_MEM\_RST field descriptions (continued)**

Field	Description
	<p>tpm = rst_mem_en[3]</p> <p>mpm = rst_mem_en[4]</p> <p>bm = rst_mem_en[5]</p> <p>rm = rst_mem_en[6]</p> <p>dstm = rst_mem_en[7]</p> <p>dsom = rst_mem_en[8]</p> <p>lut0 = rst_mem_en[9]</p> <p>lut1 = rst_mem_en[10]</p> <p>ram_smfc = rst_mem_en[11]</p> <p>vdi_fifo2 = rst_mem_en[12]</p> <p>vdi_fifo3 = rst_mem_en[13]</p> <p>icb = rst_mem_en[14]</p> <p>vdi_fifo1 = rst_mem_en[15]</p> <p>dc_template = rst_mem_en[20]</p> <p>dmfc_rd = rst_mem_en[21]</p> <p>dmfc_wr = rst_mem_en[22]</p>

### 37.5.45 Power Modes Control Register (IPUx\_PM)

This register controls the automatic transitions of the IPU between different power modes of the SoC and handles the clock change modes.

Address: Base address + E0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	LPSR_MODE	DI1_SRMM_CLOCK_CHANGE_MODE														
W																
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CLCOK_MODE_STAT	DIO_SRM_CLOCK_CHANGE_MODE														
W																

DI0\_CLK\_PERIOD\_1                            DI0\_CLK\_PERIOD\_0

Reset    0    0    0    0    1    0    0    0    0    0    0    1    0    0    0    0

**IPUx\_PM field descriptions**

Field	Description
31 LPSR_MODE	LPSR Mode This bit indicates that the next attempt for entering low power mode is an attempt to move to LPST mode. Setting this bit by the user is essential in order to assure proper response of the IPU to the assertion of the stop request from the CCM.  1 Next low power mode will be LPSR 0 Next low power mode is not LPSR
30 DI1_SRM_CLOCK_CHANGE_MODE	SRM clock change mode When the clock is going to be changed to any new ratio other than 1:1, 1:2, 1:4. The user needs to prepare an alternate set of DI setting in the SRM.  This bit enable this mode. This bit is self cleared.  1 SRM clock change mode is enabled; the next clock change will be done by updating the DI settings from the SRM 0 SRM clock change mode is disabled.
29–23 DI1_CLK_PERIOD_1	DI1_CLK period option 1. This parameter defines the period of the clock that the DI1 works with. This parameter contains integer part (bits [6:4]) and fractional part (bits [3:0]).  Setting this value to 1.0 (default) means that the DI1 works on the fastest possible clock.  Setting a value smaller than 1.0 is not allowed.

Table continues on the next page...

## IPUx\_PM field descriptions (continued)

Field	Description
	<p>The value to be programmed to the DI1_CLK_PERIOD_1 field is equal to: Fast_freq/Target_freq Where: Target_freq = The frequency that the DI clock works with Fast_freq = fastest possible clock that the DI can work with</p>
22–16 DI1_CLK_PERIOD_0	<p>DI1_CLK period option 0. This parameter defines the period of the clock that the DI1 works with. This parameter contains integer part (bits [6:4]) and fractional part (bits [3:0]). Setting this value to 1.0 (default) means that the DI1 works on the fastest possible clock. Setting a value smaller than 1.0 is not allowed. The value to be programmed to the DI1_CLK_PERIOD_1 field is equal to: Fast_freq/Target_freq Where: Target_freq = The frequency that the DI clock works with Fast_freq = fastest possible clock that the DI can work with</p>
15 CLCOK_MODE_STAT	<p>Clock mode status This is a read only bit indicating what is the current clock mode 1 current clock mode is 1 0 current clock mode is 0</p>
14 DIO_SRM_CLOCK_CHANGE_MODE	<p>SRM clock change mode When the clock is going to be changed to any new ratio other then 1:1, 1:2, 1:4. The user needs to prepare an alternate set of DI setting in the SRM. This bit enable this mode. This bit is self cleared. 1 SRM clock change mode is enabled; the next clock change will be done by updating the DI settings from the SRM 0 SRM clock change mode is disabled.</p>
13–7 DIO_CLK_PERIOD_1	<p>DIO_CLK period option 1. This parameter defines the period of the clock that the DIO works with. This parameter contains integer part (bits [6:4]) and fractional part (bits [3:0]). Setting this value to 1.0 (default) means that the DIO works on the fastest possible clock. Setting a value smaller than 1.0 is not allowed. The value to be programmed to the DIO_CLK_PERIOD_1 field is equal to: Fast_freq/Target_freq Where: Target_freq = The frequency that the DI clock works with Fast_freq = fastest possible clock that the DI can work with</p>
DIO_CLK_PERIOD_0	<p>DIO_CLK period option 0. This parameter defines the period of the clock that the DIO works with. This parameter contains integer part (bits [6:4]) and fractional part (bits [3:0]).</p>

Table continues on the next page...

**IPUx\_PM field descriptions (continued)**

Field	Description
	<p>Setting this value to 1.0 (default) means that the DI0 works on the fastest possible clock.</p> <p>Setting a value smaller than 1.0 is not allowed.</p> <p>The value to be programmed to the DI0_CLK_PERIOD_1 field is equal to:</p> <p>Fast_freq/Target_freq</p> <p>Where:</p> <p>Target_freq = The frequency that the DI clock works with</p> <p>Fast_freq = fastest possible clock that the DI can work with</p>

**37.5.46 General Purpose Register (IPUx\_GPR)**

The register contains general purpose bits.

Address: Base address + E4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IPU_CH_BUF1_RDY1_CLR	IPU_CH_BUF1_RDY0_CLR	IPU_CH_BUF0_RDY1_CLR	IPU_CH_BUF0_RDY0_CLR	IPU_ALT_CH_BUF1_RDY1_CLR	IPU_ALT_CH_BUF1_RDY0_CLR	IPU_ALT_CH_BUF0_RDY1_CLR	IPU_ALT_CH_BUF0_RDY0_CLR	IPU_D1_CLK_CHANGE_ACK_DIS	IPU_D0_CLK_CHANGE_ACK_DIS	IPU_CH_BUF2_RDY1_CLR	IPU_CH_BUF2_RDY0_CLR				
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_GPR field descriptions**

Field	Description
31 IPU_CH_BUF1_RDY1_CLR	This bit defines the IPU_CH_BUF1_RDY1 properties. This register can be a write one to clear OR write one to set.

*Table continues on the next page...*

**IPUx\_GPR field descriptions (continued)**

Field	Description
	<p>1 writing one to a bit of this register clears this bit; <b>IPU_CH_BUF1_RDY1</b> is w1c register            0 writing one to a bit of this register sets this bit <b>IPU_CH_BUF1_RDY1</b> is w1s register</p>
30 IPU_CH_BUF1_ RDY0_CLR	<p>This bit defines the <b>IPU_CH_BUF1_RDY0</b> properties. This register can be a write one to clear OR write one to set.</p> <p>1 writing one to a bit of this register clears this bit; <b>IPU_CH_BUF1_RDY0</b> is w1c register            0 writing one to a bit of this register sets this bit <b>IPU_CH_BUF1_RDY0</b> is w1s register</p>
29 IPU_CH_BUF0_ RDY1_CLR	<p>This bit defines the <b>IPU_CH_BUF0_RDY1</b> properties. This register can be a write one to clear OR write one to set.</p> <p>1 writing one to a bit of this register clears this bit; <b>IPU_CH_BUF0_RDY1</b> is w1c register            0 writing one to a bit of this register sets this bit <b>IPU_CH_BUF0_RDY1</b> is w1s register</p>
28 IPU_CH_BUF0_ RDY0_CLR	<p>This bit defines the <b>IPU_CH_BUF0_RDY0</b> properties. This register can be a write one to clear OR write one to set.</p> <p>1 writing one to a bit of this register clears this bit; <b>IPU_CH_BUF0_RDY0</b> is w1c register            0 writing one to a bit of this register sets this bit <b>IPU_CH_BUF0_RDY0</b> is w1s register</p>
27 IPU_ALT_CH_ BUF1_RDY1_ CLR	<p>This bit defines the <b>IPU_ALT_CH_BUF1_RDY1</b> properties. This register can be a write one to clear OR write one to set.</p> <p>1 writing one to a bit of this register clears this bit; <b>IPU_ALT_CH_BUF1_RDY1</b> is w1c register            0 writing one to a bit of this register sets this bit <b>IPU_ALT_CH_BUF1_RDY1</b> is w1s register</p>
26 IPU_ALT_CH_ BUF1_RDY0_ CLR	<p>This bit defines the <b>IPU_ALT_CH_BUF1_RDY0</b> properties. This register can be a write one to clear OR write one to set.</p> <p>1 writing one to a bit of this register clears this bit; <b>IPU_ALT_CH_BUF1_RDY0</b> is w1c register            0 writing one to a bit of this register sets this bit <b>IPU_ALT_CH_BUF1_RDY0</b> is w1s register</p>
25 IPU_ALT_CH_ BUF0_RDY1_ CLR	<p>This bit defines the <b>IPU_ALT_CH_BUF0_RDY1</b> properties. This register can be a write one to clear OR write one to set.</p> <p>1 writing one to a bit of this register clears this bit; <b>IPU_ALT_CH_BUF0_RDY1</b> is w1c register            0 writing one to a bit of this register sets this bit <b>IPU_ALT_CH_BUF0_RDY1</b> is w1s register</p>
24 IPU_ALT_CH_ BUF0_RDY0_ CLR	<p>This bit defines the <b>IPU_ALT_CH_BUF0_RDY0</b> properties. This register can be a write one to clear OR write one to set.</p> <p>1 writing one to a bit of this register clears this bit; <b>IPU_ALT_CH_BUF0_RDY0</b> is w1c register            0 writing one to a bit of this register sets this bit <b>IPU_ALT_CH_BUF0_RDY0</b> is w1s register</p>
23 IPU_DI1_CLK_ CHANGE_ACK_ DIS	<p>Disable DI1's clock change mechanism.</p> <p>1 clock change mechanism is disabled. DI automatically acknowledges a clock change request            0 clock change mechanism is disabled. DI performs the clock change procedure</p>
22 IPU_D10_CLK_ CHANGE_ACK_ DIS	<p>Disable DI0's clock change mechanism.</p> <p>1 clock change mechanism is disabled. DI automatically acknowledges a clock change request            0 clock change mechanism is disabled. DI performs the clock change procedure</p>
21 IPU_CH_BUF2_ RDY1_CLR	<p>This bit defines the <b>IPU_CH_BUF2_RDY1</b> properties. This register can be a write one to clear OR write one to set.</p> <p>1 writing one to a bit of this register clears this bit; <b>IPU_CH_BUF2_RDY1</b> is w1c register            0 writing one to a bit of this register sets this bit <b>IPU_CH_BUF2_RDY1</b> is w1s register</p>

*Table continues on the next page...*

**IPUx\_GPR field descriptions (continued)**

Field	Description
20 IPU_CH_BUF2_RDY0_CLR	This bit defines the IPU_CH_BUF2_RDY0 properties. This register can be a write one to clear OR write one to set. 1 writing one to a bit of this register clears this bit; IPU_CH_BUF2_RDY0 is w1c register 0 writing one to a bit of this register sets this bit IPU_CH_BUF2_RDY0 is w1s register
IPU_GPn	IPU General Purpose bit. <i>n</i> Indicates the corresponding DMA channel number. This bits are general Read/Write bits, reserved for future use

### 37.5.47 Channel Double Buffer Mode Select 0 Register (IPUx\_CH\_DB\_MODE\_SEL0)

The register contains double buffer mode select control information for 32 IPU's DMA channels.

Address: Base address + 150h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DMA_CH_DB_MODE_SEL_31	0	DMA_CH_DB_MODE_SEL_29	DMA_CH_DB_MODE_SEL_28	DMA_CH_DB_MODE_SEL_27	DMA_CH_DB_MODE_SEL_26	DMA_CH_DB_MODE_SEL_25	DMA_CH_DB_MODE_SEL_24	DMA_CH_DB_MODE_SEL_23	DMA_CH_DB_MODE_SEL_22	DMA_CH_DB_MODE_SEL_21	DMA_CH_DB_MODE_SEL_20	DMA_CH_DB_MODE_SEL_19	DMA_CH_DB_MODE_SEL_18	DMA_CH_DB_MODE_SEL_17	0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DMA_CH_DB_MODE_SEL_15	DMA_CH_DB_MODE_SEL_14	DMA_CH_DB_MODE_SEL_13	DMA_CH_DB_MODE_SEL_12	DMA_CH_DB_MODE_SEL_11	DMA_CH_DB_MODE_SEL_10	DMA_CH_DB_MODE_SEL_9	DMA_CH_DB_MODE_SEL_8	0	0	0	0	0	0	0	0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_CH\_DB\_MODE\_SEL0 field descriptions**

Field	Description
31 DMA_CH_DB_MODE_SEL_31	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_CH\_DB\_MODE\_SEL0 field descriptions (continued)**

Field	Description
	<p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
30 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
29 DMA_CH_DB_MODE_SEL_29	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
28 DMA_CH_DB_MODE_SEL_28	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
27 DMA_CH_DB_MODE_SEL_27	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
26 DMA_CH_DB_MODE_SEL_26	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
25 DMA_CH_DB_MODE_SEL_25	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
24 DMA_CH_DB_MODE_SEL_24	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
23 DMA_CH_DB_MODE_SEL_23	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
22 DMA_CH_DB_MODE_SEL_22	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>

*Table continues on the next page...*

**IPUx\_CH\_DB\_MODE\_SEL0 field descriptions (continued)**

Field	Description
21 DMA_CH_DB_MODE_SEL_21	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
20 DMA_CH_DB_MODE_SEL_20	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
19 DMA_CH_DB_MODE_SEL_19	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
18 DMA_CH_DB_MODE_SEL_18	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
17 DMA_CH_DB_MODE_SEL_17	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
16 Reserved	This read-only field is reserved and always has the value 0. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
15 DMA_CH_DB_MODE_SEL_15	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
14 DMA_CH_DB_MODE_SEL_14	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
13 DMA_CH_DB_MODE_SEL_13	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
12 DMA_CH_DB_MODE_SEL_12	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_CH\_DB\_MODE\_SEL0 field descriptions (continued)**

Field	Description
	<p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
11 DMA_CH_DB_MODE_SEL_11	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
10 DMA_CH_DB_MODE_SEL_10	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
9 DMA_CH_DB_MODE_SEL_9	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
8 DMA_CH_DB_MODE_SEL_8	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
7–6 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
5 DMA_CH_DB_MODE_SEL_5	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
4 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
3 DMA_CH_DB_MODE_SEL_3	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
2 DMA_CH_DB_MODE_SEL_2	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>

Table continues on the next page...

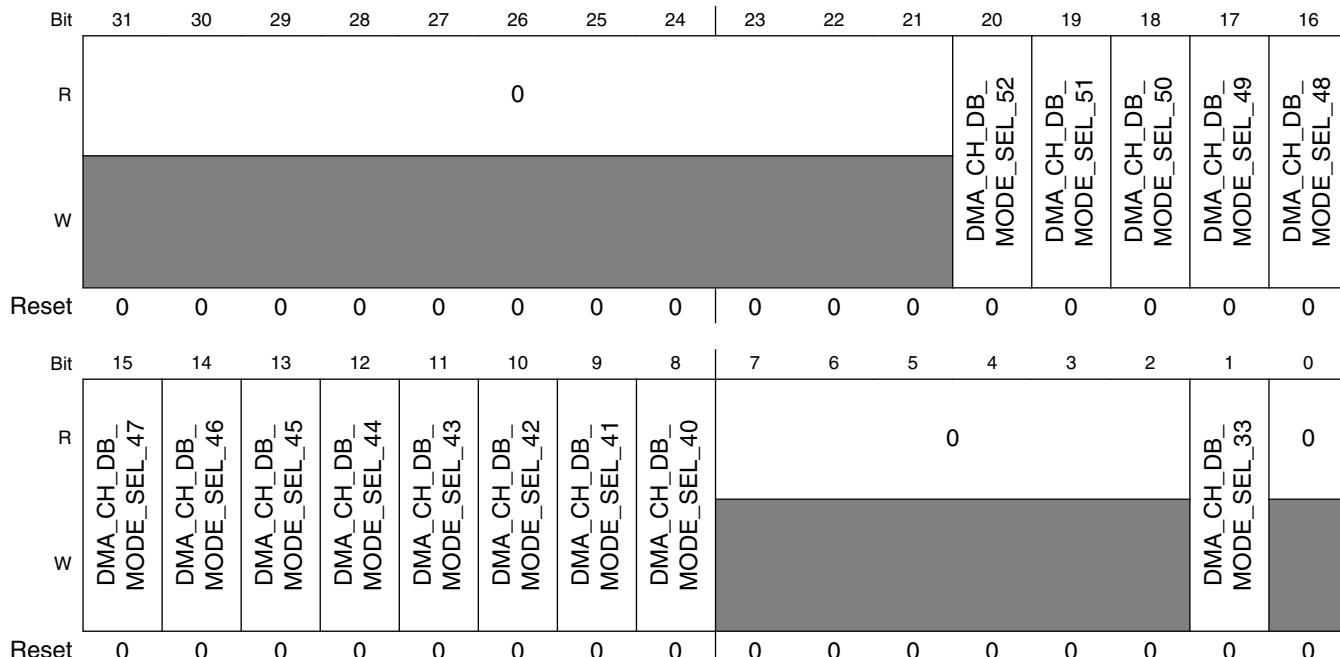
**IPUx\_CH\_DB\_MODE\_SEL0 field descriptions (continued)**

Field	Description
1 DMA_CH_DB_MODE_SEL_1	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
0 DMA_CH_DB_MODE_SEL_0	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.

**37.5.48 Channel Double Buffer Mode Select 1 Register (IPUx\_CH\_DB\_MODE\_SEL1)**

The register contains double buffer mode select control information for 32 IPU's DMA channels.

Address: Base address + 154h offset

**IPUx\_CH\_DB\_MODE\_SEL1 field descriptions**

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_CH\_DB\_MODE\_SEL1 field descriptions (continued)**

Field	Description
	0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
20 DMA_CH_DB_MODE_SEL_52	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
19 DMA_CH_DB_MODE_SEL_51	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
18 DMA_CH_DB_MODE_SEL_50	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
17 DMA_CH_DB_MODE_SEL_49	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
16 DMA_CH_DB_MODE_SEL_48	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
15 DMA_CH_DB_MODE_SEL_47	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
14 DMA_CH_DB_MODE_SEL_46	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
13 DMA_CH_DB_MODE_SEL_45	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
12 DMA_CH_DB_MODE_SEL_44	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_CH\_DB\_MODE\_SEL1 field descriptions (continued)**

Field	Description
	<p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
11 DMA_CH_DB_MODE_SEL_43	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
10 DMA_CH_DB_MODE_SEL_42	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
9 DMA_CH_DB_MODE_SEL_41	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
8 DMA_CH_DB_MODE_SEL_40	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
7–2 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
1 DMA_CH_DB_MODE_SEL_33	<p>Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>
0 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.</p>

### 37.5.49 Alternate Channel Double Buffer Mode Select 0 Register (IPUx\_ALT\_CH\_DB\_MODE\_SEL0)

The register contains double buffer mode select control information for 32 IPU's DMA channels.

Address: Base address + 168h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0		DMA_CH_ALT_DB_MODE_SEL_29		0			DMA_MODE_SEL_24					0			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									DMA_CH_ALT_DB_MODE_SEL_7	DMA_CH_ALT_DB_MODE_SEL_6	DMA_CH_ALT_DB_MODE_SEL_5	DMA_CH_ALT_DB_MODE_SEL_4			0	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_ALT\_CH\_DB\_MODE\_SEL0 field descriptions**

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.  0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
29 DMA_CH_ALT_DB_MODE_SEL_29	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.  0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
28–25 Reserved	This read-only field is reserved and always has the value 0.  0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.

Table continues on the next page...

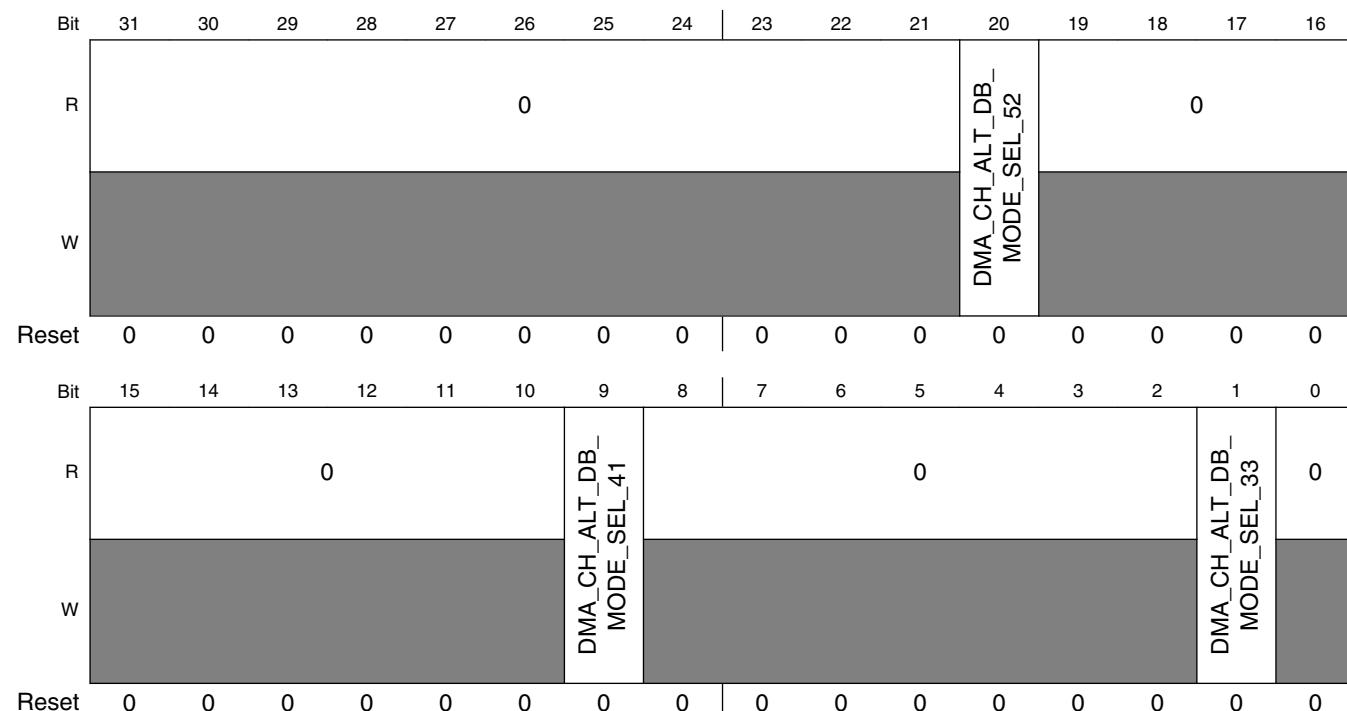
**IPUx\_ALT\_CH\_DB\_MODE\_SEL0 field descriptions (continued)**

Field	Description
24 DMA_CH_ALT_ DB_MODE_ SEL_24	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
23–8 Reserved	This read-only field is reserved and always has the value 0. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
7 DMA_CH_ALT_ DB_MODE_ SEL_7	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
6 DMA_CH_ALT_ DB_MODE_ SEL_6	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
5 DMA_CH_ALT_ DB_MODE_ SEL_5	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
4 DMA_CH_ALT_ DB_MODE_ SEL_4	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
Reserved	This read-only field is reserved and always has the value 0. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.

### 37.5.50 Alternate Channel Double Buffer Mode Select1 Register (IPUx\_ALT\_CH\_DB\_MODE\_SEL1)

The register contains double buffer mode select control information for 32 IPU's DMA channels.

Address: Base address + 16Ch offset



**IPUx\_ALT\_CH\_DB\_MODE\_SEL1 field descriptions**

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
20 DMA_CH_ALT_DB_MODE_SEL_52	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.  0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
19–10 Reserved	This read-only field is reserved and always has the value 0.  0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.

Table continues on the next page...

**IPUx\_ALT\_CH\_DB\_MODE\_SEL1 field descriptions (continued)**

Field	Description
9 DMA_CH_ALT_DB_MODE_SEL_41	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
8–2 Reserved	This read-only field is reserved and always has the value 0. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
1 DMA_CH_ALT_DB_MODE_SEL_33	Double Buffer Mode Select. This bit indicates if a double buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.
0 Reserved	This read-only field is reserved and always has the value 0. 0 Double buffer is not used for this channel. 1 Double buffer is used for this channel.

### 37.5.51 Alternate Channel Triple Buffer Mode Select 0 Register (IPUx\_ALT\_CH\_TRB\_MODE\_SEL0)

The register contains triple buffer mode select control information for 32 IPU's DMA channels.

When the channel is configured for triple buffer mode. The double buffer mode settings configured on the corresponding DB\_MODE\_SEL bit are overridden.

- Hide VPU\_SUB\_FRAME\_SYNC for all versions
- Show VPU\_SUB\_FRAME\_SYNC for IPUv3H version.
- The table below tagged with other settings (like IPU3M\_only) should be hidden in IPUv3H version.
- This requires some sophisticated conditional tag settings

Address: Base address + 178h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			0	DMA_CH_TRB_MODE_SEL_28	DMA_CH_TRB_MODE_SEL_27		0		DMA_CH_TRB_MODE_SEL_23	0	DMA_CH_TRB_MODE_SEL_21		0		0	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		DMA_CH_TRB_MODE_SEL_13	0		DMA_CH_TRB_MODE_SEL_10		DMA_CH_TRB_MODE_SEL_9		DMA_CH_TRB_MODE_SEL_8		0				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_ALT\_CH\_TRB\_MODE\_SEL0 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.  0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.
28 DMA_CH_TRB_MODE_SEL_28	Triple Buffer Mode Select. This bit indicates if a triple buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.  0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.
27 DMA_CH_TRB_MODE_SEL_27	Triple Buffer Mode Select. This bit indicates if a triple buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.  0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.
26–24 Reserved	This read-only field is reserved and always has the value 0.  0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.
23 DMA_CH_TRB_MODE_SEL_23	Triple Buffer Mode Select. This bit indicates if a triple buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.  0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.
22 Reserved	This read-only field is reserved and always has the value 0.  0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.
21 DMA_CH_TRB_MODE_SEL_21	Triple Buffer Mode Select. This bit indicates if a triple buffer is used for this channel. <i>n</i> Indicates the corresponding DMA channel number.  0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.
20–14 Reserved	This read-only field is reserved and always has the value 0.  0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.

Table continues on the next page...

**IPUx\_ALT\_CH\_TRB\_MODE\_SEL0 field descriptions (continued)**

Field	Description
13 DMA_CH_TRB_MODE_SEL_13	<p>Triple Buffer Mode Select. This bit indicates if a triple buffer is used for this channel.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.</p>
12–11 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.</p>
10 DMA_CH_TRB_MODE_SEL_10	<p>Triple Buffer Mode Select. This bit indicates if a triple buffer is used for this channel.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.</p>
9 DMA_CH_TRB_MODE_SEL_9	<p>Triple Buffer Mode Select. This bit indicates if a triple buffer is used for this channel.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.</p>
8 DMA_CH_TRB_MODE_SEL_8	<p>Triple Buffer Mode Select. This bit indicates if a triple buffer is used for this channel.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.</p>
Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Triple buffer is not used for this channel. 1 Triple buffer is used for this channel.</p>

### 37.5.52 Interrupt Status Register 1 (IPUx\_INT\_STAT\_1)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of EOF (end of frame) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 200h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_EOF_31	0	IDMAC_EOF_29	IDMAC_EOF_28	IDMAC_EOF_27	IDMAC_EOF_26	IDMAC_EOF_25	IDMAC_EOF_24	IDMAC_EOF_23	IDMAC_EOF_22	IDMAC_EOF_21	IDMAC_EOF_20	IDMAC_EOF_19	IDMAC_EOF_18	IDMAC_EOF_17	0
W	w1c		w1c													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_EOF_15	IDMAC_EOF_14	IDMAC_EOF_13	IDMAC_EOF_12	IDMAC_EOF_11	IDMAC_EOF_10	IDMAC_EOF_9	IDMAC_EOF_8	0	0	IDMAC_EOF_5	0	IDMAC_EOF_3	IDMAC_EOF_2	IDMAC_EOF_1	IDMAC_EOF_0
W	w1c		w1c		w1c	w1c	w1c	w1c	w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_STAT\_1 field descriptions

Field	Description
31 IDMAC_EOF_31	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_STAT\_1 field descriptions (continued)**

Field	Description
	0 Interrupt is cleared. 1 Interrupt is requested.
30 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
29 IDMAC_EOF_29	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
28 IDMAC_EOF_28	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
27 IDMAC_EOF_27	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
26 IDMAC_EOF_26	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
25 IDMAC_EOF_25	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
24 IDMAC_EOF_24	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
23 IDMAC_EOF_23	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
22 IDMAC_EOF_22	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.

Table continues on the next page...

**IPUx\_INT\_STAT\_1 field descriptions (continued)**

Field	Description
21 IDMAC_EOF_21	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
20 IDMAC_EOF_20	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
19 IDMAC_EOF_19	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
18 IDMAC_EOF_18	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
17 IDMAC_EOF_17	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
16 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
15 IDMAC_EOF_15	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
14 IDMAC_EOF_14	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
13 IDMAC_EOF_13	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
12 IDMAC_EOF_12	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_1 field descriptions (continued)**

Field	Description
	0 Interrupt is cleared. 1 Interrupt is requested.
11 IDMAC_EOF_11	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
10 IDMAC_EOF_10	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
9 IDMAC_EOF_9	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
8 IDMAC_EOF_8	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
7–6 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
5 IDMAC_EOF_5	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
4 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
3 IDMAC_EOF_3	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
2 IDMAC_EOF_2	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
1 IDMAC_EOF_1	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n.

Table continues on the next page...

**IPUx\_INT\_STAT\_1 field descriptions (continued)**

Field	Description
	<p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
0 IDMAC_EOF_0	<p>End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

### 37.5.53 Interrupt Status Register2 (IPUx\_INT\_STAT\_2)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of EOF (end of frame) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 204h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0			IDMAC_EOF_52				
W												IDMAC_EOF_51				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_EOF_47	IDMAC_EOF_46	IDMAC_EOF_45	IDMAC_EOF_44	IDMAC_EOF_43	IDMAC_EOF_42	IDMAC_EOF_41	IDMAC_EOF_40				0		IDMAC_EOF_33		0
W	w1c						w1c									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IPUx\_INT\_STAT\_2 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.

Table continues on the next page...

**IPUx\_INT\_STAT\_2 field descriptions (continued)**

Field	Description
20 IDMAC_EOF_52	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
19 IDMAC_EOF_51	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
18 IDMAC_EOF_50	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
17 IDMAC_EOF_49	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
16 IDMAC_EOF_48	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
15 IDMAC_EOF_47	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
14 IDMAC_EOF_46	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
13 IDMAC_EOF_45	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
12 IDMAC_EOF_44	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_2 field descriptions (continued)**

Field	Description
11 IDMAC_EOF_43	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
10 IDMAC_EOF_42	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
9 IDMAC_EOF_41	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
8 IDMAC_EOF_40	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
7–2 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
1 IDMAC_EOF_33	End of Frame of Channel interrupt. This bit is the status bit of End Of Frame of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
0 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.

### 37.5.54 Interrupt Status Register 3 (IPUx\_INT\_STAT\_3)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of NFACK (New Frame Ack) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 208h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_NFACK_31	0	IDMAC_NFACK_29	IDMAC_NFACK_28	IDMAC_NFACK_27	IDMAC_NFACK_26	IDMAC_NFACK_25	IDMAC_NFACK_24	IDMAC_NFACK_23	IDMAC_NFACK_22	IDMAC_NFACK_21	IDMAC_NFACK_20	IDMAC_NFACK_19	IDMAC_NFACK_18	IDMAC_NFACK_17	0
W	w1c		w1c													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_NFACK_15	IDMAC_NFACK_14	IDMAC_NFACK_13	IDMAC_NFACK_12	IDMAC_NFACK_11	IDMAC_NFACK_10	IDMAC_NFACK_9	IDMAC_NFACK_8	0		IDMAC_NFACK_5	0	IDMAC_NFACK_3	IDMAC_NFACK_2	IDMAC_NFACK_1	IDMAC_NFACK_0
W	w1c			w1c		w1c	w1c	w1c	w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_STAT\_3 field descriptions

Field	Description
31 IDMAC_NFACK_31	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n.  n Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
30 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
29 IDMAC_NFACK_29	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n.  n Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_STAT\_3 field descriptions (continued)**

Field	Description
	0 Interrupt is cleared. 1 Interrupt is requested.
28 IDMAC_NFACK_28	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
27 IDMAC_NFACK_27	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
26 IDMAC_NFACK_26	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
25 IDMAC_NFACK_25	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
24 IDMAC_NFACK_24	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
23 IDMAC_NFACK_23	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
22 IDMAC_NFACK_22	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
21 IDMAC_NFACK_21	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
20 IDMAC_NFACK_20	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_STAT\_3 field descriptions (continued)**

Field	Description
	0 Interrupt is cleared. 1 Interrupt is requested.
19 IDMAC_NFACK_19	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
18 IDMAC_NFACK_18	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
17 IDMAC_NFACK_17	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
16 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
15 IDMAC_NFACK_15	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
14 IDMAC_NFACK_14	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
13 IDMAC_NFACK_13	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
12 IDMAC_NFACK_12	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
11 IDMAC_NFACK_11	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.

Table continues on the next page...

**IPUx\_INT\_STAT\_3 field descriptions (continued)**

Field	Description
10 IDMAC_NFACK_10	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
9 IDMAC_NFACK_9	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
8 IDMAC_NFACK_8	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
7–6 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
5 IDMAC_NFACK_5	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
4 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
3 IDMAC_NFACK_3	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
2 IDMAC_NFACK_2	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
1 IDMAC_NFACK_1	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
0 IDMAC_NFACK_0	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_3 field descriptions (continued)**

Field	Description
	0 Interrupt is cleared. 1 Interrupt is requested.

**37.5.55 Interrupt Status Register 4 (IPUx\_INT\_STAT\_4)**

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of NFACK (New Frame Ack) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 20Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0			IDMAC_NFACK_52	IDMAC_NFACK_51	IDMAC_NFACK_50	IDMAC_NFACK_49	IDMAC_NFACK_48
W												w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_NFACK_47	IDMAC_NFACK_46	IDMAC_NFACK_45	IDMAC_NFACK_44	IDMAC_NFACK_43	IDMAC_NFACK_42	IDMAC_NFACK_41	IDMAC_NFACK_40				0		IDMAC_NFACK_33		0
W	w1c						w1c									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_STAT\_4 field descriptions**

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
20 IDMAC_NFACK_52	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. n Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_STAT\_4 field descriptions (continued)**

Field	Description
	0 Interrupt is cleared. 1 Interrupt is requested.
19 IDMAC_NFACK_51	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
18 IDMAC_NFACK_50	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
17 IDMAC_NFACK_49	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
16 IDMAC_NFACK_48	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
15 IDMAC_NFACK_47	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
14 IDMAC_NFACK_46	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
13 IDMAC_NFACK_45	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
12 IDMAC_NFACK_44	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
11 IDMAC_NFACK_43	Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_4 field descriptions (continued)**

Field	Description
	<p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
10 IDMAC_NFACK_42	<p>Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
9 IDMAC_NFACK_41	<p>Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
8 IDMAC_NFACK_40	<p>Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
7–2 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
1 IDMAC_NFACK_33	<p>Enable New Frame Ack of Channel interrupt. This bit is the status bits of New Frame Ack of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
0 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

### 37.5.56 Interrupt Status Register 5 (IPUx\_INT\_STAT\_5)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of the New-frame before end-of-frame indication (NFB4EOF\_ERR) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 210h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_NFB4EOF_ERR_31	0	IDMAC_NFB4EOF_ERR_29	IDMAC_NFB4EOF_ERR_28	IDMAC_NFB4EOF_ERR_27	IDMAC_NFB4EOF_ERR_26	IDMAC_NFB4EOF_ERR_25	IDMAC_NFB4EOF_ERR_24	IDMAC_NFB4EOF_ERR_23	IDMAC_NFB4EOF_ERR_22	IDMAC_NFB4EOF_ERR_21	IDMAC_NFB4EOF_ERR_20	IDMAC_NFB4EOF_ERR_19	IDMAC_NFB4EOF_ERR_18	IDMAC_NFB4EOF_ERR_17	0
W	w1c															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_NFB4EOF_ERR_15	IDMAC_NFB4EOF_ERR_14	IDMAC_NFB4EOF_ERR_13	IDMAC_NFB4EOF_ERR_12	IDMAC_NFB4EOF_ERR_11	IDMAC_NFB4EOF_ERR_10	IDMAC_NFB4EOF_ERR_9	IDMAC_NFB4EOF_ERR_8	0	0	0	0	IDMAC_NFB4EOF_ERR_3	IDMAC_NFB4EOF_ERR_2	IDMAC_NFB4EOF_ERR_1	IDMAC_NFB4EOF_ERR_0
W	w1c															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_STAT\_5 field descriptions**

Field	Description
31 IDMAC_ NFB4EOF_ERR_31	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
30 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
29 IDMAC_ NFB4EOF_ERR_29	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
28 IDMAC_ NFB4EOF_ERR_28	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
27 IDMAC_ NFB4EOF_ERR_27	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
26 IDMAC_ NFB4EOF_ERR_26	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
25 IDMAC_ NFB4EOF_ERR_25	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
24 IDMAC_ NFB4EOF_ERR_24	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_5 field descriptions (continued)**

Field	Description
23 IDMAC_ NFB4EOF_ERR_23	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
22 IDMAC_ NFB4EOF_ERR_22	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
21 IDMAC_ NFB4EOF_ERR_21	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
20 IDMAC_ NFB4EOF_ERR_20	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
19 IDMAC_ NFB4EOF_ERR_19	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
18 IDMAC_ NFB4EOF_ERR_18	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
17 IDMAC_ NFB4EOF_ERR_17	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
16 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.

Table continues on the next page...

**IPUx\_INT\_STAT\_5 field descriptions (continued)**

Field	Description
15 IDMAC_ NFB4EOF_ERR_15	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
14 IDMAC_ NFB4EOF_ERR_14	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
13 IDMAC_ NFB4EOF_ERR_13	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
12 IDMAC_ NFB4EOF_ERR_12	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
11 IDMAC_ NFB4EOF_ERR_11	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
10 IDMAC_ NFB4EOF_ERR_10	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
9 IDMAC_ NFB4EOF_ERR_9	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
8 IDMAC_ NFB4EOF_ERR_8	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.

Table continues on the next page...

**IPUx\_INT\_STAT\_5 field descriptions (continued)**

Field	Description
7–6 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
5 IDMAC_ NFB4EOF_ERR_5	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
4 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
3 IDMAC_ NFB4EOF_ERR_3	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
2 IDMAC_ NFB4EOF_ERR_2	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
1 IDMAC_ NFB4EOF_ERR_1	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
0 IDMAC_ NFB4EOF_ERR_0	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.

### 37.5.57 Interrupt Status Register 6 (IPUx\_INT\_STAT\_6)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of the New-frame before end-of-frame indication (NFB4EOF\_ERR) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 214h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0			IDMAC_NFB4EOF_ERR_52	IDMAC_NFB4EOF_ERR_51	IDMAC_NFB4EOF_ERR_50	IDMAC_NFB4EOF_ERR_49	IDMAC_NFB4EOF_ERR_48
W											w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_NFB4EOF_ERR_47	IDMAC_NFB4EOF_ERR_46	IDMAC_NFB4EOF_ERR_45	IDMAC_NFB4EOF_ERR_44	IDMAC_NFB4EOF_ERR_43	IDMAC_NFB4EOF_ERR_42	IDMAC_NFB4EOF_ERR_41	IDMAC_NFB4EOF_ERR_40				0		IDMAC_NFB4EOF_ERR_33		0
W	w1c						w1c									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_STAT\_6 field descriptions**

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
20 IDMAC_ NFB4EOF_ERR_ 52	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
19 IDMAC_ NFB4EOF_ERR_ 51	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
18 IDMAC_ NFB4EOF_ERR_ 50	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
17 IDMAC_ NFB4EOF_ERR_ 49	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
16 IDMAC_ NFB4EOF_ERR_ 48	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
15 IDMAC_ NFB4EOF_ERR_ 47	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
14 IDMAC_ NFB4EOF_ERR_ 46	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.

Table continues on the next page...

**IPUx\_INT\_STAT\_6 field descriptions (continued)**

Field	Description
13 IDMAC_ NFB4EOF_ERR_ 45	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
12 IDMAC_ NFB4EOF_ERR_ 44	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
11 IDMAC_ NFB4EOF_ERR_ 43	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
10 IDMAC_ NFB4EOF_ERR_ 42	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
9 IDMAC_ NFB4EOF_ERR_ 41	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
8 IDMAC_ NFB4EOF_ERR_ 40	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
7–2 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is cleared. 1 Interrupt is requested.
1 IDMAC_ NFB4EOF_ERR_ 33	New Frame before end-of-frame error indication of Channel interrupt. This bit is the status bit of New Frame before end-of-frame error interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number. 0 Interrupt is cleared. 1 Interrupt is requested.
0 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_6 field descriptions (continued)**

Field	Description
	0 Interrupt is cleared. 1 Interrupt is requested.

**37.5.58 Interrupt Status Register7 1 (IPUx\_INT\_STAT\_7)**

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of the End-of-Scroll indication (EOS) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 218h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_EOS_EN_31	0	IDMAC_EOS_EN_29	IDMAC_EOS_EN_28	IDMAC_EOS_EN_27	IDMAC_EOS_EN_26	IDMAC_EOS_EN_25	IDMAC_EOS_EN_24	IDMAC_EOS_EN_23	0	0	0	IDMAC_EOS_EN_19	0	0	0
W	w1c		w1c	w1c	w1c	w1c	w1c	w1c					w1c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_STAT\_7 field descriptions**

Field	Description
31 IDMAC_EOS_ EN_31	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
30 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
29 IDMAC_EOS_ EN_29	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
28 IDMAC_EOS_ EN_28	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
27 IDMAC_EOS_ EN_27	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
26 IDMAC_EOS_ EN_26	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
25 IDMAC_EOS_ EN_25	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
24 IDMAC_EOS_ EN_24	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

Table continues on the next page...

**IPUx\_INT\_STAT\_7 field descriptions (continued)**

Field	Description
23 IDMAC_EOS_ EN_23	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p>n Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
22–20 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
19 IDMAC_EOS_ EN_19	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p>n Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

### 37.5.59 Interrupt Status Register 8 (IPUx\_INT\_STAT\_8)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. All the status bits of the End of Scroll indication (EOS) of DMA Channels [63:32] can be found in this register.

Address: Base address + 21Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0			IDMAC_EOS_EN_52			0	
W												w1c	w1c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0	IDMAC_EOS_EN_44	IDMAC_EOS_EN_43	IDMAC_EOS_EN_42	IDMAC_EOS_EN_41			0		IDMAC_EOS_EN_33		0	
W				w1c		w1c	w1c	w1c					w1c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_STAT\_8 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_8 field descriptions (continued)**

Field	Description
	<p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
20 IDMAC_EOS_ EN_52	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
19 IDMAC_EOS_ EN_51	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
18–13 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
12 IDMAC_EOS_ EN_44	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
11 IDMAC_EOS_ EN_43	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
10 IDMAC_EOS_ EN_42	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
9 IDMAC_EOS_ EN_41	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
8–2 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

*Table continues on the next page...*

**IPUx\_INT\_STAT\_8 field descriptions (continued)**

Field	Description
1 IDMAC_EOS_ EN_33	<p>End of Scroll indication of Channel interrupt. This bit is the status bit of End of Scroll interrupt of Channel #n.</p> <p>n Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
0 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

### 37.5.60 Interrupt Status Register 9 (IPUx\_INT\_STAT\_9)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. This register holds the error interrupt indications coming from different modules within All the bits in this register are write one to clear.

Address: Base address + 220h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	CSI1_PUPE	CSI0_PUPE	0	IC_VF_BUF_OVF	IC_ENC_BUF_OVF	IC_BAYER_BUF_OVF										0
W	w1c	w1c		w1c	w1c	w1c										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							VDL FIFO1_OVF
W																w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_STAT\_9 field descriptions**

Field	Description
31 CSI1_PUPE	<p>CSI1_PUPE - CSI1 parameters update error interrupt.</p> <p>This bit indicates on an interrupt that is a result of an error generated by the CSI1. The error is generated in case where new frame arrived from the CSI1 before the completion of the CSI1's parameters update by the SRM</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
30 CSI0_PUPE	<p>CSI0_PUPE - CSI0 parameters update error interrupt.</p> <p>This bit indicates on an interrupt that is a result of an error generated by the CSI0. The error is generated in case where new frame arrived from the CSI0 before the completion of the CSI0's parameters update by the SRM</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
29 Reserved	This read-only field is reserved and always has the value 0.
28 IC_VF_BUF_OVF	<p>This bit indicates on an interrupt that is a result of the IC Buffer overflow for view finder coming from the IC. The user needs to write 1 to this bit in order to clear it.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
27 IC_ENC_BUF_OVF	<p>This bit indicates on an interrupt that is a result of the IC Buffer overflow for encoding coming from the IC. The user needs to write 1 to this bit in order to clear it.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
26 IC_BAYER_BUF_OVF	<p>This bit indicates on an interrupt that is a result of the IC Buffer overflow for Bayer coming from the IC. The user needs to write 1 to this bit in order to clear it.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
25–1 Reserved	This read-only field is reserved and always has the value 0.
0 VDI_FIFO1_OVF	<p>FIFO1 overflow Interrupt1</p> <p>The VDIC generate FIFO1 overflow interrupt1 when write pointer of FIFO1 overrun read pointer.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

### 37.5.61 Interrupt Status Register 10 (IPUx\_INT\_STAT\_10)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. This register holds error interrupt indications coming from different modules within All the bits in this register are write one to clear.

Address: Base address + 224h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	AXIR_ERR	AXIW_ERR	NON_PRIVILEGED_ACC_ERR	0	IC_BAYER_FRM_LOST_ERR	IC_ENC_FRM_LOST_ERR	IC_VF_FRM_LOST_ERR	0	D11_TIME_OUT_ERR	D10_TIME_OUT_ERR	D11_SYNC_DISP_ERR	D10_SYNC_DISP_ERR	DC_TEARING_ERR_6	DC_TEARING_ERR_2	DC_TEARING_ERR_1
W		w1c	w1c	w1c		w1c	w1c	w1c		w1c	w1c	w1c	w1c	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

## IPU Memory Map/Register Definition

Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R								0						SMFC3_FRM_LOST	SMFC2_FRM_LOST	SMFC1_FRM_LOST	SMFC0_FRM_LOST
W														w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

### IPUx\_INT\_STAT\_10 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30 AXIR_ERR	This bit indicates on an interrupt that is a result of AXI read access resulted with error response. The user needs to write 1 to this bit in order to clear it.  0 Interrupt is cleared. 1 Interrupt is requested.
29 AXIW_ERR	This bit indicates on an interrupt that is a result of AXI write access resulted with error response. The user needs to write 1 to this bit in order to clear it.  0 Interrupt is cleared. 1 Interrupt is requested.
28 NON_PRIVILEGED_ACC_ERR	Non Privileged Access Error interrupt.  This bit indicates on an interrupt that is a result of access the CPMEM or the DP memory in user mode  0 Interrupt is cleared. 1 Interrupt is requested.
27 Reserved	This read-only field is reserved and always has the value 0.
26 IC_BAYER_FRM_LOST_ERR	This bit indicates on an interrupt that is a result of IC's Bayer frame lost.  0 Interrupt is disabled. 1 Interrupt is enabled.
25 IC_ENC_FRM_LOST_ERR	This bit indicates on an interrupt that is a result of IC's encoding frame lost.

Table continues on the next page...

**IPUx\_INT\_STAT\_10 field descriptions (continued)**

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
24 IC_VF_FRM_ LOST_ERR	This bit indicates on an interrupt that is a result of IC's view finder frame lost. 0 Interrupt is disabled. 1 Interrupt is enabled.
23 Reserved	This read-only field is reserved and always has the value 0.
22 DI1_TIME_OUT_ ERR	DI1 time out error interrupt This bit indicates on the interrupt that is a result of a time out error during a read access via DI1
21 DI0_TIME_OUT_ ERR	DI0 time out error interrupt This bit indicates on the interrupt that is a result of a time out error during a read access via DI0
20 DI1_SYNC_ DISP_ERR	DI1 Synchronous display error interrupt This bit indicates on the interrupt that is a result of an error during access to a synchronous display via DI1
19 DI0_SYNC_ DISP_ERR	DI0 Synchronous display error interrupt This bit indicates on the interrupt that is a result of an error during access to a synchronous display via DI0
18 DC_TEARING_ ERR_6	Tearing Error #6 interrupt This bit indicates on the interrupt that is a result of tearing error while the anti tearing mechanism is activated for DC channel 6
17 DC_TEARING_ ERR_2	Tearing Error #2 interrupt This bit indicates on the interrupt that is a result of tearing error while the anti tearing mechanism is activated for DC channel 2
16 DC_TEARING_ ERR_1	Tearing Error #1 interrupt This bit indicates on the interrupt that is a result of tearing error while the anti tearing mechanism is activated for DC channel 1
15–4 Reserved	This read-only field is reserved and always has the value 0.
3 SMFC3_FRM_ LOST	Frame Lost of SMFC channel 3 interrupt. This bit indicates on an interrupt that is a result of a result of a Frame Lost of SMFC channel 3 0 Interrupt is cleared. 1 Interrupt is requested.
2 SMFC2_FRM_ LOST	Frame Lost of SMFC channel 2 interrupt. This bit indicates on an interrupt that is a result of a result of a Frame Lost of SMFC channel 2 0 Interrupt is cleared. 1 Interrupt is requested.
1 SMFC1_FRM_ LOST	Frame Lost of SMFC channel 1 interrupt. This bit indicates on an interrupt that is a result of a result of a Frame Lost of SMFC channel 1 0 Interrupt is cleared. 1 Interrupt is requested.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_10 field descriptions (continued)**

Field	Description
0 SMFC0_FRM_LOST	Frame Lost of SMFC channel 0 interrupt. This bit indicates on an interrupt that is a result of a result of a Frame Lost of SMFC channel 0 0 Interrupt is cleared. 1 Interrupt is requested.

**37.5.62 Interrupt Status Register 11 (IPUx\_INT\_STAT\_11)**

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of the end-of-band indication (EOBND) of DMA Channels interrupts [31:0] can be found in this register.

- Hide VDOA\_SYNC for all versions
- Show VDOA\_SYNC for IPUv3H version.
- The table below tagged with other settings (like IPU3M\_only) should be hidden in IPUv3H version.

Address: Base address + 228h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	IDMAC_EOBND_EN_26	IDMAC_EOBND_EN_25	0	0	IDMAC_EOBND_EN_22	IDMAC_EOBND_EN_21	IDMAC_EOBND_EN_20	0	0	0	0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0			IDMAC_EOBND_EN_12	IDMAC_EOBND_EN_11				0		IDMAC_EOBND_EN_5	0	IDMAC_EOBND_EN_3	IDMAC_EOBND_EN_2	IDMAC_EOBND_EN_1	IDMAC_EOBND_EN_0
W				w1c	w1c					w1c		w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_STAT\_11 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
26 IDMAC_EOBND_EN_26	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
25 IDMAC_EOBND_EN_25	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
24–23 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
22 IDMAC_EOBND_EN_22	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
21 IDMAC_EOBND_EN_21	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.

Table continues on the next page...

**IPUx\_INT\_STAT\_11 field descriptions (continued)**

Field	Description
	<p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
20 IDMAC_EOBND_ EN_20	<p>end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
19–13 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
12 IDMAC_EOBND_ EN_12	<p>end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
11 IDMAC_EOBND_ EN_11	<p>end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
10–6 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
5 IDMAC_EOBND_ EN_5	<p>end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
4 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
3 IDMAC_EOBND_ EN_3	<p>end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

Table continues on the next page...

**IPUx\_INT\_STAT\_11 field descriptions (continued)**

Field	Description
2 IDMAC_EOBND_ EN_2	<p>end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
1 IDMAC_EOBND_ EN_1	<p>end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
0 IDMAC_EOBND_ EN_0	<p>end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

### 37.5.63 Interrupt Status Register 12 (IPUx\_INT\_STAT\_12)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of the end-of-band indication (EOBND) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 22Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0					IDMAC_EOBND_EN_50	IDMAC_EOBND_EN_49	IDMAC_EOBND_EN_48
W														w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_EOBND_EN_47	IDMAC_EOBND_EN_46	IDMAC_EOBND_EN_45						0							
W	w1c	w1c	w1c													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUX\_INT\_STAT\_12 field descriptions**

Field	Description
31–19 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
18 IDMAC_EOBND_ EN_50	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
17 IDMAC_EOBND_ EN_49	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
16 IDMAC_EOBND_ EN_48	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
15 IDMAC_EOBND_ EN_47	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
14 IDMAC_EOBND_ EN_46	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
13 IDMAC_EOBND_ EN_45	end-of-band indication of Channel interrupt. This bit is the status bit of end-of-band interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.

### 37.5.64 Interrupt Status Register 13 (IPUx\_INT\_STAT\_13)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of the Threshold crossing indication (TH) of DMA Channels interrupts [31:0] can be found in this register.

Address: Base address + 230h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_TH_31	0	IDMAC_TH_29	IDMAC_TH_28	IDMAC_TH_27	IDMAC_TH_26	IDMAC_TH_25	IDMAC_TH_24	IDMAC_TH_23	IDMAC_TH_22	IDMAC_TH_21	IDMAC_TH_20	IDMAC_TH_19	IDMAC_TH_18	IDMAC_TH_17	0
W	w1c		w1c													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_TH_15	IDMAC_TH_14	IDMAC_TH_13	IDMAC_TH_12	IDMAC_TH_11	IDMAC_TH_10	IDMAC_TH_9	IDMAC_TH_8	0		IDMAC_TH_5	0	IDMAC_TH_3	IDMAC_TH_2	IDMAC_TH_1	IDMAC_TH_0
W	w1c			w1c		w1c	w1c	w1c	w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_STAT\_13 field descriptions

Field	Description
31 IDMAC_TH_31	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.

Table continues on the next page...

**IPUx\_INT\_STAT\_13 field descriptions (continued)**

Field	Description
30 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
29 IDMAC_TH_29	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
28 IDMAC_TH_28	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
27 IDMAC_TH_27	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
26 IDMAC_TH_26	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
25 IDMAC_TH_25	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
24 IDMAC_TH_24	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
23 IDMAC_TH_23	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
22 IDMAC_TH_22	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_13 field descriptions (continued)**

Field	Description
	<p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
21 IDMAC_TH_21	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
20 IDMAC_TH_20	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
19 IDMAC_TH_19	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
18 IDMAC_TH_18	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
17 IDMAC_TH_17	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
16 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
15 IDMAC_TH_15	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
14 IDMAC_TH_14	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.</p> <p><i>n</i> Indicates the corresponding DMA channel number.</p>

*Table continues on the next page...*

**IPUx\_INT\_STAT\_13 field descriptions (continued)**

Field	Description
	<p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
13 IDMAC_TH_13	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
12 IDMAC_TH_12	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
11 IDMAC_TH_11	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
10 IDMAC_TH_10	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
9 IDMAC_TH_9	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
8 IDMAC_TH_8	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
7–6 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
5 IDMAC_TH_5	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

Table continues on the next page...

**IPUx\_INT\_STAT\_13 field descriptions (continued)**

Field	Description
4 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
3 IDMAC_TH_3	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
2 IDMAC_TH_2	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
1 IDMAC_TH_1	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.
0 IDMAC_TH_0	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.  0 Interrupt is cleared. 1 Interrupt is requested.

### 37.5.65 Interrupt Status Register 14 (IPUx\_INT\_STAT\_14)

IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of the Threshold crossing indication (TH) of DMA Channels interrupts [63:32] can be found in this register.

Address: Base address + 234h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0			IDMAC_TH_52	IDMAC_TH_51	IDMAC_TH_50	IDMAC_TH_49	IDMAC_TH_48
W												w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_TH_47	IDMAC_TH_46	IDMAC_TH_45	IDMAC_TH_44	IDMAC_TH_43	IDMAC_TH_42	IDMAC_TH_41	IDMAC_TH_40				0		IDMAC_TH_33		0
W	w1c						w1c									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_INT\_STAT\_14 field descriptions

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 Interrupt is cleared. 1 Interrupt is requested.
20 IDMAC_TH_52	Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n.  <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_INT\_STAT\_14 field descriptions (continued)**

Field	Description
	<p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
19 IDMAC_TH_51	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
18 IDMAC_TH_50	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
17 IDMAC_TH_49	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
16 IDMAC_TH_48	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
15 IDMAC_TH_47	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
14 IDMAC_TH_46	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
13 IDMAC_TH_45	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
12 IDMAC_TH_44	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p>

*Table continues on the next page...*

**IPUx\_INT\_STAT\_14 field descriptions (continued)**

Field	Description
	<p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
11 IDMAC_TH_43	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
10 IDMAC_TH_42	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
9 IDMAC_TH_41	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
8 IDMAC_TH_40	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
7–2 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
1 IDMAC_TH_33	<p>Threshold crossing indication of Channel interrupt. This bit is the status bit of Threshold crossing interrupt of Channel #n. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>
0 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Interrupt is cleared. 1 Interrupt is requested.</p>

### 37.5.66 Interrupt Status Register 15 (IPUx\_INT\_STAT\_15)

IPU status registers are not stored in the SRM during power gating mode. IPU status registers are not stored in the SRM during power gating mode. This register contains part of IPU interrupts status bits. The status bits of general purpose interrupts can be found in this register.

Address: Base address + 238h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DI1_CNT_EN_PRE_8	DI1_CNT_EN_PRE_3	DI1_DISP_CLK_EN_PRE	DI0_CNT_EN_PRE_10	DI0_CNT_EN_PRE_9	DI0_CNT_EN_PRE_8	DI0_CNT_EN_PRE_7	DI0_CNT_EN_PRE_6	DI0_CNT_EN_PRE_5	DI0_CNT_EN_PRE_4	DI0_CNT_EN_PRE_3	DI0_CNT_EN_PRE_2	DI0_CNT_EN_PRE_1	DI0_CNT_EN_PRE_0	DC_ASYNC_STOP	DC_DP_START
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DI_VSYNC_PRE_1	DI_VSYNC_PRE_0	DC_FC_6	DC_FC_4	DC_FC_3	DC_FC_2	DC_FC_1	DC_FC_0	DP_ASF_BRAKE	DP_SF_BRAKE	DP ASF END	DP ASF START	DP_SF_END	DP_SF_START	SNOOPING2_INT	SNOOPING1_INT
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_INT\_STAT\_15 field descriptions**

Field	Description
31 DI1_CNT_EN_PRE_8	This bit indicates on the interrupt that is a result of a trigger generated by counter #8 of DI1 0 Interrupt is cleared. 1 Interrupt is requested.
30 DI1_CNT_EN_PRE_3	This bit indicates on the interrupt that is a result of a trigger generated by counter #3 of DI1 0 Interrupt is cleared. 1 Interrupt is requested.
29 DI1_DISP_CLK_EN_PRE	<b>DI1_DISP_CLK_EN_PRE</b> 0 Interrupt is cleared. 1 Interrupt is requested.
28 DI0_CNT_EN_PRE_10	This bit indicates on the interrupt that is a result of a trigger generated by counter #10 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
27 DI0_CNT_EN_PRE_9	This bit indicates on the interrupt that is a result of a trigger generated by counter #9 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
26 DI0_CNT_EN_PRE_8	This bit indicates on the interrupt that is a result of a trigger generated by counter #8 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
25 DI0_CNT_EN_PRE_7	This bit indicates on the interrupt that is a result of a trigger generated by counter #7 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
24 DI0_CNT_EN_PRE_6	This bit indicates on the interrupt that is a result of a trigger generated by counter #6 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
23 DI0_CNT_EN_PRE_5	This bit indicates on the interrupt that is a result of a trigger generated by counter #5 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
22 DI0_CNT_EN_PRE_4	This bit indicates on the interrupt that is a result of a trigger generated by counter #4 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
21 DI0_CNT_EN_PRE_3	This bit indicates on the interrupt that is a result of a trigger generated by counter #3 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
20 DI0_CNT_EN_PRE_2	This bit indicates on the interrupt that is a result of a trigger generated by counter #2 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_15 field descriptions (continued)**

Field	Description
19 DI0_CNT_EN_ PRE_1	This bit indicates on the interrupt that is a result of a trigger generated by counter #1 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
18 DI0_CNT_EN_ PRE_0	This bit indicates on the interrupt that is a result of a trigger generated by counter #0 of DIO 0 Interrupt is cleared. 1 Interrupt is requested.
17 DC_ASYNC_ STOP	This bit indicates on an interrupt asserted anytime the DP stops an async flow and moves to a sync flow 0 Interrupt is cleared. 1 Interrupt is requested.
16 DC_DP_START	This bit indicates on an interrupt asserted anytime the DP start a new sync or async flow or when an async flow is interrupted by a sync flow 0 Interrupt is cleared. 1 Interrupt is requested.
15 DI_VSYNC_ PRE_1	DI1 interrupt indicating of a VSYNC signal asserted 2 rows before the VSYNC sent to the display 0 Interrupt is cleared. 1 Interrupt is requested.
14 DI_VSYNC_ PRE_0	DI0 interrupt indicating of a VSYNC signal asserted 2 rows before the VSYNC sent to the display 0 Interrupt is cleared. 1 Interrupt is requested.
13 DC_FC_6	DC Frame Complete on channel #6 interrupt indication 0 Interrupt is cleared. 1 Interrupt is requested.
12 DC_FC_4	DC Frame Complete on channel #4 interrupt indication 0 Interrupt is cleared. 1 Interrupt is requested.
11 DC_FC_3	DC Frame Complete on channel #3 interrupt indication 0 Interrupt is cleared. 1 Interrupt is requested.
10 DC_FC_2	DC Frame Complete on channel #2 interrupt indication 0 Interrupt is cleared. 1 Interrupt is requested.
9 DC_FC_1	DC Frame Complete on channel #1 interrupt indication 0 Interrupt is cleared. 1 Interrupt is requested.
8 DC_FC_0	DC Frame Complete on channel #0 interrupt indication 0 Interrupt is cleared. 1 Interrupt is requested.

*Table continues on the next page...*

**IPUx\_INT\_STAT\_15 field descriptions (continued)**

Field	Description
7 DP ASF BRAKE	DP Async Flow Brake indication interrupt. This bit indicates on the interrupt that is a result of the async flow brake at the DP  0 Interrupt is cleared. 1 Interrupt is requested.
6 DP SF BRAKE	DP Sync Flow Brake indication interrupt. This bit indicates on the interrupt that is a result of the Sync flow brake at the DP  0 Interrupt is cleared. 1 Interrupt is requested.
5 DP ASF END	DP Async Flow End indication interrupt. This bit indicates on the interrupt that is a result of the Async flow end at the DP  0 Interrupt is cleared. 1 Interrupt is requested.
4 DP ASF START	DP Async Flow Start indication interrupt. This bit indicates on the interrupt that is a result of the Async flow start at the DP  0 Interrupt is cleared. 1 Interrupt is requested.
3 DP SF END	DP Sync Flow End indication interrupt. This bit indicates on the interrupt that is a result of the Sync flow end at the DP  0 Interrupt is cleared. 1 Interrupt is requested.
2 DP SF START	DP Sync Flow Start indication interrupt. This bit indicates on the interrupt that is a result of the Sync flow start at the DP  0 Interrupt is cleared. 1 Interrupt is requested.
1 SNOOPING2_INT	IPU snooping 2 event indication interrupt. This bit indicates on the interrupt that is a result of the detection of a snooping 2 signal assertion coming to the IPU  0 Interrupt is cleared. 1 Interrupt is requested.
0 SNOOPING1_INT	IPU snooping 1 event indication interrupt. This bit indicates on the interrupt that is a result of the detection of a snooping 1 signal assertion coming to the IPU  0 Interrupt is cleared. 1 Interrupt is requested.

### 37.5.67 Current Buffer Register 0 (IPUx\_CUR\_BUF\_0)

This register contains the current buffer status information bit for each DMA channel.

Address: Base address + 23Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DMA_CH_CUR_BUF_31	0	DMA_CH_CUR_BUF_29	DMA_CH_CUR_BUF_28	DMA_CH_CUR_BUF_27	DMA_CH_CUR_BUF_26	DMA_CH_CUR_BUF_25	DMA_CH_CUR_BUF_24	DMA_CH_CUR_BUF_23	DMA_CH_CUR_BUF_22	DMA_CH_CUR_BUF_21	DMA_CH_CUR_BUF_20	DMA_CH_CUR_BUF_19	DMA_CH_CUR_BUF_18	DMA_CH_CUR_BUF_17	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DMA_CH_CUR_BUF_15	DMA_CH_CUR_BUF_14	DMA_CH_CUR_BUF_13	DMA_CH_CUR_BUF_12	DMA_CH_CUR_BUF_11	DMA_CH_CUR_BUF_10	DMA_CH_CUR_BUF_9	DMA_CH_CUR_BUF_8	0	0	DMA_CH_CUR_BUF_5	0	DMA_CH_CUR_BUF_3	DMA_CH_CUR_BUF_2	DMA_CH_CUR_BUF_1	DMA_CH_CUR_BUF_0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_CUR\_BUF\_0 field descriptions**

Field	Description
31 DMA_CH_CUR_BUF_31	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
30 Reserved	This read-only field is reserved and always has the value 0. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
29 DMA_CH_CUR_BUF_29	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
28 DMA_CH_CUR_BUF_28	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.

Table continues on the next page...

**IPUx\_CUR\_BUF\_0 field descriptions (continued)**

Field	Description
27 DMA_CH_CUR_BUF_27	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
26 DMA_CH_CUR_BUF_26	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
25 DMA_CH_CUR_BUF_25	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
24 DMA_CH_CUR_BUF_24	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
23 DMA_CH_CUR_BUF_23	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
22 DMA_CH_CUR_BUF_22	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
21 DMA_CH_CUR_BUF_21	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
20 DMA_CH_CUR_BUF_20	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
19 DMA_CH_CUR_BUF_19	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.

*Table continues on the next page...*

**IPUx\_CUR\_BUF\_0 field descriptions (continued)**

Field	Description
18 DMA_CH_CUR_BUF_18	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
17 DMA_CH_CUR_BUF_17	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
16 Reserved	This read-only field is reserved and always has the value 0. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
15 DMA_CH_CUR_BUF_15	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
14 DMA_CH_CUR_BUF_14	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
13 DMA_CH_CUR_BUF_13	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
12 DMA_CH_CUR_BUF_12	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
11 DMA_CH_CUR_BUF_11	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
10 DMA_CH_CUR_BUF_10	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
9 DMA_CH_CUR_BUF_9	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.

*Table continues on the next page...*

**IPUx\_CUR\_BUF\_0 field descriptions (continued)**

Field	Description
	<p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
8 DMA_CH_CUR_BUF_8	<p>Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
7–6 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
5 DMA_CH_CUR_BUF_5	<p>Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
4 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
3 DMA_CH_CUR_BUF_3	<p>Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
2 DMA_CH_CUR_BUF_2	<p>Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
1 DMA_CH_CUR_BUF_1	<p>Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
0 DMA_CH_CUR_BUF_0	<p>Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>

### 37.5.68 Current Buffer Register 1 (IPUx\_CUR\_BUF\_1)

This register contains the current buffer status information bit for each DMA channel.

Address: Base address + 240h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0			DMA_CH_CUR_BUF_52	DMA_CH_CUR_BUF_51	DMA_CH_CUR_BUF_50	DMA_CH_CUR_BUF_49	DMA_CH_CUR_BUF_48
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DMA_CH_CUR_BUF_47	DMA_CH_CUR_BUF_46	DMA_CH_CUR_BUF_45	DMA_CH_CUR_BUF_44	DMA_CH_CUR_BUF_43	DMA_CH_CUR_BUF_42	DMA_CH_CUR_BUF_41	DMA_CH_CUR_BUF_40	0	0	0	0	0	0	DMA_CH_CUR_BUF_33	0
W																

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

**IPUx\_CUR\_BUF\_1 field descriptions**

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.
20 DMA_CH_CUR_BUF_52	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
19 DMA_CH_CUR_BUF_51	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
18 DMA_CH_CUR_BUF_50	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.

Table continues on the next page...

**IPUx\_CUR\_BUF\_1 field descriptions (continued)**

Field	Description
17 DMA_CH_CUR_BUF_49	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
16 DMA_CH_CUR_BUF_48	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
15 DMA_CH_CUR_BUF_47	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
14 DMA_CH_CUR_BUF_46	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
13 DMA_CH_CUR_BUF_45	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
12 DMA_CH_CUR_BUF_44	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
11 DMA_CH_CUR_BUF_43	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
10 DMA_CH_CUR_BUF_42	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
9 DMA_CH_CUR_BUF_41	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.

Table continues on the next page...

**IPUx\_CUR\_BUF\_1 field descriptions (continued)**

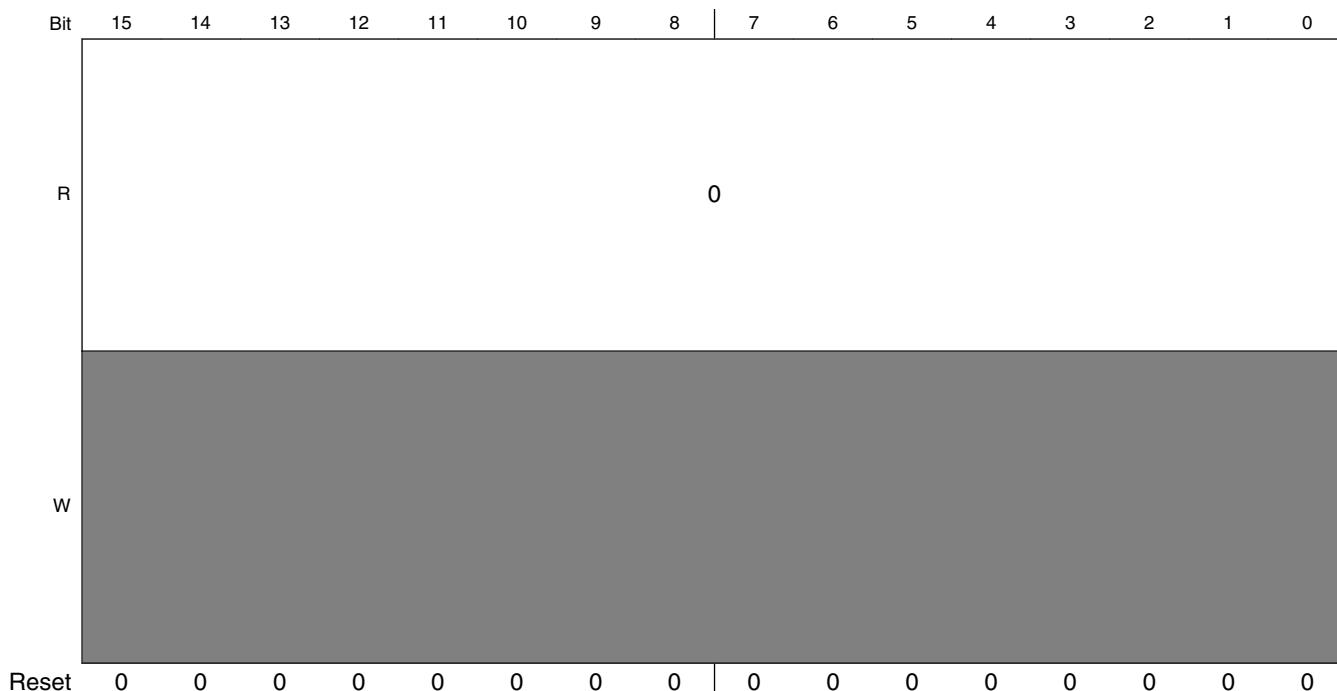
Field	Description
8 DMA_CH_CUR_ BUF_40	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
7–2 Reserved	This read-only field is reserved and always has the value 0. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
1 DMA_CH_CUR_ BUF_33	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
0 Reserved	This read-only field is reserved and always has the value 0. 0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.

### 37.5.69 Alternate Current Buffer Register 0 (IPUX\_ALT\_CUR\_0)

This register contains the current buffer status information bit for each DMA channel.

Address: Base address + 244h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0		DMA_CH_ALT_CUR_BUF_29		0			DMA_CH_ALT_CUR_BUF_24				0				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_ALT\_CUR\_0 field descriptions**

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.  0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
29 DMA_CH_ALT_ CUR_BUF_29	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.  0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
28–25 Reserved	This read-only field is reserved and always has the value 0.  0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
24 DMA_CH_ALT_ CUR_BUF_24	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.  0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
Reserved	This read-only field is reserved and always has the value 0.  0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.

### 37.5.70 Alternate Current Buffer Register 1 (IPUX\_ALT\_CUR\_1)

This register contains the current buffer status information bit for each DMA channel. The register is shown in [VDI Plane Size Register 4](#), and the register fields are described in [VDI Plane Size Register 4](#).

Address: Base address + 248h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R							DMA_CH_ALT_CUR_BUF1_n							DMA_CH_ALT_CUR_BUF0_n		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUX\_ALT\_CUR\_1 field descriptions**

Field	Description
31–21 Reserved	This read-only field is reserved and always has the value 0.  0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
20 DMA_CH_ALT_ CUR_BUF_52	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.  0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
19–10 Reserved	This read-only field is reserved and always has the value 0.  0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.
9 DMA_CH_ALT_ CUR_BUF1_n	Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.

Table continues on the next page...

**IPUx\_ALT\_CUR\_1 field descriptions (continued)**

Field	Description
	<p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
8–2 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
1 DMA_CH_ALT_CUR_BUFO_n	<p>Current Buffer. This bit indicates which buffer is in use by DMA when double buffer mode is selected. <i>n</i> Indicates the corresponding DMA channel number.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>
0 Reserved	<p>This read-only field is reserved and always has the value 0.</p> <p>0 Current buffer used by DMA is buffer 0. 1 Current buffer used by DMA is buffer 1.</p>

### 37.5.71 Shadow Registers Memory Status Register (IPUx\_SRM\_STAT)

The register contains status bits of SRM updates. There is a bit for each block. The bit is set when the SRM is currently updating the module's registers. When the SRM completes updating the registers of the block the bit is cleared. SW should not update the block's registers while it is being updated by the SRM.

Address: Base address + 24Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R									0								
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R							DI1_SRM_STAT	DIO_SRM_STAT	CSI1_SRM_STAT	CSI0_SRM_STAT	DC_6_SRM_STAT	DC_2_SRM_STAT	0	DP_A1_SRM_STAT	DP_A0_SRM_STAT	DP_S_SRM_STAT
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_SRM\_STAT field descriptions**

Field	Description
31–10 Reserved	This read-only field is reserved and always has the value 0.
9 DI1_SRM_STAT	DI1 SRM STAT This bit indicates that the SRM is currently updating the DI1 registers 1 SRM is busy updating the DI1 registers 0 SRM is not updating the DI1 registers
8 DIO_SRM_STAT	DI0 SRM STAT This bit indicates that the SRM is currently updating the DIO registers 1 SRM is busy updating the DIO registers 0 SRM is not updating the DIO registers
7 CSI1_SRM_STAT	CSI1_SRM_STAT
6 CSI0_SRM_STAT	CSI0_SRM_STAT
5 DC_6_SRM_STAT	DC group #6 SRM STAT This bit indicates that the SRM is currently updating the DC group #6 registers

*Table continues on the next page...*

**IPUx\_SRM\_STAT field descriptions (continued)**

Field	Description
	1 SRM is busy updating the DC registers 0 SRM is not updating the DC registers
4 DC_2_SRM_STAT	DC group #2 SRM STAT This bit indicates that the SRM is currently updating the DC group #2 registers 1 SRM is busy updating the DC group #6 registers 0 SRM is not updating the DC group #2 registers
3 Reserved	This read-only field is reserved and always has the value 0.
2 DP_A1_SRM_STAT	DP ASYNC1 FLOW SRM STAT This bit indicates that the SRM is currently updating the DP async flow 1 registers 1 SRM is busy updating the DP sync flow registers 0 SRM is not updating the DP sync flow registers
1 DP_A0_SRM_STAT	DP ASYNC0 FLOW SRM STAT This bit indicates that the SRM is currently updating the DP async flow 0 registers 1 SRM is busy updating the DP sync flow registers 0 SRM is not updating the DP sync flow registers
0 DP_S_SRM_STAT	DP SYNC FLOW SRM STAT This bit indicates that the SRM is currently updating the DP sync flow registers 1 SRM is busy updating the DP sync flow registers 0 SRM is not updating the DP sync flow registers

### 37.5.72 Processing Status Tasks Register (IPUx\_PROC\_TASKS\_STAT)

This register contains status bits for IPU's tasks.

Address: Base address + 250h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R									0								
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0	MEM2PRP_TSTAT		PP_ROT_TSTAT		VF_ROT_TSTAT		ENC_ROT_TSTAT		PP_TSTAT		VF_TSTAT		ENC_TSTAT			
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_PROC\_TASKS\_STAT field descriptions**

Field	Description
31–15 Reserved	This read-only field is reserved and always has the value 0.
14–12 MEM2PRP_ TSTAT	Status of the pre processing tasks (viewfinder and encoding) when the source is coming from the memory. 000 IDLE - Both pre processing tasks are idle 001 BOTH_ACTIVE - Both pre processing tasks are idle 010 ENC_ACTIVE - Encoding task is active 011 VF_ACTIVE - View finder task is active 100 BOTH_PAUSE - both tasks are paused 101 Reserved 110 Reserved 111 Reserve
11–10 PP_ROT_TSTAT	Status of the rotation for post processing task 00 IDLE - The task is idle 01 ACTIVE - The primary flow of this task is currently active 10 WAIT_FOR_READY - The task is waiting for a buffer to be ready
9–8 VF_ROT_TSTAT	Status of the rotation for viewfinder task 00 IDLE - The task is idle 01 ACTIVE - The primary flow of this task is currently active 10 WAIT_FOR_READY - The task is waiting for a buffer to be ready
7–6 ENC_ROT_ TSTAT	Status of the rotation for encoding task 00 IDLE - The task is idle 01 ACTIVE - The primary flow of this task is currently active 10 WAIT_FOR_READY - The task is waiting for a buffer to be ready
5–4 PP_TSTAT	Status of the post processing task 00 IDLE - The task is idle 01 ACTIVE - The primary flow of this task is currently active 10 WAIT_FOR_READY - The task is waiting for a buffer to be ready
3–2 VF_TSTAT	Status of the viewfinder task 00 IDLE - The task is idle 01 ACTIVE - The primary flow of this task is currently active 10 WAIT_FOR_READY - The task is waiting for a buffer to be ready
ENC_TSTAT	Status of the encoding task 00 IDLE - The task is idle 01 ACTIVE - The primary flow of this task is currently active 10 WAIT_FOR_READY - The task is waiting for a buffer to be ready

### 37.5.73 Display Tasks Status Register (IPUx\_DISP\_TASKS\_STAT)

This register contains status bits for IPU's tasks.

Address: Base address + 254h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R					DC_ASYNC2_CUR_FLOW								DC_ASYNC1_STAT		DP_ASYNC_CUR_FLOW	
W					0	DC_ASYNCH2_STAT			0	DC_ASYNC1_STAT			DP_ASYNC_STAT			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DISP\_TASKS\_STAT field descriptions**

Field	Description
31–12 Reserved	This read-only field is reserved and always has the value 0.
11 DC_ASYNC2_CUR_FLOW	Current asynchronous #2 flow via the DC 1 alternate flow 0 main flow
10–8 DC_ASYNCH2_STAT	Status of the Asynchronous flow #2 through the DC 000 IDLE - the task is idle 001 PRIM_ACTIVE - The primary flow of this task is currently active 010 ALT_ACTIVE - The alternate flow of this task is currently active 011 UPDATE_PARAM - The FSU is busy updating parameters from the SRM 100 PAUSE - The task is paused 101 Reserved 110 Reserved 111 Reserved
7–6 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**IPUx\_DISP\_TASKS\_STAT field descriptions (continued)**

Field	Description
5–4 DC_ASYNC1_STAT	Status of the Asynchronous flow #1 through the DC (ch 28)  00 IDLE - The task is idle 01 ACTIVE - This task is currently active 10 WAIT_FOR_READY - The task is waiting for a buffer to be ready
3 DP_ASYNC_CUR_FLOW	Current asynchronous flow via the DP  1 alternate flow 0 main flow
DP_ASYNC_STAT	Status of the Asynchronous flow through the DP  000 IDLE - the task is idle 001 PRIM_ACTIVE - The primary flow of this task is currently active 010 ALT_ACTIVE - The alternate flow of this task is currently active 011 UPDATE_PARAM - The FSU is busy updating parameters from the SRM 100 PAUSE - The task is paused 101 Reserved 110 Reserved 111 Reserved

### 37.5.74 Triple Current Buffer Register 0 (IPUx\_TRIPLE\_CUR\_BUF\_0)

This register contains the current buffer status information for triple buffer mode for each DMA channel.

- Hide VPU\_SUB\_FRAME\_SYNC for all versions
- Show VPU\_SUB\_FRAME\_SYNC for IPUv3H version.
- The table below tagged with other settings (like IPU3M\_only) should be hidden in IPUv3H version.
- This requires some sophisticated conditional tag settings

Address: Base address + 258h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R				0		DMA_CH_TRIPLE_CUR_BUF_13			0		DMA_CH_TRIPLE_CUR_BUF_10		DMA_CH_TRIPLE_CUR_BUF_9		DMA_CH_TRIPLE_CUR_BUF_8	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	

**IPUx\_TRIPLE\_CUR\_BUF\_0 field descriptions**

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–26 DMA_CH_ TRIPLE_CUR_ BUF_13	<p>Current Buffer for triple buffer mode. This bits indicate which buffer is in use by the DMA when triple buffer mode is selected.</p> <p>Each pair of bits indicate the corresponding DMA channel (bits [1:0] correspond to ch #0; (bits [3:2] correspond to ch #1, etc.)</p> <ul style="list-style-type: none"> <li>11 NA</li> <li>00 Current buffer used by DMA is buffer 0.</li> <li>01 Current buffer used by DMA is buffer 1.</li> <li>10 Current buffer used by DMA is buffer 2.</li> </ul>
25–22 Reserved	This read-only field is reserved and always has the value 0.
21–20 DMA_CH_ TRIPLE_CUR_ BUF_10	<p>Current Buffer for triple buffer mode. This bits indicate which buffer is in use by the DMA when triple buffer mode is selected.</p> <p>Each pair of bits indicate the corresponding DMA channel (bits [1:0] correspond to ch #0; (bits [3:2] correspond to ch #1, etc.)</p> <ul style="list-style-type: none"> <li>11 NA</li> <li>00 Current buffer used by DMA is buffer 0.</li> <li>01 Current buffer used by DMA is buffer 1.</li> <li>10 Current buffer used by DMA is buffer 2.</li> </ul>
19–18 DMA_CH_ TRIPLE_CUR_ BUF_9	<p>Current Buffer for triple buffer mode. This bits indicate which buffer is in use by the DMA when triple buffer mode is selected.</p> <p>Each pair of bits indicate the corresponding DMA channel (bits [1:0] correspond to ch #0; (bits [3:2] correspond to ch #1, etc.)</p> <ul style="list-style-type: none"> <li>11 NA</li> <li>00 Current buffer used by DMA is buffer 0.</li> <li>01 Current buffer used by DMA is buffer 1.</li> <li>10 Current buffer used by DMA is buffer 2.</li> </ul>
17–16 DMA_CH_ TRIPLE_CUR_ BUF_8	<p>Current Buffer for triple buffer mode. This bits indicate which buffer is in use by the DMA when triple buffer mode is selected.</p> <p>Each pair of bits indicate the corresponding DMA channel (bits [1:0] correspond to ch #0; (bits [3:2] correspond to ch #1, etc.)</p> <ul style="list-style-type: none"> <li>11 NA</li> <li>00 Current buffer used by DMA is buffer 0.</li> <li>01 Current buffer used by DMA is buffer 1.</li> <li>10 Current buffer used by DMA is buffer 2.</li> </ul>
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.75 Triple Current Buffer Register 1 (IPUx\_TRIPLE\_CUR\_BUF\_1)

This register contains the current buffer status information for triple buffer mode for each DMA channel.

Address: Base address + 25Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0						DMA_CH_TRIPLE_CUR_BUF_28	DMA_CH_TRIPLE_CUR_BUF_27	0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DMA_CH_TRIPLE_CUR_BUF_23		0		DMA_CH_TRIPLE_CUR_BUF_21										0	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_TRIPLE\_CUR\_BUF\_1 field descriptions

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.
25–24 DMA_CH_TRIPLE_CUR_BUF_28	Current Buffer for triple buffer mode. This bits indicate which buffer is in use by the DMA when triple buffer mode is selected.  Each pair of bits indicate the corresponding DMA channel (bits [1:0] correspond to ch #0; (bits [3:2] correspond to ch #1, etc.)  11 NA 00 Current buffer used by DMA is buffer 0. 01 Current buffer used by DMA is buffer 1. 10 Current buffer used by DMA is buffer 2.
23–22 DMA_CH_TRIPLE_CUR_BUF_27	Current Buffer for triple buffer mode. This bits indicate which buffer is in use by the DMA when triple buffer mode is selected.  Each pair of bits indicate the corresponding DMA channel (bits [1:0] correspond to ch #0; (bits [3:2] correspond to ch #1, etc.)  11 NA 00 Current buffer used by DMA is buffer 0. 01 Current buffer used by DMA is buffer 1. 10 Current buffer used by DMA is buffer 2.

Table continues on the next page...

**IPUx\_TRIPLE\_CUR\_BUF\_1 field descriptions (continued)**

Field	Description
21–16 Reserved	This read-only field is reserved and always has the value 0.
15–14 DMA_CH_ TRIPLE_CUR_ BUF_23	Current Buffer for triple buffer mode. This bits indicate which buffer is in use by the DMA when triple buffer mode is selected.  Each pair of bits indicate the corresponding DMA channel (bits [1:0] correspond to ch #0; (bits [3:2] correspond to ch #1, etc.)  11 NA 00 Current buffer used by DMA is buffer 0. 01 Current buffer used by DMA is buffer 1. 10 Current buffer used by DMA is buffer 2.
13–12 Reserved	This read-only field is reserved and always has the value 0.
11–10 DMA_CH_ TRIPLE_CUR_ BUF_21	Current Buffer for triple buffer mode. This bits indicate which buffer is in use by the DMA when triple buffer mode is selected.  Each pair of bits indicate the corresponding DMA channel (bits [1:0] correspond to ch #0; (bits [3:2] correspond to ch #1, etc.)  11 NA 00 Current buffer used by DMA is buffer 0. 01 Current buffer used by DMA is buffer 1. 10 Current buffer used by DMA is buffer 2.
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.76 IPU Channels Buffer 0 Ready 0 Register (IPUx\_CH\_BUF0\_RDY0)

The register contains buffer 0 ready control information for 32 IPU's DMA channels (31-0). This register can be a write one to set or a write one to clear according to the **IPU\_CH\_BUF0\_RDY0\_CLR** bit.

The register is shown in [IPU Channels Buffer 0 Ready 0 Register \(IPU\\_CH\\_BUF0\\_RDY0\)](#), and the register fields are described in [IPU Channels Buffer 0 Ready 0 Register \(IPU\\_CH\\_BUF0\\_RDY0\)](#).

## IPU Memory Map/Register Definition

Address: Base address + 268h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### IPUx\_CH\_BUFO\_RDY0 field descriptions

Field	Description
31 DMA_CH_BUFO_RDY_31	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
30 -	This field is reserved. Reserved.
29 DMA_CH_BUFO_RDY_29	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
28 DMA_CH_BUFO_RDY_28	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
27 DMA_CH_BUFO_RDY_27	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
26–25 -	This field is reserved. Reserved.
24 DMA_CH_BUFO_RDY_24	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.

Table continues on the next page...

**IPUx\_CH\_BUF0\_RDY0 field descriptions (continued)**

Field	Description
23 DMA_CH_BUF0_ RDY_23	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
22 DMA_CH_BUF0_ RDY_22	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
21 DMA_CH_BUF0_ RDY_21	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
20 DMA_CH_BUF0_ RDY_20	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
19 -	This field is reserved. Reserved.
18 DMA_CH_BUF0_ RDY_18	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
17 DMA_CH_BUF0_ RDY_17	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
16 -	This field is reserved. Reserved.
15 DMA_CH_BUF0_ RDY_15	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
14 DMA_CH_BUF0_ RDY_14	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
13 DMA_CH_BUF0_ RDY_13	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
12 DMA_CH_BUF0_ RDY_12	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
11 DMA_CH_BUF0_ RDY_11	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.

*Table continues on the next page...*

**IPUx\_CH\_BUF0\_RDY0 field descriptions (continued)**

Field	Description
10 DMA_CH_BUF0_ RDY_10	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
9 DMA_CH_BUF0_ RDY_9	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
8 DMA_CH_BUF0_ RDY_8	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
7 DMA_CH_BUF0_ RDY_7	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
6 DMA_CH_BUF0_ RDY_6	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
5 DMA_CH_BUF0_ RDY_5	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
4 DMA_CH_BUF0_ RDY_4	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
3 DMA_CH_BUF0_ RDY_3	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
2 DMA_CH_BUF0_ RDY_2	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
1 DMA_CH_BUF0_ RDY_1	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
0 DMA_CH_BUF0_ RDY_0	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.

### 37.5.77 IPU Channels Buffer 0 Ready 1 Register (IPUx\_CH\_BUF0\_RDY1)

The register contains buffer 0 ready control information for 32 IPU's DMA channels (63-32). This register can be a write one to set or a write one to clear according to the **IPU\_CH\_BUF0\_RDY1\_CLR** bit.

Address: Base address + 26Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R	DMA_CH_BUF0_RDY_47	DMA_CH_BUF0_RDY_46	DMA_CH_BUF0_RDY_45	DMA_CH_BUF0_RDY_44	DMA_CH_BUF0_RDY_43	DMA_CH_BUF0_RDY_42	DMA_CH_BUF0_RDY_41	DMA_CH_BUF0_RDY_40							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_CH\_BUF0\_RDY1 field descriptions

Field	Description
31–21 -	This field is reserved. Reserved.
20 DMA_CH_BUF0_RDY_52	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
19 DMA_CH_BUF0_RDY_51	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.

Table continues on the next page...

**IPUx\_CH\_BUF0\_RDY1 field descriptions (continued)**

Field	Description
18 DMA_CH_BUF0_ RDY_50	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
17 DMA_CH_BUF0_ RDY_49	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
16 DMA_CH_BUF0_ RDY_48	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
15 DMA_CH_BUF0_ RDY_47	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
14 DMA_CH_BUF0_ RDY_46	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
13 DMA_CH_BUF0_ RDY_45	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
12 DMA_CH_BUF0_ RDY_44	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
11 DMA_CH_BUF0_ RDY_43	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
10 DMA_CH_BUF0_ RDY_42	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
9 DMA_CH_BUF0_ RDY_41	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
8 DMA_CH_BUF0_ RDY_40	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
7–2 -	This field is reserved. Reserved.
1 DMA_CH_BUF0_ RDY_33	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory.

*Table continues on the next page...*

**IPUx\_CH\_BUF0\_RDY1 field descriptions (continued)**

Field	Description
	0 Buffer 0 is not ready. 1 Buffer 0 is ready.
0 -	This field is reserved. Reserved.

### 37.5.78 IPU Channels Buffer 1 Ready 0 Register (IPUx\_CH\_BUF1\_RDY0)

The register contains buffer 1 ready control information for 32 IPU's DMA channels (31-0). This register can be a write one to set or a write one to clear according to the **IPU\_CH\_BUF1\_RDY0\_CLR** bit.

Address: Base address + 270h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DMA_CH_BUF1_RDY_31	Reserved	DMA_CH_BUF1_RDY_29	DMA_CH_BUF1_RDY_28	DMA_CH_BUF1_RDY_27	DMA_CH_BUF1_RDY_26	DMA_CH_BUF1_RDY_25	DMA_CH_BUF1_RDY_24	DMA_CH_BUF1_RDY_23	DMA_CH_BUF1_RDY_22	DMA_CH_BUF1_RDY_21	DMA_CH_BUF1_RDY_20	DMA_CH_BUF1_RDY_19	DMA_CH_BUF1_RDY_18	DMA_CH_BUF1_RDY_17	Reserved
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DMA_CH_BUF1_RDY_15	DMA_CH_BUF1_RDY_14	DMA_CH_BUF1_RDY_13	DMA_CH_BUF1_RDY_12	DMA_CH_BUF1_RDY_11	DMA_CH_BUF1_RDY_10	DMA_CH_BUF1_RDY_9	DMA_CH_BUF1_RDY_8	Reserved	Reserved	DMA_CH_BUF1_RDY_5	Reserved	DMA_CH_BUF1_RDY_3	DMA_CH_BUF1_RDY_2	DMA_CH_BUF1_RDY_1	DMA_CH_BUF1_RDY_0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_CH\_BUF1\_RDY0 field descriptions**

Field	Description
31 DMA_CH_BUF1_RDY_31	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory.

*Table continues on the next page...*

**IPUx\_CH\_BUF1\_RDY0 field descriptions (continued)**

Field	Description
	0 Buffer 0 is not ready. 1 Buffer 0 is ready.
30 -	This field is reserved. Reserved.
29 DMA_CH_BUF1_RDY_29	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
28 DMA_CH_BUF1_RDY_28	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
27 DMA_CH_BUF1_RDY_27	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
26 DMA_CH_BUF1_RDY_26	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
25 DMA_CH_BUF1_RDY_25	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
24 DMA_CH_BUF1_RDY_24	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
23 DMA_CH_BUF1_RDY_23	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
22 DMA_CH_BUF1_RDY_22	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
21 DMA_CH_BUF1_RDY_21	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
20 DMA_CH_BUF1_RDY_20	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
19 DMA_CH_BUF1_RDY_19	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.

*Table continues on the next page...*

**IPUx\_CH\_BUF1\_RDY0 field descriptions (continued)**

Field	Description
18 DMA_CH_BUF1_ RDY_18	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
17 DMA_CH_BUF1_ RDY_17	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
16 -	This field is reserved. Reserved.
15 DMA_CH_BUF1_ RDY_15	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
14 DMA_CH_BUF1_ RDY_14	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
13 DMA_CH_BUF1_ RDY_13	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
12 DMA_CH_BUF1_ RDY_12	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
11 DMA_CH_BUF1_ RDY_	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
10 DMA_CH_BUF1_ RDY_10	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
9 DMA_CH_BUF1_ RDY_9	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
8 DMA_CH_BUF1_ RDY_8	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
7–6 -	This field is reserved. Reserved.
5 DMA_CH_BUF1_ RDY_5	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.

*Table continues on the next page...*

**IPUx\_CH\_BUF1\_RDY0 field descriptions (continued)**

Field	Description
4 -	This field is reserved. Reserved.
3 DMA_CH_BUF1_RDY_3	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
2 DMA_CH_BUF1_RDY_2	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
1 DMA_CH_BUF1_RDY_1	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
0 DMA_CH_BUF1_RDY_0	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.

### 37.5.79 IPU Channels Buffer 1 Ready 1Register (IPUx\_CH\_BUF1\_RDY1)

The register contains buffer 0 ready control information for 32 IPU's DMA channels (63-32). This register can be a write one to set or a write one to clear according to the **IPU\_CH\_BUF1\_RDY1\_CLR** bit.

The register is shown in [IPU Channels Buffer 1 Ready 1Register \(IPU\\_CH\\_BUF1\\_RDY1\)](#), and the register fields are described in [IPU Channels Buffer 1 Ready 1Register \(IPU\\_CH\\_BUF1\\_RDY1\)](#).

Address: Base address + 274h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R												DMA_CH_BUF0_RDY_52	DMA_CH_BUF0_RDY_51	DMA_CH_BUF0_RDY_50	DMA_CH_BUF0_RDY_49	DMA_CH_BUF0_RDY_48
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DMA_CH_BUF0_RDY_47	DMA_CH_BUF0_RDY_46	DMA_CH_BUF0_RDY_45	DMA_CH_BUF0_RDY_44	DMA_CH_BUF0_RDY_43	DMA_CH_BUF0_RDY_42	DMA_CH_BUF0_RDY_41	DMA_CH_BUF0_RDY_40	Reserved						DMA_CH_BUF0_RDY_33	Reserved
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUX\_CH\_BUF1\_RDY1 field descriptions**

Field	Description
31–21 -	This field is reserved. Reserved.
20 DMA_CH_BUF0_RDY_52	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
19 DMA_CH_BUF0_RDY_51	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
18 DMA_CH_BUF0_RDY_50	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
17 DMA_CH_BUF0_RDY_49	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
16 DMA_CH_BUF0_RDY_48	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
15 DMA_CH_BUF0_RDY_47	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
14 DMA_CH_BUF0_RDY_46	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
13 DMA_CH_BUF0_RDY_45	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.

Table continues on the next page...

**IPUx\_CH\_BUF1\_RDY1 field descriptions (continued)**

Field	Description
12 DMA_CH_BUF0_ RDY_44	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
11 DMA_CH_BUF0_ RDY_43	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
10 DMA_CH_BUF0_ RDY_42	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
9 DMA_CH_BUF0_ RDY_41	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
8 DMA_CH_BUF0_ RDY_40	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
7–2 -	This field is reserved. Reserved.
1 DMA_CH_BUF0_ RDY_33	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 Buffer 1 is ready.
0 -	This field is reserved. Reserved.

### 37.5.80 IPU Alternate Channels Buffer 0 Ready 0 Register (IPUx\_ALT\_CH\_BUF0\_RDY0)

The register contains buffer 0 ready control information for 32 IPU's DMA channels (31-0). Writing "1" to each field will set each bit. Writing "0" to each field simultaneously will clear all the bits.

Address: Base address + 278h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R				DMA_CH_ALT_BUF0_RDY_29												
W			Reserved													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

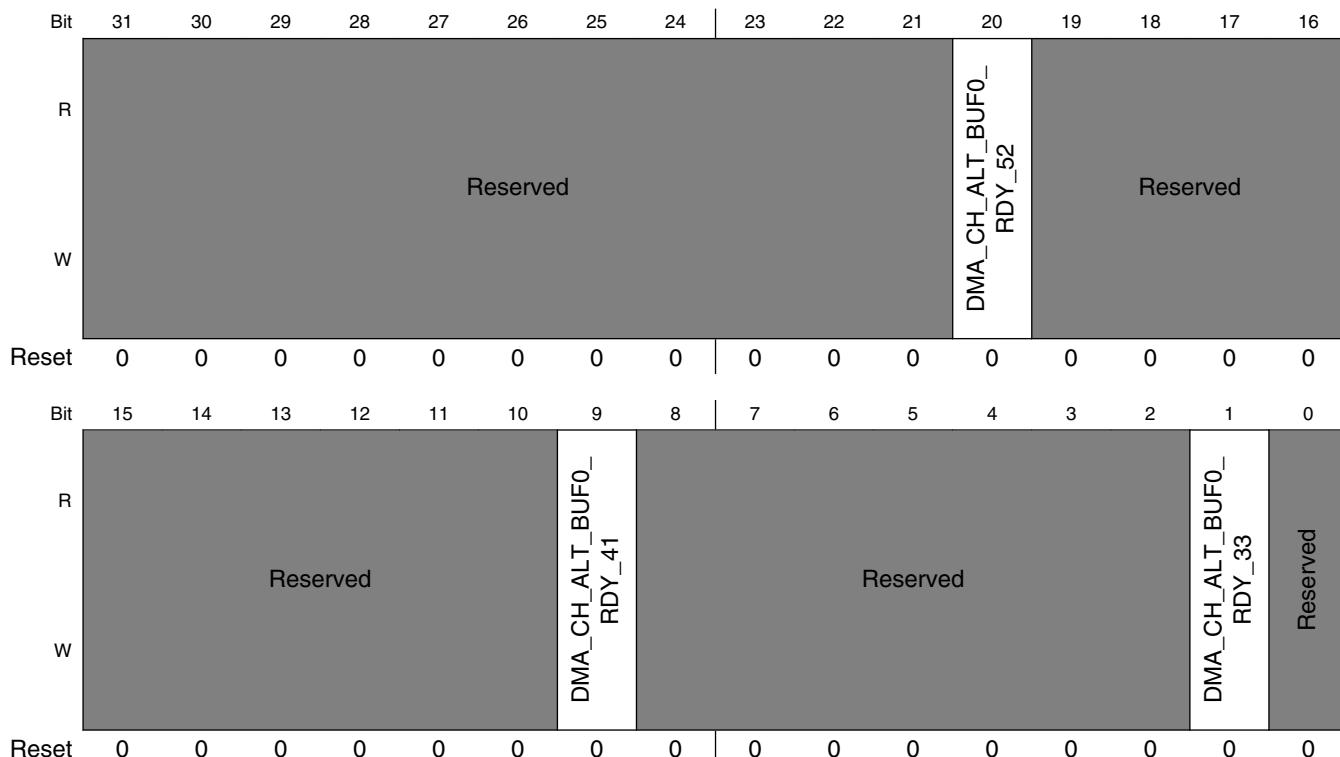
#### IPUx\_ALT\_CH\_BUF0\_RDY0 field descriptions

Field	Description
31–30 -	This field is reserved. Reserved.
29 DMA_CH_ALT_BUF0_RDY_29	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
28–25 -	This field is reserved. Reserved.
24 DMA_CH_ALT_BUF0_RDY_24	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
-	This field is reserved. Reserved.

### 37.5.81 IPU Alternate Channels Buffer 0 Ready 1 Register (IPUx\_ALT\_CH\_BUF0\_RDY1)

The register contains buffer 0 ready control information for 32 IPU's DMA channels (63-32). Writing "1" to each field will set each bit. Writing "0" to each field simultaneously will clear all the bits.

Address: Base address + 27Ch offset



#### IPUx\_ALT\_CH\_BUF0\_RDY1 field descriptions

Field	Description
31–21 -	This field is reserved. Reserved.
20 DMA_CH_ALT_BUF0_RDY_52	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
19–10 -	This field is reserved. Reserved.
9 DMA_CH_ALT_BUF0_RDY_41	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.

Table continues on the next page...

**IPUx\_ALT\_CH\_BUFO\_RDY1 field descriptions (continued)**

Field	Description
8–2 -	This field is reserved. Reserved.
1 DMA_CH_ALT_ BUF0_RDY_33	Buffer 0 is ready. This bit indicates that ARM platform finished/writing reading buffer 0 in memory. 0 Buffer 0 is not ready. 1 Buffer 0 is ready.
0 -	This field is reserved. Reserved.

### 37.5.82 IPU Alternate Channels Buffer1 Ready 0 Register (IPUx\_ALT\_CH\_BUF1\_RDY0)

The register contains buffer 1 ready control information for 32 IPU's DMA channels (31-0). Writing "1" to each field will set each bit. Writing "0" to each field simultaneously will clear all the bits.

The register is shown in [IPU Alternate Channels Buffer1 Ready 0 Register \(IPU\\_ALT\\_CH\\_BUF1\\_RDY0\)](#), and the register fields are described in [IPU Alternate Channels Buffer1 Ready 0 Register \(IPU\\_ALT\\_CH\\_BUF1\\_RDY0\)](#).

Address: Base address + 280h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
	Reserved		DMA_CH_ALT_ BUF1_RDY_29		Reserved			DMA_CH_ALT_ BUF1_RDY_24								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
	Reserved															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_ALT\_CH\_BUF1\_RDY0 field descriptions**

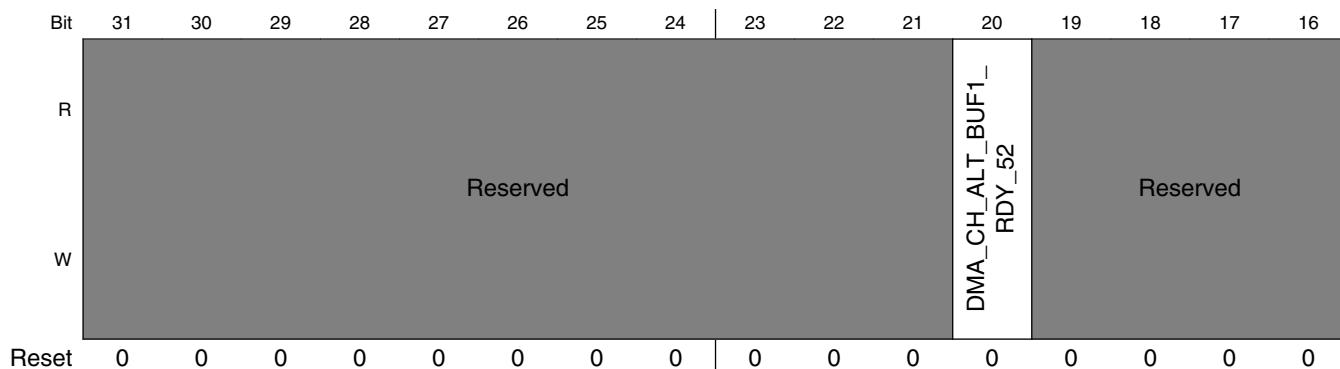
Field	Description
31–30 -	This field is reserved. Reserved.
29 DMA_CH_ALT_BUF1_RDY_29	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 buffer 1 is ready.
28–25 -	This field is reserved. Reserved.
24 DMA_CH_ALT_BUF1_RDY_24	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 buffer 1 is ready.
-	This field is reserved. Reserved.

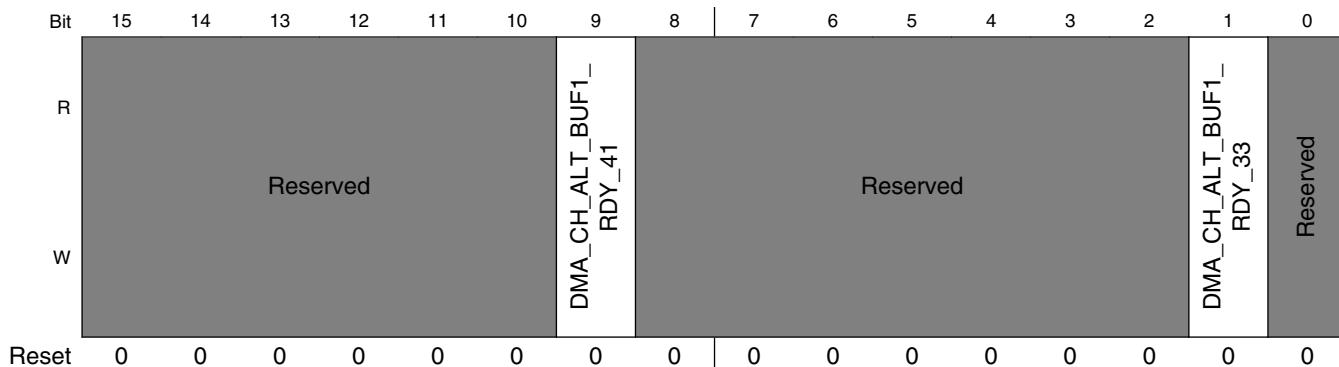
### 37.5.83 IPU Alternate Channels Buffer 1 Ready 1 Register (IPUx\_ALT\_CH\_BUF1\_RDY1)

The register contains buffer 0 ready control information for 32 IPU's DMA channels (63-32). Writing "1" to each field will set each bit. Writing "0" to each field simultaneously will clear all the bits.

The register is shown in [IPU Alternate Channels Buffer 1 Ready 1 Register \(IPU\\_ALT\\_CH\\_BUF1\\_RDY1\)](#), and the register fields are described in [IPU Alternate Channels Buffer 1 Ready 1 Register \(IPU\\_ALT\\_CH\\_BUF1\\_RDY1\)](#).

Address: Base address + 284h offset





### IPUx\_ALT\_CH\_BUF1\_RDY1 field descriptions

Field	Description
31–21 -	This field is reserved. Reserved.
20 DMA_CH_ALT_BUF1_RDY_52	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 buffer 1 is ready.
19–10 -	This field is reserved. Reserved.
9 DMA_CH_ALT_BUF1_RDY_41	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 buffer 1 is ready.
8–2 -	This field is reserved. Reserved.
1 DMA_CH_ALT_BUF1_RDY_33	Buffer 1 is ready. This bit indicates that ARM platform finished/writing reading buffer 1 in memory. 0 buffer 1 is not ready. 1 buffer 1 is ready.
0 -	This field is reserved. Reserved.

### 37.5.84 IPU Channels Buffer 2 Ready 0 Register (IPUx\_CH\_BUF2\_RDY0)

The register contains buffer 2 ready control information for 32 IPU's DMA channels (31-0). This register can be a write one to set or a write one to clear according to the **IPU\_CH\_BUF2\_RDY0\_CLR** bit.

The register is shown in [IPU Channels Buffer 2 Ready 0 Register \(IPU\\_CH\\_BUF2\\_RDY0\)](#), and the register fields are described in [IPU Channels Buffer 2 Ready 0 Register \(IPU\\_CH\\_BUF2\\_RDY0\)](#).

## IPU Memory Map/Register Definition

Address: Base address + 288h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	Reserved				DMA_CH_BUF2_RDY_28	DMA_CH_ALT_BUF1_RDY_27	Reserved				DMA_CH_BUF2_RDY_23	Reserved	DMA_CH_BUF2_RDY_21	Reserved			
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	Reserved				DMA_CH_BUF2_RDY_13	Reserved	DMA_CH_BUF2_RDY_10	DMA_CH_BUF2_RDY_9	DMA_CH_BUF2_RDY_8	Reserved				DMA_CH_BUF2_RDY_2	Reserved	DMA_CH_BUF2_RDY_0	
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

### IPUx\_CH\_BUF2\_RDY0 field descriptions

Field	Description
31–29 -	This field is reserved. Reserved.
28 DMA_CH_BUF2_RDY_28	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.
27 DMA_CH_ALT_BUF1_RDY_27	buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 buffer 2 is not ready. 1 buffer 2 is ready.
26–24 -	This field is reserved. Reserved.
23 DMA_CH_BUF2_RDY_23	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.
22 -	This field is reserved. Reserved.
21 DMA_CH_BUF2_RDY_21	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.
20–14 -	This field is reserved. Reserved.

Table continues on the next page...

**IPUx\_CH\_BUF2\_RDY0 field descriptions (continued)**

Field	Description
13 DMA_CH_BUF2_ RDY_13	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.
12–11 -	This field is reserved. Reserved.
10 DMA_CH_BUF2_ RDY_10	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.
9 DMA_CH_BUF2_ RDY_9	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.
8 DMA_CH_BUF2_ RDY_8	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.
7–3 -	This field is reserved. Reserved.
2 DMA_CH_BUF2_ RDY_2	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.
1 -	This field is reserved. Reserved.
0 DMA_CH_BUF2_ RDY_0	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.

### 37.5.85 IPU Channels Buffer 2 Ready 1 Register (IPUx\_CH\_BUF2\_RDY1)

The register contains buffer 2 ready control information for 32 IPU's DMA channels (63-32). This register can be a write one to set or a write one to clear according to the **IPU\_CH\_BUF2\_RDY1\_CLR** bit.

The register is shown in [IPU Channels Buffer 2 Ready 1 Register \(IPU\\_CH\\_BUF2\\_RDY1\)](#), and the register fields are described in [IPU Channels Buffer 2 Ready 1 Register \(IPU\\_CH\\_BUF2\\_RDY1\)](#).

## IPU Memory Map/Register Definition

Address: Base address + 28Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

### IPUx\_CH\_BUF2\_RDY1 field descriptions

Field	Description
DMA_CH_BUF2_RDY_x	Buffer 2 is ready. This bit indicates that ARM platform finished/writing reading buffer 2 in memory. 0 Buffer 2 is not ready. 1 Buffer 2 is ready.

## 37.5.86 IDMAC Configuration Register (IPUx\_IDMAC\_CONF)

Address: Base address + 8000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1

### IPUx\_IDMAC\_CONF field descriptions

Field	Description
31–26 -	This field is reserved. Reserved, should be cleared.
25 USED_BUFS_EN_R	Enables the limit on the number of pending non real time read requests.
24–21 USED_BUFS_MAX_R	Limit the number of pending non real time read requests. The value can be between 0 to 8. This field has no affect if USED_BUFS_EN_R is cleared
20 USED_BUFS_EN_W	Enables the limit on the number of pending non real time write requests.

Table continues on the next page...

**IPUx\_IDMAC\_CONF field descriptions (continued)**

Field	Description
19–17 USED_BUFS_ MAX_W	<p>Limit the number of pending non real time write requests. The value can be between 0 to 6.</p> <p>This field has no affect if USED_BUFS_EN_W is cleared</p>
16 P_ENDIAN	<p>Pixel Endianness. The pixel Endianness must not be changed while any of the IDMAC channels is enabled.</p> <p>0 little endian</p> <p>1 Big endian</p>
15–6 -	<p>This field is reserved.</p> <p>Reserved, should be cleared.</p>
5 RDI	<p>Read Data Interleaving.</p> <p>This bit must match the slave read data interleaving support. If the AXI slave connected to the IPU supports read data interleaving then this bit must be set. If the AXI slave does not support read data interleaving then the IDMAC can utilize this and issue more address phases on read. In that case it is recommended to have this bit cleared.</p> <p>0 The AXI slave does not support read data interleaving</p> <p>1 The AXI slave supports read data interleaving</p>
4–3 WIDPT	<p>Write Interleaving Depth</p> <p>These 2 bits define the Write Interleaving Depth of the AXI port. This bits should be configured by the user according to the AXI slave's Write Interleaving Depth.</p> <p>WIDPT defines the maximal number of active bursts (yet to be responded) with different IDs. IDMAC will block data phase if the next data's ID is new (no such ID active) and the number of active IDs is equal to WIDPT. 00 Write Interleaving Depth of 1</p> <p>01 Write Interleaving Depth of 2</p> <p>10 Write Interleaving Depth of 3</p> <p>11 Write Interleaving Depth of 4</p>
MAX_REQ_ READ	<p>Maximum Read Requests.</p> <p>This fields sets the maximum pending requests allowed in the AXI Read requests queue.</p>

### 37.5.87 IDMAC Channel Enable 1 Register (IPUx\_IDMAC\_CH\_EN\_1)

Address: Base address + 8004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	IDMAC_CH_EN_31	Reserved	IDMAC_CH_EN_29	IDMAC_CH_EN_28	IDMAC_CH_EN_27	IDMAC_CH_EN_26	IDMAC_CH_EN_25	IDMAC_CH_EN_24	IDMAC_CH_EN_23	IDMAC_CH_EN_22	IDMAC_CH_EN_21	IDMAC_CH_EN_20	IDMAC_CH_EN_19	IDMAC_CH_EN_18	IDMAC_CH_EN_17	Reserved
W																

#### IPUx\_IDMAC\_CH\_EN\_1 field descriptions

Field	Description	
31 IDMAC_CH_EN_31	IDMAC Channel enable bit [i]	
-	0 IDMAC channel is disabled 1 IDMAC channel is enabled	
30	This field is reserved. Reserved.	
29 IDMAC_CH_EN_29	IDMAC Channel enable bit [i]	
-	0 IDMAC channel is disabled 1 IDMAC channel is enabled	
28 IDMAC_CH_EN_28	IDMAC Channel enable bit [i]	
-	0 IDMAC channel is disabled 1 IDMAC channel is enabled	
27 IDMAC_CH_EN_27	IDMAC Channel enable bit [i]	
-	0 IDMAC channel is disabled 1 IDMAC channel is enabled	

Table continues on the next page...

**IPUx\_IDMAC\_CH\_EN\_1 field descriptions (continued)**

Field	Description
26 IDMAC_CH_EN_26	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
25 IDMAC_CH_EN_25	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
24 IDMAC_CH_EN_24	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
23 IDMAC_CH_EN_23	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
22 IDMAC_CH_EN_22	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
21 IDMAC_CH_EN_21	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
20 IDMAC_CH_EN_20	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
19 IDMAC_CH_EN_19	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
18 IDMAC_CH_EN_18	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
17 IDMAC_CH_EN_17	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
16 -	This field is reserved. Reserved.
15 IDMAC_CH_EN_15	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
14 IDMAC_CH_EN_14	IDMAC Channel enable bit [i]

*Table continues on the next page...*

**IPUx\_IDMAC\_CH\_EN\_1 field descriptions (continued)**

Field	Description
	0 IDMAC channel is disabled 1 IDMAC channel is enabled
13 IDMAC_CH_EN_13	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
12 IDMAC_CH_EN_12	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
11 IDMAC_CH_EN_11	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
10 IDMAC_CH_EN_10	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
9 IDMAC_CH_EN_9	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
8 IDMAC_CH_EN_8	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
7–6 -	This field is reserved. Reserved.
5 IDMAC_CH_EN_5	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
4 -	This field is reserved. Reserved.
3 IDMAC_CH_EN_3	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
2 IDMAC_CH_EN_2	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
1 IDMAC_CH_EN_1	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
0 IDMAC_CH_EN_0	IDMAC Channel enable bit [i]

*Table continues on the next page...*

**IPUx\_IDMAC\_CH\_EN\_1 field descriptions (continued)**

Field	Description
	0 IDMACH channel is disabled 1 IDMACH channel is enabled

### 37.5.88 IDMAC Channel Enable 2 Register (IPUx\_IDMAC\_CH\_EN\_2)

Address: Base address + 8008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R												IDMAC_CH_EN_52	IDMAC_CH_EN_51	IDMAC_CH_EN_50	IDMAC_CH_EN_49	IDMAC_CH_EN_48
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_CH_EN_47	IDMAC_CH_EN_46	IDMAC_CH_EN_45	IDMAC_CH_EN_44	IDMAC_CH_EN_43	IDMAC_CH_EN_42	IDMAC_CH_EN_41	IDMAC_CH_EN_40								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_IDMAC\_CH\_EN\_2 field descriptions**

Field	Description
31–21 -	This field is reserved. Reserved.
20 IDMAC_CH_EN_52	IDMAC Channel enable bit [i] 0 IDMACH channel is disabled 1 IDMACH channel is enabled
19 IDMAC_CH_EN_51	IDMAC Channel enable bit [i] 0 IDMACH channel is disabled 1 IDMACH channel is enabled
18 IDMAC_CH_EN_50	IDMAC Channel enable bit [i] 0 IDMACH channel is disabled 1 IDMACH channel is enabled
17 IDMAC_CH_EN_49	IDMAC Channel enable bit [i]

Table continues on the next page...

**IPUx\_IDMAC\_CH\_EN\_2 field descriptions (continued)**

Field	Description
	0 IDMAC channel is disabled 1 IDMAC channel is enabled
16 IDMAC_CH_EN_48	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
15 IDMAC_CH_EN_47	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
14 IDMAC_CH_EN_46	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
13 IDMAC_CH_EN_45	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
12 IDMAC_CH_EN_44	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
11 IDMAC_CH_EN_43	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
10 IDMAC_CH_EN_42	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
9 IDMAC_CH_EN_41	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
8 IDMAC_CH_EN_40	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
7–2 -	This field is reserved. Reserved.
1 IDMAC_CH_EN_33	IDMAC Channel enable bit [i] 0 IDMAC channel is disabled 1 IDMAC channel is enabled
0 -	Reserved.

### 37.5.89 IDMAC Separate Alpha Indication Register (IPUx\_IDMAC\_SEP\_ALPHA)

Address: Base address + 800Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved		IDMAC_SEP_AL_29	Reserved	IDMAC_SEP_AL_27	Reserved	IDMAC_SEP_AL_25	IDMAC_SEP_AL_24	IDMAC_SEP_AL_23							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_SEP_AL_15	IDMAC_SEP_AL_14														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_IDMAC\_SEP\_ALPHA field descriptions

Field	Description
31–30 -	This field is reserved. Reserved.
29 IDMAC_SEP_ AL_29	IDMAC Separate alpha indication bit [i] A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel. In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding. 0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.
28 -	This field is reserved. Reserved.
27 IDMAC_SEP_ AL_27	IDMAC Separate alpha indication bit [i] A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel.

Table continues on the next page...

**IPUx\_IDMAC\_SEP\_ALPHA field descriptions (continued)**

Field	Description
	<p>In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding.</p> <p>0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.</p>
26 -	<p>This field is reserved. Reserved.</p>
25 IDMAC_SEP_AL_25	<p>IDMAC Separate alpha indication bit [i]</p> <p>A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel.</p> <p>In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding.</p> <p>0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.</p>
24 IDMAC_SEP_AL_24	<p>IDMAC Separate alpha indication bit [i]</p> <p>A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel.</p> <p>In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding.</p> <p>0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.</p>
23 IDMAC_SEP_AL_23	<p>IDMAC Separate alpha indication bit [i]</p> <p>A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel.</p> <p>In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding.</p> <p>0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.</p>
22–16 -	<p>This field is reserved. Reserved.</p>
15 IDMAC_SEP_AL_15	<p>IDMAC Separate alpha indication bit [i]</p> <p>A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel.</p> <p>In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding.</p> <p>0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.</p>
14 IDMAC_SEP_AL_14	<p>IDMAC Separate alpha indication bit [i]</p>

*Table continues on the next page...*

**IPUx\_IDMAC\_SEP\_ALPHA field descriptions (continued)**

Field	Description
	<p>A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel.</p> <p>In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding.</p> <p>0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.</p>
-	This field is reserved. Reserved.

### 37.5.90 IDMAC Alternate Separate Alpha Indication Register (IPUx\_IDMAC\_ALT\_SEP\_ALPHA)

Address: Base address + 8010h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			IDMAC_ALT_SEP_AL_29					IDMAC_ALT_SEP_AL_24	IDMAC_ALT_SEP_AL_23							
W			Reserved													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_IDMAC\_ALT\_SEP\_ALPHA field descriptions**

Field	Description
31–30 -	This field is reserved. Reserved.
29 IDMAC_ALT_SEP_AL_29	<p>IDMAC Alternate Separate alpha indication bit [i]</p> <p>A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel.</p> <p>In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding.</p>

*Table continues on the next page...*

**IPUx\_IDMAC\_ALT\_SEP\_ALPHA field descriptions (continued)**

Field	Description
	<p>For channels that may have alternate flow and may use separate alpha. This bit indicates the mode of the alpha for the alternate flow</p> <p>0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.</p>
28–25 -	This field is reserved. Reserved.
24 IDMAC_ALT_SEP_AL_24	<p>IDMAC Alternate Separate alpha indication bit [i]</p> <p>A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel.</p> <p>In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding.</p> <p>For channels that may have alternate flow and may use separate alpha. This bit indicates the mode of the alpha for the alternate flow</p> <p>0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.</p>
23 IDMAC_ALT_SEP_AL_23	<p>IDMAC Alternate Separate alpha indication bit [i]</p> <p>A sub block may need to read data from the system's memory where the pixel data and the alpha transparency data are located in separate buffers. In that case the Alpha transparency data is read by the special Alpha channel.</p> <p>In a case where the alpha should be read from a separate buffer, the user should set the channels corresponding.</p> <p>For channels that may have alternate flow and may use separate alpha. This bit indicates the mode of the alpha for the alternate flow</p> <p>0 Channel [i] does not read Alpha transparency data from a separate buffer. 1 Channel [i] reads Alpha transparency data from a separate buffer.</p>
-	This field is reserved. Reserved.

### 37.5.91 IDMAC Channel Priority 1 Register (IPUx\_IDMAC\_CH\_PRI\_1)

Address: Base address + 8014h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	Reserved		IDMAC_CH_PRI_29	IDMAC_CH_PRI_28	IDMAC_CH_PRI_27	IDMAC_CH_PRI_26	IDMAC_CH_PRI_25	IDMAC_CH_PRI_24	Reserved		IDMAC_CH_PRI_23	IDMAC_CH_PRI_22	IDMAC_CH_PRI_21	IDMAC_CH_PRI_20	Reserved	
W	IDMAC_CH_PRI_15	IDMAC_CH_PRI_14	IDMAC_CH_PRI_13	IDMAC_CH_PRI_12	IDMAC_CH_PRI_11	IDMAC_CH_PRI_10	IDMAC_CH_PRI_9	IDMAC_CH_PRI_8	Reserved		IDMAC_CH_PRI_5	Reserved	IDMAC_CH_PRI_3	IDMAC_CH_PRI_2	IDMAC_CH_PRI_1	IDMAC_CH_PRI_0

IPUx\_IDMAC\_CH\_PRI\_1 field descriptions

Field	Description
31–30 -	This field is reserved. Reserved.
29 IDMAC_CH_PRI_29	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
28 IDMAC_CH_PRI_28	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
27 IDMAC_CH_PRI_27	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
26 IDMAC_CH_PRI_26	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority

Table continues on the next page...

**IPUx\_IDMAC\_CH\_PRI\_1 field descriptions (continued)**

Field	Description
25 IDMAC_CH_PRI_25	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
24 IDMAC_CH_PRI_24	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
23 IDMAC_CH_PRI_23	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
22 IDMAC_CH_PRI_22	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
21 IDMAC_CH_PRI_21	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
20 IDMAC_CH_PRI_20	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
19–16 -	This field is reserved. Reserved.
15 IDMAC_CH_PRI_15	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
14 IDMAC_CH_PRI_14	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
13 IDMAC_CH_PRI_13	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
12 IDMAC_CH_PRI_12	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
11 IDMAC_CH_PRI_11	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
10 IDMAC_CH_PRI_10	IDMAC Channel enable bit [i]

*Table continues on the next page...*

**IPUx\_IDMAC\_CH\_PRI\_1 field descriptions (continued)**

Field	Description
	0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
9 IDMAC_CH_PRI_9	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
8 IDMAC_CH_PRI_8	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
7–6 -	This field is reserved. Reserved.
5 IDMAC_CH_PRI_5	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
4 -	This field is reserved. Reserved.
3 IDMAC_CH_PRI_3	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
2 IDMAC_CH_PRI_2	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
1 IDMAC_CH_PRI_1	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
0 IDMAC_CH_PRI_0	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority

### 37.5.92 IDMAC Channel Priority 2 Register (IPUx\_IDMAC\_CH\_PRI\_2)

Address: Base address + 8018h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_CH_PRI_15	IDMAC_CH_PRI_14	IDMAC_CH_PRI_13	IDMAC_CH_PRI_12	IDMAC_CH_PRI_11	IDMAC_CH_PRI_10	IDMAC_CH_PRI_9	IDMAC_CH_PRI_8								
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_IDMAC\_CH\_PRI\_2 field descriptions

Field	Description
31–19 -	This field is reserved. Reserved.
18 IDMAC_CH_PRI_18	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
17 IDMAC_CH_PRI_17	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
16 IDMAC_CH_PRI_16	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
15 IDMAC_CH_PRI_15	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
14 IDMAC_CH_PRI_14	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority

Table continues on the next page...

**IPUx\_IDMAC\_CH\_PRI\_2 field descriptions (continued)**

Field	Description
13 IDMAC_CH_PRI_13	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
12 IDMAC_CH_PRI_12	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
11 IDMAC_CH_PRI_11	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
10 IDMAC_CH_PRI_10	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
9 IDMAC_CH_PRI_9	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
8 IDMAC_CH_PRI_8	IDMAC Channel enable bit [i] 0 IDMAC channel [i] is in low priority 1 IDMAC channel [i] is in high priority
-	This field is reserved. Reserved.

### 37.5.93 IDMAC Channel Watermark Enable 1 Register (IPUx\_IDMAC\_WM\_EN\_1)

Address: Base address + 801Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	Reserved		IDMAC_WM_EN_29	IDMAC_WM_EN_28	IDMAC_WM_EN_27	IDMAC_WM_EN_26	IDMAC_WM_EN_25	IDMAC_WM_EN_24	Reserved		Reserved					
W																

#### IPUx\_IDMAC\_WM\_EN\_1 field descriptions

Field	Description
31–30 -	This field is reserved. Reserved.
29 IDMAC_WM_EN_29	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
28 IDMAC_WM_EN_28	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
27 IDMAC_WM_EN_27	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
26 IDMAC_WM_EN_26	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled

Table continues on the next page...

**IPUx\_IDMAC\_WM\_EN\_1 field descriptions (continued)**

Field	Description
25 IDMAC_WM_ EN_25	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
24 IDMAC_WM_ EN_24	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
23 IDMAC_WM_ EN_23	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
22–15 -	This field is reserved. Reserved.
14 IDMAC_WM_ EN_14	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
13 IDMAC_WM_ EN_13	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
12 IDMAC_WM_ EN_12	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
11 -	This field is reserved. Reserved.
10 IDMAC_WM_ EN_10	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
9 -	This field is reserved. Reserved.
8 IDMAC_WM_ EN_8	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
7–4 -	This field is reserved. Reserved.
3 IDMAC_WM_ EN_3	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
2 IDMAC_WM_ EN_2	IDMAC Watermark enable bit [i]  0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled

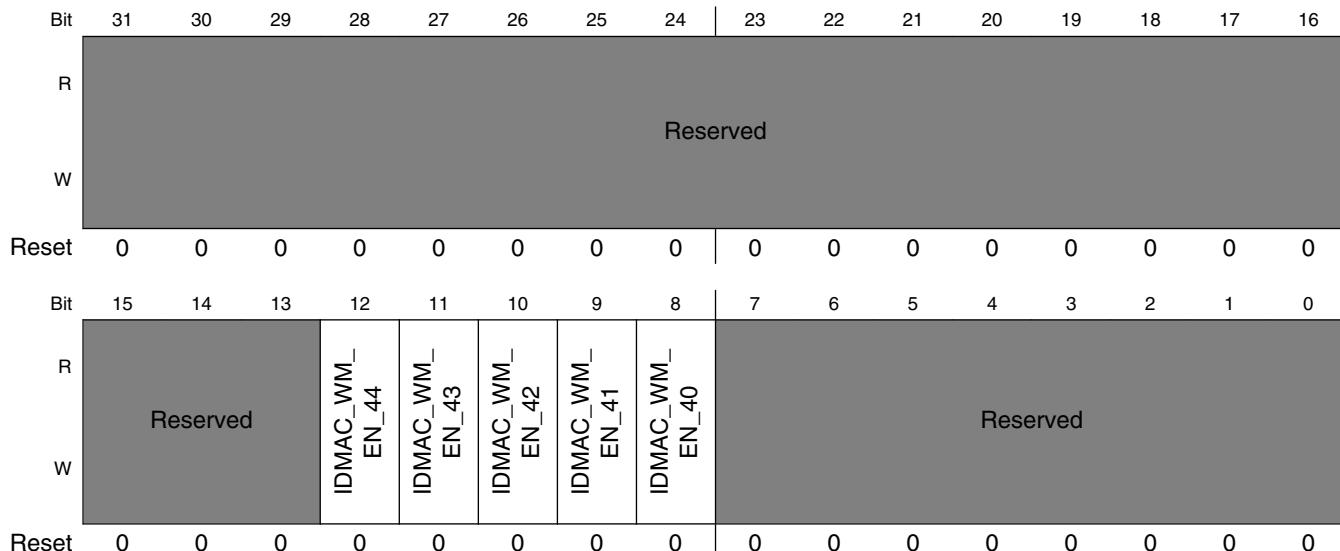
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**IPUx\_IDMAC\_WM\_EN\_1 field descriptions (continued)**

Field	Description
1 IDMAC_WM_ EN_1	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
0 IDMAC_WM_ EN_0	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled

**37.5.94 IDMAC Channel Watermark Enable 2 Register  
(IPUx\_IDMAC\_WM\_EN\_2)**

Address: Base address + 8020h offset

**IPUx\_IDMAC\_WM\_EN\_2 field descriptions**

Field	Description
31–13 -	This field is reserved. Reserved.
12 IDMAC_WM_ EN_44	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
11 IDMAC_WM_ EN_43	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled

*Table continues on the next page...*

**IPUx\_IDMAC\_WM\_EN\_2 field descriptions (continued)**

Field	Description
10 IDMAC_WM_ EN_42	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
9 IDMAC_WM_ EN_41	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
8 IDMAC_WM_ EN_40	IDMAC Watermark enable bit [i] 0 IDMAC channel [i] watermark feature is disabled 1 IDMAC channel [i] watermark feature is enabled
-	This field is reserved. Reserved.

**37.5.95 IDMAC Channel Lock Enable 1 Register  
(IPUx\_IDMAC\_LOCK\_EN\_1)**

Address: Base address + 8024h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved										IDMAC_LOCK_EN_28	IDMAC_LOCK_EN_27	IDMAC_LOCK_EN_23			
W	Reserved															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_LOCK_EN_22	IDMAC_LOCK_EN_21	IDMAC_LOCK_EN_20	IDMAC_LOCK_EN_15	IDMAC_LOCK_EN_14	IDMAC_LOCK_EN_12	IDMAC_LOCK_EN_11	IDMAC_LOCK_EN_5								
W																
Reset																

**IPUx\_IDMAC\_LOCK\_EN\_1 field descriptions**

Field	Description
31–22 -	This field is reserved. Reserved.
21–20 IDMAC_LOCK_ EN_28	IDMAC lock bits for channel [i] 00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
19–18 IDMAC_LOCK_ EN_27	IDMAC lock bits for channel [i]

Table continues on the next page...

**IPUx\_IDMAC\_LOCK\_EN\_1 field descriptions (continued)**

Field	Description
	00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
17–16 IDMAC_LOCK_ EN_23	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
15–14 IDMAC_LOCK_ EN_22	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
13–12 IDMAC_LOCK_ EN_21	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
11–10 IDMAC_LOCK_ EN_20	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
9–8 IDMAC_LOCK_ EN_15	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
7–6 IDMAC_LOCK_ EN_14	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.

*Table continues on the next page...*

**IPUx\_IDMAC\_LOCK\_EN\_1 field descriptions (continued)**

Field	Description
5–4 IDMAC_LOCK_EN_12	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
3–2 IDMAC_LOCK_EN_11	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
IDMAC_LOCK_EN_5	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.

**37.5.96 IDMAC Channel Lock Enable 2Register (IPUx\_IDMAC\_LOCK\_EN\_2)**

Address: Base address + 8028h offset

Bit	31	30	29	28	27	26	25	24	Reserved	23	22	21	20	19	18	17	16
R																	
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	Reserved	7	6	5	4	3	2	1	0
R																	
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_IDMAC\_LOCK\_EN\_2 field descriptions**

Field	Description
31–12 -	This field is reserved. Reserved
11–10 IDMAC_LOCK_50	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request.

Table continues on the next page...

**IPUx\_IDMAC\_LOCK\_EN\_2 field descriptions (continued)**

Field	Description
	10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
9–8 IDMAC_LOCK_ 49	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
7–6 IDMAC_LOCK_ 48	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
5–4 IDMAC_LOCK_ 47	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
3–2 IDMAC_LOCK_ 46	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.
IDMAC_LOCK_ 45	IDMAC lock bits for channel [i]  00 The lock feature is disabled. The IDMAC will generate one AXI burst upon the assertion of the DMA request. 01 The IDMAC will generate two AXI bursts upon the assertion of the DMA request. 10 The IDMAC will generate four AXI bursts upon the assertion of the DMA request. 11 The IDMAC will generate eight AXI bursts upon the assertion of the DMA request.

**37.5.97 IDMAC Channel Alternate Address 0 Register  
(IPUx\_IDMAC\_SUB\_ADDR\_0)**

Address: Base address + 802Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																																	
W																																	

Reset 0

**IPUx\_IDMAC\_SUB\_ADDR\_0 field descriptions**

Field	Description
IDMAC_SUB_ADDR_i	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.

### 37.5.98 IDMAC Channel Alternate Address 1 Register (IPUx\_IDMAC\_SUB\_ADDR\_1)

Address: Base address + 8030h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	R	IDMAC_SUB_ADDR_33								R	IDMAC_SUB_ADDR_29							
	W									W								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	R	IDMAC_SUB_ADDR_24								R	IDMAC_SUB_ADDR_23							
	W									W								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_IDMAC\_SUB\_ADDR\_1 field descriptions**

Field	Description
31 -	This field is reserved. Reserved.
30–24 IDMAC_SUB_ADDR_33	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.
23 -	This field is reserved. Reserved.
22–16 IDMAC_SUB_ADDR_29	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.

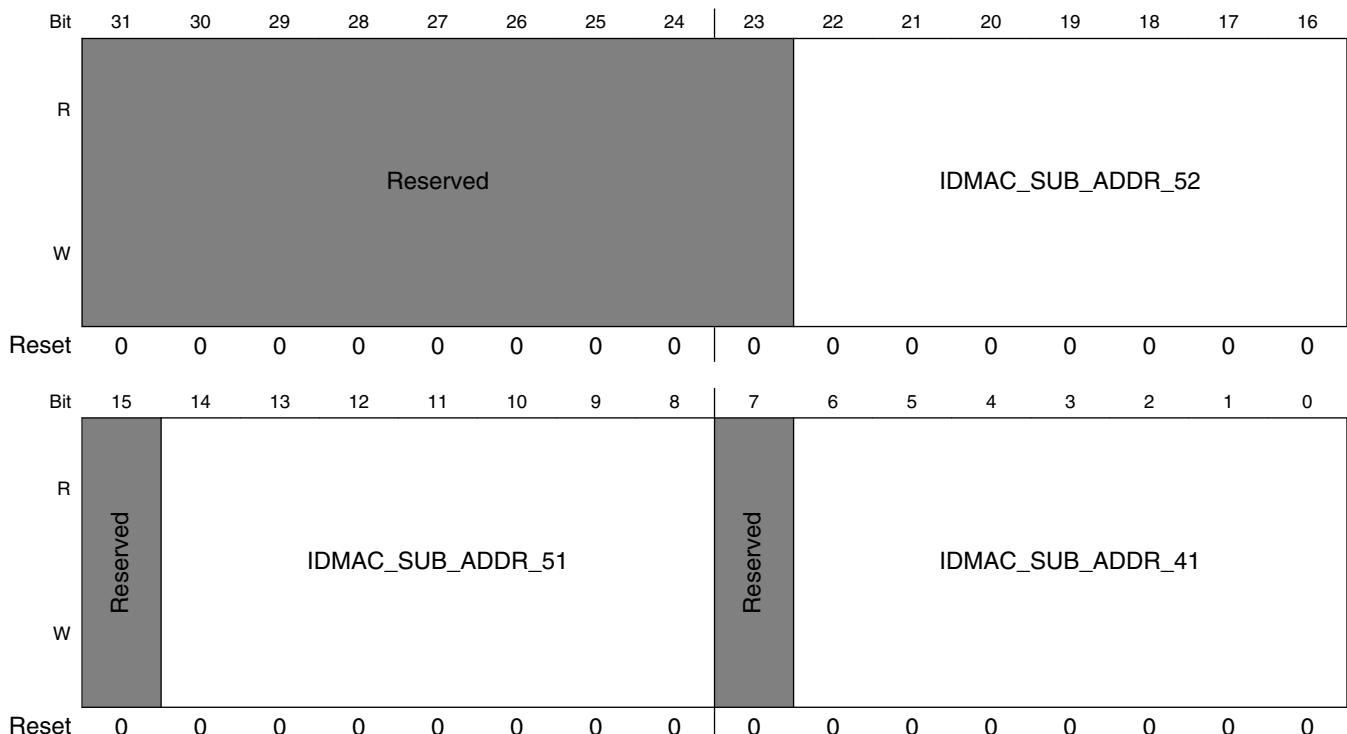
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**IPUx\_IDMAC\_SUB\_ADDR\_1 field descriptions (continued)**

Field	Description
15 -	This field is reserved. Reserved.
14–8 IDMAC_SUB_ ADDR_24	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.
7 -	This field is reserved. Reserved.
IDMAC_SUB_ ADDR_23	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.

### 37.5.99 IDMAC Channel Alternate Address 2 Register (IPUx\_IDMAC\_SUB\_ADDR\_2)

Address: Base address + 8034h offset

**IPUx\_IDMAC\_SUB\_ADDR\_2 field descriptions**

Field	Description
31–23 -	This field is reserved. Reserved.

Table continues on the next page...

**IPUx\_IDMAC\_SUB\_ADDR\_2 field descriptions (continued)**

Field	Description
22–16 IDMAC_SUB_ ADDR_52	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.
15 -	This field is reserved. Reserved.
14–8 IDMAC_SUB_ ADDR_51	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.
7 -	This field is reserved. Reserved.
IDMAC_SUB_ ADDR_41	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.

### 37.5.100 IDMAC Channel Alternate Address 3 Register (IPUx\_IDMAC\_SUB\_ADDR\_3)

Address: Base address + 8038h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved								Reserved							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved								Reserved							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_IDMAC\_SUB\_ADDR\_3 field descriptions**

Field	Description
31 -	This field is reserved. Reserved.
30–24 IDMAC_SUB_ ADDR_27	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.
23 -	This field is reserved. Reserved.
22–16 IDMAC_SUB_ ADDR_13	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.
15 -	This field is reserved. Reserved.
14–8 IDMAC_SUB_ ADDR_10	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.
7 -	This field is reserved. Reserved.
IDMAC_SUB_ ADDR_9	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.

### 37.5.101 IDMAC Channel Alternate Address 4 Register (IPUx\_IDMAC\_SUB\_ADDR\_4)

Address: Base address + 803Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_IDMAC\_SUB\_ADDR\_4 field descriptions

Field	Description
31–23 -	This field is reserved. Reserved.
22–16 IDMAC_SUB_ADDR_21	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.
15 -	This field is reserved. Reserved.
14–8 IDMAC_SUB_ADDR_8	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.
7 -	This field is reserved. Reserved.
IDMAC_SUB_ADDR_28	The CPMEM alternative entry [i] holds the parameters of the channel that is number appears in IDMAC_SUB_ADDR_i. The user must set each IDMAC_SUB_ADDR_i field to a unique channel. Alternative CPMEM entry is relevant only for channels supporting alternate flows.

### 37.5.102 IDMAC Band Mode Enable 1 Register (IPUx\_IDMAC\_BNDM\_EN\_1)

Address: Base address + 8040h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R	Reserved					IDMAC_BNDM_EN_26	IDMAC_BNDM_EN_25	Reserved			IDMAC_BNDM_EN_22	IDMAC_BNDM_EN_21	IDMAC_BNDM_EN_20	Reserved			
W																	

#### IPUx\_IDMAC\_BNDM\_EN\_1 field descriptions

Field	Description
31–27 -	This field is reserved. Reserved.
26 IDMAC_BNDM_EN_26	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode
25 IDMAC_BNDM_EN_25	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode

Table continues on the next page...

**IPUx\_IDMAC\_BNDM\_EN\_1 field descriptions (continued)**

Field	Description
24–23 -	This field is reserved. Reserved.
22 IDMAC_BNDM_EN_22	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode
21 IDMAC_BNDM_EN_21	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode
20 IDMAC_BNDM_EN_20	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode
19–13 -	This field is reserved. Reserved.
12 IDMAC_BNDM_EN_12	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode
11 IDMAC_BNDM_EN_11	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode
10–6 -	This field is reserved. Reserved.
5 IDMAC_BNDM_EN_5	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration.

*Table continues on the next page...*

**IPUx\_IDMAC\_BNDM\_EN\_1 field descriptions (continued)**

Field	Description
	<p>0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode</p>
4 -	This field is reserved. Reserved.
3 IDMAC_BNDM_EN_3	<p>IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration.</p> <p>0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode</p>
2 IDMAC_BNDM_EN_2	<p>IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration.</p> <p>0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode</p>
1 IDMAC_BNDM_EN_1	<p>IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration.</p> <p>0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode</p>
0 IDMAC_BNDM_EN_0	<p>IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration.</p> <p>0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode</p>

### 37.5.103 IDMAC Band Mode Enable 2 Register (IPUx\_IDMAC\_BNDM\_EN\_2)

Address: Base address + 8044h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	[31:0]	[30:0]	[29:0]	[28:0]	[27:0]	[26:0]	[25:0]	[24:0]	[23:0]	[22:0]	[21:0]	[20:0]	[19:0]	IDMAC_BNDM_EN_50	IDMAC_BNDM_EN_49	IDMAC_BNDM_EN_48
W	[31:0]	[30:0]	[29:0]	[28:0]	[27:0]	[26:0]	[25:0]	[24:0]	[23:0]	[22:0]	[21:0]	[20:0]	[19:0]	[18:0]	[17:0]	[16:0]
Reserved	[31:0]	[30:0]	[29:0]	[28:0]	[27:0]	[26:0]	[25:0]	[24:0]	[23:0]	[22:0]	[21:0]	[20:0]	[19:0]	[18:0]	[17:0]	[16:0]
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	IDMAC_BNDM_EN_47	IDMAC_BNDM_EN_46	IDMAC_BNDM_EN_45	[13:0]	[12:0]	[11:0]	[10:0]	[9:0]	[8:0]	[7:0]	[6:0]	[5:0]	[4:0]	[3:0]	[2:0]	[1:0]
W	IDMAC_BNDM_EN_47	IDMAC_BNDM_EN_46	IDMAC_BNDM_EN_45	[13:0]	[12:0]	[11:0]	[10:0]	[9:0]	[8:0]	[7:0]	[6:0]	[5:0]	[4:0]	[3:0]	[2:0]	[1:0]
Reserved	[15:0]	[14:0]	[13:0]	[12:0]	[11:0]	[10:0]	[9:0]	[8:0]	[7:0]	[6:0]	[5:0]	[4:0]	[3:0]	[2:0]	[1:0]	[0:0]

#### IPUx\_IDMAC\_BNDM\_EN\_2 field descriptions

Field	Description
31–19 -	This field is reserved. Reserved.
18 IDMAC_BNDM_EN_50	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode
17 IDMAC_BNDM_EN_49	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMAC channel [i] is not in band mode 1 IDMAC channel [i] is in band mode
16 IDMAC_BNDM_EN_48	IDMAC Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration.

Table continues on the next page...

**IPUx\_IDMAC\_BNDM\_EN\_2 field descriptions (continued)**

Field	Description
	0 IDMACH channel [i] is not in band mode 1 IDMACH channel [i] is in band mode
15 IDMAC_BNDM_EN_47	IDMACH Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMACH channel [i] is not in band mode 1 IDMACH channel [i] is in band mode
14 IDMAC_BNDM_EN_46	IDMACH Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMACH channel [i] is not in band mode 1 IDMACH channel [i] is in band mode
13 IDMAC_BNDM_EN_45	IDMACH Band Mode Enable bit [i] This bit controls if the channel currently works in band mode. When alternate flow is running via this channel, both the main flow and the alternate flow should have the same band mode configuration. 0 IDMACH channel [i] is not in band mode 1 IDMACH channel [i] is in band mode
-	This field is reserved. Reserved.

### 37.5.104 IDMAC Scroll Coordinations Register (IPUx\_IDMAC\_SC\_CORD)

Address: Base address + 8048h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W	Reserved				SX0								Reserved				SY0															

Reset 0

**IPUx\_IDMAC\_SC\_CORD field descriptions**

Field	Description
31–28 -	This field is reserved. Reserved, should be cleared.
27–16 SX0	Scroll X coordination This field indicates the X coordinate of the scroll. This parameter has an affect on continuos scroll mode only. Units are pixels. When the alpha buffer resides in a separate buffer and the alpha is different than 8 BPP this field should be 0.

Table continues on the next page...

**IPUx\_IDMAC\_SC\_CORD field descriptions (continued)**

Field	Description
15–11 -	This field is reserved. Reserved, should be cleared.
SY0	Scroll Y coordination  This field indicates the Y coordinate of the scroll. This parameter has an affect on continuos scroll mode only. Units are pixels. When the alpha buffer resides in a separate buffer and the alpha is different than 8 BPP this field should be 0.

**37.5.105 IDMAC Scroll Coordinations Register 1  
(IPUx\_IDMAC\_SC\_CORD\_1)**

Address: Base address + 804Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved				SX1								Reserved				SY1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_IDMAC\_SC\_CORD\_1 field descriptions**

Field	Description
31–28 -	This field is reserved. Reserved, should be cleared.
27–16 SX1	Scroll X coordination (2nd set)  This field indicates the X coordinate of the scroll. This parameter has an affect on continuos scroll mode only. Units are pixels. When the alpha buffer resides in a separate buffer and the alpha is different than 8 BPP this field should be 0.
15–11 -	This field is reserved. Reserved, should be cleared.
SY1	Scroll Y coordination (2nd set)  This field indicates the Y coordinate of the scroll. This parameter has an affect on continuos scroll mode only. Units are pixels. When the alpha buffer resides in a separate buffer and the alpha is different than 8 BPP this field should be 0.

### 37.5.106 IDMAC Channel Busy 1 Register (IPUx\_IDMAC\_CH\_BUSY\_1)

Address: Base address + 8100h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	IDMAC_CH_BUSY_	Reserved	IDMAC_CH_BUSY_29	IDMAC_CH_BUSY_28	IDMAC_CH_BUSY_27	IDMAC_CH_BUSY_26	IDMAC_CH_BUSY_25	IDMAC_CH_BUSY_24	IDMAC_CH_BUSY_23	IDMAC_CH_BUSY_22	IDMAC_CH_BUSY_21	IDMAC_CH_BUSY_20	Reserved	IDMAC_CH_BUSY_18	IDMAC_CH_BUSY_17	Reserved
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	IDMAC_CH_BUSY_15	IDMAC_CH_BUSY_14	IDMAC_CH_BUSY_13	IDMAC_CH_BUSY_12	IDMAC_CH_BUSY_11	IDMAC_CH_BUSY_10	IDMAC_CH_BUSY_9	IDMAC_CH_BUSY_8	Reserved		IDMAC_CH_BUSY_5	Reserved		IDMAC_CH_BUSY_3	IDMAC_CH_BUSY_2	IDMAC_CH_BUSY_1	IDMAC_CH_BUSY_0
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_IDMAC\_CH\_BUSY\_1 field descriptions**

Field	Description
31 IDMAC_CH_BUSY_	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
30 -	This field is reserved. Reserved.
29 IDMAC_CH_BUSY_29	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
28 IDMAC_CH_BUSY_28	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC.

*Table continues on the next page...*

**IPUx\_IDMAC\_CH\_BUSY\_1 field descriptions (continued)**

Field	Description
	0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
27 IDMAC_CH_BUSY_27	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
26 IDMAC_CH_BUSY_26	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
25 IDMAC_CH_BUSY_25	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
24 IDMAC_CH_BUSY_24	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
23 IDMAC_CH_BUSY_23	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
22 IDMAC_CH_BUSY_22	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
21 IDMAC_CH_BUSY_21	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy

*Table continues on the next page...*

**IPUx\_IDMAC\_CH\_BUSY\_1 field descriptions (continued)**

Field	Description
20 IDMAC_CH_BUSY_20	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
19 -	This field is reserved. Reserved.
18 IDMAC_CH_BUSY_18	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
17 IDMAC_CH_BUSY_17	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
16 -	This field is reserved. Reserved.
15 IDMAC_CH_BUSY_15	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
14 IDMAC_CH_BUSY_14	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
13 IDMAC_CH_BUSY_13	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
12 IDMAC_CH_BUSY_12	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC.

*Table continues on the next page...*

**IPUx\_IDMAC\_CH\_BUSY\_1 field descriptions (continued)**

Field	Description
	0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
11 IDMAC_CH_BUSY_11	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
10 IDMAC_CH_BUSY_10	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
9 IDMAC_CH_BUSY_9	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
8 IDMAC_CH_BUSY_8	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
7–6 -	This field is reserved. Reserved.
5 IDMAC_CH_BUSY_5	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
4 -	This field is reserved. Reserved.
3 IDMAC_CH_BUSY_3	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
2 IDMAC_CH_BUSY_2	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC.

*Table continues on the next page...*

**IPUx\_IDMAC\_CH\_BUSY\_1 field descriptions (continued)**

Field	Description
	<p>This bit is self cleared by the IDMAC.</p> <p>0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy</p>
1 IDMAC_CH_ BUSY_1	<p>IDMAC Channel busy bit [i]</p> <p>This bit indicates if the channel is currently served by the IDMAC.</p> <p>This bit is self cleared by the IDMAC.</p> <p>0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy</p>
0 IDMAC_CH_ BUSY_0	<p>IDMAC Channel busy bit [i]</p> <p>This bit indicates if the channel is currently served by the IDMAC.</p> <p>This bit is self cleared by the IDMAC.</p> <p>0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy</p>

### 37.5.107 IDMAC Channel Busy 2 Register (IPUx\_IDMAC\_CH\_BUSY\_2)

Address: Base address + 8104h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R												IDMAC_CH_BUSY_52	IDMAC_CH_BUSY_51	IDMAC_CH_BUSY_50	IDMAC_CH_BUSY_49	IDMAC_CH_BUSY_48
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IDMAC_CH_BUSY_47	IDMAC_CH_BUSY_46	IDMAC_CH_BUSY_45	IDMAC_CH_BUSY_44	IDMAC_CH_BUSY_43	IDMAC_CH_BUSY_42	IDMAC_CH_BUSY_41	IDMAC_CH_BUSY_40	Reserved						IDMAC_CH_BUSY_33	
W																Reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_IDMAC\_CH\_BUSY\_2 field descriptions**

Field	Description
31–21 -	This field is reserved. Reserved.
20 IDMAC_CH_ BUSY_52	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
19 IDMAC_CH_ BUSY_51	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
18 IDMAC_CH_ BUSY_50	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC.

Table continues on the next page...

**IPUx\_IDMAC\_CH\_BUSY\_2 field descriptions (continued)**

Field	Description
	0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
17 IDMAC_CH_BUSY_49	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
16 IDMAC_CH_BUSY_48	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
15 IDMAC_CH_BUSY_47	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
14 IDMAC_CH_BUSY_46	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
13 IDMAC_CH_BUSY_45	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
12 IDMAC_CH_BUSY_44	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
11 IDMAC_CH_BUSY_43	IDMAC Channel busy bit [i] This bit indicates if the channel is currently served by the IDMAC. This bit is self cleared by the IDMAC. 0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy

*Table continues on the next page...*

**IPUx\_IDMAC\_CH\_BUSY\_2 field descriptions (continued)**

Field	Description
10 IDMAC_CH_ BUSY_42	IDMAC Channel busy bit [i]  This bit indicates if the channel is currently served by the IDMAC.  This bit is self cleared by the IDMAC.  0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
9 IDMAC_CH_ BUSY_41	IDMAC Channel busy bit [i]  This bit indicates if the channel is currently served by the IDMAC.  This bit is self cleared by the IDMAC.  0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
8 IDMAC_CH_ BUSY_40	IDMAC Channel busy bit [i]  This bit indicates if the channel is currently served by the IDMAC.  This bit is self cleared by the IDMAC.  0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
7–2 -	This field is reserved. Reserved.
1 IDMAC_CH_ BUSY_33	IDMAC Channel busy bit [i]  This bit indicates if the channel is currently served by the IDMAC.  This bit is self cleared by the IDMAC.  0 IDMAC channel [i] is not busy 1 IDMAC channel [i] is busy
0 -	This field is reserved. Reserved.

### 37.5.108 DP Common Configuration Sync Flow Register (IPUx\_DP\_COM\_CONF\_SYNC)

This register contains common configuration parameters for the DP.

Address: Base address + 1\_8000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		DP_GAMMA_YUV_EN_SYNC	DP_GAMMA_EN_SYNC	DP_CSC_YUV_SAT_MODE_SYNC	DP_CSC_YUV_SYNC	DP_CSC_GAMUT_DEF_SYNC		0				DP_GWCKE_SYNC	DP_GWAM_SYNC	DP_GWSEL_SYNC	DP_FG_EN_SYNC
W													DP_CO_C_SYNC			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DP\_COM\_CONF\_SYNC field descriptions

Field	Description
31–14 Reserved	This read-only field is reserved and always has the value 0.
13 DP_GAMMA_YUV_EN_SYNC	GAMMA's YUV mode enable for sync flow 0 YUV mode is OFF. 1 YUV mode is ON.
12 DP_GAMMA_EN_SYNC	GAMMA_EN - Gamma correction block enable bit 0 disable 1 enable
11 DP_CSC_YUV_SAT_MODE_SYNC	CSC_YUV_SAT_MODE YUV saturation mode for color space conversion 0 Y/U/V range 0 -255 1 Y range 16-235, U/V range 16-240

Table continues on the next page...

**IPUx\_DP\_COM\_CONF\_SYNC field descriptions (continued)**

Field	Description
10 DP_CSC_GAMUT_SAT_EN_SYNC	CSC_GAMUT_SAT_EN Indicate if GAMUT saturation is enabled 0 disable GAMUT mapping 1 enable GAMUT mapping
9–8 DP_CSC_DEF_SYNC	CSC_DEF Enable or disable Color Space Conversion. 00 CSC disable 01 CSC enable after combining 10 CSC enable before combining on BG channel 11 CSC enable before combining on FG channel
7 Reserved	This read-only field is reserved and always has the value 0.
6–4 DP_CO_COC_SYNC	CO_COC - Cursor Operation Control Controls the format of the cursor and the type of arithmetic operations 000 Transparent, cursor is disabled. 001 Full cursor. 010 Reversed cursor. 011 AND between full plane and cursor. 100 Reserved 101 OR between full plane and cursor. 110 XOR between full plane and cursor. 111 Reserved.
3 DP_GWCKE_SYNC	GWCKE - Graphic Window Color Keying Enable Enable or disable graphic window color keying. 1 Enable color keying of graphic window 0 Disable color keying of graphic window
2 DP_GWAM_SYNC	GWAM - Graphic Window Alpha Mode Select the use of Alpha to be global or local. 1 Global Alpha. 0 Local Alpha.
1 DP_GWSEL_SYNC	GWSEL - Graphic Window Select Select graphic window to be on partial plane or full plane. 1 Graphic window is partial plane. 0 Graphic window is full plane.
0 DP_FG_EN_SYNC	FG_EN - partial plane Enable. This bit enables the partial plane channel. 1 partial plane channel is enabled. 0 partial plane channel is disabled.

### 37.5.109 DP Graphic Window Control Sync Flow Register (IPUx\_DP\_Graph\_Wind\_CTRL\_SYNC)

This register contains common configuration parameters for the DP.

Address: Base address + 1\_8004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

#### IPUx\_DP\_Graph\_Wind\_CTRL\_SYNC field descriptions

Field	Description
31–24 DP_GWAV_SYNC	<p>GWAV - Graphic Window Alpha Value</p> <p>Defines the alpha value of graphic window used for alpha blending between graphic window and full plane. The Value the number that writing to GWAV register. The Actual Value the number, that insert to calculation in Combining Module. If Value = &lt; 0.5- 1/256 (01111111) then Actual Value = Value. If Value &gt;= 0.5 (10000000), then Actual Value = Value + 1/256.</p> <p>00000000 Actual value is 00000000; Graphic window totally opaque i.e. overlay on LCD screen            01111111 Actual value is 01111111;            10000000 Actual value is 10000001            10000001 Actual value is 10000010            11111110 Actual value is 11111111            11111111 Actual value is 100000000;Graphic window totally transparent i.e. not displayed on LCD screen</p>
23–16 DP_GWCKR_SYNC	<p>GWCKR - Graphic Window Color Keying Red Component</p> <p>Defines the red component of graphic window color keying.</p> <p>00000000 No red            11111111 Full red</p>
15–8 DP_GWCKG_SYNC	<p>GWCKG - Graphic Window Color Keying Green Component</p> <p>Defines the green component of graphic window color keying.</p> <p>00000000 No Green            11111111 Full Green</p>
DP_GWCKB_SYNC	<p>GWCKB - Graphic Window Color Keying Blue Component</p> <p>Defines the blue component of graphic window color keying.</p> <p>00000000 No blue            11111111 Full blue</p>

### 37.5.110 DP Partial Plane Window Position Sync Flow Register (IPUx\_DP\_FG\_POS\_SYNC)

The DP partial plane Window Position Register is used to determine the starting position of the partial plane window relative to BG window position.

This Register is used for the synchronous flow only.

Address: Base address + 1\_8008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_DP\_FG\_POS\_SYNC field descriptions

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 DP_FGXP_SYNC	FGXP partial plane Window X Position. partial plane Window X Position - Specifies the number of pixels between the start of full plane window X position and the beginning of the first data of new line.
15–11 Reserved	This read-only field is reserved and always has the value 0.
DP_FGYP_SYNC	FGYP partial plane window Y position partial plane Window Y Position - Specifies the number of lines between the start of full plane windows Y position and the beginning of the first data.

### 37.5.111 DP Cursor Position and Size Sync Flow Register (IPUx\_DP\_CUR\_POS\_SYNC)

The LCD Cursor Position Register is used to determine the starting position of the cursor relative to BG windows position.

Address: Base address + 1\_800Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																																		
W	DP_CYP_SYNC																DP_CYH_SYNC																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

**IPUx\_DP\_CUR\_POS\_SYNC field descriptions**

Field	Description
31–27 DP_CYP_SYNC	CYP - Cursor Y Position Represents the cursors vertical starting position Y in pixel count (from 0 to CYH).Live View Resolution Mode.
26–16 DP_CYH_SYNC	CYH - Cursor Height Specifies the height of the hardware cursor in pixels.
15–11 DP_CXP_SYNC	CXP - Cursor X Position Represents the cursors horizontal starting position X in pixel count (from 0 to CXW).
DP_CXW_SYNC	CXW - Cursor Width. Specifies the width of the hardware cursor in pixels.

### 37.5.112 DP Color Cursor Mapping Sync Flow Register (IPUx\_DP\_CUR\_MAP\_SYNC)

The LCD Color Cursor Mapping Register defines the color of the cursor in passive or TFT color modes.

Address: Base address + 1\_8010h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				DP_CUR_COL_B_SYNC				DP_CUR_COL_G_SYNC				DP_CUR_COL_R_SYNC																			
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DP\_CUR\_MAP\_SYNC field descriptions**

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23–16 DP_CUR_COL_B_SYNC	CUR_COL_B - Cursor Blue Field Defines the Blue component of the cursor color in color mode 00000000 No Blue. 11111111 Full Blue.
15–8 DP_CUR_COL_G_SYNC	CUR_COL_G - Cursor Green Field Defines the Green component of the cursor color in color mode 00000000 No Green. 11111111 Full Green.
DP_CUR_COL_R_SYNC	CUR_COL_B - Cursor Red Field Defines the Red component of the cursor color in color mode

*Table continues on the next page...*

**IPUx\_DP\_CUR\_MAP\_SYNC field descriptions (continued)**

Field	Description															
	00000000 No Red. 11111111 Full Red.															

**37.5.113 DP Gamma Constants Sync Flow Register i  
(IPUx\_DP\_GAMMA\_C\_SYNC\_i)**

This registers contains CONSTANTi parameters used for gamma correction inside the display processor (DP).

Address: Base address + 1\_8014h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DP\_GAMMA\_C\_SYNC\_i field descriptions**

Field	Description																								
31–25 Reserved	This read-only field is reserved and always has the value 0.																								
24–16 DP_GAMMA_C_SYNC_2i_1	CONSTANTi+1 parameter of Gamma Correction.																								
15–9 Reserved	This read-only field is reserved and always has the value 0.																								
DP_GAMMA_C_SYNC_2i	CONSTANTi parameter of Gamma Correction.																								

**37.5.114 DP Gamma Correction Slope Sync Flow Register i  
(IPUx\_DP\_GAMMA\_S\_SYNC\_i)**

This registers contains SLOPEi parameters used for Gamma Correction inside the display processor (DP).

Address: Base address + 1\_8034h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DP\_GAMMA\_S\_SYNC\_i field descriptions**

Field	Description
31–24 DP_GAMMA_S_SYNC_4i_3	SLOPE<4*i+3> parameter of Gamma Correction.
23–16 DP_GAMMA_S_SYNC_4i_2	SLOPE<4*i+2> parameter of Gamma Correction.
15–8 DP_GAMMA_S_SYNC_4i_1	SLOPE<4*i+1> parameter of Gamma Correction.
DP_GAMMA_S_SYNC_4i	SLOPE<4*i> parameter of Gamma Correction.

**37.5.115 DP Color Space Conversion Control Sync Flow Registers (IPUx\_DP\_CSCA\_SYNC\_i)**

Address: Base address + 1\_8044h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DP\_CSCA\_SYNC\_i field descriptions**

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.
25–16 DP_CSC_A_SYNC_2i_1	A<2*i+1> parameter of color conversion
15–10 Reserved	This read-only field is reserved and always has the value 0.
DP_CSC_A_SYNC_2i	A<2*i> parameter of color conversion.

### 37.5.116 DP Color Conversion Control Sync Flow Register 0 (IPUx\_DP\_SCS\_SYNC\_0)

Address: Base address + 1\_8054h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DP_CSC_S0_SYNC															
W	DP_CSC_B0_SYNC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W	DP_CSC_A8_SYNC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DP\_SCS\_SYNC\_0 field descriptions

Field	Description
31–30 DP_CSC_S0_SYNC	S0 parameter of color conversion. 00 scale factor of 2 01 scale factor of 1 10 scale factor of 0 11 scale factor of -1
29–16 DP_CSC_B0_SYNC	B0 parameter of color conversion.
15–10 Reserved	This read-only field is reserved and always has the value 0.
DP_CSC_A8_SYNC	A9 parameter of color conversion.

### 37.5.117 DP Color Conversion Control Sync Flow Register 1 (IPUx\_DP\_SCS\_SYNC\_1)

Address: Base address + 1\_8058h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DP_CSC_S2_SYNC															
W	DP_CSC_B2_SYNC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DP_CSC_S1_SYNC															
W	DP_CSC_B1_SYNC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DP\_SCS\_SYNC\_1 field descriptions**

Field	Description
31–30 DP_CSC_S2_SYNC	S0 parameter of color conversion. 00 scale factor of 2 01 scale factor of 1 10 scale factor of 0 11 scale factor of -1
29–16 DP_CSC_B2_SYNC	B0 parameter of color conversion.
15–14 DP_CSC_S1_SYNC	S0 parameter of color conversion. 00 scale factor of 2 01 scale factor of 1 10 scale factor of 0 11 scale factor of -1
DP_CSC_B1_SYNC	B0 parameter of color conversion.

### 37.5.118 DP Cursor Position and Size Alternate Register (IPUx\_DP\_CUR\_POS\_ALT)

The LCD Cursor Position Register is used to determine the starting position of the cursor relative to BG windows position for the alternative flow.

Address: Base address + 1\_805Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	DP_CYP_SYNC_ALT				DP_CYH_SYNC_ALT				DP_CXP_SYNC_ALT				DP_CXW_SYNC_ALT																				
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DP\_CUR\_POS\_ALT field descriptions**

Field	Description
31–27 DP_CYP_SYNC_ALT	CYP_ALT - Cursor Y Position Represents the cursors vertical starting position Y in pixel count (from 0 to CYH).Live View Resolution Mode for the alternative flow.
26–16 DP_CYH_SYNC_ALT	CYH_ALT - Cursor Height Specifies the height of the hardware cursor in pixels.
15–11 DP_CXP_SYNC_ALT	CXP_ALT - Cursor X Position Represents the cursors horizontal starting position X in pixel count (from 0 to CXW) for the alternative flow.

Table continues on the next page...

**IPUx\_DP\_CUR\_POS\_ALT field descriptions (continued)**

Field	Description
DP_CXW_SYNC_ALT	CXW_ALT - Cursor Width. Specifies the width of the hardware cursor in pixels for the alternative flow.

### 37.5.119 DP Common Configuration Async 0 Flow Register (IPUx\_DP\_COM\_CONF\_ASYNC0)

This register contains common configuration parameters for the DP.

Address: Base address + 1\_8060h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		DP_GAMMA_YUV_EN_ASYNC0	DP_GAMMA_EN_ASYNC0	DP_CSC_YUV_SAT_MODE_ASYNC0	DP_CSC_GAMUT_SAT_EN_ASYNC0		0					DP_GWCKE_ASYNC0	DP_GWAM_ASYNC0	DP_GWSEL_ASYNC0	0
W													DP_CO_C_ASYNC0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DP\_COM\_CONF\_ASYNC0 field descriptions**

Field	Description
31–14 Reserved	This read-only field is reserved and always has the value 0.
13 DP_GAMMA_YUV_EN_ASYNC0	GAMMA's YUV mode enable for async flow 0 0 YUV mode is OFF. 1 YUV mode is ON.
12 DP_GAMMA_EN_ASYNC0	GAMMA_EN - Gamma correction block enable bit

*Table continues on the next page...*

**IPUx\_DP\_COM\_CONF\_ASYNC0 field descriptions (continued)**

Field	Description
	0 disable 1 enable
11 DP_CSC_YUV_SAT_MODE_ASYNC0	<b>CSC_YUV_SAT_MODE</b> YUV saturation mode for color space conversion 0 Y/U/V range 0 -255 1 Y range 16-235, U/V range 16-240
10 DP_CSC_GAMUT_SAT_EN_ASYNC0	<b>CSC_GAMUT_SAT_EN</b> Indicate if GAMUT saturation is enabled 0 disable GAMUT mapping 1 enable GAMUT mapping
9–8 DP_CSC_DEF_ASYNC0	<b>CSC_DEF</b> Enable or disable Color Space Conversion. 00 CSC disable 01 CSC enable after combining 10 CSC enable before combining on BG channel 11 CSC enable before combining on FG channel
7 Reserved	This read-only field is reserved and always has the value 0.
6–4 DP_CO_COC_ASYNC0	<b>CO_COC</b> - Cursor Operation Control Controls the format of the cursor and the type of arithmetic operations 000 Transparent, cursor is disabled. 001 Full cursor. 010 Reversed cursor. 011 AND between full plane and cursor. 100 Reserved 101 OR between full plane and cursor. 110 XOR between full plane and cursor. 111 Reserved
3 DP_GWCKE_ASYNC0	<b>GWCKE</b> - Graphic Window Color Keying Enable Enable or disable graphic window color keying. 1 Enable color keying of graphic window 0 Disable color keying of graphic window
2 DP_GWAM_ASYNC0	<b>GWAM</b> - Graphic Window Alpha Mode Select the use of Alpha to be global or local. 1 Global Alpha. 0 Local Alpha.
1 DP_GWSEL_ASYNC0	<b>GWSEL</b> - Graphic Window Select Select graphic window to be on partial plane or full plane.

*Table continues on the next page...*

**IPUx\_DP\_COM\_CONF\_ASYNC0 field descriptions (continued)**

Field	Description
	1 Graphic window is partial plane. 0 Graphic window is full plane.5
0 Reserved	This read-only field is reserved and always has the value 0.

### 37.5.120 DP Graphic Window Control Async 0 Flow Register (IPUx\_DP\_GRAPH\_WIND\_CTRL\_ASYNC0)

This register contains common configuration parameters for the DP.

Address: Base address + 1\_8064h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																																		
W																																		

Reset 0

**IPUx\_DP\_GRAPH\_WIND\_CTRL\_ASYNC0 field descriptions**

Field	Description
31–24 DP_GWAV_ASYNC0	GWAV - Graphic Window Alpha Value  Defines the alpha value of graphic window used for alpha blending between graphic window and full plane. The Value the number that writing to GWAV register. The Actual Value the number, that insert to calculation in Combining Module. If Value = < 0.5- 1/256 (01111111) then Actual Value = Value. If Value >= 0.5 (10000000), then Actual Value = Value + 1/256.  00000000 Actual value is 00000000; Graphic window totally opaque i.e. overlay on LCD screen 01111111 Actual value is 01111111; 10000000 Actual value is 10000001 10000001 Actual value is 10000010 11111110 Actual value is 11111111 11111111 Actual value is 100000000;Graphic window totally transparent i.e. not displayed on LCD screen
23–16 DP_GWCKR_ASYNC0	GWCKR - Graphic Window Color Keying Red Component  Defines the red component of graphic window color keying.  00000000 No red 11111111 Full red
15–8 DP_GWCKG_ASYNC0	GWCKG - Graphic Window Color Keying Green Component  Defines the green component of graphic window color keying.  00000000 No Green 11111111 Full Green

Table continues on the next page...

**IPUx\_DP\_GRAPH\_WIND\_CTRL\_ASYNC0 field descriptions (continued)**

Field	Description
DP_GWCKB_ASYNC0	GWCKB - Graphic Window Color Keying Blue Component Defines the blue component of graphic window color keying.  00000000 No blue 11111111 Full blue

### 37.5.121 DP Partial Plane Window Position Async 0 Flow Register (IPUx\_DP\_FG\_POS\_ASYNC0)

The DP partial plane Window Position Register is used to determine the starting position of the partial plane window relative to BG window position.

This Register is used for the synchronous flow only.

Address: Base address + 1\_8068h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DP\_FG\_POS\_ASYNC0 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 DP_FGXP_ASYNC0	FGXP partial plane Window X Position. partial plane Window X Position - Specifies the number of pixels between the start of full plane window X position and the beginning of the first data of new line.
15–11 Reserved	This read-only field is reserved and always has the value 0.
DP_FGYP_ASYNC0	FGYP partial plane window Y position partial plane Window Y Position - Specifies the number of lines between the start of full plane windows Y position and the beginning of the first data.

### 37.5.122 DP Cursor Position and Size Async 0 Flow Register (IPUx\_DP\_CUR\_POS\_ASYNC0)

The LCD Cursor Position Register is used to determine the starting position of the cursor relative to BG windows position.

Address: Base address + 1\_806Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DP_CYP_ASYNC0				DP_CYH_ASYNC0								DP_CXP_ASYNC0				DP_CXW_ASYNC0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_DP\_CUR\_POS\_ASYNC0 field descriptions

Field	Description
31–27 DP_CYP_ASYNC0	CYP - Cursor Y Position Represents the cursors vertical starting position Y in pixel count (from 0 to CYH).Live View Resolution Mode.
26–16 DP_CYH_ASYNC0	CYH - Cursor Height Specifies the height of the hardware cursor in pixels.
15–11 DP_CXP_ASYNC0	CXP - Cursor X Position Represents the cursors horizontal starting position X in pixel count (from 0 to CXW).
DP_CXW_ASYNC0	CXW - Cursor Width. Specifies the width of the hardware cursor in pixels.

### 37.5.123 DP Color Cursor Mapping Async 0 Flow Register (IPUx\_DP\_CUR\_MAP\_ASYNC0)

The LCD Color Cursor Mapping Register defines the color of the cursor in passive or TFT color modes.

Address: Base address + 1\_8070h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				DP_CUR_COL_B_ASYNC0								DP_CUR_COL_G_ASYNC0				DP_CUR_COL_R_ASYNC0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DP\_CUR\_MAP\_ASYNC0 field descriptions**

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23–16 DP_CUR_COL_B_ASYNC0	CUR_COL_B - Cursor Blue Field Defines the Blue component of the cursor color in color mode 00000000 No Blue. 11111111 Full Blue.
15–8 DP_CUR_COL_G_ASYNC0	CUR_COL_G - Cursor Green Field Defines the Green component of the cursor color in color mode 00000000 No Green. 11111111 Full Green.
DP_CUR_COL_R_ASYNC0	CUR_COL_R - Cursor Red Field Defines the Red component of the cursor color in color mode 00000000 No Red. 11111111 Full Red.

**37.5.124 DP Gamma Constant Async 0 Flow Register i  
(IPUx\_DP\_GAMMA\_C\_ASYNC0\_i)**

This register contains CONSTANTi parameters used for gamma correction inside the display processor (DP).

Address: Base address + 1\_8074h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R	0																0																	
W																																		

Reset 0

**IPUx\_DP\_GAMMA\_C\_ASYNC0\_i field descriptions**

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 DP_GAMMA_C_ASYNC0_2i_1	CONSTANTi+1 parameter of Gamma Correction.
15–9 Reserved	This read-only field is reserved and always has the value 0.
DP_GAMMA_C_ASYNC0_2i	CONSTANTi parameter of Gamma Correction.

### 37.5.125 DP Gamma Correction Slope Async 0 Flow Register i (IPUx\_DP\_GAMMA\_S\_ASYNC0\_i)

This register contains SLOPE $i$  parameters used for Gamma Correction inside the display processor (DP).

Address: Base address + 1\_8094h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DP_GAMMA_S_ASYNC0_4i_3				DP_GAMMA_S_ASYNC0_4i_2				DP_GAMMA_S_ASYNC0_4i_1				DP_GAMMA_S_ASYNC0_4i																			
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

IPUx\_DP\_GAMMA\_S\_ASYNC0\_i field descriptions

Field	Description																												
31–24 DP_GAMMA_S_ASYNC0_4i_3	SLOPE<4*i+3> parameter of Gamma Correction.																												
23–16 DP_GAMMA_S_ASYNC0_4i_2	SLOPE<4*i+2> parameter of Gamma Correction.																												
15–8 DP_GAMMA_S_ASYNC0_4i_1	SLOPE<4*i+1> parameter of Gamma Correction.																												
DP_GAMMA_S_ASYNC0_4i	SLOPE<4*i> parameter of Gamma Correction.																												

### 37.5.126 DP Color Space Conversion Control Async 0 Flow Register i (IPUx\_DP\_CSCA\_ASYNC0\_i)

Address: Base address + 1\_80A4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				DP_CSC_A_ASYNC0_2i_1				0				DP_CSC_A_ASYNC0_2i																			
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

IPUx\_DP\_CSCA\_ASYNC0\_i field descriptions

Field	Description																												
31–26 Reserved	This read-only field is reserved and always has the value 0.																												

Table continues on the next page...

**IPUx\_DP\_CSCA\_ASYNC0\_i field descriptions (continued)**

Field	Description
25–16 DP_CSC_A_ ASYNC0_2i_1	A<2*i+1> parameter of color conversion
15–10 Reserved	This read-only field is reserved and always has the value 0.
DP_CSC_A_ ASYNC0_2i	A<2*i> parameter of color conversion.

### 37.5.127 DP Color Conversion Control Async 0 Flow Register 0 (IPUx\_DP\_CSC\_ASYNC0\_0)

Address: Base address + 1\_80B4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DP_CSC_ S0_ASYNC0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0												
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DP\_CSC\_ASYNC0\_0 field descriptions**

Field	Description
31–30 DP_CSC_S0_ ASYNC0	S0 parameter of color conversion. 00 scale factor of 2 01 scale factor of 1 10 scale factor of 0 11 scale factor of -1
29–16 DP_CSC_B0_ ASYNC0	B0 parameter of color conversion.
15–10 Reserved	This read-only field is reserved and always has the value 0.
DP_CSC_A8_ ASYNC0	A9 parameter of color conversion.

### 37.5.128 DP Color Conversion Control Async 1 Flow Register (IPUx\_DP\_CSC\_ASYNC\_1)

Address: Base address + 1\_80B8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DP_CSC_S2_ASYNC0															DP_CSC_B2_ASYNC0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DP_CSC_S1_ASYNC0															DP_CSC_B1_ASYNC0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DP\_CSC\_ASYNC\_1 field descriptions

Field	Description
31–30 DP_CSC_S2_ASYNC0	S0 parameter of color conversion.  00 scale factor of 2 01 scale factor of 1 10 scale factor of 0 11 scale factor of -1
29–16 DP_CSC_B2_ASYNC0	B0 parameter of color conversion.
15–14 DP_CSC_S1_ASYNC0	S0 parameter of color conversion.  00 scale factor of 2 01 scale factor of 1 10 scale factor of 0 11 scale factor of -1
DP_CSC_B1_ASYNC0	B0 parameter of color conversion.

### 37.5.129 DP Common Configuration Async 1 Flow Register (IPUx\_DP\_COM\_CONF\_ASYNC1)

This register contains common configuration parameters for the DP.

Address: Base address + 1\_80BCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		DP_GAMMA_YUV_EN_ASYNC1	DP_GAMMA_EN_ASYNC1	DP_CSC_YUV_SAT_MODE_ASYNC1	DP_CSC_YUV_SAT_MODE_ASYNC1	DP_CSC_GAMUT_SAT_EN_ASYNC1	DP_CSC_DEF_ASYNC1	0				DP_GWCKE_ASYNC1	DP_GWAM_ASYNC1	DP_GWSEL_ASYNC1	0
W													DP_CO_C_ASYNC1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DP\_COM\_CONF\_ASYNC1 field descriptions

Field	Description
31–14 Reserved	This read-only field is reserved and always has the value 0.
13 DP_GAMMA_YUV_EN_ASYNC1	GAMMA's YUV mode enable for async flow 1 0 YUV mode is OFF. 1 YUV mode is ON.
12 DP_GAMMA_EN_ASYNC1	GAMMA_EN - Gamma correction block enable bit 0 disable 1 enable
11 DP_CSC_YUV_SAT_MODE_ASYNC1	CSC_YUV_SAT_MODE YUV saturation mode for color space conversion 0 Y/U/V range 0 -255 1 Y range 16-235, U/V range 16-240

Table continues on the next page...

**IPUx\_DP\_COM\_CONF\_ASYNC1 field descriptions (continued)**

Field	Description
10 DP_CSC_GAMUT_SAT_EN_ASYNC1	CSC_GAMUT_SAT_EN Indicate if GAMUT saturation is enabled 0 disable GAMUT mapping 1 enable GAMUT mapping
9–8 DP_CSC_DEF_ASYNC1	CSC_DEF Enable or disable Color Space Conversion. 00 CSC disable 01 CSC enable after combining 10 CSC enable before combining on BG channel 11 CSC enable before combining on FG channel
7 Reserved	This read-only field is reserved and always has the value 0.
6–4 DP_CO_COC_ASYNC1	CO_COC - Cursor Operation Control Controls the format of the cursor and the type of arithmetic operations 000 Transparent, cursor is disabled. 001 Full cursor. 010 Reversed cursor. 011 AND between full plane and cursor. 100 Reserved 101 OR between full plane and cursor. 110 XOR between full plane and cursor. 111 Reserved
3 DP_GWCKE_ASYNC1	GWCKE - Graphic Window Color Keying Enable Enable or disable graphic window color keying. 1 Enable color keying of graphic window 0 Disable color keying of graphic window
2 DP_GWAM_ASYNC1	GWAM - Graphic Window Alpha Mode Select the use of Alpha to be global or local. 1 Global Alpha. 0 Local Alpha.
1 DP_GWSEL_ASYNC1	GWSEL - Graphic Window Select Select graphic window to be on partial plane or full plane. 1 Graphic window is partial plane. 0 Graphic window is full plane.
0 Reserved	This read-only field is reserved and always has the value 0.

### 37.5.130 DP Debug Control Register (IPUx\_DP\_DEBUG\_CNT)

This is the debug unit control register. This register is not stored in the SRM.

Address: Base address + 1\_80BCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								BRAKE_CNT_1				BRAKE_CNT_0			BRAKE_STATUS_EN_0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DP\_DEBUG\_CNT field descriptions

Field	Description
31–8 Reserved	This read-only field is reserved and always has the value 0.
7–5 BRAKE_CNT_1	The async flow can be broken multiple times. It possible to control which breaking event will cause the interrupt. This field counts the breaking events for unit #1
4 BRAKE_STATUS_EN_1	This bit enables the break/status unit #1
3–1 BRAKE_CNT_0	The async flow can be broken multiple times. It possible to control which breaking event will cause the interrupt. This field counts the breaking events for unit #0
0 BRAKE_STATUS_EN_0	This bit enables the break/status unit #0

### 37.5.131 DP Graphic Window Control Async 1 Flow Register (IPUx\_DP\_GRAPH\_WIND\_CTRL\_ASYNC1)

This register contains common configuration parameters for the DP.

Address: Base address + 1\_80C0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R	DP_GWAV_ASYNC1																DP_GWCKG_ASYNC1																	
W	DP_GWCKR_ASYNC1																DP_GWCKB_ASYNC1																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DP\_GRAPH\_WIND\_CTRL\_ASYNC1 field descriptions

Field	Description
31–24 DP_GWAV_ASYNC1	GWAV - Graphic Window Alpha Value Defines the alpha value of graphic window used for alpha blending between graphic window and full plane. The Value the number that writing to GWAV register. The Actual Value the number, that insert to calculation in Combining Module. If Value = < 0.5- 1/256 (01111111) then Actual Value = Value. If Value >= 0.5 (10000000), then Actual Value = Value + 1/256.  00000000 Actual value is 00000000; Graphic window totally opaque i.e. overlay on LCD screen 01111111 Actual value is 01111111; 10000000 Actual value is 10000001 10000001 Actual value is 10000010 11111110 Actual value is 11111111 11111111 Actual value is 100000000;Graphic window totally transparent i.e. not displayed on LCD screen
23–16 DP_GWCKR_ASYNC1	GWCKR - Graphic Window Color Keying Red Component Defines the red component of graphic window color keying.  00000000 No red 11111111 Full red
15–8 DP_GWCKG_ASYNC1	GWCKG - Graphic Window Color Keying Green Component Defines the green component of graphic window color keying.  00000000 No Green 11111111 Full Green
DP_GWCKB_ASYNC1	GWCKB - Graphic Window Color Keying Blue Component Defines the blue component of graphic window color keying.  00000000 No blue 11111111 Full blue

### 37.5.132 DP Debug Status Register (IPUx\_DP\_DEBUG\_STAT)

Address: Base address + 1\_80C0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0		CYP_EN_OLD_1		COMBYP_EN_OLD_1								V_CNT_OLD_1			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0		CYP_EN_OLD_0		COMBYP_EN_OLD_0		FG_ACTIVE_0			V_CNT_OLD_0							
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DP\_DEBUG\_STAT field descriptions**

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.
29 CYP_EN_OLD_1	The async flow has been broken in the middle of a cursor (This filed is relevant for debug unit #1)
28 COMBYP_EN_OLD_1	the async1 flow has been broken in the middle of combining (This filed is relevant for debug unit #1)
27 FG_ACTIVE_1	Displaying the partial frame has been started (This filed is relevant for debug unit #1)
26–16 V_CNT_OLD_1	The exact row where the async flow has been broken (This filed is relevant for debug unit #0)
15–14 Reserved	This read-only field is reserved and always has the value 0.
13 CYP_EN_OLD_0	The async flow has been broken in the middle of a cursor (This filed is relevant for debug unit #0)
12 COMBYP_EN_OLD_0	the async flow has been broken in the middle of combining (This filed is relevant for debug unit #0)
11 FG_ACTIVE_0	Displaying the partial frame has been started for async flow (This filed is relevant for debug unit #0)
V_CNT_OLD_0	The exact row where the async flow has been broken (This filed is relevant for debug unit #0)

### 37.5.133 DP Partial Plane Window Position Async 1 Flow Register (IPUx\_DP\_FG\_POS\_ASYNC1)

The DP partial plane Window Position Register is used to determine the starting position of the partial plane window relative to BG window position.

This Register is used for the synchronous flow only.

Address: Base address + 1\_80C4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_DP\_FG\_POS\_ASYNC1 field descriptions

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 DP_FGXP_ASYNC1	FGXP partial plane Window X Position. partial plane Window X Position - Specifies the number of pixels between the start of full plane window X position and the beginning of the first data of new line.
15–11 Reserved	This read-only field is reserved and always has the value 0.
DP_FGYP_ASYNC1	FGYP partial plane window Y position partial plane Window Y Position - Specifies the number of lines between the start of full plane windows Y position and the beginning of the first data.

### 37.5.134 DP Cursor Postion and Size Async 1 Flow Register (IPUx\_DP\_CUR\_POS\_ASYNC1)

The LCD Cursor Position Register is used to determine the starting position of the cursor relative to BG windows position.

Address: Base address + 1\_80C8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	DP_CYP_ASYNC1																DP_CXP_ASYNC1																
W																																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DP\_CUR\_POS\_ASYNC1 field descriptions**

Field	Description
31–27 DP_CYP_ASYNC1	CYP - Cursor Y Position Represents the cursors vertical starting position Y in pixel count (from 0 to CYH).Live View Resolution Mode.
26–16 DP_CYH_ASYNC1	CYH - Cursor Height Specifies the height of the hardware cursor in pixels.
15–11 DP_CXP_ASYNC1	CXP - Cursor X Position Represents the cursors horizontal starting position X in pixel count (from 0 to CXW).
DP_CXW_ASYNC1	CXW - Cursor Width. Specifies the width of the hardware cursor in pixels.

**37.5.135 DP Color Cursor Mapping Async 1 Flow Register (IPUx\_DP\_CUR\_MAP\_ASYNC1)**

The LCD Color Cursor Mapping Register defines the color of the cursor in passive or TFT color modes.

Address: Base address + 1\_80CCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0																
W																		DP_CUR_COL_B_ASYNC1		DP_CUR_COL_G_ASYNC1		DP_CUR_COL_R_ASYNC1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DP\_CUR\_MAP\_ASYNC1 field descriptions**

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23–16 DP_CUR_COL_B_ASYNC1	CUR_COL_B - Cursor Blue Field Defines the Blue component of the cursor color in color mode 00000000 No Blue. 11111111 Full Blue.
15–8 DP_CUR_COL_G_ASYNC1	CUR_COL_G - Cursor Green Field Defines the Green component of the cursor color in color mode 00000000 No Green. 11111111 Full Green.
DP_CUR_COL_R_ASYNC1	CUR_COL_R - Cursor Red Field Defines the Red component of the cursor color in color mode

*Table continues on the next page...*

**IPUx\_DP\_CUR\_MAP\_ASYNC1 field descriptions (continued)**

Field	Description															
	00000000 No Red. 11111111 Full Red.															

### 37.5.136 DP Gamma Constants Async 1 Flow Register i (IPUx\_DP\_GAMMA\_C\_ASYNC1\_i)

This register contains CONSTANTi parameters used for gamma correction inside the display processor (DP).

Address: Base address + 1\_80D0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DP\_GAMMA\_C\_ASYNC1\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 DP_GAMMA_C_ ASYNC1_2i_1	CONSTANTi+1 parameter of Gamma Correction.
15–9 Reserved	This read-only field is reserved and always has the value 0.
DP_GAMMA_C_ ASYNC1_2i	CONSTANTi parameter of Gamma Correction.

### 37.5.137 DP Gamma Correction Slope Async 1 Flow Register i (IPUx\_DP\_GAMMA\_S\_ASYNC1\_i)

This register contains SLOPE $i$  parameters used for Gamma Correction inside the display processor (DP).

Address: Base address + 1\_80F0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DP_GAMMA_S_ASYNC1_4i_3				DP_GAMMA_S_ASYNC1_4i_2				DP_GAMMA_S_ASYNC1_4i_1				DP_GAMMA_S_ASYNC1_4i																			
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

IPUx\_DP\_GAMMA\_S\_ASYNC1\_i field descriptions

Field	Description																												
31–24 DP_GAMMA_S_ASYNC1_4i_3	SLOPE<4*i+3> parameter of Gamma Correction.																												
23–16 DP_GAMMA_S_ASYNC1_4i_2	SLOPE<4*i+2> parameter of Gamma Correction.																												
15–8 DP_GAMMA_S_ASYNC1_4i_1	SLOPE<4*i+1> parameter of Gamma Correction.																												
DP_GAMMA_S_ASYNC1_4i	SLOPE<4*i> parameter of Gamma Correction.																												

### 37.5.138 DP Color Space Converstion Control Async 1 Flow Register i (IPUx\_DP\_CSCA\_ASYNC1\_i)

Address: Base address + 1\_8100h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0				DP_CSC_A_ASYNC1_2i_1				0				DP_CSC_A_ASYNC1_2i																			
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

IPUx\_DP\_CSCA\_ASYNC1\_i field descriptions

Field	Description																												
31–26 Reserved	This read-only field is reserved and always has the value 0.																												

Table continues on the next page...

**IPUx\_DP\_CSCA\_ASYNC1\_i field descriptions (continued)**

Field	Description
25–16 DP_CSC_A_ ASYNC1_2i_1	A $<2*i+1>$ parameter of color conversion.
15–10 Reserved	This read-only field is reserved and always has the value 0.
DP_CSC_A_ ASYNC1_2i	A $<2*i>$ parameter of color conversion.

### 37.5.139 DP Color Conversion Control Async 1 Flow Register 0 (IPUx\_DP\_CSC\_ASYNC1\_0)

Address: Base address + 1\_8110h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DP_CSC_ S0_ASYNC1		DP_CSC_B0_ASYNC1													
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0						DP_CSC_A8_ASYNC1									
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DP\_CSC\_ASYNC1\_0 field descriptions**

Field	Description
31–30 DP_CSC_S0_ ASYNC1	S0 parameter of color conversion.  00 scale factor of 2 01 scale factor of 1 10 scale factor of 0 11 scale factor of -1
29–16 DP_CSC_B0_ ASYNC1	B0 parameter of color conversion.
15–10 Reserved	This read-only field is reserved and always has the value 0.
DP_CSC_A8_ ASYNC1	A9 parameter of color conversion.

### 37.5.140 DP Color Conversion Control Async 1 Flow Register 1 (IPUx\_DP\_CSC\_ASYNC1\_1)

Address: Base address + 1\_8114h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DP_CSC_S2_ASYNC1	DP_CSC_B2_ASYNC1														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DP_CSC_S1_ASYNC1	DP_CSC_B1_ASYNC1														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DP\_CSC\_ASYNC1\_1 field descriptions

Field	Description
31–30 DP_CSC_S2_ASYNC1	S0 parameter of color conversion. 00 scale factor of 2 01 scale factor of 1 10 scale factor of 0 11 scale factor of -1
29–16 DP_CSC_B2_ASYNC1	B0 parameter of color conversion.
15–14 DP_CSC_S1_ASYNC1	S0 parameter of color conversion. 00 scale factor of 2 01 scale factor of 1 10 scale factor of 0 11 scale factor of -1
DP_CSC_B1_ASYNC1	B0 parameter of color conversion.

### 37.5.141 IC Configuration Register (IPUx\_IC\_CONF)

This register contains control parameter for IC 3 tasks (pre-processing for encoding, pre-processing for view-finder and post processing).

Address: Base address + 2\_0000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	CSI_MEM_WR_EN	RWS_EN	IC_KEY_COLOR_EN	IC_GLB_LOC_A					0			PP_ROT_EN	PP_CMB	PP_CSC2	PP_CSC1	PP_EN
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R			0	PRPVF_ROT_EN	PRPVF_CMB	PRPVF_CSC2	PRPVF_CSC1	PRPVF_EN			0		PRPENC_ROT_EN	PRPENC_CSC1	PRPENC_EN	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_IC\_CONF field descriptions

Field	Description
31 CSI_MEM_WR_EN	CSI direct memory write enable. This bit enables writing data from sensor directly to memory even when a raw sensor is not attached.  0 CSI direct writing to memory is disabled. 1 CSI direct writing to memory is enabled.
30 RWS_EN	Raw sensor enable. This bit indicate if a Raw sensor is attached (Bayer format).  This bit is used together with the CSI_MEM_WR_EN bit as follows:  CSI_MEM_WR_EN=0, RWS_EN=0 - data is fed from the CSI to the IC for processing; CSI_MEM_WR_EN=1, RWS_EN=0 - data is fed from the CSI to the IC for processing and also for writing to the system memory;  CSI_MEM_WR_EN=0, RWS_EN=1 - data is fed from the CSI to the system memory (via the IC) and from the system memory to the IC for processing;  CSI_MEM_WR_EN=1, RWS_EN=1 - non-valid configuration.  0 Raw sensor is not attached. 1 Raw sensor is attached.
29 IC_KEY_COLOR_EN	Key Color enable. This bit enables the key color feature.

Table continues on the next page...

**IPUx\_IC\_CONF field descriptions (continued)**

Field	Description
	0 Key color is disabled. 1 Key color is enabled.
28 IC_GLB_LOC_A	Global Alpha. This bit select the source of Alpha parameter. 0 Alpha parameter is local. 1 Alpha parameter is global.
27–21 Reserved	This read-only field is reserved and always has the value 0.
20 PP_ROT_EN	Post-Processing Rotation Task enable. This bit enable Post-Processing Rotation Task. 0 Rotation is disabled. 1 Rotation is enabled.
19 PP_CMB	Post-Processing Task combining enable. This bit enables combining. 0 Combining is disabled. 1 Combining is enabled.
18 PP_CSC2	Post-Processing Task color conversion RGB-->YUV enable. This bit enables YUV-->RGB. Reserved 0 RGB-->YUV is disabled. 1 RGB-->YUV is enabled.
17 PP_CSC1	Post-Processing Task color conversion YUV-->RGB enable. This bit enables YUV-->RGB. 0 YUV-->RGB is disabled. 1 YUV-->RGB is enabled.
16 PP_EN	Post-Processing Task enable. This bit enables the Post-Processing task. 0 Task is disabled. 1 Task is enabled.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12 PRPVF_ROT_EN	Preprocessing Rotation Task for viewfinder enable. This bit enable Preprocessing Rotation Task for viewfinder. 0 Rotation is disabled. 1 Rotation is enabled.
11 PRPVF_CMB	Preprocessing Task for View-Finder combining enable. This bit enables combining. 0 Combining is disabled. 1 Combining is enabled.
10 PRPVF_CSC2	Reserved
9 PRPVF_CSC1	Pre-processing task for view-finder first color conversion enable. This bit enables first color conversion. 0 First color conversion is disabled. 1 First color conversion is enabled.
8 PRPVF_EN	Preprocessing Task for View-Finder enable. This bit enables the View-Finder task.

*Table continues on the next page...*

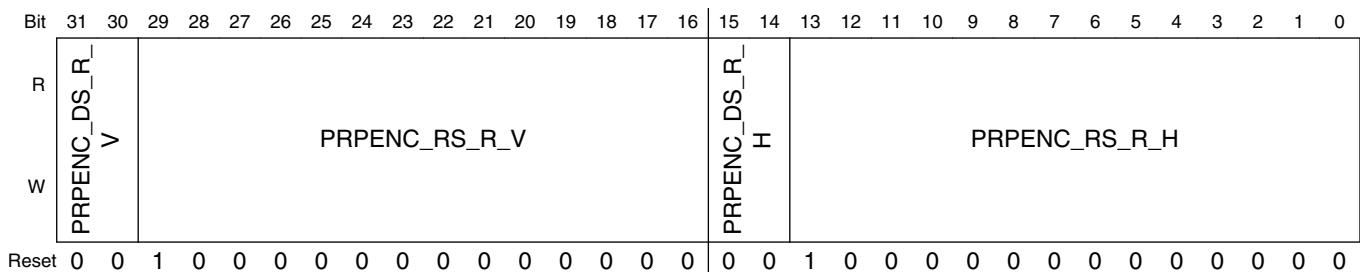
**IPUx\_IC\_CONF field descriptions (continued)**

Field	Description
	0 Task is disabled. 1 Task is enabled.
7–3 Reserved	This read-only field is reserved and always has the value 0.
2 PRPENC_ROT_EN	Preprocessing Rotation Task for encoding enable. This bit enable Preprocessing Rotation Task for encoding.  0 Rotation is disabled. 1 Rotation is enabled.
1 PRPENC_CSC1	Preprocessing Task for encoding color conversion enable. This bit enables color conversion.  0 Color conversion is disabled. 1 Color conversion is enabled.
0 PRPENC_EN	Preprocessing Task for encoding enable. This bit enables the encoding task.  0 Task is disabled. 1 Task is enabled.

### 37.5.142 IC Preprocessing Encoder Resizing Coefficients Register (IPUx\_IC\_PRP\_ENC\_RSC)

This register contains the resizing and downsizing parameters for Preprocessing task for encoding.

Address: Base address + 2\_0004h offset

**IPUx\_IC\_PRP\_ENC\_RSC field descriptions**

Field	Description
31–30 PRPENC_DS_R_V	Preprocessing task for encoding Downsizing vertical Ratio. This field contains the downsizing vertical coefficient of Preprocessing for Encoding.
29–16 PRPENC_RS_R_V	Preprocessing task for encoding Resizing vertical Ratio. This field contains the resizing vertical coefficient of Preprocessing for Encoding.  Resizing Ratio is equal to PRPENC_RS_R_V: M

*Table continues on the next page...*

**IPUx\_IC\_PRP\_ENC\_RSC field descriptions (continued)**

Field	Description
	Where $M = 2^{13}$ ; SI - input size; SO - output size $\text{PRPENC_RS_R_V} = \text{floor}(M * (\text{SI}-1) / (\text{SO}-1))$ ;
15–14 PRPENC_DS_R_H	Preprocessing task for encoding Downsizing horizontal Ratio. This field contains the downsizing horizontal coefficient of Preprocessing for Encoding. Values: 00 1 01 2 10 4 11 RSV
PRPENC_RS_R_H	Preprocessing task for encoding Resizing horizontal Ratio. This field contains the resizing horizontal coefficient of Preprocessing for Encoding. Resizing Ratio is equal to PRPENC_RS_R_H: M Where $M = 2^{13}$ ; SI - input size; SO - output size $\text{PRPENC_RS_R_H} = \text{floor}(M * (\text{SI}-1) / (\text{SO}-1))$ ;

**37.5.143 IC Preprocessing View-Finder Resizing Coefficients Register (IPUx\_IC\_PRP\_VF\_RSC)**

This register contains the resizing and downsizing parameters for preprocessing task for display.

Address: Base address + 2\_0008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	PRPVF_DS_R_V															
W	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PRPVF_DS_R_H															
W	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset																

**IPUx\_IC\_PRP\_VF\_RSC field descriptions**

Field	Description
31–30 PRPVF_DS_R_V	Preprocessing task for encoding Downsizing vertical Ratio. This field contains the downsizing vertical coefficient of Preprocessing for View-Finder.
29–16 PRPVF_RS_R_V	Preprocessing task for encoding Resizing vertical Ratio. This field contains the resizing vertical coefficient of Preprocessing for View-Finder. Resizing Ratio is equal to PRPVF_RS_R_V: M

*Table continues on the next page...*

**IPUx\_IC\_PRP\_VF\_RSC field descriptions (continued)**

Field	Description
	Where M = 2^13; SI - input size; SO - output size PRPVF_RS_R_V = floor(M*(SI-1)/(SO-1));
15–14 PRPVF_DS_R_H	Preprocessing task for encoding Downsizing horizontal Ratio. This field contains the downsizing horizontal coefficient of Preprocessing for View-Finder.  Values:  00 1 01 2 10 4 11 RSV
PRPVF_RS_R_H	Preprocessing task for view-finding resizing horizontal ratio. This field contains the resizing horizontal coefficient of preprocessing Task For View-finder.  Resizing Ratio is equal to PRPVF_RS_R_H: M  Where M = 2^13; SI - input size; SO - output size PRPVF_RS_R_H = floor(M*(SI-1)/(SO-1));

**37.5.144 IC Postprocessing Encoder Resizing Coefficients Register (IPUx\_IC\_PP\_RSC)**

This register contains the resizing and downsizing parameters for Post-Processing task for display.

Address: Base address + 2\_000Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PP_DS_R_V																PP_DS_R_H															
W																																

**IPUx\_IC\_PP\_RSC field descriptions**

Field	Description
31–30 PP_DS_R_V	Post-Processing task Downsizing vertical Ratio. This field contains the downsizing vertical coefficient of Post-Processing.
29–16 PP_RS_R_V	Post-Processing task Resizing vertical Ratio. This field contains the resizing vertical coefficient of Post-Processing.  Resizing Ratio is equal to PP_RS_R_V: M  Where M = 2^13; SI - input size; SO - output size PP_RS_R_V = floor(M*(SI-1)/(SO-1));

*Table continues on the next page...*

**IPUx\_IC\_PP\_RSC field descriptions (continued)**

Field	Description
15–14 PP_DS_R_H	Post-Processing task Downsizing horizontal Ratio. This field contains the downsizing horizontal coefficient of Post-Processing.  00 1 01 2 10 4 11 RSV
PP_RS_R_H	Post-Processing task Resizing horizontal Ratio. This field contains the resizing horizontal coefficient of Post-Processing.  Resizing Ratio is equal to PP_RS_R_H: M Where M = $2^{13}$ ; SI - input size; SO - output size $PP_RS_R_H = \text{floor}(M * (\text{SI}-1) / (\text{SO}-1))$ ;

**37.5.145 IC Combining Parameters Register 1 (IPUx\_IC\_CMBP\_1)**

Address: Base address + 2\_0010h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_IC\_CMBP\_1 field descriptions**

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 IC_PP_ALPHA_V	Post-Processing task Global Alpha. This field contains the Global Alpha value of Post-Processing.
IC_PRPVF_ALPHA_V	Preprocessing task for viewfinder Global Alpha. This field contains the Global Alpha value of Preprocessing for viewfinder.

**37.5.146 IC Combining Parameters Register 2 (IPUx\_IC\_CMBP\_2)**

Address: Base address + 2\_0014h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_IC\_CMBP\_2 field descriptions**

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23–16 IC_KEY_ COLOR_R	Key Color Red.
15–8 IC_KEY_ COLOR_G	Key Color Green.
IC_KEY_ COLOR_B	Key Color Blue.

**37.5.147 IC IDMAC Parameters 1 Register (IPUx\_IC\_IDMAC\_1)**

Address: Base address + 2\_0018h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R							0		0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	T2_FLIP_LR	T2_ROT	T1_FLIP_UD	T1_FLIP_LR	T1_ROT	0	0	0	CB7_BURST_16	CB6_BURST_16	CB5_BURST_16	CB4_BURST_16	CB3_BURST_16	CB2_BURST_16	CB1_BURST_16	CBO_BURST_16
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_IC\_IDMAC\_1 field descriptions**

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.
25 ALT_CB7_ BURST_16	Reserved
24 ALT_CB6_ BURST_16	Reserved
23 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_IC\_IDMAC\_1 field descriptions (continued)**

Field	Description
22 T3_FLIP_RS	LEFT/RIGHT flip for Post Processing (PP) task; this bit affect the flipping done on the resizing unit. The value of this field must be identical to the corresponding channel's HF parameter in the IDMAC's CPMEM  1 horizontal flip enabled 0 no flip
21 T2_FLIP_RS	LEFT/RIGHT flip for View Finder (VF) task; this bit affect the flipping done on the resizing unit. The value of this field must be identical to the corresponding channel's HF parameter in the IDMAC's CPMEM  1 horizontal flip enabled 0 no flip
20 T1_FLIP_RS	LEFT/RIGHT flip for Encoding (ENC) task; this bit affect the flipping done on the resizing unit. The value of this field must be identical to the corresponding channel's HF parameter in the IDMAC's CPMEM  1 horizontal flip enabled 0 no flip
19 T3_FLIP_UD	UP/DOWN flip for Post Processing (PP) task The value of this field must be identical to the corresponding channel's VF parameters in the IDMAC's CPMEM  1 Vertical flip enable 0 no flip
18 T3_FLIP_LR	LEFT/RIGHT flip for Post Processing (PP) task; this bit affect the flipping done on the rotation unit The value of this field must be identical to the corresponding channel's HF parameter in the IDMAC's CPMEM  1 horizontal flip enabled 0 no flip
17 T3_ROT	Rotation for Post Processing (PP) task The value of this field must be identical to the corresponding channel's ROT parameters in the IDMAC's CPMEM  1 90 degree rotation clockwise 0 no rotation
16 T2_FLIP_UD	UP/DOWN flip for View Finder (VF) task The value of this field must be identical to the corresponding channel's VF parameters in the IDMAC's CPMEM  1 Vertical flip enable 0 no flip
15 T2_FLIP_LR	LEFT/RIGHT flip for View Finder (VF) task; this bit affect the flipping done on the rotation unit The value of this field must be identical to the corresponding channel's HF parameter in the IDMAC's CPMEM  1 horizontal flip enabled 0 no flip

*Table continues on the next page...*

**IPUx\_IC\_IDMAC\_1 field descriptions (continued)**

Field	Description
14 T2_ROT	<p>Rotation for View Finder (VF) task</p> <p>The value of this field must be identical to the corresponding channel's ROT parameters in the IDMAC's CPMEM</p> <p>1 90 degree rotation clockwise 0 no rotation</p>
13 T1_FLIP_UD	<p>UP/DOWN flip for Encoding (ENC) task</p> <p>The value of this field must be identical to the corresponding channel's VF parameters in the IDMAC's CPMEM</p> <p>1 Vertical flip enable 0 no flip</p>
12 T1_FLIP_LR	<p>LEFT/RIGHT flip for Encoding (ENC) task; this bit affect the flipping done on the rotation unit</p> <p>The value of this field must be identical to the corresponding channel's HF parameter in the IDMAC's CPMEM</p> <p>1 horizontal flip enabled 0 no flip</p>
11 T1_ROT	<p>Rotation for Encoding (ENC) task</p> <p>The value of this field must be identical to the corresponding channel's ROT parameters in the IDMAC's CPMEM</p> <p>1 90 degree rotation clockwise 0 no rotation</p>
10–8 Reserved	This read-only field is reserved and always has the value 0.
7 CB7_BURST_16	<p>This bit defines the number of active cycles within a burst (burst size) coming from the IDMAC for IC's CB7</p> <p>For pixel data the number of pixels should match the NPB[6:2] value on the IDMAC's CPMEM</p> <p>0 Burst size is 8 pixels; The Matching NPB[6:2] should be 00111 1 Burst size is 16 pixels; The Matching NPB[6:2] should be 01111</p>
6 CB6_BURST_16	<p>This bit defines the number of active cycles within a burst (burst size) coming from the IDMAC for IC's CB6</p> <p>For pixel data the number of pixels should match the NPB[6:2] value on the IDMAC's CPMEM</p> <p>0 Burst size is 8 pixels; The Matching NPB[6:2] should be 00111 1 Burst size is 16 pixels; The Matching NPB[6:2] should be 01111</p>
5 CB5_BURST_16	<p>This bit defines the number of active cycles within a burst (burst size) coming from the IDMAC for IC's CB5</p> <p>For pixel data the number of pixels should match the NPB[6:2] value on the IDMAC's CPMEM</p> <p>0 Burst size is 8 pixels; The Matching NPB[6:2] should be 00111 1 Burst size is 16 pixels; The Matching NPB[6:2] should be 01111</p>
4 CB4_BURST_16	<p>This bit defines the number of active cycles within a burst (burst size) coming from the IDMAC for IC's CB4</p> <p>For pixel data the number of pixels should match the NPB[6:2] value on the IDMAC's CPMEM</p>

*Table continues on the next page...*

**IPUx\_IC\_IDMAC\_1 field descriptions (continued)**

Field	Description
	0 Burst size is 8 pixels; The Matching NPB[6:2] should be 00111 1 Burst size is 16 pixels; The Matching NPB[6:2] should be 01111
3 CB3_BURST_16	This bit defines the number of active cycles within a burst (burst size) coming from the IDMAC for IC's CB3  For pixel data the number of pixels should match the NPB[6:2] value on the IDMAC's CPMEM  0 Burst size is 8 pixels; The Matching NPB[6:2] should be 00111 1 Burst size is 16 pixels; The Matching NPB[6:2] should be 01111
2 CB2_BURST_16	This bit defines the number of active cycles within a burst (burst size) coming from the IDMAC for IC's CB2  For pixel data the number of pixels should match the NPB[6:2] value on the IDMAC's CPMEM  0 Burst size is 8 pixels; The Matching NPB[6:2] should be 00111 1 Burst size is 16 pixels; The Matching NPB[6:2] should be 01111
1 CB1_BURST_16	This bit defines the number of active cycles within a burst (burst size) coming from the IDMAC for IC's CB1  For pixel data the number of pixels should match the NPB[6:2] value on the IDMAC's CPMEM  0 Burst size is 8 pixels; The Matching NPB[6:2] should be 00111 1 Burst size is 16 pixels; The Matching NPB[6:2] should be 01111
0 CB0_BURST_16	This bit defines the number of active cycles within a burst (burst size) coming from the IDMAC for IC's CB0  For pixel data the number of pixels should match the NPB[6:2] value on the IDMAC's CPMEM  0 Burst size is 8 pixels; The Matching NPB[6:2] should be 00111 1 Burst size is 16 pixels; The Matching NPB[6:2] should be 01111

**37.5.148 IC IDMAC Parameters 2 Register (IPUx\_IC\_IDMAC\_2)**

Address: Base address + 2\_001Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	0																																
W																																	

Reset 0

**IPUx\_IC\_IDMAC\_2 field descriptions**

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.
29–20 T3_FR_HEIGHT	Frame Height for Post Processing (PP) task  The value of this field must be identical to the corresponding FH channel's parameters in the IDMAC's CPMEM. This parameter refers to the output's size -1
19–10 T2_FR_HEIGHT	Frame Height for View Finder (VF) task

Table continues on the next page...

**IPUx\_IC\_IDMAC\_2 field descriptions (continued)**

Field	Description
	The value of this field must be identical to the corresponding FH channel's parameters in the IDMAC's CPMEM. This parameter refers to the output's size -1
T1_FR_HEIGHT	Frame Height for Encoding (ENC) task The value of this field must be identical to corresponding FH channel's parameters in the IDMAC's CPMEM. This parameter refers to the output's size -1

**37.5.149 IC IDMAC Parameters 3 Register (IPUx\_IC\_IDMAC\_3)**

Address: Base address + 2\_0020h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	0																																
W																																	

Reset 0

**IPUx\_IC\_IDMAC\_3 field descriptions**

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.
29–20 T3_FR_WIDTH	Frame Width for Post Processing (PP) task The value of this field must be identical to the corresponding FW channel's parameters in the IDMAC's CPMEM. This parameter refers to the output's size -1
19–10 T2_FR_WIDTH	Frame Width for View Finder (VF) task The value of this field must be identical to the corresponding FW channel's parameters in the IDMAC's CPMEM. This parameter refers to the output's size -1
T1_FR_WIDTH	Frame Width for Encoding (ENC) task The value of this field must be identical to corresponding FW channel's parameters in the IDMAC's CPMEM. This parameter refers to the output's size -1

**37.5.150 IC IDMAC Parameters 4 Register (IPUx\_IC\_IDMAC\_4)**

Address: Base address + 2\_0024h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																0																		
W																																		

Reset 0

**IPUx\_IC\_IDMAC\_4 field descriptions**

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.
15–12 rm_brdg_max_rq	RM memory Bridge Max Requests 0000 Feature is disabled 0001 Max request is 1 1111 Max request are15
11–8 ibm_brdg_max_rq	IBM memory Bridge Max Requests 0000 Feature is disabled 0001 Max request is 1 1111 Max request are15
7–4 mpm_dmfc_brdg_max_rq	MPM memory Bridge Max Requests for the IC DMFC interface 0000 Feature is disabled 0001 Max request is 1 1111 Max request are15
mpm_rw_brdg_max_rq	MPM memory Bridge Max Requests between MPM's read and writes 0000 Feature is disabled 0001 Max request is 1 1111 Max request are15

**37.5.151 CSI0 Sensor Configuration Register (IPUx\_CSI0\_SENS\_CONF)**

Address: Base address + 3\_0000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	CSI0_DATA_EN_POL	0	CSI0_FORCE_EOF	CSI0_JPEG_MODE	CSI0_JPEG8_EN	CSI0_DATA_DEST										
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CSI0_EXT_VSYNC		CSI0_DATA_WIDTH		CSI0_SENS_DATA_FORMAT		CSI0_PACK_TIGHT		CSI0_SENS_PIX_CLK_POL		CSI0_DATA_POL		CSI0_HSYNC_POL		CSI0_VSYNC_POL	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_CSI0\_SENS\_CONF field descriptions**

Field	Description
31 CSI0_DATA_EN_POL	Invert IPP_IND_SENSB_DATA_EN input. This bit selects the polarity of IPP_IND_SENSB_DATA_EN signal.  0 IPP_IND_SENSB_DATA_EN is directly applied to internal circuitry. 1 IPP_IND_SENSB_DATA_EN is inverted before applied to internal circuitry.
30 Reserved	This read-only field is reserved and always has the value 0.
29 CSI0_FORCE_EOF	Force End of frame  This is a self clear bit allowing the user to force an End-of-frame event; This bit can be used in cases where the frame sent by the sensor was not completed.  1 force end of frame 0 no action
28 CSI0_JPEG_MODE	JPEG Mode - this bit defines the mode of the control signals when working in JPEG mode  1 The data is valid as long as HSYNC and VSYNC signals are active; HSYNC is valid for single frame 0 The frame starts with the assertion of VSYNC. The frame ends on the next VSYNC or by setting the <b>CSI0_FORCE_EOF</b> bit.
27 CSI0_JPEG8_EN	JPEG8 enable bit  1 JPEG8 detection is enabled 0 JPEG8 is disabled
26–24 CSI0_DATA_DEST	These bits enable the destination of the data coming from the CSI.  CSI0_DATA_DEST[0] - Reserved  CSI0_DATA_DEST[1] - destination is IC  CSI0_DATA_DEST[2] - destination is IDMAC via SMFC
23–16 CSI0_DIV_RATIO	DIV Ratio Clock division ratio minus 1. This field defines the division ratio of HSP_CLK into SENS_B_MCLK: SENS_B_MCLK rate = HSP_CLK rate / (DIV_RATIO+1)
15 CSI0_EXT_VSYNC	External VSYNC enable. This bits select between external and internal VSYNC.  0 Internal VSYNC mode. 1 External VSYNC mode.
14–11 CSI0_DATA_WIDTH	Data width. This field defines the number of bits per color.  Values:  0000 4 bits per color 0001 8 bits per color 0010 9 bits per color 0011 10 bits per color 0100 11 bits per color 0101 12 bits per color 0110 13 bits per color 0111 14 bits per color 1000 15 bits per color 1001 16 bits per color

*Table continues on the next page...*

**IPUx\_CSI0\_SENS\_CONF field descriptions (continued)**

Field	Description
10–8 CSI0_SENS_ DATA_FORMAT	<p>Data format from the sensor. This field defines the data format for the input of the CSI sensor.</p> <p>Values:</p> <ul style="list-style-type: none"> <li>000 full RGB or YUV444</li> <li>001 YUV422 (YUYV...)</li> <li>010 YUV422 (UYVY...)</li> <li>011 Bayer or Generic data</li> <li>100 RGB565</li> <li>101 RGB555</li> <li>110 RGB444</li> <li>111 JPEG</li> </ul>
7 CSI0_PACK_ TIGHT	<p>CSI0 Pack Tight</p> <p>When the data format is YUV or RGB and the component's width is 9-16 bits, it can be sent to the memory in 2 different ways.</p> <ul style="list-style-type: none"> <li>1 Three 10 bits components are packed into a 32 bit word. Color extension/reduction is performed</li> <li>0 Each component is written as a 16 bit word where the MSB is written to bit #15, color extension is done for the remaining least significant bits.</li> </ul>
6–4 CSI0_SENS_ PRTCL	<p>Sensor Protocol. This bit defines the Sensor timing/data mode protocol.</p> <p>Values:</p> <ul style="list-style-type: none"> <li>000 Gated clock mode</li> <li>001 Non-gated clock mode</li> <li>010 CCIR progressive mode (BT.656)</li> <li>011 CCIR interlaced mode (BT.656)</li> <li>100 CCIR progressive (BT.1120 DDR mode: data arrives on every edge of the clock)</li> <li>101 CCIR progressive (BT.1120 SDR mode: data arrives only on the positive edge of the clock)</li> <li>110 CCIR interlaced mode (BT.1120 DDR mode: data arrives on every edge of the clock)</li> <li>111 CCIR interlaced mode (BT.1120 SDR mode: data arrives only on the positive edge of the clock)</li> </ul>
3 CSI0_SENS_ PIX_CLK_POL	<p>Invert Pixel clock input. This bit selects the polarity of pixel clock.</p> <ul style="list-style-type: none"> <li>0 pixel clock is directly applied to internal circuitry.</li> <li>1 pixel clock is inverted before applied to internal circuitry.</li> </ul>
2 CSI0_DATA_ POL	<p>Invert data input. This bit selects the polarity of data input.</p> <ul style="list-style-type: none"> <li>0 data lines are directly applied to internal circuitry.</li> <li>1 data lines are inverted before applied to internal circuitry.</li> </ul>
1 CSI0_HSYNC_ POL	<p>Invert IPP_IND_SENSB_HSYNC input. This bit selects the polarity of IPP_IND_SENSB_HSYNC signal.</p> <ul style="list-style-type: none"> <li>0 IPP_IND_SENSB_HSYNC is directly applied to internal circuitry.</li> <li>1 IPP_IND_SENSB_HSYNC is inverted before applied to internal circuitry.</li> </ul>
0 CSI0_VSYNC_ POL	<p>Invert IPP_IND_SENSB_VSYNC input. This bit selects the polarity of IPP_IND_SENSB_VSYNC signal.</p> <ul style="list-style-type: none"> <li>0 IPP_IND_SENSB_VSYNC is not inverted before applied to internal circuitry.</li> <li>1 IPP_IND_SENSB_VSYNC is inverted before applied to internal circuitry.</li> </ul>

### 37.5.152 CSI0 Sense Frame Size Register (IPUx\_CSI0\_SENS\_FRM\_SIZE)

Address: Base address + 3\_0004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W																																

Reset 0

#### IPUx\_CSI0\_SENS\_FRM\_SIZE field descriptions

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 CSI0_SENS_ FRM_HEIGHT	Sensor frame height minus 1. This field defines the sensor frame rows number minus 1.
15–13 Reserved	This read-only field is reserved and always has the value 0.
CSI0_SENS_ FRM_WIDTH	Sensor frame width minus 1. This field defines the sensor frame column number minus 1.

### 37.5.153 CSI0 Actual Frame Size Register (IPUx\_CSI0\_ACT\_FRM\_SIZE)

Address: Base address + 3\_0008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W																																

Reset 0

#### IPUx\_CSI0\_ACT\_FRM\_SIZE field descriptions

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 CSI0_ACT_ FRM_HEIGHT	Actual frame height minus 1. This field defines the CSI output frame rows number minus 1.
15–13 Reserved	This read-only field is reserved and always has the value 0.
CSI0_ACT_ FRM_WIDTH	Actual frame width minus 1. This field defines the CSI output frame columns number minus 1.

### 37.5.154 CSI0 Output Control Register (IPUx\_CSI0\_OUT\_FRM\_CTRL)

Address: Base address + 3\_000Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	CSI0_HORZ_DWNS	CSI0_VERT_DWNS	0														
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R			0														
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IPUx\_CSI0\_OUT\_FRM\_CTRL field descriptions

Field	Description
31 CSI0_HORZ_DWNS	Enable horizontal downsizing (decimation) by 2. 0 Downsizing disabled 1 Downsizing enabled
30 CSI0_VERT_DWNS	Enable vertical downsizing (decimation) by 2. 0 Downsizing disabled 1 Downsizing enabled
29 Reserved	This read-only field is reserved and always has the value 0.
28–16 CSI0_HSC	Horizontal skip. This field defines the number of columns to skip. In Interlaced mode this number refers to the number of lines per field.
15–12 Reserved	This read-only field is reserved and always has the value 0.
CSI0_VSC	Vertical skip. This field defines the number of rows to skip.

### 37.5.155 CSIO Test Control Register (IPUx\_CSI0\_TST\_CTRL)

Address: Base address + 3\_0010h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	PG_B_VALUE									PG_R_VALUE							
W	PG_G_VALUE																
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_CSI0\_TST\_CTRL field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24 TEST_GEN_MODE	Test generator mode. This bit activates the signal generation. 0 Test signal generator is inactive. 1 Test signal generator is active.
23–16 PG_B_VALUE	Pattern generator B value. This field selects the B value for the generated pattern of even pixel.
15–8 PG_G_VALUE	Pattern generator G value. This field selects the G value for the generated pattern of even pixel.
PG_R_VALUE	Pattern generator R value. This field selects the R value for the generated pattern of even pixel.

### 37.5.156 CSIO CCIR Code Register 1 (IPUx\_CSIO\_CCIR\_CODE\_1)

Address: Base address + 3\_0014h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R								CSIO_CCIR_ERR_DET_EN	0							
W											CSI0_STRT_FLD0_ACTV			CSI0_END_FLD0_ACTV		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0					CSI0_STRT_FLD0_BLNK_2ND		CSI0_END_FLD0_BLNK_2ND		CSI0_STRT_FLD0_BLNK_1ST		CSI0_END_FLD0_BLNK_1ST	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_CSIO\_CCIR\_CODE\_1 field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24 CSIO_CCIR_ERR_DET_EN	Enable error detection and correction for CCIR interlaced mode with protection bit. 0 Error detection and correction is disabled. 1 Error detection and correction is enabled.
23–22 Reserved	This read-only field is reserved and always has the value 0.
21–19 CSIO_STRT_FLD0_ACTV	Start of field 0 active line command (interlaces mode). (In progressive mode, start of active line command mode).
18–16 CSIO_END_FLD0_ACTV	End of field 0 active line command (interlaces mode). (In progressive mode, end of active line command mode).
15–12 Reserved	This read-only field is reserved and always has the value 0.
11–9 CSIO_STRT_FLD0_BLNK_2ND	Start of field 0 second blanking line command (interlaces mode). (In progressive mode this field is ignored).
8–6 CSIO_END_FLD0_BLNK_2ND	End of field 0 second blanking line command (interlaces mode). (In progressive mode this field is ignored).

Table continues on the next page...

**IPUx\_CSI0\_CCIR\_CODE\_1 field descriptions (continued)**

Field	Description
5–3 CSI0_STRT_ FLD0_BLNK_ 1ST	Start of field 0 first blanking line command (interlaces mode). (In progressive mode this field indicates start of blanking line command).
CSI0_END_ FLD0_BLNK_ 1ST	End of field 0 first blanking line command (interlaces mode). (In progressive mode this field is ignored).

**37.5.157 CSIO CCIR Code Register 2 (IPUx\_CSI0\_CCIR\_CODE\_2)**

Address: Base address + 3\_0018h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0																
W																																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_CSI0\_CCIR\_CODE\_2 field descriptions**

Field	Description
31–22 Reserved	This read-only field is reserved and always has the value 0.
21–19 CSI0_STRT_ FLD1_ACTV	Start of field 1 active line command (interlaces mode). (In progressive mode this field is ignored).
18–16 CSI0_END_ FLD1_ACTV	End of field 1 active line command (interlaces mode). (In progressive mode this field is ignored).
15–12 Reserved	This read-only field is reserved and always has the value 0.
11–9 CSI0_STRT_ FLD1_BLNK_ 2ND	Start of field 1 second blanking line command (interlaces mode). (In progressive mode this field is ignored).
8–6 CSI0_END_ FLD1_BLNK_ 2ND	End of field 1 second blanking line command (interlaces mode). (In progressive mode this field is ignored).
5–3 CSI0_STRT_ FLD1_BLNK_ 1ST	Start of field 1 first blanking line command (interlaces mode). (In progressive mode this field is ignored).
CSI0_END_ FLD1_BLNK_ 1ST	End of field 1 first blanking line command (interlaces mode). (In progressive mode this field is ignored).

### 37.5.158 CSIO CCIR Code Register 3 (IPUx\_CSIO\_CCIR\_CODE\_3)

Address: Base address + 3\_001Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																	CSI0_CCIR_PRECOM															
W																																	

Reset 0

#### IPUx\_CSIO\_CCIR\_CODE\_3 field descriptions

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.
CSI0_CCIR_PRECOM	CCIR pre command. This field defines the sequence which comes before the CCIR command. For BT.656 the code should be written to bits [23:0] while bits [29:24] are ignored (3X8bit) For BT.1120 the code should be written to bits [29:0] (3X10bit)

### 37.5.159 CSIO Data Identifier Register (IPUx\_CSIO\_DI)

Address: Base address + 3\_0020h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	CSI0_MIPI_DI3		CSI0_MIPI_DI2		CSI0_MIPI_DI1		CSI0_MIPI_DI0										
W	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

Reset 1

#### IPUx\_CSIO\_DI field descriptions

Field	Description
31–24 CSI0_MIPI_DI3	CSI0_MIPI_DI3 This field holds the Data Identifier #3 handled by the CSI.
23–16 CSI0_MIPI_DI2	CSI0_MIPI_DI2 This field holds the Data Identifier #2 handled by the CSI.
15–8 CSI0_MIPI_DI1	CSI0_MIPI_DI1 This field holds the Data Identifier #1 handled by the CSI
CSI0_MIPI_DI0	CSI0_MIPI_DI0 This field holds the Data Identifier #0 handled by the CSI; This is the main stream.

### 37.5.160 CSI0 SKIP Register (IPUx\_CSI0\_SKIP)

This register controls the frame skipping supported between CSI0 and the SMFC.

Address: Base address + 3\_0024h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								CSI0_ID_2_SKIP		CSI0_SKIP_SMFC				CSI0_MAX_RATIO_SKIP_SMFC	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_CSI0\_SKIP field descriptions

Field	Description
31–10 Reserved	This read-only field is reserved and always has the value 0.
9–8 CSI0_ID_2_SKIP	CSI0 to SMFC Skipping ID. Data from the CSI0 to the SMFC has an ID associated with it. The ID is received from the MIPI interface. The skipping mechanism between the CSI0 and the SMFC can be used for only one ID. There is no skipping for data coming with ID different from the ID programmed in this bits  00 - Skipping mechanism is activated on frames with ID equal to 00 01 - Skipping mechanism is activated on frames with ID equal to 01 10 - Skipping mechanism is activated on frames with ID equal to 10 11 - Skipping mechanism is activated on frames with ID equal to 11
7–3 CSI0_SKIP_SMFC	CSI0 SKIP SMFC These 5 bits define the skipping pattern of the frames send to the SMFC. Skipping is done for a set of frames. The number of frames in a set is defined at CSI0_MAX_RATIO_SKIP_SMFC.  when CSI0_MAX_RATIO_SKIP_SMFC = 1 => CSI0_SKIP_SMFC[0] is used; other bits are ignored when CSI0_MAX_RATIO_SKIP_SMFC = 2 => CSI0_SKIP_SMFC[1:0] are used; other bits are ignored when CSI0_MAX_RATIO_SKIP_SMFC = 3 => CSI0_SKIP_SMFC[2:0] are used; other bits are ignored when CSI0_MAX_RATIO_SKIP_SMFC = 4 => CSI0_SKIP_SMFC[3:0] are used; other bits are ignored when CSI0_MAX_RATIO_SKIP_SMFC = 5 => CSI0_SKIP_SMFC[4:0] are used; Setting bit #n of CSI0_SKIP_SMFC means that the #n frame in the set is skipped.  For example: if CSI0_MAX_RATIO_SKIP_SMFC = 4 and CSI0_SKIP_SMFC = 11010 Frames #0 & Frame #2 will not be skipped as bit0 and bit2 are cleared Frames #1 & Frame #3 will be skipped as bit1 and bit3 are set bit #4 is ignored as CSI0_MAX_RATIO_SKIP_SMFC is set to 4

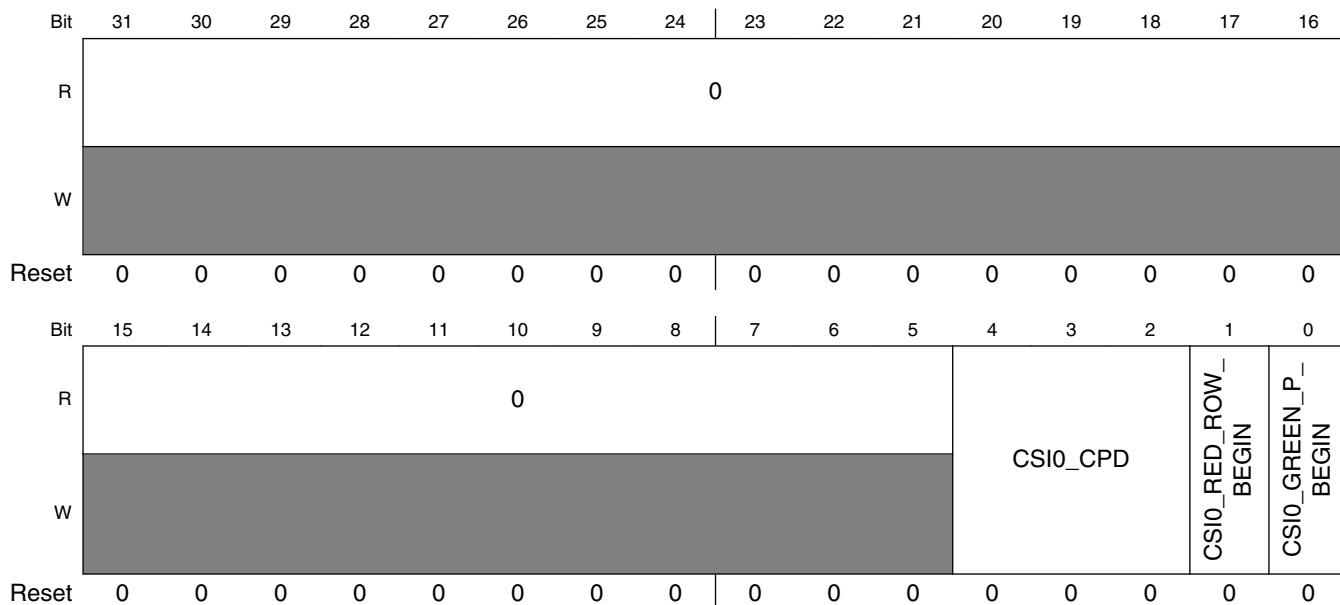
Table continues on the next page...

**IPUx\_CSIO\_SKIP field descriptions (continued)**

Field	Description
CSIO_MAX_RATIO_SKIP_SMFC	CSIO Maximum Ratio Skip for SMFC These bits define the number of frames in a skipping set. The skipping number is equal to CSIO_MAX_RATIO_SKIP_SMFC+1; The maximum value of this bits is 5. When set to 0 the skipping is disabled.

### 37.5.161 CSI0 Compander Control Register (IPUx\_CSIO\_CPD\_CTRL)

Address: Base address + 3\_0028h offset

**IPUx\_CSIO\_CPD\_CTRL field descriptions**

Field	Description
31–5 Reserved	This read-only field is reserved and always has the value 0.
4–2 CSIO_CPD	CSI0_CPD These bits enable the compander in the path to different destination. CSI0_CPD[0] - CSI0_CPD[1] - Enable for the compander for data sent to the IC CSI0_CPD[2] - Enable for the compander for data sent to the IDMAC via SMFC If all the 3 bits are zero the compander is disabled Reserved
1 CSIO_RED_ROW_BEGIN	Color of first row in the frame. Reserved

Table continues on the next page...

**IPUx\_CSIO\_CPD\_CTRL field descriptions (continued)**

Field	Description
	0 First row in the frame is GBGB. 1 First row in the frame is GRGR.
0 CSI0_GREEN_ P_BEGIN	Color of first component in the frame. Reserved 0 First component in the frame is blue or red, depending from RED_ROW bit. 1 First component in the frame is green

### 37.5.162 CSI0 Red Component Compander Constants Register <i> (IPUx\_CSIO\_CPD\_RC\_i)

These registers contain CONSTANT <i> parameters used for companding of red component.

Address: Base address + 3\_002Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

**IPUx\_CSIO\_CPD\_RC\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 CSI0_CPD_RC_2i_1	CONSTANT <2*i+1> parameter of Compander, Red component. Reserved
15–9 Reserved	This read-only field is reserved and always has the value 0.
CSI0_CPD_RC_2i	CONSTANT <2*i> parameter of Compander, Red component. Reserved

### 37.5.163 CSI0 Red Component Compander SLOPE Register <i> (IPUx\_CSIO\_CPD\_RS\_i)

These registers contain SLOPE <i> parameters used for companding of red component.

Address: Base address + 3\_004Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CSI0_CPD_RS_4i_3								CSI0_CPD_RS_4i_2								CSI0_CPD_RS_4i_1				CSI0_CPD_RS_4i											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_CSIO\_CPD\_RS\_i field descriptions

Field	Description
31–24 CSI0_CPD_RS_4i_3	Reserved
23–16 CSI0_CPD_RS_4i_2	Reserved
15–8 CSI0_CPD_RS_4i_1	Reserved
CSI0_CPD_RS_4i	Reserved

### 37.5.164 CSI0 GR Component Compander Constants Register <i> (IPUx\_CSIO\_CPD\_GRC\_i)

These registers contain CONSTANTi parameters used for companding of green components in GRGR rows.

Address: Base address + 3\_005Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								CSI0_CPD_GRC_2i_1								0				CSI0_CPD_GRC_2i											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_CSIO\_CPD\_GRC\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 CSI0_CPD_GRC_2i_1	Reserved
15–9 Reserved	This read-only field is reserved and always has the value 0.
CSI0_CPD_GRC_2i	Reserved

**37.5.165 CSI0 GR Component Compander SLOPE Register <i> (IPUx\_CSIO\_CPD\_GRS\_i)**

These registers contain SLOPEi parameters used for companding of green components in GRGR rows.

Address: Base address + 3\_007Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CSI0_CPD_GRS_4i_3					CSI0_CPD_GRS_4i_2					CSI0_CPD_GRS_4i_1					CSI0_CPD_GRS_4i																
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_CSIO\_CPD\_GRS\_i field descriptions**

Field	Description
31–24 CSI0_CPD_GRS_4i_3	Reserved
23–16 CSI0_CPD_GRS_4i_2	Reserved
15–8 CSI0_CPD_GRS_4i_1	Reserved
CSI0_CPD_GRS_4i	Reserved

### 37.5.166 CSI0 GB Component Compander Constants Register <i> (IPUx\_CSIO\_CPD\_GBC\_i)

These registers contain CONSTANT<sub>i</sub> parameters used for companding of green components in GBGB rows.

Address: Base address + 3\_008Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_CSIO\_CPD\_GBC\_i field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 CSI0_CPD_GBC_2i_1	Reserved
15–9 Reserved	This read-only field is reserved and always has the value 0.
CSI0_CPD_GBC_2i	Reserved

### 37.5.167 CSI0 GB Component Compander SLOPE Register <i> (IPUx\_CSIO\_CPD\_GBS\_i)

These registers contain SLOPE<sub>i</sub> parameters used for companding of green components in GBGB rows.

Address: Base address + 3\_00ACh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_CSIO\_CPD\_GBS\_i field descriptions**

Field	Description
31–24 CSIO_CPD_ GBS_4i_3	Reserved
23–16 CSIO_CPD_ GBS_4i_2	Reserved
15–8 CSIO_CPD_ GBS_4i_1	Reserved
CSIO_CPD_ GBS_4i	Reserved

### 37.5.168 CSI0 Blue Component Compander Constants Register <i> (IPUx\_CSIO\_CPD\_BC\_i)

These registers contain CONSTANTi parameters used for companding of blue component.

Address: Base address + 3\_00BCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R	0																0																	
W																																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

**IPUx\_CSIO\_CPD\_BC\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 CSIO_CPD_BC_ 2i_1	Reserved
15–9 Reserved	This read-only field is reserved and always has the value 0.
CSIO_CPD_BC_ 2i	Reserved

### 37.5.169 CSI0 Blue Component Compander SLOPE Register <i> (IPUx\_CSIO\_CPD\_BS\_i)

These registers contain SLOPEi parameters used for companding of red component.

Address: Base address + 3\_00DCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CSI0_CPD_BS_4i_3								CSI0_CPD_BS_4i_2								CSI0_CPD_BS_4i_1				CSI0_CPD_BS_4i											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_CSIO\_CPD\_BS\_i field descriptions

Field	Description
31–24 CSI0_CPD_BS_4i_3	Reserved
23–16 CSI0_CPD_BS_4i_2	Reserved
15–8 CSI0_CPD_BS_4i_1	Reserved
CSI0_CPD_BS_4i	Reserved

### 37.5.170 CSI0 Compander Offset Register 1 (IPUx\_CSIO\_CPD\_OFFSET1)

These registers contain Offset parameters used for companding.

Address: Base address + 3\_00ECh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		CSI0_CPD_B_OFFSET								CSI0_GB_OFFSET								CSI0_GR_OFFSET													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_CSIO\_CPD\_OFFSET1 field descriptions

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_CSI0\_CPD\_OFFSET1 field descriptions (continued)**

Field	Description
29–20 CSI0_CPD_B_OFFSET	Reserved
19–10 CSI0_GB_OFFSET	Reserved
CSI0_GR_OFFSET	Reserved

### 37.5.171 CSI0 Compander Offset Register 2 (IPUx\_CSI0\_CPD\_OFFSET2)

This register contain Offset parameters used for companding.

Address: Base address + 3\_00F0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
R																	0																		
W																																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

**IPUx\_CSI0\_CPD\_OFFSET2 field descriptions**

Field	Description
31–10 Reserved	This read-only field is reserved and always has the value 0.
CSI0_CPD_R_OFFSET	CSI0 Red component offset The value is between -512 to 511. The value is added to the red component before companding. Clipping: If the result of the red components value + the offset is smaller than 0, the result is zero If the result of the red components value + the offset is greater than 1023, the result is 1023 Reserved

### 37.5.172 CSI1 Sensor Configuration Register (IPUx\_CSI1\_SENS\_CONF)

Address: Base address + 3\_8000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	CSI0_DATA_EN_POL	0	CSI1_FORCE_EOF	CSI1_JPEG_MODE	CSI1_JPEG8_EN	CSI1_DATA_DEST										
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CSI1_EXT_VSYNC								CSI1_PACK_TIGHT				CSI1_SENS_PIX_CLK_POL	CSI1_DATA_POL	CSI1_HSYNC_POL	CSI1_VSYNC_POL
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_CSI1\_SENS\_CONF field descriptions

Field	Description
31 CSI0_DATA_EN_POL	Invert IPP_IND_SENSB_DATA_EN input. This bit selects the polarity of IPP_IND_SENSB_DATA_EN signal.  0 IPP_IND_SENSB_DATA_EN is directly applied to internal circuitry. 1 IPP_IND_SENSB_DATA_EN is inverted before applied to internal circuitry.
30 Reserved	This read-only field is reserved and always has the value 0.
29 CSI1_FORCE_EOF	Force End of frame  This is a self clear bit allowing the user to force an End-of-frame event; This bit can be used in cases where the frame sent by the sensor was not completed.  1 force end of frame 0 no action
28 CSI1_JPEG_MODE	JPEG Mode - this bit defines the mode of the control signals when working in JPEG mode  1 The data is valid as long as HSYNC and VSYNC signals are active; HSYNC is valid for single frame 0 The frame starts with the assertion of VSYNC. The frame ends on the next VSYNC or by setting the <b>CSI0_FORCE_EOF</b> bit
27 CSI1_JPEG8_EN	JPEG8 enable bit  1 JPEG8 detection is enabled 0 JPEG8 is disabled

Table continues on the next page...

**IPUx\_CSI1\_SENS\_CONF field descriptions (continued)**

Field	Description
26–24 CSI1_DATA_DEST	These bits enable the destination of the data coming from the CSI. CSI1_DATA_DEST[0] - Reserved CSI1_DATA_DEST[1] - destination is IC CSI1_DATA_DEST[2] - destination is IDMAC via SMFC
23–16 CSI1_DIV_RATIO	DIV Ratio Clock division ratio minus 1. This field defines the division ratio of HSP_CLK into SENS_B_MCLK: SENS_B_MCLK rate = HSP_CLK rate /(DIV_RATIO+1)
15 CSI1_EXT_VSYNC	External VSYNC enable. This bits select between external and internal VSYNC. 0 Internal VSYNC mode. 1 External VSYNC mode.
14–11 CSI1_DATA_WIDTH	Data width. This fields defines the number of bits per color. Values: 0000 4 bits per color 0000 Reserved 0001 8 bits per color 0010 9 bits per color 0010 Reserved 0011 10 bits per color 0100 11 bits per color 0100 Reserved 0101 12 bits per color 0101 Reserved 0110 13 bits per color 0110 Reserved 0111 14 bits per color 0111 Reserved 1000 15 bits per color 1000 Reserved 1001 16 bits per color
10–8 CSI1_SENS_DATA_FORMAT	Data format from the sensor. This field defines the data format for the input of the CSI sensor. Values: 000 full RGB or YUV444 001 YUV422 (YUYV...) 010 YUV422 (UYVY...) 011 Bayer or Generic data 100 RGB565 101 RGB555 110 RGB444 111 JPEG
7 CSI1_PACK_TIGHT	<b>CSI1 Pack Tight</b> When the data format is YUV or RGB and the component's width is 9-16 bits, it can be sent to the memory in 2 different ways

*Table continues on the next page...*

**IPUx\_CSI1\_SENS\_CONF field descriptions (continued)**

Field	Description
	<p>1 Three 10 bits components are packed into a 32 bit word. Color extension/reduction is performed      0 Each component is written as a 16 bit word where the MSB is written to bit #15, color extension is done for the remaining least significant bits.</p>
6–4 CSI1_SENS_PRTCL	<p>Sensor Protocol. This bit defines the Sensor timing/data mode protocol.      Values:</p> <ul style="list-style-type: none"> <li>000 Gated clock mode</li> <li>001 Non-gated clock mode</li> <li>010 CCIR progressive mode (BT.656)</li> <li>011 CCIR interlaced mode (BT.656)</li> <li>100 CCIR progressive (BT.1120 DDR mode: data arrives on every edge of the clock)</li> <li>101 CCIR progressive (BT.1120 SDR mode: data arrives only on the positive edge of the clock)</li> <li>110 CCIR interlaced mode (BT.1120 DDR mode: data arrives on every edge of the clock)</li> <li>111 CCIR interlaced mode (BT.1120 SDR mode: data arrives only on the positive edge of the clock)</li> </ul>
3 CSI1_SENS_PIX_CLK_POL	<p>Invert Pixel clock input. This bit selects the polarity of pixel clock.      0 pixel clock is directly applied to internal circuitry.      1 pixel clock is inverted before applied to internal circuitry.</p>
2 CSI1_DATA_POL	<p>Invert data input. This bit selects the polarity of data input.      0 data lines are directly applied to internal circuitry.      1 data lines are inverted before applied to internal circuitry.</p>
1 CSI1_HSYNC_POL	<p>Invert IPP_IND_SENSB_HSYNC input. This bit selects the polarity of IPP_IND_SENSB_HSYNC signal.      0 IPP_IND_SENSB_HSYNC is directly applied to internal circuitry.      1 IPP_IND_SENSB_HSYNC is inverted before applied to internal circuitry.</p>
0 CSI1_VSYNC_POL	<p>Invert IPP_IND_SENSB_VSYNC input. This bit selects the polarity of IPP_IND_SENSB_VSYNC signal.      0 IPP_IND_SENSB_VSYNC is not inverted before applied to internal circuitry.      1 IPP_IND_SENSB_VSYNC is inverted before applied to internal circuitry.</p>

**37.5.173 CSI1 Sense Frame Size Register (IPUx\_CSI1\_SENS\_FRM\_SIZE)**

Address: Base address + 3\_8004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R					0												0																	
W																																		

Reset 0

**IPUx\_CSI1\_SENS\_FRM\_SIZE field descriptions**

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_CSI1\_SENS\_FRM\_SIZE field descriptions (continued)**

Field	Description
27–16 CSI1_SENS_ FRM_HEIGHT	Sensor frame height minus 1. This field defines the sensor frame rows number minus 1.
15–13 Reserved	This read-only field is reserved and always has the value 0.
CSI1_SENS_ FRM_WIDTH	Sensor frame width minus 1. This field defines the sensor frame column number minus 1.

### 37.5.174 CSI1 Actual Frame Size Register (IPUx\_CSI1\_ACT\_FRM\_SIZE)

Address: Base address + 3\_8008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R	0																0																	
W																																		

Reset 0

**IPUx\_CSI1\_ACT\_FRM\_SIZE field descriptions**

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 CSI1_ACT_ FRM_HEIGHT	Actual frame height minus 1. This field defines the CSI output frame rows number minus 1.
15–13 Reserved	This read-only field is reserved and always has the value 0.
CSI1_ACT_ FRM_WIDTH	Actual frame width minus 1. This field defines the CSI output frame columns number minus 1.

### 37.5.175 CSI1 Output Control Register (IPUx\_CSI1\_OUT\_FRM\_CTRL)

Address: Base address + 3\_800Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	CSI1_HORZ_DWNS	CSI1_VERT_DWNS	0														
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R			0														
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_CSI1\_OUT\_FRM\_CTRL field descriptions

Field	Description
31 CSI1_HORZ_DWNS	Enable horizontal downsizing (decimation) by 2. 0 Downsizing disabled 1 Downsizing enabled
30 CSI1_VERT_DWNS	Enable vertical downsizing (decimation) by 2. 0 Downsizing disabled 1 Downsizing enabled
29 Reserved	This read-only field is reserved and always has the value 0.
28–16 CSI1_HSC	Horizontal skip. This field defines the number of columns to skip. In Interlaced mode this number refers to the number of lines per field
15–12 Reserved	This read-only field is reserved and always has the value 0.
CSI1_VSC	Vertical skip. This field defines the number of rows to skip.

### 37.5.176 CSI1 Test Control Register (IPUx\_CSI1\_TST\_CTRL)

Address: Base address + 3\_8010h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R								0									
W															PG_B_VALUE		
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R															PG_R_VALUE		
W															PG_G_VALUE		
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_CSI1\_TST\_CTRL field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24 TEST_GEN_MODE	Test generator mode. This bit activates the signal generation. 0 Test signal generator is inactive. 1 Test signal generator is active.
23–16 PG_B_VALUE	Pattern generator B value. This field selects the B value for the generated pattern of even pixel.
15–8 PG_G_VALUE	Pattern generator G value. This field selects the G value for the generated pattern of even pixel.
PG_R_VALUE	Pattern generator R value. This field selects the R value for the generated pattern of even pixel.

### 37.5.177 CSI1 CCIR Code Register 1 (IPUx\_CSI1\_CCIR\_CODE\_1)

Address: Base address + 3\_8014h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R								CSI1_CCIR_ERR_DET_EN	0							
W											CSI1_STRT_FLD0_ACTV			CSI1_END_FLD0_ACTV		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0					CSI1_STRT_FLD0_BLNK_2ND		CSI1_END_FLD0_BLNK_2ND		CSI1_STRT_FLD0_BLNK_1ST		CSI1_END_FLD0_BLNK_1ST	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_CSI1\_CCIR\_CODE\_1 field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24 CSI1_CCIR_ERR_DET_EN	Enable error detection and correction for CCIR interlaced mode with protection bit. 0 Error detection and correction is disabled. 1 Error detection and correction is enabled.
23–22 Reserved	This read-only field is reserved and always has the value 0.
21–19 CSI1_STRT_FLD0_ACTV	Start of field 0 active line command (interlaces mode). (In progressive mode, start of active line command mode).
18–16 CSI1_END_FLD0_ACTV	End of field 0 active line command (interlaces mode). (In progressive mode, end of active line command mode).
15–12 Reserved	This read-only field is reserved and always has the value 0.
11–9 CSI1_STRT_FLD0_BLNK_2ND	Start of field 0 second blanking line command (interlaces mode). (In progressive mode this field is ignored).
8–6 CSI1_END_FLD0_BLNK_2ND	End of field 0 second blanking line command (interlaces mode). (In progressive mode this field is ignored).

Table continues on the next page...

**IPUx\_CSI1\_CCIR\_CODE\_1 field descriptions (continued)**

Field	Description
5–3 CSI1_STRT_ FLD0_BLNK_ 1ST	Start of field 0 first blanking line command (interlaces mode). (In progressive mode this field indicates start of blanking line command).
CSI1_END_ FLD0_BLNK_ 1ST	End of field 0 first blanking line command (interlaces mode). (In progressive mode this field is ignored).

**37.5.178 CSI1 CCIR Code Register 2 (IPUx\_CSI1\_CCIR\_CODE\_2)**

Address: Base address + 3\_8018h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_CSI1\_CCIR\_CODE\_2 field descriptions**

Field	Description
31–22 Reserved	This read-only field is reserved and always has the value 0.
21–19 CSI1_STRT_ FLD1_ACTV	Start of field 1 active line command (interlaces mode). (In progressive mode this field is ignored).
18–16 CSI1_END_ FLD1_ACTV	End of field 1 active line command (interlaces mode). (In progressive mode this field is ignored).
15–12 Reserved	This read-only field is reserved and always has the value 0.
11–9 CSI1_STRT_ FLD1_BLNK_ 2ND	Start of field 1 second blanking line command (interlaces mode). (In progressive mode this field is ignored).
8–6 CSI1_END_ FLD1_BLNK_ 2ND	End of field 1 second blanking line command (interlaces mode). (In progressive mode this field is ignored).
5–3 CSI1_STRT_ FLD1_BLNK_ 1ST	Start of field 1 first blanking line command (interlaces mode). (In progressive mode this field is ignored).
CSI1_END_ FLD1_BLNK_ 1ST	End of field 1 first blanking line command (interlaces mode). (In progressive mode this field is ignored).

### 37.5.179 CSI1 CCIR Code Register 3 (IPUx\_CSI1\_CCIR\_CODE\_3)

Address: Base address + 3\_801Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																	CSI1_CCIR_PRECOM															
W																																	

Reset 0

#### IPUx\_CSI1\_CCIR\_CODE\_3 field descriptions

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.
CSI1_CCIR_PRECOM	CCIR pre command. This field defines the sequence which comes before the CCIR command. For BT.656 the code should be written to bits [23:0] while bits [29:24] are ignored (3X8bit) For BT.1120 the code should be written to bits [29:0] (3X10bit)

### 37.5.180 CSI1 Data Identifier Register (IPUx\_CSI1\_DI)

Address: Base address + 3\_8020h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	CSI1_MIPI_DI3		CSI1_MIPI_DI2		CSI0_MIPI_DI1		CSI1_MIPI_DI0										
W	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

Reset 1

#### IPUx\_CSI1\_DI field descriptions

Field	Description
31–24 CSI1_MIPI_DI3	CSI1_MIPI_DI3 This field holds the Data Identifier #3 handled by the CSI.
23–16 CSI1_MIPI_DI2	CSI1_MIPI_DI2 This field holds the Data Identifier #2 handled by the CSI.
15–8 CSI0_MIPI_DI1	CSI1_MIPI_DI1 This field holds the Data Identifier #1 handled by the CSI
CSI1_MIPI_DI0	CSI1_MIPI_DI0 This field holds the Data Identifier #0 handled by the CSI; This is the main stream.

### 37.5.181 CSI1 SKIP Register (IPUx\_CSI1\_SKIP)

This register controls the frame skipping supported between CSI1 and the SMFC.

Address: Base address + 3\_8024h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								CSI1_ID_2_SKIP		CSI1_SKIP_SMFC				CSI1_MAX_RATIO_SKIP_SMFC	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_CSI1\_SKIP field descriptions

Field	Description
31–10 Reserved	This read-only field is reserved and always has the value 0.
9–8 CSI1_ID_2_SKIP	CSI1 to SMFC Skipping ID. Data from the CSI1 to the SMFC has an ID associated with it. The ID is received from the MIPI interface. The skipping mechanism between the CSI1 and the SMFC can be used for only one ID. There is no skipping for data coming with ID different from the ID programmed in this bits  00 - Skipping mechanism is activated on frames with ID equal to 00 01 - Skipping mechanism is activated on frames with ID equal to 01 10 - Skipping mechanism is activated on frames with ID equal to 10 11 - Skipping mechanism is activated on frames with ID equal to 11
7–3 CSI1_SKIP_SMFC	CSI1 SKIP SMFC These 5 bits define the skipping pattern of the frames sent to the SMFC. Skipping is done for a set of frames. The number of frames in a set is defined at CSI1_MAX_RATIO_SKIP_SMFC.  when CSI1_MAX_RATIO_SKIP_SMFC = 1 => CSI1_SKIP_SMFC[0] is used; other bits are ignored when CSI1_MAX_RATIO_SKIP_SMFC = 2 => CSI1_SKIP_SMFC[1:0] are used; other bits are ignored when CSI1_MAX_RATIO_SKIP_SMFC = 3 => CSI1_SKIP_SMFC[2:0] are used; other bits are ignored when CSI1_MAX_RATIO_SKIP_SMFC = 4 => CSI1_SKIP_SMFC[3:0] are used; other bits are ignored when CSI1_MAX_RATIO_SKIP_SMFC = 5 => CSI1_SKIP_SMFC[4:0] are used; Setting bit #n of CSI1_SKIP_SMFC means that the #n frame in the set is skipped.  For example: if CSI1_MAX_RATIO_SKIP_SMFC = 4 and CSI1_SKIP_SMFC = 11010 Frames #0 & Frame #2 will not be skipped as bit0 and bit2 are cleared Frames #1 & Frame #3 will be skipped as bit1 and bit3 are set bit #4 is ignored as CSI1_MAX_RATIO_SKIP_SMFC is set to 4

Table continues on the next page...

**IPUx\_CSI1\_SKIP field descriptions (continued)**

Field	Description
CSI1_MAX_RATIO_SKIP_SMFC	CSI1 Maximum Ratio Skip for SMFC These bits define the number of frames in a skipping set. These bits define the number of frames in a skipping set. The skipping number is equal to CSI1_MAX_RATIO_SKIP_SMFC+1; The maximum value of this bits is 5. When set to 0 the skipping is disabled.

### 37.5.182 CSI1 Compander Control Register (IPUx\_CSI1\_CPD\_CTRL)

Address: Base address + 3\_8028h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	R								0							
	W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R								0				0	0	0	0
	W													0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_CSI1\_CPD\_CTRL field descriptions**

Field	Description
31–5 Reserved	This read-only field is reserved and always has the value 0.
4–2 Reserved	This read-only field is reserved and always has the value 0.
1 Reserved	This read-only field is reserved and always has the value 0.
0 Reserved	This read-only field is reserved and always has the value 0.

### 37.5.183 CSI1 Red Component Comander Constants Register <i> (IPUx\_CSI1\_CPD\_RC\_i)

These registers contain CONSTANT <i> parameters used for companding of red component.

Address: Base address + 3\_802Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_CSI1\_CPD\_RC\_i field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 CSI1_CPD_RC_2i_1	CONSTANT <2*i+1> parameter of Comander, Red component. Reserved
15–9 Reserved	This read-only field is reserved and always has the value 0.
CSI1_CPD_RC_2i	CONSTANT <2*i> parameter of Comander, Red component. Reserved

### 37.5.184 CSI1 Red Component Comander SLOPE Register <i> (IPUx\_CSI1\_CPD\_RS\_i)

These registers contain SLOPE <i> parameters used for companding of red component.

Address: Base address + 3\_804Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_CSI1\_CPD\_RS\_i field descriptions**

Field	Description
31–24 CSI1_CPD_RS_4i_3	SLOPE<4*i+3> parameter of Compander, Red component. Reserved
23–16 CSI1_CPD_RS_4i_2	SLOPE<4*i+2> parameter of Compander, Red component. Reserved
15–8 CSI1_CPD_RS_4i_1	SLOPE<4*i+1> parameter of Compander, Red component. Reserved
CSI1_CPD_RS_4i	SLOPE<4*i> parameter of Compander, Red component. Reserved

**37.5.185 CSI1 GR Component Compander Constants Register <i> (IPUx\_CSI1\_CPD\_GRC\_i)**

These registers contain CONSTANTi parameters used for companding of green components in GRGR rows.

Address: Base address + 3\_805Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_CSI1\_CPD\_GRC\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 CSI1_CPD_GRC_2i_1	CONST<2*i+1> parameter of Compander, GR component. If the input format is RGB/YUV then CSI1_CPD_GRC should be equal to CSI1_CPD_GBC Reserved
15–9 Reserved	This read-only field is reserved and always has the value 0.
CSI1_CPD_GRC_2i	CONSTANT<2*i> parameter of Compander, GR component. If the input format is RGB/YUV then CSI1_CPD_GRC should be equal to CSI1_CPD_GBC Reserved

### 37.5.186 CSI1 GR Component Compander SLOPE Register <i> (IPUx\_CSI1\_CPD\_GRS\_i)

These registers contain SLOPEi parameters used for companding of green components in GRGR rows.

Address: Base address + 3\_807Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CSI1_CPD_GRS_4i_3								CSI1_CPD_GRS_4i_2								CSI1_CPD_GRS_4i_1				CSI1_CPD_GRS_4i											
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_CSI1\_CPD\_GRS\_i field descriptions

Field	Description
31–24 CSI1_CPD_GRS_4i_3	SLOPE<4*i+3> parameter of Compander, GR component. If the input format is RGB/YUV then CSI1_CPD_GRS should be equal to CSI1_CPD_GBS Reserved
23–16 CSI1_CPD_GRS_4i_2	SLOPE<4*i+2> parameter of Compander, GR component. If the input format is RGB/YUV then CSI1_CPD_GRS should be equal to CSI1_CPD_GBS Reserved
15–8 CSI1_CPD_GRS_4i_1	SLOPE<4*i+1> parameter of Compander, GR component. If the input format is RGB/YUV then CSI1_CPD_GRS should be equal to CSI1_CPD_GBS Reserved
CSI1_CPD_GRS_4i	SLOPE<4*i> parameter of Compander, GR component. If the input format is RGB/YUV then CSI1_CPD_GRS should be equal to CSI1_CPD_GBS Reserved

### 37.5.187 CSI1 GB Component Compander Constants Register <i> (IPUx\_CSI1\_CPD\_GBC\_i)

These registers contain CONSTANTi parameters used for companding of green components in GBGB rows.

Address: Base address + 3\_808Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								CSI1_CPD_GBC_2i_1								0				CSI1_CPD_GBC_2i											
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_CSI1\_CPD\_GBC\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 CSI1_CPD_GBC_2i_1	CONST $i+1$ parameter of Compander, GB component. If the input format is RGB/YUV then CSI1_CPD_GBC should be equal to CSI1_CPD_GRC Reserved
15–9 Reserved	This read-only field is reserved and always has the value 0.
CSI1_CPD_GBC_2i	CONSTANT $i$ parameter of Compander, GB component. If the input format is RGB/YUV then CSI1_CPD_GBC should be equal to CSI1_CPD_GRC Reserved

**37.5.188 CSI1 GB Component Compander SLOPE Register <i> (IPUx\_CSI1\_CPD\_GBS\_i)**

These registers contain SLOPE $i$  parameters used for companding of green components in GBGB rows.

Address: Base address + 3\_80ACh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CSI1_CPD_GBS_4i_3								CSI1_CPD_GBS_4i_2								CSI1_CPD_GBS_4i_1								CSI1_CPD_GBS_4i							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_CSI1\_CPD\_GBS\_i field descriptions**

Field	Description
31–24 CSI1_CPD_GBS_4i_3	SLOPE<4*i+3> parameter of Compander, GB component. If the input format is RGB/YUV then CSI1_CPD_GBS should be equal to CSI1_CPD_GRS Reserved
23–16 CSI1_CPD_GBS_4i_2	SLOPE<4*i+2> parameter of Compander, GB component. If the input format is RGB/YUV then CSI1_CPD_GBS should be equal to CSI1_CPD_GRS Reserved
15–8 CSI1_CPD_GBS_4i_1	SLOPE<4*i+1> parameter of Compander, GB component. If the input format is RGB/YUV then CSI1_CPD_GBS should be equal to CSI1_CPD_GRS Reserved
CSI1_CPD_GBS_4i	SLOPE<4*i> parameter of Compander, GB component. If the input format is RGB/YUV then CSI1_CPD_GBS should be equal to CSI1_CPD_GRS Reserved

### 37.5.189 CSI1 Blue Component Compander Constants Register <i> (IPUx\_CSI1\_CPD\_BC\_i)

These registers contend CONSTANT $i$  parameters used for companding of blue component.

Address: Base address + 3\_80BCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_CSI1\_CPD\_BC\_i field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 CSI1_CPD_BC_2i_1	CONSTANT $<2*i+1>$ parameter of Compander, Blue component. Reserved
15–9 Reserved	This read-only field is reserved and always has the value 0.
CSI1_CPD_BC_2i	CONSTANT $<2*i>$ parameter of Compander, Blue component. Reserved

### 37.5.190 CSI1 Blue Component Compander SLOPE Register <i> (IPUx\_CSI1\_CPD\_BS\_i)

This registers contain SLOPE $i$  parameters used for companding of red component.

Address: Base address + 3\_80DCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_CSI1\_CPD\_BS\_i field descriptions**

Field	Description
31–24 CSI1_CPD_BS_4i_3	SLOPE<4*i+3> parameter of Compander, Blue component. Reserved
23–16 CSI1_CPD_BS_4i_2	SLOPE<4*i+2> parameter of Compander, Blue component. Reserved
15–8 CSI1_CPD_BS_4i_1	SLOPE<4*i+1> parameter of Compander, Blue component. Reserved
CSI1_CPD_BS_4i	SLOPE<4*i> parameter of Compander, Blue component. Reserved

### 37.5.191 CSI1 Compander Offset Register 1 (IPUx\_CSI1\_CPD\_OFFSET1)

These registers contain Offset parameters used for companding.

Address: Base address + 3\_80ECh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

**IPUx\_CSI1\_CPD\_OFFSET1 field descriptions**

Field	Description
31–30 Reserved	This read-only field is reserved and always has the value 0.
29–20 CSI1_CPD_B_OFFSET	CSI1 Blue component offset The value is between -512 to 511. The value is added to the blue component before companding. Clipping: If the result of the blue components value + the offset is smaller than 0, the result is zero If the result of the blue components value + the offset is greater than 1023, the result is 1023 Reserved
19–10 CSI1_CPD_GB_OFFSET	CSI1 Green Blue component offset The value is between -512 to 511. The value is added to the blue component before companding. Clipping: If the result of the green-blue components value + the offset is smaller than 0, the result is zero If the result of the green-blue components value + the offset is greater than 1023, the result is 1023

*Table continues on the next page...*

**IPUx\_CSI1\_CPD\_OFFSET1 field descriptions (continued)**

Field	Description
	If the input format is RGB/YUV then CSI1_GR_OFFSET must be equal to CSI1_GR_OFFSET Reserved
CSI1_CPD_GR_OFFSET	CSI1 Green Red component offset The value is between -512 to 511. The value is added to the green-red component before companding. Clipping: If the result of the green-red components value + the offset is smaller than 0, the result is zero If the result of the green-red components value + the offset is greater than 1023, the result is 1023 Reserved

### 37.5.192 CSI1 Compander Offset Register 2 (IPUx\_CSI1\_CPD\_OFFSET2)

These registers contain Offset parameters used for companding.

Address: Base address + 3\_80F0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																0																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_CSI1\_CPD\_OFFSET2 field descriptions**

Field	Description
31–10 Reserved	This read-only field is reserved and always has the value 0.
CSI1_CPD_R_OFFSET	CSI1 Red component offset The value is between -512 to 511. The value is added to the red component before companding. Clipping: If the result of the red components value + the offset is smaller than 0, the result is zero If the result of the red components value + the offset is greater than 1023, the result is 1023 Reserved

### 37.5.193 DI0 General Register (IPUx\_DI0\_GENERAL)

Address: Base address + 4\_0000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	di0_pin8_pin15_sel		di0_disp_y_sel		DI0_CLOCK_STOP_MODE				DI0_DISP_CLOCK_INIT	di0_mask_sel	di0_vsync_ext	di0_clk_ext	DI0_WATCHDOG_MODE	di0_polarity_disp_clk	0	
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		di0_sync_count_sel		di0_err_treatment	di0_err_vsync_sel	di0_polarity_cs1	di0_polarity_cs0									di0_polarity_i_1
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_GENERAL field descriptions

Field	Description
31 di0_pin8_pin15_sel	This bit routes PIN8 over PIN15  1 PIN8 is routed to PIN15, PIN8 is also routed to PIN8 0 PIN15 is routed to PIN15, PIN8 is routed to PIN8
30–28 di0_disp_y_sel	DI0 Display Vertical coordinate (Y) select.  This field defines which one of the 8 counters will be used as a display's line counter.  000 counter #1 is selected 111 counter #8 is selected
27–24 DI0_CLOCK_STOP_MODE	DI clock stop mode  When performing a clock change. The DI stops the clock to the display.  These field defines when the clock will be stopped.  Stopping at EOL/EOF is supported for the case where the data is coming from the IDMAC (DMA access). In case that only direct accesses is performed, the user should set this field to 0000  0001-1001 stop at the next event of one of the counters (counter #1 to counter #9)  0000 stop at the next edge of the display clock 1100 stop at EOL (end of a line), but if stop request is during blanking interval, stop now 1101 stop at EOF (end of a frame), but if stop request is during blanking interval, stop now 1110 stop at EOL (end of a line), but if stop request is during blanking interval, stop at the end of the next line 1111 stop at EOF (end of a frame), but if stop request is during blanking interval, stop at the end of the next frame

Table continues on the next page...

**IPUX\_DIO\_GENERAL field descriptions (continued)**

Field	Description
23 DIO_DISP_CLOCK_INIT	Display clock's initial mode For synchronization error conditions the display clock can be stopped on the next VSYNC 1 The display's clock is running after the next VSYNC (indicating new frame) 0 The display's clock is stopped after the next VSYNC (indicating new frame)
22 di0_mask_sel	DIO Mask select. IPP_PIN_2 output of the DI that functions as MASK signal can come from 2 sources: counter #2 or extracted from the MASK data coming from the memory. 1 IPP_PIN_2 is coming from extracted MASK data coming from the memory 0 IPP_PIN_2 is coming from counter #2
21 di0_vsync_ext	DIO External VSYNC. This bit selects the source of the VSYNC signal 1 External to the IPU 0 Internally generated by the IPU
20 di0_clk_ext	DIO External Clock. This bit selects the source of the DIO's clock 1 The source of the clock is external to the IPU 0 The clock is internally generated by the IPU
19–18 DIO_WATCHDOG_MODE	DIO watchdog mode In case of a display error where the DI clock is stopped (defined at di0_err_treatment). An internal watchdog counts DI clocks. If this timer reached its pre defined value the DI will skip the current frame and restart on the frame. This 2 bits define the number of DI clock cycles that the timer counts. 00 The timer counts 4 DI cycles 01 The timer counts 16 DI cycles 10 The timer counts 64 DI cycles 11 The timer counts 128 DI cycles
17 di0_polarity_disp_clk	DIO Output Clock's polarity This bits define the polarity of the DIO's clock. 1 The output clock is active high 0 The output clock is active low
16 Reserved	This read-only field is reserved and always has the value 0.
15–12 di0_sync_count_sel	For synchronous flow error: selects synchronous flow synchronization counter in DI:
11 di0_err_treatment	In case of synchronous flow error there are 2 ways to handle the display 1 to wait (stop clock) 0 Drive the last component
10 di0_err_vsystc_sel	DIO error recovery block's VSYNC source select The error recovery block detect a case where the DI's VSYNC is asserted before the EOF. This bit selects the source of the VSYNC signal monitored by this mechanism.

*Table continues on the next page...*

**IPUx\_DI0\_GENERAL field descriptions (continued)**

Field	Description
	1 vsync_post - an internal VSYNC signal asserted 2 lines after the DI's VSYNC 0 vsync_pre - an internal VSYNC signal asserted 2 lines before the DI's VSYNC
9 di0_polarity_cs1	DI0 Chip Select's 1 polarity This bits define the polarity of the DI's CS1. 1 The CS1 is active high 0 The CS1 is active low
8 di0_polarity_cs0	DI0 Chip Select's 0 polarity This bits define the polarity of the DI's CS0. 1 The CS0 is active high 0 The CS0 is active low
di0_polarity_i_1	DI0 output pin's polarity This bits define the polarity of each of the DI's outputs. 1 The output pin is active high 0 The output pin is active low

### 37.5.194 DI0 Base Sync Clock Gen 0 Register (IPUx\_DI0\_BS\_CLKGEN0)

Address: Base address + 4\_0004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

**IPUx\_DI0\_BS\_CLKGEN0 field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di0_disp_clk_offset	DI0 Display Clock Offset The DI has the ability to delay the display's clock This field defines the amount of IPU's clock cycles added as delay on this clock.
15–12 Reserved	This read-only field is reserved and always has the value 0.
di0_disp_clk_period	DI0 Display Clock Period This field defines the Display interface clock period for display write access. This parameter contains an integer part (bits 11:4) and a fractional part (bits 3:0). It defines a fractional division ratio of the HSP_CLK clock for generation of the display's interface clock.

### 37.5.195 DI0 Base Sync Clock Gen 1 Register (IPUx\_DI0\_BS\_CLKGEN1)

Address: Base address + 4\_0008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

#### IPUx\_DI0\_BS\_CLKGEN1 field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di0_disp_clk_down	DI0 display clock falling edge position This parameter contains an integer part (bits 24:17) and a fractional part (bit 16). The position value is a time interval between display's access start point and display's interface clock falling edge.
15–9 Reserved	This read-only field is reserved and always has the value 0.
di0_disp_clk_up	DI0 display clock rising edge position This parameter contains an integer part (bits 8:1) and a fractional part (bit 0). The position value is a time interval between display's access start point and display's interface clock rising edge.

### 37.5.196 DI0 Sync Wave Gen 1 Register 0 (IPUx\_DI0\_SW\_GEN0\_1)

Address: Base address + 4\_000Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN0\_1 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN0\_1 field descriptions (continued)**

Field	Description
30–19 di0_run_value_m1_1	<p>DI0 counter #1 pre defined value</p> <p>This fields defines the counter #1 pre defines value. When the counter is auto reload mode (di0_cnt_auto_reload_1 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di0_step_repeat field.</p>
18–16 di0_run_resolution_1	<p>DI0 counter #1 Run Resolution</p> <p>This field defines the trigger causing the counter to increment.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 NA</li> <li>011 NA</li> <li>100 NA</li> <li>101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSIs according to the CSI_VSYNC_DEST bit. —</li> <li>110 External VSYNC</li> <li>111 Counter is always on.</li> </ul>
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di0_offset_value_1	<p>DI0 counter #1 offset value</p> <p>The counter can start counting after a pre defined delay</p> <p>This field defines the amount of cycles that the counter will be delayed by</p>
di0_offset_resolution_1	<p>DI0 counter #1 offset Resolution</p> <p>This field defines the trigger causing the offset counter to increment</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock</li> <li>010 NA</li> <li>011 NA</li> <li>100 NA</li> <li>101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSIs according to the CSI_VSYNC_DEST bit. —</li> <li>110 External VSYNC</li> <li>111 Counter is always on.</li> </ul>

### 37.5.197 DI0 Sync Wave Gen 2 Register 0 (IPUx\_DI0\_SW\_GEN0\_2)

Address: Base address + 4\_0010h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															di0_run_resolution_2
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															di0_offset_resolution_2
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN0\_2 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di0_run_value_m1_2	DI0 counter #2 pre defined value  This fields defines the counter #2 pre defines value. When the counter is auto reload mode (di0_cnt_auto_reload_2 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di0_step_repeat field.
18–16 di0_run_resolution_2	DI0 counter #2 Run Resolution  This field defines the trigger causing the counter to increment.  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock 010 The Counter is triggered by counter #1 011 NA 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di0_offset_value_2	DI0 counter #2 offset value  The counter can start counting after a pre defined delay  This field defines the amount of cycles that the counter will be delayed by
di0_offset_resolution_2	DI0 counter #2 offset Resolution  This field defines the trigger causing the offset counter to increment  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN0\_2 field descriptions (continued)**

Field	Description
	011 NA 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSIs according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.

### 37.5.198 DI0 Sync Wave Gen 3 Register 0 (IPUx\_DI0\_SW\_GEN0\_3)

Address: Base address + 4\_0014h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DI0\_SW\_GEN0\_3 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di0_run_value_m1_3	DI0 counter #3 pre defined value  This fields defines the counter #3 pre defines value. When the counter is auto reload mode (di0_cnt_auto_reload_3 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di0_step_repeat field.
18–16 di0_run_resolution_3	DI0 counter #3 Run Resolution  This field defines the trigger causing the counter to increment.  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN0\_3 field descriptions (continued)**

Field	Description
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di0_offset_value_3	DI0 counter #3 offset value The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by
di0_offset_resolution_3	DI0 counter #3 offset Resolution This field defines the trigger causing the offset counter to increment 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.

**37.5.199 DI0 Sync Wave Gen 4 Register 0  
(IPUx\_DI0\_SW\_GEN0\_4)**

Address: Base address + 4\_0018h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	di0_run_value_m1_4														
W																di0_run_resolution_4
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	di0_offset_value_4														
W																di0_offset_resolution_4
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DI0\_SW\_GEN0\_4 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di0_run_value_m1_4	DI0 counter #4 pre defined value This fields defines the counter #4 pre defines value. When the counter is auto reload mode (di0_cnt_auto_reload_4 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di0_step_repeat field.

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN0\_4 field descriptions (continued)**

Field	Description
18–16 di0_run_resolution_4	<p>DI0 counter #4 Run Resolution</p> <p>This field defines the trigger causing the counter to increment.</p> <p>000 Counter is disabled</p> <p>001 The counter is triggered by the same trigger that triggers the displays clock.</p> <p>010 The Counter is triggered by counter #1</p> <p>011 The Counter is triggered by counter #2</p> <p>100 The Counter is triggered by counter #3</p> <p>101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.</p> <p>—</p> <p>110 External VSYNC</p> <p>111 Counter is always on.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di0_offset_value_4	<p>DI0 counter #4 offset value</p> <p>The counter can start counting after a pre defined delay</p> <p>This field defines the amount of cycles that the counter will be delayed by</p>
di0_offset_resolution_4	<p>DI0 counter #4 offset Resolution</p> <p>This field defines the trigger causing the offset counter to increment</p> <p>000 Counter is disabled</p> <p>001 The counter is triggered by the same trigger that triggers the displays clock.</p> <p>010 The Counter is triggered by counter #1</p> <p>011 The Counter is triggered by counter #2</p> <p>100 The Counter is triggered by counter #3</p> <p>101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.</p> <p>—</p> <p>110 External VSYNC</p> <p>111 Counter is always on.</p>

### 37.5.200 DI0 Sync Wave Gen 5 Register 0 (IPUx\_DI0\_SW\_GEN0\_5)

Address: Base address + 4\_001Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	di0_run_value_m1_5														
W																di0_run_resolution_5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	di0_offset_value_5														
W																di0_offset_resolution_5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DI0\_SW\_GEN0\_5 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di0_run_value_m1_5	DI0 counter #5 pre defined value  This fields defines the counter #5 pre defines value. When the counter is auto reload mode (di0_cnt_auto_reload_5 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di0_step_repeat field.
18–16 di0_run_resolution_5	DI0 counter #5 Run Resolution  This field defines the trigger causing the counter to increment.  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 External VSYNC 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di0_offset_value_5	DI0 counter #5 offset value  The counter can start counting after a pre defined delay  This field defines the amount of cycles that the counter will be delayed by
di0_offset_resolution_5	DI0 counter #5 offset Resolution  This field defines the trigger causing the offset counter to increment  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 -The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 External VSYNC 111 Counter is always on.

### 37.5.201 DI0 Sync Wave Gen 6 Register 0 (IPUx\_DI0\_SW\_GEN0\_6)

Address: Base address + 4\_0020h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN0\_6 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di0_run_value_m1_6	DI0 counter #6 pre defined value This fields defines the counter #6 pre defines value. When the counter is auto reload mode (di0_cnt_auto_reload_6 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di0_step_repeat field.
18–16 di0_run_resolution_6	DI0 counter #6 Run Resolution This field defines the trigger causing the counter to increment. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 The Counter is triggered by counter #5 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di0_offset_value_6	DI0 counter #6 offset value The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by
di0_offset_resolution_6	DI0 counter #6 offset Resolution This field defines the trigger causing the offset counter to increment 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN0\_6 field descriptions (continued)**

Field	Description
	101 The Counter is triggered by counter #4
	110 The Counter is triggered by counter #5
	111 Counter is always on.

### 37.5.202 DI0 Sync Wave Gen 7 Register 0 (IPUx\_DI0\_SW\_GEN0\_7)

Address: Base address + 4\_0024h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DI0\_SW\_GEN0\_7 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di0_run_value_m1_7	DI0 counter #7 pre defined value This fields defines the counter #7 pre defines value. When the counter is auto reload mode (di0_cnt_auto_reload_7 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di0_step_repeat field.
18–16 di0_run_resolution_7	DI0 counter #1 Run Resolution This field defines the trigger causing the counter to increment. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 The Counter is triggered by counter #5 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di0_offset_value_7	DI0 counter #7 offset value The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN0\_7 field descriptions (continued)**

Field	Description																
di0_offset_resolution_1	<p>DI0 counter #7 offset Resolution</p> <p>This field defines the trigger causing the offset counter to increment</p> <table style="margin-left: 20px;"> <tr><td>000</td><td>Counter is disabled</td></tr> <tr><td>001</td><td>The counter is triggered by the same trigger that triggers the displays clock.</td></tr> <tr><td>010</td><td>The Counter is triggered by counter #1</td></tr> <tr><td>011</td><td>The Counter is triggered by counter #2</td></tr> <tr><td>100</td><td>The Counter is triggered by counter #3</td></tr> <tr><td>101</td><td>The Counter is triggered by counter #4</td></tr> <tr><td>110</td><td>The Counter is triggered by counter #5</td></tr> <tr><td>111</td><td>Counter is always on.</td></tr> </table>	000	Counter is disabled	001	The counter is triggered by the same trigger that triggers the displays clock.	010	The Counter is triggered by counter #1	011	The Counter is triggered by counter #2	100	The Counter is triggered by counter #3	101	The Counter is triggered by counter #4	110	The Counter is triggered by counter #5	111	Counter is always on.
000	Counter is disabled																
001	The counter is triggered by the same trigger that triggers the displays clock.																
010	The Counter is triggered by counter #1																
011	The Counter is triggered by counter #2																
100	The Counter is triggered by counter #3																
101	The Counter is triggered by counter #4																
110	The Counter is triggered by counter #5																
111	Counter is always on.																

### 37.5.203 DI0 Sync Wave Gen 8 Register 0 (IPUx\_DI0\_SW\_GEN0\_8)

Address: Base address + 4\_0028h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
	R	0															di0_run_resolution_8
	W																
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
	R	0															di0_offset_resolution_8
	W																
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DI0\_SW\_GEN0\_8 field descriptions**

Field	Description												
31 Reserved	This read-only field is reserved and always has the value 0.												
30–19 di0_run_value_m1_8	<p>DI0 counter #8 pre defined value</p> <p>This fields defines the counter #8 pre defines value. When the counter is auto reload mode (di0_cnt_auto_reload_8 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di0_step_repeat field.</p>												
18–16 di0_run_resolution_8	<p>DI0 counter #8 Run Resolution</p> <p>This field defines the trigger causing the counter to increment.</p> <table style="margin-left: 20px;"> <tr><td>000</td><td>Counter is disabled</td></tr> <tr><td>001</td><td>The counter is triggered by the same trigger that triggers the displays clock.</td></tr> <tr><td>010</td><td>The Counter is triggered by counter #1</td></tr> <tr><td>011</td><td>The Counter is triggered by counter #2</td></tr> <tr><td>100</td><td>The Counter is triggered by counter #3</td></tr> <tr><td>101</td><td>The Counter is triggered by counter #4</td></tr> </table>	000	Counter is disabled	001	The counter is triggered by the same trigger that triggers the displays clock.	010	The Counter is triggered by counter #1	011	The Counter is triggered by counter #2	100	The Counter is triggered by counter #3	101	The Counter is triggered by counter #4
000	Counter is disabled												
001	The counter is triggered by the same trigger that triggers the displays clock.												
010	The Counter is triggered by counter #1												
011	The Counter is triggered by counter #2												
100	The Counter is triggered by counter #3												
101	The Counter is triggered by counter #4												

*Table continues on the next page...*

**IPUx\_DI0\_SW\_GEN0\_8 field descriptions (continued)**

Field	Description
	110 The Counter is triggered by counter #5 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di0_offset_value_8	DI0 counter #8 offset value The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by
di0_offset_resolution_8	DI0 counter #8 offset Resolution This field defines the trigger causing the offset counter to increment 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 The Counter is triggered by counter #5 111 Counter is always on.

### 37.5.204 DI0 Sync Wave Gen 9 Register 0 (IPUx\_DI0\_SW\_GEN0\_9)

Address: Base address + 4\_002Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																di0_run_resolution_9
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																di0_offset_resolution_9
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DI0\_SW\_GEN0\_9 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di0_run_value_m1_9	DI0 counter #9 pre defined value This fields defines the counter #9 pre defines value. When the counter is auto reload mode (di0_cnt_auto_reload_9 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di0_step_repeat field.

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN0\_9 field descriptions (continued)**

Field	Description
18–16 di0_run_resolution_9	<p>DI0 counter #9 Run Resolution</p> <p>This field defines the trigger causing the counter to increment.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> <li>011 The Counter is triggered by counter #2</li> <li>100 The Counter is triggered by counter #3</li> <li>101 The Counter is triggered by counter #4</li> <li>110 The Counter is triggered by counter #5</li> <li>111 Counter is always on.</li> </ul>
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di0_offset_value_9	<p>DI0 counter #9 offset value</p> <p>The counter can start counting after a pre defined delay</p> <p>This field defines the amount of cycles that the counter will be delayed by</p>
di0_offset_resolution_9	<p>DI0 counter #9 offset Resolution</p> <p>This field defines the trigger causing the offset counter to increment</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> <li>011 The Counter is triggered by counter #2</li> <li>100 The Counter is triggered by counter #3</li> <li>101 The Counter is triggered by counter #4</li> <li>110 The Counter is triggered by counter #5</li> <li>111 Counter is always on.</li> </ul>

### 37.5.205 DI0 Sync Wave Gen 1 Register 1 (IPUx\_DI0\_SW\_GEN1\_1)

Address: Base address + 4\_0030h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di0_cnt_polarity_gen_en_1		di0_cnt_auto_reload_1		di0_cnt_clr_sel_1						di0_cnt_down_1				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0											di0_cnt_up_1				
W		di0_cnt_polarity_trigger_sel_1		di0_cnt_polarity_clr_sel_1												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN1\_1 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di0_cnt_polarity_gen_en_1	<p>DI0 Counter polarity generator enable</p> <p>The counter's output polarity can be changed on the fly.</p> <ul style="list-style-type: none"> <li>00 Dynamic polarity change is disabled</li> <li>01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2.</li> <li>10 Dynamic polarity change is enabled</li> <li>11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value</li> </ul>
28 di0_cnt_auto_reload_1	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di0_step_repeat_&lt;i&gt;i&lt;/i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di0_step_repeat_1 field</li> </ul>
27–25 di0_cnt_clr_sel_1	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 Reserved</li> </ul>

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN1\_1 field descriptions (continued)**

Field	Description
	<p>011 Reserved      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
24–16 di0_cnt_down_1	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di0_cnt_polarity_trigger_sel_1	<p>DI0 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 Reserved      011 Reserved      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
11–9 di0_cnt_polarity_clr_sel_1	<p>DI0 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Reserved      011 Reserved      100 Reserved      101 Reserved      110 Reserved      111 Reserved</p>
di0_cnt_up_1	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.206 DI0 Sync Wave Gen 2 Register 1 (IPUx\_DI0\_SW\_GEN1\_2)

Address: Base address + 4\_0034h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W				di0_cnt_polarity_gen_en_2		di0_cnt_auto_reload_2										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W				di0_cnt_polarity_trigger_sel_2		di0_cnt_polarity_clr_sel_2										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN1\_2 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di0_cnt_polarity_gen_en_2	<p>DI0 Counter polarity generator enable</p> <p>The counter's output polarity can be changed on the fly.</p> <ul style="list-style-type: none"> <li>00 Dynamic polarity change is disabled</li> <li>01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2.</li> <li>10 Dynamic polarity change is enabled</li> <li>11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value</li> </ul>
28 di0_cnt_auto_reload_2	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di0_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di0_step_repeat_&lt;i&gt; field</li> </ul>
27–25 di0_cnt_clr_sel_2	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> </ul>

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN1\_2 field descriptions (continued)**

Field	Description
	<p>011 Reserved      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
24–16 di0_cnt_down_2	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di0_cnt_polarity_trigger_sel_2	<p>DI0 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 Reserved      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
11–9 di0_cnt_polarity_clr_sel_2	<p>DI0 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Reserved      011 Reserved      100 Reserved      101 Reserved      110 Reserved      111 Reserved</p>
di0_cnt_up_2	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.207 DI0 Sync Wave Gen 3 Register 1 (IPUx\_DI0\_SW\_GEN1\_3)

Address: Base address + 4\_0038h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di0_cnt_polarity_gen_en_3		di0_cnt_auto_reload_3		di0_cnt_clr_sel_3						di0_cnt_down_3				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0											di0_cnt_up_3				
W		di0_cnt_polarity_trigger_sel_3		di0_cnt_polarity_clr_sel_3												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN1\_3 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di0_cnt_polarity_gen_en_3	<p>DI0 Counter polarity generator enable</p> <p>The counter's output polarity can be changed on the fly.</p> <ul style="list-style-type: none"> <li>00 Dynamic polarity change is disabled</li> <li>01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2.</li> <li>10 Dynamic polarity change is enabled</li> <li>11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value</li> </ul>
28 di0_cnt_auto_reload_3	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di0_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di0_step_repeat_&lt;i&gt; field</li> </ul>
27–25 di0_cnt_clr_sel_3	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> </ul>

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN1\_3 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
24–16 di0_cnt_down_3	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di0_cnt_polarity_trigger_sel_3	<p>DI0 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
11–9 di0_cnt_polarity_clr_sel_3	<p>DI0 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Reserved      101 Reserved      110 Reserved      111 Reserved</p>
di0_cnt_up_3	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.208 DI0 Sync Wave Gen 4 Register 1 (IPUx\_DI0\_SW\_GEN1\_4)

Address: Base address + 4\_003Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di0_cnt_polarity_gen_en_4		di0_cnt_auto_reload_4		di0_cnt_clr_sel_4						di0_cnt_down_4				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0											di0_cnt_up_4				
W		di0_cnt_polarity_trigger_sel_4		di0_cnt_polarity_clr_sel_4												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN1\_4 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di0_cnt_polarity_gen_en_4	<p>DI0 Counter polarity generator enable</p> <p>The counter's output polarity can be changed on the fly.</p> <ul style="list-style-type: none"> <li>00 Dynamic polarity change is disabled</li> <li>01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2.</li> <li>10 Dynamic polarity change is enabled</li> <li>11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value</li> </ul>
28 di0_cnt_auto_reload_4	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di0_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di0_step_repeat_&lt;i&gt; field</li> </ul>
27–25 di0_cnt_clr_sel_4	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> </ul>

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN1\_4 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
24–16 di0_cnt_down_4	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di0_cnt_polarity_trigger_sel_4	<p>DI0 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
11–9 di0_cnt_polarity_clr_sel_4	<p>DI0 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Reserved      110 Reserved      111 Reserved</p>
di0_cnt_up_4	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.209 DI0 Sync Wave Gen 5 Register 1 (IPUx\_DI0\_SW\_GEN1\_5)

Address: Base address + 4\_0040h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W				di0_cnt_polarity_gen_en_5		di0_cnt_auto_reload_5										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W				di0_cnt_polarity_trigger_sel_5		di0_cnt_polarity_clr_sel_5										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN1\_5 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di0_cnt_polarity_gen_en_5	<p>DI0 Counter polarity generator enable</p> <p>The counter's output polarity can be changed on the fly.</p> <ul style="list-style-type: none"> <li>00 Dynamic polarity change is disabled</li> <li>01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2.</li> <li>10 Dynamic polarity change is enabled</li> <li>11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value</li> </ul>
28 di0_cnt_auto_reload_5	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di0_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di0_step_repeat_&lt;i&gt; field</li> </ul>
27–25 di0_cnt_clr_sel_5	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> </ul>

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN1\_5 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 External VSYNC      111 Counter is always on.</p>
24–16 di0_cnt_down_5	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di0_cnt_polarity_trigger_sel_5	<p>DI0 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 External VSYNC      111 Counter is always on.</p>
11–9 di0_cnt_polarity_clr_sel_5	<p>DI0 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Output is inverted if the output of counter #4 is set      110 Reserved      111 Reserved</p>
di0_cnt_up_5	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.210 DI0 Sync Wave Gen 6 Register 1 (IPUx\_DI0\_SW\_GEN1\_6)

Address: Base address + 4\_0044h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di0_cnt_polarity_gen_en_6		di0_cnt_auto_reload_6		di0_cnt_clr_sel_6							di0_cnt_down_6			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												di0_cnt_up_6			
W		di0_cnt_polarity_trigger_sel_6		di0_cnt_polarity_clr_sel_6												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN1\_6 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di0_cnt_polarity_gen_en_6	<p>DI0 Counter polarity generator enable</p> <p>The counter's output polarity can be changed on the fly.</p> <ul style="list-style-type: none"> <li>00 Dynamic polarity change is disabled</li> <li>01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2.</li> <li>10 Dynamic polarity change is enabled</li> <li>11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value</li> </ul>
28 di0_cnt_auto_reload_6	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di0_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di0_step_repeat_&lt;i&gt; field</li> </ul>
27–25 di0_cnt_clr_sel_6	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> </ul>

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN1\_6 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
24–16 di0_cnt_down_6	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di0_cnt_polarity_trigger_sel_6	<p>DI0 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
11–9 di0_cnt_polarity_clr_sel_6	<p>DI0 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Output is inverted if the output of counter #4 is set      110 Output is inverted if the output of counter #5 is set      111 Reserved</p>
di0_cnt_up_6	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.211 DI0 Sync Wave Gen 7 Register 1 (IPUx\_DI0\_SW\_GEN1\_7)

Address: Base address + 4\_0048h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W				di0_cnt_polarity_gen_en_7		di0_cnt_auto_reload_7		di0_cnt_clr_sel_7					di0_cnt_down_7			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												di0_cnt_up_7			
W				di0_cnt_polarity_trigger_sel_7		di0_cnt_polarity_clr_sel_7										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN1\_7 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di0_cnt_polarity_gen_en_7	DI0 Counter polarity generator enable The counter's output polarity can be changed on the fly. 00 Dynamic polarity change is disabled 01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2. 10 Dynamic polarity change is enabled 11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value
28 di0_cnt_auto_reload_7	Counter auto reload mode 1 The counter will automatically be reloaded forever, ignoring the value of the di0_step_repeat_<i> field 0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di0_step_repeat_<i> field
27–25 di0_cnt_clr_sel_7	Counter Clear select This field defines the source of the signals that clears the counter. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN1\_7 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
24–16 di0_cnt_down_7	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di0_cnt_polarity_trigger_sel_7	<p>DI0 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
11–9 di0_cnt_polarity_clr_sel_7	<p>DI0 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Output is inverted if the output of counter #4 is set      110 Output is inverted if the output of counter #5 is set      111 Output is inverted if the output of counter #6 is set</p>
di0_cnt_up_7	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.212 DI0 Sync Wave Gen 8 Register 1 (IPUx\_DI0\_SW\_GEN1\_8)

Address: Base address + 4\_004Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W				di0_cnt_polarity_gen_en_8		di0_cnt_auto_reload_8										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W				di0_cnt_polarity_trigger_sel_8		di0_cnt_polarity_clr_sel_8										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN1\_8 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di0_cnt_polarity_gen_en_8	<p>DI0 Counter polarity generator enable</p> <p>The counter's output polarity can be changed on the fly.</p> <ul style="list-style-type: none"> <li>00 Dynamic polarity change is disabled</li> <li>01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2.</li> <li>10 Dynamic polarity change is enabled</li> <li>11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value</li> </ul>
28 di0_cnt_auto_reload_8	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di0_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di0_step_repeat_&lt;i&gt; field</li> </ul>
27–25 di0_cnt_clr_sel_8	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> </ul>

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN1\_8 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
24–16 di0_cnt_down_8	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di0_cnt_polarity_trigger_sel_8	<p>DI0 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
11–9 di0_cnt_polarity_clr_sel_8	<p>DI0 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Output is inverted if the output of counter #4 is set      110 Output is inverted if the output of counter #5 is set      111 Output is inverted if the output of counter #6 is set</p>
di0_cnt_up_8	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.213 DI0 Sync Wave Gen 9 Register 1 (IPUx\_DI0\_SW\_GEN1\_9)

Address: Base address + 4\_0050h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
	di0_gentime_sel_9			di0_cnt_auto_reload_9		di0_cnt_clr_sel_9							di0_cnt_down_9			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	di0_tag_sel_9			0									di0_cnt_up_9			
W	di0_tag_sel_9															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SW\_GEN1\_9 field descriptions

Field	Description
31–29 di0_gentime_sel_9	<p>Counter #9 main waveform select</p> <p>This field defines the counter that counter #9's auxiliary waveform will be attached too.</p> <ul style="list-style-type: none"> <li>000 Counter #9's waveform is attached to counter #1's waveform</li> <li>001 Counter #9's waveform is attached to counter #2's waveform</li> <li>010 Counter #9's waveform is attached to counter #3's waveform</li> <li>011 Counter #9's waveform is attached to counter #4's waveform</li> <li>100 Counter #9's waveform is attached to counter #5's waveform</li> <li>101 Counter #9's waveform is attached to counter #6's waveform</li> <li>110 Counter #9's waveform is attached to counter #7's waveform</li> <li>111 Counter #9's waveform is attached to counter #8's waveform</li> </ul>
28 di0_cnt_auto_reload_9	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di0_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di0_step_repeat_&lt;i&gt; field</li> </ul>
27–25 di0_cnt_clr_sel_9	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> </ul>

Table continues on the next page...

**IPUx\_DI0\_SW\_GEN1\_9 field descriptions (continued)**

Field	Description
	011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 The Counter is triggered by counter #5 111 Counter is always on.
24–16 di0_cnt_down_9	Counter falling edge position This parameter contains an integer part (bits 24:17) and a fractional part (bit 16). The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.
15 di0_tag_sel_9	Counter #9 can send a synchronous tag when counter #9 reaches its predefined value or when it's triggering counter reaches its pre defined value. 1 tag source is counter #9 0 Tag's source is the triggering counter.
14–9 Reserved	This read-only field is reserved and always has the value 0.
di0_cnt_up_9	Counter rising edge position This parameter contains an integer part (bits 24:17) and a fractional part (bit 16). The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.

### 37.5.214 DI0 Sync Assistance Gen Register (IPUx\_DI0\_SYNC\_AS\_GEN)

Address: Base address + 4\_0054h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R				0										0		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0												
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DI0\_SYNC\_AS\_GEN field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28 di0_sync_start_en	di0_sync_start_en
27–16 Reserved	This read-only field is reserved and always has the value 0.
15–13 di0_vsync_sel	VSYNC select This field defines which of the counters functions as VSYNC signal 000 VSYNC is coming from counter #1 001 VSYNC is coming from counter #2 111 VSYNC is coming from counter #8
12 Reserved	This read-only field is reserved and always has the value 0.
di0_sync_start	DI0 Sync start This field defines the number of low (including blanking rows) on the which the DI0 starts preparing the data for the next frame.

**37.5.215 DI0 Data Wave Gen <i> Register (IPUx\_DI0\_DW\_GEN\_i)**

The DI0\_DW\_GEN\_<i> register holds pointers for the waveform generators.

These registers have different bit arrangements for parallel and serial display. When using a parallel display [VDI Plane Size Register 4](#) is applicable. When using a serial interface [VDI Plane Size Register 4](#) is applicable.

**Table 37-667. Register Field Descriptions for Serial Display**

Field	Description
31–24 di0_serial_period_<i>	DI0 Serial Period <i> This field defines the period of the time base serial display clock. The units are the internal DI clock
23–16 di0_start_period_<i>	DI0 start period This field defines the amount of cycles between the point where the access is ready to be launched to the actual point where the time base serial display clock restarts. The units are the internal DI clock
15–14 di0_cst_<i>	DI0 Chip Select pointer for waveform <i> This field points to a register that defines the waveform of the CS pin. For serial displays the down value as defined on DI0_DW_SET*_<i> is measured from the assertion of the last serial display time base clock. 00 The waveform is defined according to the settings on DI0_DW_SET0_<i> 01 The waveform is defined according to the settings on DI0_DW_SET1_<i>

*Table continues on the next page...*

**Table 37-667. Register Field Descriptions for Serial Display (continued)**

Field	Description
	10 The waveform is defined according to the settings on DI0_DW_SET2_<i> 11 The waveform is defined according to the settings on DI0_DW_SET3_<i>
13-9	Reserved
8-4 di0_serial_valid_bits<i>	DI0 Serial valid bits. This field defines the amount of valid bits to be transmitted within the 32 bits internal word aligned to bit[0]. The actual amount of valid bits is di0_serial_valid_bits_<i> + 1
3-2 di0_serial_rs_<i>	DI0 Serial RS This field points to a register that defines the waveform of the RS pin. For serial displays the down value as defined on DI0_DW_SET*_<i> is measured from the assertion of the last serial display time base clock. 00 The waveform is defined according to the settings on DI0_DW_SET0_<i> 01 The waveform is defined according to the settings on DI0_DW_SET1_<i> 10 The waveform is defined according to the settings on DI0_DW_SET2_<i> 11 The waveform is defined according to the settings on DI0_DW_SET3_<i>
1-0 di0_serial_clk_<i>	DI0 serial clock<i> This field points to a register that defines the waveform of the Serial clock pin. 00 The waveform is defined according to the settings on DI0_DW_SET0_<i> 01 The waveform is defined according to the settings on DI0_DW_SET1_<i> 10 The waveform is defined according to the settings on DI0_DW_SET2_<i> 11 The waveform is defined according to the settings on DI0_DW_SET3_<i>

Address: Base address + 4\_0058h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																	di0_cst_i	di0_pt_6_i	di0_pt_5_i	di0_pt_4_i	di0_pt_3_i	di0_pt_2_i	di0_pt_1_i	di0_pt_0_i										
W	di0_access_size_i		di0_componnent_size_i																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

**IPUx\_DI0\_DW\_GEN\_i field descriptions**

Field	Description
31-24 di0_access_size_i	DI0 Access Size <i> This field defines the amount of IPU cycles between any 2 accesses (an access may be a pixel or generic data that may have more than one component)
23-16 di0_componnent_size_i	DI0 component Size This field defines the amount of IPU cycles between any 2 components
15-14 di0_cst_i	DI0 Chip Select pointer for waveform <i> This field points to a register that defines the waveform of the CS pin. The CS is automatically mapped to a specific display

Table continues on the next page...

**IPUx\_DIO\_DW\_GEN\_i field descriptions (continued)**

Field	Description
	<p>00 The waveform is defined according to the settings on DIO_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DIO_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DIO_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DIO_DW_SET3_&lt;i&gt;</p>
13–12 di0_pt_6_i	<p>DIO PIN_17 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_17 pin.</p> <p>00 The waveform is defined according to the settings on DIO_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DIO_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DIO_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DIO_DW_SET3_&lt;i&gt;</p>
11–10 di0_pt_5_i	<p>DIO PIN_16 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_16 pin.</p> <p>00 The waveform is defined according to the settings on DIO_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DIO_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DIO_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DIO_DW_SET3_&lt;i&gt;</p>
9–8 di0_pt_4_i	<p>DIO PIN_15 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_15 pin.</p> <p>00 The waveform is defined according to the settings on DIO_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DIO_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DIO_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DIO_DW_SET3_&lt;i&gt;</p>
7–6 di0_pt_3_i	<p>DIO PIN_14 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_14 pin.</p> <p>00 The waveform is defined according to the settings on DIO_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DIO_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DIO_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DIO_DW_SET3_&lt;i&gt;</p>
5–4 di0_pt_2_i	<p>DIO PIN_13 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_13 pin.</p> <p>00 The waveform is defined according to the settings on DIO_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DIO_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DIO_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DIO_DW_SET3_&lt;i&gt;</p>
3–2 di0_pt_1_i	<p>DIO PIN_12 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_12 pin.</p> <p>00 The waveform is defined according to the settings on DIO_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DIO_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DIO_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DIO_DW_SET3_&lt;i&gt;</p>

*Table continues on the next page...*

**IPUx\_DI0\_DW\_GEN\_i field descriptions (continued)**

Field	Description
di0_pt_0_i	<p>DI0 PIN_11 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_11 pin.</p> <p>00 The waveform is defined according to the settings on DI0_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DI0_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DI0_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DI0_DW_SET3_&lt;i&gt;</p>

**37.5.216 DI0 Data Wave Set 0 <i> Register  
(IPUx\_DI0\_DW\_SET0\_i)**

Address: Base address + 4\_0088h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DI0\_DW\_SET0\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di0_data_cnt_down0_i	<p>Waveform's falling edge position.</p> <p>This field defines the Waveform's falling edge position. The Waveform is mapped to a point according to the corresponding di0_pt_*_&lt;i&gt;</p>
15–9 Reserved	This read-only field is reserved and always has the value 0.
di0_data_cnt_up0_i	<p>Waveform's rising edge position.</p> <p>This field defines the Waveform's rising edge position. The Waveform is mapped to a point according to the corresponding di0_pt_*_&lt;i&gt;</p>

**37.5.217 DI0 Data Wave Set 1 <i> Register  
(IPUx\_DI0\_DW\_SET1\_i)**

Address: Base address + 4\_00B8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DI0\_DW\_SET1\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di0_data_cnt_ down1_i	Waveform's falling edge position. This field defines the Waveform's falling edge position. The Waveform is mapped to a pint according to the corresponding di0_pt_*_<i>
15–9 Reserved	This read-only field is reserved and always has the value 0.
di0_data_cnt_ up1_i	Waveform's rising edge position. This field defines the Waveform's rising edge position. The Waveform is mapped to a pint according to the corresponding di0_pt_*_<i>

**37.5.218 DI0 Data Wave Set 2 <i> Register  
(IPUx\_DI0\_DW\_SET2\_i)**

Address: Base address + 4\_00E8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DI0\_DW\_SET2\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di0_data_cnt_ down2_i	Waveform's falling edge position. This field defines the Waveform's falling edge position. The Waveform is mapped to a pint according to the corresponding di0_pt_*_<i>
15–9 Reserved	This read-only field is reserved and always has the value 0.
di0_data_cnt_ up2_i	Waveform's rising edge position. This field defines the Waveform's rising edge position. The Waveform is mapped to a pint according to the corresponding di0_pt_*_<i>

### 37.5.219 DI0 Data Wave Set 3 <i> Register (IPUx\_DI0\_DW\_SET3\_i)

Address: Base address + 4\_0118h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

#### IPUx\_DI0\_DW\_SET3\_i field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di0_data_cnt_down3_i	Waveform's falling edge position. This field defines the Waveform's falling edge position. The Waveform is mapped to a pint according to the corresponding di0_pt_*_<i>
15–9 Reserved	This read-only field is reserved and always has the value 0.
di0_data_cnt_up3_i	Waveform's rising edge position. This field defines the Waveform's rising edge position. The Waveform is mapped to a pint according to the corresponding di0_pt_*_<i>

### 37.5.220 DI0 Step Repeat <i> Registers (IPUx\_DI0\_STP\_REP\_i)

Address: Base address + 4\_0148h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

#### IPUx\_DI0\_STP\_REP\_i field descriptions

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 di0_step_repeat_2i	Step Repeat <i> This fields defines the amount of repetitions that will be performed by the counter <i>
15–12 Reserved	This read-only field is reserved and always has the value 0.
di0_step_repeat_2i_minus_1	Step Repeat <i> This fields defines the amount of repetitions that will be performed by the counter <i>

### 37.5.221 DI0 Step Repeat 9 Registers (IPUx\_DI0\_STP\_REPEAT\_9)

Address: Base address + 4\_0158h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0																	
W																																		

Reset 0

#### IPUx\_DI0\_STP\_REPEAT\_9 field descriptions

Field	Description
31–12 Reserved	This read-only field is reserved and always has the value 0.
di0_step_repeat_9	Step Repeat 9 This fields defines the amount of repetitions that will be performed by the counter 9

### 37.5.222 DI0 Serial Display Control Register (IPUx\_DI0\_SER\_CONF)

Address: Base address + 4\_015Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16																
R																																	
W																																	

Reset 0

Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0																	
R																																		
W																																		

Reset 0

**IPUx\_DIO\_SER\_CONF field descriptions**

Field	Description
31–28 DIO_SERIAL_LLA_PNTR_RS_R_1	RS 3 waveform pointer for read low level access  This pointer defines which waveform set will be chosen when the read low level access is targeted to RS group 1.  0000 Waveform set #1 0001 Waveform set #2 1011 Waveform set #12 1100 Reserved 1101 Reserved 1100 Reserved
27–24 DIO_SERIAL_LLA_PNTR_RS_R_0	RS 2 waveform pointer for read low level access  This pointer defines which waveform set will be chosen when the read low level access is targeted to RS group 0.  0000 Waveform set #1 0001 Waveform set #2 1011 Waveform set #12 1100 Reserved 1101 Reserved 1100 Reserved
23–20 DIO_SERIAL_LLA_PNTR_RS_W_1	RS 1 waveform pointer for write low level access  This pointer defines which waveform set will be chosen when the low level write access is targeted to RS group 1.  0000 Waveform set #1 0001 Waveform set #2 1011 Waveform set #12 1100 Reserved 1101 Reserved 1100 Reserved
19–16 DIO_SERIAL_LLA_PNTR_RS_W_0	RS 0 waveform pointer for write low level access  This pointer defines which waveform set will be chosen when the low level write access is targeted to RS group 0.  0000 Waveform set #1 0001 Waveform set #2 1011 Waveform set #12 1100 Reserved 1101 Reserved 1100 Reserved
15–8 DIO_SERIAL_LATCH	DIO Serial Latch  This field defines how many cycles to insert between serial read accesses start to data sampling in the
7–6 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**IPUx\_DIO\_SER\_CONF field descriptions (continued)**

Field	Description
5 DIO_LLA_SER_ACCESS	<p>Direct Low Level Access to Serial display</p> <p>1 ARM platform access is performed via a direct path to the serial display in LLA mode, in this mode only the ARM platform in LLA mode can access the serial port</p> <p>0 ARM platform access to the serial display port is not done directly, hence other source are allowed to access the serial port. The arbitration is done automatically</p>
4 DIO_SER_CLK_POLARITY	<p>Serial Clock Polarity</p> <p>The output polarity of the SER_CLK pin</p> <p>1 The clock is inverted</p> <p>0 The clock is not inverted</p>
3 DIO_SERIAL_DATA_POLARITY	<p>Serial Data Polarity</p> <p>The output polarity of the SER_DATA pin</p> <p>1 The data is inverted</p> <p>0 The data is not inverted</p>
2 DIO_SERIAL_RS_POLARITY	<p>Serial RS Polarity</p> <p>The output polarity of the SER_RS pin</p> <p>1 The RS is inverted</p> <p>0 The RS is not inverted</p>
1 DIO_SERIAL_CS_POLARITY	<p>Serial Chip Select Polarity</p> <p>The output polarity of the SER_CS pin</p> <p>1 The CS is inverted</p> <p>0 The CS is not inverted</p>
0 DIO_WAIT4SERIAL	<p>Wait for Serial</p> <p>When the parallel display share pins with the serial port. Accessing the parallel port is not allowed till the serial port completes its access.</p> <p>1 The parallel port should wait to the serial port as the pins are shared</p> <p>0 The parallel port should not wait to the serial port as the pins are not shared</p>

### 37.5.223 DI0 Special Signals Control Register (IPUx\_DI0\_SSC)

Address: Base address + 4\_0160h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									DIO_PIN17_ERM	DIO_PIN16_ERM	DIO_PIN15_ERM	DIO_PIN14_ERM	DIO_PIN13_ERM	DIO_PIN12_ERM	DIO_PIN11_ERM	DIO_CS_ERM
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									DIO_WAIT_ON		0		DIO_BYTE_EN_RD_IN		DIO_BYTE_EN_PNTR	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI0\_SSC field descriptions

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23 DIO_PIN17_ERM	DIO PIN17 error recovery mode. This bit defines the error recovery mode of the PIN17 pin. 1 The PIN17 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC 0 Nothing is done to the PIN17 pin following a display error detection
22 DIO_PIN16_ERM	DIO PIN16 error recovery mode. This bit defines the error recovery mode of the PIN16 pin. 1 The PIN16 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC 0 Nothing is done to the PIN16 pin following a display error detection
21 DIO_PIN15_ERM	DIO PIN15 error recovery mode. This bit defines the error recovery mode of the PIN15 pin. 1 The PIN15 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC 0 Nothing is done to the PIN15 pin following a display error detection
20 DIO_PIN14_ERM	DIO PIN14 error recovery mode. This bit defines the error recovery mode of the PIN14 pin.

Table continues on the next page...

**IPUx\_DIO\_SSC field descriptions (continued)**

Field	Description
	<p>1 The PIN14 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC 0 Nothing is done to the PIN14 pin following a display error detection</p>
19 DIO_PIN13_ERM	<p>DIO PIN13 error recovery mode. This bit defines the error recovery mode of the PIN13 pin.</p> <p>1 The PIN13 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC 0 Nothing is done to the PIN13 pin following a display error detection</p>
18 DIO_PIN12_ERM	<p>DIO PIN12 error recovery mode. This bit defines the error recovery mode of the PIN12 pin.</p> <p>1 The PIN12 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC 0 Nothing is done to the PIN12 pin following a display error detection</p>
17 DIO_PIN11_ERM	<p>DIO PIN11 error recovery mode. This bit defines the error recovery mode of the PIN11 pin.</p> <p>1 The PIN11 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC 0 Nothing is done to the PIN11 pin following a display error detection</p>
16 DIO_CS_ERM	<p>DIO GLUELOGIC error recovery mode. This bit defines the error recovery mode of the GLUELOGIC.</p> <p>1 The GLUELOGIC is release in case of a synchronous display error. The release will be done on the next VSYNC 0 Nothing is done to the GLUELOGIC following a display error detection</p>
15–6 Reserved	This read-only field is reserved and always has the value 0.
5 DIO_WAIT_ON	<p>Wait On This field defines the DC's response to WAIT signal</p> <p>1 The DC holds the flow as long as WAIT is asserted 0 The DC continues the flow regardless the WAIT signal</p>
4 Reserved	This read-only field is reserved and always has the value 0.
3 DIO_BYTE_EN_ RD_IN	<p>Byte Enable Read In This bit selects the source of the byte enable pins</p> <p>1 The write byte enable signals are routed via bits [17:16] of the display's data, The read byte enable signals are routed via bits [19:18 of the display's data 0 The byte enable signals are routed via bits [17:16] of the display's data for both read and write</p>
DIO_BYTE_EN_ PNTR	<p>Byte Enable Pointer This pointer selects the pin asserted along with the byte enables signals</p> <p>000 wave form of byte enable as pin_11</p>

*Table continues on the next page...*

**IPUx\_DIO\_SSC field descriptions (continued)**

Field	Description
	001 wave form of byte enable as pin_12 111 wave form of byte enable as suitable CS pin

**37.5.224 DI0 Polarity Register (IPUx\_DIO\_POL)**

Address: Base address + 4\_0164h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R						0										
W							DIO_WAIT_POLARITY	DIO_CS1_BYTE_EN_POLARITY	DIO_CS0_BYTE_EN_POLARITY	DIO_CS1_DATA_POLARITY						di0_cs1_polarity
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DIO_CS0_DATA_POLARITY								DIO_DRDY_DATA_POLARITY							di0_drdy_polarity
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DIO\_POL field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26 DIO_WAIT_POLARITY	WAIT polarity This bit defines the polarity of the wait signal input coming from the display 1 active high 0 active low
25 DIO_CS1_BYTE_EN_POLARITY	Byte Enable associated with CS1 polarity This bit defines the polarity of the byte enable signals to the display 1 active high 0 active low
24 DIO_CS0_BYTE_EN_POLARITY	Byte Enable associated with CS0 polarity This bit defines the polarity of the byte enable signals to the display

*Table continues on the next page...*

**IPUx\_DI0\_POL field descriptions (continued)**

Field	Description
	1 active high 0 active low
23 DI0_CS1_DATA_ POLARITY	Data Polarity associated with CS1
22–16 di0_cs1_polarity	DI0 output pin's polarity for CS1 This bits define the polarity of each of the DI's outputs when CS1 is asserted 1 The output pin is active high 0 The output pin is active low
15 DI0_CS0_DATA_ POLARITY	Data Polarity associated with CS0
14–8 di0_cs0_polarity	DI0 output pin's polarity for CS1 This bits define the polarity of each of the DI's outputs when CS1 is asserted 1 The output pin is active high 0 The output pin is active low
7 DI0_DRDY_ DATA_ POLARITY	Data Polarity associated with DRDY
di0_drdy_polarity	DI0 output dynamic pin's polarity for synchronous access This bits define the polarity of each of the DI's outputs when synchronous display access is asserted The pins' default polarity is the same as defined in the di0_drdy_polarity bits 1 The output pin is active high 0 The output pin is active low

**37.5.225 DI0 Active Window 0 Register (IPUx\_DI0\_AW0)**

Address: Base address + 4\_0168h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DI0_AW_ TRIG_SEL				DI0_AW_HEND								DI0_AW_ HCOUNT_ SEL				DI0_AW_HSTART															
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DI0\_AW0 field descriptions**

Field	Description
31–28 DI0_AW_TRIG_ SEL	This field selects the trigger for sending data during the display's active window 000 disabled 001 The trigger is the same trigger that triggers the displays clock. 010 The trigger is counter #1

*Table continues on the next page...*

**IPUx\_DIO\_AW0 field descriptions (continued)**

Field	Description
	011 The trigger is counter #2 100 The trigger is counter #3 101 The trigger is counter #4 110 The trigger is counter #5 111 The trigger is always on.
27–16 DIO_AW_HEND	This field defines the horizontal end of the active window
15–12 DIO_AW_ HCOUNT_SEL	GM: This field selects the counter that counts the horizontal position of the display's active window 0000 disabled 0001 reserved 0010 The counter is counter #1 0011 The counter is counter #2 0100 The counter is counter #3 0101 The counter is counter #4 0110 The counter is counter #5 1001 The counter is counter #8
DIO_AW_ HSTART	This field defines the horizontal start of the active window DIO_AW_HSTART < DIO_AW_HEND

**37.5.226 DIO Active Window 1 Register (IPUx\_DIO\_AW1)**

Address: Base address + 4\_016Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	0																DIO_AW_ VCOUNT_ SEL																
W																																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DIO\_AW1 field descriptions**

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 DIO_AW_VEND	This field defines the vertical end of the active window
15–12 DIO_AW_ VCOUNT_SEL	This field selects the counter that counts the vertical position of the display's active window 0000 disabled 0001 reserved 0010 The counter is counter #1 0011 The counter is counter #2 0100 The counter is counter #3 0101 The counter is counter #4

*Table continues on the next page...*

**IPUx\_DI0\_AW1 field descriptions (continued)**

Field	Description
	0110 The counter is counter #5 1001 The counter is counter #8
DIO_AW_VSTART	This field defines the vertical start of the active window DIO_AW_VSTART < DIO_AW_VEND

### 37.5.227 DI0 Screen Configuration Register (IPUx\_DI0\_SCR\_CONF)

Address: Base address + 4\_0170h offset

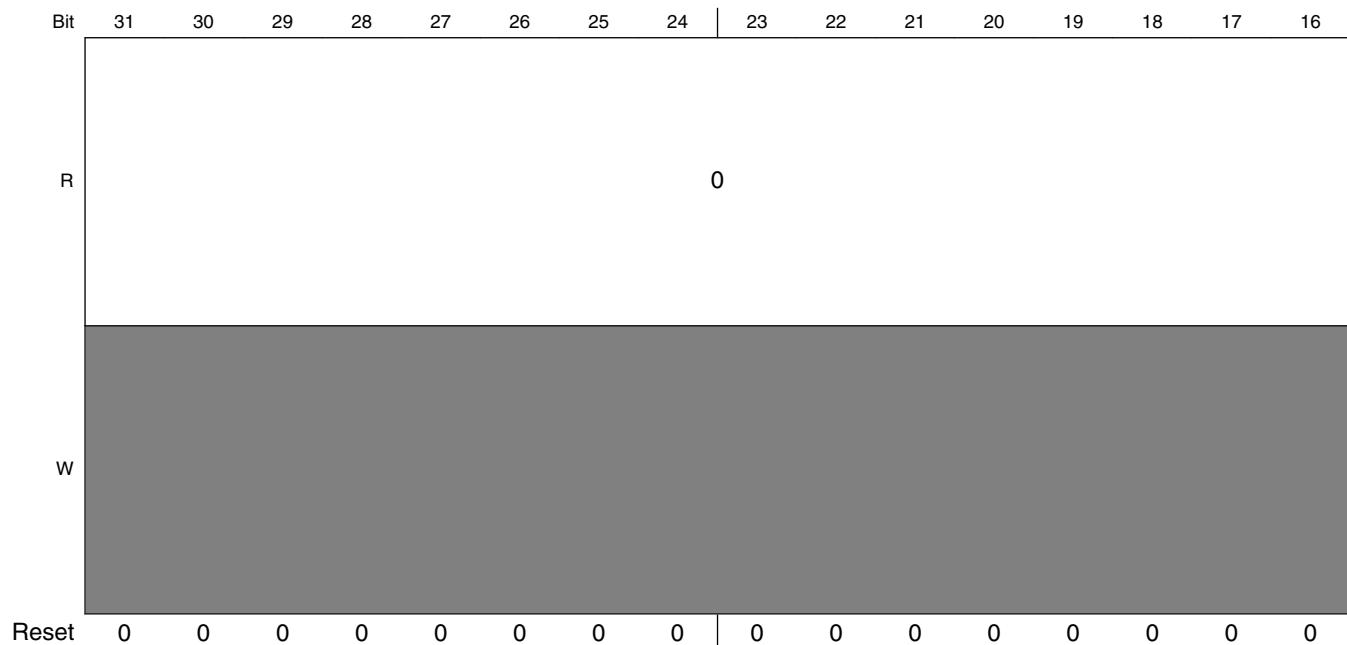
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																	0																	
W																																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

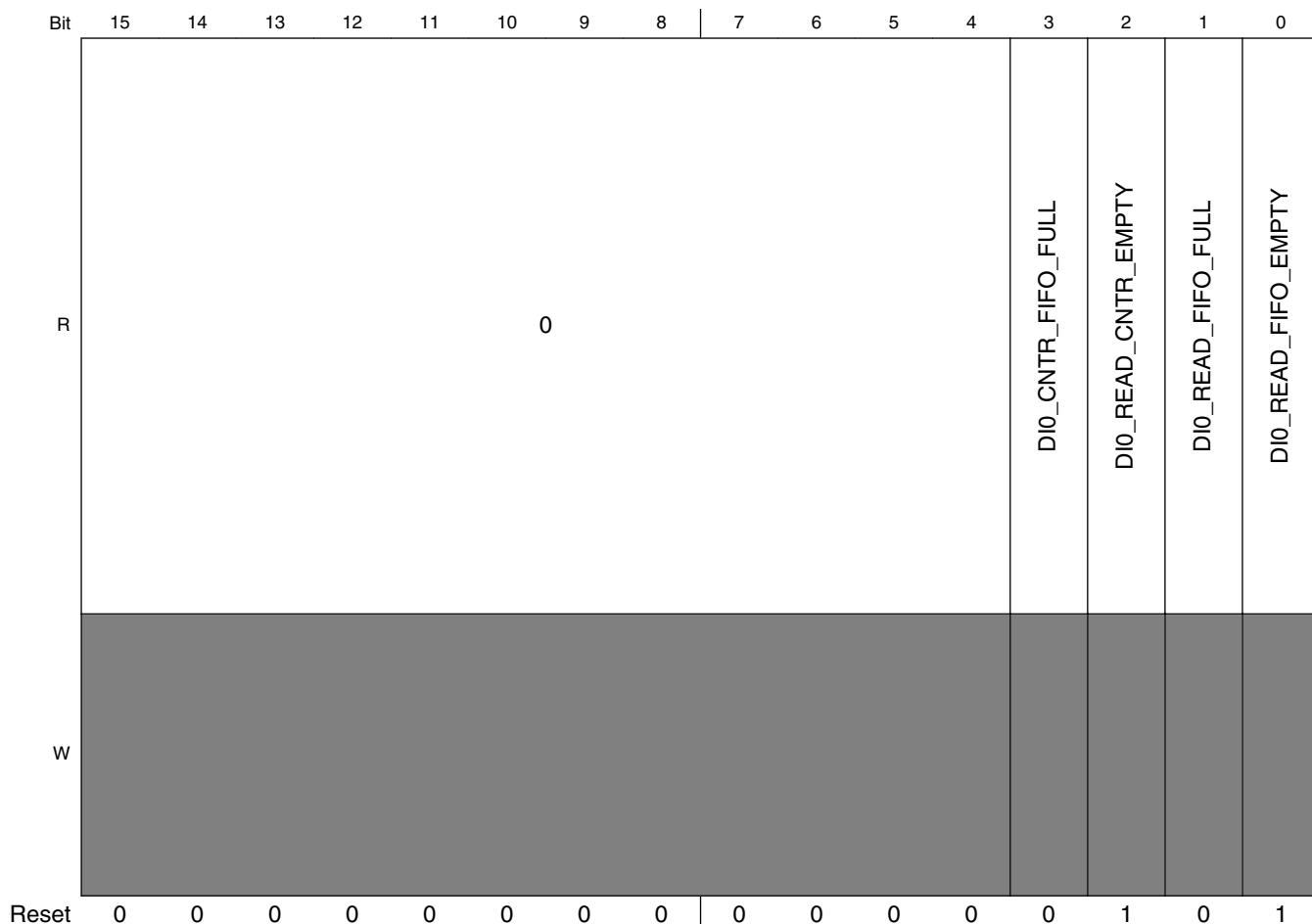
**IPUx\_DI0\_SCR\_CONF field descriptions**

Field	Description
31–12 Reserved	This read-only field is reserved and always has the value 0.
DIO_SCREEN_HEIGHT	This field defines the number of display rows (Number_of_ROWS = DIO_SCREEN_HEIGHT+1) This field is used for VSYNC calculation and for anti-tearing

### 37.5.228 DI0 Status Register (IPUx\_DI0\_STAT)

Address: Base address + 4\_0174h offset



**IPUx\_DIO\_STAT field descriptions**

Field	Description
31–4 Reserved	This read-only field is reserved and always has the value 0.
3 DIO_CNTR_ FIFO_FULL	This bit indicates a full state of the DIO FIFO. This FIFO is part of the DIO synchronizer.
2 DIO_READ_ CNTR_EMPTY	This bit indicates an empty state of the DIO FIFO. This FIFO is part of the DIO synchronizer.
1 DIO_READ_ FIFO_FULL	This bit indicates a full state of the DIO FIFO when performing a read. This FIFO is part of the DIO synchronizer.
0 DIO_READ_ FIFO_EMPTY	This bit indicates an empty state of the DIO FIFO when performing a read. This FIFO is part of the DIO synchronizer.

### 37.5.229 DI1General Register (IPUx\_DI1\_GENERAL)

Address: Base address + 4\_8000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	di1_pin8_pin15_sel		di1_disp_y_sel		DI1_CLOCK_STOP_MODE				DI1_DISP_CLOCK_INIT	di1_mask_sel	di1_vsync_ext	di1_clk_ext	DI1_WATCHDOG_MODE	di1_polarity_disp_clk	0	
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		di1_sync_count_sel		di1_err_treatment	di1_errm_vsync_sel	di1_polarity_cs1	di1_polarity_cs0									di1_polarity_i_1
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_GENERAL field descriptions

Field	Description
31 di1_pin8_pin15_sel	This bit routes PIN8 over PIN15  1 PIN8 is routed to PIN15, PIN8 is also routed to PIN15 0 PIN15 is routed to PIN15, PIN8 is routed to PIN8
30–28 di1_disp_y_sel	DI1 Display Vertical coordinate (Y) select.  This field defines which one of the 8 counters will be used as a display's line counter.  000 counter #1 is selected 111 counter #8 is selected
27–24 DI1_CLOCK_STOP_MODE	DI clock stop mode  When performing a clock change. The DI stops the clock to the display.  These field defines when the clock will be stopped  Stopping at EOL/EOF is supported for the case where the data is coming from the IDMAC (DMA access). In case that only direct accesses is performed, the user should set this field to 0000  0001-1001 stop at the next event of one of the counters (counter #1 to counter #9)  0000 stop at the next edge of the display clock 1100 stop at EOL (end of a line), but if stop request is during blanking interval, stop now 1101 stop at EOF (end of a frame), but if stop request is during blanking interval, stop now 1110 stop at EOL (end of a line), but if stop request is during blanking interval, stop at the end of the next line 1111 stop at EOF (end of a frame), but if stop request is during blanking interval, stop at the end of the next frame

Table continues on the next page...

**IPUx\_DI1\_GENERAL field descriptions (continued)**

Field	Description
23 DI1_DISP_CLOCK_INIT	Display clock's initial mode For synchronization error conditions the display clock can be stopped on the next VSYNC 1 The display's clock is running after the next VSYNC (indicating new frame) 0 The display's clock is stopped after the next VSYNC (indicating new frame)
22 di1_mask_sel	DI1 Mask select. IPP_PIN_2 output of the DI that functions as MASK signal can come from 2 sources: counter #2 or extracted from the MASK data coming from the memory. 1 IPP_PIN_2 is coming from extracted MASK data coming from the memory 0 IPP_PIN_2 is coming from counter #2
21 di1_vsync_ext	DI1 External VSYNC. This bit selects the source of the VSYNC signal 1 External to the IPU 0 Internally generated by the IPU
20 di1_clk_ext	DI1 External Clock. This bit selects the source of the DI's clock 1 The source of the clock is external to the IPU 0 The clock is internally generated by the IPU
19–18 DI1_WATCHDOG_MODE	DI1 watchdog mode In case of a display error where the DI clock is stopped (defined at di0_err_treatment). An internal watchdog counts DI clocks. If this timer reached its pre defined value the DI will skip the current frame and restart on the frame. This 2 bits define the number of DI clock cycles that the timer counts. 00 The timer counts 4 DI cycles 01 The timer counts 16 DI cycles 10 The timer counts 64 DI cycles 11 The timer counts 128 DI cycles
17 di1_polarity_disp_clk	DI1 Output Clock's polarity This bits define the polarity of the DI's clock. 1 The output clock is active high 0 The output clock is active low
16 Reserved	This read-only field is reserved and always has the value 0.
15–12 di1_sync_count_sel	For synchronous flow error: selects synchronous flow synchronization counter in DI:
11 di1_err_treatment	In case of synchronous flow error there are 2 ways to handle the display 1 to wait (i.e. stop clock) 0 Drive the last component
10 di1_erm_vsync_sel	DI1 error recovery module's VSYNC source select The error recovery block detect a case where the DI's VSYNC is asserted before the EOF. This bit selects the source of the VSYNC signal monitored by this mechanism.

*Table continues on the next page...*

**IPUx\_DI1\_GENERAL field descriptions (continued)**

Field	Description
	1 vsync_post - an internal VSYNC signal asserted 2 lines after the DI's VSYNC 0 vsync_pre - an internal VSYNC signal asserted 2 lines before the DI's VSYNC
9 di1_polarity_cs1	DI1 Chip Select's 1 polarity This bits define the polarity of the DI's CS1. 1 The CS1 is active high 0 The CS1 is active low
8 di1_polarity_cs0	DI1 Chip Select's 0 polarity This bits define the polarity of the DI's CS0. 1 The CS0 is active high 0 The CS0 is active low
di1_polarity_i_1	DI1 output pin's polarity This bits define the polarity of each of the DI's outputs. 1 The output pin is active high 0 The output pin is active low

**37.5.230 DI1 Base Sync Clock Gen 0 Register  
(IPUx\_DI1\_BS\_CLKGEN0)**

Address: Base address + 4\_8004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

**IPUx\_DI1\_BS\_CLKGEN0 field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di1_disp_clk_offset	DI1 Display Clock Offset The DI has the ability to delay the display's clock This field defines the amount of IPU's clock cycles added as delay on this clock.
15–12 Reserved	This read-only field is reserved and always has the value 0.
di1_disp_clk_period	DI1 Display Clock Period This field defines the Display interface clock period for display write access. This parameter contains an integer part (bits 11:4) and a fractional part (bits 3:0). It defines a fractional division ratio of the HSP_CLK clock for generation of the display's interface clock.

### 37.5.231 DI1 Base Sync Clock Gen 1 Register (IPUx\_DI1\_BS\_CLKGEN1)

Address: Base address + 4\_8008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

#### IPUx\_DI1\_BS\_CLKGEN1 field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di1_disp_clk_down	DI1 display clock falling edge position This parameter contains an integer part (bits 24:17) and a fractional part (bit 16). The position value is a time interval between display's access start point and display 's interface clock falling edge.
15–9 Reserved	This read-only field is reserved and always has the value 0.
di1_disp_clk_up	DI1 display clock rising edge position This parameter contains an integer part (bits 8:1) and a fractional part (bit 0). The position value is a time interval between display's access start point and display 's interface clock rising edge.

### 37.5.232 DI1 Sync Wave Gen 1 Register 0 (IPUx\_DI1\_SW\_GEN0\_1)

Address: Base address + 4\_800Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															di1_run_resolution_1
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0														di1_offset_resolution_1	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN0\_1 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN0\_1 field descriptions (continued)**

Field	Description
30–19 di1_run_value_m1_1	DI1 counter #1 pre defined value  This fields defines the counter #1 pre defines value. When the counter is auto reload mode (di1_cnt_auto_reload_1 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di1_step_repeat field.
18–16 di1_run_resolution_1	DI1 counter #1 Run Resolution  This field defines the trigger causing the counter to increment.  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 NA 011 NA 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di1_offset_value_1	DI1 counter #1 offset value  The counter can start counting after a pre defined delay  This field defines the amount of cycles that the counter will be delayed by
di1_offset_resolution_1	DI1 counter #1 offset Resolution  This field defines the trigger causing the offset counter to increment  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 NA 011 NA 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.

### 37.5.233 DI1 Sync Wave Gen 2 Register 0 (IPUx\_DI1\_SW\_GEN0\_2)

Address: Base address + 4\_8010h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	di1_run_value_m1_2														di1_run_resolution_2
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	di1_offset_value_2														di1_offset_resolution_2
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN0\_2 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di1_run_value_m1_2	DI1 counter #2 pre defined value  This fields defines the counter #2 pre defines value. When the counter is auto reload mode (di1_cnt_auto_reload_2 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di1_step_repeat field.
18–16 di1_run_resolution_2	DI1 counter #2 Run Resolution  This field defines the trigger causing the counter to increment.  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 NA 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di1_offset_value_2	DI1 counter #2 offset value  The counter can start counting after a pre defined delay  This field defines the amount of cycles that the counter will be delayed by
di1_offset_resolution_2	DI1 counter #2 offset Resolution  This field defines the trigger causing the offset counter to increment  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN0\_2 field descriptions (continued)**

Field	Description
	011 NA 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.

### 37.5.234 DI1 Sync Wave Gen 3 Register 0 (IPUx\_DI1\_SW\_GEN0\_3)

Address: Base address + 4\_8014h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DI1\_SW\_GEN0\_3 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di1_run_value_m1_3	DI1 counter #3 pre defined value  This fields defines the counter #3 pre defines value. When the counter is auto reload mode (di1_cnt_auto_reload_3 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di1_step_repeat field.
18–16 di1_run_resolution_3	DI1 counter #3 Run Resolution  This field defines the trigger causing the counter to increment.  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN0\_3 field descriptions (continued)**

Field	Description
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di1_offset_value_3	DI1 counter #3 offset value The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by
di1_offset_resolution_3	DI1 counter #3 offset Resolution This field defines the trigger causing the offset counter to increment 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 NA 101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit. — 110 External VSYNC 111 Counter is always on.

**37.5.235 DI1 Sync Wave Gen 4 Register 0  
(IPUx\_DI1\_SW\_GEN0\_4)**

Address: Base address + 4\_8018h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	di1_run_value_m1_4														
W																di1_run_resolution_4
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	di1_offset_value_4														
W																di1_offset_resolution_4
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DI1\_SW\_GEN0\_4 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di1_run_value_m1_4	DI1 counter #4 pre defined value This fields defines the counter #4 pre defines value. When the counter is auto reload mode (di1_cnt_auto_reload_4 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di1_step_repeat field.

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN0\_4 field descriptions (continued)**

Field	Description
18–16 di1_run_resolution_4	<p>DI1 counter #4 Run Resolution</p> <p>This field defines the trigger causing the counter to increment.</p> <p>000 Counter is disabled</p> <p>001 The counter is triggered by the same trigger that triggers the displays clock.</p> <p>010 The Counter is triggered by counter #1</p> <p>011 The Counter is triggered by counter #2</p> <p>100 The Counter is triggered by counter #3</p> <p>101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.</p> <p>—</p> <p>110 External VSYNC</p> <p>111 Counter is always on.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di1_offset_value_4	<p>DI1 counter #4 offset value</p> <p>The counter can start counting after a pre defined delay</p> <p>This field defines the amount of cycles that the counter will be delayed by</p>
di1_offset_resolution_4	<p>DI1 counter #4 offset Resolution</p> <p>This field defines the trigger causing the offset counter to increment</p> <p>000 Counter is disabled</p> <p>001 The counter is triggered by the same trigger that triggers the displays clock.</p> <p>010 The Counter is triggered by counter #1</p> <p>011 The Counter is triggered by counter #2</p> <p>100 The Counter is triggered by counter #3</p> <p>101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.</p> <p>—</p> <p>110 External VSYNC</p> <p>111 Counter is always on.</p>

### 37.5.236 DI1 Sync Wave Gen 5 Register 0 (IPUx\_DI1\_SW\_GEN0\_5)

Address: Base address + 4\_801Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	di1_run_value_m1_5														
W																di1_run_resolution_5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	di1_offset_value_5														
W																di1_offset_resolution_5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DI1\_SW\_GEN0\_5 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di1_run_value_m1_5	DI1 counter #5 pre defined value  This fields defines the counter #5 pre defines value. When the counter is auto reload mode (di1_cnt_auto_reload_5 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di1_step_repeat field.
18–16 di1_run_resolution_5	DI1 counter #5 Run Resolution  This field defines the trigger causing the counter to increment.  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 External VSYNC 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di1_offset_value_5	DI1 counter #5 offset value  The counter can start counting after a pre defined delay  This field defines the amount of cycles that the counter will be delayed by
di1_offset_resolution_5	DI1 counter #5 offset Resolution  This field defines the trigger causing the offset counter to increment  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 -The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 External VSYNC 111 Counter is always on.

### 37.5.237 DI1 Sync Wave Gen 6 Register 0 (IPUx\_DI1\_SW\_GEN0\_6)

Address: Base address + 4\_8020h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0	di1_run_value_m1_6															di1_run_resolution_6
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0	di1_offset_value_6															di1_offset_resolution_6
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN0\_6 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di1_run_value_m1_6	DI1 counter #6 pre defined value This fields defines the counter #6 pre defines value. When the counter is auto reload mode (di1_cnt_auto_reload_6 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di1_step_repeat field.
18–16 di1_run_resolution_6	DI1 counter #6 Run Resolution This field defines the trigger causing the counter to increment. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 The Counter is triggered by counter #5 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di1_offset_value_6	DI1 counter #6 offset value The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by
di1_offset_resolution_6	DI1 counter #6 offset Resolution This field defines the trigger causing the offset counter to increment 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN0\_6 field descriptions (continued)**

Field	Description
	101 The Counter is triggered by counter #4
	110 The Counter is triggered by counter #5
	111 Counter is always on.

### 37.5.238 DI1 Sync Wave Gen 7 Register 0 (IPUx\_DI1\_SW\_GEN0\_7)

Address: Base address + 4\_8024h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DI1\_SW\_GEN0\_7 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di1_run_value_m1_7	DI1 counter #7 pre defined value This fields defines the counter #7 pre defines value. When the counter is auto reload mode (di1_cnt_auto_reload_7 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di1_step_repeat field.
18–16 di1_run_resolution_7	DI1 counter #1 Run Resolution This field defines the trigger causing the counter to increment. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 The Counter is triggered by counter #5 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di1_offset_value_7	DI1 counter #7 offset value The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN0\_7 field descriptions (continued)**

Field	Description																
di1_offset_resolution_1	<p>DI1 counter #7 offset Resolution</p> <p>This field defines the trigger causing the offset counter to increment</p> <table style="margin-left: 20px;"> <tr><td>000</td><td>Counter is disabled</td></tr> <tr><td>001</td><td>The counter is triggered by the same trigger that triggers the displays clock.</td></tr> <tr><td>010</td><td>The Counter is triggered by counter #1</td></tr> <tr><td>011</td><td>The Counter is triggered by counter #2</td></tr> <tr><td>100</td><td>The Counter is triggered by counter #3</td></tr> <tr><td>101</td><td>The Counter is triggered by counter #4</td></tr> <tr><td>110</td><td>The Counter is triggered by counter #5</td></tr> <tr><td>111</td><td>Counter is always on.</td></tr> </table>	000	Counter is disabled	001	The counter is triggered by the same trigger that triggers the displays clock.	010	The Counter is triggered by counter #1	011	The Counter is triggered by counter #2	100	The Counter is triggered by counter #3	101	The Counter is triggered by counter #4	110	The Counter is triggered by counter #5	111	Counter is always on.
000	Counter is disabled																
001	The counter is triggered by the same trigger that triggers the displays clock.																
010	The Counter is triggered by counter #1																
011	The Counter is triggered by counter #2																
100	The Counter is triggered by counter #3																
101	The Counter is triggered by counter #4																
110	The Counter is triggered by counter #5																
111	Counter is always on.																

### 37.5.239 DI1 Sync Wave Gen 8 Register 0 (IPUx\_DI1\_SW\_GEN0\_8)

Address: Base address + 4\_8028h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
	R	0															di1_run_resolution_8
	W																
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
	R	0															di1_offset_resolution_8
	W																
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DI1\_SW\_GEN0\_8 field descriptions**

Field	Description												
31 Reserved	This read-only field is reserved and always has the value 0.												
30–19 di1_run_value_m1_8	<p>DI1 counter #8 pre defined value</p> <p>This fields defines the counter #8 pre defines value. When the counter is auto reload mode (di1_cnt_auto_reload_8 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di1_step_repeat field.</p>												
18–16 di1_run_resolution_8	<p>DI1 counter #8 Run Resolution</p> <p>This field defines the trigger causing the counter to increment.</p> <table style="margin-left: 20px;"> <tr><td>000</td><td>Counter is disabled</td></tr> <tr><td>001</td><td>The counter is triggered by the same trigger that triggers the displays clock.</td></tr> <tr><td>010</td><td>The Counter is triggered by counter #1</td></tr> <tr><td>011</td><td>The Counter is triggered by counter #2</td></tr> <tr><td>100</td><td>The Counter is triggered by counter #3</td></tr> <tr><td>101</td><td>The Counter is triggered by counter #4</td></tr> </table>	000	Counter is disabled	001	The counter is triggered by the same trigger that triggers the displays clock.	010	The Counter is triggered by counter #1	011	The Counter is triggered by counter #2	100	The Counter is triggered by counter #3	101	The Counter is triggered by counter #4
000	Counter is disabled												
001	The counter is triggered by the same trigger that triggers the displays clock.												
010	The Counter is triggered by counter #1												
011	The Counter is triggered by counter #2												
100	The Counter is triggered by counter #3												
101	The Counter is triggered by counter #4												

*Table continues on the next page...*

**IPUx\_DI1\_SW\_GEN0\_8 field descriptions (continued)**

Field	Description
	110 The Counter is triggered by counter #5 111 Counter is always on.
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di1_offset_value_8	DI1 counter #8 offset value The counter can start counting after a pre defined delay This field defines the amount of cycles that the counter will be delayed by
di1_offset_resolution_8	DI1 counter #8 offset Resolution This field defines the trigger causing the offset counter to increment 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1 011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 The Counter is triggered by counter #5 111 Counter is always on.

**37.5.240 DI1Sync Wave Gen 9 Register 0  
(IPUx\_DI1\_SW\_GEN0\_9)**

Address: Base address + 4\_802Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																di1_run_resolution_9
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																di1_offset_resolution_9
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DI1\_SW\_GEN0\_9 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–19 di1_run_value_m1_9	DI1 counter #9 pre defined value This fields defines the counter #9 pre defines value. When the counter is auto reload mode (di1_cnt_auto_reload_9 bit is set), the counter automatically restarts. otherwise the counter restarts for the amount of time defined on the corresponding di1_step_repeat field.

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN0\_9 field descriptions (continued)**

Field	Description
18–16 di1_run_resolution_9	<p>DI1 counter #9 Run Resolution</p> <p>This field defines the trigger causing the counter to increment.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> <li>011 The Counter is triggered by counter #2</li> <li>100 The Counter is triggered by counter #3</li> <li>101 The Counter is triggered by counter #4</li> <li>110 The Counter is triggered by counter #5</li> <li>111 Counter is always on.</li> </ul>
15 Reserved	This read-only field is reserved and always has the value 0.
14–3 di1_offset_value_9	<p>DI1 counter #9 offset value</p> <p>The counter can start counting after a pre defined delay</p> <p>This field defines the amount of cycles that the counter will be delayed by</p>
di1_offset_resolution_9	<p>DI1 counter #9 offset Resolution</p> <p>This field defines the trigger causing the offset counter to increment</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> <li>011 The Counter is triggered by counter #2</li> <li>100 The Counter is triggered by counter #3</li> <li>101 The Counter is triggered by counter #4</li> <li>110 The Counter is triggered by counter #5</li> <li>111 Counter is always on.</li> </ul>

### 37.5.241 DI1 Sync Wave Gen 1 Register 1 (IPUx\_DI1\_SW\_GEN1\_1)

Address: Base address + 4\_8030h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di1_cnt_polarity_gen_en_1		di1_cnt_auto_reload_1		di1_cnt_clr_sel_1						di1_cnt_down_1				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W		di1_cnt_polarity_trigger_sel_1		di1_cnt_polarity_clr_sel_1								di1_cnt_up_1				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN1\_1 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di1_cnt_polarity_gen_en_1	<p>DI1 Counter polarity generator enable</p> <p>The counter's output polarity can be changed on the fly.</p> <ul style="list-style-type: none"> <li>00 Dynamic polarity change is disabled</li> <li>01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2.</li> <li>10 Dynamic polarity change is enabled</li> <li>11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value</li> </ul>
28 di1_cnt_auto_reload_1	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di1_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di1_step_repeat_1 field</li> </ul>
27–25 di1_cnt_clr_sel_1	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 Reserved</li> </ul>

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN1\_1 field descriptions (continued)**

Field	Description
	<p>011 Reserved      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
24–16 di1_cnt_down_1	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di1_cnt_polarity_trigger_sel_1	<p>DI1 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 Reserved      011 Reserved      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
11–9 di1_cnt_polarity_clr_sel_1	<p>DI1 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Reserved      011 Reserved      100 Reserved      101 Reserved      110 Reserved      111 Reserved</p>
di1_cnt_up_1	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.242 DI1 Sync Wave Gen 2 Register 1 (IPUx\_DI1\_SW\_GEN1\_2)

Address: Base address + 4\_8034h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di1_cnt_polarity_gen_en_2		di1_cnt_auto_reload_2		di1_cnt_clr_sel_2							di1_cnt_down_2			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0													di1_cnt_up_2		
W		di1_cnt_polarity_trigger_sel_2		di1_cnt_polarity_clr_sel_2												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN1\_2 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di1_cnt_polarity_gen_en_2	DI1 Counter polarity generator enable The counter's output polarity can be changed on the fly.  00 Dynamic polarity change is disabled 01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2. 10 Dynamic polarity change is enabled 11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value
28 di1_cnt_auto_reload_2	Counter auto reload mode  1 The counter will automatically be reloaded forever, ignoring the value of the di1_step_repeat_<i> field 0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di1_step_repeat_<i> field
27–25 di1_cnt_clr_sel_2	Counter Clear select This field defines the source of the signals that clears the counter.  000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN1\_2 field descriptions (continued)**

Field	Description
	<p>011 Reserved      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
24–16 di1_cnt_down_2	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di1_cnt_polarity_trigger_sel_2	<p>DI1 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 Reserved      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
11–9 di1_cnt_polarity_clr_sel_2	<p>DI1 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Reserved      011 Reserved      100 Reserved      101 Reserved      110 Reserved      111 Reserved</p>
di1_cnt_up_2	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.243 DI1 Sync Wave Gen 3 Register 1 (IPUx\_DI1\_SW\_GEN1\_3)

Address: Base address + 4\_8038h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di1_cnt_polarity_gen_en_3		di1_cnt_auto_reload_3		di1_cnt_clr_sel_3							di1_cnt_down_3			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												di1_cnt_up_3			
W		di1_cnt_polarity_trigger_sel_3		di1_cnt_polarity_clr_sel_3												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN1\_3 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di1_cnt_polarity_gen_en_3	DI1 Counter polarity generator enable The counter's output polarity can be changed on the fly. 00 Dynamic polarity change is disabled 01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2. 10 Dynamic polarity change is enabled 11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value
28 di1_cnt_auto_reload_3	Counter auto reload mode 1 The counter will automatically be reloaded forever, ignoring the value of the di1_step_repeat_<i> field 0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di1_step_repeat_<i> field
27–25 di1_cnt_clr_sel_3	Counter Clear select This field defines the source of the signals that clears the counter. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN1\_3 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
24–16 di1_cnt_down_3	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di1_cnt_polarity_trigger_sel_3	<p>DI1 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 Reserved      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
11–9 di1_cnt_polarity_clr_sel_3	<p>DI1 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Reserved      101 Reserved      110 Reserved      111 Reserved</p>
di1_cnt_up_3	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.244 DI1 Sync Wave Gen 4 Register 1 (IPUx\_DI1\_SW\_GEN1\_4)

Address: Base address + 4\_803Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di1_cnt_polarity_gen_en_4		di1_cnt_auto_reload_4		di1_cnt_clr_sel_4							di1_cnt_down_4			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												di1_cnt_up_4			
W		di1_cnt_polarity_trigger_sel_4		di1_cnt_polarity_clr_sel_4												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN1\_4 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di1_cnt_polarity_gen_en_4	DI1 Counter polarity generator enable The counter's output polarity can be changed on the fly. 00 Dynamic polarity change is disabled 01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2. 10 Dynamic polarity change is enabled 11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value
28 di1_cnt_auto_reload_4	Counter auto reload mode 1 The counter will automatically be reloaded forever, ignoring the value of the di1_step_repeat_<i> field 0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di1_step_repeat_<i> field
27–25 di1_cnt_clr_sel_4	Counter Clear select This field defines the source of the signals that clears the counter. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN1\_4 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
24–16 di1_cnt_down_4	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di1_cnt_polarity_trigger_sel_4	<p>DI1 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 - Counter is disabled      001 - The counter is triggered by the same trigger that triggers the displays clock.      010 - The Counter is triggered by counter #1      011 - The Counter is triggered by counter #2      100 - The Counter is triggered by counter #3      101 - CSI VSYNC. The VSYNC is a trigger coming from one of the CSI's according to the CSI_VSYNC_DEST bit.      —      110 External VSYNC      111 Counter is always on.</p>
11–9 di1_cnt_polarity_clr_sel_4	<p>DI1 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Reserved      110 Reserved      111 Reserved</p>
di1_cnt_up_4	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.245 DI1 Sync Wave Gen 5 Register 1 (IPUx\_DI1\_SW\_GEN1\_5)

Address: Base address + 4\_8040h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di1_cnt_polarity_gen_en_5		di1_cnt_auto_reload_5		di1_cnt_clr_sel_5						di1_cnt_down_5				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W		di1_cnt_polarity_trigger_sel_5		di1_cnt_polarity_clr_sel_5								di1_cnt_up_5				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN1\_5 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di1_cnt_polarity_gen_en_5	<p>DI1 Counter polarity generator enable</p> <p>The counter's output polarity can be changed on the fly.</p> <ul style="list-style-type: none"> <li>00 Dynamic polarity change is disabled</li> <li>01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2.</li> <li>10 Dynamic polarity change is enabled</li> <li>11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value</li> </ul>
28 di1_cnt_auto_reload_5	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di1_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di1_step_repeat_&lt;i&gt; field</li> </ul>
27–25 di1_cnt_clr_sel_5	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> </ul>

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN1\_5 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 External VSYNC      111 Counter is always on.</p>
24–16 di1_cnt_down_5	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di1_cnt_polarity_trigger_sel_5	<p>DI1 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 External VSYNC      111 Counter is always on.</p>
11–9 di1_cnt_polarity_clr_sel_5	<p>DI1 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Output is inverted if the output of counter #4 is set      110 Reserved      111 Reserved</p>
di1_cnt_up_5	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.246 DI1 Sync Wave Gen 6 Register 1 (IPUx\_DI1\_SW\_GEN1\_6)

Address: Base address + 4\_8044h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di1_cnt_polarity_gen_en_6		di1_cnt_auto_reload_6		di1_cnt_clr_sel_6							di1_cnt_down_6			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												di1_cnt_up_6			
W		di1_cnt_polarity_trigger_sel_6		di1_cnt_polarity_clr_sel_6												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN1\_6 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di1_cnt_polarity_gen_en_6	DI1 Counter polarity generator enable The counter's output polarity can be changed on the fly. 00 Dynamic polarity change is disabled 01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2. 10 Dynamic polarity change is enabled 11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value
28 di1_cnt_auto_reload_6	Counter auto reload mode 1 The counter will automatically be reloaded forever, ignoring the value of the di1_step_repeat_<i> field 0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di1_step_repeat_<i> field
27–25 di1_cnt_clr_sel_6	Counter Clear select This field defines the source of the signals that clears the counter. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN1\_6 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
24–16 di1_cnt_down_6	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di1_cnt_polarity_trigger_sel_6	<p>DI1 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
11–9 di1_cnt_polarity_clr_sel_6	<p>DI1 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Output is inverted if the output of counter #4 is set      110 Output is inverted if the output of counter #5 is set      111 Reserved</p>
di1_cnt_up_6	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.247 DI1Sync Wave Gen 7 Register 1 (IPUx\_DI1\_SW\_GEN1\_7)

Address: Base address + 4\_8048h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W		di1_cnt_polarity_gen_en_7		di1_cnt_auto_reload_7		di1_cnt_clr_sel_7							di1_cnt_down_7			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												di1_cnt_up_7			
W		di1_cnt_polarity_trigger_sel_7		di1_cnt_polarity_clr_sel_7												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN1\_7 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di1_cnt_polarity_gen_en_7	DI1 Counter polarity generator enable The counter's output polarity can be changed on the fly. 00 Dynamic polarity change is disabled 01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2. 10 Dynamic polarity change is enabled 11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value
28 di1_cnt_auto_reload_7	Counter auto reload mode 1 The counter will automatically be reloaded forever, ignoring the value of the di1_step_repeat_<i> field 0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di1_step_repeat_<i> field
27–25 di1_cnt_clr_sel_7	Counter Clear select This field defines the source of the signals that clears the counter. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN1\_7 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
24–16 di1_cnt_down_7	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di1_cnt_polarity_trigger_sel_7	<p>DI1 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
11–9 di1_cnt_polarity_clr_sel_7	<p>DI1 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Output is inverted if the output of counter #4 is set      110 Output is inverted if the output of counter #5 is set      111 Output is inverted if the output of counter #6 is set</p>
di1_cnt_up_7	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.248 DI1 Sync Wave Gen 8 Register 1 (IPUx\_DI1\_SW\_GEN1\_8)

Address: Base address + 4\_804Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W				di1_cnt_polarity_gen_en_8		di1_cnt_auto_reload_8								di1_cnt_down_8		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0													di1_cnt_up_8		
W				di1_cnt_polarity_trigger_sel_8		di1_cnt_polarity_clr_sel_8										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN1\_8 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–29 di1_cnt_polarity_gen_en_8	DI1 Counter polarity generator enable The counter's output polarity can be changed on the fly. 00 Dynamic polarity change is disabled 01 The counters UP and DOWN value are calculated according to the trigger selected by cnt_polarity_trigger_sel field. When selecting this mode the UP and DOWN values has to be a multiple of 2. 10 Dynamic polarity change is enabled 11 Outputs polarity is dynamically changed every time the counter reaches its pre defined value
28 di1_cnt_auto_reload_8	Counter auto reload mode 1 The counter will automatically be reloaded forever, ignoring the value of the di1_step_repeat_<i> field 0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di1_step_repeat_<i> field
27–25 di1_cnt_clr_sel_8	Counter Clear select This field defines the source of the signals that clears the counter. 000 Counter is disabled 001 The counter is triggered by the same trigger that triggers the displays clock. 010 The Counter is triggered by counter #1

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN1\_8 field descriptions (continued)**

Field	Description
	<p>011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
24–16 di1_cnt_down_8	<p>Counter falling edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.</p>
15 Reserved	This read-only field is reserved and always has the value 0.
14–12 di1_cnt_polarity_trigger_sel_8	<p>DI1 Counter's toggling trigger select      This field selects the counter's trigger causing the output to toggle</p> <p>000 Counter is disabled      001 The counter is triggered by the same trigger that triggers the displays clock.      010 The Counter is triggered by counter #1      011 The Counter is triggered by counter #2      100 The Counter is triggered by counter #3      101 The Counter is triggered by counter #4      110 The Counter is triggered by counter #5      111 Counter is always on.</p>
11–9 di1_cnt_polarity_clr_sel_8	<p>DI1 counter's polarity Clear select      This field selects the input to the counter telling the counter whether to invert the output</p> <p>000 Output is always inverted      001 Output is kept the same (no inversion)      010 Output is inverted if the output of counter #1 is set      011 Output is inverted if the output of counter #2 is set      100 Output is inverted if the output of counter #3 is set      101 Output is inverted if the output of counter #4 is set      110 Output is inverted if the output of counter #5 is set      111 Output is inverted if the output of counter #6 is set</p>
di1_cnt_up_8	<p>Counter rising edge position      This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).      The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.</p>

### 37.5.249 DI1 Sync Wave Gen 9 Register 1 (IPUx\_DI1\_SW\_GEN1\_9)

Address: Base address + 4\_8050h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
	di1_gentime_sel_9			di1_cnt_auto_reload_9		di1_cnt_clr_sel_9							di1_cnt_down_9			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	di1_tag_sel_9			0									di1_cnt_up_9			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SW\_GEN1\_9 field descriptions

Field	Description
31–29 di1_gentime_sel_9	<p>Counter #9 main waveform select</p> <p>This field defines the counter that counter #9's auxiliary waveform will be attached too.</p> <ul style="list-style-type: none"> <li>000 Counter #9's waveform is attached to counter #1's waveform</li> <li>001 Counter #9's waveform is attached to counter #2's waveform</li> <li>010 Counter #9's waveform is attached to counter #3's waveform</li> <li>011 Counter #9's waveform is attached to counter #4's waveform</li> <li>100 Counter #9's waveform is attached to counter #5's waveform</li> <li>101 Counter #9's waveform is attached to counter #6's waveform</li> <li>110 Counter #9's waveform is attached to counter #7's waveform</li> <li>111 Counter #9's waveform is attached to counter #8's waveform</li> </ul>
28 di1_cnt_auto_reload_9	<p>Counter auto reload mode</p> <ul style="list-style-type: none"> <li>1 The counter will automatically be reloaded forever, ignoring the value of the di1_step_repeat_&lt;i&gt; field</li> <li>0 The counter will not be automatically reloaded, It will be reloaded for the amount of repeat times defined on the di1_step_repeat_&lt;i&gt; field</li> </ul>
27–25 di1_cnt_clr_sel_9	<p>Counter Clear select</p> <p>This field defines the source of the signals that clears the counter.</p> <ul style="list-style-type: none"> <li>000 Counter is disabled</li> <li>001 The counter is triggered by the same trigger that triggers the displays clock.</li> <li>010 The Counter is triggered by counter #1</li> </ul>

Table continues on the next page...

**IPUx\_DI1\_SW\_GEN1\_9 field descriptions (continued)**

Field	Description
	011 The Counter is triggered by counter #2 100 The Counter is triggered by counter #3 101 The Counter is triggered by counter #4 110 The Counter is triggered by counter #5 111 Counter is always on.
24–16 di1_cnt_down_9	Counter falling edge position  This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).  The position value is the amount of cycles between the trigger's start point and the waveform's falling edge.
15 di1_tag_sel_9	Counter #9 can send a synchronous tag when counter #9 reaches its predefined value or when it's triggering counter reaches its pre defined value.  1 tag source is counter #9 0 Tag's source is the triggering counter.
14–9 Reserved	This read-only field is reserved and always has the value 0.
di1_cnt_up_9	Counter rising edge position  This parameter contains an integer part (bits 24:17) and a fractional part (bit 16).  The position value is the amount of cycles between the trigger's start point and the waveform's rising edge.

### 37.5.250 DI1 Sync Assistance Gen Register (IPUx\_DI1\_SYNC\_AS\_GEN)

Address: Base address + 4\_8054h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DI1\_SYNC\_AS\_GEN field descriptions**

Field	Description
31–29 -	Reserve
28 di1_sync_start_en	di1_sync_start_en
27–16 Reserved	This read-only field is reserved and always has the value 0.
15–13 di1_vsync_sel	VSYNC select This field defines which of the counters functions as VSYNC signal 000 VSYNC is coming from counter #1 001 VSYNC is coming from counter #2 111 VSYNC is coming from counter #8
12 Reserved	This read-only field is reserved and always has the value 0.
di1_sync_start	DI1 Sync start This field defines the number of low (including blanking rows) on the which the DI1 starts preparing the data for the next frame.

**37.5.251 DI1 Data Wave Gen <i> Register (IPUx\_DI1\_DW\_GEN\_i)**

The DI1\_DW\_GEN\_<i> register holds pointers for the waveform generators.

These registers have different bit arrangements for parallel and serial display. When using a parallel display [VDI Plane Size Register 4](#) is applicable. When using a serial interface [VDI Plane Size Register 4](#) is applicable.

**Table 37-704. Register Field Descriptions for Serial display**

Field	Description
31–24 di1_serial_period_<i>	DI1 Serial Period <i> This field defines the period of the time base serial display clock. The units are the internal DI clock
23–16 di1_start_period_<i>	DI1 start period This field defines the amount of cycles between the point where the access is ready to be launched to the actual point where the time base serial display clock restarts. The units are the internal DI clock.
15–14 di1_cst_<i>	DI1 Chip Select pointer for waveform <i> This field points to a register that defines the waveform of the CS pin. For serial displays the down value as defined on DI1_DW_SET*_<i> is measured from the assertion of the last serial display time base clock. 00 The waveform is defined according to the settings on DI1_DW_SET0_<i> 01 The waveform is defined according to the settings on DI1_DW_SET1_<i>

*Table continues on the next page...*

**Table 37-704. Register Field Descriptions for Serial display (continued)**

Field	Description
	10 The waveform is defined according to the settings on DI1_DW_SET2_<i> 11 The waveform is defined according to the settings on DI1_DW_SET3_<i>
13-9	Reserved
8-4 di1_serial_valid_bits_<i>	DI1 Serial valid bits. This field defines the amount of valid bits to be transmitted within the 32 bits internal word aligned to bit[0]. The actual amount of valid bits is di1_serial_valid_bits_<i> + 1
3-2 di1_serial_rs_<i>	DI1 Serial RS This field points to a register that defines the waveform of the RS pin. For serial displays the down value as defined on DI1_DW_SET*_<i> is measured from the assertion of the last serial display time base clock. 00 The waveform is defined according to the settings on DI1_DW_SET0_<i> 01 The waveform is defined according to the settings on DI1_DW_SET1_<i> 10 The waveform is defined according to the settings on DI1_DW_SET2_<i> 11 The waveform is defined according to the settings on DI1_DW_SET3_<i>
1-0 di1_serial_clk_<i>	DI1 serial clock<i> This field points to a register that defines the waveform of the Serial clock pin. 00 The waveform is defined according to the settings on DI1_DW_SET0_<i> 01 The waveform is defined according to the settings on DI1_DW_SET1_<i> 10 The waveform is defined according to the settings on DI1_DW_SET2_<i> 11 The waveform is defined according to the settings on DI1_DW_SET3_<i>

Address: Base address + 4\_8058h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																	di1_cst_i	di1_pt_6_i	di1_pt_5_i	di1_pt_4_i	di1_pt_3_i	di1_pt_2_i	di1_pt_1_i	di1_pt_0_i										
W	di1_access_size_i																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

**IPUx\_DI1\_DW\_GEN\_i field descriptions**

Field	Description
31-24 di1_access_size_i	DI1 Access Size <i> This field defines the amount of IPU cycles between any 2 accesses (an access may be a pixel or generic data that may have more than one component)
23-16 di1_component_size_i	DI1 component Size This field defines the amount of IPU cycles between any 2 components
15-14 di1_cst_i	DI1 Chip Select pointer for waveform <i> This field points to a register that defines the waveform of the CS pin. The CS is automatically mapped to a specific display

Table continues on the next page...

**IPUx\_DI1\_DW\_GEN\_i field descriptions (continued)**

Field	Description
	<p>00 The waveform is defined according to the settings on DI1_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DI1_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DI1_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DI1_DW_SET3_&lt;i&gt;</p>
13–12 di1_pt_6_i	<p>DI1 PIN_17 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_17 pin.</p> <p>00 The waveform is defined according to the settings on DI1_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DI1_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DI1_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DI1_DW_SET3_&lt;i&gt;</p>
11–10 di1_pt_5_i	<p>DI1 PIN_16 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_16 pin.</p> <p>00 The waveform is defined according to the settings on DI1_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DI1_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DI1_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DI1_DW_SET3_&lt;i&gt;</p>
9–8 di1_pt_4_i	<p>DI1 PIN_15 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_15 pin.</p> <p>00 The waveform is defined according to the settings on DI1_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DI1_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DI1_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DI1_DW_SET3_&lt;i&gt;</p>
7–6 di1_pt_3_i	<p>DI1 PIN_14 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_14 pin.</p> <p>00 The waveform is defined according to the settings on DI1_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DI1_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DI1_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DI1_DW_SET3_&lt;i&gt;</p>
5–4 di1_pt_2_i	<p>DI1 PIN_13 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_13 pin.</p> <p>00 The waveform is defined according to the settings on DI1_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DI1_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DI1_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DI1_DW_SET3_&lt;i&gt;</p>
3–2 di1_pt_1_i	<p>DI1 PIN_12 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_12 pin.</p> <p>00 The waveform is defined according to the settings on DI1_DW_SET0_&lt;i&gt;</p> <p>01 The waveform is defined according to the settings on DI1_DW_SET1_&lt;i&gt;</p> <p>10 The waveform is defined according to the settings on DI1_DW_SET2_&lt;i&gt;</p> <p>11 The waveform is defined according to the settings on DI1_DW_SET3_&lt;i&gt;</p>

*Table continues on the next page...*

**IPUx\_DI1\_DW\_GEN\_i field descriptions (continued)**

Field	Description
di1_pt_0_i	<p>DI1 PIN_11 pointer for waveform &lt;i&gt;</p> <p>This field points to a register that defines the waveform of the PIN_11 pin.</p> <p>00 The waveform is defined according to the settings on DI1_DW_SET0_&lt;i&gt;      01 The waveform is defined according to the settings on DI1_DW_SET1_&lt;i&gt;      10 The waveform is defined according to the settings on DI1_DW_SET2_&lt;i&gt;      11 - The waveform is defined according to the settings on DI1_DW_SET3_&lt;i&gt;</p>

**37.5.252 DI1 Data Wave Set 0 <i> Register  
(IPUx\_DI1\_DW\_SET0\_i)**

Address: Base address + 4\_8088h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DI1\_DW\_SET0\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di1_data_cnt_down0_i	<p>Waveform's falling edge position.</p> <p>This field defines the Waveform's falling edge position. The Waveform is mapped to a pint according to the corresponding di1_pt_*_&lt;i&gt;</p>
15–9 Reserved	This read-only field is reserved and always has the value 0.
di1_data_cnt_up0_i	<p>Waveform's rising edge position.</p> <p>This field defines the Waveform's rising edge position. The Waveform is mapped to a pint according to the corresponding di1_pt_*_&lt;i&gt;</p>

**37.5.253 DI1 Data Wave Set 1 <i> Register  
(IPUx\_DI1\_DW\_SET1\_i)**

Address: Base address + 4\_80B8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DI1\_DW\_SET1\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di1_data_cnt_down1_i	Waveform's falling edge position. This field defines the Waveform's falling edge position. The Waveform is mapped to a pint according to the corresponding di1_pt_*_<i>
15–9 Reserved	This read-only field is reserved and always has the value 0.
di1_data_cnt_up1_i	Waveform's rising edge position. This field defines the Waveform's rising edge position. The Waveform is mapped to a pint according to the corresponding di1_pt_*_<i>

**37.5.254 DI1 Data Wave Set 2 <i> Register  
(IPUx\_DI1\_DW\_SET2\_i)**

Address: Base address + 4\_80E8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DI1\_DW\_SET2\_i field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di1_data_cnt_down2_i	Waveform's falling edge position. This field defines the Waveform's falling edge position. The Waveform is mapped to a pint according to the corresponding di1_pt_*_<i>
15–9 Reserved	This read-only field is reserved and always has the value 0.
di1_data_cnt_up2_i	Waveform's rising edge position. This field defines the Waveform's rising edge position. The Waveform is mapped to a pint according to the corresponding di1_pt_*_<i>

### 37.5.255 DI1 Data Wave Set 3 <i> Register (IPUx\_DI1\_DW\_SET3\_i)

Address: Base address + 4\_8118h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

#### IPUx\_DI1\_DW\_SET3\_i field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24–16 di1_data_cnt_down3_i	Waveform's falling edge position. This field defines the Waveform's falling edge position. The Waveform is mapped to a pint according to the corresponding di1_pt_*_<i>
15–9 Reserved	This read-only field is reserved and always has the value 0.
di1_data_cnt_up3_i	Waveform's rising edge position. This field defines the Waveform's rising edge position. The Waveform is mapped to a pint according to the corresponding di1_pt_*_<i>

### 37.5.256 DI1 Step Repeat <i> Registers (IPUx\_D1\_STP\_REP\_i)

Address: Base address + 4\_8148h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

#### IPUx\_D1\_STP\_REP\_i field descriptions

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 di1_step_repeat_2i	Step Repeat <i> This fields defines the amount of repetitions that will be performed by the counter <i>
15–12 Reserved	This read-only field is reserved and always has the value 0.
di1_step_repeat_2i_minus_1	Step Repeat <i> This fields defines the amount of repetitions that will be performed by the counter <i>

### 37.5.257 DI1Step Repeat 9 Registers (IPUx\_DI1\_STP\_REPEAT\_9)

Address: Base address + 4\_8158h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0																	
W																																		

Reset 0

#### IPUx\_DI1\_STP\_REPEAT\_9 field descriptions

Field	Description
31–12 Reserved	This read-only field is reserved and always has the value 0.
di1_step_repeat_9	Step Repeat 9 This fields defines the amount of repetitions that will be performed by the counter 9.

### 37.5.258 DI1 Serial Display Control Register (IPUx\_DI1\_SER\_CONF)

Address: Base address + 4\_815Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16																
R																																	
W																																	

Reset 0

Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0																	
R																																		
W																																		

Reset 0

**IPUx\_DI1\_SER\_CONF field descriptions**

Field	Description
31–28 DI1_SERIAL_ LLA_PNTR_RS_ R_1	RS 3 waveform pointer for read low level access  This pointer defines which waveform set will be chosen when the read low level access is targeted to RS group 1.  0000 Waveform set #1 0001 Waveform set #2 1011 Waveform set #12 1100 Reserved 1101 Reserved 1100 Reserved
27–24 DI1_SERIAL_ LLA_PNTR_RS_ R_0	RS 2 waveform pointer for low level access  This pointer defines which waveform set will be chosen when the read low level access is targeted to RS group 0.  0000 Waveform set #1 0001 Waveform set #2 1011 Waveform set #12 1100 Reserved 1101 Reserved 1100 Reserved
23–20 DI1_SERIAL_ LLA_PNTR_RS_ W_1	RS 1 waveform pointer for write low level access  This pointer defines which waveform set will be chosen when the write low level access is targeted to RS group 1.  0000 Waveform set #1 0001 Waveform set #2 1011 Waveform set #12 1100 Reserved 1101 Reserved 1100 Reserved
19–16 DI1_SERIAL_ LLA_PNTR_RS_ W_0	RS 0 waveform pointer for write low level access  This pointer defines which waveform set will be chosen when the write low level access is targeted to RS group 0.  0000 Waveform set #1 0001 Waveform set #2 1011 Waveform set #12 1100 Reserved 1101 Reserved 1100 Reserved
15–8 DI1_SERIAL_ LATCH	DI1 Serial Latch  This field defines how many cycles to insert between serial read accesses start to data sampling in the
7–6 Reserved	This read-only field is reserved and always has the value 0.

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**IPUx\_DI1\_SER\_CONF field descriptions (continued)**

Field	Description
5 DI1_LLA_SER_ACCESS	<p>Direct Low Level Access to Serial display</p> <p>1 ARM platform access is performed via a direct path to the serial display in LLA mode, in this mode only the ARM platform in LLA mode can access the serial port</p> <p>0 ARM platform access to the serial display port is not done directly, hence other source are allowed to access the serial port. The arbitration is done automatically</p>
4 DI1_SER_CLK_POLARITY	<p>Serial Clock Polarity</p> <p>The output polarity of the SER_CLK pin</p> <p>1 The clock is inverted</p> <p>0 The clock is not inverted</p>
3 DI1_SERIAL_DATA_POLARITY	<p>Serial Data Polarity</p> <p>The output polarity of the SER_DATA pin</p> <p>1 The data is inverted</p> <p>0 The data is not inverted</p>
2 DI1_SERIAL_RS_POLARITY	<p>Serial RS Polarity</p> <p>The output polarity of the SER_RS pin</p> <p>1 The RS is inverted</p> <p>0 The RS is not inverted</p>
1 DI1_SERIAL_CS_POLARITY	<p>Serial Chip Select Polarity</p> <p>The output polarity of the SER_CS pin</p> <p>1 The CS is inverted</p> <p>0 The CS is not inverted</p>
0 DI1_WAIT4SERIAL	<p>Wait for Serial</p> <p>When the parallel display share pins with the serial port. Accessing the parallel port is not allowed till the serial port completes its access.</p> <p>1 The parallel port should wait to the serial port as the pins are shared</p> <p>0 The parallel port should not wait to the serial port as the pins are not shared</p>

### 37.5.259 DI1 Special Signals Control Register (IPUx\_DI1\_SSC)

Address: Base address + 4\_8160h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									DI1_PIN17_ERM	DI1_PIN16_ERM	DI1_PIN15_ERM	DI1_PIN14_ERM	DI1_PIN13_ERM	DI1_PIN12_ERM	DI1_PIN11_ERM	DI1_CS_ERM
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									DI1_WAIT_ON	DI1_BYTE_EN_POLARITY	DI1_BYTE_EN_RD_IN	DI1_BYTE_EN_PNTR				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DI1\_SSC field descriptions

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23 DI1_PIN17_ERM	DI1 PIN17 error recovery mode. This bit defines the error recovery mode of the PIN17 pin.  1 The PIN17 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC. 0 Nothing is done to the PIN17 pin following a display error detection.
22 DI1_PIN16_ERM	DI1 PIN16 error recovery mode. This bit defines the error recovery mode of the PIN16 pin.  1 The PIN16 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC. 0 Nothing is done to the PIN16 pin following a display error detection.
21 DI1_PIN15_ERM	DI1 PIN15 error recovery mode. This bit defines the error recovery mode of the PIN15 pin.  1 The PIN15 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC. 0 Nothing is done to the PIN15 pin following a display error detection.
20 DI1_PIN14_ERM	DI1 PIN14 error recovery mode. This bit defines the error recovery mode of the PIN14 pin.

*Table continues on the next page...*

## IPUx\_DI1\_SSC field descriptions (continued)

Field	Description
	<p>1 The PIN14 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC. 0 Nothing is done to the PIN14 pin following a display error detection.</p>
19 DI1_PIN13_ERM	<p>DI1 PIN13 error recovery mode. This bit defines the error recovery mode of the PIN13 pin.</p> <p>1 The PIN13 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC. 0 Nothing is done to the PIN13 pin following a display error detection.</p>
18 DI1_PIN12_ERM	<p>DI1 PIN12 error recovery mode. This bit defines the error recovery mode of the PIN12 pin.</p> <p>1 The PIN12 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC. 0 Nothing is done to the PIN12 pin following a display error detection.</p>
17 DI1_PIN11_ERM	<p>DI1 PIN11 error recovery mode. This bit defines the error recovery mode of the PIN11 pin.</p> <p>1 The PIN11 pin is cleared in case of a synchronous display error. The clear will be done on the next VSYNC. 0 Nothing is done to the PIN11 pin following a display error detection.</p>
16 DI1_CS_ERM	<p>DI1 GLUELOGIC error recovery mode. This bit defines the error recovery mode of the GLUELOGIC.</p> <p>1 The GLUELOGIC is release in case of a synchronous display error. The release will be done on the next VSYNC. 0 Nothing is done to the GLUELOGIC following a display error detection.</p>
15–6 Reserved	This read-only field is reserved and always has the value 0.
5 DI1_WAIT_ON	<p>Wait On This field defines the DC's response to WAIT signal</p> <p>1 The DC holds the flow as long as WAIT is asserted. 0 The DC continues the flow regardless the WAIT signal.</p>
4 DI1_BYTE_EN_POLARITY	<p>Byte Enable polarity This bit defines the polarity of the byte enable signals to the display.</p> <p>1 active high. 0 active low.</p>
3 DI1_BYTE_EN_RD_IN	<p>Byte Enable Read In This bit selects the source of the byte enable pins</p> <p>1 The write byte enable signals are routed via bits [17:16] of the display's data, The read byte enable signals are routed via bits [19:18 of the display's data 0 The byte enable signals are routed via bits [17:16] of the display's data for both read and write</p>
DI1_BYTE_EN_PNTR	Byte Enable Pointer This pointer selects the pin asserted along with the byte enables signals

*Table continues on the next page...*

**IPUx\_DI1\_SSC field descriptions (continued)**

Field	Description
	000 wave form of byte enable as pin_11 001 wave form of byte enable as pin_12 111 wave form of byte enable as suitable CS pin

**37.5.260 DI1 Polarity Register (IPUx\_DI1\_POL)**

Address: Base address + 4\_8164h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R						DI1_WAIT_POLARITY	DI1_CS1_BYTE_EN_POLARITY	DI1_CS0_BYTE_EN_POLARITY	DI1_CS1_DATA_POLARITY							
W						0	0	0								di1_cs1_polarity
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DI1_CS0_DATA_POLARITY								DI1_DRDY_DATA_POLARITY							di1_drdy_polarity
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DI1\_POL field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26 DI1_WAIT_POLARITY	WAIT polarity This bit defines the polarity of the wait signal input coming from the display 1 active high 0 active low
25 DI1_CS1_BYTE_EN_POLARITY	Byte Enable associated with CS1 polarity This bit defines the polarity of the byte enable signals to the display 1 active high 0 active low

Table continues on the next page...

**IPUx\_DI1\_POL field descriptions (continued)**

Field	Description
24 DI1_CS0_BYTE_EN_POLARITY	Byte Enable associated with CS0 polarity This bit defines the polarity of the byte enable signals to the display 1 active high 0 active low
23 DI1_CS1_DATA_POLARITY	Data Polarity associated with CS1
22–16 di1_cs1_polarity	DI1 output pin's polarity for CS1 These bits define the polarity of each of the DI's outputs when CS1 is asserted 1 The output pin is active high 0 The output pin is active low
15 DI1_CS0_DATA_POLARITY	Data Polarity associated with CS0
14–8 di1_cs0_polarity	DI1 output pin's polarity for CS1 These bits define the polarity of each of the DI's outputs when CS1 is asserted 1 The output pin is active high 0 The output pin is active low
7 DI1_DRDY_DATA_POLARITY	Data Polarity associated with DRDY
di1_drdy_polarity	DI1 output dynamic pin's polarity for synchronous access These bits define the polarity of each of the DI's outputs when synchronous display access is asserted The pins' default polarity is the same as defined in the di0_drdy_polarity bits 1 The output pin is active high 0 The output pin is active low

**37.5.261 DI1Active Window 0 Register (IPUx\_DI1\_AW0)**

Address: Base address + 4\_8168h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DI1\_AW0 field descriptions**

Field	Description
31–28 DI1_AW_TRIG_SEL	This field selects the trigger for sending data during the display's active window  000 disabled 001 The trigger is the same trigger that triggers the displays clock. 010 The trigger is counter #1 011 The trigger is counter #2 100 The trigger is counter #3 101 The trigger is counter #4 110 The trigger is counter #5 111 The trigger is always on.
27–16 DI1_AW_HEND	This field defines the horizontal end of the active window
15–12 DI1_AW_HCOUNTER_SEL	This field selects the counter that counts the horizontal position of the display's active window  0000 disabled 0001 reserved 0010 The counter is counter #1 0011 The counter is counter #2 0100 The counter is counter #3 0101 The counter is counter #4 0110 The counter is counter #5 1001 The counter is counter #8
DI1_AW_HSTART	This field defines the horizontal start of the active window  DI1_AW_HSTART < DI1_AW_HEND

**37.5.262 DI1 Active Window 1 Register (IPUx\_DI1\_AW1)**

Address: Base address + 4\_816Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	0																DI1_AW_VCOUNT_SEL																
W																																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DI1\_AW1 field descriptions**

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–16 DI1_AW_VEND	This field defines the vertical end of the active window
15–12 DI1_AW_VCOUNT_SEL	This field selects the counter that counts the vertical position of the display's active window  0000 disabled 0001 reserved

Table continues on the next page...

**IPUx\_DI1\_AW1 field descriptions (continued)**

Field	Description
	0010 The counter is counter #1 0011 The counter is counter #2 0100 The counter is counter #3 0101 The counter is counter #4 0110 The counter is counter #5 1001 The counter is counter #8
DI1_AW_VSTART	This field defines the vertical start of the active window $\text{DI1\_AW\_VSTART} < \text{DI1\_AW\_VEND}$

### 37.5.263 DI1 Screen Configuration Register (IPUx\_DI1\_SCR\_CONF)

Address: Base address + 4\_8170h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																0																		
W																																		

Reset 0

**IPUx\_DI1\_SCR\_CONF field descriptions**

Field	Description
31–12 Reserved	This read-only field is reserved and always has the value 0.
DI1_SCREEN_HEIGHT	This field defines the number of display rows (Number_of_ROWS = DI1_SCREEN_HEIGHT+1) This field is used for VSYNC calculation and for anti-tearing

### 37.5.264 DI1 Status Register (IPUx\_DI1\_STAT)

Address: Base address + 4\_8174h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0				DI1_CNT_R_FIFO_FULL	DI1_CNT_R_FIFO_EMPTY	DI1_READ_FIFO_FULL	DI1_READ_FIFO_EMPTY
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

**IPUx\_DI1\_STAT field descriptions**

Field	Description
31–4 Reserved	This read-only field is reserved and always has the value 0.
3 DI1_CNTR_ FIFO_FULL	This bit indicates a full state of the DI1 FIFO. This FIFO is part of the DI1 synchronizer.
2 DI1_CNTR_ FIFO_EMPTY	This bit indicates an empty state of the DI1 FIFO. This FIFO is part of the DI1 synchronizer.
1 DI1_READ_ FIFO_FULL	This bit indicates a full state of the DI1 FIFO when performing a read. This FIFO is part of the DI1 synchronizer.
0 DI1_READ_ FIFO_EMPTY	This bit indicates an empty state of the DI1 FIFO when performing a read. This FIFO is part of the DI1 synchronizer.

**37.5.265 SMFC Mapping Register (IPUx\_SMFC\_MAP)**

The purpose of this register is to map CSI frames to IDMAC channels.

Address: Base address + 5\_0000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_SMFC\_MAP field descriptions**

Field	Description
31–12 Reserved	This read-only field is reserved and always has the value 0.
11–9 MAP_CH3	DMASMFC channel 3 mapping bits. 000 CSI0, ID=0 mapped to DMASMFC channel 3. 001 CSI0, ID=1 mapped to DMASMFC channel 3. 010 CSI0, ID=2 mapped to DMASMFC channel 3. 011 CSI0, ID=3 mapped to DMASMFC channel 3. 100 CSI1, ID=0 mapped to DMASMFC channel 3. 101 CSI1, ID=1 mapped to DMASMFC channel 3. 110 CSI1, ID=2 mapped to DMASMFC channel 3. 111 CSI1, ID=3 mapped to DMASMFC channel 3.
8–6 MAP_CH2	DMASMFC channel 2 mapping bits. 000 CSI0, ID=0 mapped to DMASMFC channel 2.

*Table continues on the next page...*

**IPUx\_SMFC\_MAP field descriptions (continued)**

Field	Description
	001 CSI0, ID=1 mapped to DMASMFC channel 2. 010 CSI0, ID=2 mapped to DMASMFC channel 2. 011 CSI0, ID=3 mapped to DMASMFC channel 2. 100 CSI1, ID=0 mapped to DMASMFC channel 2. 101 CSI1, ID=1 mapped to DMASMFC channel 2. 110 CSI1, ID=2 mapped to DMASMFC channel 2. 111 CSI1, ID=3 mapped to DMASMFC channel 2.
5–3 MAP_CH1	DMASMFC channel 1 mapping bits.  000 CSI0, ID=0 mapped to DMASMFC channel 1. 001 CSI0, ID=1 mapped to DMASMFC channel 1. 010 CSI0, ID=2 mapped to DMASMFC channel 1. 011 CSI0, ID=3 mapped to DMASMFC channel 1. 100 CSI1, ID=0 mapped to DMASMFC channel 1. 101 CSI1, ID=1 mapped to DMASMFC channel 1. 110 CSI1, ID=2 mapped to DMASMFC channel 1. 111 CSI1, ID=3 mapped to DMASMFC channel 1.
MAP_CH0	DMASMFC channel 0 mapping bits.  000 CSI0, ID=0 mapped to DMASMFC channel 0. 001 CSI0, ID=1 mapped to DMASMFC channel 0. 010 CSI0, ID=2 mapped to DMASMFC channel 0. 011 CSI0, ID=3 mapped to DMASMFC channel 0. 100 CSI1, ID=0 mapped to DMASMFC channel 0. 101 CSI1, ID=1 mapped to DMASMFC channel 0. 110 CSI1, ID=2 mapped to DMASMFC channel 0. 111 CSI1, ID=3 mapped to DMASMFC channel 0.

**37.5.266 SMFC Watermark Control Register (IPUx\_SMFC\_WMC)**

The purpose of this register is to control watermark levels of DMA channels. The bit setting given relative to FIFO size and not in number of words since FIFO size depend from number of enabled DMA channels.

Address: Base address + 5\_0004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0 1 0 0 0 1 1 0 1 0 0 1 1 0 0

**IPUx\_SMFC\_WMC field descriptions**

Field	Description
31–28 Reserved	This read-only field is reserved and always has the value 0.
27–25 WM3_CLR	Watermark "clear" level of DMASMFC channel 3.  000 clear watermark level when FIFO is full on 1/8 of their size. 001 clear watermark level when FIFO is full on 2/8 of their size. 110 clear watermark level when FIFO is full on 7/8 of their size. 111 clear watermark level when FIFO is full.
24–22 WM3_SET	Watermark "set" level of DMASMFC channel 3  000 set watermark level when FIFO is full on 1/8 of their size. 001 set watermark level when FIFO is full on 2/8 of their size. 110 set watermark level when FIFO is full on 7/8 of their size. 111 set watermark level when FIFO is full.
21–19 WM2_CLR	Watermark "clear" level of DMASMFC channel 2.  000 clear watermark level when FIFO is full on 1/8 of their size. 001 clear watermark level when FIFO is full on 2/8 of their size. 110 clear watermark level when FIFO is full on 7/8 of their size. 111 clear watermark level when FIFO is full.
18–16 WM2_SET	Watermark "set" level of DMASMFC channel 2.  000 set watermark level when FIFO is full on 1/8 of their size. 001 set watermark level when FIFO is full on 2/8 of their size. 110 set watermark level when FIFO is full on 7/8 of their size. 111 set watermark level when FIFO is full.
15–12 Reserved	This read-only field is reserved and always has the value 0.
11–9 WM1_CLR	Watermark "clear" level of DMASMFC channel 1.  000 clear watermark level when FIFO is full on 1/8 of their size. 001 clear watermark level when FIFO is full on 2/8 of their size. 110 clear watermark level when FIFO is full on 7/8 of their size. 111 clear watermark level when FIFO is full.
8–6 WM1_SET	Watermark "set" level of DMASMFC channel 1.  000 set watermark level when FIFO is full on 1/8 of their size. 001 set watermark level when FIFO is full on 2/8 of their size. 110 set watermark level when FIFO is full on 7/8 of their size. 111 set watermark level when FIFO is full.
5–3 WM0_CLR	Watermark "clear" level of DMASMFC channel 0.  000 clear watermark level when FIFO is full on 1/8 of their size. 001 clear watermark level when FIFO is full on 2/8 of their size. 110 clear watermark level when FIFO is full on 7/8 of their size. 111 clear watermark level when FIFO is full.
WM0_SET	Watermark "set" level of DMASMFC channel 0.

*Table continues on the next page...*

**IPUx\_SMFC\_WMC field descriptions (continued)**

Field	Description
	000 set watermark level when FIFO is full on 1/8 of their size.
	001 set watermark level when FIFO is full on 2/8 of their size.
	110 set watermark level when FIFO is full on 7/8 of their size.
	111 set watermark level when FIFO is full.

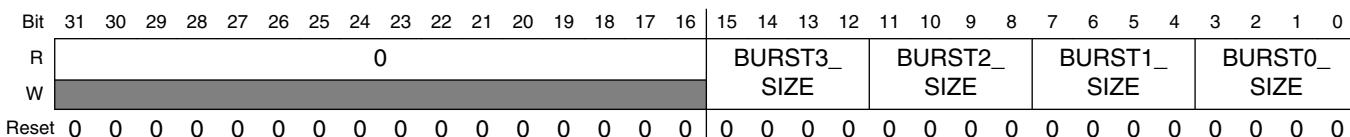
**37.5.267 SMFC Burst Size Register (IPUx\_SMFC\_BS)**

This register holds the burst size value for each DMASMFC channel. The burst size is the number of IDMAC's active accesses that will done for each IDMAC's burst. This number is a function of PFS, BPP & NPB parameters in the IDMAC's CPMEM. These are the parameters corresponding to the IDMAC's channel used. The table below describes what should be the burst size according to PFS, BPP & NPB settings

**Table 37-721. SMFC Burst Size**

BPP	PFS	BURST_SIZE
8	6	NPB[6:4]
16	6	NPB[6:3]
All other	All other	NPB[6:2]

Address: Base address + 5\_0008h offset

**IPUx\_SMFC\_BS field descriptions**

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.
15–12 BURST3_SIZE	Burst Size of SMFCDMA channel 3. The value programed here should be BURST_SIZE-1 (for example: for a burst size of 1, write 0 to these bits)
11–8 BURST2_SIZE	Burst Size of SMFCDMA channel 2. The value programed here should be BURST_SIZE-1 (for example: for a burst size of 1, write 0 to these bits)
7–4 BURST1_SIZE	Burst Size of SMFCDMA channel 1. The value programed here should be BURST_SIZE-1 (for example: for a burst size of 1, write 0 to these bits)
BURST0_SIZE	Burst Size of SMFCDMA channel 0.

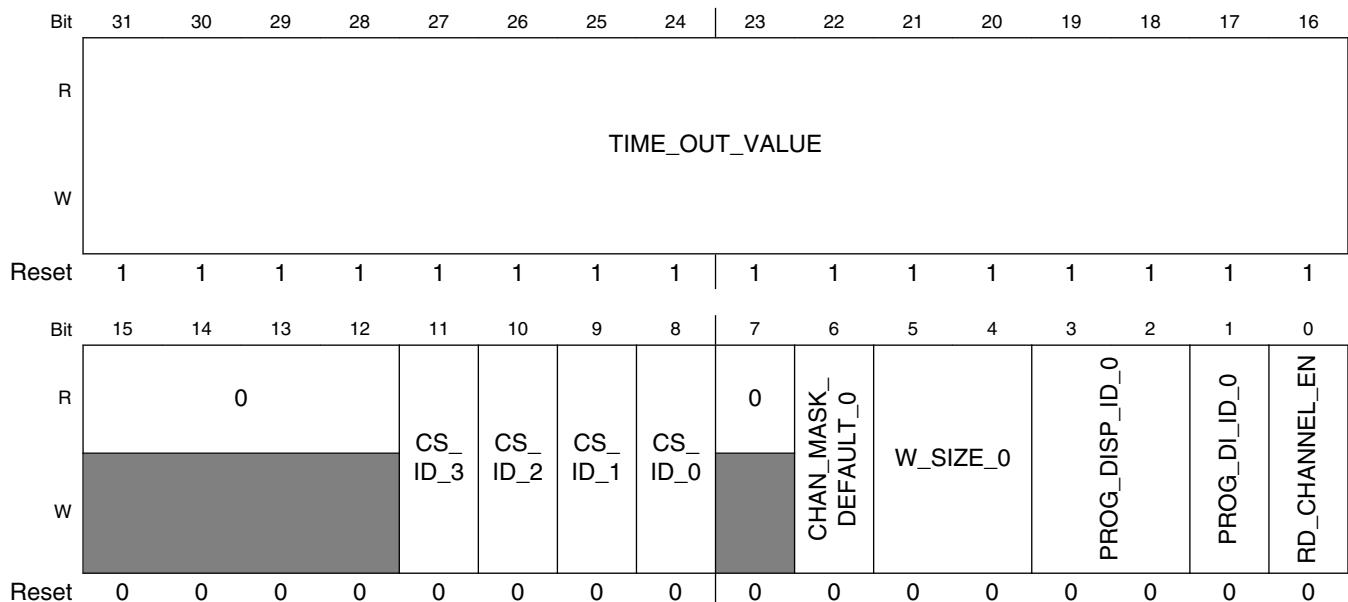
Table continues on the next page...

**IPUx\_SMFC\_BS field descriptions (continued)**

Field	Description
	The value programmed here should be BURST_SIZE-1 (for example: for a burst size of 1, write 0 to these bits)

### 37.5.268 DC Read Channel Configuration Register (IPUx\_DC\_READ\_CH\_CONF)

Address: Base address + 5\_8000h offset

**IPUx\_DC\_READ\_CH\_CONF field descriptions**

Field	Description
31–16 TIME_OUT_VALUE	Time out value. In case of a error during read accesses to the display, where no response from the display was received. A time-out counter will terminate the current access and perform the next command defined in the microcode. This field defines the amount of the hsp_clk cycles counted before the time-out event is issued. This event is tied to the interrupt controller and can generate an error interrupt.
15–12 Reserved	This read-only field is reserved and always has the value 0.
11 CS_ID_3	This bit maps an asynchronous display to a chip select 1 display #3 is connected to CS1 0 display #3 is connected to CS0
10 CS_ID_2	This bit maps an asynchronous display to a chip select 1 display #2 is connected to CS1 0 display #2 is connected to CS0

Table continues on the next page...

**IPUx\_DC\_READ\_CH\_CONF field descriptions (continued)**

Field	Description
9 CS_ID_1	This bit maps an asynchronous display to a chip select  1 display #1 is connected to CS1 0 display #1 is connected to CS0
8 CS_ID_0	This bit maps an asynchronous display to a chip select  1 display #0 is connected to CS1 0 display #0 is connected to CS0
7 Reserved	This read-only field is reserved and always has the value 0.
6 CHAN_MASK_DEFAULT_0	Event mask bit for the read channel  When more than one event is used during a flow (EOF, EOL, NL, NF, EOFIELD, etc.) masks all the event besides the event that is defined as the highest priority event  1 All the events are used - no mask 0 Only the highest priority event is used, the rest are masked
5–4 W_SIZE_0	Word Size  The data coming from the IDMAC is 32bit wide. This field defines the size of the word used by the DC  00 8 bits are used - a 32 bit words includes 4X8bit valid words. 01 16 LSB bits - a 32 bit words includes 2 X16bit valid words. 10 24 MSB bits are used (RGB) - 8 LSB bits are ignored by the DC 11 32 bits are used
3–2 PROG_DISP_ID_0	The field defines which one of the 4 displays can be read.  00 display #0 01 display #1 10 display #2 11 display #3
1 PROG_DI_ID_0	This bit select the DI which a read transaction can be performed through  1 DI #1 0 DI #0
0 RD_CHANNEL_EN	This bit enables the read channel.  1 The Read channel is enabled 0 The Read channel is disabled

### 37.5.269 DC Read Channel Start Address Register (IPUx\_DC\_READ\_SH\_ADDR)

Address: Base address + 5\_8004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

**IPUx\_DC\_READ\_SH\_ADDR field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
ST_ADDR_0	This field defines the start address within the display's memory space where the read transactions will be done from.

### 37.5.270 DC Routine Link Register 0 Channel 0 (IPUx\_DC\_RL0\_CH\_0)

Address: Base address + 5\_8008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NL_START_CHAN_0					0	COD_NL_PRIORITY_CHAN_0		COD_NF_START_CHAN_0					0	COD_NF_PRIORITY_CHAN_0																	
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_RL0\_CH\_0 field descriptions**

Field	Description
31–24 COD_NL_START_CHAN_0	This field is a pointer to the address within the microcode memory where the routine that handles the new line event (NL) resides
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NL_PRIORITY_CHAN_0	This field defines the priority of the new line (NL) event The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_NF_START_CHAN_0	This field is a pointer to the address within the microcode memory where the routine that handles the new Frame event (NF) resides
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NF_PRIORITY_CHAN_0	This field defines the priority of the new frame (NF) event The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2

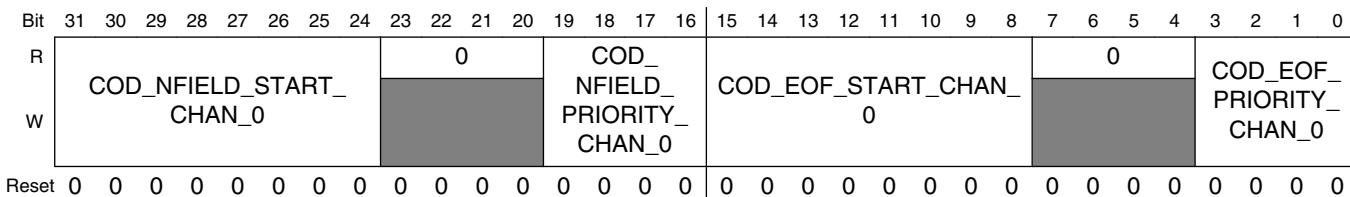
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**IPUx\_DC\_RL0\_CH\_0 field descriptions (continued)**

Field	Description
	1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.271 DC Routine Link Register 1 Channel 0 (IPUx\_DC\_RL1\_CH\_0)

Address: Base address + 5\_800Ch offset

**IPUx\_DC\_RL1\_CH\_0 field descriptions**

Field	Description
31–24 COD_NFIELD_ START_CHAN_0	This field is a pointer to the address within the microcode memory where the routine that handles the new field event resides
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NFIELD_ PRIORITY_ CHAN_0	This field defines the priority of the new field event The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_EOF_ START_CHAN_0	This field is a pointer to the address within the microcode memory where the routine that handles the end-of-frame event (EOF) resides
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOF_ PRIORITY_ CHAN_0	This field defines the priority of the end-of-frame event (EOF) event The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2

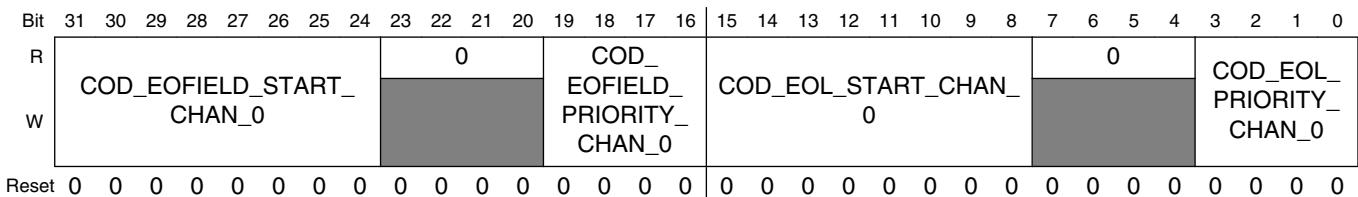
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**IPUx\_DC\_RL1\_CH\_0 field descriptions (continued)**

Field	Description
	1101 Priority #13 (highest)
	1110 Reserved
	1111 Reserved

### 37.5.272 DC Routine Link Register2 Channel 0 (IPUx\_DC\_RL2\_CH\_0)

Address: Base address + 5\_8010h offset

**IPUx\_DC\_RL2\_CH\_0 field descriptions**

Field	Description
31–24 COD_EOFILED_ START_CHAN_0	This field is a pointer to the address within the microcode memory where the routine that handles the end-of-field event resides
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_EOFILED_ PRIORITY_ CHAN_0	This field defines the priority of the end-of-field event The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_EOL_ START_CHAN_0	This field is a pointer to the address within the microcode memory where the routine that handles the end-of-line event (EOL) resides
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOL_ PRIORITY_ CHAN_0	This field defines the priority of the end-of-line event (EOL) event The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2

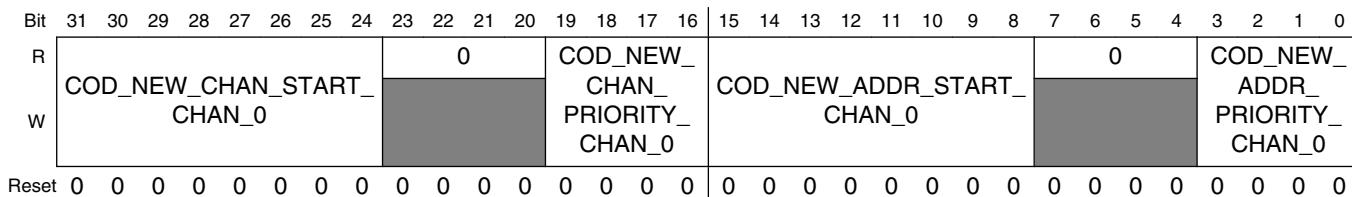
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**IPUx\_DC\_RL2\_CH\_0 field descriptions (continued)**

Field	Description
	1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

**37.5.273 DC Routine Link Register Channel 0  
(IPUx\_DC\_RL3\_CH\_0)**

Address: Base address + 5\_8014h offset

**IPUx\_DC\_RL3\_CH\_0 field descriptions**

Field	Description
31–24 COD_NEW_CHAN_START_CHAN_0	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NEW_CHAN_PRIORITY_CHAN_0	This field defines the priority of the new channel event  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_NEW_ADDR_START_CHAN_0	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ADDR_PRIORITY_CHAN_0	This field defines the priority of the new address event  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable

*Table continues on the next page...*

**IPUx\_DC\_RL3\_CH\_0 field descriptions (continued)**

Field	Description
	0001 Priority #1 (lowest)
	0010 Priority #2
	1101 Priority #13 (highest)
	1110 Reserved
	1111 Reserved

### 37.5.274 DC Routine Link Register 4 Channel 0 (IPUx\_DC\_RL4\_CH\_0)

Address: Base address + 5\_8018h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0									0		COD_NEW_DATA_PRIORITY_CHAN_0				
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_RL4\_CH\_0 field descriptions**

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_DATA_START_CHAN_0	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_DATA_PRIORITY_CHAN_0	This field defines the priority of the new data event  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.275 DC Write Channel 1 Configuration Register (IPUx\_DC\_WR\_CH\_CONF\_1)

Address: Base address + 5\_801Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DC\_WR\_CH\_CONF\_1 field descriptions

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 PROG_START_TIME_1	This field defines the delay between display's vertical synchronization pulse and the start time point of DC's channel 1 window. The delay is defined in pairs of rows. It is used for tearing elimination
15–10 Reserved	This read-only field is reserved and always has the value 0.
9 FIELD_MODE_1	Field mode bit for channel #1 This bit defines if the channel works in field mode or frame mode; This bit is relevant if the flow is sync flow 1 Field mode 0 Frame mode
8 CHAN_MASK_DEFAULT_1	Event mask bit for channel #1 When more than one event is used during a flow (EOF, EOL, NL, NF, EOFIELD, etc.) masks all the event besides the event that is defined as the highest priority event 1 All the events are used - no mask 0 Only the highest priority event is used, the rest are masked
7–5 PROG_CHAN_TYP_1	This field defines the mode of operation of channel #1 000 Disable 001 Reserved

Table continues on the next page...

**IPUx\_DC\_WR\_CH\_CONF\_1 field descriptions (continued)**

Field	Description
	010 Reserved 100 Normal mode without anti-tearing. For sync display this is the only mode allowed 101 Normal mode with anti-tearing 110 Reserved 111 Additional command channel is added to the flow handled by DC channel #1
4–3 PROG_DISP_ID_1	The field defines which one of the 4 displays is associated with channel #1.  00 display #0 01 display #1 10 display #2 11 display #3
2 PROG_DI_ID_1	This bit select the DI which a transaction associated with channel #1 can be performed to  1 DI #1 0 DI #0
W_SIZE_1	Word Size associated with channel #1  The data coming from the IDMAC is 32bit wide. This field defines the size of the word used by the DC  00 8 bits are used - a 32 bit words includes 4X8bit valid words. 01 16 LSB bits - a 32 bit words includes 2 X16bit valid words. 10 24 MSB bits are used (RGB) - 8 LSB bits are ignored by the DC 11 32 bits are used

### 37.5.276 DC Write Channel 1 Address Configuration Register (IPUx\_DC\_WR\_CH\_ADDR\_1)

Address: Base address + 5\_8020h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R	0																																
W																																	

Reset 0

**IPUx\_DC\_WR\_CH\_ADDR\_1 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
ST_ADDR_1	This field defines the start address within the display's memory space where the write transactions will be done to for channel #1.

### 37.5.277 DC Routine Link Register 0 Channel 1 (IPUx\_DC\_RL0\_CH\_1)

Address: Base address + 5\_8024h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NL_START_CHAN_1								0		COD_NL_PRIORITY_CHAN_1		COD_NF_START_CHAN_1		0		COD_NF_PRIORITY_CHAN_1															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_DC\_RL0\_CH\_1 field descriptions

Field	Description
31–24 COD_NL_START_CHAN_1	This field is a pointer to the address within the microcode memory where the routine that handles the new line event resides (associated with channel #1)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NL_PRIORITY_CHAN_1	This field defines the priority of the new line event (associated with channel #1)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_NF_START_CHAN_1	This field is a pointer to the address within the microcode memory where the routine that handles the new frame event resides (associated with channel #1)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NF_PRIORITY_CHAN_1	This field defines the priority of the new frame event (associated with channel #1)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.278 DC Routine Link Register 1 Channel 1 (IPUx\_DC\_RL1\_CH\_1)

Address: Base address + 5\_8028h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																	0		COD_NFIELD_PRIORITY_CHAN_1		COD_EOF_START_CHAN_1		0		COD_EOF_PRIORITY_CHAN_1									
W																																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_DC\_RL1\_CH\_1 field descriptions

Field	Description
31–24 COD_NFIELD_START_CHAN_1	This field is a pointer to the address within the microcode memory where the routine that handles the new field event resides (associated with channel #1)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NFIELD_PRIORITY_CHAN_1	This field defines the priority of the new field event (associated with channel #1)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_EOF_START_CHAN_1	This field is a pointer to the address within the microcode memory where the routine that handles the end of frame event resides (associated with channel #1)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOF_PRIORITY_CHAN_1	This field defines the priority of the end of frame event (associated with channel #1)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.279 DC Routine Link Register 2 Channel 1 (IPUx\_DC\_RL2\_CH\_1)

Address: Base address + 5\_8030h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_EOFIELD_START_CHAN_1								0		COD_EOFIELD_PRIORITY_CHAN_1				0		COD_EOL_START_CHAN_1				0		COD_EOL_PRIORITY_CHAN_1									
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL2\_CH\_1 field descriptions

Field	Description
31–24 COD_EOFIELD_START_CHAN_1	This field is a pointer to the address within the microcode memory where the routine that handles the end of field event resides (associated with channel #1)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_EOFIELD_PRIORITY_CHAN_1	<p>This field defines the priority of the end of field event (associated with channel #1)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <ul style="list-style-type: none"> <li>0000 disable</li> <li>0001 Priority #1 (lowest)</li> <li>0010 Priority #2</li> <li>1101 Priority #13 (highest)</li> <li>1110 Reserved</li> <li>1111 Reserved</li> </ul>
15–8 COD_EOL_START_CHAN_1	This field is a pointer to the address within the microcode memory where the routine that handles the end of line event resides (associated with channel #1)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOL_PRIORITY_CHAN_1	<p>This field defines the priority of the end of line event (associated with channel #1)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <ul style="list-style-type: none"> <li>0000 disable</li> <li>0001 Priority #1 (lowest)</li> <li>0010 Priority #2</li> <li>1101 Priority #13 (highest)</li> <li>1110 Reserved</li> <li>1111 Reserved</li> </ul>

### 37.5.280 DC Routine Link Register 3 Channel 1 (IPUx\_DC\_RL3\_CH\_1)

Address: Base address + 5\_8032h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																0		COD_NEW_															
	COD_NEW_CHAN_START_																CHAN_1																
W																																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL3\_CH\_1 field descriptions

Field	Description
31–24 COD_NEW_ CHAN_START_ CHAN_1	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #1)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NEW_ CHAN_ PRIORITY_ CHAN_1	This field defines the priority of the new channel event (associated with channel #1)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_NEW_ ADDR_START_ CHAN_1	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #1)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ ADDR_ PRIORITY_ CHAN_1	This field defines the priority of the new address event (associated with channel #1)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.281 DC Routine Link Register 4 Channel 1 (IPUx\_DC\_RL4\_CH\_1)

Address: Base address + 5\_8034h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0																
W																		COD_NEW_DATA_START_CHAN_1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

#### IPUx\_DC\_RL4\_CH\_1 field descriptions

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ DATA_START_ CHAN_1	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #1)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ DATA_ PRIORITY_ CHAN_1	<p>This field defines the priority of the new data event (associated with channel #1)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <p>0000 disable      0001 Priority #1 (lowest)      0010 Priority #2      1101 Priority #13 (highest)      1110 Reserved      1111 Reserved</p>

### 37.5.282 DC Write Channel 2 Configuration Register (IPUx\_DC\_WR\_CH\_CONF\_2)

Address: Base address + 5\_8038h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DC\_WR\_CH\_CONF\_2 field descriptions

Field	Description														
31–27 Reserved	This read-only field is reserved and always has the value 0.														
26–16 PROG_START_TIME_2	This field defines the delay between display's vertical synchronization pulse and the start time point of DC's channel 2 window. The delay is defined in pairs of rows. It is used for tearing elimination														
15–9 Reserved	This read-only field is reserved and always has the value 0.														
8 CHAN_MASK_DEFAULT_2	<p>Event mask bit for channel #2</p> <p>When more than one event is used during a flow (EOF, EOL, NL, NF, EOFIELD, etc.) masks all the event besides the event that is defined as the highest priority event</p> <table> <tr> <td>1</td> <td>All the events are used - no mask</td> </tr> <tr> <td>0</td> <td>Only the highest priority event is used, the rest are masked</td> </tr> </table>	1	All the events are used - no mask	0	Only the highest priority event is used, the rest are masked										
1	All the events are used - no mask														
0	Only the highest priority event is used, the rest are masked														
7–5 PROG_CHAN_TYP_2	<p>This field defines the mode of operation of channel #2</p> <table> <tr> <td>000</td> <td>Disable</td> </tr> <tr> <td>001</td> <td>Reserved</td> </tr> <tr> <td>010</td> <td>Reserved</td> </tr> <tr> <td>100</td> <td>Normal mode without anti-tearing. For sync display this is the only mode allowed</td> </tr> <tr> <td>101</td> <td>Normal mode with anti-tearing</td> </tr> <tr> <td>110</td> <td>Reserved</td> </tr> <tr> <td>111</td> <td>Additional command channel is added to the flow handled by DC channel #2</td> </tr> </table>	000	Disable	001	Reserved	010	Reserved	100	Normal mode without anti-tearing. For sync display this is the only mode allowed	101	Normal mode with anti-tearing	110	Reserved	111	Additional command channel is added to the flow handled by DC channel #2
000	Disable														
001	Reserved														
010	Reserved														
100	Normal mode without anti-tearing. For sync display this is the only mode allowed														
101	Normal mode with anti-tearing														
110	Reserved														
111	Additional command channel is added to the flow handled by DC channel #2														

Table continues on the next page...

**IPUx\_DC\_WR\_CH\_CONF\_2 field descriptions (continued)**

Field	Description
4–3 PROG_DISP_ID_2	The field defines which one of the 4 displays is associated with channel #2.  00 display #0 01 display #1 10 display #2 11 display #3
2 PROG_DI_ID_2	This bit select the DI which a transaction associated with channel #2 can be performed to  1 DI #1 0 DI #0
W_SIZE_2	Word Size  The data coming from the IDMAC is 32bit wide. This field defines the size of the word used by the DC  00 8 bits are used - a 32 bit words includes 4X8bit valid words. 01 16 LSB bits - a 32 bit words includes 2 X16bit valid words. 10 24 MSB bits are used (RGB) - 8 LSB bits are ignored by the DC 11 32 bits are used

**37.5.283 DC Write Channel 2 Address Configuration Register (IPUx\_DC\_WR\_CH\_ADDR\_2)**

Address: Base address + 5\_803Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_WR\_CH\_ADDR\_2 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
ST_ADDR_2	This field defines the start address within the display's memory space where the write transactions will be done to for channel #2.

### 37.5.284 DC Routine Link Register 0 Channel 2 (IPUx\_DC\_RL0\_CH\_2)

Address: Base address + 5\_8040h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NL_START_CHAN_2										0	COD_NL_PRIORITY_CHAN_2				COD_NF_START_CHAN_2										0	COD_NF_PRIORITY_CHAN_2					
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_DC\_RL0\_CH\_2 field descriptions

Field	Description
31–24 COD_NL_ START_CHAN_2	This field is a pointer to the address within the microcode memory where the routine that handles the new line event resides (associated with channel #2)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NL_ PRIORITY_ CHAN_2	This field defines the priority of the new line event (associated with channel #2)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_NF_ START_CHAN_2	This field is a pointer to the address within the microcode memory where the routine that handles the new frame event resides (associated with channel #2)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NF_ PRIORITY_ CHAN_2	This field defines the priority of the new frame event (associated with channel #2)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.285 DC Routine Link Register 1 Channel 2 (IPUx\_DC\_RL1\_CH\_2)

Address: Base address + 5\_8044h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0		COD_NFIELD_PRIORITY_CHAN_2		COD_EOF_START_CHAN_2		0		COD_EOF_PRIORITY_CHAN_2								
W																																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL1\_CH\_2 field descriptions

Field	Description
31–24 COD_NFIELD_START_CHAN_2	This field is a pointer to the address within the microcode memory where the routine that handles the new field event resides (associated with channel #2)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NFIELD_PRIORITY_CHAN_2	This field defines the priority of the new field event (associated with channel #2)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_EOF_START_CHAN_2	This field is a pointer to the address within the microcode memory where the routine that handles the end of frame event resides (associated with channel #2)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOF_PRIORITY_CHAN_2	This field defines the priority of the end of frame event (associated with channel #2)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.286 DC Routine Link Register 2 Channel 2 (IPUx\_DC\_RL2\_CH\_2)

Address: Base address + 5\_8048h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_EOFIELD_START_CHAN_2										0	COD_EOFIELD_PRIORITY_CHAN_2				COD_EOL_START_CHAN_2					0	COD_EOL_PRIORITY_CHAN_2										
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_DC\_RL2\_CH\_2 field descriptions

Field	Description
31–24 COD_EOFIELD_START_CHAN_2	This field is a pointer to the address within the microcode memory where the routine that handles the end of field event resides (associated with channel #2)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_EOFIELD_PRIORITY_CHAN_2	<p>This field defines the priority of the end of field event (associated with channel #2)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <ul style="list-style-type: none"> <li>0000 disable</li> <li>0001 Priority #1 (lowest)</li> <li>0010 Priority #2</li> <li>1101 Priority #13 (highest)</li> <li>1110 Reserved</li> <li>1111 Reserved</li> </ul>
15–8 COD_EOL_START_CHAN_2	This field is a pointer to the address within the microcode memory where the routine that handles the end of line event resides (associated with channel #2)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOL_PRIORITY_CHAN_2	<p>This field defines the priority of the end of line event (associated with channel #2)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <ul style="list-style-type: none"> <li>0000 disable</li> <li>0001 Priority #1 (lowest)</li> <li>0010 Priority #2</li> <li>1101 Priority #13 (highest)</li> <li>1110 Reserved</li> <li>1111 Reserved</li> </ul>

### 37.5.287 DC Routine Link Register 3 Channel 2 (IPUx\_DC\_RL3\_CH\_2)

Address: Base address + 5\_804Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																0		COD_NEW_															
	COD_NEW_CHAN_START_																CHAN_	PRIORITY_															
W	CHAN_2																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL3\_CH\_2 field descriptions

Field	Description
31–24 COD_NEW_ CHAN_START_ CHAN_2	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #2)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NEW_ CHAN_ PRIORITY_ CHAN_2	This field defines the priority of the end of line event (associated with channel #2)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_NEW_ ADDR_START_ CHAN_2	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #2)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ ADDR_ PRIORITY_ CHAN_2	This field defines the priority of the end of line event (associated with channel #2)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.288 DC Routine Link Register 4 Channel 2 (IPUx\_DC\_RL4\_CH\_2)

Address: Base address + 5\_8050h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W																		COD_NEW_DATA_START_CHAN_2														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL4\_CH\_2 field descriptions

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ DATA_START_ CHAN_2	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #2)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ DATA_ PRIORITY_ CHAN_2	This field defines the priority of the end of line event (associated with channel #2)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.289 DC Command Channel 3 Configuration Register (IPUx\_DC\_CMD\_CH\_CONF\_3)

Address: Base address + 5\_8054h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									COD_CMND_START_CHAN_RS1_3				0			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									COD_CMND_START_CHAN_RS0_3				0			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DC\_CMD\_CH\_CONF\_3 field descriptions**

Field	Description
31–24 COD_CMND_ START_CHAN_ RS1_3	This field is a pointer to the address within the microcode memory where the routine that handles the command start event resides (associated with channel #3); This field is relevant when RS is equal to 1
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_CMND_ START_CHAN_ RS0_3	This field is a pointer to the address within the microcode memory where the routine that handles the command start event resides (associated with channel #3); This field is relevant when RS is equal to 0
7–2 Reserved	This read-only field is reserved and always has the value 0.
W_SIZE_3	Word Size associated with channel #3  The data coming from the IDMAC is 32bit wide. This field defines the size of the word used by the DC  00 8 bits are used - a 32 bit words includes 4X8bit valid words. 01 16 LSB bits - a 32 bit words includes 2 X16bit valid words. 10 24 MSB bits are used (RGB) - 8 LSB bits are ignored by the DC 11 32 bits are used

**37.5.290 DC Command Channel 4 Configuration Register  
(IPUx\_DC\_CMD\_CH\_CONF\_4)**

Address: Base address + 5\_8058h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	COD_CMND_START_CHAN_RS1_4								0							
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_CMND_START_CHAN_RS0_4								0				W_SIZE_4			
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DC\_CMD\_CH\_CONF\_4 field descriptions**

Field	Description
31–24 COD_CMND_ START_CHAN_ RS1_4	This field is a pointer to the address within the microcode memory where the routine that handles the command start event resides (associated with channel #4); This field is relevant when RS is equal to 1
23–16 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_DC\_CMD\_CH\_CONF\_4 field descriptions (continued)**

Field	Description
15–8 COD_CMND_ START_CHAN_ RS0_4	This field is a pointer to the address within the microcode memory where the routine that handles the command start event resides (associated with channel #4); This field is relevant when RS is equal to 0
7–2 Reserved	This read-only field is reserved and always has the value 0.
W_SIZE_4	Word Size associated with channel #4  The data coming from the IDMAC is 32bit wide. This field defines the size of the word used by the DC  00 8 bits are used - a 32 bit words includes 4X8bit valid words. 01 16 LSB bits - a 32 bit words includes 2 X16bit valid words. 10 24 MSB bits are used (RGB) - 8 LSB bits are ignored by the DC 11 32 bits are used

### 37.5.291 DC Write Channel 5 Configuration Register (IPUx\_DC\_WR\_CH\_CONF\_5)

Address: Base address + 5\_805Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	R	0				PROG_START_TIME_5										
	W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R	0				FIELD_MODE_5	CHAN_MASK_DEFAULT_5	PROG_CHAN_TYP_5			PROG_DISP_ID_5			PROG_DL_ID_5	W_SIZE_5	
	W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DC\_WR\_CH\_CONF\_5 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 PROG_START_ TIME_5	This field defines the delay between display's vertical synchronization pulse and the start time point of DC's channel 5 window. The delay is defined in pairs of rows. It is used for tearing elimination

Table continues on the next page...

**IPUx\_DC\_WR\_CH\_CONF\_5 field descriptions (continued)**

Field	Description
15–10 Reserved	This read-only field is reserved and always has the value 0.
9 FIELD_MODE_5	Field mode bit for channel #5 This bit defines if the channel works in field mode or frame mode; This bit is relevant if the flow is sync flow 1 Field mode 0 Frame mode
8 CHAN_MASK_DEFAULT_5	Event mask bit for channel #5 When more than one event is used during a flow (EOF, EOL, NL, NF, EOFIELD, etc.) masks all the event besides the event that is defined as the highest priority event 1 All the events are used - no mask 0 Only the highest priority event is used, the rest are masked
7–5 PROG_CHAN_TYP_5	This field define the mode of operation of channel #5 000 Disable 001 Reserved 010 Reserved 100 Normal mode without anti-tearing. For sync display this is the only mode allowed 101 Normal mode with anti-tearing 110 Reserved 111 Additional command channel is added to the flow handled by DC channel #5
4–3 PROG_DISP_ID_5	The field defines which one of the 4 displays is associated with channel #5. 00 display #0 01 display #1 10 display #2 11 display #3
2 PROG_DI_ID_5	This bit select the DI which a transaction associated with channel #5 can be performed to. When channel 28 is connected to DI0, channel 23 must be connected to DI1 even if ch23 is not used. This is done by writing 1 to this bit. 1 DI #1 0 DI #0
W_SIZE_5	Word Size associated with channel #5 The data coming from the IDMAC is 32bit wide. This field defines the size of the word used by the DC 00 8 bits are used - a 32 bit words includes 4X8bit valid words. 01 16 LSB bits - a 32 bit words includes 2 X16bit valid words. 10 24 MSB bits are used (RGB) - 8 LSB bits are ignored by the DC 11 32 bits are used

### 37.5.292 DC Write Channel 5Address Configuration Register (IPUx\_DC\_WR\_CH\_ADDR\_5)

Address: Base address + 5\_8060h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_WR\_CH\_ADDR\_5 field descriptions

Field	Description																												
31–29 Reserved	This read-only field is reserved and always has the value 0.																												
ST_ADDR_5	This field defines the start address within the display's memory space where the write transactions will be done to for channel #5.																												

### 37.5.293 DC Routine Link Register 0 Channel 5 (IPUx\_DC\_RL0\_CH\_5)

Address: Base address + 5\_8064h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0		COD_NL_PRIORITY_CHAN_5														
W																																	

Reset 0

#### IPUx\_DC\_RL0\_CH\_5 field descriptions

Field	Description																												
31–24 COD_NL_START_CHAN_5	This field is a pointer to the address within the microcode memory where the routine that handles the new line event resides (associated with channel #5)																												
23–20 Reserved	This read-only field is reserved and always has the value 0.																												
19–16 COD_NL_PRIORITY_CHAN_5	This field defines the priority of the new line event (associated with channel #5)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved																												

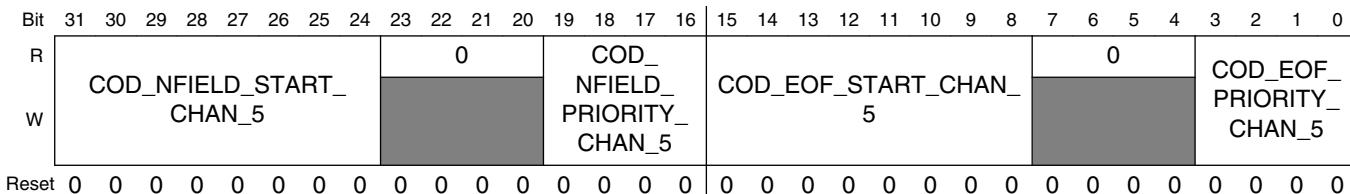
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**IPUx\_DC\_RL0\_CH\_5 field descriptions (continued)**

Field	Description
15–8 COD_NF_ START_CHAN_5	This field is a pointer to the address within the microcode memory where the routine that handles the new frame event resides (associated with channel #5)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NF_ PRIORITY_ CHAN_5	This field defines the priority of the new line event (associated with channel #5)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.294 DC Routine Link Register 1 Channel 5 (IPUx\_DC\_RL1\_CH\_5)

Address: Base address + 5\_8068h offset

**IPUx\_DC\_RL1\_CH\_5 field descriptions**

Field	Description
31–24 COD_NFIELD_ START_CHAN_5	This field is a pointer to the address within the microcode memory where the routine that handles the new field event resides (associated with channel #5)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NFIELD_ PRIORITY_ CHAN_5	This field defines the priority of the new line event (associated with channel #5)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

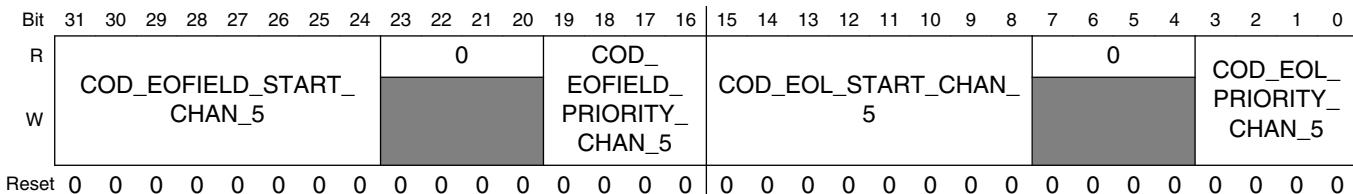
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**IPUx\_DC\_RL1\_CH\_5 field descriptions (continued)**

Field	Description
15–8 COD_EOF_ START_CHAN_5	This field is a pointer to the address within the microcode memory where the routine that handles the end of frame event resides (associated with channel #5)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOF_ PRIORITY_ CHAN_5	This field defines the priority of the new line event (associated with channel #5)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.295 DC Routine Link Register 2 Channel 5 (IPUx\_DC\_RL2\_CH\_5)

Address: Base address + 5\_806Ch offset

**IPUx\_DC\_RL2\_CH\_5 field descriptions**

Field	Description
31–24 COD_EOFIELD_ START_CHAN_5	This field is a pointer to the address within the microcode memory where the routine that handles the end of field event resides (associated with channel #5)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_EOFIELD_ PRIORITY_ CHAN_5	This field defines the priority of the new line event (associated with channel #5)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

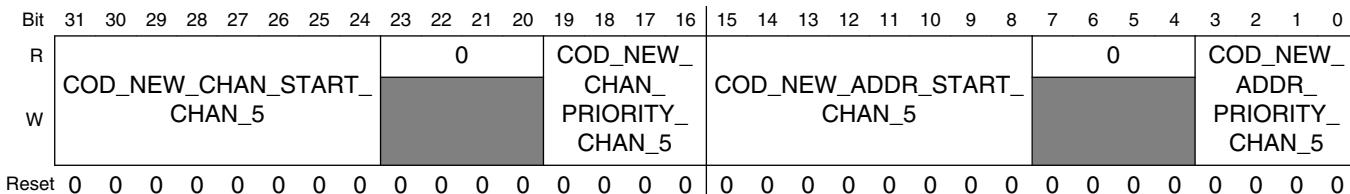
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**IPUx\_DC\_RL2\_CH\_5 field descriptions (continued)**

Field	Description
15–8 COD_EOL_ START_CHAN_5	This field is a pointer to the address within the microcode memory where the routine that handles the end of line event resides (associated with channel #5)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOL_ PRIORITY_ CHAN_5	This field defines the priority of the new line event (associated with channel #5)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

**37.5.296 DC Routine Link Register3 Channel 5  
(IPUx\_DC\_RL3\_CH\_5)**

Address: Base address + 5\_8070h offset

**IPUx\_DC\_RL3\_CH\_5 field descriptions**

Field	Description
31–24 COD_NEW_ CHAN_START_ CHAN_5	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #5)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NEW_ CHAN_ PRIORITY_ CHAN_5	This field defines the priority of the new line event (associated with channel #5)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest)

Table continues on the next page...

**IPUx\_DC\_RL3\_CH\_5 field descriptions (continued)**

Field	Description
	1110 Reserved 1111 Reserved
15–8 COD_NEW_ ADDR_START_ CHAN_5	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #5)
7–4 Reserved	This read-only field is reserved and always has the value 0.

### 37.5.297 DC Routine Link Register 4 Channel 5 (IPUx\_DC\_RL4\_CH\_5)

Address: Base address + 5\_8074h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																0									0				COD_NEW_ DATA_ PRIORITY_ CHAN_5			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_RL4\_CH\_5 field descriptions**

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ DATA_START_ CHAN_5	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #5)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ DATA_ PRIORITY_ CHAN_5	This field defines the priority of the new line event (associated with channel #5) The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)

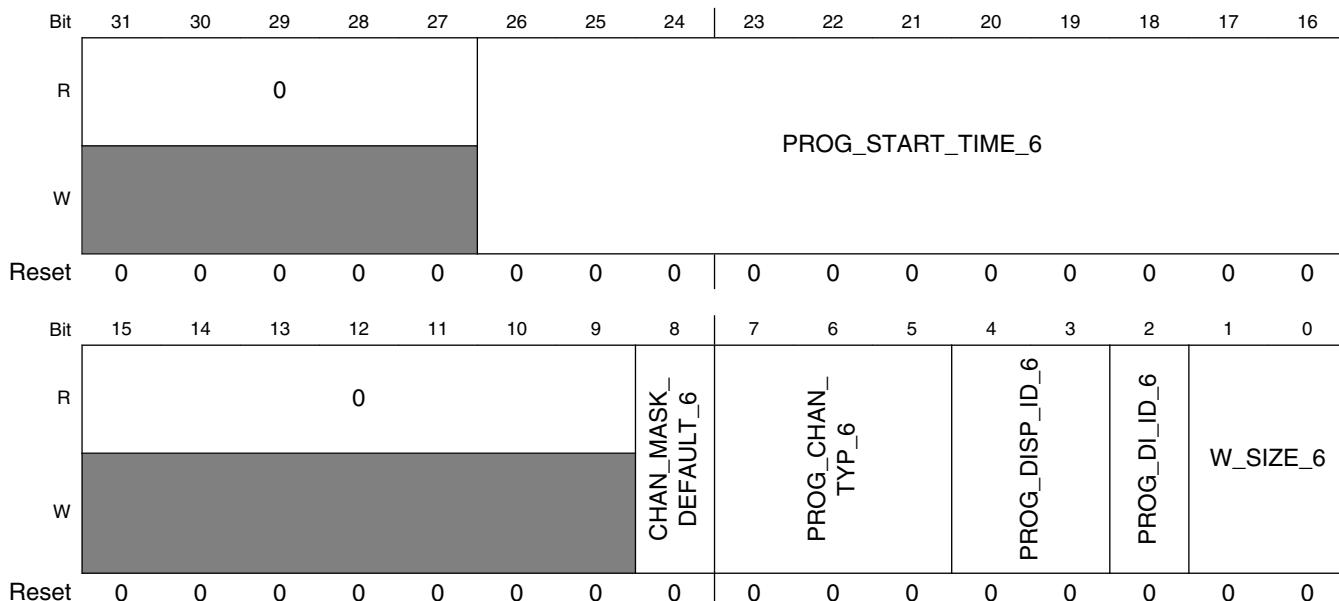
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**IPUx\_DC\_RL4\_CH\_5 field descriptions (continued)**

Field	Description
	0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

**37.5.298 DC Write Channel 6 Configuration Register (IPUx\_DC\_WR\_CH\_CONF\_6)**

Address: Base address + 5\_8078h offset

**IPUx\_DC\_WR\_CH\_CONF\_6 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 PROG_START_TIME_6	This field defines the delay between display's vertical synchronization pulse and the start time point of DC's channel 6 window. The delay is defined in pairs of rows. It is used for tearing elimination
15–9 Reserved	This read-only field is reserved and always has the value 0.
8 CHAN_MASK_DEFAULT_6	Event mask bit for channel #6 When more than one event is used during a flow (EOF, EOL, NL, NF, EOFIELD, etc.) masks all the event besides the event that is defined as the highest priority event

*Table continues on the next page...*

**IPUx\_DC\_WR\_CH\_CONF\_6 field descriptions (continued)**

Field	Description
	1 All the events are used - no mask 0 Only the highest priority event is used, the rest are masked
7–5 PROG_CHAN_ TYP_6	This field define the mode of operation of channel #6 000 Disable 001 Reserved 010 Reserved 100 Normal mode without anti-tearing. For sync display this is the only mode allowed 101 Normal mode with anti-tearing 110 Reserved 111 Additional command channel is added to the flow handled by DC channel #6
4–3 PROG_DISP_ ID_6	The field defines which one of the 4 displays is associated with channel #6. 00 display #0 01 display #1 10 display #2 11 display #3
2 PROG_DI_ID_6	This bit select the DI which a transaction associated with channel #6 can be performed to 1 DI #1 0 DI #0
W_SIZE_6	Word Size associated with channel #6 The data coming from the IDMAC is 32bit wide. This field defines the size of the word used by the DC 00 8 bits are used - a 32 bit words includes 4X8bit valid words. 01 16 LSB bits - a 32 bit words includes 2 X16bit valid words. 10 24 MSB bits are used (RGB) - 8 LSB bits are ignored by the DC 11 32 bits are used

### 37.5.299 DC Write Channel 6 Address Configuration Register (IPUx\_DC\_WR\_CH\_ADDR\_6)

Address: Base address + 5\_807Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

**IPUx\_DC\_WR\_CH\_ADDR\_6 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
ST_ADDR_6	This field defines the start address within the display's memory space where the write transactions will be done to for channel #6.

### 37.5.300 DC Routine Link Register 0Channel 6 (IPUx\_DC\_RL0\_CH\_6)

Address: Base address + 5\_8080h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NL_START_CHAN_6								0		COD_NL_PRIORITY_CHAN_6		COD_NF_START_CHAN_6								0		COD_NF_PRIORITY_CHAN_6									
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DC\_RL0\_CH\_6 field descriptions

Field	Description
31–24 COD_NL_START_CHAN_6	This field is a pointer to the address within the microcode memory where the routine that handles the new line event resides (associated with channel #6)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NL_PRIORITY_CHAN_6	This field defines the priority of the new line event (associated with channel #6)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_NF_START_CHAN_6	This field is a pointer to the address within the microcode memory where the routine that handles the new frame event resides (associated with channel #6)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NF_PRIORITY_CHAN_6	This field defines the priority of the new frame event (associated with channel #6)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.301 DC Routine Link Register 1 Channel 6 (IPUx\_DC\_RL1\_CH\_6)

Address: Base address + 5\_8084h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																	0																
W																	COD_NFIELD_PRIORITY_CHAN_6																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

#### IPUx\_DC\_RL1\_CH\_6 field descriptions

Field	Description
31–24 COD_NFIELD_START_CHAN_6	This field is a pointer to the address within the microcode memory where the routine that handles the new field event resides (associated with channel #6)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NFIELD_PRIORITY_CHAN_6	<p>This field defines the priority of the new field event (associated with channel #6)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <ul style="list-style-type: none"> <li>0000 disable</li> <li>0001 Priority #1 (lowest)</li> <li>0010 Priority #2</li> <li>1101 Priority #13 (highest)</li> <li>1110 Reserved</li> <li>1111 Reserved</li> </ul>
15–8 COD_EOF_START_CHAN_6	This field is a pointer to the address within the microcode memory where the routine that handles the end of frame event resides (associated with channel #6)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOF_PRIORITY_CHAN_6	<p>This field defines the priority of the new field event (associated with channel #6)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <ul style="list-style-type: none"> <li>0000 disable</li> <li>0001 Priority #1 (lowest)</li> <li>0010 Priority #2</li> <li>1101 Priority #13 (highest)</li> <li>1110 Reserved</li> <li>1111 Reserved</li> </ul>

### 37.5.302 DC Routine Link Register 2 Channel 6 (IPUx\_DC\_RL2\_CH\_6)

Address: Base address + 5\_8088h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_EOFIELD_START_CHAN_6								0		COD_EOFIELD_PRIORITY_CHAN_6		COD_EOL_START_CHAN_6								0		COD_EOL_PRIORITY_CHAN_6									
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL2\_CH\_6 field descriptions

Field	Description
31–24 COD_EOFIELD_START_CHAN_6	This field is a pointer to the address within the microcode memory where the routine that handles the end of field event resides (associated with channel #6)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_EOFIELD_PRIORITY_CHAN_6	<p>This field defines the priority of the new field event (associated with channel #6)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <ul style="list-style-type: none"> <li>0000 disable</li> <li>0001 Priority #1 (lowest)</li> <li>0010 Priority #2</li> <li>1101 Priority #13 (highest)</li> <li>1110 Reserved</li> <li>1111 Reserved</li> </ul>
15–8 COD_EOL_START_CHAN_6	This field is a pointer to the address within the microcode memory where the routine that handles the end of line event resides (associated with channel #6)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_EOL_PRIORITY_CHAN_6	<p>This field defines the priority of the new field event (associated with channel #6)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <ul style="list-style-type: none"> <li>0000 disable</li> <li>0001 Priority #1 (lowest)</li> <li>0010 Priority #2</li> <li>1101 Priority #13 (highest)</li> <li>1110 Reserved</li> <li>1111 Reserved</li> </ul>

### 37.5.303 DC Routine Link Register 3 Channel 6 (IPUx\_DC\_RL3\_CH\_6)

Address: Base address + 5\_808Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R																0		COD_NEW_																
	COD_NEW_CHAN_START_															CHAN_6																		
W																																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

#### IPUx\_DC\_RL3\_CH\_6 field descriptions

Field	Description
31–24 COD_NEW_ CHAN_START_ CHAN_6	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #6)
23–20 Reserved	This read-only field is reserved and always has the value 0.
19–16 COD_NEW_ CHAN_ PRIORITY_ CHAN_6	This field defines the priority of the new field event (associated with channel #6)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
15–8 COD_NEW_ ADDR_START_ CHAN_6	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #6)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ ADDR_ PRIORITY_ CHAN_6	This field defines the priority of the new field event (associated with channel #6)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.304 DC Routine Link Register 4 Channel 6 (IPUx\_DC\_RL4\_CH\_6)

Address: Base address + 5\_8090h offset

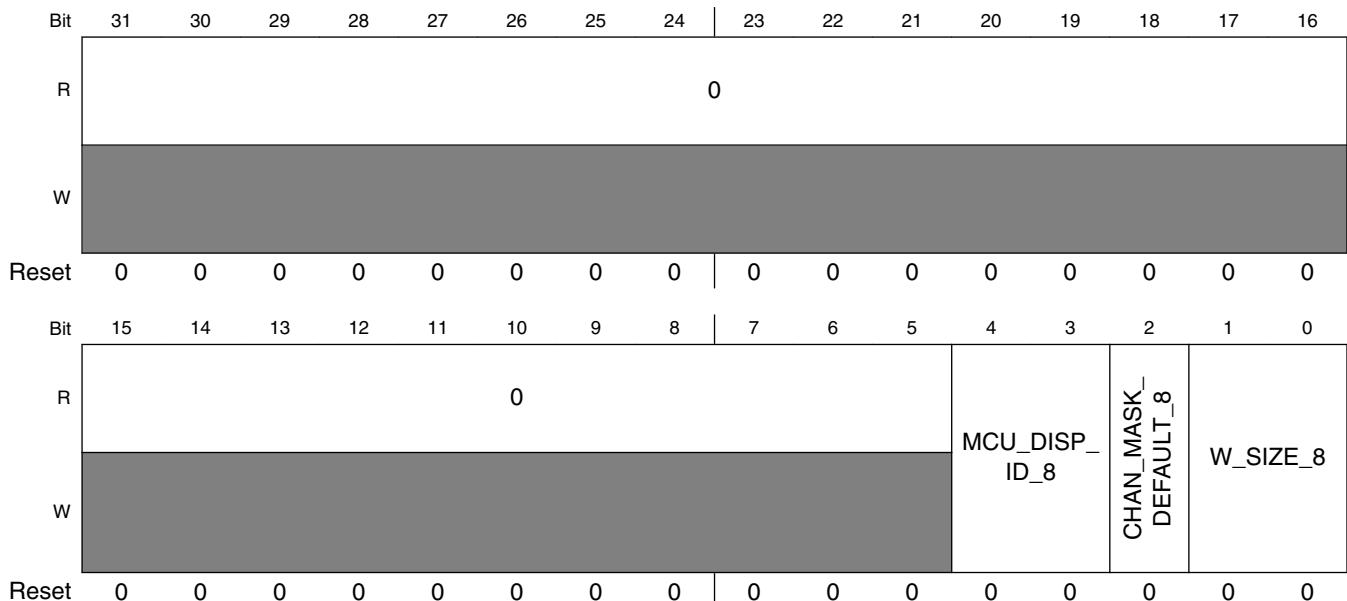
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W																			COD_NEW_DATA_START_CHAN_6				0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL4\_CH\_6 field descriptions

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ DATA_START_ CHAN_6	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #6)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ DATA_ PRIORITY_ CHAN_6	This field defines the priority of the new field event (associated with channel #6)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.305 DC Write Channel 8 Configuration 1 Register (IPUx\_DC\_WR\_CH\_CONF1\_8)

Address: Base address + 5\_8094h offset



#### IPUx\_DC\_WR\_CH\_CONF1\_8 field descriptions

Field	Description
31–5 Reserved	This read-only field is reserved and always has the value 0.
4–3 MCU_DISP_ID_8	The field defines which one of the 4 displays is associated with channel #8.  00 display #0 01 display #1 10 display #2 11 display #3
2 CHAN_MASK_DEFAULT_8	Event mask bit for channel #8  When more than one event is used during a flow (EOF, EOL, NL, NF, EOFIELD, etc.) masks all the events besides the event that is defined as the highest priority event  1 All the events are used - no mask 0 Only the highest priority event is used, the rest are masked
W_SIZE_8	Word Size associated with channel #8  The data coming from the IDMAC is 32bit wide. This field defines the size of the word used by the DC  00 8 bits are used - a 32 bit words includes 4X8bit valid words. 01 16 LSB bits - a 32 bit words includes 2 X16bit valid words. 10 24 MSB bits are used (RGB) - 8 LSB bits are ignored by the DC 11 32 bits are used

### 37.5.306 DC Write Channel 8 Configuration 2 Register (IPUx\_DC\_WR\_CH\_CONF2\_8)

Address: Base address + 5\_8098h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_WR\_CH\_CONF2\_8 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
NEW_ADDR_SPACE_SA_8	Channel #8 is used for ARM platform direct access to the display. This field defines the base address of the second region accessible on the display

### 37.5.307 DC Routine Link Register 1 Channel 8 (IPUx\_DC\_RL1\_CH\_8)

Address: Base address + 5\_809Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W	COD_NEW_ADDR_START_CHAN_W_8_1																0															

Reset 0

#### IPUx\_DC\_RL1\_CH\_8 field descriptions

Field	Description
31–24 COD_NEW_ADDR_START_CHAN_W_8_1	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #8, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ADDR_START_CHAN_W_8_0	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #8, first region)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ADDR_	This field defines the priority of the new address event (associated with channel #8, both regions)

Table continues on the next page...

**IPUx\_DC\_RL1\_CH\_8 field descriptions (continued)**

Field	Description
PRIORITY_CHAN_8	The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.308 DC Routine Link Register 2 Channel 8 (IPUx\_DC\_RL2\_CH\_8)

Address: Base address + 5\_80A0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NEW_CHAN_START_CHAN_W_8_1								0								0								COD_NEW_CHAN_PRIORITY_CHAN_8							
W	COD_NEW_CHAN_START_CHAN_W_8_1								0								0								0							

**IPUx\_DC\_RL2\_CH\_8 field descriptions**

Field	Description
31–24 COD_NEW_CHAN_START_CHAN_W_8_1	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #8, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_CHAN_START_CHAN_W_8_0	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #8, first region)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_CHAN_PRIORITY_CHAN_8	This field defines the priority of the new address event (associated with channel #8, both regions)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.309 DC Routine Link Register 3 Channel 8 (IPUx\_DC\_RL3\_CH\_8)

Address: Base address + 5\_80A4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W	COD_NEW_DATA_START_CHAN_W_8_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL3\_CH\_8 field descriptions

Field	Description
31–24 COD_NEW_ DATA_START_ CHAN_W_8_1	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #8,second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ DATA_START_ CHAN_W_8_0	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #8, first region)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ DATA_ PRIORITY_ CHAN_8	This field defines the priority of the new address event (associated with channel #8, both regions)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.310 DC Routine Link Register 4 Channel 8 (IPUx\_DC\_RL4\_CH\_8)

Address: Base address + 5\_80A8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																	0															
W	COD_NEW_ADDR_START_CHAN_R_8_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_RL4\_CH\_8 field descriptions**

Field	Description
31–24 COD_NEW_ ADDR_START_ CHAN_R_8_1	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #8, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ ADDR_START_ CHAN_R_8_0	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #8, first region)
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.311 DC Routine Link Register 5 Channel 8 (IPUx\_DC\_RL5\_CH\_8)

Address: Base address + 5\_80ACh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NEW_CHAN_START_ CHAN_R_8_1																COD_NEW_CHAN_START_ CHAN_R_8_0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_RL5\_CH\_8 field descriptions**

Field	Description
31–24 COD_NEW_ CHAN_START_ CHAN_R_8_1	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #8, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ CHAN_START_ CHAN_R_8_0	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #8, first region)
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.312 DC Routine Link Register 6 Channel 8 (IPUx\_DC\_RL6\_CH\_8)

Address: Base address + 5\_80B0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R	COD_NEW_DATA_START_																COD_NEW_DATA_START_																	
W	CHAN_R_8_1																CHAN_R_8_0																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

#### IPUx\_DC\_RL6\_CH\_8 field descriptions

Field	Description
31–24 COD_NEW_ DATA_START_ CHAN_R_8_1	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #8, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ DATA_START_ CHAN_R_8_0	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #8, first region)
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.313 DC Write Channel 9 Configuration 1 Register (IPUx\_DC\_WR\_CH\_CONF1\_9)

Address: Base address + 5\_80B4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16																			
R																	0																		
W																																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																			
R																	0																		
W																																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

**IPUx\_DC\_WR\_CH\_CONF1\_9 field descriptions**

Field	Description
31–5 Reserved	This read-only field is reserved and always has the value 0.
4–3 MCU_DISP_ID_9	The field defines which one of the 4 displays is associated with channel #9. 00 display #0 01 display #1 10 display #2 11 display #3
2 CHAN_MASK_DEFAULT_9	Event mask bit for channel #9 When more than one event is used during a flow (EOF, EOL, NL, NF, EOFIELD, etc.) masks all the event besides the event that is defined as the highest priority event 1 All the events are used - no mask 0 Only the highest priority event is used, the rest are masked
W_SIZE_9	Word Size associated with channel #9 The data coming from the IDMAC is 32bit wide. This field defines the size of the word used by the DC 00 8 bits are used - a 32 bit words includes 4X8bit valid words. 01 16 LSB bits - a 32 bit words includes 2 X16bit valid words. 10 24 MSB bits are used (RGB) - 8 LSB bits are ignored by the DC 11 32 bits are used

**37.5.314 DC Write Channel 9 Configuration 2 Register  
(IPUx\_DC\_WR\_CH\_CONF2\_9)**

Address: Base address + 5\_80B8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_WR\_CH\_CONF2\_9 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
NEW_ADDR_SPACE_SA_9	Channel #8 is used for ARM platform direct access to the display. This field defines the base address of the second region accessible on the display

### 37.5.315 DC Routine Link Register 1 Channel 9 (IPUx\_DC\_RL1\_CH\_9)

Address: Base address + 5\_80BCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NEW_ADDR_START_CHAN_W_9_1								0								COD_NEW_ADDR_START_CHAN_W_9_0								0							
W																									COD_NEW_ADDR_PRIORITY_CHAN_9							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL1\_CH\_9 field descriptions

Field	Description
31–24 COD_NEW_ ADDR_START_ CHAN_W_9_1	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #9, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ ADDR_START_ CHAN_W_9_0	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #9, first region)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ ADDR_ PRIORITY_ CHAN_9	This field defines the priority of the new address event (associated with channel #9, both regions)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

### 37.5.316 DC Routine Link Register 2 Channel 9 (IPUx\_DC\_RL2\_CH\_9)

Address: Base address + 5\_80C0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NEW_CHAN_START_CHAN_W_9_1								0								COD_NEW_CHAN_START_CHAN_W_9_0								0							
W																									COD_NEW_CHAN_PRIORITY_CHAN_9							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_RL2\_CH\_9 field descriptions**

Field	Description
31–24 COD_NEW_ CHAN_START_ CHAN_W_9_1	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #9, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ CHAN_START_ CHAN_W_9_0	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #9, first region)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ CHAN_ PRIORITY_ CHAN_9	<p>This field defines the priority of the new address event (associated with channel #9, both regions)</p> <p>The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)</p> <p>0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved</p>

### 37.5.317 DC Routine Link Register 3Channel 9 (IPUx\_DC\_RL3\_CH\_9)

Address: Base address + 5\_80C4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NEW_DATA_START_ CHAN_W_9_1								0								0								COD_NEW_ DATA_ PRIORITY_ CHAN_9							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DC\_RL3\_CH\_9 field descriptions**

Field	Description
31–24 COD_NEW_ DATA_START_ CHAN_W_9_1	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #9, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_DC\_RL3\_CH\_9 field descriptions (continued)**

Field	Description
15–8 COD_NEW_ DATA_START_ CHAN_W_9_0	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #9, first region)
7–4 Reserved	This read-only field is reserved and always has the value 0.
COD_NEW_ DATA_ PRIORITY_ CHAN_9	This field defines the priority of the new address event (associated with channel #9, both regions)  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved

**37.5.318 DC Routine Link Register 4 Channel 9  
(IPUx\_DC\_RL4\_CH\_9)**

Address: Base address + 5\_80C8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NEW_ADDR_START_ CHAN_R_9_1				0				COD_NEW_ADDR_START_ CHAN_R_9_0				0																			
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_RL4\_CH\_9 field descriptions**

Field	Description
31–24 COD_NEW_ ADDR_START_ CHAN_R_9_1	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #9, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ ADDR_START_ CHAN_R_9_0	This field is a pointer to the address within the microcode memory where the routine that handles the new address event resides (associated with channel #9, first region)
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.319 DC Routine Link Register 5 Channel 9 (IPUx\_DC\_RL5\_CH\_9)

Address: Base address + 5\_80CCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NEW_CHAN_START_ CHAN_R_9_1															0	COD_NEW_CHAN_START_ CHAN_R_9_0															0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL5\_CH\_9 field descriptions

Field	Description
31–24 COD_NEW_ CHAN_START_ CHAN_R_9_1	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #9, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.
15–8 COD_NEW_ CHAN_START_ CHAN_R_9_0	This field is a pointer to the address within the microcode memory where the routine that handles the new channel event resides (associated with channel #9, first region)
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.320 DC Routine Link Register 6 Channel 9 (IPUx\_DC\_RL6\_CH\_9)

Address: Base address + 5\_80D0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	COD_NEW_DATA_START_ CHAN_R_9_1															0	COD_NEW_DATA_START_ CHAN_R_9_0														0	
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

#### IPUx\_DC\_RL6\_CH\_9 field descriptions

Field	Description
31–24 COD_NEW_ DATA_START_ CHAN_R_9_1	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #9, second region)
23–16 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_DC\_RL6\_CH\_9 field descriptions (continued)**

Field	Description
15–8 COD_NEW_ DATA_START_ CHAN_R_9_0	This field is a pointer to the address within the microcode memory where the routine that handles the new data event resides (associated with channel #9, first region)
Reserved	This read-only field is reserved and always has the value 0.

**37.5.321 DC General Register (IPUx\_DC\_GEN)**

Address: Base address + 5\_80D4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
								0								
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																
								0								
W																
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
DC_CH5_TYPE									SYNC_PRIORITY_1	SYNC_PRIORITY_5	MASK4CHAN_5	MASK_EN		SYNC_1_6		
									0	1	1	0	0	0	0	0

**IPUx\_DC\_GEN field descriptions**

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24 DC_BK_EN	Cursor blinking enable 1 blinking is enabled 0 blinking is disabled
23–16 DC_BKDIV	Blinking Rate This field defines the blinking rate. The blinking occurs every N-th frame While N is defined by DC_BKDIV
15–9 Reserved	This read-only field is reserved and always has the value 0.
8 DC_CH5_TYPE	Channel 5 is used for synchronous flow. When this channel is used for accessing asynchronous display that is activated in a synchronous way

Table continues on the next page...

**IPUx\_DC\_GEN field descriptions (continued)**

Field	Description
	<p>1 Enable the asynchronous interface via channel 5 0 normal mode, synchronous flow via channel 5</p>
7 SYNC_PRIORITY_1	<p>When 2 sync flows are running, this bit sets the priority of channel #1. both SYNC_PRIORITY_5 and SYNC_PRIORITY_1 should not have the value of 0 This bit should be</p> <p>1 high Priority 0 low Priority</p>
6 SYNC_PRIORITY_5	<p>When 2 sync flows are running, this bit sets the priority of channel #5. both SYNC_PRIORITY_5 and SYNC_PRIORITY_1 should not have the value of 0 This bit should be</p> <p>1 high priority 0 low Priority</p>
5 MASK4CHAN_5	<p>Sync flow can be associated with a mask channel. Only one sync flow can have a mask. This bit is ignored if MASK_EN is clear</p> <p>1 mask channel is associated to the sync flow via DP 0 mask channel is associated to the sync flow via DC (without DP)</p>
4 MASK_EN	<p>Enable of the mask channel</p> <p>1 mask channel is enabled 0 mask channel is disabled</p>
3 Reserved	This read-only field is reserved and always has the value 0.
2–1 SYNC_1_6	<p>This field</p> <p>00 Channel 1 of the DC handles async flow 01 Illegal 10 Channel 1 of the DC handles sync flow 11 illegal</p>
0 Reserved	This read-only field is reserved and always has the value 0.

### 37.5.322 DC Display Configuration 1 Register 0 (IPUx\_DC\_DISP\_CONF1\_0)

Address: Base address + 5\_80D8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W									DISP_RD_VALUE_PTR_0	MCU_ACC_LB_MASK_0	ADDR_BE_L_INC_0	ADDR_INCREMENT_0	DISP_TYP_0			
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

#### IPUx\_DC\_DISP\_CONF1\_0 field descriptions

Field	Description
31–8 Reserved	This read-only field is reserved and always has the value 0.
7 DISP_RD_ VALUE_PTR_0	When the display works in wait for status mode. The IPU polls the display and compare the value to the value stored on the status DI_READ_DATA_ACK_VALUE and mask it with DI_READ_DATA_MASK. The DC holds 2 sets of mask and value. This field holds a pointer to the corresponding set of mask and value.  1 DI_READ_DATA_ACK_VALUE_1 & DI_READ_DATA_MASK_1 are used for display 0 0 DI_READ_DATA_ACK_VALUE_0 & DI_READ_DATA_MASK_0 are used for display 0
6 MCU_ACC_LB_ MASK_0	The DC compares between the current access to the a calculated address. The calculated address is the next consecutive address following the last address. This bit defines the comparing mode  1 The 2 addresses are fully compared 0 The 2 addresses are compared, but the ADDR[0] bit of the new address is ignored
5–4 ADDR_BE_L_ INC_0	This bits define the increment mode when the latest access was done with some of the byte enable signals are low, in that case different increment should be done instead of the normal auto increment of the address  IF MCU_ACC_LB_MASK_0 is 0 then only 00 and 10 values are allowed.  00 No increment 01 Increment by 1 10 Increment by 2 11 Increment by 3

Table continues on the next page...

**IPUx\_DC\_DISP\_CONF1\_0 field descriptions (continued)**

Field	Description
3–2 ADDR_ INCREMENT_0	This field is the increment step for auto increment mode  00 Increment the address by 1 01 Increment the address by 2 10 Increment the address by 3 11 Increment the address by 4
DISP_TYP_0	This field defines the type of the display  00 Serial accesses display 01 Reserved 10 parallel display, without byte_enable support 11 parallel display, with byte_enable support

### 37.5.323 DC Display Configuration 1 Register 1 (IPUx\_DC\_DISP\_CONF1\_1)

Address: Base address + 5\_80DCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W										DISP_RD_VALUE_ PTR_1	MCU_ACC_LB_ MASK_1	ADDR_BE_L_INC_ 1	ADDR_INCREMENT_1		DISP_TYP_1	
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

**IPUx\_DC\_DISP\_CONF1\_1 field descriptions**

Field	Description
31–8 Reserved	This read-only field is reserved and always has the value 0.
7 DISP_RD_ VALUE_PTR_1	When the display works in wait for status mode. The IPU polls the display and compare the value to the value stored on the status DI_READ_DATA_ACK_VALUE and mask it with DI_READ_DATA_MASK. The DC holds 2 sets of mask and value. This field holds a pointer to the corresponding set of mask and value.

*Table continues on the next page...*

**IPUx\_DC\_DISP\_CONF1\_1 field descriptions (continued)**

Field	Description
	1 DI_READ_DATA_ACK_VALUE_1 & DI_READ_DATA_MASK_1 are used for display 1 0 DI_READ_DATA_ACK_VALUE_0 & DI_READ_DATA_MASK_0 are used for display 1
6 MCU_ACC_LB_ MASK_1	The DC compares between the current access to the a calculated address. The calculated address is the next consecutive address following the last address. This bit defines the comparing mode 1 The 2 addresses are fully compared 0 The 2 addresses are compared, but the ADDR[0] bit of the new address is ignored
5–4 ADDR_BE_L_ INC_1	These bits define the increment mode when the latest access was done with some of the byte enable signals are low, in that case different increment should be done instead of the normal auto increment of the address  IF MCU_ACC_LB_MASK_1 is 0 then only 00 and 10 values are allowed.  00 No increment 01 Increment by 1 10 Increment by 2 11 Increment by 3
3–2 ADDR_ INCREMENT_1	This field is the increment step for auto increment mode  00 Increment the address by 1 01 Increment the address by 2 10 Increment the address by 3 11 Increment the address by 4
DISP_TYP_1	This field defines the type of the display  00 Serial accesses display 01 Reserved 10 parallel display, without byte_enable support 11 parallel display, with byte_enable support

### 37.5.324 DC Display Configuration 1 Register 2 (IPUx\_DC\_DISP\_CONF1\_2)

Address: Base address + 5\_80E0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W									DISP_RD_VALUE_PTR_2	MCU_ACC_LB_MASK_2	ADDR_BE_L_INC_2	ADDR_INCREMENT_2	DISP_TYP_2			
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

#### IPUx\_DC\_DISP\_CONF1\_2 field descriptions

Field	Description
31–8 Reserved	This read-only field is reserved and always has the value 0.
7 DISP_RD_VALUE_PTR_2	When the display works in wait for status mode. The IPU polls the display and compare the value to the value stored on the status DI_READ_DATA_ACK_VALUE and mask it with DI_READ_DATA_MASK. The DC holds 2 sets of mask and value. This field holds a pointer to the corresponding set of mask and value.  1 DI_READ_DATA_ACK_VALUE_1 & DI_READ_DATA_MASK_1 are used for display 2 0 DI_READ_DATA_ACK_VALUE_0 & DI_READ_DATA_MASK_0 are used for display 2
6 MCU_ACC_LB_MASK_2	The DC compares between the current access to the a calculated address. The calculated address is the next consecutive address following the last address. This bit defines the comparing mode  1 The 2 addresses are fully compared 0 The 2 addresses are compared, but the ADDR[0] bit of the new address is ignored
5–4 ADDR_BE_L_INC_2	This bits define the increment mode when the latest access was done with some of the byte enable signals are low, in that case different increment should be done instead of the normal auto increment of the address  IF MCU_ACC_LB_MASK_2 is 0 then only 00 and 10 values are allowed.  00 No increment 01 Increment by 1 10 Increment by 2 11 Increment by 3

Table continues on the next page...

**IPUx\_DC\_DISP\_CONF1\_2 field descriptions (continued)**

Field	Description
3–2 ADDR_ INCREMENT_2	This field is the increment step for auto increment mode  00 Increment the address by 1 01 Increment the address by 2 10 Increment the address by 3 11 Increment the address by 4
DISP_TYP_2	This field defines the type of the display  00 Serial accesses display 01 Reserved 10 parallel display, without byte_enable support 11 parallel display, with byte_enable support

**37.5.325 DC Display Configuration 1 Register 3  
(IPUx\_DC\_DISP\_CONF1\_3)**

Address: Base address + 5\_80E4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W										DISP_RD_VALUE_ PTR_3	MCU_ACC_LB_ MASK_3	ADDR_BE_L_INC_ 3	ADDR_INCREMENT_3		DISP_TYP_3	
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

**IPUx\_DC\_DISP\_CONF1\_3 field descriptions**

Field	Description
31–8 Reserved	This read-only field is reserved and always has the value 0.
7 DISP_RD_ VALUE_PTR_3	When the display works in wait for status mode. The IPU polls the display and compare the value to the value stored on the status DI_READ_DATA_ACK_VALUE and mask it with DI_READ_DATA_MASK. The DC holds 2 sets of mask and value. This field holds a pointer to the corresponding set of mask and value.

*Table continues on the next page...*

**IPUx\_DC\_DISP\_CONF1\_3 field descriptions (continued)**

Field	Description
	1 DI_READ_DATA_ACK_VALUE_1 & DI_READ_DATA_MASK_1 are used for display 3 0 DI_READ_DATA_ACK_VALUE_0 & DI_READ_DATA_MASK_0 are used for display 3
6 MCU_ACC_LB_ MASK_3	The DC compares between the current access to the a calculated address. The calculated address is the next consecutive address following the last address. This bit defines the comparing mode 1 The 2 addresses are fully compared 0 The 2 addresses are compared, but the ADDR[0] bit of the new address is ignored
5–4 ADDR_BE_L_ INC_3	These bits define the increment mode when the latest access was done with some of the byte enable signals are low, in that case different increment should be done instead of the normal auto increment of the address  IF MCU_ACC_LB_MASK_3 is 0 then only 00 and 10 values are allowed.  00 No increment 01 Increment by 1 10 Increment by 2 11 Increment by 3
3–2 ADDR_ INCREMENT_3	This field is the increment step for auto increment mode  00 Increment the address by 1 01 Increment the address by 2 10 Increment the address by 3 11 Increment the address by 4
DISP_TYP_3	This field defines the type of the display  00 Serial accesses display 01 Reserved 10 parallel display, without byte_enable support 11 parallel display, with byte_enable support

### 37.5.326 DC Display Configuration 2 Register 0 (IPUx\_DC\_DISP\_CONF2\_0)

Address: Base address + 5\_80E8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																SL_0															
W																																

Reset 0

**IPUx\_DC\_DISP\_CONF2\_0 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
SL_0	Stride line of display 0

### 37.5.327 DC Display Configuration 2 Register 1 (IPUx\_DC\_DISP\_CONF2\_1)

Address: Base address + 5\_80ECh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		0																														
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_DC\_DISP\_CONF2\_1 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
SL_1	Stride line of display 1

### 37.5.328 DC Display Configuration 2 Register 2 (IPUx\_DC\_DISP\_CONF2\_2)

Address: Base address + 5\_80F0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		0																														
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

#### IPUx\_DC\_DISP\_CONF2\_2 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
SL_2	Stride line of display 2

### 37.5.329 DC Display Configuration 2 Register 3 (IPUx\_DC\_DISP\_CONF2\_3)

Address: Base address + 5\_80F4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		0																														
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_DISP\_CONF2\_3 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
SL_3	Stride line of display 3

**37.5.330 DC DI0Configuration Register 1 (IPUx\_DC\_DI0\_CONF\_1)**

Address: Base address + 5\_80F8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DI_READ_DATA_MASK_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_DI0\_CONF\_1 field descriptions**

Field	Description
DI_READ_DATA_MASK_0	This field defines the mask value of the data read from the display.

**37.5.331 DC DI0Configuration Register 2 (IPUx\_DC\_DI0\_CONF\_2)**

Address: Base address + 5\_80FCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DI_READ_DATA_ACK_VALUE_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_DI0\_CONF\_2 field descriptions**

Field	Description
DI_READ_DATA_ACK_VALUE_0	This is the expected data to be read from the display. The value reads from the display is anded with the DI_READ_DATA_MASK_0 and compared with the DI_READ_DATA_ACK_VALUE_0. This field is used for the READ_STATUS task of the DC

**37.5.332 DC DI1Configuration Register 1 (IPUx\_DC\_DI1\_CONF\_1)**

Address: Base address + 5\_8100h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DI_READ_DATA_MASK_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_DI1\_CONF\_1 field descriptions**

Field	Description
DI_READ_DATA_MASK_1	This field defines the mask value of the data read from the display.

**37.5.333 DC DI1 Configuration Register 2 (IPUx\_DC\_DI1\_CONF\_2)**

Address: Base address + 5\_8104h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

**IPUx\_DC\_DI1\_CONF\_2 field descriptions**

Field	Description
DI_READ_DATA_ACK_VALUE_1	This is the expected data to be read from the display. The value reads from the display is anded with the DI_READ_DATA_MASK_1 and compared with the DI_READ_DATA_ACK_VALUE_1. This field is used for the READ_STATUS task of the DC

**37.5.334 DC Mapping Configuration Register 0 (IPUx\_DC\_MAP\_CONF\_0)**

Address: Base address + 5\_8108h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
MAPPING_PNTR_BYTE2_1																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W																
MAPPING_PNTR_BYTE2_0																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DC\_MAP\_CONF\_0 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_1	Mapping pointer #1 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i></i> and MD_MASK_<i></i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_1	Mapping pointer #1 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i></i> and MD_MASK_<i></i> used for mapping byte #1

Table continues on the next page...

**IPUx\_DC\_MAP\_CONF\_0 field descriptions (continued)**

Field	Description
20–16 MAPPING_PNTR_BYTE0_1	Mapping pointer #1 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTE2_0	Mapping pointer #0 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_0	Mapping pointer #0 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTE0_0	Mapping pointer #0 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

**37.5.335 DC Mapping Configuration Register 1  
(IPUx\_DC\_MAP\_CONF\_1)**

Address: Base address + 5\_810Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DC\_MAP\_CONF\_1 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_3	Mapping pointer #3 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_3	Mapping pointer #3 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTE0_3	Mapping pointer #3 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

**IPUx\_DC\_MAP\_CONF\_1 field descriptions (continued)**

Field	Description
14–10 MAPPING_PNTR_BYTE2_2	Mapping pointer #1 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_2	Mapping pointer #1 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTE0_2	Mapping pointer #1 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

**37.5.336 DC Mapping Configuration Register 2  
(IPUx\_DC\_MAP\_CONF\_2)**

Address: Base address + 5\_8110h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	MAPPING_PNTR_BYTE2_5					MAPPING_PNTR_BYTE1_5					MAPPING_PNTR_BYTE0_5				
W		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	MAPPING_PNTR_BYTE2_4					MAPPING_PNTR_BYTE1_4					MAPPING_PNTR_BYTE0_4				
W		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DC\_MAP\_CONF\_2 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_5	Mapping pointer #5 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_5	Mapping pointer #5 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTE0_5	Mapping pointer #5 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTE2_4	Mapping pointer #4 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_4	Mapping pointer #4 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1

Table continues on the next page...

**IPUx\_DC\_MAP\_CONF\_2 field descriptions (continued)**

Field	Description
MAPPING_PNTR_BYTE0_4	Mapping pointer #4 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.337 DC Mapping Configuration Register 3 (IPUx\_DC\_MAP\_CONF\_3)

Address: Base address + 5\_8114h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_DC\_MAP\_CONF\_3 field descriptions**

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_7	Mapping pointer #7 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_7	Mapping pointer #7 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTE0_7	Mapping pointer #7 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTE2_6	Mapping pointer #6 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_6	Mapping pointer #6 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTE0_6	Mapping pointer #6 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.338 DC Mapping Configuration Register 4 (IPUx\_DC\_MAP\_CONF\_4)

Address: Base address + 5\_8118h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0	MAPPING_PNTR_BYTEx_9					MAPPING_PNTR_BYTEx_1				MAPPING_PNTR_BYTEx_0						
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0	MAPPING_PNTR_BYTEx_8					MAPPING_PNTR_BYTEx_1_8				MAPPING_PNTR_BYTEx_0_8						
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_4 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTEx_9	Mapping pointer #9 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTEx_1	Mapping pointer #9 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTEx_0	Mapping pointer #9 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTEx_8	Mapping pointer #8 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTEx_1_8	Mapping pointer #8 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTEx_0_8	Mapping pointer #8 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.339 DC Mapping Configuration Register 5 (IPUx\_DC\_MAP\_CONF\_5)

Address: Base address + 5\_811Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0								MAPPING_PNTR_BYTE2_11								
W										MAPPING_PNTR_BYTE1_11							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0								MAPPING_PNTR_BYTE2_10								
W										MAPPING_PNTR_BYTE1_10							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_5 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_11	Mapping pointer #11 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_11	Mapping pointer #11 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTE0_11	Mapping pointer #11 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTE2_10	Mapping pointer #10 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_10	Mapping pointer #10 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTE0_10	Mapping pointer #10 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.340 DC Mapping Configuration Register 6 (IPUx\_DC\_MAP\_CONF\_6)

Address: Base address + 5\_8120h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0								MAPPING_PNTR_BYTE2_13								
W										MAPPING_PNTR_BYTE1_13							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0								MAPPING_PNTR_BYTE2_12								
W										MAPPING_PNTR_BYTE1_12							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_6 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_13	Mapping pointer #13 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_13	Mapping pointer #13 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTE0_13	Mapping pointer #13 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTE2_12	Mapping pointer #12 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_12	Mapping pointer #12 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTE0_12	Mapping pointer #12 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.341 DC Mapping Configuration Register 7 (IPUx\_DC\_MAP\_CONF\_7)

Address: Base address + 5\_8124h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_7 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_ PNTR_BYT E2_15	Mapping pointer #15 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_ PNTR_BYT E1_15	Mapping pointer #15 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_ PNTR_BYT E0_15	Mapping pointer #15 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_ PNTR_BYT E2_14	Mapping pointer #14 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_ PNTR_BYT E1_14	Mapping pointer #14 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_ PNTR_BYT E0_14	Mapping pointer #14 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.342 DC Mapping Configuration Register 8 (IPUx\_DC\_MAP\_CONF\_8)

Address: Base address + 5\_8128h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0								MAPPING_PNTR_BYT2_17								
W										MAPPING_PNTR_BYT1_17							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0								MAPPING_PNTR_BYT2_16								
W										MAPPING_PNTR_BYT1_16							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_8 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYT2_17	Mapping pointer #17 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYT1_17	Mapping pointer #17 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYT0_17	Mapping pointer #17 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYT2_16	Mapping pointer #16 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYT1_16	Mapping pointer #16 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYT0_16	Mapping pointer #16 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.343 DC Mapping Configuration Register 9 (IPUx\_DC\_MAP\_CONF\_9)

Address: Base address + 5\_812Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0	MAPPING_PNTR_BYT2_19					MAPPING_PNTR_BYT1_19				MAPPING_PNTR_BYT0_19						
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0	MAPPING_PNTR_BYT2_18					MAPPING_PNTR_BYT1_18				MAPPING_PNTR_BYT0_18						
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_9 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYT2_19	Mapping pointer #19 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYT1_19	Mapping pointer #19 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYT0_19	Mapping pointer #19 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYT2_18	Mapping pointer #18 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYT1_18	Mapping pointer #18 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYT0_18	Mapping pointer #18 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.344 DC Mapping Configuration Register 10 (IPUx\_DC\_MAP\_CONF\_10)

Address: Base address + 5\_8130h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0								MAPPING_PNTR_BYTE2_21								
W										MAPPING_PNTR_BYTE1_21							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0								MAPPING_PNTR_BYTE2_20								
W										MAPPING_PNTR_BYTE1_20							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_10 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_21	Mapping pointer #21 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_21	Mapping pointer #21 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTE0_21	Mapping pointer #21 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTE2_20	Mapping pointer #20 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_20	Mapping pointer #20 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTE0_20	Mapping pointer #20 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.345 DC Mapping Configuration Register 11 (IPUx\_DC\_MAP\_CONF\_11)

Address: Base address + 5\_8134h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0																
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_11 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_ PNTR_BYT2_23	Mapping pointer #23 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_ PNTR_BYT1_23	Mapping pointer #23 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_ PNTR_BYT0_23	Mapping pointer #23 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_ PNTR_BYT2_22	Mapping pointer #22 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_ PNTR_BYT1_22	Mapping pointer #22 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_ PNTR_BYT0_22	Mapping pointer #22 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.346 DC Mapping Configuration Register 12 (IPUx\_DC\_MAP\_CONF\_12)

Address: Base address + 5\_8138h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0	MAPPING_PNTR_BYTE2_25					MAPPING_PNTR_BYTE1_25				MAPPING_PNTR_BYTE0_25						
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0	MAPPING_PNTR_BYTE2_24					MAPPING_PNTR_BYTE1_24				MAPPING_PNTR_BYTE0_24						
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_12 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_25	Mapping pointer #25 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_25	Mapping pointer #25 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTE0_25	Mapping pointer #25 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTE2_24	Mapping pointer #24 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_24	Mapping pointer #24 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTE0_24	Mapping pointer #24 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.347 DC Mapping Configuration Register 13 (IPUx\_DC\_MAP\_CONF\_13)

Address: Base address + 5\_813Ch offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0								MAPPING_PNTR_BYTE2_27								
W										MAPPING_PNTR_BYTE1_27							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0								MAPPING_PNTR_BYTE2_26								
W										MAPPING_PNTR_BYTE1_26							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_13 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_27	Mapping pointer #27 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_27	Mapping pointer #27 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTE0_27	Mapping pointer #27 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTE2_26	Mapping pointer #26 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_26	Mapping pointer #26 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTE0_26	Mapping pointer #26 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.348 DC Mapping Configuration Register 14 (IPUx\_DC\_MAP\_CONF\_14)

Address: Base address + 5\_8140h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R	0								MAPPING_PNTR_BYTE2_29								
W										MAPPING_PNTR_BYTE1_29							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	0								MAPPING_PNTR_BYTE2_28f								
W										MAPPING_PNTR_BYTE1_28							
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

#### IPUx\_DC\_MAP\_CONF\_14 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_PNTR_BYTE2_29	Mapping pointer #29 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_PNTR_BYTE1_29	Mapping pointer #29 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_PNTR_BYTE0_29	Mapping pointer #29 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_PNTR_BYTE2_28f	Mapping pointer #28 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_PNTR_BYTE1_28	Mapping pointer #28 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_PNTR_BYTE2_28	Mapping pointer #28 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

### 37.5.349 DC Mapping Configuration Register 15 (IPUx\_DC\_MAP\_CONF\_15)

Address: Base address + 5\_8144h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

#### IPUx\_DC\_MAP\_CONF\_15 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_1	Mapping unit's offset parameter #1 This field defines the offset parameter #1 within the 24bit word coming from the DC.
23–16 MD_MASK_1	Mapping unit's mask value #1 This field defines the mask value #1 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_0	Mapping unit's offset parameter #0 This field defines the offset parameter #0 within the 24bit word coming from the DC.
MD_MASK_0	Mapping unit's mask value #0 This field defines the mask value #0 within the 8bit word coming from the DC.

### 37.5.350 DC Mapping Configuration Register 16 (IPUx\_DC\_MAP\_CONF\_16)

Address: Base address + 5\_8148h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

#### IPUx\_DC\_MAP\_CONF\_16 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_3	Mapping unit's offset parameter #3 This field defines the offset parameter #3 within the 24bit word coming from the DC.

*Table continues on the next page...*

**IPUx\_DC\_MAP\_CONF\_16 field descriptions (continued)**

Field	Description
23–16 MD_MASK_3	Mapping unit's mask value #3 This field defines the mask value #3 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_2	Mapping unit's offset parameter #2 This field defines the offset parameter #2 within the 24bit word coming from the DC.
MD_MASK_0	Mapping unit's mask value #2 This field defines the mask value #2 within the 8bit word coming from the DC.

**37.5.351 DC Mapping Configuration Register 17  
(IPUx\_DC\_MAP\_CONF\_17)**

Address: Base address + 5\_814Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_MAP\_CONF\_17 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_5	Mapping unit's offset parameter #5 This field defines the offset parameter #5 within the 24bit word coming from the DC.
23–16 MD_MASK_5	Mapping unit's mask value #5 This field defines the mask value #5 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_4	Mapping unit's offset parameter #4 This field defines the offset parameter #4 within the 24bit word coming from the DC.
MD_MASK_4	Mapping unit's mask value #4 This field defines the mask value #4 within the 8bit word coming from the DC.

### 37.5.352 DC Mapping Configuration Register 18 (IPUX\_DC\_MAP\_CONF\_18)

Address: Base address + 5\_8150h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

#### IPUX\_DC\_MAP\_CONF\_18 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_7	Mapping unit's offset parameter #7 This field defines the offset parameter #7 within the 24bit word coming from the DC.
23–16 MD_MASK_7	Mapping unit's mask value #7 This field defines the mask value #7 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_6	Mapping unit's offset parameter #6 This field defines the offset parameter #6 within the 24bit word coming from the DC.
MD_MASK_6	Mapping unit's mask value #6 This field defines the mask value #6 within the 8bit word coming from the DC.

### 37.5.353 DC Mapping Configuration Register 19 (IPUX\_DC\_MAP\_CONF\_19)

Address: Base address + 5\_8154h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

#### IPUX\_DC\_MAP\_CONF\_19 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_9	Mapping unit's offset parameter #9 This field defines the offset parameter #9 within the 24bit word coming from the DC.

*Table continues on the next page...*

**IPUx\_DC\_MAP\_CONF\_19 field descriptions (continued)**

Field	Description
23–16 MD_MASK_9	Mapping unit's mask value #9 This field defines the mask value #9 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_8	Mapping unit's offset parameter #8 This field defines the offset parameter #8 within the 24bit word coming from the DC.
MD_MASK_8	Mapping unit's mask value #8 This field defines the mask value #8 within the 8bit word coming from the DC.

**37.5.354 DC Mapping Configuration Register 20  
(IPUx\_DC\_MAP\_CONF\_20)**

Address: Base address + 5\_8158h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_MAP\_CONF\_20 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_11	Mapping unit's offset parameter #11 This field defines the offset parameter #11 within the 24bit word coming from the DC.
23–16 MD_MASK_11	Mapping unit's mask value #11 This field defines the mask value #11 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_10	Mapping unit's offset parameter #10 This field defines the offset parameter #10 within the 24bit word coming from the DC.
MD_MASK_10	Mapping unit's mask value #10 This field defines the mask value #10 within the 8bit word coming from the DC.

### 37.5.355 DC Mapping Configuration Register 21 (IPUX\_DC\_MAP\_CONF\_21)

Address: Base address + 5\_815Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

#### IPUX\_DC\_MAP\_CONF\_21 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_13	Mapping unit's offset parameter #13 This field defines the offset parameter #13 within the 24bit word coming from the DC.
23–16 MD_MASK_13	Mapping unit's mask value #13 This field defines the mask value #13 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_12	Mapping unit's offset parameter #12 This field defines the offset parameter #12 within the 24bit word coming from the DC.
MD_MASK_12	Mapping unit's mask value #12 This field defines the mask value #12 within the 8bit word coming from the DC.

### 37.5.356 DC Mapping Configuration Register 22 (IPUX\_DC\_MAP\_CONF\_22)

Address: Base address + 5\_8160h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

#### IPUX\_DC\_MAP\_CONF\_22 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_15	Mapping unit's offset parameter #15 This field defines the offset parameter #15 within the 24bit word coming from the DC.

Table continues on the next page...

**IPUx\_DC\_MAP\_CONF\_22 field descriptions (continued)**

Field	Description
23–16 MD_MASK_15	Mapping unit's mask value #15 This field defines the mask value #15 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_14	Mapping unit's offset parameter #14 This field defines the offset parameter #14 within the 24bit word coming from the DC.
MD_MASK_14	Mapping unit's mask value #14 This field defines the mask value #14 within the 8bit word coming from the DC.

**37.5.357 DC Mapping Configuration Register 23  
(IPUx\_DC\_MAP\_CONF\_23)**

Address: Base address + 5\_8164h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_MAP\_CONF\_23 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_17	Mapping unit's offset parameter #17 This field defines the offset parameter #17 within the 24bit word coming from the DC.
23–16 MD_MASK_17	Mapping unit's mask value #17 This field defines the mask value #17 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_16	Mapping unit's offset parameter #16 This field defines the offset parameter #16 within the 24bit word coming from the DC.
MD_MASK_16	Mapping unit's mask value #16 This field defines the mask value #16 within the 8bit word coming from the DC.

### 37.5.358 DC Mapping Configuration Register 24 (IPUX\_DC\_MAP\_CONF\_24)

Address: Base address + 5\_8168h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

#### IPUX\_DC\_MAP\_CONF\_24 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_19	Mapping unit's offset parameter #19 This field defines the offset parameter #19 within the 24bit word coming from the DC.
23–16 MD_MASK_19	Mapping unit's mask value #19 This field defines the mask value #19 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_18	Mapping unit's offset parameter #18 This field defines the offset parameter #18 within the 24bit word coming from the DC.
MD_MASK_18	Mapping unit's mask value #18 This field defines the mask value #18 within the 8bit word coming from the DC.

### 37.5.359 DC Mapping Configuration Register 25 (IPUX\_DC\_MAP\_CONF\_25)

Address: Base address + 5\_816Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

#### IPUX\_DC\_MAP\_CONF\_25 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_21	Mapping unit's offset parameter #21 This field defines the offset parameter #21 within the 24bit word coming from the DC.

Table continues on the next page...

**IPUx\_DC\_MAP\_CONF\_25 field descriptions (continued)**

Field	Description
23–16 MD_MASK_21	Mapping unit's mask value #21 This field defines the mask value #21 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_20	Mapping unit's offset parameter #20 This field defines the offset parameter #20 within the 24bit word coming from the DC.
MD_MASK_20	Mapping unit's mask value #20 This field defines the mask value #20 within the 8bit word coming from the DC.

**37.5.360 DC Mapping Configuration Register 26  
(IPUx\_DC\_MAP\_CONF\_26)**

Address: Base address + 5\_8170h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_MAP\_CONF\_26 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–24 MD_OFFSET_23	Mapping unit's offset parameter #23 This field defines the offset parameter #23 within the 24bit word coming from the DC.
23–16 MD_MASK_23	Mapping unit's mask value #23 This field defines the mask value #23 within the 8bit word coming from the DC.
15–13 Reserved	This read-only field is reserved and always has the value 0.
12–8 MD_OFFSET_22	Mapping unit's offset parameter #22 This field defines the offset parameter #22 within the 24bit word coming from the DC.
MD_MASK_22	Mapping unit's mask value #22 This field defines the mask value #22 within the 8bit word coming from the DC.

### 37.5.361 DC User General Data Event 0 Register 0 (IPUx\_DC\_UGDE0\_0)

Address: Base address + 5\_8174h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
	0															
				NF_NL_0		AUTORESTART_0	ODD_EN_0	0						COD_ODD_START_0		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
														COD_EV_START_0		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DC\_UGDE0\_0 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–27 NF_NL_0	the user may attach his general event #0 to New-line New-Frame and New-field events. One of these event triggers the user's general event #0's counter. The actual internal trigger is the pixel following the occurrence of the selected event.  00 New Line 01 New Frame 10 New Field 11 Reserved
26 AUTORESTART_0	User's general event #0 auto restart mode  0 disable 1 User's general event #0's counter is automatically restarted.
25 ODD_EN_0	The user's general event #0 may be split into 2 internal signals. One one mode all the events are sent on one signal, on the second mode odd events are sent over one signal while even events are sent over the other signal (ODD_MODE)  1 ODD_MODE is enabled 0 ODD_MODE is disabled
24 Reserved	This read-only field is reserved and always has the value 0.
23–16 COD_ODD_START_0	This field holds a pointer in the microcode holding the routine to be performed following the user general event #0. When ODD_MODE is enabled, only the odd events will use this pointer

Table continues on the next page...

**IPUx\_DC\_UGDE0\_0 field descriptions (continued)**

Field	Description
	When ODD_MODE is disabled this field is ignored
15–8 COD_EV_ START_0	This field holds a pointer in the microcode holding the routine to be performed following the user general event #0. When ODD_MODE is enabled, only the even events will use this pointer  When ODD_MODE is disabled, all the events will use this pointer
7 Reserved	This read-only field is reserved and always has the value 0.
6–3 COD_EV_ PRIORITY_0	This field defines the priority of the user general event #0  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
ID_CODED_0	This field defines the number of DC channel number that user's general event #0 will be associated to.  000 DC channel_0 001 DC channel_1 010 DC channel_2 011 DC channel_5 (DP_SYNC) 100 DC channel_6 (DP_ASYNC) 101 Reserved 110 Reserved. 111 Reserved.

### 37.5.362 DC User General Data Event 0 Register 1 (IPUx\_DC\_UGDE0\_1)

Address: Base address + 5\_8178h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

**IPUx\_DC\_UGDE0\_1 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
STEP_0	This field holds the pre defined value that the counter counts too.

### 37.5.363 DC User General Data Event 0 Register2 (IPUx\_DC\_UGDE0\_2)

Address: Base address + 5\_817Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_UGDE0\_2 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
OFFSET_DT_0	This field defines the offset value from which the counter of user general event #0 will start counting from

### 37.5.364 DC User General Data Event 0 Register 3 (IPUx\_DC\_UGDE0\_3)

Address: Base address + 5\_8180h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_UGDE0\_3 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
STEP_REPEAT_0	When auto reload mode is disabled this field defines the number of events that will be generated by the user general event #0 mechanism

### 37.5.365 DC User General Data Event 1 Register0 (IPUx\_DC\_UGDE1\_0)

Address: Base address + 5\_8184h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			0													
							NF_NL_1		AUTORESTART_1							
W									ODD_EN_1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
							COD_EV_START_1									
W									0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DC\_UGDE1\_0 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–27 NF_NL_1	the user may attach his general event #1 to New-line New-Frame and New-field events. One of these event triggers the user's general event #1's counter. The actual internal trigger is the pixel following the occurrence of the selected event.  00 New Line 01 New Frame 10 New Field 11 Reserved
26 AUTORESTART_1	User's general event #1 auto restart mode  0 disable 1 User's general event #1's counter is automatically restarted.
25 ODD_EN_1	The user's general event #1 may be split into 2 internal signals. One one mode all the events are sent on one signal, on the second mode odd events are sent over one signal while even events are sent over the other signal (ODD_MODE)  1 ODD_MODE is enabled 0 ODD_MODE is disabled
24 Reserved	This read-only field is reserved and always has the value 0.
23–16 COD_ODD_START_1	This field holds a pointer in the microcode holding the routine to be performed following the user general event #1. When ODD_MODE is enabled, only the odd events will use this pointer

Table continues on the next page...

**IPUx\_DC\_UGDE1\_0 field descriptions (continued)**

Field	Description
	When ODD_MODE is disabled this field is ignored
15–8 COD_EV_ START_1	This field holds a pointer in the microcode holding the routine to be performed following the user general event #1. When ODD_MODE is enabled, only the even events will use this pointer  When ODD_MODE is disabled, all the events will use this pointer
7 Reserved	This read-only field is reserved and always has the value 0.
6–3 COD_EV_ PRIORITY_1	This field defines the priority of the user general event #1  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
ID_CODED_1	This field defines the number of DC channel number that user's general event #1 will be associated to  000 DC channel_0 001 DC channel_1 010 DC channel_2 011 DC channel_5 (DP_SYNC) 100 DC channel_6 (DP_ASYNC) 101 Reserved 110 Reserved 111 Reserved

### 37.5.366 DC User General Data Event 1 Register 1 (IPUx\_DC\_UGDE1\_1)

Address: Base address + 5\_8188h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_UGDE1\_1 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
STEP_1	This field hold the pre defined value that the counter counts too

### 37.5.367 DC User General Data Event 1 Register 2 (IPUx\_DC\_UGDE1\_2)

Address: Base address + 5\_818Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_UGDE1\_2 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
OFFSET_DT_1	This field defines the offset value from which the counter of user general event #1 will start counting from

### 37.5.368 DC User General Data Event 1 Register 3 (IPUx\_DC\_UGDE1\_3)

Address: Base address + 5\_8190h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_UGDE1\_3 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
STEP_REPEAT_1	When auto reload mode is disabled this field defines the number of events that will be generated by the user general event #1 mechanism

### 37.5.369 DC User General Data Event 2 Register 0 (IPUx\_DC\_UGDE2\_0)

Address: Base address + 5\_8194h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
	0															
				NF_NL_2		AUTORESTART_2		ODD_EN_2								COD_ODD_START_2
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DC\_UGDE2\_0 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–27 NF_NL_2	the user may attach his general event #2 to New-line New-Frame and New-field events. One of these event triggers the user's general event #2's counter. The actual internal trigger is the pixel following the occurrence of the selected event.  00 New Line 01 New Frame 10 New Field 11 Reserved
26 AUTORESTART_2	User's general event #2 auto restart mode  0 disable 1 User's general event #2's counter is automatically restarted.
25 ODD_EN_2	The user's general event #2 may be split into 2 internal signals. One one mode all the events are sent on one signal, on the second mode odd events are sent over one signal while even events are sent over the other signal (ODD_MODE)  1 ODD_MODE is enabled 0 ODD_MODE is disabled
24 Reserved	This read-only field is reserved and always has the value 0.
23–16 COD_ODD_START_2	This field holds a pointer in the microcode holding the routine to be performed following the user general event #2 When ODD_MODE is enabled, only the odd events will use this pointer

Table continues on the next page...

**IPUx\_DC\_UGDE2\_0 field descriptions (continued)**

Field	Description
	When ODD_MODE is disabled this field is ignored
15–8 COD_EV_ START_2	This field holds a pointer in the microcode holding the routine to be performed following the user general event #2. When ODD_MODE is enabled, only the even events will use this pointer  When ODD_MODE is disabled, all the events will use this pointer
7 Reserved	This read-only field is reserved and always has the value 0.
6–3 COD_EV_ PRIORITY_2	This field defines the priority of the user general event #2  The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable)  0000 disable 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
ID_CODED_2	This field defines the number of DC channel number that user's general event #2 will be associated to  000 DC channel_0 001 DC channel_1 010 DC channel_2 011 DC channel_5 (DP_SYNC) 100 DC channel_6 (DP_ASYNC) 101 Reserved 110 Reserved 111 Reserved

### 37.5.370 DC User General Data Event 2 Register 1 (IPUx\_DC\_UGDE2\_1)

Address: Base address + 5\_8198h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_UGDE2\_1 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
STEP_2	This field hold the pre defined value that the counter counts too

### 37.5.371 DC User General Data Event 2Register 2 (IPUx\_DC\_UGDE2\_2)

Address: Base address + 5\_819Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_UGDE2\_2 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
OFFSET_DT_2	This field defines the offset value from which the counter of user general event #2 will start counting from

### 37.5.372 DC User General Data Event 2Register 3 (IPUx\_DC\_UGDE2\_3)

Address: Base address + 5\_81A0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_UGDE2\_3 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
STEP_REPEAT_2	When auto reload mode is disabled this field defines the number of events that will be generated by the user general event #2 mechanism

### 37.5.373 DC User General Data Event 3 Register 0 (IPUx\_DC\_UGDE3\_0)

Address: Base address + 5\_81A4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R																
	0															
						NF_NL_3		AUTORESTART_3								
W								ODD_EN_3								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0							
										COD_EV_PRIORITY_3						
W									0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DC\_UGDE3\_0 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–27 NF_NL_3	the user may attach his general event #3 to New-line New-Frame and New-field events. One of these event triggers the user's general event #3's counter. The actual internal trigger is the pixel following the occurrence of the selected event.  00 New Line 01 New Frame 10 New Field 11 Reserved
26 AUTORESTART_3	User's general event #3 auto restart mode  0 disable 1 User's general event #3's counter is automatically restarted.
25 ODD_EN_3	The user's general event #3 may be split into 2 internal signals. One mode all the events are sent on one signal, on the second mode odd events are sent over one signal while even events are sent over the other signal (ODD_MODE)  1 ODD_MODE is enabled 0 ODD_MODE is disabled
24 Reserved	This read-only field is reserved and always has the value 0.
23–16 COD_ODD_START_3	This field holds a pointer in the microcode holding the routine to be performed following the user general event #3. When ODD_MODE is enabled, only the odd events will use this pointer

Table continues on the next page...

**IPUx\_DC\_UGDE3\_0 field descriptions (continued)**

Field	Description
	When ODD_MODE is disabled this field is ignored
15–8 COD_EV_ START_3	This field holds a pointer in the microcode holding the routine to be performed following the user general event #3. When ODD_MODE is enabled, only the even events will use this pointer  When ODD_MODE is disabled, all the events will use this pointer
7 Reserved	This read-only field is reserved and always has the value 0.
6–3 COD_EV_ PRIORITY_3	This field defines the priority of the user general event #3  0000 disable The priority between the events should be set to a unique value. i.e. two events must not have the same priority (except 0000 - disable) 0001 Priority #1 (lowest) 0010 Priority #2 1101 Priority #13 (highest) 1110 Reserved 1111 Reserved
ID_CODED_3	This field defines the number of DC channel number that user's general event #3 will be associated to  000 DC channel_0 001 DC channel_1 010 DC channel_2 011 DC channel_5 (DP_SYNC) 100 DC channel_6 (DP_ASYNC) 101 Reserved 110 Reserved 111 Reserved.

**37.5.374 DC User General Data Event 3Register 1  
(IPUx\_DC\_UGDE3\_1)**

Address: Base address + 5\_81A8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R	0																																	
W																																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_UGDE3\_1 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
STEP_3	This field hold the pre defined value that the counter counts too

### 37.5.375 DC User General Data Event 3Register 2 (IPUx\_DC\_UGDE3\_2)

Address: Base address + 5\_81ACh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_UGDE3\_2 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
OFFSET_DT_3	This field defines the offset value from which the counter of user general event #3 will start counting from

### 37.5.376 DC User General Data Event 3Register 2 (IPUx\_DC\_UGDE3\_3)

Address: Base address + 5\_81B0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W																																

Reset 0

#### IPUx\_DC\_UGDE3\_3 field descriptions

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
STEP_REPEAT_3	When auto reload mode is disabled this field defines the number of events that will be generated by the user general event #3 mechanism

### 37.5.377 DC Low Level Access Control Register 0 (IPUx\_DC\_LLA0)

Address: Base address + 5\_81B4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

**IPUx\_DC\_LLA0 field descriptions**

Field	Description
31–24 MCU_RS_3_0	This field holds a pointer in the microcode handling the RS_3 routine for the display defined at DISP_ID_8, when in Low level access mode,
23–16 MCU_RS_2_0	This field holds a pointer in the microcode handling the RS_2 routine for the display defined at DISP_ID_8, when in Low level access mode,
15–8 MCU_RS_1_0	This field holds a pointer in the microcode handling the RS_1 routine for the display defined at DISP_ID_8, when in Low level access mode,
MCU_RS_0_0	This field holds a pointer in the microcode handling the RS_0 routine for the display defined at DISP_ID_8, when in Low level access mode,

**37.5.378 DC Low Level Access Control Register 1  
(IPUx\_DC\_LLA1)**

Address: Base address + 5\_81B8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MCU_RS_3_1				MCU_RS_2_1				MCU_RS_1_1				MCU_RS_0_1																			
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_LLA1 field descriptions**

Field	Description
31–24 MCU_RS_3_1	This field holds a pointer in the microcode handling the RS_3 routine for the display defined at DISP_ID_9, when in Low level access mode,
23–16 MCU_RS_2_1	This field holds a pointer in the microcode handling the RS_2 routine for the display defined at DISP_ID_9, when in Low level access mode,
15–8 MCU_RS_1_1	This field holds a pointer in the microcode handling the RS_1 routine for the display defined at DISP_ID_9, when in Low level access mode,
MCU_RS_0_1	This field holds a pointer in the microcode handling the RS_0 routine for the display defined at DISP_ID_9, when in Low level access mode,

**37.5.379 DC Read Low Level Read Access Control Register 0  
(IPUx\_DC\_R\_LLA0)**

Address: Base address + 5\_81BCh offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MCU_RS_3_0				MCU_RS_2_0				MCU_RS_R_1_0				MCU_RS_R_0_0																			
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_DC\_R\_LLA0 field descriptions**

Field	Description
31–24 MCU_RS_3_0	This field holds a pointer in the microcode handling the RS_3 routine for the display defined at DISP_ID_8, when in Read Low level access mode,
23–16 MCU_RS_2_0	This field holds a pointer in the microcode handling the RS_2 routine for the display defined at DISP_ID_8, when in Read Low level access mode,
15–8 MCU_RS_R_1_0	This field holds a pointer in the microcode handling the RS_1 routine for the display defined at DISP_ID_8, when in Read Low level access mode,
MCU_RS_R_0_0	This field holds a pointer in the microcode handling the RS_0 routine for the display defined at DISP_ID_8, when in Read Low level access mode,

**37.5.380 DC Read Low Level Read Access Control Register1  
(IPUx\_DC\_R\_LLA1)**

Address: Base address + 5\_81C0h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MCU_RS_R_3_1								MCU_RS_R_2_1								MCU_RS_R_1_1								MCU_RS_R_0_1							
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_R\_LLA1 field descriptions**

Field	Description
31–24 MCU_RS_R_3_1	This field holds a pointer in the microcode handling the RS_3 routine for the display defined at DISP_ID_9, when in Read Low level access mode,
23–16 MCU_RS_R_2_1	This field holds a pointer in the microcode handling the RS_2 routine for the display defined at DISP_ID_9, when in Read Low level access mode,
15–8 MCU_RS_R_1_1	This field holds a pointer in the microcode handling the RS_1 routine for the display defined at DISP_ID_9, when in Read Low level access mode,
MCU_RS_R_0_1	This field holds a pointer in the microcode handling the RS_0 routine for the display defined at DISP_ID_9, when in Read Low level access mode,

**37.5.381 DC Write Channel 5 Configuration Register  
(IPUx\_DC\_WR\_CH\_ADDR\_5\_ALT)**

Address: Base address + 5\_81C4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								ST_ADDR_5_ALT																							
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DC\_WR\_CH\_ADDR\_5\_ALT field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
ST_ADDR_5_ ALT	This field defines the start address within the display's memory space where the write transactions will be done to for channel #5, when alternate flow is performed via channel #5

### 37.5.382 DC Status Register (IPUx\_DC\_STAT)

Address: Base address + 5\_81C8h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R										0							
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									DC_TRIPLE_BUF_DATA_EMPTY_1	DC_TRIPLE_BUF_DATA_FULL_1	DC_TRIPLE_BUF_CNT_EMPTY_1	DC_TRIPLE_BUF_CNT_FULL_1	DC_TRIPLE_BUF_DATA_EMPTY_0	DC_TRIPLE_BUF_DATA_FULL_0	DC_TRIPLE_BUF_CNT_EMPTY_0	DC_TRIPLE_BUF_CNT_FULL_0
W																
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0

**IPUx\_DC\_STAT field descriptions**

Field	Description
31–8 Reserved	This read-only field is reserved and always has the value 0.
7 DC_TRIPLE_ BUF_DATA_ EMPTY_1	This bit indicates a FIFO full state on the DC FIFO accessing DI1 when write to the display flow is used
6 DC_TRIPLE_ BUF_DATA_ FULL_1	This bit indicates a FIFO empty state on the DC FIFO accessing DI1 when read from the display flow is used

*Table continues on the next page...*

**IPUx\_DC\_STAT field descriptions (continued)**

Field	Description
5 DC_TRIPLE_ BUF_CNT_ EMPTY_1	This bit indicates a FIFO empty state on the DC FIFO accessing DI1 when write to the display flow is used
4 DC_TRIPLE_ BUF_CNT_ FULL_1	This bit indicates a FIFO full state on the DC FIFO accessing DI1 when write to the display flow is used
3 DC_TRIPLE_ BUF_DATA_ EMPTY_0	This bit indicates a FIFO empty state on the DC FIFO accessing DI0 when read from the display flow is used
2 DC_TRIPLE_ BUF_DATA_ FULL_0	This bit indicates a FIFO full state on the DC FIFO accessing DI0 when read from the display flow is used
1 DC_TRIPLE_ BUF_CNT_ EMPTY_0	This bit indicates a FIFO empty state on the DC FIFO accessing DI0 when write to the display flow is used
0 DC_TRIPLE_ BUF_CNT_ FULL_0	This bit indicates a FIFO full state on the DC FIFO accessing DI0 when write to the display flow is used

**37.5.383 DMFC Read Channel Register (IPUx\_DMFC\_RD\_CHAN)**

Address: Base address + 6\_0000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R				0												
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				0										0		
W																
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	dmfc_ppw_c	dmfc_wm_clr_0	dmfc_wm_set_0	dmfc_wm_en_0	dmfc_burst_size_0	0	0	0	0	0	0	0	0	0	0	0
R																
W																

**IPUx\_DMFC\_RD\_CHAN field descriptions**

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.
25–24 dmfc_ppw_c	<p>Pixel Per Word coded.</p> <p>This field defines the size of the read data from the display.</p> <ul style="list-style-type: none"> <li>00 8 bit per pixel</li> <li>01 16 bit per pixel</li> <li>10 24 (rgb) bit per pixel or 32 bit per pixel</li> <li>11 Reserved</li> </ul>
23–21 dmfc_wm_clr_0	<p>Watermark Clear</p> <p>This field defines the watermark's level of the DMFC read FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of free bursts at the FIFO (dmfc_wm_clr_0 &gt; dmfc_wm_set_0)</p>
20–18 dmfc_wm_set_0	<p>Watermark Set</p> <p>This field defines the watermark's level of the DMFC read FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of free bursts at the FIFO (dmfc_wm_clr_0 &gt; dmfc_wm_set_0)</p>
17 dmfc_wm_en_0	<p>Watermark enable.</p> <p>This bit enables the watermark feature of the FIFO</p> <ul style="list-style-type: none"> <li>1 WM feature is enabled</li> <li>0 WM feature is disabled</li> </ul>
16–8 Reserved	This read-only field is reserved and always has the value 0.
7–6 dmfc_burst_size_0	<p>Read burst Size</p> <p>This field defines the burst size of the DMFC's read accesses. This settings must match the settings in the corresponding IDMAC channel's settings.</p> <ul style="list-style-type: none"> <li>00 32 words of 128 bit (4 pixels of 32 bit each, going to the IDMAC)</li> <li>01 16 words of 128 bit</li> <li>10 8 words of 128 bit</li> <li>11 4 words of 128 bit</li> </ul>
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.384 DMFC Write Channel Register (IPUx\_DMFC\_WR\_CHAN)

Address: Base address + 6\_0004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	dmfc_burst_size_2c		dmfc_fifo_size_2c		dmfc_st_addr_2c		dmfc_burst_size_1c		dmfc_fifo_size_1c		dmfc_st_addr_1c					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	dmfc_burst_size_2		dmfc_fifo_size_2		dmfc_st_addr_2		dmfc_burst_size_1		dmfc_fifo_size_1		dmfc_st_addr_1					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DMFC\_WR\_CHAN field descriptions

Field	Description
31–30 dmfc_burst_size_2c	Burst size of IDMAC's channel 43  This field defines the burst size of the IDMAC's channel 43 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.  00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC) 01 16 words of 128 bit 10 8 words of 128 bit 11 4 words of 128 bit
29–27 dmfc_fifo_size_2c	DMFC FIFO size for IDMAC's channel 43  This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 43  000 All (512X128 words) the DMFC's FIFO is allocated to this channel 001 256X128 words are allocated to this channel 010 128X128 words are allocated to this channel 011 64X128 words are allocated to this channel 100 32X128 words are allocated to this channel 101 16X128 words are allocated to this channel 110 8X128 words are allocated to this channel 111 4X128 words are allocated to this channel
26–24 dmfc_st_addr_2c	DMFC Start Address for IDMAC's channel 43  This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 43. The FIFO is partitioned to 8 equal segments.  Each segment is 64X128 words  The value of this field is the number of the segment  000 Segment 0 001 Segment 1 111 Segment 7
23–22 dmfc_burst_size_1c	Burst size of IDMAC's channel 42  This field defines the burst size of the IDMAC's channel 42 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.

Table continues on the next page...

**IPUx\_DMFC\_WR\_CHAN field descriptions (continued)**

Field	Description
	<p>00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC)      01 16 words of 128 bit      10 8 words of 128 bit      11 4 words of 128 bit</p>
21–19 dmfc_fifo_size_1c	<p>DMFC FIFO size for IDMAC's channel 42      This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 42</p> <p>000 All (512X128 words) the DMFC's FIFO is allocated to this channel      001 256X128 words are allocated to this channel      010 128X128 words are allocated to this channel      011 64X128 words are allocated to this channel      100 32X128 words are allocated to this channel      101 16X128 words are allocated to this channel      110 8X128 words are allocated to this channel      111 4X128 words are allocated to this channel</p>
18–16 dmfc_st_addr_1c	<p>DMFC Start Address for IDMAC's channel 42      This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 42. The FIFO is partitioned to 8 equal segments.      Each segment is 64X128 words      The value of this field is the number of the segment</p> <p>000 Segment 0      001 Segment 1      111 Segment 7</p>
15–14 dmfc_burst_size_2	<p>Burst size of IDMAC's channel 41      This field defines the burst size of the IDMAC's channel 41 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.</p> <p>00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC)      01 16 words of 128 bit      10 8 words of 128 bit      11 4 words of 128 bit</p>
13–11 dmfc_fifo_size_2	<p>DMFC FIFO size for IDMAC's channel 41      This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 41</p> <p>000 All (512X128 words) the DMFC's FIFO is allocated to this channel      001 256X128 words are allocated to this channel      010 128X128 words are allocated to this channel      011 64X128 words are allocated to this channel      100 32X128 words are allocated to this channel      101 16X128 words are allocated to this channel      110 8X128 words are allocated to this channel      111 4X128 words are allocated to this channel</p>
10–8 dmfc_st_addr_2	<p>DMFC Start Address for IDMAC's channel 41      This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 41. The FIFO is partitioned to 8 equal segments.</p>

*Table continues on the next page...*

**IPUx\_DMFC\_WR\_CHAN field descriptions (continued)**

Field	Description
	<p>Each segment is 64X128 words</p> <p>The value of this field is the number of the segment</p> <p>000 Segment 0 001 Segment 1 111 Segment 7</p>
7–6 dmfc_burst_size_1	<p>Burst size of IDMAC's channel 28</p> <p>This field defines the burst size of the IDMAC's channel 28 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.</p> <p>00 32 words of 1bit</p>
5–3 dmfc_fifo_size_1	<p>DMFC FIFO size for IDMAC's channel 28</p> <p>This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 28</p> <p>000 All (512X128 words) the DMFC's FIFO is allocated to this channel 001 256X128 words are allocated to this channel 010 128X128 words are allocated to this channel 011 64X128 words are allocated to this channel 100 32X128 words are allocated to this channel 101 16X128 words are allocated to this channel 110 8X128 words are allocated to this channel 111 4X128 words are allocated to this channel</p>
dmfc_st_addr_1	<p>DMFC Start Address for IDMAC's channel 28</p> <p>This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 28. The FIFO is partitioned to 8 equal segments.</p> <p>Each segment is 64X128 words</p> <p>The value of this field is the number of the segment</p> <p>000 Segment 0 001 Segment 1 111 Segment 7</p>

### 37.5.385 DMFC Write Channel Definition Register (IPUx\_DMFC\_WR\_CHAN\_DEF)

Address: Base address + 6\_0008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	dmfc_wm_clr_2c				dmfc_wm_set_2c			dmfc_wm_en_2c	0	dmfc_wm_clr_1c				dmfc_wm_set_1c	dmfc_wm_en_1c	0
W																
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	dmfc_wm_clr_2				dmfc_wm_set_2			dmfc_wm_en_2	0	dmfc_wm_clr_1				dmfc_wm_set_1	dmfc_wm_en_1	0
W																
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

#### IPUx\_DMFC\_WR\_CHAN\_DEF field descriptions

Field	Description
31–29 dmfc_wm_clr_2c	Watermark Clear This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO ( $dmfc\_wm\_clr > dmfc\_wm\_set$ )
28–26 dmfc_wm_set_2c	Watermark Set This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO ( $dmfc\_wm\_clr > dmfc\_wm\_set$ )
25 dmfc_wm_en_2c	Watermark enable. This bit enables the watermark feature of the FIFO  1 WM feature is enabled 0 WM feature is disabled
24 Reserved	This read-only field is reserved and always has the value 0.
23–21 dmfc_wm_clr_1c	Watermark Clear This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO ( $dmfc\_wm\_clr > dmfc\_wm\_set$ )
20–18 dmfc_wm_set_1c	Watermark Set

Table continues on the next page...

**IPUx\_DMFC\_WR\_CHAN\_DEF field descriptions (continued)**

Field	Description				
	This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)				
17 dmfc_wm_en_1c	<p>Watermark enable.</p> <p>This bit enables the watermark feature of the FIFO</p> <table> <tr> <td>1</td> <td>WM feature is enabled</td> </tr> <tr> <td>0</td> <td>WM feature is disabled</td> </tr> </table>	1	WM feature is enabled	0	WM feature is disabled
1	WM feature is enabled				
0	WM feature is disabled				
16 Reserved	This read-only field is reserved and always has the value 0.				
15–13 dmfc_wm_clr_2	<p>Watermark Clear</p> <p>This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr &gt; dmfc_wm_set)</p>				
12–10 dmfc_wm_set_2	<p>Watermark Set</p> <p>This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr &gt; dmfc_wm_set)</p>				
9 dmfc_wm_en_2	<p>Watermark enable.</p> <p>This bit enables the watermark feature of the FIFO</p> <table> <tr> <td>1</td> <td>WM feature is enabled</td> </tr> <tr> <td>0</td> <td>WM feature is disabled</td> </tr> </table>	1	WM feature is enabled	0	WM feature is disabled
1	WM feature is enabled				
0	WM feature is disabled				
8 Reserved	This read-only field is reserved and always has the value 0.				
7–5 dmfc_wm_clr_1	<p>Watermark Clear</p> <p>This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr &gt; dmfc_wm_set)</p>				
4–2 dmfc_wm_set_1	<p>Watermark Set</p> <p>This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr &gt; dmfc_wm_set)</p>				
1 dmfc_wm_en_1	<p>Watermark enable.</p> <p>This bit enables the watermark feature of the FIFO</p> <table> <tr> <td>1</td> <td>WM feature is enabled</td> </tr> <tr> <td>0</td> <td>WM feature is disabled</td> </tr> </table>	1	WM feature is enabled	0	WM feature is disabled
1	WM feature is enabled				
0	WM feature is disabled				
0 Reserved	This read-only field is reserved and always has the value 0.				

### 37.5.386 DMFC Display Processor Channel Register (IPUx\_DMFC\_DP\_CHAN)

Address: Base address + 6\_000Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	dmfc_burst_size_6f		dmfc_fifo_size_6f		dmfc_st_addr_6f		dmfc_burst_size_6b		dmfc_fifo_size_6b		dmfc_st_addr_6b					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	dmfc_burst_size_5f		dmfc_fifo_size_5f		dmfc_st_addr_5f		dmfc_burst_size_5b		dmfc_fifo_size_5b		dmfc_st_addr_5b					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DMFC\_DP\_CHAN field descriptions

Field	Description
31–30 dmfc_burst_size_6f	Burst size of IDMAC's channel 29  This field defines the burst size of the IDMAC's channel 29 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.  00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC) 01 16 words of 128 bit 10 8 words of 128 bit 11 4 words of 128 bit
29–27 dmfc_fifo_size_6f	DMFC FIFO size for IDMAC's channel 29  This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 29  000 All (512X128 words) the DMFC's FIFO is allocated to this channel 001 256X128 words are allocated to this channel 010 128X128 words are allocated to this channel 011 64X128 words are allocated to this channel 100 32X128 words are allocated to this channel 101 16X128 words are allocated to this channel 110 8X128 words are allocated to this channel 111 4X128 words are allocated to this channel
26–24 dmfc_st_addr_6f	DMFC Start Address for IDMAC's channel 29  This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 29. The FIFO is partitioned to 8 equal segments.  Each segment is 64X128 words  The value of this field is the number of the segment  000 Segment 0 001 Segment 1 111 Segment 7

Table continues on the next page...

**IPUx\_DMFC\_DP\_CHAN field descriptions (continued)**

Field	Description
23–22 dmfc_burst_size_6b	Burst size of IDMAC's channel 24  This field defines the burst size of the IDMAC's channel 24 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.  00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC) 01 16 words of 128 bit 10 8 words of 128 bit 11 4 words of 128 bit
21–19 dmfc_fifo_size_6b	DMFC FIFO size for IDMAC's channel 24  This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 24  000 All (512X128 words) the DMFC's FIFO is allocated to this channel 001 256X128 words are allocated to this channel 010 128X128 words are allocated to this channel 011 64X128 words are allocated to this channel 100 32X128 words are allocated to this channel 101 16X128 words are allocated to this channel 110 8X128 words are allocated to this channel 111 4X128 words are allocated to this channel
18–16 dmfc_st_addr_6b	DMFC Start Address for IDMAC's channel 24  This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 24. The FIFO is partitioned to 8 equal segments.  Each segment is 64X128 words  The value of this field is the number of the segment  000 Segment 0 001 Segment 1 111 Segment 7
15–14 dmfc_burst_size_5f	Burst size of IDMAC's channel 27  This field defines the burst size of the IDMAC's channel 27 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.  00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC) 01 16 words of 128 bit 10 8 words of 128 bit 11 4 words of 128 bit
13–11 dmfc_fifo_size_5f	DMFC FIFO size for IDMAC's channel 27  This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 27  000 All (512X128 words) the DMFC's FIFO is allocated to this channel 001 256X128 words are allocated to this channel 010 128X128 words are allocated to this channel 011 64X128 words are allocated to this channel 100 32X128 words are allocated to this channel 101 16X128 words are allocated to this channel 110 8X128 words are allocated to this channel 111 4X128 words are allocated to this channel

*Table continues on the next page...*

**IPUx\_DMFC\_DP\_CHAN field descriptions (continued)**

Field	Description																
10–8 dmfc_st_addr_5f	<p>DMFC Start Address for IDMAC's channel 27</p> <p>This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 27. The FIFO is partitioned to 8 equal segments.</p> <p>Each segment is 64X128 words</p> <p>The value of this field is the number of the segment</p> <table> <tr><td>000</td><td>Segment 0</td></tr> <tr><td>001</td><td>Segment 1</td></tr> <tr><td>111</td><td>Segment 7</td></tr> </table>	000	Segment 0	001	Segment 1	111	Segment 7										
000	Segment 0																
001	Segment 1																
111	Segment 7																
7–6 dmfc_burst_size_5b	<p>Burst size of IDMAC's channel 23</p> <p>This field defines the burst size of the IDMAC's channel 23 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.</p> <table> <tr><td>00</td><td>32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC)</td></tr> <tr><td>01</td><td>16 words of 128 bit</td></tr> <tr><td>10</td><td>8 words of 128 bit</td></tr> <tr><td>11</td><td>4 words of 128 bit</td></tr> </table>	00	32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC)	01	16 words of 128 bit	10	8 words of 128 bit	11	4 words of 128 bit								
00	32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC)																
01	16 words of 128 bit																
10	8 words of 128 bit																
11	4 words of 128 bit																
5–3 dmfc_fifo_size_5b	<p>DMFC FIFO size for IDMAC's channel 23</p> <p>This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 23</p> <table> <tr><td>000</td><td>All (512X128 words) the DMFC's FIFO is allocated to this channel</td></tr> <tr><td>001</td><td>256X128 words are allocated to this channel</td></tr> <tr><td>010</td><td>128X128 words are allocated to this channel</td></tr> <tr><td>011</td><td>64X128 words are allocated to this channel</td></tr> <tr><td>100</td><td>32X128 words are allocated to this channel</td></tr> <tr><td>101</td><td>16X128 words are allocated to this channel</td></tr> <tr><td>110</td><td>8X128 words are allocated to this channel</td></tr> <tr><td>111</td><td>4X128 words are allocated to this channel</td></tr> </table>	000	All (512X128 words) the DMFC's FIFO is allocated to this channel	001	256X128 words are allocated to this channel	010	128X128 words are allocated to this channel	011	64X128 words are allocated to this channel	100	32X128 words are allocated to this channel	101	16X128 words are allocated to this channel	110	8X128 words are allocated to this channel	111	4X128 words are allocated to this channel
000	All (512X128 words) the DMFC's FIFO is allocated to this channel																
001	256X128 words are allocated to this channel																
010	128X128 words are allocated to this channel																
011	64X128 words are allocated to this channel																
100	32X128 words are allocated to this channel																
101	16X128 words are allocated to this channel																
110	8X128 words are allocated to this channel																
111	4X128 words are allocated to this channel																
dmfc_st_addr_5b	<p>DMFC Start Address for IDMAC's channel 23</p> <p>This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 23. The FIFO is partitioned to 8 equal segments.</p> <p>Each segment is 64X128 words</p> <p>The value of this field is the number of the segment</p> <table> <tr><td>000</td><td>Segment 0</td></tr> <tr><td>001</td><td>Segment 1</td></tr> <tr><td>111</td><td>Segment 7</td></tr> </table>	000	Segment 0	001	Segment 1	111	Segment 7										
000	Segment 0																
001	Segment 1																
111	Segment 7																

### 37.5.387 DMFC Display Processor Channel Definition Register (IPUx\_DMFC\_DP\_CHAN\_DEF)

Address: Base address + 6\_0010h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R							dmfc_wm_en_6f	0							dmfc_wm_en_6b	0
W	dmfc_wm_clr_6f			dmfc_wm_set_6f					dmfc_wm_clr_6b		dmfc_wm_set_6b					
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R							dmfc_wm_en_5f	0							dmfc_wm_en_5b	0
W	dmfc_wm_clr_5f			dmfc_wm_set_5f					dmfc_wm_clr_5b		dmfc_wm_set_5b					
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

#### IPUx\_DMFC\_DP\_CHAN\_DEF field descriptions

Field	Description
31–29 dmfc_wm_clr_6f	Watermark Clear This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO ( $dmfc\_wm\_clr > dmfc\_wm\_set$ )
28–26 dmfc_wm_set_6f	Watermark Set This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO ( $dmfc\_wm\_clr > dmfc\_wm\_set$ )
25 dmfc_wm_en_6f	Watermark enable. This bit enables the watermark feature of the FIFO  1 WM feature is enabled 0 WM feature is disabled
24 Reserved	This read-only field is reserved and always has the value 0.
23–21 dmfc_wm_clr_6b	Watermark Clear This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO ( $dmfc\_wm\_clr > dmfc\_wm\_set$ )
20–18 dmfc_wm_set_6b	Watermark Set

Table continues on the next page...

**IPUx\_DMFC\_DP\_CHAN\_DEF field descriptions (continued)**

Field	Description
	This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)
17 dmfc_wm_en_6b	<p>Watermark enable.</p> <p>This bit enables the watermark feature of the FIFO</p> <p>1 WM feature is enabled 0 WM feature is disabled</p>
16 Reserved	This read-only field is reserved and always has the value 0.
15–13 dmfc_wm_clr_5f	<p>Watermark Clear</p> <p>This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr &gt; dmfc_wm_set)</p>
12–10 dmfc_wm_set_5f	<p>Watermark Set</p> <p>This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr &gt; dmfc_wm_set)</p>
9 dmfc_wm_en_5f	<p>Watermark enable.</p> <p>This bit enables the watermark feature of the FIFO</p> <p>1 WM feature is enabled 0 WM feature is disabled</p>
8 Reserved	This read-only field is reserved and always has the value 0.
7–5 dmfc_wm_clr_5b	<p>Watermark Clear</p> <p>This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr &gt; dmfc_wm_set)</p>
4–2 dmfc_wm_set_5b	<p>Watermark Set</p> <p>This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr &gt; dmfc_wm_set)</p>
1 dmfc_wm_en_5b	<p>Watermark enable.</p> <p>This bit enables the watermark feature of the FIFO</p> <p>1 WM feature is enabled 0 WM feature is disabled</p>
0 Reserved	This read-only field is reserved and always has the value 0.

### 37.5.388 DMFC General 1 Register (IPUx\_DMFC\_GENERAL\_1)

Address: Base address + 6\_0014h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R								WAIT4EOT_9	WAIT4EOT_6F	WAIT4EOT_6B	WAIT4EOT_5F	WAIT4EOT_5B	WAIT4EOT_4	WAIT4EOT_3	WAIT4EOT_2	WAIT4EOT_1
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R							dmfc_wm_en_9	0	0				0			dmfc_dcdp_sync_pr
W							dmfc_wm_clr_9	dmfc_wm_set_9								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

#### IPUx\_DMFC\_GENERAL\_1 field descriptions

Field	Description
31–25 Reserved	This read-only field is reserved and always has the value 0.
24 WAIT4EOT_9	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode. 1 FIFO #9 is in wait4eot mode 0 FIFO #9 is in normal mode
23 WAIT4EOT_6F	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode. 1 FIFO #6F is in wait4eot mode 0 FIFO #6F is in normal mode
22 WAIT4EOT_6B	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode. 1 FIFO #6B is in wait4eot mode 0 FIFO #6B is in normal mode

Table continues on the next page...

**IPUx\_DMFC\_GENERAL\_1 field descriptions (continued)**

Field	Description
21 WAIT4EOT_5F	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode.  1 FIFO #5F is in wait4eot mode 0 FIFO #5F is in normal mode
20 WAIT4EOT_5B	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode.  1 FIFO #5B is in wait4eot mode 0 FIFO #5B is in normal mode
19 WAIT4EOT_4	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode.  1 FIFO #4 is in wait4eot mode 0 FIFO #4 is in normal mode
18 WAIT4EOT_3	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode.  1 FIFO #3 is in wait4eot mode 0 FIFO #3 is in normal mode
17 WAIT4EOT_2	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode.  1 FIFO #2 is in wait4eot mode 0 FIFO #2 is in normal mode
16 WAIT4EOT_1	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode.  1 FIFO #1 is in wait4eot mode 0 FIFO #1 is in normal mode
15–13 dmfc_wm_clr_9	Watermark Clear  This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)

*Table continues on the next page...*

**IPUx\_DMFC\_GENERAL\_1 field descriptions (continued)**

Field	Description
12–10 dmfc_wm_set_9	Watermark Set This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)
9 dmfc_wm_en_9	Watermark enable. This bit enables the watermark feature of the FIFO 1 WM feature is enabled 0 WM feature is disabled
8 Reserved	This read-only field is reserved and always has the value 0.
7 Reserved	This read-only field is reserved and always has the value 0.
6–5 dmfc_burst_size_9	Burst size of IDMAC's channel 44 This field defines the burst size of the IDMAC's channel 44 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings. This channel is targeted for MASK - the FIFO size is always 32X128; The base address is always the upper half of the 8th segment 00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC) 01 16 words of 128 bit 10 8 words of 128 bit 11 4 words of 128 bit
4–2 Reserved	This read-only field is reserved and always has the value 0.
dmfc_dcdp_sync_pr	DMFC's memory access priority settings for simultaneous synchronous flows from DC & DP 00 Forbidden - should not be used. 01 DC has higher priority over DP 10 DP has higher priority over DC 11 Round Robin

**37.5.389 DMFC General 2 Register (IPUx\_DMFC\_GENERAL\_2)**

Address: Base address + 6\_0018h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_DMFC\_GENERAL\_2 field descriptions**

Field	Description
31–29 Reserved	This read-only field is reserved and always has the value 0.
28–16 dmfc_frame_height_rd	Frame height for read channel from the display to the IDMAC; Units are pixels
15–13 Reserved	This read-only field is reserved and always has the value 0.
dmfc_frame_width_rd	Frame width for read channel from the display to the IDMAC; Units are pixels

**37.5.390 DMFC IC Interface Control Register (IPUx\_DMFC\_IC\_CTRL)**

Address: Base address + 6\_001Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	dmfc_ic_frame_height_rd														dmfc_ic_frame_width_rd	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	dmfc_ic_frame_width_rd														dmfc_ic_ppw_c	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

**IPUx\_DMFC\_IC\_CTRL field descriptions**

Field	Description
31–19 dmfc_ic_frame_height_rd	Frame's height for the channel coming from IC. Units are lines
18–6 dmfc_ic_frame_width_rd	Frame's width for the channel coming from IC. Units are pixels
5–4 dmfc_ic_ppw_c	Pixel Per Word coded from IC. This field defines the size of the data coming from the IC.  00 8 bit per pixel 01 16 bit per pixel 10 24 bit per pixel 11 Reserved
3 Reserved	This read-only field is reserved and always has the value 0.
dmfc_ic_in_port	DMFC input port

Table continues on the next page...

**IPUx\_DMFC\_IC\_CTRL field descriptions (continued)**

Field	Description
	<p>When data is coming from the IC, the IC channel replaces one of the IDMAC's channels connected to the DMFC. This field defines which IDMAC's channel is replaced by the IC channel.</p> <p>000 CH28      001 CH41      010 Reserved, IC channel is disabled      011 Reserved, IC channel is disabled      100 CH23      101 CH27      110 CH24      111 CH29</p>

**37.5.391 DMFC Write Channel Alternate Register (IPUx\_DMFC\_WR\_CHAN\_ALT)**

Address: Base address + 6\_0020h offset

Bit	31	30	29	28	27	26	25	24		23	22	21	20	19	18	17	16
R									0								
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
R	dmfc_burst_size_2_alt		dmfc_fifo_size_2_alt		dmfc_st_addr_2_alt					0							
W																	
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0

**IPUx\_DMFC\_WR\_CHAN\_ALT field descriptions**

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.
15–14 dmfc_burst_size_2_alt	Burst size of IDMAC's channel 41 (for alternate flow)  This field defines the burst size of the IDMAC's channel 41 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.  00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC) 01 16 words of 128 bit 10 8 words of 128 bit 11 4 words of 128 bit
13–11 dmfc_fifo_size_2_alt	DMFC FIFO size for IDMAC's channel 41 (for alternate flow)  This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 41  000 All (512X128 words) the DMFC's FIFO is allocated to this channel 001 256X128 words are allocated to this channel 010 128X128 words are allocated to this channel

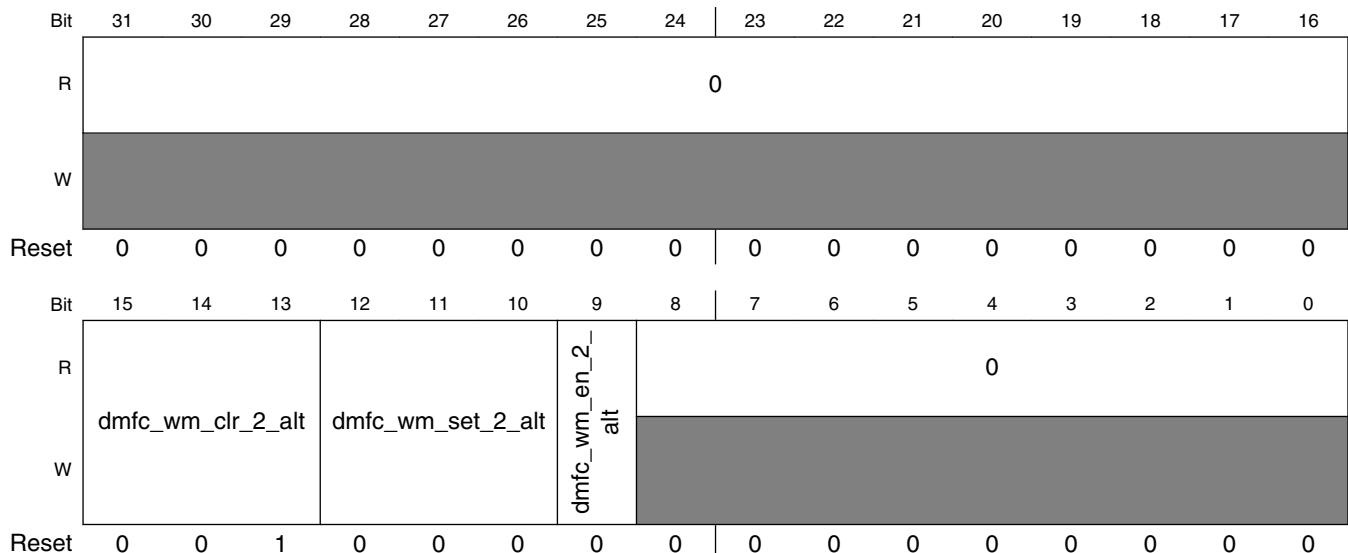
Table continues on the next page...

**IPUx\_DMFC\_WR\_CHAN\_ALT field descriptions (continued)**

Field	Description
	011 64X128 words are allocated to this channel 100 32X128 words are allocated to this channel 101 16X128 words are allocated to this channel 110 8X128 words are allocated to this channel 111 4X128 words are allocated to this channel
10–8 dmfc_st_addr_2 alt	DMFC Start Address for IDMAC's channel 41 (for alternate flow) This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 41. The FIFO is partitioned to 8 equal segments. Each segment is 64X128 words The value of this field is the number of the segment 000 Segment 0 001 Segment 1 111 Segment 7
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.392 DMFC Write Channel Definition Alternate Register (IPUx\_DMFC\_WR\_CHAN\_DEF\_ALT)

Address: Base address + 6\_0024h offset

**IPUx\_DMFC\_WR\_CHAN\_DEF\_ALT field descriptions**

Field	Description
31–16 Reserved	This read-only field is reserved and always has the value 0.

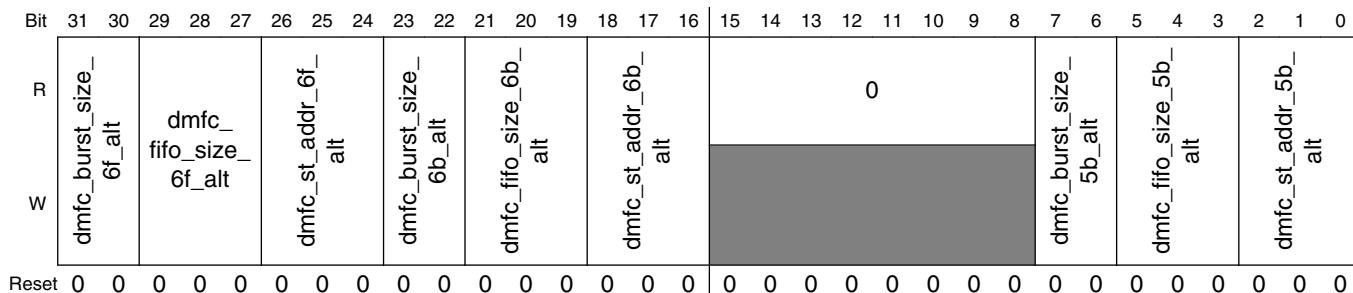
Table continues on the next page...

**IPUx\_DMFC\_WR\_CHAN\_DEF\_ALT field descriptions (continued)**

Field	Description
15–13 dmfc_wm_clr_2_alt	Watermark Clear (for alternate flow)  This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)
12–10 dmfc_wm_set_2_alt	Watermark Set (for alternate flow)  This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)
9 dmfc_wm_en_2_alt	Watermark enable. (for alternate flow)  This bit enables the watermark feature of the FIFO  1 WM feature is enabled 0 WM feature is disabled
Reserved	This read-only field is reserved and always has the value 0.

**37.5.393 DMFC MFC Display Processor Channel Alternate Register (IPUx\_DMFC\_DP\_CHAN\_ALT)**

Address: Base address + 6\_0028h offset

**IPUx\_DMFC\_DP\_CHAN\_ALT field descriptions**

Field	Description
31–30 dmfc_burst_size_6f_alt	Burst size of IDMAC's channel 29 (for alternate flow)  This field defines the burst size of the IDMAC's channel 29 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.  00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC) 01 16 words of 128 bit 10 8 words of 128 bit 11 4 words of 128 bit
29–27 dmfc_fifo_size_6f_alt	DMFC FIFO size for IDMAC's channel 29 (for alternate flow)  This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 29  000 All (512X128 words) the DMFC's FIFO is allocated to this channel

Table continues on the next page...

**IPUx\_DMFC\_DP\_CHAN\_ALT field descriptions (continued)**

Field	Description
	<p>001 256X128 words are allocated to this channel      010 128X128 words are allocated to this channel      011 64X128 words are allocated to this channel      100 32X128 words are allocated to this channel      101 16X128 words are allocated to this channel      110 8X128 words are allocated to this channel      111 4X128 words are allocated to this channel</p>
26–24 dmfc_st_addr_6f_alt	<p>DMFC Start Address for IDMAC's channel 29 (for alternate flow)      This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 29. The FIFO is partitioned to 8 equal segments.      Each segment is 64X128 words      The value of this field is the number of the segment</p> <p>000 Segment 0      001 Segment 1      111 Segment 7</p>
23–22 dmfc_burst_size_6b_alt	<p>Burst size of IDMAC's channel 24 (for alternate flow)      This field defines the burst size of the IDMAC's channel 24 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.</p> <p>00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC)      01 16 words of 128 bit      10 8 words of 128 bit      11 4 words of 128 bit</p>
21–19 dmfc_fifo_size_6b_alt	<p>DMFC FIFO size for IDMAC's channel 24 (for alternate flow)      This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 24</p> <p>000 All (512X128 words) the DMFC's FIFO is allocated to this channel      001 256X128 words are allocated to this channel      010 128X128 words are allocated to this channel      011 64X128 words are allocated to this channel      100 32X128 words are allocated to this channel      101 16X128 words are allocated to this channel      110 8X128 words are allocated to this channel      111 4X128 words are allocated to this channel</p>
18–16 dmfc_st_addr_6b_alt	<p>DMFC Start Address for IDMAC's channel 24 (for alternate flow)      This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 24. The FIFO is partitioned to 8 equal segments.      Each segment is 64X128 words      The value of this field is the number of the segment</p> <p>000 Segment 0      001 Segment 1      111 Segment 7</p>
15–8 Reserved	This read-only field is reserved and always has the value 0.

*Table continues on the next page...*

**IPUx\_DMFC\_DP\_CHAN\_ALT field descriptions (continued)**

Field	Description
7–6 dmfc_burst_size_5b_alt	<p>Burst size of IDMAC's channel 23 (for alternate flow)</p> <p>This field defines the burst size of the IDMAC's channel 23 write accesses. This settings must match the settings in the corresponding IDMAC channel's settings.</p> <ul style="list-style-type: none"> <li>00 32 words of 128 bit (4 pixels of 32 bit each, coming from the IDMAC)</li> <li>01 16 words of 128 bit</li> <li>10 8 words of 128 bit</li> <li>11 4 words of 128 bit</li> </ul>
5–3 dmfc_fifo_size_5b_alt	<p>DMFC FIFO size for IDMAC's channel 23 (for alternate flow)</p> <p>This field defines the FIFO partition for the DMFC channel connected to IDMAC's channel 23</p> <ul style="list-style-type: none"> <li>000 All (512X128 words) the DMFC's FIFO is allocated to this channel</li> <li>001 256X128 words are allocated to this channel</li> <li>010 128X128 words are allocated to this channel</li> <li>011 64X128 words are allocated to this channel</li> <li>100 32X128 words are allocated to this channel</li> <li>101 16X128 words are allocated to this channel</li> <li>110 8X128 words are allocated to this channel</li> <li>111 4X128 words are allocated to this channel</li> </ul>
dmfc_st_addr_5b_alt	<p>DMFC Start Address for IDMAC's channel 23 (for alternate flow)</p> <p>This field defines the base address at the DMFC's FIFO of the partition allocated to the channel connected to IDMAC's channel 23. The FIFO is partitioned to 8 equal segments.</p> <p>Each segment is 64X128 words</p> <p>The value of this field is the number of the segment</p> <ul style="list-style-type: none"> <li>000 Segment 0</li> <li>001 Segment 1</li> <li>111 Segment 7</li> </ul>

### 37.5.394 DMFC Display Channel Definition Alternate Register (IPUx\_DMFC\_DP\_CHAN\_DEF\_ALT)

Address: Base address + 6\_002Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R							dmfc_wm_en_6f_alt	0	dmfc_wm_clr_6b_alt				dmfc_wm_set_6b_alt		dmfc_wm_en_6b_alt	0
W	dmfc_wm_clr_6f_alt			dmfc_wm_set_6f_alt												
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R								0	dmfc_wm_clr_5b_alt				dmfc_wm_set_5b_alt		dmfc_wm_en_5b_alt	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

#### IPUx\_DMFC\_DP\_CHAN\_DEF\_ALT field descriptions

Field	Description
31–29 dmfc_wm_clr_6f_alt	Watermark Clear (for alternate flow) This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)
28–26 dmfc_wm_set_6f_alt	Watermark Set (for alternate flow) This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)
25 dmfc_wm_en_6f_alt	Watermark enable. (for alternate flow) This bit enables the watermark feature of the FIFO 1 WM feature is enabled 0 WM feature is disabled
24 Reserved	This read-only field is reserved and always has the value 0.
23–21 dmfc_wm_clr_6b_alt	Watermark Clear (for alternate flow) This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)

Table continues on the next page...

**IPUx\_DMFC\_DP\_CHAN\_DEF\_ALT field descriptions (continued)**

Field	Description
20–18 dmfc_wm_set_6b_alt	Watermark Set (for alternate flow)  This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)
17 dmfc_wm_en_6b_alt	Watermark enable. (for alternate flow)  This bit enables the watermark feature of the FIFO  1 WM feature is enabled 0 WM feature is disabled
16–8 Reserved	This read-only field is reserved and always has the value 0.
7–5 dmfc_wm_clr_5b_alt	Watermark Clear (for alternate flow)  This field defines the watermark's level of the DMFC's write FIFO. Crossing this level will clear the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)
4–2 dmfc_wm_set_5b_alt	Watermark Set (for alternate flow)  This field defines the watermark's level of the DMFC write FIFO. Crossing this level will send the watermark signal to the IDMAC. The WM level is the amount of occupied bursts at the FIFO (dmfc_wm_clr > dmfc_wm_set)
1 dmfc_wm_en_5b_alt	Watermark enable. (for alternate flow)  This bit enables the watermark feature of the FIFO  1 WM feature is enabled 0 WM feature is disabled
0 Reserved	This read-only field is reserved and always has the value 0.

### 37.5.395 DMFC General 1 Alternate Register (IPUx\_DMFC\_GENERAL1\_ALT)

Address: Base address + 6\_0030h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0								WAIT4EOT_6F_	WAIT4EOT_6B_	0	WAIT4EOT_5B_	0	0	WAIT4EOT_2_	0
W									ALT	ALT	ALT	ALT	ALT	ALT	ALT	ALT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### IPUx\_DMFC\_GENERAL1\_ALT field descriptions

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23 WAIT4EOT_6F_	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode. 1 FIFO #6F is in wait4eot mode (for alternate flow) 0 FIFO #6F is in normal mode (for alternate flow)
22 WAIT4EOT_6B_	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode. 1 FIFO #6B is in wait4eot mode (for alternate flow) 0 FIFO #6B is in normal mode (for alternate flow)
21 Reserved	This read-only field is reserved and always has the value 0.
20 WAIT4EOT_5B_	In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO. When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode) When the FIFO is larger then the size of the line, the user should work in wait4eot mode.

Table continues on the next page...

**IPUx\_DMFC\_GENERAL1\_ALT field descriptions (continued)**

Field	Description
	1 FIFO #5B is in wait4eot mode (for alternate flow) 0 FIFO #5B is in normal mode (for alternate flow)
19–18 Reserved	This read-only field is reserved and always has the value 0.
17 WAIT4EOT_2_ ALT	<p>In normal operation the DMFC sends requests to the IDMAC whenever there is room in the FIFO.</p> <p>When this bit is set the DMFC sends the request only after the current transfer is terminated, (wait4eot mode)</p> <p>When the FIFO is larger then the size of the line, the user should work in wait4eot mode.</p> <p>1 FIFO #2 is in wait4eot mode (for alternate flow)            0 FIFO #2 is in normal mode (for alternate flow)</p>
Reserved	This read-only field is reserved and always has the value 0.

### 37.5.396 DMFC Status Register (IPUx\_DMFC\_STAT)

This register contains DMFC's status bits. All the bits in this register are read-only.

Address: Base address + 6\_0034h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R							DMFC_IC_BUFFER_EMPTY									
	0															
W																
Reset	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DMFC_FIFO_EMPTY_i								DMFC_FIFO_FULL_i							
W																
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

IPUx\_DMFC\_STAT field descriptions

Field	Description
31–26 Reserved	This read-only field is reserved and always has the value 0.
25 DMFC_IC_ BUFFER_ EMPTY	This bit indicates on a IC FIFO, inside the DMFC, empty condition. 0 IC FIFO not empty 1 IC FIFO is empty

Table continues on the next page...

**IPUx\_DMFC\_STAT field descriptions (continued)**

Field	Description
24 DMFC_IC_ BUFFER_FULL	This bit indicates on a IC FIFO, inside the DMFC, full condition. 0 IC FIFO not full 1 IC FIFO is full
23–12 DMFC_FIFO_ EMPTY_i	This bit indicates on a DMFC FIFO#<i> empty condition. Mapping of these bit to an actual FIFO number is as follows: bit 0 => 0 bit 1=> 1 bit 2 => 2 bit 3 =>1c bit 4 => 2c bit 5 => 5b bit 6 => 5f bit 7 => 6b bit 8 => 6f bit 9 => 9 bit 10 => 10 (ARM platform access) bit 11 => 11 (ARM platform access) 0 FIFO #<i> is not empty 1 FIFO #<i> is empty
DMFC_FIFO_ FULL_i	This bit indicates on a DMFC FIFO#<i> full condition. Mapping of these bit to an actual FIFO number is as follows: bit 0 => 0 bit 1=> 1 bit 2 => 2 bit 3 =>1c bit 4 => 2c bit 5 => 5b bit 6 => 5f bit 7 => 6b bit 8 => 6f bit 9 => 9 bit 10 => 10 (ARM platform access) bit 11 => 11 (ARM platform access) 0 FIFO #<i> is not full 1 FIFO #<i> is full

**37.5.397 VDI Field Size Register (IPUx\_VDI\_FSIZE)**

The register used to control size of VDIC input fields.

Address: Base address + 6\_8000h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

**IPUx\_VDI\_FSIZE field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 VDI_FHEIGHT	Frame height The value to be written to this register is the frame's height minus 1. The frame height should not be smaller than 16. When VDI_CMB_EN bit is clear: <ul style="list-style-type: none"><li>• The frame height should not be greater than 1080.</li><li>• The frame's height must be even (which means that both fields have the same height)</li><li>• The frame's height in 4:2:0 format, must be multiple of 4 (which means that both chroma fields have the same height)</li></ul>

Table continues on the next page...

**IPUx\_VDI\_FSIZE field descriptions (continued)**

Field	Description
	<p>When VDI_CMB_EN bit is set:</p> <ul style="list-style-type: none"> <li>The frame height should not be greater than 1200.</li> </ul>
15–11 Reserved	This read-only field is reserved and always has the value 0.
VDI_FWIDTH	<p>Frame width.</p> <p>The value to be written to this register is the frame's width minus 1.</p> <p>The Frame width should not be smaller than 16.</p> <p>The width must be even.</p> <p>When VDI_CMB_EN bit is clear</p> <ul style="list-style-type: none"> <li>The Frame width should not be greater than 720968.</li> </ul> <p>When VDI_CMB_EN bit is set:</p> <ul style="list-style-type: none"> <li>The Frame width should not be greater than 1920.</li> </ul>

**37.5.398 VDI Control Register (IPUx\_VDI\_C)**

The register used to control modes of operations of VDIC module.

Address: Base address + 6\_8004h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	-	-	0		VDI_VWM3_CLR		VDI_VWM3_SET		VDI_VWM1_CLR		VDI_VWM1_SET					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		VDI_BURST_SIZE3		VDI_BURST_SIZE2		VDI_BURST_SIZE1		VDI_MOT_SEL		VDI_CH_422		0				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_VDI\_C field descriptions**

Field	Description
31 -	<p>VDIC top filed (automatic)</p> <p>This defines what would be the top field to be processed when the data is coming from the CSI</p> <p>0 top field is field 0 1 top field is field 1</p>
30 -	<p>VDIC top filed (manual)</p> <p>This defines what would be the next top field to be processed when the data is coming from the memory</p>

*Table continues on the next page...*

**IPUx\_VDI\_C field descriptions (continued)**

Field	Description
	0 top field is field 0 1 top field is field 1
29–28 Reserved	This read-only field is reserved and always has the value 0.
27–25 VDI_VWM3_CLR	VDIC WaterMark "clear" level for channel 3. 0 clear watermark level when FIFO3 is full on 1/8 of their size. 1 clear watermark level when FIFO3 is full on 2/8 of their size. 7 clear watermark level when FIFO3 is full.
24–22 VDI_VWM3_SET	VDIC WaterMark "set" level for channel 3. 0 set watermark level when FIFO3 is full on 1/8 of their size. 1 set watermark level when FIFO3 is full on 2/8 of their size. 7 set watermark level when FIFO3 is full.
21–19 VDI_VWM1_CLR	VDIC WaterMark "clear" level for channel 1 or channel 4 (channels 1 and 4 are not working simultaneously). 0 clear watermark level when FIFO1 is full on 1/8 of their size. 1 clear watermark level when FIFO1 is full on 2/8 of their size. 7 clear watermark level when FIFO1 is full.
18–16 VDI_VWM1_SET	VDIC WaterMark "set" level for channel 1 or channel 2 (channels 1 and 4 are not working simultaneously). 0 set watermark level when FIFO1 is full on 1/8 of their size. 1 set watermark level when FIFO1 is full on 2/8 of their size. 7 set watermark level when FIFO1 is full.
15–12 VDI_BURST_SIZE3	Burst Size for channel 3. The VDIC's burst size is restrict by the IDMAC's restriction - This value must match the IDMAC settings and follow the IDMAC's restrictions 0 Burst size is 1 access. 1 Burst size is 2 accesses. 15 Burst size is 16 accesses.
11–8 VDI_BURST_SIZE2	Burst Size for channel 2. The VDIC's burst size is restrict by the IDMAC's restriction - This value must match the IDMAC settings and follow the IDMAC's restrictions 0 Burst size is 1 access. 1 Burst size is 2 accesses. 15 Burst size is 16 accesses.
7–4 VDI_BURST_SIZE1	Burst Size for channels 1 or 4 (channels 1 and 4 are not working simultaneously). The VDIC's burst size is restrict by the IDMAC's restriction - This value must match the IDMAC settings and follow the IDMAC's restrictions 0 Burst size is 1 access. 1 Burst size is 2 accesses. 15 Burst size is 16 accesses.
3–2 VDI_MOT_SEL	Motion select.

*Table continues on the next page...*

**IPUx\_VDI\_C field descriptions (continued)**

Field	Description
	0 Motion determined by ROM "1" (shared toward medium/high motion). 1 Motion determined by ROM "2" (This option will not work well for high motion). 2 Full motion, only vertical filter is used 3 Forbidden.
1 VDI_CH_422	Chroma format at input and output of VDIC. 0 Chroma format is 420. 1 Chroma format is 422.
0 Reserved	This read-only field is reserved and always has the value 0.

**37.5.399 VDI Control Register 2 (IPUx\_VDI\_C2\_)**

The register used to control modes of operations of VDIC module.

Address: Base address + 6\_8008h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R									0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									0				VDI_PLANE_1_EN	VDI_GLB_A_EN	VDI_KEY_COLOR_EN	VDI_CMB_EN
W													0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**IPUx\_VDI\_C2\_ field descriptions**

Field	Description
31–4 Reserved	This read-only field is reserved and always has the value 0.
3 VDI_PLANE_1_EN	Plane 1 enable 0 plane #1 is disabled 1 plane #1 is enabled

Table continues on the next page...

**IPUx\_VDI\_C2\_field descriptions (continued)**

Field	Description
2 VDI_GLB_A_EN	Global alpha enable 0 Alpha is local 1 Alpha is global
1 VDI_KEY_COLOR_EN	Key Color Enable 0 Key Color disabled. 1 Key color enabled
0 VDI_CMB_EN	Combining enable 0 Combining disabled. The VDIC works in de-interlacing mode 1 Combining enabled. The de-interlacing mode is not functional

### 37.5.400 VDI Combining Parameters Register 1 (IPUx\_VDI\_CMDP\_1)

The register holds combining parameters.

Address: Base address + 6\_800Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R																																	
W																																	

Reset 0

**IPUx\_VDI\_CMDP\_1 field descriptions**

Field	Description
31–24 VDI_ALPHA	Global Alpha Actual value of the alpha is VDI_ALPHA + VDI_ALPHA[7]
23–16 VDI_KEY_COLOR_R	Red component of Key Color
15–8 VDI_KEY_COLOR_G	Green component of Key Color
VDI_KEY_COLOR_B	Blue component of Key Color

### 37.5.401 VDI Combining Parameters Register 2 (IPUx\_VDI\_CMDP\_2)

The register holds combining parameters.

Address: Base address + 6\_8010h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

#### IPUx\_VDI\_CMDP\_2 field descriptions

Field	Description
31–24 Reserved	This read-only field is reserved and always has the value 0.
23–16 VDI_KEY_COLOR_R	Red component of background Color
15–8 VDI_KEY_COLOR_G	Green component of background Color
VDI_KEY_COLOR_B	Blue component of background Color

### 37.5.402 VDI Plane Size Register 1 (IPUx\_VDI\_PS\_1)

The register holds the plane size's parameters.

Address: Base address + 6\_8014h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																

Reset 0

#### IPUx\_VDI\_PS\_1 field descriptions

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 VDI_FHEIGHT1	Plane 1 height

Table continues on the next page...

**IPUx\_VDI\_PS\_1 field descriptions (continued)**

Field	Description
	The value to be written to this register is the plane's height minus 1. The Plane height should not be smaller than 16. The Plane height should not be greater than 1200. The Plane's height must be even
15–11 Reserved	This read-only field is reserved and always has the value 0.
VDI_FWIDTH1	Plane 1 width. The value to be written to this register is the plane's width minus 1. The Plane width should not be smaller than 16. The Plane width should not be greater than 1920. The width must be even.

**37.5.403 VDI Plane Size Register 2 (IPUx\_VDI\_PS\_2)**

The register holds the plane's offset parameters.

Address: Base address + 6\_8018h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R																																
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

**IPUx\_VDI\_PS\_2 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 VDI_OFFSET_ VER1	Vertical offset of plane 1
15–11 Reserved	This read-only field is reserved and always has the value 0.
VDI_OFFSET_ HOR1	Horizontal offset of plane 1

### 37.5.404 VDI Plane Size Register 3 (IPUx\_VDI\_PS\_3)

The register holds the plane size's parameters.

Address: Base address + 6\_801Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

#### IPUx\_VDI\_PS\_3 field descriptions

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 VDI_FHEIGHT3	Plane 3 height The value to be written to this register is the plane's height minus 1. The Plane height should not be smaller than 16. The Plane height should not be greater than 1200. The Plane's height must be even
15–11 Reserved	This read-only field is reserved and always has the value 0.
VDI_FWIDTH3	Plane 3 width. The value to be written to this register is the plane's width minus 1. The Plane width should not be smaller than 16. The Plane width should not be greater than 1920. The width must be even.

### 37.5.405 VDI Plane Size Register 4 (IPUx\_VDI\_PS\_4)

The register holds the plane's offset parameters.

Address: Base address + 6\_8020h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																0															
W																																

Reset 0

**IPUx\_VDI\_PS\_4 field descriptions**

Field	Description
31–27 Reserved	This read-only field is reserved and always has the value 0.
26–16 VDI_OFFSET_ VER3	Vertical offset of plane 3
15–11 Reserved	This read-only field is reserved and always has the value 0.
VDI_OFFSET_ HOR3	Horizontal offset of plane 3

