

36.4 IOMUXC Memory Map/Register Definition

The main groups of IOMUXC registers are:

The General Purpose Registers IOMUXC_GPR[13:0] are used to select operating modes for general features in the SoC, usually not related to the IOMUX itself.

The Software MUX Control Registers are used to configure the IOMUX muxing, and "connect" the pad to a given port in a module.

The PAD Settings Registers are used to control the pad settings configuration. For some pads (in order to save chip route) the pad settings are grouped in one register; changing the group register will affect the settings for all pads in the group.

The following table shows the IOMUXC register summary.

IOMUXC memory map

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|------------------------|--|-----------------|--------|-------------|------------------------------|
| 20E_0000 | GPR (IOMUXC_GPR0) | 32 | R/W | 0000_0000h | 36.4.1/1950 |
| 20E_0004 | GPR (IOMUXC_GPR1) | 32 | R/W | 4840_0005h | 36.4.2/1953 |
| 20E_0008 | GPR (IOMUXC_GPR2) | 32 | R/W | 0000_0000h | 36.4.3/1956 |
| 20E_000C | GPR (IOMUXC_GPR3) | 32 | R/W | 01E0_0000h | 36.4.4/1958 |
| 20E_0010 | GPR (IOMUXC_GPR4) | 32 | R/W | 0000_0000h | 36.4.5/1962 |
| 20E_0014 | GPR (IOMUXC_GPR5) | 32 | R/W | 0000_0000h | 36.4.6/1965 |
| 20E_0018 | GPR (IOMUXC_GPR6) | 32 | R/W | 2222_2222h | 36.4.7/1966 |
| 20E_001C | GPR (IOMUXC_GPR7) | 32 | R/W | 2222_2222h | 36.4.8/1967 |
| 20E_0020 | GPR (IOMUXC_GPR8) | 32 | R/W | 0000_0000h | 36.4.9/1968 |
| 20E_0024 | GPR (IOMUXC_GPR9) | 32 | R/W | 0000_0000h | 36.4.10/1969 |
| 20E_0028 | GPR (IOMUXC_GPR10) | 32 | R/W | 0000_3800h | 36.4.11/1970 |
| 20E_002C | GPR (IOMUXC_GPR11) | 32 | R/W | 0000_3800h | 36.4.12/1972 |
| 20E_0030 | GPR (IOMUXC_GPR12) | 32 | R/W | 0F00_0000h | 36.4.13/1972 |
| 20E_0034 | GPR (IOMUXC_GPR13) | 32 | R/W | 0591_24C4h | 36.4.14/1974 |
| 20E_004C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_DATA1) | 32 | R/W | 0000_0005h | 36.4.15/1977 |
| 20E_0050 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_DATA2) | 32 | R/W | 0000_0005h | 36.4.16/1978 |
| 20E_0054 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_DATA0) | 32 | R/W | 0000_0005h | 36.4.17/1979 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|------------------------------|
| 20E_0058 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TXC) | 32 | R/W | 0000_0005h | 36.4.18/1980 |
| 20E_005C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TDO) | 32 | R/W | 0000_0005h | 36.4.19/1981 |
| 20E_0060 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TD1) | 32 | R/W | 0000_0005h | 36.4.20/1982 |
| 20E_0064 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TD2) | 32 | R/W | 0000_0005h | 36.4.21/1983 |
| 20E_0068 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TD3) | 32 | R/W | 0000_0005h | 36.4.22/1984 |
| 20E_006C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RX_CTL) | 32 | R/W | 0000_0005h | 36.4.23/1985 |
| 20E_0070 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RD0) | 32 | R/W | 0000_0005h | 36.4.24/1986 |
| 20E_0074 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TX_CTL) | 32 | R/W | 0000_0005h | 36.4.25/1987 |
| 20E_0078 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RD1) | 32 | R/W | 0000_0005h | 36.4.26/1988 |
| 20E_007C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RD2) | 32 | R/W | 0000_0005h | 36.4.27/1989 |
| 20E_0080 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RD3) | 32 | R/W | 0000_0005h | 36.4.28/1990 |
| 20E_0084 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RXC) | 32 | R/W | 0000_0005h | 36.4.29/1991 |
| 20E_0088 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR25) | 32 | R/W | 0000_0000h | 36.4.30/1992 |
| 20E_008C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_EB2_B) | 32 | R/W | 0000_0005h | 36.4.31/1993 |
| 20E_0090 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA16) | 32 | R/W | 0000_0005h | 36.4.32/1994 |
| 20E_0094 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA17) | 32 | R/W | 0000_0005h | 36.4.33/1995 |
| 20E_0098 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA18) | 32 | R/W | 0000_0005h | 36.4.34/1996 |
| 20E_009C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA19) | 32 | R/W | 0000_0005h | 36.4.35/1997 |
| 20E_00A0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA20) | 32 | R/W | 0000_0005h | 36.4.36/1998 |
| 20E_00A4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA21) | 32 | R/W | 0000_0005h | 36.4.37/1999 |
| 20E_00A8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA22) | 32 | R/W | 0000_0005h | 36.4.38/2000 |
| 20E_00AC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA23) | 32 | R/W | 0000_0005h | 36.4.39/2001 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|------------------------------|
| 20E_00B0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_EB3_B) | 32 | R/W | 0000_0005h | 36.4.40/2002 |
| 20E_00B4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA24) | 32 | R/W | 0000_0005h | 36.4.41/2003 |
| 20E_00B8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA25) | 32 | R/W | 0000_0005h | 36.4.42/2004 |
| 20E_00BC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA26) | 32 | R/W | 0000_0005h | 36.4.43/2005 |
| 20E_00C0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA27) | 32 | R/W | 0000_0005h | 36.4.44/2006 |
| 20E_00C4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA28) | 32 | R/W | 0000_0005h | 36.4.45/2007 |
| 20E_00C8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA29) | 32 | R/W | 0000_0005h | 36.4.46/2008 |
| 20E_00CC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA30) | 32 | R/W | 0000_0005h | 36.4.47/2009 |
| 20E_00D0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA31) | 32 | R/W | 0000_0005h | 36.4.48/2010 |
| 20E_00D4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR24) | 32 | R/W | 0000_0000h | 36.4.49/2011 |
| 20E_00D8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR23) | 32 | R/W | 0000_0000h | 36.4.50/2012 |
| 20E_00DC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR22) | 32 | R/W | 0000_0000h | 36.4.51/2013 |
| 20E_00E0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR21) | 32 | R/W | 0000_0000h | 36.4.52/2014 |
| 20E_00E4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR20) | 32 | R/W | 0000_0000h | 36.4.53/2015 |
| 20E_00E8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR19) | 32 | R/W | 0000_0000h | 36.4.54/2016 |
| 20E_00EC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR18) | 32 | R/W | 0000_0000h | 36.4.55/2017 |
| 20E_00F0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR17) | 32 | R/W | 0000_0000h | 36.4.56/2018 |
| 20E_00F4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR16) | 32 | R/W | 0000_0000h | 36.4.57/2019 |
| 20E_00F8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_CS0_B) | 32 | R/W | 0000_0000h | 36.4.58/2020 |
| 20E_00FC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_CS1_B) | 32 | R/W | 0000_0000h | 36.4.59/2021 |
| 20E_0100 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_OE_B) | 32 | R/W | 0000_0000h | 36.4.60/2022 |
| 20E_0104 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_RW) | 32 | R/W | 0000_0000h | 36.4.61/2023 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|------------------------------|
| 20E_0108 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_LBA_B) | 32 | R/W | 0000_0000h | 36.4.62/2024 |
| 20E_010C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_EB0_B) | 32 | R/W | 0000_0000h | 36.4.63/2025 |
| 20E_0110 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_EB1_B) | 32 | R/W | 0000_0000h | 36.4.64/2026 |
| 20E_0114 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD00) | 32 | R/W | 0000_0000h | 36.4.65/2027 |
| 20E_0118 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD01) | 32 | R/W | 0000_0000h | 36.4.66/2028 |
| 20E_011C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD02) | 32 | R/W | 0000_0000h | 36.4.67/2029 |
| 20E_0120 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD03) | 32 | R/W | 0000_0000h | 36.4.68/2030 |
| 20E_0124 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD04) | 32 | R/W | 0000_0000h | 36.4.69/2031 |
| 20E_0128 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD05) | 32 | R/W | 0000_0000h | 36.4.70/2032 |
| 20E_012C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD06) | 32 | R/W | 0000_0000h | 36.4.71/2033 |
| 20E_0130 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD07) | 32 | R/W | 0000_0000h | 36.4.72/2034 |
| 20E_0134 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD08) | 32 | R/W | 0000_0000h | 36.4.73/2035 |
| 20E_0138 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD09) | 32 | R/W | 0000_0000h | 36.4.74/2036 |
| 20E_013C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD10) | 32 | R/W | 0000_0000h | 36.4.75/2037 |
| 20E_0140 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD11) | 32 | R/W | 0000_0000h | 36.4.76/2038 |
| 20E_0144 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD12) | 32 | R/W | 0000_0000h | 36.4.77/2039 |
| 20E_0148 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD13) | 32 | R/W | 0000_0000h | 36.4.78/2040 |
| 20E_014C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD14) | 32 | R/W | 0000_0000h | 36.4.79/2041 |
| 20E_0150 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD15) | 32 | R/W | 0000_0000h | 36.4.80/2042 |
| 20E_0154 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_WAIT_B) | 32 | R/W | 0000_0000h | 36.4.81/2043 |
| 20E_0158 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_BCLK) | 32 | R/W | 0000_0000h | 36.4.82/2044 |
| 20E_015C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DIO_DISP_CLK) | 32 | R/W | 0000_0005h | 36.4.83/2045 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_0160 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DIO_PIN15) | 32 | R/W | 0000_0005h | 36.4.84/2046 |
| 20E_0164 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DIO_PIN02) | 32 | R/W | 0000_0005h | 36.4.85/2047 |
| 20E_0168 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DIO_PIN03) | 32 | R/W | 0000_0005h | 36.4.86/2048 |
| 20E_016C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DIO_PIN04) | 32 | R/W | 0000_0005h | 36.4.87/2049 |
| 20E_0170 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA00) | 32 | R/W | 0000_0005h | 36.4.88/2050 |
| 20E_0174 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA01) | 32 | R/W | 0000_0005h | 36.4.89/2051 |
| 20E_0178 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA02) | 32 | R/W | 0000_0005h | 36.4.90/2052 |
| 20E_017C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA03) | 32 | R/W | 0000_0005h | 36.4.91/2053 |
| 20E_0180 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA04) | 32 | R/W | 0000_0005h | 36.4.92/2054 |
| 20E_0184 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA05) | 32 | R/W | 0000_0005h | 36.4.93/2055 |
| 20E_0188 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA06) | 32 | R/W | 0000_0005h | 36.4.94/2056 |
| 20E_018C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA07) | 32 | R/W | 0000_0005h | 36.4.95/2057 |
| 20E_0190 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA08) | 32 | R/W | 0000_0005h | 36.4.96/2058 |
| 20E_0194 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA09) | 32 | R/W | 0000_0005h | 36.4.97/2059 |
| 20E_0198 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA10) | 32 | R/W | 0000_0005h | 36.4.98/2060 |
| 20E_019C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA11) | 32 | R/W | 0000_0005h | 36.4.99/2061 |
| 20E_01A0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA12) | 32 | R/W | 0000_0005h | 36.4.100/2062 |
| 20E_01A4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA13) | 32 | R/W | 0000_0005h | 36.4.101/2063 |
| 20E_01A8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA14) | 32 | R/W | 0000_0005h | 36.4.102/2064 |
| 20E_01AC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA15) | 32 | R/W | 0000_0005h | 36.4.103/2065 |
| 20E_01B0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA16) | 32 | R/W | 0000_0005h | 36.4.104/2066 |
| 20E_01B4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA17) | 32 | R/W | 0000_0005h | 36.4.105/2067 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_01B8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA18) | 32 | R/W | 0000_0005h | 36.4.106/2068 |
| 20E_01BC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA19) | 32 | R/W | 0000_0005h | 36.4.107/2069 |
| 20E_01C0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA20) | 32 | R/W | 0000_0005h | 36.4.108/2070 |
| 20E_01C4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA21) | 32 | R/W | 0000_0005h | 36.4.109/2071 |
| 20E_01C8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA22) | 32 | R/W | 0000_0005h | 36.4.110/2072 |
| 20E_01CC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA23) | 32 | R/W | 0000_0005h | 36.4.111/2073 |
| 20E_01D0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_MDIO) | 32 | R/W | 0000_0005h | 36.4.112/2074 |
| 20E_01D4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_REF_CLK) | 32 | R/W | 0000_0005h | 36.4.113/2075 |
| 20E_01D8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_RX_ER) | 32 | R/W | 0000_0005h | 36.4.114/2076 |
| 20E_01DC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_CRS_DV) | 32 | R/W | 0000_0005h | 36.4.115/2077 |
| 20E_01E0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_RX_DATA1) | 32 | R/W | 0000_0005h | 36.4.116/2078 |
| 20E_01E4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_RX_DATA0) | 32 | R/W | 0000_0005h | 36.4.117/2079 |
| 20E_01E8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_TX_EN) | 32 | R/W | 0000_0005h | 36.4.118/2080 |
| 20E_01EC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_TX_DATA1) | 32 | R/W | 0000_0005h | 36.4.119/2081 |
| 20E_01F0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_TX_DATA0) | 32 | R/W | 0000_0005h | 36.4.120/2082 |
| 20E_01F4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_MDC) | 32 | R/W | 0000_0005h | 36.4.121/2083 |
| 20E_01F8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL0) | 32 | R/W | 0000_0005h | 36.4.122/2084 |
| 20E_01FC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW0) | 32 | R/W | 0000_0005h | 36.4.123/2085 |
| 20E_0200 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL1) | 32 | R/W | 0000_0005h | 36.4.124/2086 |
| 20E_0204 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW1) | 32 | R/W | 0000_0005h | 36.4.125/2087 |
| 20E_0208 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL2) | 32 | R/W | 0000_0005h | 36.4.126/2088 |
| 20E_020C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW2) | 32 | R/W | 0000_0005h | 36.4.127/2089 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_0210 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL3) | 32 | R/W | 0000_0005h | 36.4.128/2090 |
| 20E_0214 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW3) | 32 | R/W | 0000_0005h | 36.4.129/2091 |
| 20E_0218 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL4) | 32 | R/W | 0000_0005h | 36.4.130/2092 |
| 20E_021C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW4) | 32 | R/W | 0000_0005h | 36.4.131/2093 |
| 20E_0220 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO00) | 32 | R/W | 0000_0005h | 36.4.132/2094 |
| 20E_0224 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO01) | 32 | R/W | 0000_0005h | 36.4.133/2095 |
| 20E_0228 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO09) | 32 | R/W | 0000_0005h | 36.4.134/2096 |
| 20E_022C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO03) | 32 | R/W | 0000_0005h | 36.4.135/2097 |
| 20E_0230 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO06) | 32 | R/W | 0000_0005h | 36.4.136/2098 |
| 20E_0234 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO02) | 32 | R/W | 0000_0005h | 36.4.137/2099 |
| 20E_0238 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO04) | 32 | R/W | 0000_0005h | 36.4.138/2100 |
| 20E_023C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO05) | 32 | R/W | 0000_0005h | 36.4.139/2101 |
| 20E_0240 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO07) | 32 | R/W | 0000_0005h | 36.4.140/2102 |
| 20E_0244 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO08) | 32 | R/W | 0000_0005h | 36.4.141/2103 |
| 20E_0248 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO16) | 32 | R/W | 0000_0005h | 36.4.142/2104 |
| 20E_024C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO17) | 32 | R/W | 0000_0005h | 36.4.143/2105 |
| 20E_0250 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO18) | 32 | R/W | 0000_0005h | 36.4.144/2106 |
| 20E_0254 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO19) | 32 | R/W | 0000_0005h | 36.4.145/2107 |
| 20E_0258 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_PIXCLK) | 32 | R/W | 0000_0005h | 36.4.146/2108 |
| 20E_025C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_HSYNC) | 32 | R/W | 0000_0005h | 36.4.147/2109 |
| 20E_0260 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA_EN) | 32 | R/W | 0000_0005h | 36.4.148/2110 |
| 20E_0264 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_VSYNC) | 32 | R/W | 0000_0005h | 36.4.149/2111 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_0268 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA04) | 32 | R/W | 0000_0005h | 36.4.150/2112 |
| 20E_026C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA05) | 32 | R/W | 0000_0005h | 36.4.151/2113 |
| 20E_0270 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA06) | 32 | R/W | 0000_0005h | 36.4.152/2114 |
| 20E_0274 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA07) | 32 | R/W | 0000_0005h | 36.4.153/2115 |
| 20E_0278 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA08) | 32 | R/W | 0000_0005h | 36.4.154/2116 |
| 20E_027C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA09) | 32 | R/W | 0000_0005h | 36.4.155/2117 |
| 20E_0280 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA10) | 32 | R/W | 0000_0005h | 36.4.156/2118 |
| 20E_0284 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA11) | 32 | R/W | 0000_0005h | 36.4.157/2119 |
| 20E_0288 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA12) | 32 | R/W | 0000_0005h | 36.4.158/2120 |
| 20E_028C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA13) | 32 | R/W | 0000_0005h | 36.4.159/2121 |
| 20E_0290 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA14) | 32 | R/W | 0000_0005h | 36.4.160/2122 |
| 20E_0294 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA15) | 32 | R/W | 0000_0005h | 36.4.161/2123 |
| 20E_0298 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA16) | 32 | R/W | 0000_0005h | 36.4.162/2124 |
| 20E_029C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA17) | 32 | R/W | 0000_0005h | 36.4.163/2125 |
| 20E_02A0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA18) | 32 | R/W | 0000_0005h | 36.4.164/2126 |
| 20E_02A4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA19) | 32 | R/W | 0000_0005h | 36.4.165/2127 |
| 20E_02A8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA7) | 32 | R/W | 0000_0005h | 36.4.166/2128 |
| 20E_02AC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA6) | 32 | R/W | 0000_0005h | 36.4.167/2129 |
| 20E_02B0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA5) | 32 | R/W | 0000_0005h | 36.4.168/2130 |
| 20E_02B4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA4) | 32 | R/W | 0000_0005h | 36.4.169/2131 |
| 20E_02B8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_CMD) | 32 | R/W | 0000_0005h | 36.4.170/2132 |
| 20E_02BC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_CLK) | 32 | R/W | 0000_0005h | 36.4.171/2133 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_02C0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA0) | 32 | R/W | 0000_0005h | 36.4.172/2134 |
| 20E_02C4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA1) | 32 | R/W | 0000_0005h | 36.4.173/2135 |
| 20E_02C8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA2) | 32 | R/W | 0000_0005h | 36.4.174/2136 |
| 20E_02CC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA3) | 32 | R/W | 0000_0005h | 36.4.175/2136 |
| 20E_02D0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_RESET) | 32 | R/W | 0000_0005h | 36.4.176/2137 |
| 20E_02D4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CLE) | 32 | R/W | 0000_0005h | 36.4.177/2138 |
| 20E_02D8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_ALE) | 32 | R/W | 0000_0005h | 36.4.178/2139 |
| 20E_02DC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_WP_B) | 32 | R/W | 0000_0005h | 36.4.179/2140 |
| 20E_02E0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_READY_B) | 32 | R/W | 0000_0005h | 36.4.180/2141 |
| 20E_02E4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CS0_B) | 32 | R/W | 0000_0005h | 36.4.181/2142 |
| 20E_02E8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CS1_B) | 32 | R/W | 0000_0005h | 36.4.182/2142 |
| 20E_02EC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CS2_B) | 32 | R/W | 0000_0005h | 36.4.183/2143 |
| 20E_02F0 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CS3_B) | 32 | R/W | 0000_0005h | 36.4.184/2144 |
| 20E_02F4 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_CMD) | 32 | R/W | 0000_0005h | 36.4.185/2145 |
| 20E_02F8 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_CLK) | 32 | R/W | 0000_0005h | 36.4.186/2146 |
| 20E_02FC | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA00) | 32 | R/W | 0000_0005h | 36.4.187/2147 |
| 20E_0300 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA01) | 32 | R/W | 0000_0005h | 36.4.188/2148 |
| 20E_0304 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA02) | 32 | R/W | 0000_0005h | 36.4.189/2149 |
| 20E_0308 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA03) | 32 | R/W | 0000_0005h | 36.4.190/2150 |
| 20E_030C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA04) | 32 | R/W | 0000_0005h | 36.4.191/2151 |
| 20E_0310 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA05) | 32 | R/W | 0000_0005h | 36.4.192/2152 |
| 20E_0314 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA06) | 32 | R/W | 0000_0005h | 36.4.193/2153 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 20E_0318 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA07) | 32 | R/W | 0000_0005h | 36.4.194/2154 |
| 20E_031C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA0) | 32 | R/W | 0000_0005h | 36.4.195/2155 |
| 20E_0320 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA1) | 32 | R/W | 0000_0005h | 36.4.196/2156 |
| 20E_0324 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA2) | 32 | R/W | 0000_0005h | 36.4.197/2157 |
| 20E_0328 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA3) | 32 | R/W | 0000_0005h | 36.4.198/2158 |
| 20E_032C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA4) | 32 | R/W | 0000_0005h | 36.4.199/2158 |
| 20E_0330 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA5) | 32 | R/W | 0000_0005h | 36.4.200/2159 |
| 20E_0334 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA6) | 32 | R/W | 0000_0005h | 36.4.201/2160 |
| 20E_0338 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA7) | 32 | R/W | 0000_0005h | 36.4.202/2161 |
| 20E_033C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_DATA1) | 32 | R/W | 0000_0005h | 36.4.203/2162 |
| 20E_0340 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_DATA0) | 32 | R/W | 0000_0005h | 36.4.204/2163 |
| 20E_0344 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_DATA3) | 32 | R/W | 0000_0005h | 36.4.205/2164 |
| 20E_0348 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_CMD) | 32 | R/W | 0000_0005h | 36.4.206/2165 |
| 20E_034C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_DATA2) | 32 | R/W | 0000_0005h | 36.4.207/2166 |
| 20E_0350 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_CLK) | 32 | R/W | 0000_0005h | 36.4.208/2167 |
| 20E_0354 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_CLK) | 32 | R/W | 0000_0005h | 36.4.209/2168 |
| 20E_0358 | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_CMD) | 32 | R/W | 0000_0005h | 36.4.210/2169 |
| 20E_035C | Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_DATA3) | 32 | R/W | 0000_0005h | 36.4.211/2170 |
| 20E_0360 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_DATA1) | 32 | R/W | 0001_B0B0h | 36.4.212/2171 |
| 20E_0364 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_DATA2) | 32 | R/W | 0001_B0B0h | 36.4.213/2172 |
| 20E_0368 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_DATA0) | 32 | R/W | 0001_B0B0h | 36.4.214/2174 |
| 20E_036C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TXC) | 32 | R/W | 0001_3030h | 36.4.215/2176 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_0370 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TD0) | 32 | R/W | 0001_B030h | 36.4.216/2178 |
| 20E_0374 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TD1) | 32 | R/W | 0001_B030h | 36.4.217/2179 |
| 20E_0378 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TD2) | 32 | R/W | 0001_B030h | 36.4.218/2181 |
| 20E_037C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TD3) | 32 | R/W | 0001_B030h | 36.4.219/2183 |
| 20E_0380 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RX_CTL) | 32 | R/W | 0001_3030h | 36.4.220/2184 |
| 20E_0384 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RD0) | 32 | R/W | 0001_B030h | 36.4.221/2186 |
| 20E_0388 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TX_CTL) | 32 | R/W | 0001_3030h | 36.4.222/2188 |
| 20E_038C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RD1) | 32 | R/W | 0001_B030h | 36.4.223/2189 |
| 20E_0390 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RD2) | 32 | R/W | 0001_B030h | 36.4.224/2191 |
| 20E_0394 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RD3) | 32 | R/W | 0001_B030h | 36.4.225/2193 |
| 20E_0398 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RXC) | 32 | R/W | 0001_3030h | 36.4.226/2194 |
| 20E_039C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR25) | 32 | R/W | 0000_B0B1h | 36.4.227/2196 |
| 20E_03A0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_EB2_B) | 32 | R/W | 0001_B0B0h | 36.4.228/2198 |
| 20E_03A4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA16) | 32 | R/W | 0001_B0B0h | 36.4.229/2199 |
| 20E_03A8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA17) | 32 | R/W | 0001_B0B0h | 36.4.230/2201 |
| 20E_03AC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA18) | 32 | R/W | 0001_B0B0h | 36.4.231/2203 |
| 20E_03B0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA19) | 32 | R/W | 0001_B0B0h | 36.4.232/2205 |
| 20E_03B4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA20) | 32 | R/W | 0001_B0B0h | 36.4.233/2206 |
| 20E_03B8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA21) | 32 | R/W | 0001_B0B0h | 36.4.234/2208 |
| 20E_03BC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA22) | 32 | R/W | 0001_B0B0h | 36.4.235/2210 |
| 20E_03C0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA23) | 32 | R/W | 0001_B0B0h | 36.4.236/2212 |
| 20E_03C4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_EB3_B) | 32 | R/W | 0001_B0B0h | 36.4.237/2213 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_03C8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA24) | 32 | R/W | 0001_B0B0h | 36.4.238/2215 |
| 20E_03CC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA25) | 32 | R/W | 0001_B0B0h | 36.4.239/2217 |
| 20E_03D0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA26) | 32 | R/W | 0001_B0B0h | 36.4.240/2219 |
| 20E_03D4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA27) | 32 | R/W | 0001_B0B0h | 36.4.241/2220 |
| 20E_03D8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA28) | 32 | R/W | 0001_B0B0h | 36.4.242/2222 |
| 20E_03DC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA29) | 32 | R/W | 0001_B0B0h | 36.4.243/2224 |
| 20E_03E0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA30) | 32 | R/W | 0001_B0B0h | 36.4.244/2226 |
| 20E_03E4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA31) | 32 | R/W | 0001_B0B0h | 36.4.245/2227 |
| 20E_03E8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR24) | 32 | R/W | 0000_B0B1h | 36.4.246/2229 |
| 20E_03EC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR23) | 32 | R/W | 0000_B0B1h | 36.4.247/2231 |
| 20E_03F0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR22) | 32 | R/W | 0000_B0B1h | 36.4.248/2233 |
| 20E_03F4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR21) | 32 | R/W | 0000_B0B1h | 36.4.249/2234 |
| 20E_03F8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR20) | 32 | R/W | 0000_B0B1h | 36.4.250/2236 |
| 20E_03FC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR19) | 32 | R/W | 0000_B0B1h | 36.4.251/2238 |
| 20E_0400 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR18) | 32 | R/W | 0000_B0B1h | 36.4.252/2240 |
| 20E_0404 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR17) | 32 | R/W | 0000_B0B1h | 36.4.253/2241 |
| 20E_0408 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR16) | 32 | R/W | 0000_B0B1h | 36.4.254/2243 |
| 20E_040C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_CS0_B) | 32 | R/W | 0000_B0B1h | 36.4.255/2245 |
| 20E_0410 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_CS1_B) | 32 | R/W | 0000_B0B1h | 36.4.256/2247 |
| 20E_0414 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_OE_B) | 32 | R/W | 0000_B0B1h | 36.4.257/2248 |
| 20E_0418 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_RW) | 32 | R/W | 0000_B0B1h | 36.4.258/2250 |
| 20E_041C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_LBA_B) | 32 | R/W | 0000_B0B1h | 36.4.259/2252 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_0420 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_EB0_B) | 32 | R/W | 0000_B0B1h | 36.4.260/2254 |
| 20E_0424 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_EB1_B) | 32 | R/W | 0000_B0B1h | 36.4.261/2255 |
| 20E_0428 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD00) | 32 | R/W | 0000_B0B1h | 36.4.262/2257 |
| 20E_042C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD01) | 32 | R/W | 0000_B0B1h | 36.4.263/2259 |
| 20E_0430 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD02) | 32 | R/W | 0000_B0B1h | 36.4.264/2261 |
| 20E_0434 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD03) | 32 | R/W | 0000_B0B1h | 36.4.265/2262 |
| 20E_0438 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD04) | 32 | R/W | 0000_B0B1h | 36.4.266/2264 |
| 20E_043C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD05) | 32 | R/W | 0000_B0B1h | 36.4.267/2266 |
| 20E_0440 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD06) | 32 | R/W | 0000_B0B1h | 36.4.268/2268 |
| 20E_0444 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD07) | 32 | R/W | 0000_B0B1h | 36.4.269/2269 |
| 20E_0448 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD08) | 32 | R/W | 0000_B0B1h | 36.4.270/2271 |
| 20E_044C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD09) | 32 | R/W | 0000_B0B1h | 36.4.271/2273 |
| 20E_0450 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD10) | 32 | R/W | 0000_B0B1h | 36.4.272/2275 |
| 20E_0454 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD11) | 32 | R/W | 0000_B0B1h | 36.4.273/2276 |
| 20E_0458 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD12) | 32 | R/W | 0000_B0B1h | 36.4.274/2278 |
| 20E_045C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD13) | 32 | R/W | 0000_B0B1h | 36.4.275/2280 |
| 20E_0460 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD14) | 32 | R/W | 0000_B0B1h | 36.4.276/2282 |
| 20E_0464 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD15) | 32 | R/W | 0000_B0B1h | 36.4.277/2283 |
| 20E_0468 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_WAIT_B) | 32 | R/W | 0000_B060h | 36.4.278/2285 |
| 20E_046C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_BCLK) | 32 | R/W | 0000_B0B1h | 36.4.279/2287 |
| 20E_0470 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DI0_DISP_CLK) | 32 | R/W | 0001_B0B0h | 36.4.280/2289 |
| 20E_0474 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DI0_PIN15) | 32 | R/W | 0001_B0B0h | 36.4.281/2290 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_0478 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DIO_PIN02) | 32 | R/W | 0001_B0B0h | 36.4.282/2292 |
| 20E_047C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DIO_PIN03) | 32 | R/W | 0001_B0B0h | 36.4.283/2294 |
| 20E_0480 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DIO_PIN04) | 32 | R/W | 0001_B0B0h | 36.4.284/2296 |
| 20E_0484 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA00) | 32 | R/W | 0001_B0B0h | 36.4.285/2297 |
| 20E_0488 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA01) | 32 | R/W | 0001_B0B0h | 36.4.286/2299 |
| 20E_048C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA02) | 32 | R/W | 0001_B0B0h | 36.4.287/2301 |
| 20E_0490 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA03) | 32 | R/W | 0001_B0B0h | 36.4.288/2303 |
| 20E_0494 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA04) | 32 | R/W | 0001_B0B0h | 36.4.289/2304 |
| 20E_0498 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA05) | 32 | R/W | 0001_B0B0h | 36.4.290/2306 |
| 20E_049C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA06) | 32 | R/W | 0001_B0B0h | 36.4.291/2308 |
| 20E_04A0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA07) | 32 | R/W | 0001_B0B0h | 36.4.292/2310 |
| 20E_04A4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA08) | 32 | R/W | 0001_B0B0h | 36.4.293/2311 |
| 20E_04A8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA09) | 32 | R/W | 0001_B0B0h | 36.4.294/2313 |
| 20E_04AC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA10) | 32 | R/W | 0001_B0B0h | 36.4.295/2315 |
| 20E_04B0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA11) | 32 | R/W | 0001_B0B0h | 36.4.296/2317 |
| 20E_04B4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA12) | 32 | R/W | 0001_B0B0h | 36.4.297/2318 |
| 20E_04B8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA13) | 32 | R/W | 0001_B0B0h | 36.4.298/2320 |
| 20E_04BC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA14) | 32 | R/W | 0001_B0B0h | 36.4.299/2322 |
| 20E_04C0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA15) | 32 | R/W | 0001_B0B0h | 36.4.300/2324 |
| 20E_04C4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA16) | 32 | R/W | 0001_B0B0h | 36.4.301/2325 |
| 20E_04C8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA17) | 32 | R/W | 0001_B0B0h | 36.4.302/2327 |
| 20E_04CC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA18) | 32 | R/W | 0001_B0B0h | 36.4.303/2329 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 20E_04D0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA19) | 32 | R/W | 0001_B0B0h | 36.4.304/2331 |
| 20E_04D4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA20) | 32 | R/W | 0001_B0B0h | 36.4.305/2332 |
| 20E_04D8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA21) | 32 | R/W | 0001_B0B0h | 36.4.306/2334 |
| 20E_04DC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA22) | 32 | R/W | 0001_B0B0h | 36.4.307/2336 |
| 20E_04E0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA23) | 32 | R/W | 0001_B0B0h | 36.4.308/2338 |
| 20E_04E4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_MDIO) | 32 | R/W | 0001_B0B0h | 36.4.309/2339 |
| 20E_04E8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_REF_CLK) | 32 | R/W | 0001_B0B0h | 36.4.310/2341 |
| 20E_04EC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_RX_ER) | 32 | R/W | 0001_B0B0h | 36.4.311/2343 |
| 20E_04F0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_CRS_DV) | 32 | R/W | 0001_B0B0h | 36.4.312/2345 |
| 20E_04F4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_RX_DATA1) | 32 | R/W | 0001_B0B0h | 36.4.313/2346 |
| 20E_04F8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_RX_DATA0) | 32 | R/W | 0001_B0B0h | 36.4.314/2348 |
| 20E_04FC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_TX_EN) | 32 | R/W | 0001_B0B0h | 36.4.315/2350 |
| 20E_0500 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_TX_DATA1) | 32 | R/W | 0001_B0B0h | 36.4.316/2352 |
| 20E_0504 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_TX_DATA0) | 32 | R/W | 0001_B0B0h | 36.4.317/2353 |
| 20E_0508 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_MDC) | 32 | R/W | 0001_B0B0h | 36.4.318/2355 |
| 20E_050C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS5_P) | 32 | R/W | 0000_2030h | 36.4.319/2357 |
| 20E_0510 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM5) | 32 | R/W | 0000_8030h | 36.4.320/2359 |
| 20E_0514 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM4) | 32 | R/W | 0000_8030h | 36.4.321/2361 |
| 20E_0518 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS4_P) | 32 | R/W | 0000_2030h | 36.4.322/2363 |
| 20E_051C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS3_P) | 32 | R/W | 0000_2030h | 36.4.323/2365 |
| 20E_0520 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM3) | 32 | R/W | 0000_8030h | 36.4.324/2367 |
| 20E_0524 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS2_P) | 32 | R/W | 0000_2030h | 36.4.325/2369 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 20E_0528 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM2) | 32 | R/W | 0000_8030h | 36.4.326/2371 |
| 20E_052C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR00) | 32 | R/W | 0000_8000h | 36.4.327/2373 |
| 20E_0530 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR01) | 32 | R/W | 0000_8000h | 36.4.328/2375 |
| 20E_0534 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR02) | 32 | R/W | 0000_8000h | 36.4.329/2377 |
| 20E_0538 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR03) | 32 | R/W | 0000_8000h | 36.4.330/2379 |
| 20E_053C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR04) | 32 | R/W | 0000_8000h | 36.4.331/2381 |
| 20E_0540 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR05) | 32 | R/W | 0000_8000h | 36.4.332/2383 |
| 20E_0544 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR06) | 32 | R/W | 0000_8000h | 36.4.333/2385 |
| 20E_0548 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR07) | 32 | R/W | 0000_8000h | 36.4.334/2387 |
| 20E_054C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR08) | 32 | R/W | 0000_8000h | 36.4.335/2389 |
| 20E_0550 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR09) | 32 | R/W | 0000_8000h | 36.4.336/2391 |
| 20E_0554 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR10) | 32 | R/W | 0000_8000h | 36.4.337/2393 |
| 20E_0558 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR11) | 32 | R/W | 0000_8000h | 36.4.338/2395 |
| 20E_055C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR12) | 32 | R/W | 0000_8000h | 36.4.339/2397 |
| 20E_0560 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR13) | 32 | R/W | 0000_8000h | 36.4.340/2399 |
| 20E_0564 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR14) | 32 | R/W | 0000_8000h | 36.4.341/2401 |
| 20E_0568 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR15) | 32 | R/W | 0000_8000h | 36.4.342/2403 |
| 20E_056C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_CAS_B) | 32 | R/W | 0000_8030h | 36.4.343/2405 |
| 20E_0570 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_CS0_B) | 32 | R/W | 0000_8000h | 36.4.344/2407 |
| 20E_0574 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_CS1_B) | 32 | R/W | 0000_8000h | 36.4.345/2409 |
| 20E_0578 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_RAS_B) | 32 | R/W | 0000_8030h | 36.4.346/2411 |
| 20E_057C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_RESET) | 32 | R/W | 0008_3030h | 36.4.347/2413 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 20E_0580 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA0) | 32 | R/W | 0000_8000h | 36.4.348/2415 |
| 20E_0584 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA1) | 32 | R/W | 0000_8000h | 36.4.349/2417 |
| 20E_0588 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK0_P) | 32 | R/W | 0000_8030h | 36.4.350/2419 |
| 20E_058C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA2) | 32 | R/W | 0000_B000h | 36.4.351/2421 |
| 20E_0590 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE0) | 32 | R/W | 0000_3000h | 36.4.352/2423 |
| 20E_0594 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK1_P) | 32 | R/W | 0000_8030h | 36.4.353/2425 |
| 20E_0598 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE1) | 32 | R/W | 0000_3000h | 36.4.354/2427 |
| 20E_059C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ODT0) | 32 | R/W | 0000_3030h | 36.4.355/2429 |
| 20E_05A0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ODT1) | 32 | R/W | 0000_3030h | 36.4.356/2431 |
| 20E_05A4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDWE_B) | 32 | R/W | 0000_8000h | 36.4.357/2433 |
| 20E_05A8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS0_P) | 32 | R/W | 0000_2030h | 36.4.358/2435 |
| 20E_05AC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM0) | 32 | R/W | 0000_8030h | 36.4.359/2437 |
| 20E_05B0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS1_P) | 32 | R/W | 0000_2030h | 36.4.360/2439 |
| 20E_05B4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM1) | 32 | R/W | 0000_8030h | 36.4.361/2441 |
| 20E_05B8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS6_P) | 32 | R/W | 0000_2030h | 36.4.362/2443 |
| 20E_05BC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM6) | 32 | R/W | 0000_8030h | 36.4.363/2445 |
| 20E_05C0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS7_P) | 32 | R/W | 0000_2030h | 36.4.364/2447 |
| 20E_05C4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM7) | 32 | R/W | 0000_8030h | 36.4.365/2449 |
| 20E_05C8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_COL0) | 32 | R/W | 0001_B0B0h | 36.4.366/2451 |
| 20E_05CC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW0) | 32 | R/W | 0001_B0B0h | 36.4.367/2452 |
| 20E_05D0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_COL1) | 32 | R/W | 0001_B0B0h | 36.4.368/2454 |
| 20E_05D4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW1) | 32 | R/W | 0001_B0B0h | 36.4.369/2456 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 20E_05D8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_COL2) | 32 | R/W | 0001_B0B0h | 36.4.370/2458 |
| 20E_05DC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW2) | 32 | R/W | 0001_B0B0h | 36.4.371/2459 |
| 20E_05E0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_COL3) | 32 | R/W | 0001_B0B0h | 36.4.372/2461 |
| 20E_05E4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW3) | 32 | R/W | 0001_B0B0h | 36.4.373/2463 |
| 20E_05E8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_COL4) | 32 | R/W | 0001_B0B0h | 36.4.374/2465 |
| 20E_05EC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW4) | 32 | R/W | 0001_B0B0h | 36.4.375/2466 |
| 20E_05F0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO00) | 32 | R/W | 0001_B0B0h | 36.4.376/2468 |
| 20E_05F4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO01) | 32 | R/W | 0001_B0B0h | 36.4.377/2470 |
| 20E_05F8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO09) | 32 | R/W | 0001_B0B0h | 36.4.378/2472 |
| 20E_05FC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO03) | 32 | R/W | 0001_B0B0h | 36.4.379/2473 |
| 20E_0600 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO06) | 32 | R/W | 0001_B0B0h | 36.4.380/2475 |
| 20E_0604 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO02) | 32 | R/W | 0001_B0B0h | 36.4.381/2477 |
| 20E_0608 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO04) | 32 | R/W | 0001_B0B0h | 36.4.382/2479 |
| 20E_060C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO05) | 32 | R/W | 0001_B0B0h | 36.4.383/2480 |
| 20E_0610 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO07) | 32 | R/W | 0001_B0B0h | 36.4.384/2482 |
| 20E_0614 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO08) | 32 | R/W | 0001_B0B0h | 36.4.385/2484 |
| 20E_0618 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO16) | 32 | R/W | 0001_B0B0h | 36.4.386/2486 |
| 20E_061C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO17) | 32 | R/W | 0001_B0B0h | 36.4.387/2487 |
| 20E_0620 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO18) | 32 | R/W | 0001_B0B0h | 36.4.388/2489 |
| 20E_0624 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO19) | 32 | R/W | 0001_B0B0h | 36.4.389/2491 |
| 20E_0628 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_PIXCLK) | 32 | R/W | 0001_B0B0h | 36.4.390/2492 |
| 20E_062C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_HSYNC) | 32 | R/W | 0001_B0B0h | 36.4.391/2494 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_0630 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA_EN) | 32 | R/W | 0001_B0B0h | 36.4.392/2496 |
| 20E_0634 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_VSYNC) | 32 | R/W | 0001_B0B0h | 36.4.393/2498 |
| 20E_0638 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA04) | 32 | R/W | 0001_B0B0h | 36.4.394/2499 |
| 20E_063C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA05) | 32 | R/W | 0001_B0B0h | 36.4.395/2501 |
| 20E_0640 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA06) | 32 | R/W | 0001_B0B0h | 36.4.396/2503 |
| 20E_0644 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA07) | 32 | R/W | 0001_B0B0h | 36.4.397/2505 |
| 20E_0648 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA08) | 32 | R/W | 0001_B0B0h | 36.4.398/2506 |
| 20E_064C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA09) | 32 | R/W | 0001_B0B0h | 36.4.399/2508 |
| 20E_0650 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA10) | 32 | R/W | 0001_B0B0h | 36.4.400/2510 |
| 20E_0654 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA11) | 32 | R/W | 0001_B0B0h | 36.4.401/2512 |
| 20E_0658 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA12) | 32 | R/W | 0001_B0B0h | 36.4.402/2513 |
| 20E_065C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA13) | 32 | R/W | 0001_B0B0h | 36.4.403/2515 |
| 20E_0660 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA14) | 32 | R/W | 0001_B0B0h | 36.4.404/2517 |
| 20E_0664 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA15) | 32 | R/W | 0001_B0B0h | 36.4.405/2519 |
| 20E_0668 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA16) | 32 | R/W | 0001_B0B0h | 36.4.406/2520 |
| 20E_066C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA17) | 32 | R/W | 0001_B0B0h | 36.4.407/2522 |
| 20E_0670 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA18) | 32 | R/W | 0001_B0B0h | 36.4.408/2524 |
| 20E_0674 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA19) | 32 | R/W | 0001_B0B0h | 36.4.409/2526 |
| 20E_0678 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TMS) | 32 | R/W | 0000_7060h | 36.4.410/2527 |
| 20E_067C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_MOD) | 32 | R/W | 0000_B060h | 36.4.411/2529 |
| 20E_0680 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TRSTB) | 32 | R/W | 0000_7060h | 36.4.412/2531 |
| 20E_0684 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TDI) | 32 | R/W | 0000_7060h | 36.4.413/2532 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|------------------------|---|-----------------|--------|-------------|--------------------------------|
| 20E_0688 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TCK) | 32 | R/W | 0000_7060h | 36.4.414/ 2534 |
| 20E_068C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TDO) | 32 | R/W | 0000_90B1h | 36.4.415/ 2536 |
| 20E_0690 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA7) | 32 | R/W | 0001_B0B0h | 36.4.416/ 2537 |
| 20E_0694 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA6) | 32 | R/W | 0001_B0B0h | 36.4.417/ 2539 |
| 20E_0698 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA5) | 32 | R/W | 0001_B0B0h | 36.4.418/ 2541 |
| 20E_069C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA4) | 32 | R/W | 0001_B0B0h | 36.4.419/ 2542 |
| 20E_06A0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_CMD) | 32 | R/W | 0001_B0B0h | 36.4.420/ 2544 |
| 20E_06A4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_CLK) | 32 | R/W | 0001_B0B0h | 36.4.421/ 2546 |
| 20E_06A8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA0) | 32 | R/W | 0001_B0B0h | 36.4.422/ 2548 |
| 20E_06AC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA1) | 32 | R/W | 0001_B0B0h | 36.4.423/ 2549 |
| 20E_06B0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA2) | 32 | R/W | 0001_B0B0h | 36.4.424/ 2551 |
| 20E_06B4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA3) | 32 | R/W | 0001_B0B0h | 36.4.425/ 2553 |
| 20E_06B8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_RESET) | 32 | R/W | 0001_B0B0h | 36.4.426/ 2555 |
| 20E_06BC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CLE) | 32 | R/W | 0001_B0B0h | 36.4.427/ 2556 |
| 20E_06C0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_ALE) | 32 | R/W | 0001_B0B0h | 36.4.428/ 2558 |
| 20E_06C4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_WP_B) | 32 | R/W | 0001_B0B0h | 36.4.429/ 2560 |
| 20E_06C8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_READY_B) | 32 | R/W | 0001_B0B0h | 36.4.430/ 2562 |
| 20E_06CC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CS0_B) | 32 | R/W | 0001_B0B0h | 36.4.431/ 2563 |
| 20E_06D0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CS1_B) | 32 | R/W | 0001_B0B0h | 36.4.432/ 2565 |
| 20E_06D4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CS2_B) | 32 | R/W | 0001_B0B0h | 36.4.433/ 2567 |
| 20E_06D8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CS3_B) | 32 | R/W | 0001_B0B0h | 36.4.434/ 2569 |
| 20E_06DC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_CMD) | 32 | R/W | 0001_B0B0h | 36.4.435/ 2570 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 20E_06E0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_CLK) | 32 | R/W | 0001_B0B0h | 36.4.436/2572 |
| 20E_06E4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA00) | 32 | R/W | 0001_B0B0h | 36.4.437/2574 |
| 20E_06E8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA01) | 32 | R/W | 0001_B0B0h | 36.4.438/2576 |
| 20E_06EC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA02) | 32 | R/W | 0001_B0B0h | 36.4.439/2577 |
| 20E_06F0 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA03) | 32 | R/W | 0001_B0B0h | 36.4.440/2579 |
| 20E_06F4 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA04) | 32 | R/W | 0001_B0B0h | 36.4.441/2581 |
| 20E_06F8 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA05) | 32 | R/W | 0001_B0B0h | 36.4.442/2583 |
| 20E_06FC | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA06) | 32 | R/W | 0001_B0B0h | 36.4.443/2584 |
| 20E_0700 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA07) | 32 | R/W | 0001_B0B0h | 36.4.444/2586 |
| 20E_0704 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA0) | 32 | R/W | 0001_B0B0h | 36.4.445/2588 |
| 20E_0708 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA1) | 32 | R/W | 0001_B0B0h | 36.4.446/2590 |
| 20E_070C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA2) | 32 | R/W | 0001_B0B0h | 36.4.447/2591 |
| 20E_0710 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA3) | 32 | R/W | 0001_B0B0h | 36.4.448/2593 |
| 20E_0714 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA4) | 32 | R/W | 0001_B0B0h | 36.4.449/2595 |
| 20E_0718 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA5) | 32 | R/W | 0001_B0B0h | 36.4.450/2597 |
| 20E_071C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA6) | 32 | R/W | 0001_B0B0h | 36.4.451/2598 |
| 20E_0720 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA7) | 32 | R/W | 0001_B0B0h | 36.4.452/2600 |
| 20E_0724 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_DATA1) | 32 | R/W | 0001_B0B0h | 36.4.453/2602 |
| 20E_0728 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_DATA0) | 32 | R/W | 0001_B0B0h | 36.4.454/2604 |
| 20E_072C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_DATA3) | 32 | R/W | 0001_B0B0h | 36.4.455/2605 |
| 20E_0730 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_CMD) | 32 | R/W | 0001_B0B0h | 36.4.456/2607 |
| 20E_0734 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_DATA2) | 32 | R/W | 0001_B0B0h | 36.4.457/2609 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|------------------------|--|-----------------|--------|-------------|--------------------------------|
| 20E_0738 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_CLK) | 32 | R/W | 0001_B0B0h | 36.4.458/ 2611 |
| 20E_073C | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_CLK) | 32 | R/W | 0001_B0B0h | 36.4.459/ 2612 |
| 20E_0740 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_CMD) | 32 | R/W | 0001_B0B0h | 36.4.460/ 2614 |
| 20E_0744 | Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_DATA3) | 32 | R/W | 0001_B0B0h | 36.4.461/ 2616 |
| 20E_0748 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B7DS) | 32 | R/W | 0000_0030h | 36.4.462/ 2618 |
| 20E_074C | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_ADDDS) | 32 | R/W | 0000_0030h | 36.4.463/ 2618 |
| 20E_0750 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRMODE_CTL) | 32 | R/W | 0000_0000h | 36.4.464/ 2619 |
| 20E_0754 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL0) | 32 | R/W | 0000_0000h | 36.4.465/ 2620 |
| 20E_0758 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRPKE) | 32 | R/W | 0000_1000h | 36.4.466/ 2621 |
| 20E_075C | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL1) | 32 | R/W | 0000_0000h | 36.4.467/ 2621 |
| 20E_0760 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL2) | 32 | R/W | 0000_0000h | 36.4.468/ 2622 |
| 20E_0764 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL3) | 32 | R/W | 0000_0000h | 36.4.469/ 2623 |
| 20E_0768 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRPK) | 32 | R/W | 0000_2000h | 36.4.470/ 2624 |
| 20E_076C | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL4) | 32 | R/W | 0000_0000h | 36.4.471/ 2624 |
| 20E_0770 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRHYS) | 32 | R/W | 0000_0000h | 36.4.472/ 2625 |
| 20E_0774 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRMODE) | 32 | R/W | 0000_0000h | 36.4.473/ 2626 |
| 20E_0778 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL5) | 32 | R/W | 0000_0000h | 36.4.474/ 2627 |
| 20E_077C | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL6) | 32 | R/W | 0000_0000h | 36.4.475/ 2628 |
| 20E_0780 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL7) | 32 | R/W | 0000_0000h | 36.4.476/ 2628 |
| 20E_0784 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B0DS) | 32 | R/W | 0000_0030h | 36.4.477/ 2629 |
| 20E_0788 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B1DS) | 32 | R/W | 0000_0030h | 36.4.478/ 2630 |
| 20E_078C | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_CTLDS) | 32 | R/W | 0000_0030h | 36.4.479/ 2630 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_0790 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII) | 32 | R/W | 0008_0000h | 36.4.480/2631 |
| 20E_0794 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B2DS) | 32 | R/W | 0000_0030h | 36.4.481/2632 |
| 20E_0798 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE) | 32 | R/W | 0008_0000h | 36.4.482/2633 |
| 20E_079C | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B3DS) | 32 | R/W | 0000_0030h | 36.4.483/2634 |
| 20E_07A0 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B4DS) | 32 | R/W | 0000_0030h | 36.4.484/2634 |
| 20E_07A4 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B5DS) | 32 | R/W | 0000_0030h | 36.4.485/2635 |
| 20E_07A8 | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B6DS) | 32 | R/W | 0000_0030h | 36.4.486/2636 |
| 20E_07AC | Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM) | 32 | R/W | 0000_0000h | 36.4.487/2636 |
| 20E_07B0 | Select Input Register (IOMUXC_ASRC_ASRCK_CLOCK_6_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.488/2637 |
| 20E_07B4 | Select Input Register (IOMUXC_AUD4_INPUT_DA_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.489/2638 |
| 20E_07B8 | Select Input Register (IOMUXC_AUD4_INPUT_DB_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.490/2639 |
| 20E_07BC | Select Input Register (IOMUXC_AUD4_INPUT_RXCLK_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.491/2640 |
| 20E_07C0 | Select Input Register (IOMUXC_AUD4_INPUT_RXFS_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.492/2641 |
| 20E_07C4 | Select Input Register (IOMUXC_AUD4_INPUT_TXCLK_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.493/2642 |
| 20E_07C8 | Select Input Register (IOMUXC_AUD4_INPUT_TXFS_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.494/2643 |
| 20E_07CC | Select Input Register (IOMUXC_AUD5_INPUT_DA_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.495/2644 |
| 20E_07D0 | Select Input Register (IOMUXC_AUD5_INPUT_DB_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.496/2645 |
| 20E_07D4 | Select Input Register (IOMUXC_AUD5_INPUT_RXCLK_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.497/2646 |
| 20E_07D8 | Select Input Register (IOMUXC_AUD5_INPUT_RXFS_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.498/2647 |
| 20E_07DC | Select Input Register (IOMUXC_AUD5_INPUT_TXCLK_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.499/2648 |
| 20E_07E0 | Select Input Register (IOMUXC_AUD5_INPUT_TXFS_AMX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.500/2649 |
| 20E_07E4 | Select Input Register (IOMUXC_FLEXCAN1_RX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.501/2649 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/ page |
|------------------------|--|-----------------|--------|-------------|--------------------------------|
| 20E_07E8 | Select Input Register (IOMUXC_FLEXCAN2_RX_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.502/ 2650 |
| 20E_07F0 | Select Input Register (IOMUXC_CCM_PMIC_READY_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.503/ 2651 |
| 20E_07F4 | Select Input Register (IOMUXC_ECSPI1_CSPI_CLK_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.504/ 2651 |
| 20E_07F8 | Select Input Register (IOMUXC_ECSPI1_MISO_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.505/ 2652 |
| 20E_07FC | Select Input Register (IOMUXC_ECSPI1_MOSI_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.506/ 2653 |
| 20E_0800 | Select Input Register (IOMUXC_ECSPI1_SS0_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.507/ 2653 |
| 20E_0804 | Select Input Register (IOMUXC_ECSPI1_SS1_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.508/ 2654 |
| 20E_0808 | Select Input Register (IOMUXC_ECSPI1_SS2_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.509/ 2655 |
| 20E_080C | Select Input Register (IOMUXC_ECSPI1_SS3_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.510/ 2656 |
| 20E_0810 | Select Input Register (IOMUXC_ECSPI2_CSPI_CLK_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.511/ 2656 |
| 20E_0814 | Select Input Register (IOMUXC_ECSPI2_MISO_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.512/ 2657 |
| 20E_0818 | Select Input Register (IOMUXC_ECSPI2_MOSI_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.513/ 2658 |
| 20E_081C | Select Input Register (IOMUXC_ECSPI2_SS0_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.514/ 2658 |
| 20E_0820 | Select Input Register (IOMUXC_ECSPI2_SS1_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.515/ 2659 |
| 20E_0824 | Select Input Register (IOMUXC_ECSPI4_SS0_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.516/ 2660 |
| 20E_0828 | Select Input Register (IOMUXC_ECSPI5_CSPI_CLK_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.517/ 2661 |
| 20E_082C | Select Input Register (IOMUXC_ECSPI5_MISO_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.518/ 2662 |
| 20E_0830 | Select Input Register (IOMUXC_ECSPI5_MOSI_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.519/ 2663 |
| 20E_0834 | Select Input Register (IOMUXC_ECSPI5_SS0_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.520/ 2664 |
| 20E_0838 | Select Input Register (IOMUXC_ECSPI5_SS1_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.521/ 2665 |
| 20E_083C | Select Input Register (IOMUXC_ENET_REF_CLK_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.522/ 2666 |
| 20E_0840 | Select Input Register (IOMUXC_ENET_MAC0_MDIO_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.523/ 2667 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 20E_0844 | Select Input Register (IOMUXC_ENET_MAC0_RX_CLK_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.524/2668 |
| 20E_0848 | Select Input Register (IOMUXC_ENET_MAC0_RX_DATA0_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.525/2669 |
| 20E_084C | Select Input Register (IOMUXC_ENET_MAC0_RX_DATA1_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.526/2670 |
| 20E_0850 | Select Input Register (IOMUXC_ENET_MAC0_RX_DATA2_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.527/2671 |
| 20E_0854 | Select Input Register (IOMUXC_ENET_MAC0_RX_DATA3_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.528/2672 |
| 20E_0858 | Select Input Register (IOMUXC_ENET_MAC0_RX_EN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.529/2673 |
| 20E_085C | Select Input Register (IOMUXC_ESAI_RX_FS_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.530/2674 |
| 20E_0860 | Select Input Register (IOMUXC_ESAI_TX_FS_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.531/2675 |
| 20E_0864 | Select Input Register (IOMUXC_ESAI_RX_HF_CLK_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.532/2676 |
| 20E_0868 | Select Input Register (IOMUXC_ESAI_TX_HF_CLK_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.533/2677 |
| 20E_086C | Select Input Register (IOMUXC_ESAI_RX_CLK_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.534/2678 |
| 20E_0870 | Select Input Register (IOMUXC_ESAI_TX_CLK_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.535/2679 |
| 20E_0874 | Select Input Register (IOMUXC_ESAI_SDO0_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.536/2680 |
| 20E_0878 | Select Input Register (IOMUXC_ESAI_SDO1_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.537/2681 |
| 20E_087C | Select Input Register (IOMUXC_ESAI_SDO2_SDID3_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.538/2682 |
| 20E_0880 | Select Input Register (IOMUXC_ESAI_SDO3_SDID2_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.539/2683 |
| 20E_0884 | Select Input Register (IOMUXC_ESAI_SDO4_SDID1_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.540/2684 |
| 20E_0888 | Select Input Register (IOMUXC_ESAI_SDO5_SDID0_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.541/2685 |
| 20E_088C | Select Input Register (IOMUXC_HDMI_ICECIN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.542/2686 |
| 20E_0890 | Select Input Register (IOMUXC_HDMI_I2C_CLKIN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.543/2687 |
| 20E_0894 | Select Input Register (IOMUXC_HDMI_I2C_DATAIN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.544/2688 |
| 20E_0898 | Select Input Register (IOMUXC_I2C1_SCL_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.545/2689 |

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IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 20E_089C | Select Input Register (IOMUXC_I2C1_SDA_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.546/2690 |
| 20E_08A0 | Select Input Register (IOMUXC_I2C2_SCL_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.547/2691 |
| 20E_08A4 | Select Input Register (IOMUXC_I2C2_SDA_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.548/2692 |
| 20E_08A8 | Select Input Register (IOMUXC_I2C3_SCL_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.549/2692 |
| 20E_08AC | Select Input Register (IOMUXC_I2C3_SDA_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.550/2693 |
| 20E_08B0 | Select Input Register (IOMUXC_IPU2_SENS1_DATA10_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.551/2694 |
| 20E_08B4 | Select Input Register (IOMUXC_IPU2_SENS1_DATA11_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.552/2695 |
| 20E_08B8 | Select Input Register (IOMUXC_IPU2_SENS1_DATA12_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.553/2696 |
| 20E_08BC | Select Input Register (IOMUXC_IPU2_SENS1_DATA13_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.554/2697 |
| 20E_08C0 | Select Input Register (IOMUXC_IPU2_SENS1_DATA14_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.555/2698 |
| 20E_08C4 | Select Input Register (IOMUXC_IPU2_SENS1_DATA15_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.556/2699 |
| 20E_08C8 | Select Input Register (IOMUXC_IPU2_SENS1_DATA16_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.557/2700 |
| 20E_08CC | Select Input Register (IOMUXC_IPU2_SENS1_DATA17_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.558/2701 |
| 20E_08D0 | Select Input Register (IOMUXC_IPU2_SENS1_DATA18_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.559/2702 |
| 20E_08D4 | Select Input Register (IOMUXC_IPU2_SENS1_DATA19_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.560/2703 |
| 20E_08D8 | Select Input Register (IOMUXC_IPU2_SENS1_DATA_EN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.561/2704 |
| 20E_08DC | Select Input Register (IOMUXC_IPU2_SENS1_HSYNC_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.562/2705 |
| 20E_08E0 | Select Input Register (IOMUXC_IPU2_SENS1_PIX_CLK_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.563/2706 |
| 20E_08E4 | Select Input Register (IOMUXC_IPU2_SENS1_VSYNC_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.564/2707 |
| 20E_08E8 | Select Input Register (IOMUXC_KEY_COL5_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.565/2707 |
| 20E_08EC | Select Input Register (IOMUXC_KEY_COL6_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.566/2708 |
| 20E_08F0 | Select Input Register (IOMUXC_KEY_COL7_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.567/2709 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|--|-----------------|--------|-------------|-------------------------------|
| 20E_08F4 | Select Input Register (IOMUXC_KEY_ROW5_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.568/2709 |
| 20E_08F8 | Select Input Register (IOMUXC_KEY_ROW6_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.569/2710 |
| 20E_08FC | Select Input Register (IOMUXC_KEY_ROW7_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.570/2711 |
| 20E_0900 | Select Input Register (IOMUXC_MLB_MLB_CLK_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.571/2711 |
| 20E_0904 | Select Input Register (IOMUXC_MLB_MLB_DATA_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.572/2712 |
| 20E_0908 | Select Input Register (IOMUXC_MLB_MLB_SIG_IN_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.573/2713 |
| 20E_090C | Select Input Register (IOMUXC_SDMA_EVENTS14_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.574/2714 |
| 20E_0910 | Select Input Register (IOMUXC_SDMA_EVENTS15_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.575/2715 |
| 20E_0914 | Select Input Register (IOMUXC_SPDIF_SPDIF_IN1_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.576/2715 |
| 20E_0918 | Select Input Register (IOMUXC_SPDIF_TX_CLK2_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.577/2716 |
| 20E_091C | Select Input Register (IOMUXC_UART1_UART_RTS_B_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.578/2717 |
| 20E_0920 | Select Input Register (IOMUXC_UART1_UART_RX_DATA_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.579/2717 |
| 20E_0924 | Select Input Register (IOMUXC_UART2_UART_RTS_B_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.580/2718 |
| 20E_0928 | Select Input Register (IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.581/2719 |
| 20E_092C | Select Input Register (IOMUXC_UART3_UART_RTS_B_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.582/2719 |
| 20E_0930 | Select Input Register (IOMUXC_UART3_UART_RX_DATA_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.583/2720 |
| 20E_0934 | Select Input Register (IOMUXC_UART4_UART_RTS_B_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.584/2721 |
| 20E_0938 | Select Input Register (IOMUXC_UART4_UART_RX_DATA_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.585/2721 |
| 20E_093C | Select Input Register (IOMUXC_UART5_UART_RTS_B_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.586/2722 |
| 20E_0940 | Select Input Register (IOMUXC_UART5_UART_RX_DATA_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.587/2723 |
| 20E_0944 | Select Input Register (IOMUXC_USB_OTG_OC_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.588/2724 |
| 20E_0948 | Select Input Register (IOMUXC_USB_H1_OC_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.589/2725 |

Table continues on the next page...

IOMUXC memory map (continued)

| Absolute address (hex) | Register name | Width (in bits) | Access | Reset value | Section/page |
|------------------------|---|-----------------|--------|-------------|-------------------------------|
| 20E_094C | Select Input Register (IOMUXC_USDHC1_WP_ON_SELECT_INPUT) | 32 | R/W | 0000_0000h | 36.4.590/2726 |

36.4.1 GPR (IOMUXC_GPR0)

Address: 20E_0000h base + 0h offset = 20E_0000h

| | | | | | | | | | | | | | | | | |
|-------|-----------------|--------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | CLOCK_8_MUX_SEL | CLOCK_0_MUX_SEL | CLOCK_B_MUX_SEL | CLOCK_3_MUX_SEL | CLOCK_A_MUX_SEL | CLOCK_2_MUX_SEL | CLOCK_9_MUX_SEL | CLOCK_1_MUX_SEL | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | TX_CLK2_MUX_SEL | AUDIO_VIDEO_MUXING | | | | | | DMAREQ_MUX_SEL7 | DMAREQ_MUX_SEL6 | DMAREQ_MUX_SEL5 | DMAREQ_MUX_SEL4 | DMAREQ_MUX_SEL3 | DMAREQ_MUX_SEL2 | DMAREQ_MUX_SEL1 | DMAREQ_MUX_SEL0 | |
| W | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_GPR0 field descriptions

| Field | Description |
|--------------------------|--|
| 31–30 CLOCK_8_MUX_SEL | Selects the source of asrck_clock_8 in ASRC according to clock muxing scheme 00 audmux.amx_output_rxclk_p7 muxed with ssi3.ssi_srck 01 audmux.amx_output_rxclk_p7 10 ssi3.ssi_srck 11 ssi3.rx_bit_clk |
| 29–28 CLOCK_0_MUX_SEL | Selects the source of asrck_clock_0 in ASRC according to clock muxing scheme: 00 esai.ipp_ind_sckr muxed with esai.ipp_do_sckr 01 esai.ipp_ind_sckr 10 esai.ipp_do_sckr 11 Reserved |
| 27–26 CLOCK_B_MUX_SEL | Selects the source of asrck_clock_b in ASRC according to clock muxing scheme: 00 audmux.amx_output_txclk_p7 muxed with ssi3.ssi_stck 01 audmux.amx_output_txclk_p7 10 ssi3.ssi_stck 11 ssi3.tx_bit_clk |

Table continues on the next page...

IOMUXC_GPR0 field descriptions (continued)

| Field | Description |
|----------------------------|--|
| 25–24 CLOCK_3_MUX_SEL | Selects the source of asrck_clock_3 in ASRC according to clock muxing scheme: 00 audmux.amx_output_rxclk_p7 muxed with ssi3.ssi_srck 01 audmux.amx_output_rxclk_p7 10 ssi3.ssi_srck 11 ssi3.rx_bit_clk |
| 23–22 CLOCK_A_MUX_SEL | Selects the source of asrck_clock_a in ASRC according to clock muxing scheme: 00 audmux.amx_output_txclk_p2 muxed with ssi2.ssi_stck 01 audmux.amx_output_txclk_p2 10 ssi2.ssi_stck 11 ssi2.tx_bit_clk |
| 21–20 CLOCK_2_MUX_SEL | Selects the source of asrck_clock_2 in ASRC according to clock muxing scheme: 00 audmux.amx_output_rxclk_p2 muxed with ssi2.ssi_srck 01 audmux.amx_output_rxclk_p2 10 ssi2.ssi_srck 11 ssi2.rx_bit_clk |
| 19–18 CLOCK_9_MUX_SEL | Selects the source of asrck_clock_9 in ASRC according to clock muxing scheme: 00 audmux.amx_output_txclk_p1 muxed with ssi1.ssi_stck 01 audmux.amx_output_txclk_p1 10 ssi1.ssi_stck 11 ssi1.tx_bit_clk |
| 17–16 CLOCK_1_MUX_SEL | Selects the source of asrck_clock_1 in ASRC according to clock muxing scheme: 00 audmux.amx_output_rxclk_p1 muxed with ssi1.ssi_srck 01 audmux.amx_output_rxclk_p1 10 ssi1.ssi_srck 11 ssi1.rx_bit_clk |
| 15–14 TX_CLK2_MUX_SEL | Selects the source of tx_clk2 in SPDIF according to ASRC clock muxing scheme: 00 same source as for asrc.asrck_clock_1 01 same source as for asrc.asrck_clock_2 10 same source as for asrc.asrck_clock_3 11 Reserved |
| 13–8 AUDIO_VIDEO_MUXING | See section (TBD) for details. |
| 7 DMAREQ_MUX_SEL7 | Selects between two possible sources for SDMA_EVENT[14]: 0 spdif.drq0_spdif_b 1 iomux.sdma_ext_events[1] - External DMA Request via DISP0_DAT17 or GPIO_18 |
| 6 DMAREQ_MUX_SEL6 | Selects between two possible sources for SDMA_EVENT[23]: 0 esai. 1 i2c3.ipi_int_b |

Table continues on the next page...

IOMUXC_GPR0 field descriptions (continued)

| Field | Description |
|----------------------|--|
| 5 DMAREQ_MUX_SEL5 | Selects between two possible sources for SDMA_EVENT[9]: 0 ecspi4.ipd_req_cspi_rdma_b 1 epit2.ipi_int_epit_oc |
| 4 DMAREQ_MUX_SEL4 | Selects between two possible sources for SDMA_EVENT[10]: 0 ecspi4.ipd_req_cspi_tdma_b 1 i2c1.ipi_int_b |
| 3 DMAREQ_MUX_SEL3 | Selects between two possible sources for SDMA_EVENT[5]: 0 ecspi2.ipd_req_cspi_rdma_b 1 i2c1.ipi_int_b |
| 2 DMAREQ_MUX_SEL2 | Selects between two possible sources for SDMA_EVENT[4]: 0 ecspi1.ipd_req_cspi_tdma_b 1 i2c2.ipi_int_b |
| 1 DMAREQ_MUX_SEL1 | Selects between two possible sources for SDMA_EVENT[3]: 0 ecspi1.ipd_req_cspi_rdma_b 1 i2c3.ipi_int_b |
| 0 DMAREQ_MUX_SEL0 | Selects between two possible sources for SDMA_EVENT[2]: 0 ipu1.ipu_sdma_event 1 hdmi_tx.hdmi_tx_ophydtb[0] |

36.4.2 GPR (IOMUXC_GPR1)

Address: 20E_0000h base + 4h offset = 20E_0004h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------------|---------------|----------------|-----------------|--------------------|-----------------|---------------|--------------|----|---------|--------------|---------------|---------------|----------------|-------------|------------|
| R | CFG_L1_CLK_REMOVAL_EN | APP_CLK_REQ_N | 0 | APP_REQ_EXIT_L1 | APP_READY_ENTR_L23 | APP_REQ_ENTR_L1 | MPII_COLOR_SW | MPII_DPI_OFF | 0 | EXC_MON | ENET_CLK_SEL | MPII_IPU2_MUX | MPII_IPU1_MUX | TEST_POWERDOWN | IPU_VPU_MUX | REF_SSP_EN |
| W | | | | | | | | | 0 | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | USB_EXP_MODE | SYS_INT | USB_OTG_ID_SEL | GINT | ADDRS3[10] | ACT_CS3 | ADDRS2[10] | ACT_CS2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| W | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_GPR1 field descriptions

| Field | Description |
|-----------------------------|---|
| 31 CFG_L1_CLK_REMOVAL_EN | PCIe_CTL (CLK LOGIC CONTROLLER GLUE) - Enable the reference clock removal in L1 state. This is a bit from application register. |
| 30 APP_CLK_REQ_N | PCIe_CTL (CLK LOGIC CONTROLLER GLUE) - Indicates that application logic is ready to have reference clock removed. |
| 29 Reserved | This read-only field is reserved and always has the value 0. |
| 28 APP_REQ_EXIT_L1 | PCIe_CTL - Application Request to Exit L1. Request from the application to exit ASPM state L1. 0 PCIe application request is not set 1 PCIe application request is set |
| 27 APP_READY_ENTR_L23 | PCIe_CTL - Application Ready to Enter L23. Indication from the application that it is ready to enter the L23 state. 0 PCIe application is not ready to enter L23 1 PCIe application is ready to enter L23 |
| 26 APP_REQ_ENTR_L1 | PCIe_CTL - Application Request to Enter L1. Request from the application to enter ASPM state L1. 0 PCIe application request is not set 1 PCIe application request is set |

Table continues on the next page...

IOMUXC_GPR1 field descriptions (continued)

| Field | Description |
|----------------------|---|
| 25 MIPI_COLOR_SW | MIPI color switch control 0 MIPI color switch request is not set 1 MIPI color switch request is set |
| 24 MIPI_DPI_OFF | MIPI DPI shutdown request 0 MIPI DPI shutdown request is not set 1 MIPI DPI shutdown request is set |
| 23 Reserved | This read-only field is reserved and always has the value 0. |
| 22 EXC_MON | Exclusive monitor response select of illegal command (of lal gaskets, except MMDC) 0 OKEY response 1 SLVError (default) |
| 21 ENET_CLK_SEL | ENET TX reference clock 0 get enet tx reference clk from pad (external OSC for both external PHY and Internal Controller) 1 get enet tx reference clk from internal clock from anatop (loopback through pad), this clock also sent out to external PHY |
| 20 MIPI_IPU2_MUX | MIPI sensor to IPU-2 mux control 0 Enable mipi to IPU2 CSI1 - virtual channel is fixed to 3. 1 Enable parallel interface to IPU2 CSI1. |
| 19 MIPI_IPU1_MUX | MIPI sensor to IPU-1 mux control 0 Enable mipi to IPU1 CSI0 - virtual channel is fixed to 0. 1 Enable parallel interface to IPU1 CSI0. |
| 18 TEST_POWERDOWN | PCIe_PHY - All Circuits Power-Down Control Function: Powers down all circuitry in the PHY for IDQ testing. 0 Power down is not requested 1 Power down is requested |
| 17 IPU_VPU_MUX | IPU-1/IPU-2 to VPU signals control. This control selects between IPU-1 and IPU-2 outputs that are going to the VPU (current buffer, new frame, end of line) 0 IPU-1 is selected 1 IPU-2 is selected |
| 16 REF_SSP_EN | PCIe_PHY - Reference Clock Enable for SS function. Function: Enables the reference clock to the prescaler. The phy_ref_ssp_en signal must remain deasserted until the reference clock is running at the appropriate frequency, at which point phy_ref_ssp_en can be asserted. For lower power states, phy_ref_ssp_en can also be deasserted. 0 PCIe PHY reference clock is disabled 1 PCIe PHY reference clock is enabled |
| 15 USB_EXP_MODE | USB Exposure mode 0 Exposure mode is disabled. 1 Exposure mode is enabled. |
| 14 SYS_INT | PCIe_CTL - When SYS_INT goes from low to high, the core generates an Assert_INTx Message. When sys_int goes from high to low, the core generates a Deassert_INTx Message. |

Table continues on the next page...

IOMUXC_GPR1 field descriptions (continued)

| Field | Description |
|----------------------|--|
| | <p>0 PCIe system interrupt request is not asserted 1 PCIe system interrupt request is asserted</p> |
| 13 USB_OTG_ID_SEL | <p>"usb_otg_id' pin iomux select control. (It functions as the 'daisy chain' mux control)</p> <p>0 selects ENET_RX_ER 1 selects GPIO_1.</p> |
| 12 GINT | <p>Global interrupt "0" bit (connected to ARM IRQ#0 and GPC)</p> <p>0 Global interrupt request is not asserted 1 Global interrupt request is asserted</p> |
| 11–10 ADDRS3[10] | <p>Active Chip Select and Address Space.</p> <p>Each of the ACT_CSx represents one of the four chip selects of the EIM. When ACT_CSx=1'b1, the corresponding chip select is active and has a valid address space according to its address space configuration determined by ADDRSx[10] bits</p> <p>ADDRSx[10] is setting the space for each chip select which is active. The address space of the first active chip select must be the largest one, the following active chip select address spaces may be equal or smaller.</p> <p>Total address space size is 128 MByte.</p> <p>The supported configurations are:</p> <ul style="list-style-type: none"> CS0(128M), CS1 (0M), CS2 (0M), CS3(0M) [default configuration] CS0(64M), CS1(64M), CS2(0M), CS3(0M) CS0(64M), CS1(32M), CS2(32M), CS3(0M) CS0(32M), CS1(32M), CS2(32M), CS3(32M) <p>Address Space Configuration options (ADDRSx[10]):</p> <ul style="list-style-type: none"> 00 32 MByte 01 64 MByte 10 128 MByte 11 Reserved |
| 9 ACT_CS3 | See description for ADDRS3[10] |
| 8–7 ADDRS2[10] | See description for ADDRS3[10] |
| 6 ACT_CS2 | See description for ADDRS3[10] |
| 5–4 ADDRS1[10] | See description for ADDRS3[10] |
| 3 ACT_CS1 | See description for ADDRS3[10] |
| 2–1 ADDRS0[10] | See description for ADDRS3[10] |
| 0 ACT_CS0 | See description for ADDRS3[10] |

36.4.3 GPR (IOMUXC_GPR2)

Address: 20E_0000h base + 8h offset = 20E_0008h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------------|-----------------|-----------------|----------------|-----------------|-----------------------|---------------|--------------|--------------|---------------------|----|
| R | | | | | | | | | 0 | | | | 0 | | | |
| W | | | | | | | | | | | COUNTER_RESET_VAL[10] | | 0 | | LVDS_CLK_SHIFT[2:0] | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | D11_VS_Polarity | DIO_VS_Polarity | BIT_MAPPING_CH1 | DATA_WIDTH_CH1 | BIT_MAPPING_CH0 | DATA_WIDTH_CH0 | SPLIT_MODE_EN | CH1_MODE[10] | CH0_MODE[10] | | |
| W | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_GPR2 field descriptions

| Field | Description |
|--------------------------------|---|
| 31–22 Reserved | This read-only field is reserved and always has the value 0. |
| 21–20 COUNTER_RESET_VAL[10] | Reset value for the LDB counter which determines when the shift registers are loaded with data. NOTE: Used for debug purposes only. In normal functional operation must be '00' 00 Reset value is 5 01 Reset value is 3 10 Reset value is 4 11 Reset value is 6 |
| 19 Reserved | This read-only field is reserved and always has the value 0. |
| 18–16 LVDS_CLK_SHIFT[2:0] | Shifts the LVDS output clock in relation to the data. NOTE: Used for debug purposes only. In normal functional operation must be '000' 000 Output clock is '1100011' (normal operation) 001 Output clock is '1110001' 010 Output clock is '1111000' 011 Output clock is '1000111' 100 Output clock is '0001111' 101 Output clock is '0011111' 110 Output clock is '0111100' 111 Output clock is '1100011' |
| 15–11 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_GPR2 field descriptions (continued)

| Field | Description |
|---------------------------|--|
| 10 DI1_VS_ POLARITY | Vsync polarity for IPU's DI1 interface. 0 ipu_di1_vsync is active high. 1 ipu_di1_vsync is active low. |
| 9 DIO_VS_ POLARITY | Vsync polarity for IPU's DI0 interface. 0 ipu_di0_vsync is active high. 1 ipu_di0_vsync is active low. |
| 8 BIT_MAPPING_ CH1 | Data mapping for LVDS channel 1. 0 Use SPWG standard. 1 Use JEIDA standard. |
| 7 DATA_WIDTH_ CH1 | Data width for LVDS channel 1. NOTE: This bit must be set when using JEIDA standard (bit_mapping_ch1 is set) 0 Data width is 18 bits wide (lvds1_tx3 is not used) 1 Data width is 24 bits wide. |
| 6 BIT_MAPPING_ CH0 | Data mapping for LVDS channel 0. 0 Use SPWG standard. 1 Use JEIDA standard. |
| 5 DATA_WIDTH_ CH0 | Data width for LVDS channel 0. NOTE: This bit must be set when using JEIDA standard (bit_mapping_ch0 is set) 0 Data width is 18 bits wide (lvds0_tx3 is not used) 1 Data width is 24 bits wide. |
| 4 SPLIT_MODE_ EN | Enable split mode. 0 Split mode is disabled. 1 Split mode is enabled. In this mode both channels should be enabled and working with the same DI (ch0_mode and ch1_mode should both be either '01' or '11') |
| 3–2 CH1_MODE[10] | LVDS channel 1 operation mode 00 Channel disabled. 01 Channel enabled, routed to DIO 10 Channel disabled. 11 Channel enabled, routed to DI1. |
| CH0_MODE[10] | LVDS channel 0 operation mode 00 Channel disabled. 01 Channel enabled, routed to DIO 10 Channel disabled. 11 Channel enabled, routed to DI1. |

36.4.4 GPR (IOMUXC_GPR3)

Address: 20E_0000h base + Ch offset = 20E_000Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|------------------|------------------|------------------|------------------|----------|---------------|---------------|--------------|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | CORE2_DBG_ACK_EN | CORE1_DBG_ACK_EN | CORE0_DBG_ACK_EN | TZASC2_BOOT_LOCK | TZASC1_BOOT_LOCK | IPU_DIAG | LVDS1_MUX_CTL | LVDS0_MUX_CTL | MIPI_MUX_CTL | | | | | | | 0 |
| | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_GPR3 field descriptions

| Field | Description |
|------------------|---|
| 31 Reserved | This read-only field is reserved and always has the value 0. |
| 30–29 GPU_DBG | GPU debug busses to IOMUX 00 GPU3D 01 GPU2D 10 OpenVG 11 Reserved |

Table continues on the next page...

IOMUXC_GPR3 field descriptions (continued)

| Field | Description |
|-------------------------------|--|
| 28 BCH_WR_ CACHE_CTL | Control BCH block cacheable attribute of AXI write transactions ¹ 0 Cacheable attribute is off for write transactions. 1 Cacheable attribute is on for write transactions. |
| 27 BCH_RD_ CACHE_CTL | Control BCH block cacheable attribute of AXI read transactions ¹ 0 Cacheable attribute is off for read transactions. 1 Cacheable attribute is on for read transactions. |
| 26 uSDHCx_WR_ CACHE_CTL | Control uSDHCx [1-4] blocks cacheable attribute of AXI write transactions ¹ 0 Cacheable attribute is off for write transactions. 1 Cacheable attribute is on for write transactions. |
| 25 uSDHCx_RD_ CACHE_CTL | Control uSDHCx [1-4] blocks cacheable attribute of AXI read transactions ¹ 0 Cacheable attribute is off for read transactions. 1 Cacheable attribute is on for read transactions. |
| 24-21 OCRAM_CTL | OCRAM_CTL[24] write address pipeline control bit. When this feature is enabled, the write address from the AXI master would be delayed 1 cycle before it can be accepted by the on-chip RAM. This can avoid any setup time issue for the write access on the memory cell at high frequency. Enabling this feature would cost at most 1 more clock cycle for each AXI write transaction, i.e., at most 1 more clock cycle for each write burst with multiple beats of data. When this feature is disabled, the write address from the AXI master can be accepted by the on-chip RAM without delay, and data can be written to memory at this cycle (if no other access and write data is also ready at this cycle). 0 write address pipeline is disabled 1 write address pipeline is enabled OCRAM_CTL[23] - write data pipeline control bit When this feature is enabled, the write data from the AXI master would be delayed 1 cycle before it can be accepted by the on-chip RAM. This can avoid any setup time issue for the write access on the memory cell at high frequency. Enabling this feature would cost at most 1 more clock cycle for each AXI write transaction, i.e., at most 1 more clock cycle for each write burst with multiple beats of data. When this feature is disabled, the write data from the AXI master can be accepted by the on-chip RAM without delay, and data can be written to memory at this cycle (if no other access and write address is also ready at this cycle). 0 write data pipeline is disabled 1 write data pipeline is enabled OCRAM_CTL[22] read address pipeline control bit. When this feature is enabled, the read address from the AXI master would be delayed 1 cycle before it can be accepted by the on-chip RAM. This can avoid any setup time issue for the read access on the memory cell at high frequency. Enabling this feature would cost at most 1 more clock cycle for each AXI read transaction, i.e., at most 1 more clock cycle for each read burst with multiple beats of data. When this feature is disabled, the read address from the AXI master can be accepted by the on-chip RAM without delay, and data can become ready for master at next clock cycle (if no other access and no read data wait). 0 read address pipeline is disabled 1 read address pipeline is enabled OCRAM_CTL[21] - read data wait state control bit |

Table continues on the next page...

IOMUXC_GPR3 field descriptions (continued)

| Field | Description |
|------------------------|---|
| | <p>When the read data wait state is enabled, it will cost 2 cycles for each read access, (each beat of a read burst). This can avoid the potential timing problem caused by the relatively longer memory access time at higher frequency. When this feature is disabled, it only costs 1 clock cycle to finish a read transaction, i.e., get read data back in the next cycle of read request becomes valid on the bus.</p> <p>0 read data pipeline is disabled 1 read data pipeline is enabled</p> |
| 20–17 OCRAM_STATUS | <p>This field shows the OCRAM pipeline settings status, controlled by OCRAM_CTL[24:21] bits respectively. When the control bit is changed, the corresponding status bit goes high and keeps high until this new configuration is applied the internal logic. This provides a way for software to detect that the configuration has become valid. The suggested flow for changing the configuration in software is:</p> <ul style="list-style-type: none"> • set/clear the control bit • poll the status bit until it goes to 0 <p>OCRAM_STATUS[17] shows the write address pipeline status. This bit value reflects the propagation of the respective control bit to OCRAM memory.</p> <p>OCRAM_STATUS[18] shows the write data pipeline status. This bit value reflects the propagation of the respective control bit to OCRAM memory.</p> <p>OCRAM_STATUS[19] shows the read address pipeline status. This bit value reflects the propagation of the respective control bit to OCRAM memory.</p> <p>OCRAM_STATUS[20] shows the read data pipeline status. This bit value reflects the propagation of the respective control bit to OCRAM memory.</p> <p>0 read data pipeline configuration valid 1 read data pipeline control bit changed</p> |
| 16 CORE3_DBG_ACK_EN | <p>Mask control of Core 3 debug acknowledge to global debug acknowledge</p> <p>0 Core 3 debug acknowledge is part of global acknowledge. 1 Core 3 debug acknowledge is masked by this bit, and it is not part of global acknowledge.</p> |
| 15 CORE2_DBG_ACK_EN | <p>Mask control of Core 2 debug acknowledge to global debug acknowledge</p> <p>0 Core 2 debug acknowledge is part of global acknowledge. 1 Core 2 debug acknowledge is masked by this bit, and it is not part of global acknowledge.</p> |
| 14 CORE1_DBG_ACK_EN | <p>Mask control of Core 1 debug acknowledge to global debug acknowledge.</p> <p>0 Core 1 debug acknowledge is part of global acknowledge. 1 Core 1 debug acknowledge is masked by this bit, and it is not part of global acknowledge.</p> |
| 13 CORE0_DBG_ACK_EN | <p>Mask control of Core 0 debug acknowledge to global debug acknowledge</p> <p>0 Core 0 debug acknowledge is part of global acknowledge. 1 Core 0 debug acknowledge is masked by this bit, and it is not part of global acknowledge.</p> |
| 12 TZASC2_BOOT_LOCK | <p>TZASC-2 secure boot lock</p> <p>0 secure boot lock is disabled. 1 secure boot lock is enabled</p> |
| 11 TZASC1_BOOT_LOCK | <p>TZASC-1 secure boot lock</p> <p>0 secure boot lock is disabled. 1 secure boot lock is enabled</p> |

Table continues on the next page...

IOMUXC_GPR3 field descriptions (continued)

| Field | Description |
|----------------------|---|
| 10 IPU_DIAG | IPU diagnostic debug bus mux 0 IPU1 diagnostic bus is selected 1 IPU2 diagnostic bus is selected |
| 9–8 LVDS1_MUX_CTL | LVDS1 MUX control 00 LVDS1 source is IPU1 DI0 port 01 LVDS1 source is IPU1 DI1 port 10 LVDS1 source is IPU2 DI0 port 11 LVDS1 source is IPU2 DI1 port |
| 7–6 LVDS0_MUX_CTL | LVDS0 MUX control 00 LVDS0 source is IPU1 DI0 port 01 LVDS0 source is IPU1 DI1 port 10 LVDS0 source is IPU2 DI0 port 11 LVDS0 source is IPU2 DI1 port |
| 5–4 MIPI_MUX_CTL | MIPI MUX control 00 MIPI source is IPU1 DI0 port 01 MIPI source is IPU1 DI1 port 10 MIPI source is IPU2 DI0 port 11 MIPI source is IPU2 DI1 port |
| 3–2 HDMI_MUX_CTL | HDMI MUX control 00 HDMI source is IPU1 DI0 port 01 HDMI source is IPU1 DI1 port 10 HDMI source is IPU2 DI0 port 11 HDMI source is IPU2 DI1 port |
| Reserved | This read-only field is reserved and always has the value 0. |

- Set of the cache bits, enable packet optimization through the bus system to DDR controller. The only side effect is that bus may change the nature of the accesses, which may lead to problems when accessing FIFO type address. In most typical cases, these bits should be set. For the GPU3D, GPU2D and OpenVG, such settings are possible through the IP programming model. For few peripherals, for these bits to take effect, it is required to also select set '1' to 'cache-mux' control bit.

36.4.5 GPR (IOMUXC_GPR4)

Address: 20E_0000h base + 10h offset = 20E_0010h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------|------------------|----|----|--------------------|--------------------|------------------|------------------|
| R | VDOA_WR_CACHE_SEL | VDOA_RD_CACHE_SEL | VDOA_WR_CACHE_VAL | VDOA_RD_CACHE_VAL | PCIe_WR_CACHE_SEL | PCIe_RD_CACHE_SEL | PCIe_WR_CACHE_VAL | PCIe_RD_CACHE_VAL | 0 | | | | SDMA_STOP_ACK | CAN2_STOP_ACK | CAN1_STOP_ACK | ENET_STOP_ACK |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | VPU_WR_CACHE_SEL | VPU_RD_CACHE_SEL | 0 | 0 | VPU_P_WR_CACHE_VAL | VPU_P_RD_CACHE_VAL | IPU_WR_CACHE_CTL | IPU_RD_CACHE_CTL |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_GPR4 field descriptions

| Field | Description |
|----------------------|--|
| 31 VDOA_WR_CACHE_SEL | This bit selects the cacheable attribute of VDOA AXI write transactions ¹ 0 The write transactions cacheable attribute is driven by the VDOA core 1 The write transactions cacheable attribute is driven by VDOA_WR_CACHE_VAL. |
| 30 VDOA_RD_CACHE_SEL | This bit selects the cacheable attribute of VDOA AXI read transactions ¹ 0 The read transaction cacheable attribute is driven by the VDOA core 1 The read transaction cacheable attribute is driven by VDOA_RD_CACHE_VAL. |
| 29 VDOA_WR_CACHE_VAL | VDOA block cacheable attribute value of AXI write transactions The value of VDOA_WR_CACHE_VAL is affecting the transactions only if VDOA_WR_CACHE_SEL is set. ¹ 0 Cacheable attribute is off for write transactions. 1 Cacheable attribute is on for write transactions. |
| 28 VDOA_RD_CACHE_VAL | VDOA block cacheable attribute value of AXI read transactions The value of VDOA_RD_CACHE_VAL is affecting the transactions only if VDOA_RD_CACHE_SEL is set. ¹ 0 Cacheable attribute is off for read transactions. 1 Cacheable attribute is on for read transactions. |
| 27 PCIe_WR_CACHE_SEL | This bit selects the cacheable attribute of PCIe AXI write transactions ¹ |

Table continues on the next page...

IOMUXC_GPR4 field descriptions (continued)

| Field | Description |
|-------------------------|---|
| | <p>0 The write transactions cacheable attribute is driven by the PCIe core 1 The write transactions cacheable attribute is driven by PCIe_WR_CACHE_VAL.</p> |
| 26 PCIe_RD_CACHE_SEL | <p>This bit selects the cacheable attribute of PCIe AXI read transactions)¹</p> <p>0 The read transaction cacheable attribute is driven by the PCIe core 1 The read transaction cacheable attribute is driven by PCIe_RD_CACHE_VAL.</p> |
| 25 PCIe_WR_CACHE_VAL | <p>PCIe block cacheable attribute value of AXI write transactions The value of PCIe_WR_CACHE_VAL is affecting the transactions only if PCIe_WR_CACHE_SEL is set.¹</p> <p>0 Cacheable attribute is off for write transactions. 1 Cacheable attribute is on for write transactions.</p> |
| 24 PCIe_RD_CACHE_VAL | <p>PCIe block cacheable attribute value of AXI read transactions The value of PCIe_RD_CACHE_VAL is affecting the transactions only if PCIe_RD_CACHE_SEL is set.¹</p> <p>0 Cacheable attribute is off for read transactions. 1 Cacheable attribute is on for read transactions.</p> |
| 23–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19 SDMA_STOP_ACK | <p>SDMA stop acknowledge. This is status (read only) bit.</p> <p>0 SDMA stop acknowledge is not asserted. 1 SDMA stop acknowledge is asserted, SDMA is in STOP mode.</p> |
| 18 CAN2_STOP_ACK | <p>CAN-2 stop acknowledge. This is status (read only) bit.</p> <p>0 CAN-2 stop acknowledge is not asserted. 1 CAN-2 stop acknowledge is asserted, CAN-2 is in STOP mode.</p> |
| 17 CAN1_STOP_ACK | <p>CAN-1 stop acknowledge. This is status (read only) bit.</p> <p>0 CAN-1 stop acknowledge is not asserted. 1 CAN-1 stop acknowledge is asserted, CAN-1 is in STOP mode.</p> |
| 16 ENET_STOP_ACK | <p>ENET stop acknowledge. This is status (read only) bit.</p> <p>0 ENET stop acknowledge is not asserted. 1 ENET stop acknowledge is asserted, ENET is in STOP mode.</p> |
| 15–8 SOC_VERSION | This is status (read only) field. |
| 7 VPU_WR_CACHE_SEL | <p>This bit selects the cacheable attribute of VPU AXI write transactions (both primary and secondary AXI buses)¹</p> <p>0 The write transactions cacheable attribute is driven by the VPU core 1 The write transactions cacheable attribute is driven by VPU_SEC_WR_CACHE_VAL for secondary bus and VPU_P_WR_CACHE_VAL for primary bus.</p> |
| 6 VPU_RD_CACHE_SEL | <p>This bit selects the cacheable attribute of VPU AXI read transactions (both primary and secondary AXI buses)¹</p> <p>0 The read transaction cacheable attribute is driven by the VPU core 1 The read transaction cacheable attribute is driven by VPU_SEC_RD_CACHE_VAL for secondary bus and VPU_P_RD_CACHE_VAL for primary bus.</p> |

Table continues on the next page...

IOMUXC_GPR4 field descriptions (continued)

| Field | Description |
|-------------------------|--|
| 5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 Reserved | This read-only field is reserved and always has the value 0. |
| 3 VPU_P_WR_CACHE_VAL | VPU (primary bus) block cacheable attribute value of AXI write transactions The value of VPU_P_WR_CACHE_VAL is affecting the transactions only if VPU_WR_CACHE_SEL is set. ¹ 0 Cacheable attribute is off for write transactions. 1 Cacheable attribute is on for write transactions. |
| 2 VPU_P_RD_CACHE_VAL | VPU (primary bus) block cacheable attribute value of AXI read transactions The value of VPU_P_RD_CACHE_VAL is affecting the transactions only if VPU_RD_CACHE_SEL is set. ¹ 0 Cacheable attribute is off for read transactions. 1 Cacheable attribute is on for read transactions. |
| 1 IPU_WR_CACHE_CTL | Control IPU-1 and IPU-2 block cacheable attribute of AXI write transactions ¹ 0 Cacheable attribute is off for write transactions. 1 Cacheable attribute is on for write transactions. |
| 0 IPU_RD_CACHE_CTL | Control IPU-1 and IPU-2 block cacheable attribute of AXI read transactions ¹ 0 Cacheable attribute is off for read transactions. 1 Cacheable attribute is on for read transactions. |

1. Set of the cache bits, enable packet optimization through the bus system to DDR controller. The only side effect is that bus may change the nature of the accesses, which may lead to problems when accessing FIFO type address. In most typical cases, these bits should be set. For the GPU3D, GPU2D and OpenVG, such settings are possible through the IP programming model. For few peripherals, for these bits to take effect, it is required to also select set '1' to 'cache-mux' control bit.

36.4.6 GPR (IOMUXC_GPR5)

Address: 20E_0000h base + 14h offset = 20E_0014h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|---------|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | ARM_WFE | | ARM_WFI | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_GPR5 field descriptions

| Field | Description |
|------------------|---|
| 31–9 Reserved | This read-only field is reserved and always has the value 0. |
| 8 L2_CLK_STOP | L2 cache clock stop indication (this is a status, read only bit) 0 L2 cache clock is running 1 L2 cache clock stopped |
| 7–4 ARM_WFE | ARM WFE event out indication on WFE state of the cores (these are status, read only bits) |

Table continues on the next page...

IOMUXC_GPR5 field descriptions (continued)

| Field | Description |
|---------|---|
| | 0 ARM Core[GPR5-index - 4] is not in “Wait for Event” mode 1 ARM Core[GPR5-index - 4] is in “Wait for Event” mode |
| ARM_WFI | ARM WFI event out indicating on WFI state of the cores (these are status, read only bits) 0 ARM Core[GPR5-index] is not in “Wait for Interrupt” mode 1 ARM Core[GPR5-index] is in “Wait for Interrupt” mode |

36.4.7 GPR (IOMUXC_GPR6)

Address: 20E 0000h base + 18h offset = 20E 0018h

IOMUXC_GPR6 field descriptions

| Field | Description |
|---------------------------|--|
| 31–28 IPU1_ID11_RD_QoS | IPU1 Read AXI ID=11 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 27–24 IPU1_ID10_RD_QoS | IPU1 Read AXI ID=10 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 23–20 IPU1_ID01_RD_QoS | IPU1 Read AXI ID=01 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 19–16 IPU1_ID00_RD_QoS | IPU1 Read AXI ID=00 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 15–12 IPU1_ID11_WR_QoS | IPU1 Write AXI ID=11 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 11–8 IPU1_ID10_WR_QoS | IPU1 Write AXI ID=10 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 7–4 IPU1_ID01_WR_QoS | IPU1 Write AXI ID=01 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |

Table continues on the next page...

IOMUXC_GPR6 field descriptions (continued)

| Field | Description |
|------------------|--|
| IPU1_ID00_WR_QoS | IPU1 Write AXI ID=00 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |

36.4.8 GPR (IOMUXC_GPR7)

Address: 20E_0000h base + 1Ch offset = 20E_001Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Reset 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0

IOMUXC_GPR7 field descriptions

| Field | Description |
|---------------------------|--|
| 31–28 IPU2_ID11_RD_QoS | IPU2 Read AXI ID=11 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 27–24 IPU2_ID10_RD_QoS | IPU2 Read AXI ID=10 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 23–20 IPU2_ID01_RD_QoS | IPU2 Read AXI ID=01 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 19–16 IPU2_ID00_RD_QoS | IPU2 Read AXI ID=00 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 15–12 IPU2_ID11_WR_QoS | IPU2 Write AXI ID=11 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 11–8 IPU2_ID10_WR_QoS | IPU2 Write AXI ID=10 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| 7–4 IPU2_ID01_WR_QoS | IPU2 Write AXI ID=01 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |
| IPU2_ID00_WR_QoS | IPU2 Write AXI ID=00 Quality of Service (QoS) priority 0xxx - 3 lsb's will be passed as configured 1xxx - 1111 |

36.4.9 GPR (IOMUXC_GPR8)

Address: 20E_0000h base + 20h offset = 20E_0020h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Reset 0

IOMUXC_GPR8 field descriptions

| Field | Description |
|----------------------------------|--|
| 31–25 PCS_TX_SWING_LOW | PCIe_PHY - This static value sets the launch amplitude of the transmitter when pipe0_tx_swing is set to 1'b0 (default state). 7'hxx - TX launch amplitude swing_low value. |
| 24–18 PCS_TX_SWING_FULL | PCIe_PHY - This static value sets the Tx driver SWING_FULL value. 7'hxx - Gen2 TX SWING FULL value. |
| 17–12 PCS_TX_DEEMPH_GEN2_6DB | PCIe_PHY - This static value sets the Tx driver de-emphasis value in the case where pipe0_tx_deemph is set to 1'b0 and the PHY is running at the Gen2 (6db) rate. 6'hxx - Gen2 (6db) De-emphasis value. |
| 11–6 PCS_TX_DEEMPH_GEN2_3P5DB | PCIe_PHY - This static value sets the Tx driver de-emphasis value in the case where pipe0_tx_deemph is set to 1'b1 (the default setting) and the PHY is running at the Gen2 (3p5db) rate. 6'hxx - Gen2 De-emphasis value. |
| PCS_TX_DEEMPH_GEN1 | PCIe_PHY - This static value sets the Tx driver de-emphasis value in the case where pipe0_tx_deemph is set to 1'b1 (the default setting) and the PHY is running at the Gen1 rate. 6'hxx - Gen1 De-emphasis value. |

36.4.10 GPR (IOMUXC_GPR9)

Address: 20E_0000h base + 24h offset = 20E_0024h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_GPR9 field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| 1 TZASC2_BYP | TZASC-2 BYPASS MUX control 0 The TZASC-2 is bypassed and the transactions to DDR are not being checked. 1 The TZASC-2 is not bypassed and the transactions to DDR are being monitored / checked. |
| 0 TZASC1_BYP | TZASC-1 BYPASS MUX control 0 The TZASC-1 is bypassed and the transactions to DDR are not being checked. 1 The TZASC-1 is not bypassed and the transactions to DDR are being monitored / checked. |

36.4.11 GPR (IOMUXC_GPR10)

Address: 20E_0000h base + 28h offset = 20E_0028h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|-------------|-----------------|-------------------|----|----|----|----|----|----|------------------|----|--------------------|----|--------------------|
| R | 0 | | LOCK_DBG_EN | LOCK_DBG_CLK_EN | LOCK_SEC_ERR_RESP | | | | | | | LOCK_OCRAM_TZ_EN | | LOCK_DCIC2_MUX_CTL | | LOCK_DCIC1_MUX_CTL |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | DBG_EN | DBG_CLK_EN | SEC_ERR_RESP | | | | | | | OCRAM_TZ_EN | | DCIC2_MUX_CTL | | DCIC1_MUX_CTL |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_GPR10 field descriptions

| Field | Description |
|-----------------------------|--|
| 31–30 Reserved | This read-only field is reserved and always has the value 0. |
| 29 LOCK_DBG_EN | Lock DBG_EN field for changes. This is a sticky field, once set it can't be cleared (only by reset). 0 Field is not locked 1 Field is locked (read access only) |
| 28 LOCK_DBG_CLK_EN | Lock DBG_CLK_EN field for changes. This is a sticky field, once set it can't be cleared (only by reset). 0 Field is not locked 1 Field is locked (read access only) |
| 27 LOCK_SEC_ERR_RESP | Lock SEC_ERR_RESP field for changes. This is a sticky field, once set it can't be cleared (only by reset). 0 Field is not locked 1 Field is locked (read access only) |
| 26–21 LOCK_OCRAM_TZ_ADDR | Lock OCRAM_TZ_ADDR field for changes. This is a sticky field, once set it can't be cleared (only by reset). 0 Field is not locked 1 Field is locked (read access only) |
| 20 LOCK_OCRAM_TZ_EN | Lock OCRAM_TZ_EN field for changes. This is a sticky field, once set it can't be cleared (only by reset). 0 Field is not locked 1 Field is locked (read access only) |

Table continues on the next page...

IOMUXC_GPR10 field descriptions (continued)

| Field | Description |
|---------------------------------|--|
| 19–18 LOCK_DCIC2_ MUX_CTL | Lock DCIC2_MUX_CTL field for changes. This is a sticky field, once set it can't be cleared (only by reset). 0 Field is not locked 1 Field is locked (read access only) |
| 17–16 LOCK_DCIC1_ MUX_CTL | Lock DCIC1_MUX_CTL field for changes. This is a sticky field, once set it can't be cleared (only by reset). 0 Field is not locked 1 Field is locked (read access only) |
| 15–14 Reserved | This read-only field is reserved and always has the value 0. |
| 13 DBG_EN | ARM non secure (non-invasive) debug enable 0 Debug turned off. 1 Debug enabled (default). |
| 12 DBG_CLK_EN | ARM Debug clock enable 0 Debug turned off. 1 Debug enabled (default). |
| 11 SEC_ERR_ RESP | Security error response enable for all security gaskets (on both AHB and AXI busses) 0 OKEY response 1 SLVError (default) |
| 10–5 OCRAM_TZ_ ADDR | OCRAM TrustZone (TZ) start address. This is the start address of the secure memory region within the OCRAM memory space is 4KB granularity. The start address affects the OCRAM transactions only if OCRAM_TZ_EN bit is set. The OCRAM TZ ENDADDR is not configurable and is set to the end of OCRAM memory space. |
| 4 OCRAM_TZ_EN | OCRAM TrustZone (TZ) enable. 0 The TrustZone feature is disabled. Entire OCRAM space is available for all access types (secure/non-secure/user/supervisor). 1 The TrustZone feature is enabled. Access to address in the range specified by [ENDADDR:STARTADDR] follows the execution mode access policy described in CSU chapter. |
| 3–2 DCIC2_MUX_ CTL | DCIC-2 MUX control 00 DCIC-2 source is IPU1 DI1 port 01 DCIC-2 source is LVDS0 10 DCIC-2 source is LVDS1 11 DCIC-2 source is MIPI DPI |
| DCIC1_MUX_ CTL | DCIC-1 MUX control 00 DCIC-1 source is IPU1 or IPU2 DI0 port 01 DCIC-1 source is LVDS0 10 DCIC-1 source is LVDS1 11 DCIC-1 source is HDMI |

36.4.12 GPR (IOMUXC_GPR11)

Address: 20E_0000h base + 2Ch offset = 20E_002Ch

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | 0 |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | | | | | 0 |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_GPR11 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 Reserved | This read-only field is reserved and always has the value 0. |
| 15–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 Reserved | This read-only field is reserved and always has the value 0. |

36.4.13 GPR (IOMUXC_GPR12)

Address: 20E_0000h base + 30h offset = 20E_0030h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|-------------|-----------------|------------------|-----------------|-----------------|----|----|----|----|---------------|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | 0 | | | | | | | | | | | | |
| W | | | | | | ARMP_IPG_CLK_EN | ARMP_AHB_CLK_EN | ARMP_ATB_CLK_EN | ARMP_APB_CLK_EN | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | DEVICE_TYPE | | APP_LTSSM_ENABLE | APP_PM_XMT_PME | | | | | | uSDHC_DBG_MUX | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_GPR12 field descriptions

| Field | Description |
|------------------------------------|--|
| 31–28 Reserved | This read-only field is reserved and always has the value 0. |
| 27 ARMP_IPG_ CLK_EN | ARM platform IPG clock enable 0 IPG clock is not running (gated). 1 IPG clock is running (enabled). |
| 26 ARMP_AHB_ CLK_EN | ARM platform AHB clock enable 0 IPG clock is not running (gated). 1 IPG clock is running (enabled). |
| 25 ARMP_ATB_ CLK_EN | ARM platform ATB clock enable 0 IPG clock is not running (gated). 1 IPG clock is running (enabled). |
| 24 ARMP_APB_ CLK_EN | ARM platform APB clock enable 0 IPG clock is not running (gated). 1 IPG clock is running (enabled). |
| 23–21 PCIe_CTL_7 | PCIe control of diagnostic bus select (Drive 'cxpl_diag_ctrl' PCI controller input) |
| 20–17 DIA_STATUS_ BUS_SELECT | PCIe_CTL - used for debug to select what part of diag_status_bus will be reflected on the 32 bits of the iomux |
| 16 APPS_PM_ XMT_TURNOFF | PCIe_CTL - Request from the application to generate a PM_Turn_Off Message. |
| 15–12 DEVICE_TYPE | PCIe_CTL - Device/Port Type. Indicates the specific type of this PCI Express Function (EP or RC) DEVICE_TYPE field values 0011–1111 are reserved. 0000 PCIE_EP — EP Mode 0010 PCIE_RC — RC Mode |
| 11 APP_INIT_RST | PCIe_CTL - Request from the application to send a Hot Reset to the downstream device. |
| 10 APP_LTSSM_ ENABLE | PCIe_CTL - Driven low by the application after reset to hold the LTSSM in the Detect state until the application is ready. When the application has finished initializing the core configuration registers, it asserts app_ltssm_enable to allow the LTSSM to continue Link establishment. 0 Application is not ready. 1 Application is ready. |
| 9 APPS_PM_ XMT_PME | PCIe_CTL - Wake Up. Used by application logic to wake up the PMC state machine from a D1, D2 or D3 power state. Upon wake-up, the core sends a PM_PME Message |
| 8–4 LOS_LEVEL | PCIe_PHY - Loss-of-Signal Detector Sensitivity Level Control Function: Sets the sensitivity level for the Loss-of-Signal detector. This signal must be set to 0x9 |
| 3–2 uSDHC_DBG_ MUX | uSDHC debug bus IO mux control '00' - uSDHC1 debug '01' - uSDHC2 debug |

Table continues on the next page...

IOMUXC_GPR12 field descriptions (continued)

| Field | Description |
|----------|--|
| | '10' - uSDHC3 debug '11' - uSDHC4 debug |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.14 GPR (IOMUXC_GPR13)

| SATA_PHY_6 | PHUG | FRUG | fast_startup | Frequency Tolerance (ppm) |
|------------|----------|------|--------------|---------------------------|
| 000 | 1 | 1 | None | 780 |
| 001 | 2 | 2 | None | 780 |
| 010 | 1 | 4 | None | 6,250 |
| 011 | 2 | 4 | None | 6,250 |
| 1xx | Reserved | | | |

Address: 20E_0000h base + 34h offset = 20E_0034h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|---------------|---------------|---------------|---------------|------------|----|----|------------|----|------------|----|----|------------|------------|----|
| R | 0 | SDMA_STOP_REQ | CAN2_STOP_REQ | CAN1_STOP_REQ | ENET_STOP_REQ | SATA_PHY_8 | | | SATA_PHY_7 | | SATA_PHY_6 | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | SATA_SPEED | SATA_PHY_5 | SATA_PHY_4 | SATA_PHY_3 | SATA_PHY_2 | | | | | | | | | SATA_PHY_1 | SATA_PHY_0 | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

IOMUXC_GPR13 field descriptions

| Field | Description |
|---------------------|--|
| 31 Reserved | This read-only field is reserved and always has the value 0. |
| 30 SDMA_STOP_REQ | SDMA stop request 0 Stop request off. 1 Stop request on. |

Table continues on the next page...

IOMUXC_GPR13 field descriptions (continued)

| Field | Description |
|---------------------|--|
| 29 CAN2_STOP_REQ | CAN2 stop request 0 Stop request off. 1 Stop request on. |
| 28 CAN1_STOP_REQ | CAN1 stop request 0 Stop request off. 1 Stop request on. |
| 27 ENET_STOP_REQ | ENET stop request 0 Stop request off. 1 Stop request on. |
| 26–24 SATA_PHY_8 | SATA_PHY Rx - Receiver Equalization control 000 0.5 dB 001 1.0 dB 010 1.5 dB 011 2.0 dB 100 2.5 dB 101 3.0 dB (default) 110 3.5 dB 111 4.0 dB |
| 23–19 SATA_PHY_7 | SATA PHY Rx - Loss of signal detector level. Below the recommended value are shown 10000 SATA1i 10000 SATA1m 11010 SATA1x 10010 SATA2i 10010 (default) SATA2m 11010 SATA2x |
| 18–16 SATA_PHY_6 | SATA PHY Rx - DPLL mode control, sets phase and frequency gain of receiver DPLL For bits encoding see GPR (IOMUXC_GPR13) below. |
| 15 SATA_SPEED | Indicates SATA PHY speed mode 0 1.5 GHz 1 3.0 GHz |
| 14 SATA_PHY_5 | SATA PHY - Spread Spectrum Enable. Enables spread spectrum clock production. If the applied RefClk is already spread spectrum, this bit must be deasserted. 0 Spread Spectrum disabled 1 Spread spectrum enabled |
| 13–11 SATA_PHY_4 | SATA PHY -Transmit Attenuation control, provides discrete driver attenuation factors (from full driver level). 000 16/16 001 14/16 010 12/16 011 10/16 |

Table continues on the next page...

IOMUXC_GPR13 field descriptions (continued)

| Field | Description |
|--------------------|---|
| | 100 9/16 (default) 101 8/16 110 Reserved 111 Reserved |
| 10–7 SATA_PHY_3 | SATA PHY Tx -Transmit Boost Control, ratio of drive level of transmission bit to non transmission bit. 0000 0dB 0001 0.37 dB 0010 0.74 dB 0011 1.11 dB 0100 1.48 dB 0101 1.85 dB 0110 2.22 dB 0111 2.59 dB 1000 2.96 dB 1001 3.33 dB (default) 1010 3.70 dB 1011 4.07 dB 1100 4.44 dB 1101 4.81 dB 1110 5.28 dB 1111 5.75 dB |
| 6–2 SATA_PHY_2 | SATA PHY - Transmit level settings. Fine resolution settings of transmit signal level, common to all lanes connected to one clock module. 00000 0.937 V 00001 0.947 V 00010 0.957 V 00011 0.966 V 00100 0.976 V 00101 0.986 V 00110 0.996 V 00111 1.005 V 01000 1.015 V 01001 1.025 V 01010 1.035 V 01011 1.045 V 01100 1.054 V 01101 1.064 V 01110 1.074 V 01111 1.084 V 10000 1.094 V 10001 1.104 V (default) 10010 1.113 V 10011 1.123 V 10100 1.133 V 10101 1.143 V |

Table continues on the next page...

IOMUXC_GPR13 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 10110 1.152 V 10111 1.162 V 11000 1.172 V 11001 1.182 V 11010 1.191 V 11011 1.201 V 11100 1.211 V 11101 1.221 V 11110 1.230 V 11111 1.240 V |
| 1 SATA_PHY_1 | SATA PHY internal PLL Reference Clock Enable 0 Disable the reference clock to the internal PLL of SATA PHY 1 Enable the reference clock to the internal PLL of SATA PHY |
| 0 SATA_PHY_0 | SATA PHY - Tx Edge rate control enables the SATA PHY to meet the edge rate requirements for all SATA variants 0 Fast edge rate 1 Medium edge rate |

36.4.15 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_DATA1)

Address: 20E_0000h base + 4Ch offset = 20E_004Ch

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|------|----|----|----------|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | SION | 0 | | MUX_MODE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD2_DATA1 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD2_DAT1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |

Table continues on the next page...

IOMUXC_SW_MUX_CTL_PAD_SD2_DATA1 field descriptions (continued)

| Field | Description |
|------------|--|
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 6 iomux modes to be used for pad: SD2_DAT1.</p> <p>NOTE: Pad SD2_DAT1 is involved in Daisy Chain.</p> <p>000 ALT0 — Select signal SD2_DATA1. 001 ALT1 — Select signal ECSPI5_SS0. - Configure register IOMUXC_ESCPI5_SS0_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal EIM_CS2_B. 011 ALT3 — Select signal AUD4_TXFS. - Configure register IOMUXC_AUD4_INPUT_TXFS_AMX_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal KEY_COL7. - Configure register IOMUXC_KEY_COL7_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO1_IO14.</p> |

36.4.16 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_DATA2)

Address: 20E_0000h base + 50h offset = 20E_0050h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|------|----|----|----------|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | SION | 0 | | MUX_MODE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD2_DATA2 field descriptions

| Field | Description |
|---------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad SD2_DAT2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_MUX_CTL_PAD_SD2_DATA2 field descriptions (continued)

| Field | Description |
|----------|--|
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 6 iomux modes to be used for pad: SD2_DAT2.</p> <p>NOTE: Pad SD2_DAT2 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal SD2_DATA2. 001 ALT1 — Select signal ECSPI5_SS1. <ul style="list-style-type: none"> - Configure register IOMUXC_ECSPI5_SS1_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal EIM_CS3_B. 011 ALT3 — Select signal AUD4_TXD. <ul style="list-style-type: none"> - Configure register IOMUXC_AUD4_INPUT_DB_AMX_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal KEY_ROW6. <ul style="list-style-type: none"> - Configure register IOMUXC_KEY_ROW6_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO1_IO13. |

36.4.17 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_DATA0)

Address: 20E_0000h base + 54h offset = 20E_0054h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|------|----|----|----------|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | | 0 | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD2_DATA0 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <ul style="list-style-type: none"> 1 ENABLED — Force input path of pad SD2_DAT0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 6 iomux modes to be used for pad: SD2_DAT0.</p> |

Table continues on the next page...

IOMUXC_SW_MUX_CTL_PAD_SD2_DATA0 field descriptions (continued)

| Field | Description |
|-------|---|
| | <p>NOTE: Pad SD2_DATA0 is involved in Daisy Chain.</p> <p>000 ALT0 — Select signal SD2_DATA0. 001 ALT1 — Select signal ECSP15_MISO. - Configure register IOMUXC_ECSP15_MISO_SELECT_INPUT for mode ALT1. 011 ALT3 — Select signal AUD4_RXD. - Configure register IOMUXC_AUD4_INPUT_DA_AMX_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal KEY_ROW7. - Configure register IOMUXC_KEY_ROW7_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO1_IO15. 110 ALT6 — Select signal DCIC2_OUT.</p> |

36.4.18 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TXC)

Address: 20E_0000h base + 58h offset = 20E_0058h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|------|----|----|----------|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | SION | 0 | | MUX_MODE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_TXC field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad RGMII_TXC. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 5 iomux modes to be used for pad: RGMII_TXC.</p> <p>NOTE: Pad RGMII_TXC is involved in Daisy Chain.</p> <p>000 ALT0 — Select signal USB_H2_DATA.</p> |

Table continues on the next page...

IOMUXC_SW_MUX_CTL_PAD_RGMII_TXC field descriptions (continued)

| Field | Description |
|-------|--|
| | <p>001 ALT1 — Select signal RGMII_TXC.</p> <p>010 ALT2 — Select signal SPDIF_EXT_CLK. - Configure register IOMUXC_SPDIF_TX_CLK2_SELECT_INPUT for mode ALT2.</p> <p>101 ALT5 — Select signal GPIO6_IO19.</p> <p>111 ALT7 — Select signal XTALOSC_REF_CLK_24M.</p> |

36.4.19 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TD0)

Address: 20E_0000h base + 5Ch offset = 20E_005Ch

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|------|----|----|----------|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | SION | 0 | | MUX_MODE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_TD0 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad RGMII_TD0.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 3 iomux modes to be used for pad: RGMII_TD0.</p> <p>000 ALT0 — Select signal HSI_TX_READY.</p> <p>001 ALT1 — Select signal RGMII_TD0.</p> <p>101 ALT5 — Select signal GPIO6_IO20.</p> |

36.4.20 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TD1)

Address: 20E_0000h base + 60h offset = 20E_0060h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_TD1 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_TD1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: RGMII_TD1. 000 ALT0 — Select signal HSI_RX_FLAG. 001 ALT1 — Select signal RGMII_TD1. 101 ALT5 — Select signal GPIO6_IO21. |

36.4.21 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TD2)

Address: 20E_0000h base + 64h offset = 20E_0064h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | |
| W | | | | | | | | | | | | | | | MUX_MODE | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_TD2 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_TD2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: RGMII_TD2. 000 ALT0 — Select signal HSI_RX_DATA. 001 ALT1 — Select signal RGMII_TD2. 101 ALT5 — Select signal GPIO6_IO22. |

36.4.22 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TD3)

Address: 20E_0000h base + 68h offset = 20E_0068h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_TD3 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_TD3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: RGMII_TD3. 000 ALT0 — Select signal HSI_RX_WAKE. 001 ALT1 — Select signal RGMII_TD3. 101 ALT5 — Select signal GPIO6_IO23. |

36.4.23 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RX_CTL)

Address: 20E_0000h base + 6Ch offset = 20E_006Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 0 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_RX_CTL field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_RX_CTL. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: RGMII_RX_CTL. NOTE: Pad RGMII_RX_CTL is involved in Daisy Chain. 000 ALT0 — Select signal USB_H3_DATA. 001 ALT1 — Select signal RGMII_RX_CTL. - Configure register IOMUXC_ENET_MAC0_RX_EN_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO6_IO24. |

36.4.24 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RD0)

Address: 20E_0000h base + 70h offset = 20E_0070h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_RD0 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_RD0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: RGMII_RD0. NOTE: Pad RGMII_RD0 is involved in Daisy Chain. 000 ALT0 — Select signal HSI_RX_READY. 001 ALT1 — Select signal RGMII_RD0. - Configure register IOMUXC_ENET_MAC0_RX_DATA0_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO6_IO25. |

36.4.25 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_TX_CTL)

Address: 20E_0000h base + 74h offset = 20E_0074h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_TX_CTL field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_TX_CTL. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: RGMII_TX_CTL. NOTE: Pad RGMII_TX_CTL is involved in Daisy Chain. 000 ALT0 — Select signal USB_H2_STROBE. 001 ALT1 — Select signal RGMII_TX_CTL. 101 ALT5 — Select signal GPIO6_IO26. 111 ALT7 — Select signal ENET_REF_CLK. - Configure register IOMUXC_ENET_REF_CLK_SELECT_INPUT for mode ALT7. |

36.4.26 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RD1)

Address: 20E_0000h base + 78h offset = 20E_0078h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_RD1 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_RD1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: RGMII_RD1. NOTE: Pad RGMII_RD1 is involved in Daisy Chain. 000 ALT0 — Select signal HSI_TX_FLAG. 001 ALT1 — Select signal RGMII_RD1. - Configure register IOMUXC_ENET_MAC0_RX_DATA1_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO6_IO27. |

36.4.27 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RD2)

Address: 20E_0000h base + 7Ch offset = 20E_007Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 0 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_RD2 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_RD2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: RGMII_RD2. NOTE: Pad RGMII_RD2 is involved in Daisy Chain. 000 ALT0 — Select signal HSI_TX_DATA. 001 ALT1 — Select signal RGMII_RD2. - Configure register IOMUXC_ENET_MAC0_RX_DATA2_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO6_IO28. |

36.4.28 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RD3)

Address: 20E_0000h base + 80h offset = 20E_0080h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_RD3 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_RD3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: RGMII_RD3. NOTE: Pad RGMII_RD3 is involved in Daisy Chain. 000 ALT0 — Select signal HSI_TX_WAKE. 001 ALT1 — Select signal RGMII_RD3. - Configure register IOMUXC_ENET_MAC0_RX_DATA3_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO6_IO29. |

36.4.29 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_RGMII_RXC)

Address: 20E_0000h base + 84h offset = 20E_0084h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | |
| W | | | | | | | | | | | | | | | MUX_MODE | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_RGMII_RXC field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad RGMII_RXC. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: RGMII_RXC. NOTE: Pad RGMII_RXC is involved in Daisy Chain. 000 ALT0 — Select signal USB_H3_STROBE. 001 ALT1 — Select signal RGMII_RXC. - Configure register IOMUXC_ENET_MAC0_RX_CLK_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO6_IO30. |

36.4.30 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR25)

Address: 20E_0000h base + 88h offset = 20E_0088h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR25 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A25. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_A25. NOTE: Pad EIM_A25 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR25. 001 ALT1 — Select signal ECSPI4_SS1. 010 ALT2 — Select signal ECSPI2_RDY. 011 ALT3 — Select signal IPU1_DI1_PIN12. 100 ALT4 — Select signal IPU1_DIO_D1_CS. 101 ALT5 — Select signal GPIO5_IO02. 110 ALT6 — Select signal HDMI_TX_CEC_LINE. - Configure register IOMUXC_HDMI_ICECIN_SELECT_INPUT for mode ALT6. |

36.4.31 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_EB2_B)

Address: 20E_0000h base + 8Ch offset = 20E_008Ch

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | 0 | | | |
| W | | | | | | | | | | | | | | 0 | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_EB2_B field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_EB2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_EB2. NOTE: Pad EIM_EB2 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_EB2_B. 001 ALT1 — Select signal ECSPI1_SS0. - Configure register IOMUXC_ECSP1_SS0_SELECT_INPUT for mode ALT1. 011 ALT3 — Select signal IPU2_CSI1_DATA19. - Configure register IOMUXC_IPU2_SENS1_DATA19_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal HDMI_TX_DDC_SCL. - Configure register IOMUXC_HDMI_I2C_CLKIN_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO2_IO30. 110 ALT6 — Select signal I2C2_SCL. - Configure register IOMUXC_I2C2_SCL_IN_SELECT_INPUT for mode ALT6. 111 ALT7 — Select signal SRC_BOOT_CFG30. |

36.4.32 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA16)

Address: 20E_0000h base + 90h offset = 20E_0090h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA16 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad EIM_D16.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: EIM_D16.</p> <p>NOTE: Pad EIM_D16 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal EIM_DATA16. 001 ALT1 — Select signal ECSPI1_SCLK.<ul style="list-style-type: none"> - Configure register IOMUXC_ECSP1_CSPI_CLK_IN_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal IPU1_DI0_PIN05. 011 ALT3 — Select signal IPU2_CSI1_DATA18.<ul style="list-style-type: none"> - Configure register IOMUXC_IPU2_SENSE1_DATA18_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal HDMI_TX_DDC_SDA.<ul style="list-style-type: none"> - Configure register IOMUXC_HDMI_I2C_DATAIN_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO16. 110 ALT6 — Select signal I2C2_SDA.<ul style="list-style-type: none"> - Configure register IOMUXC_I2C2_SDA_IN_SELECT_INPUT for mode ALT6. |

36.4.33 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA17)

Address: 20E_0000h base + 94h offset = 20E_0094h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA17 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_D17. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_D17. NOTE: Pad EIM_D17 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_DATA17. 001 ALT1 — Select signal ECSPI1_MISO. - Configure register IOMUXC_ECSP1_MISO_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal IPU1_DI0_PIN06. 011 ALT3 — Select signal IPU2_CSI1_PIXCLK. - Configure register IOMUXC_IPU2_SENS1_PIX_CLK_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal DCIC1_OUT. 101 ALT5 — Select signal GPIO3_IO17. 110 ALT6 — Select signal I2C3_SCL. - Configure register IOMUXC_I2C3_SCL_IN_SELECT_INPUT for mode ALT6. |

36.4.34 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA18)

Address: 20E_0000h base + 98h offset = 20E_0098h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA18 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad EIM_D18.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: EIM_D18.</p> <p>NOTE: Pad EIM_D18 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal EIM_DATA18. 001 ALT1 — Select signal ECSPI1_MOSI. <ul style="list-style-type: none"> - Configure register IOMUXC_ECSP1_MOSI_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal IPU1_DI0_PIN07. 011 ALT3 — Select signal IPU2_CSI1_DATA17. <ul style="list-style-type: none"> - Configure register IOMUXC_IPU2_SENS1_DATA17_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal IPU1_DI1_D0_CS. 101 ALT5 — Select signal GPIO3_IO18. 110 ALT6 — Select signal I2C3_SDA. <ul style="list-style-type: none"> - Configure register IOMUXC_I2C3_SDA_IN_SELECT_INPUT for mode ALT6. |

36.4.35 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA19)

Address: 20E_0000h base + 9Ch offset = 20E_009Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 0 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA19 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_D19. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_D19. NOTE: Pad EIM_D19 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_DATA19. 001 ALT1 — Select signal ECSPI1_SS1. - Configure register IOMUXC_ECSPI1_SS1_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal IPU1_DI0_PIN08. 011 ALT3 — Select signal IPU2_CSI1_DATA16. - Configure register IOMUXC_IPU2_SENS1_DATA16_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal UART1_CTS_B. - Configure register IOMUXC_UART1_UART_RTS_B_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO19. 110 ALT6 — Select signal EPIT1_OUT. |

36.4.36 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA20)

Address: 20E_0000h base + A0h offset = 20E_00A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA20 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_D20. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_D20. NOTE: Pad EIM_D20 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_DATA20. 001 ALT1 — Select signal ECSPI4_SS0. - Configure register IOMUXC_ECSPi4_SS0_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal IPU1_DI0_PIN16. 011 ALT3 — Select signal IPU2_CSI1_DATA15. - Configure register IOMUXC_IPU2_SENS1_DATA15_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal UART1_RTS_B. - Configure register IOMUXC_UART1_UART_RTS_B_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO20. 110 ALT6 — Select signal EPIT2_OUT. |

36.4.37 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA21)

Address: 20E_0000h base + A4h offset = 20E_00A4h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | 0 | | | |
| W | | | | | | | | | | | | | | 0 | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA21 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad EIM_D21.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 8 iomux modes to be used for pad: EIM_D21.</p> <p>NOTE: Pad EIM_D21 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal EIM_DATA21. 001 ALT1 — Select signal ECSPI4_SCLK. 010 ALT2 — Select signal IPU1_DI0_PIN17. 011 ALT3 — Select signal IPU2_CSI1_DATA11. <ul style="list-style-type: none"> - Configure register IOMUXC_IPU2_SENS1_DATA11_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal USB_OTG_OC. <ul style="list-style-type: none"> - Configure register IOMUXC_USB_OTG_OC_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO21. 110 ALT6 — Select signal I2C1_SCL. <ul style="list-style-type: none"> - Configure register IOMUXC_I2C1_SCL_IN_SELECT_INPUT for mode ALT6. 111 ALT7 — Select signal SPDIF_IN. <ul style="list-style-type: none"> - Configure register IOMUXC_SPDIF_SPDIF_IN1_SELECT_INPUT for mode ALT7. |

36.4.38 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA22)

Address: 20E_0000h base + A8h offset = 20E_00A8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA22 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_D22. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_D22. NOTE: Pad EIM_D22 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_DATA22. 001 ALT1 — Select signal ECSPI4_MISO. 010 ALT2 — Select signal IPU1_DI0_PIN01. 011 ALT3 — Select signal IPU2_CS1_DATA10. - Configure register IOMUXC_IPU2_SENS1_DATA10_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal USB_OTG_PWR. 101 ALT5 — Select signal GPIO3_IO22. 110 ALT6 — Select signal SPDIF_OUT. |

36.4.39 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA23)

Address: 20E_0000h base + ACh offset = 20E_00ACh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA23 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_D23. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 8 iomux modes to be used for pad: EIM_D23. NOTE: Pad EIM_D23 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_DATA23. 001 ALT1 — Select signal IPU1_DI0_D0_CS. 010 ALT2 — Select signal UART3_CTS_B. - Configure register IOMUXC_UART3_UART_RTS_B_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal UART1_DCD_B. 100 ALT4 — Select signal IPU2_CSI1_DATA_EN. - Configure register IOMUXC_IPU2_SENSE1_DATA_EN_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO23. 110 ALT6 — Select signal IPU1_DI1_PIN02. 111 ALT7 — Select signal IPU1_DI1_PIN14. |

36.4.40 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_EB3_B)

Address: 20E_0000h base + B0h offset = 20E_00B0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_EB3_B field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_EB3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 8 iomux modes to be used for pad: EIM_EB3. NOTE: Pad EIM_EB3 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_EB3_B. 001 ALT1 — Select signal ECSPI4_RDY. 010 ALT2 — Select signal UART3 RTS_B. - Configure register IOMUXC_UART3_UART_RTS_B_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal UART1 RI_B. 100 ALT4 — Select signal IPU2_CSI1_HSYNC. - Configure register IOMUXC_IPU2_SENS1_HSYNC_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO2_IO31. 110 ALT6 — Select signal IPU1_DI1_PIN03. 111 ALT7 — Select signal SRC_BOOT_CFG31. |

36.4.41 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA24)

Address: 20E_0000h base + B4h offset = 20E_00B4h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | 0 | | | |
| W | | | | | | | | | | | | | | 0 | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA24 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_D24. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 8 iomux modes to be used for pad: EIM_D24. NOTE: Pad EIM_D24 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_DATA24. 001 ALT1 — Select signal ECSPI4_SS2. 010 ALT2 — Select signal UART3_TX_DATA. - Configure register IOMUXC_UART3_UART_RX_DATA_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal ECSPI1_SS2. - Configure register IOMUXC_ECSP1_SS2_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal ECSPI2_SS2. 101 ALT5 — Select signal GPIO3_IO24. 110 ALT6 — Select signal AUD5_RXFS. - Configure register IOMUXC_AUD5_INPUT_RXFS_AMX_SELECT_INPUT for mode ALT6. 111 ALT7 — Select signal UART1_DTR_B. |

36.4.42 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA25)

Address: 20E_0000h base + B8h offset = 20E_00B8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA25 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad EIM_D25.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 8 iomux modes to be used for pad: EIM_D25.</p> <p>NOTE: Pad EIM_D25 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal EIM_DATA25. 001 ALT1 — Select signal ECSPI4_SS3. 010 ALT2 — Select signal UART3_RX_DATA. <ul style="list-style-type: none"> - Configure register IOMUXC_UART3_UART_RX_DATA_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal ECSPI1_SS3. <ul style="list-style-type: none"> - Configure register IOMUXC_ECSP1_SS3_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal ECSPI2_SS3. 101 ALT5 — Select signal GPIO3_IO25. 110 ALT6 — Select signal AUD5_RXC. <ul style="list-style-type: none"> - Configure register IOMUXC_AUD5_INPUT_RXCLK_AMX_SELECT_INPUT for mode ALT6. 111 ALT7 — Select signal UART1_DSR_B. |

36.4.43 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA26)

Address: 20E_0000h base + BCh offset = 20E_00BCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA26 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad EIM_D26.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 8 iomux modes to be used for pad: EIM_D26.</p> <p>NOTE: Pad EIM_D26 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal EIM_DATA26. 001 ALT1 — Select signal IPU1_DI1_PIN11. 010 ALT2 — Select signal IPU1_CSI0_DATA01. 011 ALT3 — Select signal IPU2_CSI1_DATA14. <ul style="list-style-type: none"> - Configure register IOMUXC_IPU2_SENS1_DATA14_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal UART2_TX_DATA. <ul style="list-style-type: none"> - Configure register IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO26. 110 ALT6 — Select signal IPU1_SISG2. 111 ALT7 — Select signal IPU1_DISP1_DATA22. |

36.4.44 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA27)

Address: 20E_0000h base + C0h offset = 20E_00C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA27 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad EIM_D27.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 8 iomux modes to be used for pad: EIM_D27.</p> <p>NOTE: Pad EIM_D27 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal EIM_DATA27. 001 ALT1 — Select signal IPU1_DI1_PIN13. 010 ALT2 — Select signal IPU1_CSI0_DATA00. 011 ALT3 — Select signal IPU2_CSI1_DATA13. <ul style="list-style-type: none"> - Configure register IOMUXC_IPU2_SENS1_DATA13_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal UART2_RX_DATA. <ul style="list-style-type: none"> - Configure register IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO27. 110 ALT6 — Select signal IPU1_SISG3. 111 ALT7 — Select signal IPU1_DISP1_DATA23. |

36.4.45 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA28)

Address: 20E_0000h base + C4h offset = 20E_00C4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA28 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_D28. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 8 iomux modes to be used for pad: EIM_D28. NOTE: Pad EIM_D28 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_DATA28. 001 ALT1 — Select signal I2C1_SDA. - Configure register IOMUXC_I2C1_SDA_IN_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal ECSPI4_MOSI. 011 ALT3 — Select signal IPU2_CSI1_DATA12. - Configure register IOMUXC_IPU2_SENS1_DATA12_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal UART2_CTS_B. - Configure register IOMUXC_UART2_UART_RTS_B_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO28. 110 ALT6 — Select signal IPU1_EXT_TRIG. 111 ALT7 — Select signal IPU1_DIO_PIN13. |

36.4.46 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA29)

Address: 20E_0000h base + C8h offset = 20E_00C8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA29 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad EIM_D29.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: EIM_D29.</p> <p>NOTE: Pad EIM_D29 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal EIM_DATA29. 001 ALT1 — Select signal IPU1_DI1_PIN15. 010 ALT2 — Select signal ECSPI4_SS0. <ul style="list-style-type: none"> - Configure register IOMUXC_ECSPI4_SS0_SELECT_INPUT for mode ALT2. 100 ALT4 — Select signal UART2_RTS_B. <ul style="list-style-type: none"> - Configure register IOMUXC_UART2_UART_RTS_B_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO29. 110 ALT6 — Select signal IPU2_CSI1_VSYNC. <ul style="list-style-type: none"> - Configure register IOMUXC_IPU2_SENS1_VSYNC_SELECT_INPUT for mode ALT6. 111 ALT7 — Select signal IPU1_DI0_PIN14. |

36.4.47 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA30)

Address: 20E_0000h base + CCh offset = 20E_00CCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA30 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_D30. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_D30. NOTE: Pad EIM_D30 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_DATA30. 001 ALT1 — Select signal IPU1_DISP1_DATA21. 010 ALT2 — Select signal IPU1_DI0_PIN11. 011 ALT3 — Select signal IPU1_CSI0_DATA03. 100 ALT4 — Select signal UART3_CTS_B. - Configure register IOMUXC_UART3_UART_RTS_B_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO30. 110 ALT6 — Select signal USB_H1_OC. - Configure register IOMUXC_USB_H1_OC_SELECT_INPUT for mode ALT6. |

36.4.48 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_DATA31)

Address: 20E_0000h base + D0h offset = 20E_00D0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_EIM_DATA31 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_D31. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_D31. NOTE: Pad EIM_D31 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_DATA31. 001 ALT1 — Select signal IPU1_DISP1_DATA20. 010 ALT2 — Select signal IPU1_DI0_PIN12. 011 ALT3 — Select signal IPU1_CSI0_DATA02. 100 ALT4 — Select signal UART3_RTS_B. - Configure register IOMUXC_UART3_UART_RTS_B_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO3_IO31. 110 ALT6 — Select signal USB_H1_PWR. |

36.4.49 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR24)

Address: 20E_0000h base + D4h offset = 20E_00D4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR24 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A24. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_A24. NOTE: Pad EIM_A24 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR24. 001 ALT1 — Select signal IPU1_DISP1_DATA19. 010 ALT2 — Select signal IPU2_CS1_DATA19. - Configure register IOMUXC_IPU2_SENS1_DATA19_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal IPU2_SISG2. 100 ALT4 — Select signal IPU1_SISG2. 101 ALT5 — Select signal GPIO5_IO04. 111 ALT7 — Select signal SRC_BOOT_CFG24. |

36.4.50 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR23)

Address: 20E_0000h base + D8h offset = 20E_00D8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR23 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A23. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_A23. NOTE: Pad EIM_A23 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR23. 001 ALT1 — Select signal IPU1_DISP1_DATA18. 010 ALT2 — Select signal IPU2_CSI1_DATA18. - Configure register IOMUXC_IPU2_SENS1_DATA18_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal IPU2_SISG3. 100 ALT4 — Select signal IPU1_SISG3. 101 ALT5 — Select signal GPIO6_IO06. 111 ALT7 — Select signal SRC_BOOT_CFG23. |

36.4.51 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR22)

Address: 20E_0000h base + DCh offset = 20E_00DCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR22 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A22. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_A22. NOTE: Pad EIM_A22 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR22. 001 ALT1 — Select signal IPU1_DISP1_DATA17. 010 ALT2 — Select signal IPU2_CSI1_DATA17. - Configure register IOMUXC_IPU2_SENS1_DATA17_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO16. 111 ALT7 — Select signal SRC_BOOT_CFG22. |

36.4.52 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR21)

Address: 20E_0000h base + E0h offset = 20E_00E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR21 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A21. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_A21. NOTE: Pad EIM_A21 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR21. 001 ALT1 — Select signal IPU1_DISP1_DATA16. 010 ALT2 — Select signal IPU2_CSI1_DATA16. - Configure register IOMUXC_IPU2_SENS1_DATA16_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO17. 111 ALT7 — Select signal SRC_BOOT_CFG21. |

36.4.53 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR20)

Address: 20E_0000h base + E4h offset = 20E_00E4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR20 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A20. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_A20. NOTE: Pad EIM_A20 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR20. 001 ALT1 — Select signal IPU1_DISP1_DATA15. 010 ALT2 — Select signal IPU2_CSI1_DATA15. - Configure register IOMUXC_IPU2_SENS1_DATA15_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO18. 111 ALT7 — Select signal SRC_BOOT_CFG20. |

36.4.54 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR19)

Address: 20E_0000h base + E8h offset = 20E_00E8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR19 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A19. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_A19. NOTE: Pad EIM_A19 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR19. 001 ALT1 — Select signal IPU1_DISP1_DATA14. 010 ALT2 — Select signal IPU2_CSI1_DATA14. - Configure register IOMUXC_IPU2_SENS1_DATA14_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO19. 111 ALT7 — Select signal SRC_BOOT_CFG19. |

36.4.55 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR18)

Address: 20E_0000h base + ECh offset = 20E_00ECh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR18 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A18. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_A18. NOTE: Pad EIM_A18 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR18. 001 ALT1 — Select signal IPU1_DISP1_DATA13. 010 ALT2 — Select signal IPU2_CSI1_DATA13. - Configure register IOMUXC_IPU2_SENS1_DATA13_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO20. 111 ALT7 — Select signal SRC_BOOT_CFG18. |

36.4.56 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR17)

Address: 20E_0000h base + F0h offset = 20E_00F0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR17 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A17. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_A17. NOTE: Pad EIM_A17 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR17. 001 ALT1 — Select signal IPU1_DISP1_DATA12. 010 ALT2 — Select signal IPU2_CSI1_DATA12. - Configure register IOMUXC_IPU2_SENS1_DATA12_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO21. 111 ALT7 — Select signal SRC_BOOT_CFG17. |

36.4.57 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR16)

Address: 20E_0000h base + F4h offset = 20E_00F4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_ADDR16 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_A16. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_A16. NOTE: Pad EIM_A16 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_ADDR16. 001 ALT1 — Select signal IPU1_DI1_DISP_CLK. 010 ALT2 — Select signal IPU2_CSI1_PIXCLK. - Configure register IOMUXC_IPU2_SENS1_PIX_CLK_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO22. 111 ALT7 — Select signal SRC_BOOT_CFG16. |

36.4.58 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_CS0_B)

Address: 20E_0000h base + F8h offset = 20E_00F8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_CS0_B field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_CS0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: EIM_CS0. NOTE: Pad EIM_CS0 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_CS0_B. 001 ALT1 — Select signal IPU1_DI1_PIN05. 010 ALT2 — Select signal ECSPI2_SCLK. - Configure register IOMUXC_ECSPi2_CSPI_CLK_IN_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO23. |

36.4.59 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_CS1_B)

Address: 20E_0000h base + FCh offset = 20E_00FCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_CS1_B field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_CS1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: EIM_CS1. NOTE: Pad EIM_CS1 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_CS1_B. 001 ALT1 — Select signal IPU1_DI1_PIN06. 010 ALT2 — Select signal ECSPI2_MOSI. - Configure register IOMUXC_ECSPI2_MOSI_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO24. |

36.4.60 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_OE_B)

Address: 20E_0000h base + 100h offset = 20E_0100h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_OE_B field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_OE. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: EIM_OE. NOTE: Pad EIM_OE is involved in Daisy Chain. 000 ALT0 — Select signal EIM_OE_B. 001 ALT1 — Select signal IPU1_DI1_PIN07. 010 ALT2 — Select signal ECSPI2_MISO. - Configure register IOMUXC_ECSPI2_MISO_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO25. |

36.4.61 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_RW)

Address: 20E_0000h base + 104h offset = 20E_0104h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_RW field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_RW. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_RW. NOTE: Pad EIM_RW is involved in Daisy Chain. 000 ALT0 — Select signal EIM_RW. 001 ALT1 — Select signal IPU1_DI1_PIN08. 010 ALT2 — Select signal ECSPI2_SS0. - Configure register IOMUXC_ECSPI2_SS0_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO26. 111 ALT7 — Select signal SRC_BOOT_CFG29. |

36.4.62 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_LBA_B)

Address: 20E_0000h base + 108h offset = 20E_0108h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_LBA_B field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_LBA. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_LBA. NOTE: Pad EIM_LBA is involved in Daisy Chain. 000 ALT0 — Select signal EIM_LBA_B. 001 ALT1 — Select signal IPU1_DI1_PIN17. 010 ALT2 — Select signal ECSPI2_SS1. - Configure register IOMUXC_ECSPI2_SS1_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO27. 111 ALT7 — Select signal SRC_BOOT_CFG26. |

36.4.63 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_EB0_B)

Address: 20E_0000h base + 10Ch offset = 20E_010Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_EB0_B field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_EB0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 6 iomux modes to be used for pad: EIM_EB0. NOTE: Pad EIM_EB0 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_EB0_B. 001 ALT1 — Select signal IPU1_DISP1_DATA11. 010 ALT2 — Select signal IPU2_CSI1_DATA11. - Configure register IOMUXC_IPU2_SENS1_DATA11_SELECT_INPUT for mode ALT2. 100 ALT4 — Select signal CCM_PMIC_READY. - Configure register IOMUXC_CCM_PMIC_READY_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO2_IO28. 111 ALT7 — Select signal SRC_BOOT_CFG27. |

36.4.64 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_EB1_B)

Address: 20E_0000h base + 110h offset = 20E_0110h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_EB1_B field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_EB1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_EB1. NOTE: Pad EIM_EB1 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_EB1_B. 001 ALT1 — Select signal IPU1_DISP1_DATA10. 010 ALT2 — Select signal IPU2_CSI1_DATA10. - Configure register IOMUXC_IPU2_SENS1_DATA10_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO29. 111 ALT7 — Select signal SRC_BOOT_CFG28. |

36.4.65 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD00)

Address: 20E_0000h base + 114h offset = 20E_0114h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD00 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA0. 000 ALT0 — Select signal EIM_AD00. 001 ALT1 — Select signal IPU1_DISP1_DATA09. 010 ALT2 — Select signal IPU2_CSI1_DATA09. 101 ALT5 — Select signal GPIO3_IO00. 111 ALT7 — Select signal SRC_BOOT_CFG00. |

36.4.66 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD01)

Address: 20E_0000h base + 118h offset = 20E_0118h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD01 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA1. 000 ALT0 — Select signal EIM_AD01. 001 ALT1 — Select signal IPU1_DISP1_DATA08. 010 ALT2 — Select signal IPU2_CSI1_DATA08. 101 ALT5 — Select signal GPIO3_IO01. 111 ALT7 — Select signal SRC_BOOT_CFG01. |

36.4.67 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD02)

Address: 20E_0000h base + 11Ch offset = 20E_011Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD02 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA2. 000 ALT0 — Select signal EIM_AD02. 001 ALT1 — Select signal IPU1_DISP1_DATA07. 010 ALT2 — Select signal IPU2_CSI1_DATA07. 101 ALT5 — Select signal GPIO3_IO02. 111 ALT7 — Select signal SRC_BOOT_CFG02. |

36.4.68 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD03)

Address: 20E_0000h base + 120h offset = 20E_0120h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD03 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA3. 000 ALT0 — Select signal EIM_AD03. 001 ALT1 — Select signal IPU1_DISP1_DATA06. 010 ALT2 — Select signal IPU2_CSI1_DATA06. 101 ALT5 — Select signal GPIO3_IO03. 111 ALT7 — Select signal SRC_BOOT_CFG03. |

36.4.69 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD04)

Address: 20E_0000h base + 124h offset = 20E_0124h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 0 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | 0 | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD04 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA4. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA4. 000 ALT0 — Select signal EIM_AD04. 001 ALT1 — Select signal IPU1_DISP1_DATA05. 010 ALT2 — Select signal IPU2_CSI1_DATA05. 101 ALT5 — Select signal GPIO3_IO04. 111 ALT7 — Select signal SRC_BOOT_CFG04. |

36.4.70 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD05)

Address: 20E_0000h base + 128h offset = 20E_0128h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD05 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA5. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA5. 000 ALT0 — Select signal EIM_AD05. 001 ALT1 — Select signal IPU1_DISP1_DATA04. 010 ALT2 — Select signal IPU2_CSI1_DATA04. 101 ALT5 — Select signal GPIO3_IO05. 111 ALT7 — Select signal SRC_BOOT_CFG05. |

36.4.71 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD06)

Address: 20E_0000h base + 12Ch offset = 20E_012Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD06 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA6. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA6. 000 ALT0 — Select signal EIM_AD06. 001 ALT1 — Select signal IPU1_DISP1_DATA03. 010 ALT2 — Select signal IPU2_CSI1_DATA03. 101 ALT5 — Select signal GPIO3_IO06. 111 ALT7 — Select signal SRC_BOOT_CFG06. |

36.4.72 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD07)

Address: 20E_0000h base + 130h offset = 20E_0130h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD07 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA7. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA7. 000 ALT0 — Select signal EIM_AD07. 001 ALT1 — Select signal IPU1_DISP1_DATA02. 010 ALT2 — Select signal IPU2_CSI1_DATA02. 101 ALT5 — Select signal GPIO3_IO07. 111 ALT7 — Select signal SRC_BOOT_CFG07. |

36.4.73 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD08)

Address: 20E_0000h base + 134h offset = 20E_0134h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD08 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA8. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA8. 000 ALT0 — Select signal EIM_AD08. 001 ALT1 — Select signal IPU1_DISP1_DATA01. 010 ALT2 — Select signal IPU2_CSI1_DATA01. 101 ALT5 — Select signal GPIO3_IO08. 111 ALT7 — Select signal SRC_BOOT_CFG08. |

36.4.74 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD09)

Address: 20E_0000h base + 138h offset = 20E_0138h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD09 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA9. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA9. 000 ALT0 — Select signal EIM_AD09. 001 ALT1 — Select signal IPU1_DISP1_DATA00. 010 ALT2 — Select signal IPU2_CSI1_DATA00. 101 ALT5 — Select signal GPIO3_IO09. 111 ALT7 — Select signal SRC_BOOT_CFG09. |

36.4.75 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD10)

Address: 20E_0000h base + 13Ch offset = 20E_013Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD10 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA10. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA10. NOTE: Pad EIM_DA10 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_AD10. 001 ALT1 — Select signal IPU1_DI1_PIN15. 010 ALT2 — Select signal IPU2_CSI1_DATA_EN. - Configure register IOMUXC_IPU2_SENS1_DATA_EN_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO3_IO10. 111 ALT7 — Select signal SRC_BOOT_CFG10. |

36.4.76 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD11)

Address: 20E_0000h base + 140h offset = 20E_0140h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD11 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA11. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA11. NOTE: Pad EIM_DA11 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_AD11. 001 ALT1 — Select signal IPU1_DI1_PIN02. 010 ALT2 — Select signal IPU2_CSI1_HSYNC. - Configure register IOMUXC_IPU2_SENS1_HSYNC_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO3_IO11. 111 ALT7 — Select signal SRC_BOOT_CFG11. |

36.4.77 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD12)

Address: 20E_0000h base + 144h offset = 20E_0144h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD12 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA12. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA12. NOTE: Pad EIM_DA12 is involved in Daisy Chain. 000 ALT0 — Select signal EIM_AD12. 001 ALT1 — Select signal IPU1_DI1_PIN03. 010 ALT2 — Select signal IPU2_CSI1_VSYNC. - Configure register IOMUXC_IPU2_SENSE1_VSYNC_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO3_IO12. 111 ALT7 — Select signal SRC_BOOT_CFG12. |

36.4.78 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD13)

Address: 20E_0000h base + 148h offset = 20E_0148h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD13 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad EIM_DA13.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 4 iomux modes to be used for pad: EIM_DA13.</p> <p>000 ALT0 — Select signal EIM_AD13.</p> <p>001 ALT1 — Select signal IPU1_DI1_D0_CS.</p> <p>101 ALT5 — Select signal GPIO3_IO13.</p> <p>111 ALT7 — Select signal SRC_BOOT_CFG13.</p> |

36.4.79 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD14)

Address: 20E_0000h base + 14Ch offset = 20E_014Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD14 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA14. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: EIM_DA14. 000 ALT0 — Select signal EIM_AD14. 001 ALT1 — Select signal IPU1_DI1_D1_CS. 101 ALT5 — Select signal GPIO3_IO14. 111 ALT7 — Select signal SRC_BOOT_CFG14. |

36.4.80 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_AD15)

Address: 20E_0000h base + 150h offset = 20E_0150h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_AD15 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_DA15. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: EIM_DA15. 000 ALT0 — Select signal EIM_AD15. 001 ALT1 — Select signal IPU1_DI1_PIN01. 010 ALT2 — Select signal IPU1_DI1_PIN04. 101 ALT5 — Select signal GPIO3_IO15. 111 ALT7 — Select signal SRC_BOOT_CFG15. |

36.4.81 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_WAIT_B)

Address: 20E_0000h base + 154h offset = 20E_0154h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_WAIT_B field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad EIM_WAIT. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 4 iomux modes to be used for pad: EIM_WAIT.</p> <p>000 ALT0 — Select signal EIM_WAIT_B. 001 ALT1 — Select signal EIM_DTACK_B. 101 ALT5 — Select signal GPIO5_IO00. 111 ALT7 — Select signal SRC_BOOT_CFG25.</p> |

36.4.82 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_BCLK)

Address: 20E_0000h base + 158h offset = 20E_0158h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_MUX_CTL_PAD_EIM_BCLK field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad EIM_BCLK. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: EIM_BCLK. 000 ALT0 — Select signal EIM_BCLK. 001 ALT1 — Select signal IPU1_DI1_PIN16. 101 ALT5 — Select signal GPIO6_IO31. |

36.4.83 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DI0_DISP_CLK)

Address: 20E_0000h base + 15Ch offset = 20E_015Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DI0_DISP_CLK field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DI0_DISP_CLK. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: DI0_DISP_CLK. 000 ALT0 — Select signal IPU1_DI0_DISP_CLK. 001 ALT1 — Select signal IPU2_DI0_DISP_CLK. 101 ALT5 — Select signal GPIO4_IO16. |

36.4.84 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DI0_PIN15)

Address: 20E_0000h base + 160h offset = 20E_0160h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DI0_PIN15 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DI0_PIN15. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DI0_PIN15. 000 ALT0 — Select signal IPU1_DI0_PIN15. 001 ALT1 — Select signal IPU2_DI0_PIN15. 010 ALT2 — Select signal AUD6_TXC. 101 ALT5 — Select signal GPIO4_IO17. |

36.4.85 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DI0_PIN02)

Address: 20E_0000h base + 164h offset = 20E_0164h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DI0_PIN02 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DI0_PIN2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DI0_PIN2. 000 ALT0 — Select signal IPU1_DI0_PIN02. 001 ALT1 — Select signal IPU2_DI0_PIN02. 010 ALT2 — Select signal AUD6_TXD. 101 ALT5 — Select signal GPIO4_IO18. |

36.4.86 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DI0_PIN03)

Address: 20E_0000h base + 168h offset = 20E_0168h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DI0_PIN03 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DI0_PIN3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DI0_PIN3. 000 ALT0 — Select signal IPU1_DI0_PIN03. 001 ALT1 — Select signal IPU2_DI0_PIN03. 010 ALT2 — Select signal AUD6_TXFS. 101 ALT5 — Select signal GPIO4_IO19. |

36.4.87 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DI0_PIN04)

Address: 20E_0000h base + 16Ch offset = 20E_016Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DI0_PIN04 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DI0_PIN4. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: DI0_PIN4. NOTE: Pad DI0_PIN4 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_DI0_PIN04. 001 ALT1 — Select signal IPU2_DI0_PIN04. 010 ALT2 — Select signal AUD6_RXD. 011 ALT3 — Select signal SD1_WP. - Configure register IOMUXC_USDHC1_WP_ON_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO4_IO20. |

36.4.88 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA00)

Address: 20E_0000h base + 170h offset = 20E_0170h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA00 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad DISP0_DATA0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 4 iomux modes to be used for pad: DISP0_DATA0.</p> <p>000 ALT0 — Select signal IPU1_DISP0_DATA00. 001 ALT1 — Select signal IPU2_DISP0_DATA00. 010 ALT2 — Select signal ECSPI3_SCLK. 101 ALT5 — Select signal GPIO4_IO21.</p> |

36.4.89 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA01)

Address: 20E_0000h base + 174h offset = 20E_0174h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA01 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DISP0_DAT1. 000 ALT0 — Select signal IPU1_DISP0_DATA01. 001 ALT1 — Select signal IPU2_DISP0_DATA01. 010 ALT2 — Select signal ECSPI3_MOSI. 101 ALT5 — Select signal GPIO4_IO22. |

36.4.90 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA02)

Address: 20E_0000h base + 178h offset = 20E_0178h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA02 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DISP0_DAT2. 000 ALT0 — Select signal IPU1_DISP0_DATA02. 001 ALT1 — Select signal IPU2_DISP0_DATA02. 010 ALT2 — Select signal ECSPI3_MISO. 101 ALT5 — Select signal GPIO4_IO23. |

36.4.91 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA03)

Address: 20E_0000h base + 17Ch offset = 20E_017Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA03 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DISP0_DAT3. 000 ALT0 — Select signal IPU1_DISP0_DATA03. 001 ALT1 — Select signal IPU2_DISP0_DATA03. 010 ALT2 — Select signal ECSPI3_SS0. 101 ALT5 — Select signal GPIO4_IO24. |

36.4.92 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA04)

Address: 20E_0000h base + 180h offset = 20E_0180h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA04 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT4. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DISP0_DAT4. 000 ALT0 — Select signal IPU1_DISP0_DATA04. 001 ALT1 — Select signal IPU2_DISP0_DATA04. 010 ALT2 — Select signal ECSPI3_SS1. 101 ALT5 — Select signal GPIO4_IO25. |

36.4.93 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA05)

Address: 20E_0000h base + 184h offset = 20E_0184h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA05 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT5. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: DISP0_DAT5. 000 ALT0 — Select signal IPU1_DISP0_DATA05. 001 ALT1 — Select signal IPU2_DISP0_DATA05. 010 ALT2 — Select signal ECSPI3_SS2. 011 ALT3 — Select signal AUD6_RXFS. 101 ALT5 — Select signal GPIO4_IO26. |

36.4.94 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA06)

Address: 20E_0000h base + 188h offset = 20E_0188h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA06 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT6. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: DISP0_DAT6. 000 ALT0 — Select signal IPU1_DISP0_DATA06. 001 ALT1 — Select signal IPU2_DISP0_DATA06. 010 ALT2 — Select signal ECSPI3_SS3. 011 ALT3 — Select signal AUD6_RXC. 101 ALT5 — Select signal GPIO4_IO27. |

36.4.95 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA07)

Address: 20E_0000h base + 18Ch offset = 20E_018Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA07 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT7. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DISP0_DAT7. 000 ALT0 — Select signal IPU1_DISP0_DATA07. 001 ALT1 — Select signal IPU2_DISP0_DATA07. 010 ALT2 — Select signal ECSPI3_RDY. 101 ALT5 — Select signal GPIO4_IO28. |

36.4.96 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA08)

Address: 20E_0000h base + 190h offset = 20E_0190h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA08 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT8. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: DISP0_DAT8. 000 ALT0 — Select signal IPU1_DISP0_DATA08. 001 ALT1 — Select signal IPU2_DISP0_DATA08. 010 ALT2 — Select signal PWM1_OUT. 011 ALT3 — Select signal WDOG1_B. 101 ALT5 — Select signal GPIO4_IO29. |

36.4.97 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA09)

Address: 20E_0000h base + 194h offset = 20E_0194h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA09 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT9. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: DISP0_DAT9. 000 ALT0 — Select signal IPU1_DISP0_DATA09. 001 ALT1 — Select signal IPU2_DISP0_DATA09. 010 ALT2 — Select signal PWM2_OUT. 011 ALT3 — Select signal WDOG2_B. 101 ALT5 — Select signal GPIO4_IO30. |

36.4.98 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA10)

Address: 20E_0000h base + 198h offset = 20E_0198h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA10 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad DISP0_DAT10.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 3 iomux modes to be used for pad: DISP0_DAT10.</p> <p>000 ALT0 — Select signal IPU1_DISP0_DATA10.</p> <p>001 ALT1 — Select signal IPU2_DISP0_DATA10.</p> <p>101 ALT5 — Select signal GPIO4_IO31.</p> |

36.4.99 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA11)

Address: 20E_0000h base + 19Ch offset = 20E_019Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA11 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad DISP0_DAT11.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 3 iomux modes to be used for pad: DISP0_DAT11.</p> <p>000 ALT0 — Select signal IPU1_DISP0_DATA11.</p> <p>001 ALT1 — Select signal IPU2_DISP0_DATA11.</p> <p>101 ALT5 — Select signal GPIO5_IO05.</p> |

36.4.100 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA12)

Address: 20E_0000h base + 1A0h offset = 20E_01A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA12 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad DISP0_DAT12.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 3 iomux modes to be used for pad: DISP0_DAT12.</p> <p>000 ALT0 — Select signal IPU1_DISP0_DATA12.</p> <p>001 ALT1 — Select signal IPU2_DISP0_DATA12.</p> <p>101 ALT5 — Select signal GPIO5_IO06.</p> |

36.4.101 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA13)

Address: 20E_0000h base + 1A4h offset = 20E_01A4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA13 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT13. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DISP0_DAT13. NOTE: Pad DISP0_DAT13 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_DISP0_DATA13. 001 ALT1 — Select signal IPU2_DISP0_DATA13. 011 ALT3 — Select signal AUD5_RXFS. - Configure register IOMUXC_AUD5_INPUT_RXFS_AMX_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO07. |

36.4.102 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA14)

Address: 20E_0000h base + 1A8h offset = 20E_01A8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|------|----|----|----------|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | SION | | 0 | MUX_MODE | | | | |
| W | | | | | | | | | | | 0 | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA14 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT14. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DISP0_DAT14. NOTE: Pad DISP0_DAT14 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_DISP0_DATA14. 001 ALT1 — Select signal IPU2_DISP0_DATA14. 011 ALT3 — Select signal AUD5_RXC. - Configure register IOMUXC_AUD5_INPUT_RXCLK_AMX_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO08. |

36.4.103 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA15)

Address: 20E_0000h base + 1ACh offset = 20E_01ACh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA15 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT15. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: DISP0_DAT15. NOTE: Pad DISP0_DAT15 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_DISP0_DATA15. 001 ALT1 — Select signal IPU2_DISP0_DATA15. 010 ALT2 — Select signal ECSPI1_SS1. - Configure register IOMUXC_ECSPI1_SS1_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal ECSPI2_SS1. - Configure register IOMUXC_ECSPI2_SS1_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO09. |

36.4.104 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA16)

Address: 20E_0000h base + 1B0h offset = 20E_01B0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA16 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT16. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 6 iomux modes to be used for pad: DISP0_DAT16. NOTE: Pad DISP0_DAT16 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_DISP0_DATA16. 001 ALT1 — Select signal IPU2_DISP0_DATA16. 010 ALT2 — Select signal ECSPI2_MOSI. - Configure register IOMUXC_ECSPI2_MOSI_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD5_TXC. - Configure register IOMUXC_AUD5_INPUT_TXCLK_AMX_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal SDMA_EXT_EVENT0. - Configure register IOMUXC_SDMA_EVENTS14_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO5_IO10. |

36.4.105 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA17)

Address: 20E_0000h base + 1B4h offset = 20E_01B4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA17 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad DISP0_DAT17.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 6 iomux modes to be used for pad: DISP0_DAT17.</p> <p>NOTE: Pad DISP0_DAT17 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal IPU1_DISP0_DATA17. 001 ALT1 — Select signal IPU2_DISP0_DATA17. 010 ALT2 — Select signal ECSPI2_MISO. <ul style="list-style-type: none"> - Configure register IOMUXC_ECSPI2_MISO_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD5_TXD. <ul style="list-style-type: none"> - Configure register IOMUXC_AUD5_INPUT_DB_AMX_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal SDMA_EXT_EVENT1. <ul style="list-style-type: none"> - Configure register IOMUXC_SDMA_EVENTS15_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO5_IO11. |

36.4.106 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA18)

Address: 20E_0000h base + 1B8h offset = 20E_01B8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA18 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad DISP0_DAT18.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: DISP0_DAT18.</p> <p>NOTE: Pad DISP0_DAT18 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal IPU1_DISP0_DATA18. 001 ALT1 — Select signal IPU2_DISP0_DATA18. 010 ALT2 — Select signal ECSPI2_SS0. <ul style="list-style-type: none"> - Configure register IOMUXC_ECSPI2_SS0_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD5_TXFS. <ul style="list-style-type: none"> - Configure register IOMUXC_AUD5_INPUT_TXFS_AMX_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal AUD4_RXFS. <ul style="list-style-type: none"> - Configure register IOMUXC_AUD4_INPUT_RXFS_AMX_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO5_IO12. 111 ALT7 — Select signal EIM_CS2_B. |

36.4.107 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA19)

Address: 20E_0000h base + 1BCh offset = 20E_01BCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA19 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT19. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: DISP0_DAT19. NOTE: Pad DISP0_DAT19 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_DISP0_DATA19. 001 ALT1 — Select signal IPU2_DISP0_DATA19. 010 ALT2 — Select signal ECSPI2_SCLK. - Configure register IOMUXC_ECSPI2_CSPI_CLK_IN_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD5_RXD. - Configure register IOMUXC_AUD5_INPUT_DA_AMX_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal AUD4_RXC. - Configure register IOMUXC_AUD4_INPUT_RXCLK_AMX_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO5_IO13. 111 ALT7 — Select signal EIM_CS3_B. |

36.4.108 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA20)

Address: 20E_0000h base + 1C0h offset = 20E_01C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA20 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad DISP0_DAT20.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 5 iomux modes to be used for pad: DISP0_DAT20.</p> <p>NOTE: Pad DISP0_DAT20 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal IPU1_DISP0_DATA20. 001 ALT1 — Select signal IPU2_DISP0_DATA20. 010 ALT2 — Select signal ECSPI1_SCLK. <ul style="list-style-type: none"> - Configure register IOMUXC_ECSPI1_CSPI_CLK_IN_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD4_TXC. <ul style="list-style-type: none"> - Configure register IOMUXC_AUD4_INPUT_TXCLK_AMX_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO14. |

36.4.109 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA21)

Address: 20E_0000h base + 1C4h offset = 20E_01C4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA21 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT21. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: DISP0_DAT21. NOTE: Pad DISP0_DAT21 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_DISP0_DATA21. 001 ALT1 — Select signal IPU2_DISP0_DATA21. 010 ALT2 — Select signal ECSPI1_MOSI. - Configure register IOMUXC_ECSPI1_MOSI_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD4_TXD. - Configure register IOMUXC_AUD4_INPUT_DB_AMX_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO15. |

36.4.110 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA22)

Address: 20E_0000h base + 1C8h offset = 20E_01C8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA22 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT22. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: DISP0_DAT22. NOTE: Pad DISP0_DAT22 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_DISP0_DATA22. 001 ALT1 — Select signal IPU2_DISP0_DATA22. 010 ALT2 — Select signal ECSPI1_MISO. - Configure register IOMUXC_ECSPI1_MISO_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD4_TXFS. - Configure register IOMUXC_AUD4_INPUT_TXFS_AMX_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO16. |

36.4.111 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA23)

Address: 20E_0000h base + 1CCh offset = 20E_01CCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_DISP0_DATA23 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad DISP0_DAT23. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: DISP0_DAT23. NOTE: Pad DISP0_DAT23 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_DISP0_DATA23. 001 ALT1 — Select signal IPU2_DISP0_DATA23. 010 ALT2 — Select signal ECSPI1_SS0. - Configure register IOMUXC_ECSPI1_SS0_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD4_RXD. - Configure register IOMUXC_AUD4_INPUT_DA_AMX_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO17. |

36.4.112 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_MDIO)

Address: 20E_0000h base + 1D0h offset = 20E_01D0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_ENET_MDIO field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_MDIO. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: ENET_MDIO. NOTE: Pad ENET_MDIO is involved in Daisy Chain. 001 ALT1 — Select signal ENET_MDIO. - Configure register IOMUXC_ENET_MAC0_MDIO_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal ESAI_RX_CLK. - Configure register IOMUXC_ESAI_RX_CLK_SELECT_INPUT for mode ALT2. 100 ALT4 — Select signal ENET_1588_EVENT1_OUT. 101 ALT5 — Select signal GPIO1_IO22. 110 ALT6 — Select signal SPDIF_LOCK. |

36.4.113 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_REF_CLK)

Address: 20E_0000h base + 1D4h offset = 20E_01D4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_ENET_REF_CLK field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_REF_CLK. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: ENET_REF_CLK. NOTE: Pad ENET_REF_CLK is involved in Daisy Chain. 001 ALT1 — Select signal ENET_TX_CLK. 010 ALT2 — Select signal ESAI_RX_FS. - Configure register IOMUXC_ESAI_RX_FS_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO1_IO23. 110 ALT6 — Select signal SPDIF_SR_CLK. |

36.4.114 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_RX_ER)

Address: 20E_0000h base + 1D8h offset = 20E_01D8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

IOMUXC_SW_MUX_CTL_PAD_ENET_RX_ER field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_RX_ER. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 6 iomux modes to be used for pad: ENET_RX_ER. NOTE: Pad ENET_RX_ER is involved in Daisy Chain. 000 ALT0 — Select signal USB_OTG_ID. 001 ALT1 — Select signal ENET_RX_ER. 010 ALT2 — Select signal ESAI_RX_HF_CLK. - Configure register IOMUXC_ESAI_RX_HF_CLK_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal SPDIF_IN. - Configure register IOMUXC_SPDIF_SPDIF_IN1_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal ENET_1588_EVENT2_OUT. 101 ALT5 — Select signal GPIO1_IO24. |

36.4.115 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_CRS_DV)

Address: 20E_0000h base + 1DCh offset = 20E_01DCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_ENET_CRS_DV field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_CRS_DV. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: ENET_CRS_DV. NOTE: Pad ENET_CRS_DV is involved in Daisy Chain. 001 ALT1 — Select signal ENET_RX_EN. - Configure register IOMUXC_ENET_MAC0_RX_EN_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal ESDI_TX_CLK. - Configure register IOMUXC_ESDI_TX_CLK_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal SPDIF_EXT_CLK. - Configure register IOMUXC_SPDIF_TX_CLK2_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO1_IO25. |

36.4.116 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_RX_DATA1)

Address: 20E_0000h base + 1E0h offset = 20E_01E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_ENET_RX_DATA1 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_RXD1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: ENET_RXD1. NOTE: Pad ENET_RXD1 is involved in Daisy Chain. 000 ALT0 — Select signal MLB_SIG. - Configure register IOMUXC_MLB_MLB_SIG_IN_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_RX_DATA1. - Configure register IOMUXC_ENET_MAC0_RX_DATA1_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal ESAI_TX_FS. - Configure register IOMUXC_ESAI_TX_FS_SELECT_INPUT for mode ALT2. 100 ALT4 — Select signal ENET_1588_EVENT3_OUT. 101 ALT5 — Select signal GPIO1_IO26. |

36.4.117 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_RX_DATA0)

Address: 20E_0000h base + 1E4h offset = 20E_01E4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_ENET_RX_DATA0 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_RXD0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: ENET_RXD0. NOTE: Pad ENET_RXD0 is involved in Daisy Chain. 000 ALT0 — Select signal XTALOSC_OSC32K_32K_OUT. 001 ALT1 — Select signal ENET_RX_DATA0. - Configure register IOMUXC_ENET_MAC0_RX_DATA0_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal ESAI_TX_HF_CLK. - Configure register IOMUXC_ESAI_TX_HF_CLK_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal SPDIF_OUT. 101 ALT5 — Select signal GPIO1_IO27. |

36.4.118 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_TX_EN)

Address: 20E_0000h base + 1E8h offset = 20E_01E8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_ENET_TX_EN field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_TX_EN. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: ENET_TX_EN. NOTE: Pad ENET_TX_EN is involved in Daisy Chain. 001 ALT1 — Select signal ENET_TX_EN. 010 ALT2 — Select signal ESAI_RX3_RX2. - Configure register IOMUXC_ESAI_SDO3_SD12_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO1_IO28. |

36.4.119 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_TX_DATA1)

Address: 20E_0000h base + 1ECh offset = 20E_01ECh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | |
| W | | | | | | | | | | | | | | | MUX_MODE | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_ENET_TX_DATA1 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_TXD1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: ENET_TXD1. NOTE: Pad ENET_TXD1 is involved in Daisy Chain. 000 ALT0 — Select signal MLB_CLK. - Configure register IOMUXC_MLB_MLB_CLK_IN_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_TX_DATA1. 010 ALT2 — Select signal ESAI_RX3. - Configure register IOMUXC_ESAI_SDO2_SD13_SELECT_INPUT for mode ALT2. 100 ALT4 — Select signal ENET_1588_EVENT0_IN. 101 ALT5 — Select signal GPIO1_IO29. |

36.4.120 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_TX_DATA0)

Address: 20E_0000h base + 1F0h offset = 20E_01F0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_ENET_TX_DATA0 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_TXD0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: ENET_TXD0. NOTE: Pad ENET_TXD0 is involved in Daisy Chain. 001 ALT1 — Select signal ENET_TX_DATA0. 010 ALT2 — Select signal ESDAI_RX1. - Configure register IOMUXC_ESDAI_SDO4_SD1_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO1_IO30. |

36.4.121 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_ENET_MDC)

Address: 20E_0000h base + 1F4h offset = 20E_01F4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_ENET_MDC field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad ENET_MDC. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: ENET_MDC. NOTE: Pad ENET_MDC is involved in Daisy Chain. 000 ALT0 — Select signal MLB_DATA. - Configure register IOMUXC_MLB_MLB_DATA_IN_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_MDC. 010 ALT2 — Select signal ESAI_TX5_RX0. - Configure register IOMUXC_ESAI_SDO5_SDIO_SELECT_INPUT for mode ALT2. 100 ALT4 — Select signal ENET_1588_EVENT1_IN. 101 ALT5 — Select signal GPIO1_IO31. |

36.4.122 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL0)

Address: 20E_0000h base + 1F8h offset = 20E_01F8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_COL0 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad KEY_COL0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: KEY_COL0. NOTE: Pad KEY_COL0 is involved in Daisy Chain. 000 ALT0 — Select signal ECSPI1_SCLK. - Configure register IOMUXC_ECSPI1_CSPI_CLK_IN_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_RX_DATA3. - Configure register IOMUXC_ENET_MAC0_RX_DATA3_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal AUD5_TXC. - Configure register IOMUXC_AUD5_INPUT_TXCLK_AMX_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_COL0. 100 ALT4 — Select signal UART4_TX_DATA. - Configure register IOMUXC_UART4_UART_RX_DATA_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO4_IO06. 110 ALT6 — Select signal DCIC1_OUT. |

36.4.123 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW0)

Address: 20E_0000h base + 1FCh offset = 20E_01FCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_ROW0 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad KEY_ROW0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: KEY_ROW0. NOTE: Pad KEY_ROW0 is involved in Daisy Chain. 000 ALT0 — Select signal ECSPI1_MOSI. - Configure register IOMUXC_ECSPI1_MOSI_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_TX_DATA3. 010 ALT2 — Select signal AUD5_TXD. - Configure register IOMUXC_AUD5_INPUT_DB_AMX_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_ROW0. 100 ALT4 — Select signal UART4_RX_DATA. - Configure register IOMUXC_UART4_UART_RX_DATA_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO4_IO07. 110 ALT6 — Select signal DCIC2_OUT. |

36.4.124 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL1)

Address: 20E_0000h base + 200h offset = 20E_0200h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_COL1 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad KEY_COL1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: KEY_COL1. NOTE: Pad KEY_COL1 is involved in Daisy Chain. 000 ALT0 — Select signal ECSPI1_MISO. - Configure register IOMUXC_ECSPI1_MISO_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_MDIO. - Configure register IOMUXC_ENET_MAC0_MDIO_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal AUD5_TXFS. - Configure register IOMUXC_AUD5_INPUT_TXFS_AMX_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_COL1. 100 ALT4 — Select signal UART5_TX_DATA. - Configure register IOMUXC_UART5_UART_RX_DATA_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO4_IO08. 110 ALT6 — Select signal SD1_VSELECT. |

36.4.125 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW1)

Address: 20E_0000h base + 204h offset = 20E_0204h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_ROW1 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad KEY_ROW1.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: KEY_ROW1.</p> <p>NOTE: Pad KEY_ROW1 is involved in Daisy Chain.</p> <p>000 ALT0 — Select signal ECSPI1_SS0. - Configure register IOMUXC_ECSPI1_SS0_SELECT_INPUT for mode ALT0.</p> <p>001 ALT1 — Select signal ENET_COL.</p> <p>010 ALT2 — Select signal AUD5_RXD. - Configure register IOMUXC_AUD5_INPUT_DA_AMX_SELECT_INPUT for mode ALT2.</p> <p>011 ALT3 — Select signal KEY_ROW1.</p> <p>100 ALT4 — Select signal UART5_RX_DATA. - Configure register IOMUXC_UART5_UART_RX_DATA_SELECT_INPUT for mode ALT4.</p> <p>101 ALT5 — Select signal GPIO4_IO09.</p> <p>110 ALT6 — Select signal SD2_VSELECT.</p> |

36.4.126 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL2)

Address: 20E_0000h base + 208h offset = 20E_0208h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_COL2 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad KEY_COL2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: KEY_COL2. NOTE: Pad KEY_COL2 is involved in Daisy Chain. 000 ALT0 — Select signal ECSPI1_SS1. - Configure register IOMUXC_ECSPI1_SS1_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_RX_DATA2. - Configure register IOMUXC_ENET_MAC0_RX_DATA2_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal FLEXCAN1_TX. 011 ALT3 — Select signal KEY_COL2. 100 ALT4 — Select signal ENET_MDC. 101 ALT5 — Select signal GPIO4_IO10. 110 ALT6 — Select signal USB_H1_PWR_CTL_WAKE. |

36.4.127 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW2)

Address: 20E_0000h base + 20Ch offset = 20E_020Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | |
| W | | | | | | | | | | | | | | | MUX_MODE | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_ROW2 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad KEY_ROW2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: KEY_ROW2. NOTE: Pad KEY_ROW2 is involved in Daisy Chain. 000 ALT0 — Select signal ECSPI1_SS2. - Configure register IOMUXC_ECSPI1_SS2_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_TX_DATA2. 010 ALT2 — Select signal FLEXCAN1_RX. - Configure register IOMUXC_FLEXCAN1_RX_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_ROW2. 100 ALT4 — Select signal SD2_VSELECT. 101 ALT5 — Select signal GPIO4_IO11. 110 ALT6 — Select signal HDMI_TX_CEC_LINE. - Configure register IOMUXC_HDMI_ICECIN_SELECT_INPUT for mode ALT6. |

36.4.128 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL3)

Address: 20E_0000h base + 210h offset = 20E_0210h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_COL3 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad KEY_COL3.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: KEY_COL3.</p> <p>NOTE: Pad KEY_COL3 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal ECSPI1_SS3. <ul style="list-style-type: none"> - Configure register IOMUXC_ECSPI1_SS3_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_CRS. 010 ALT2 — Select signal HDMI_TX_DDC_SCL. <ul style="list-style-type: none"> - Configure register IOMUXC_HDMI_I2C_CLKIN_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_COL3. 100 ALT4 — Select signal I2C2_SCL. <ul style="list-style-type: none"> - Configure register IOMUXC_I2C2_SCL_IN_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO4_IO12. 110 ALT6 — Select signal SPDIF_IN. <ul style="list-style-type: none"> - Configure register IOMUXC_SPDIF_SPDIF_IN1_SELECT_INPUT for mode ALT6. |

36.4.129 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW3)

Address: 20E_0000h base + 214h offset = 20E_0214h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 0 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_ROW3 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad KEY_ROW3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: KEY_ROW3. NOTE: Pad KEY_ROW3 is involved in Daisy Chain. 000 ALT0 — Select signal XTALOSC_OSC32K_32K_OUT. 001 ALT1 — Select signal ASRC_EXT_CLK. - Configure register IOMUXC_ASRC_ASRCK_CLOCK_6_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal HDMI_TX_DDC_SDA. - Configure register IOMUXC_HDMI_I2C_DATAIN_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_ROW3. 100 ALT4 — Select signal I2C2_SDA. - Configure register IOMUXC_I2C2_SDA_IN_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO4_IO13. 110 ALT6 — Select signal SD1_VSELECT. |

36.4.130 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_COL4)

Address: 20E_0000h base + 218h offset = 20E_0218h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_COL4 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad KEY_COL4. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 6 iomux modes to be used for pad: KEY_COL4. NOTE: Pad KEY_COL4 is involved in Daisy Chain. 000 ALT0 — Select signal FLEXCAN2_TX. 001 ALT1 — Select signal IPU1_SISG4. 010 ALT2 — Select signal USB_OTG_OC. - Configure register IOMUXC_USB_OTG_OC_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_COL4. 100 ALT4 — Select signal UART5_RTS_B. - Configure register IOMUXC_UART5_UART_RTS_B_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO4_IO14. |

36.4.131 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_KEY_ROW4)

Address: 20E_0000h base + 21Ch offset = 20E_021Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_KEY_ROW4 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad KEY_ROW4.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 6 iomux modes to be used for pad: KEY_ROW4.</p> <p>NOTE: Pad KEY_ROW4 is involved in Daisy Chain.</p> <p>000 ALT0 — Select signal FLEXCAN2_RX. - Configure register IOMUXC_FLEXCAN2_RX_SELECT_INPUT for mode ALT0.</p> <p>001 ALT1 — Select signal IPU1_SISG5.</p> <p>010 ALT2 — Select signal USB_OTG_PWR.</p> <p>011 ALT3 — Select signal KEY_ROW4.</p> <p>100 ALT4 — Select signal UART5_CTS_B. - Configure register IOMUXC_UART5_UART_RTS_B_SELECT_INPUT for mode ALT4.</p> <p>101 ALT5 — Select signal GPIO4_IO15.</p> |

36.4.132 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO00)

Address: 20E_0000h base + 220h offset = 20E_0220h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO00 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad GPIO_0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: GPIO_0. NOTE: Pad GPIO_0 is involved in Daisy Chain. 000 ALT0 — Select signal CCM_CLKO1. 010 ALT2 — Select signal KEY_COL5. - Configure register IOMUXC_KEY_COL5_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal ASRC_EXT_CLK. - Configure register IOMUXC_ASRC_ASRCK_CLOCK_6_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal EPIT1_OUT. 101 ALT5 — Select signal GPIO1_IO00. 110 ALT6 — Select signal USB_H1_PWR. 111 ALT7 — Select signal SNVS_VIO_5. |

36.4.133 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO01)

Address: 20E_0000h base + 224h offset = 20E_0224h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO01 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad GPIO_1.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: GPIO_1.</p> <p>NOTE: Pad GPIO_1 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal ESAI_RX_CLK. - Configure register IOMUXC_ESAI_RX_CLK_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal WDOG2_B. 010 ALT2 — Select signal KEY_ROW5. - Configure register IOMUXC_KEY_ROW5_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal USB_OTG_ID. 100 ALT4 — Select signal PWM2_OUT. 101 ALT5 — Select signal GPIO1_IO01. 110 ALT6 — Select signal SD1_CD_B. |

36.4.134 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO09)

Address: 20E_0000h base + 228h offset = 20E_0228h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO09 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad GPIO_9. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: GPIO_9. NOTE: Pad GPIO_9 is involved in Daisy Chain. 000 ALT0 — Select signal ESAI_RX_FS. - Configure register IOMUXC_ESAI_RX_FS_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal WDOG1_B. 010 ALT2 — Select signal KEY_COL6. - Configure register IOMUXC_KEY_COL6_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal CCM_REF_EN_B. 100 ALT4 — Select signal PWM1_OUT. 101 ALT5 — Select signal GPIO1_IO09. 110 ALT6 — Select signal SD1_WP. - Configure register IOMUXC_USDHC1_WP_ON_SELECT_INPUT for mode ALT6. |

36.4.135 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO03)

Address: 20E_0000h base + 22Ch offset = 20E_022Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO03 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad GPIO_3.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: GPIO_3.</p> <p>NOTE: Pad GPIO_3 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal ESAI_RX_HF_CLK. <ul style="list-style-type: none"> - Configure register IOMUXC_ESAI_RX_HF_CLK_SELECT_INPUT for mode ALT0. 010 ALT2 — Select signal I2C3_SCL. <ul style="list-style-type: none"> - Configure register IOMUXC_I2C3_SCL_IN_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal XTALOSC_REF_CLK_24M. 100 ALT4 — Select signal CCM_CLKO2. 101 ALT5 — Select signal GPIO1_IO03. 110 ALT6 — Select signal USB_H1_OC. <ul style="list-style-type: none"> - Configure register IOMUXC_USB_H1_OC_SELECT_INPUT for mode ALT6. 111 ALT7 — Select signal MLB_CLK. <ul style="list-style-type: none"> - Configure register IOMUXC_MLB_MLB_CLK_IN_SELECT_INPUT for mode ALT7. |

36.4.136 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO06)

Address: 20E_0000h base + 230h offset = 20E_0230h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

IOMUXC_SW_MUX_CTL_PAD_GPIO06 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad GPIO_6.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 5 iomux modes to be used for pad: GPIO_6.</p> <p>NOTE: Pad GPIO_6 is involved in Daisy Chain.</p> <p>000 ALT0 — Select signal ESAI_TX_CLK. - Configure register IOMUXC_ESAI_TX_CLK_SELECT_INPUT for mode ALT0.</p> <p>010 ALT2 — Select signal I2C3_SDA. - Configure register IOMUXC_I2C3_SDA_IN_SELECT_INPUT for mode ALT2.</p> <p>101 ALT5 — Select signal GPIO1_IO06.</p> <p>110 ALT6 — Select signal SD2_LCTL.</p> <p>111 ALT7 — Select signal MLB_SIG. - Configure register IOMUXC_MLB_MLB_SIG_IN_SELECT_INPUT for mode ALT7.</p> |

36.4.137 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO02)

Address: 20E_0000h base + 234h offset = 20E_0234h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----------|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | 0 | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION | |
| W | | | | | | | | | | | | | | | | MUX_MODE | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |

IOMUXC_SW_MUX_CTL_PAD_GPIO02 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad GPIO_2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 5 iomux modes to be used for pad: GPIO_2.</p> <p>NOTE: Pad GPIO_2 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal ESAI_TX_FS. <ul style="list-style-type: none"> - Configure register IOMUXC_ESAI_TX_FS_SELECT_INPUT for mode ALT0. 010 ALT2 — Select signal KEY_ROW6. <ul style="list-style-type: none"> - Configure register IOMUXC_KEY_ROW6_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO1_IO02. 110 ALT6 — Select signal SD2_WP. 111 ALT7 — Select signal MLB_DATA. <ul style="list-style-type: none"> - Configure register IOMUXC_MLB_MLB_DATA_IN_SELECT_INPUT for mode ALT7. |

36.4.138 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO04)

Address: 20E_0000h base + 238h offset = 20E_0238h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO04 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad GPIO_4.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 4 iomux modes to be used for pad: GPIO_4.</p> <p>NOTE: Pad GPIO_4 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal ESAI_TX_HF_CLK. <ul style="list-style-type: none"> - Configure register IOMUXC_ESAI_TX_HF_CLK_SELECT_INPUT for mode ALT0. 010 ALT2 — Select signal KEY_COL7. <ul style="list-style-type: none"> - Configure register IOMUXC_KEY_COL7_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO1_IO04. 110 ALT6 — Select signal SD2_CD_B. |

36.4.139 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO05)

Address: 20E_0000h base + 23Ch offset = 20E_023Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO05 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad GPIO_5. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 6 iomux modes to be used for pad: GPIO_5. NOTE: Pad GPIO_5 is involved in Daisy Chain. 000 ALT0 — Select signal ESAI_TX2_RX3. - Configure register IOMUXC_ESAI_SDO2_SD13_SELECT_INPUT for mode ALT0. 010 ALT2 — Select signal KEY_ROW7. - Configure register IOMUXC_KEY_ROW7_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal CCM_CLKO1. 101 ALT5 — Select signal GPIO1_IO05. 110 ALT6 — Select signal I2C3_SCL. - Configure register IOMUXC_I2C3_SCL_IN_SELECT_INPUT for mode ALT6. 111 ALT7 — Select signal ARM_EVENTI. |

36.4.140 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO07)

Address: 20E_0000h base + 240h offset = 20E_0240h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO07 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad GPIO_7.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 8 iomux modes to be used for pad: GPIO_7.</p> <p>NOTE: Pad GPIO_7 is involved in Daisy Chain.</p> <p>000 ALT0 — Select signal ESAI_TX4_RX1. - Configure register IOMUXC_ESAI_SDO4_SD1_SELECT_INPUT for mode ALT0.</p> <p>001 ALT1 — Select signal ECSPI5_RDY.</p> <p>010 ALT2 — Select signal EPIT1_OUT.</p> <p>011 ALT3 — Select signal FLEXCAN1_TX.</p> <p>100 ALT4 — Select signal UART2_TX_DATA. - Configure register IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT for mode ALT4.</p> <p>101 ALT5 — Select signal GPIO1_IO07.</p> <p>110 ALT6 — Select signal SPDIF_LOCK.</p> <p>111 ALT7 — Select signal USB_OTG_HOST_MODE.</p> |

36.4.141 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO08)

Address: 20E_0000h base + 244h offset = 20E_0244h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO08 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad GPIO_8. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 8 iomux modes to be used for pad: GPIO_8. NOTE: Pad GPIO_8 is involved in Daisy Chain. 000 ALT0 — Select signal ESAI_TX5_RX0. - Configure register IOMUXC_ESAI_SDO5_SDIO_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal XTALOSC_REF_CLK_32K. 010 ALT2 — Select signal EPIT2_OUT. 011 ALT3 — Select signal FLEXCAN1_RX. - Configure register IOMUXC_FLEXCAN1_RX_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal UART2_RX_DATA. - Configure register IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO1_IO08. 110 ALT6 — Select signal SPDIF_SR_CLK. 111 ALT7 — Select signal USB_OTG_PWR_CTL_WAKE. |

36.4.142 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO16)

Address: 20E_0000h base + 248h offset = 20E_0248h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO16 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad GPIO_16. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 8 iomux modes to be used for pad: GPIO_16. NOTE: Pad GPIO_16 is involved in Daisy Chain. 000 ALT0 — Select signal ESAI_TX3_RX2. - Configure register IOMUXC_ESAI_SDO3_SD12_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_1588_EVENT2_IN. 010 ALT2 — Select signal ENET_REF_CLK. - Configure register IOMUXC_ENET_REF_CLK_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal SD1_LCTL. 100 ALT4 — Select signal SPDIF_IN. - Configure register IOMUXC_SPDIF_SPDIF_IN1_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO7_IO11. 110 ALT6 — Select signal I2C3_SDA. - Configure register IOMUXC_I2C3_SDA_IN_SELECT_INPUT for mode ALT6. 111 ALT7 — Select signal JTAG_DE_B. |

36.4.143 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO17)

Address: 20E_0000h base + 24Ch offset = 20E_024Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO17 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad GPIO_17.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 6 iomux modes to be used for pad: GPIO_17.</p> <p>NOTE: Pad GPIO_17 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal ESAI_TX0. <ul style="list-style-type: none"> - Configure register IOMUXC_ESAI_SDO0_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_1588_EVENT3_IN. 010 ALT2 — Select signal CCM_PMIC_READY. <ul style="list-style-type: none"> - Configure register IOMUXC_CCM_PMIC_READY_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal SDMA_EXT_EVENT0. <ul style="list-style-type: none"> - Configure register IOMUXC_SDMA_EVENTS14_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal SPDIF_OUT. 101 ALT5 — Select signal GPIO7_IO12. |

36.4.144 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO18)

Address: 20E_0000h base + 250h offset = 20E_0250h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO18 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad GPIO_18.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: GPIO_18.</p> <p>NOTE: Pad GPIO_18 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal ESAI_TX1. <ul style="list-style-type: none"> - Configure register IOMUXC_ESAI_SDO1_SELECT_INPUT for mode ALT0. 001 ALT1 — Select signal ENET_RX_CLK. <ul style="list-style-type: none"> - Configure register IOMUXC_ENET_MAC0_RX_CLK_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal SD3_VSELECT. 011 ALT3 — Select signal SDMA_EXT_EVENT1. <ul style="list-style-type: none"> - Configure register IOMUXC_SDMA_EVENTS15_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal ASRC_EXT_CLK. <ul style="list-style-type: none"> - Configure register IOMUXC_ASRC_ASRCK_CLOCK_6_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO7_IO13. 110 ALT6 — Select signal SNVS_VIO_5_CTL. |

36.4.145 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_GPIO19)

Address: 20E_0000h base + 254h offset = 20E_0254h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_GPIO19 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad GPIO_19.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: GPIO_19.</p> <p>NOTE: Pad GPIO_19 is involved in Daisy Chain.</p> <p>000 ALT0 — Select signal KEY_COL5. - Configure register IOMUXC_KEY_COL5_SELECT_INPUT for mode ALT0.</p> <p>001 ALT1 — Select signal ENET_1588_EVENT0_OUT.</p> <p>010 ALT2 — Select signal SPDIF_OUT.</p> <p>011 ALT3 — Select signal CCM_CLKO1.</p> <p>100 ALT4 — Select signal ECSPI1_RDY.</p> <p>101 ALT5 — Select signal GPIO4_IO05.</p> <p>110 ALT6 — Select signal ENET_TX_ER.</p> |

36.4.146 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_PIXCLK)

Address: 20E_0000h base + 258h offset = 20E_0258h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_PIXCLK field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_PIXCLK. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: CSI0_PIXCLK. 000 ALT0 — Select signal IPU1_CSI0_PIXCLK. 101 ALT5 — Select signal GPIO5_IO18. 111 ALT7 — Select signal ARM_EVENTO. |

36.4.147 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_HSYNC)

Address: 20E_0000h base + 25Ch offset = 20E_025Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_HSYNC field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_MCLK. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: CSI0_MCLK. 000 ALT0 — Select signal IPU1_CSI0_HSYNC. 011 ALT3 — Select signal CCM_CLKO1. 101 ALT5 — Select signal GPIO5_IO19. 111 ALT7 — Select signal ARM_TRACE_CTL. |

36.4.148 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA_EN)

Address: 20E_0000h base + 260h offset = 20E_0260h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA_EN field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DATA_EN. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: CSI0_DATA_EN. 000 ALT0 — Select signal IPU1_CSI0_DATA_EN. 001 ALT1 — Select signal EIM_DATA00. 101 ALT5 — Select signal GPIO5_IO20. 111 ALT7 — Select signal ARM_TRACE_CLK. |

36.4.149 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_VSYNC)

Address: 20E_0000h base + 264h offset = 20E_0264h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_VSYNC field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_VSYNC. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: CSI0_VSYNC. 000 ALT0 — Select signal IPU1_CSI0_VSYNC. 001 ALT1 — Select signal EIM_DATA01. 101 ALT5 — Select signal GPIO5_IO21. 111 ALT7 — Select signal ARM_TRACE00. |

36.4.150 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA04)

Address: 20E_0000h base + 268h offset = 20E_0268h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA04 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT4. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: CSI0_DAT4. NOTE: Pad CSI0_DAT4 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA04. 001 ALT1 — Select signal EIM_DATA02. 010 ALT2 — Select signal ECSPI1_SCLK. - Configure register IOMUXC_ECSPI1_CSPI_CLK_IN_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_COL5. - Configure register IOMUXC_KEY_COL5_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal AUD3_TXC. 101 ALT5 — Select signal GPIO5_IO22. 111 ALT7 — Select signal ARM_TRACE01. |

36.4.151 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA05)

Address: 20E_0000h base + 26Ch offset = 20E_026Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA05 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT5. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: CSI0_DAT5. NOTE: Pad CSI0_DAT5 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA05. 001 ALT1 — Select signal EIM_DATA03. 010 ALT2 — Select signal ECSPI1_MOSI. - Configure register IOMUXC_ECSPI1_MOSI_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_ROW5. - Configure register IOMUXC_KEY_ROW5_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal AUD3_TXD. 101 ALT5 — Select signal GPIO5_IO23. 111 ALT7 — Select signal ARM_TRACE02. |

36.4.152 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA06)

Address: 20E_0000h base + 270h offset = 20E_0270h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 0 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA06 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT6. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: CSI0_DAT6. NOTE: Pad CSI0_DAT6 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA06. 001 ALT1 — Select signal EIM_DATA04. 010 ALT2 — Select signal ECSPI1_MISO. - Configure register IOMUXC_ECSPI1_MISO_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_COL6. - Configure register IOMUXC_KEY_COL6_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal AUD3_TXFS. 101 ALT5 — Select signal GPIO5_IO24. 111 ALT7 — Select signal ARM_TRACE03. |

36.4.153 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA07)

Address: 20E_0000h base + 274h offset = 20E_0274h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA07 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT7. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: CSI0_DAT7. NOTE: Pad CSI0_DAT7 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA07. 001 ALT1 — Select signal EIM_DATA05. 010 ALT2 — Select signal ECSPI1_SS0. - Configure register IOMUXC_ECSPI1_SS0_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_ROW6. - Configure register IOMUXC_KEY_ROW6_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal AUD3_RXD. 101 ALT5 — Select signal GPIO5_IO25. 111 ALT7 — Select signal ARM_TRACE04. |

36.4.154 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA08)

Address: 20E_0000h base + 278h offset = 20E_0278h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | SION |
| W | | | | | | | | | | | | | | | | MUX_MODE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA08 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT8. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: CSI0_DAT8. NOTE: Pad CSI0_DAT8 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA08. 001 ALT1 — Select signal EIM_DATA06. 010 ALT2 — Select signal ECSPI2_SCLK. - Configure register IOMUXC_ECSPI2_CSPI_CLK_IN_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_COL7. - Configure register IOMUXC_KEY_COL7_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal I2C1_SDA. - Configure register IOMUXC_I2C1_SDA_IN_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO5_IO26. 111 ALT7 — Select signal ARM_TRACE05. |

36.4.155 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA09)

Address: 20E_0000h base + 27Ch offset = 20E_027Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA09 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad CSI0_DAT9.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: CSI0_DAT9.</p> <p>NOTE: Pad CSI0_DAT9 is involved in Daisy Chain.</p> <ul style="list-style-type: none"> 000 ALT0 — Select signal IPU1_CSI0_DATA09. 001 ALT1 — Select signal EIM_DATA07. 010 ALT2 — Select signal ECSPI2_MOSI. <ul style="list-style-type: none"> - Configure register IOMUXC_ECSPI2_MOSI_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal KEY_ROW7. <ul style="list-style-type: none"> - Configure register IOMUXC_KEY_ROW7_SELECT_INPUT for mode ALT3. 100 ALT4 — Select signal I2C1_SCL. <ul style="list-style-type: none"> - Configure register IOMUXC_I2C1_SCL_IN_SELECT_INPUT for mode ALT4. 101 ALT5 — Select signal GPIO5_IO27. 111 ALT7 — Select signal ARM_TRACE06. |

36.4.156 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA10)

Address: 20E_0000h base + 280h offset = 20E_0280h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA10 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT10. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 6 iomux modes to be used for pad: CSI0_DAT10. NOTE: Pad CSI0_DAT10 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA10. 001 ALT1 — Select signal AUD3_RXC. 010 ALT2 — Select signal ECSPI2_MISO. - Configure register IOMUXC_ECSPI2_MISO_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal UART1_TX_DATA. - Configure register IOMUXC_UART1_UART_RX_DATA_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO28. 111 ALT7 — Select signal ARM_TRACE07. |

36.4.157 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA11)

Address: 20E_0000h base + 284h offset = 20E_0284h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA11 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT11. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 6 iomux modes to be used for pad: CSI0_DAT11. NOTE: Pad CSI0_DAT11 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA11. 001 ALT1 — Select signal AUD3_RXFS. 010 ALT2 — Select signal ECSPI2_SS0. - Configure register IOMUXC_ECSPI2_SS0_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal UART1_RX_DATA. - Configure register IOMUXC_UART1_UART_RX_DATA_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO29. 111 ALT7 — Select signal ARM_TRACE08. |

36.4.158 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA12)

Address: 20E_0000h base + 288h offset = 20E_0288h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA12 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT12. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: CSI0_DAT12. NOTE: Pad CSI0_DAT12 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA12. 001 ALT1 — Select signal EIM_DATA08. 011 ALT3 — Select signal UART4_TX_DATA. - Configure register IOMUXC_UART4_UART_RX_DATA_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO30. 111 ALT7 — Select signal ARM_TRACE09. |

36.4.159 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA13)

Address: 20E_0000h base + 28Ch offset = 20E_028Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|------|----|----|----------|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | SION | | 0 | MUX_MODE | | | | |
| W | | | | | | | | | | | 0 | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA13 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT13. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: CSI0_DAT13. NOTE: Pad CSI0_DAT13 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA13. 001 ALT1 — Select signal EIM_DATA09. 011 ALT3 — Select signal UART4_RX_DATA. - Configure register IOMUXC_UART4_UART_RX_DATA_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO5_IO31. 111 ALT7 — Select signal ARM_TRACE10. |

36.4.160 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA14)

Address: 20E_0000h base + 290h offset = 20E_0290h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA14 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT14. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: CSI0_DAT14. NOTE: Pad CSI0_DAT14 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA14. 001 ALT1 — Select signal EIM_DATA10. 011 ALT3 — Select signal UART5_TX_DATA. - Configure register IOMUXC_UART5_UART_RX_DATA_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO6_IO00. 111 ALT7 — Select signal ARM_TRACE11. |

36.4.161 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA15)

Address: 20E_0000h base + 294h offset = 20E_0294h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA15 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT15. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: CSI0_DAT15. NOTE: Pad CSI0_DAT15 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA15. 001 ALT1 — Select signal EIM_DATA11. 011 ALT3 — Select signal UART5_RX_DATA. - Configure register IOMUXC_UART5_UART_RX_DATA_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO6_IO01. 111 ALT7 — Select signal ARM_TRACE12. |

36.4.162 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA16)

Address: 20E_0000h base + 298h offset = 20E_0298h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA16 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT16. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: CSI0_DAT16. NOTE: Pad CSI0_DAT16 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA16. 001 ALT1 — Select signal EIM_DATA12. 011 ALT3 — Select signal UART4_RTS_B. - Configure register IOMUXC_UART4_UART_RTS_B_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO6_IO02. 111 ALT7 — Select signal ARM_TRACE13. |

36.4.163 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA17)

Address: 20E_0000h base + 29Ch offset = 20E_029Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA17 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT17. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: CSI0_DAT17. NOTE: Pad CSI0_DAT17 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA17. 001 ALT1 — Select signal EIM_DATA13. 011 ALT3 — Select signal UART4_CTS_B. - Configure register IOMUXC_UART4_UART_RTS_B_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO6_IO03. 111 ALT7 — Select signal ARM_TRACE14. |

36.4.164 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA18)

Address: 20E_0000h base + 2A0h offset = 20E_02A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA18 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT18. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: CSI0_DAT18. NOTE: Pad CSI0_DAT18 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA18. 001 ALT1 — Select signal EIM_DATA14. 011 ALT3 — Select signal UART5_RTS_B. - Configure register IOMUXC_UART5_UART_RTS_B_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO6_IO04. 111 ALT7 — Select signal ARM_TRACE15. |

36.4.165 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA19)

Address: 20E_0000h base + 2A4h offset = 20E_02A4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_CSI0_DATA19 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad CSI0_DAT19. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: CSI0_DAT19. NOTE: Pad CSI0_DAT19 is involved in Daisy Chain. 000 ALT0 — Select signal IPU1_CSI0_DATA19. 001 ALT1 — Select signal EIM_DATA15. 011 ALT3 — Select signal UART5_CTS_B. - Configure register IOMUXC_UART5_UART_RTS_B_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO6_IO05. |

36.4.166 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA7)

Address: 20E_0000h base + 2A8h offset = 20E_02A8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|------|----|----|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | SION | | | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | 0 | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_DATA7 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_DAT7. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD3_DAT7. NOTE: Pad SD3_DAT7 is involved in Daisy Chain. 000 ALT0 — Select signal SD3_DATA7. 001 ALT1 — Select signal UART1_TX_DATA. - Configure register IOMUXC_UART1_UART_RX_DATA_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO6_IO17. |

36.4.167 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA6)

Address: 20E_0000h base + 2ACh offset = 20E_02ACh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|------|----|----|----------|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | SION | | 0 | MUX_MODE | | | | |
| W | | | | | | | | | | | 0 | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_DATA6 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_DAT6. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD3_DAT6. NOTE: Pad SD3_DAT6 is involved in Daisy Chain. 000 ALT0 — Select signal SD3_DATA6. 001 ALT1 — Select signal UART1_RX_DATA. - Configure register IOMUXC_UART1_UART_RX_DATA_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO6_IO18. |

36.4.168 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA5)

Address: 20E_0000h base + 2B0h offset = 20E_02B0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|------|----|----|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | SION | | | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | 0 | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_DATA5 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_DAT5. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD3_DAT5. NOTE: Pad SD3_DAT5 is involved in Daisy Chain. 000 ALT0 — Select signal SD3_DATA5. 001 ALT1 — Select signal UART2_TX_DATA. - Configure register IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO7_IO00. |

36.4.169 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA4)

Address: 20E_0000h base + 2B4h offset = 20E_02B4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|------|----|----|----------|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | SION | | 0 | MUX_MODE | | | | |
| W | | | | | | | | | | | 0 | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_DATA4 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_DATA4. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD3_DATA4. NOTE: Pad SD3_DATA4 is involved in Daisy Chain. 000 ALT0 — Select signal SD3_DATA4. 001 ALT1 — Select signal UART2_RX_DATA. - Configure register IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO7_IO01. |

36.4.170 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_CMD)

Address: 20E_0000h base + 2B8h offset = 20E_02B8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_CMD field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_CMD. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: SD3_CMD. NOTE: Pad SD3_CMD is involved in Daisy Chain. 000 ALT0 — Select signal SD3_CMD. 001 ALT1 — Select signal UART2_CTS_B. - Configure register IOMUXC_UART2_UART_RTS_B_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal FLEXCAN1_TX. 101 ALT5 — Select signal GPIO7_IO02. |

36.4.171 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_CLK)

Address: 20E_0000h base + 2BCh offset = 20E_02BCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_CLK field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_CLK. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: SD3_CLK. NOTE: Pad SD3_CLK is involved in Daisy Chain. 000 ALT0 — Select signal SD3_CLK. 001 ALT1 — Select signal UART2 RTS_B. - Configure register IOMUXC_UART2_UART_RTS_B_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal FLEXCAN1_RX. - Configure register IOMUXC_FLEXCAN1_RX_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO7_IO03. |

36.4.172 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA0)

Address: 20E_0000h base + 2C0h offset = 20E_02C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_DATA0 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_DAT0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: SD3_DAT0. NOTE: Pad SD3_DAT0 is involved in Daisy Chain. 000 ALT0 — Select signal SD3_DATA0. 001 ALT1 — Select signal UART1_CTS_B. - Configure register IOMUXC_UART1_UART_RTS_B_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal FLEXCAN2_TX. 101 ALT5 — Select signal GPIO7_IO4. |

36.4.173 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA1)

Address: 20E_0000h base + 2C4h offset = 20E_02C4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_DATA1 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_DAT1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: SD3_DAT1. NOTE: Pad SD3_DAT1 is involved in Daisy Chain. 000 ALT0 — Select signal SD3_DATA1. 001 ALT1 — Select signal UART1_RTS_B. - Configure register IOMUXC_UART1_UART_RTS_B_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal FLEXCAN2_RX. - Configure register IOMUXC_FLEXCAN2_RX_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO7_IO05. |

36.4.174 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA2)

Address: 20E_0000h base + 2C8h offset = 20E_02C8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_DATA2 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_DAT2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 2 iomux modes to be used for pad: SD3_DAT2. 000 ALT0 — Select signal SD3_DATA2. 101 ALT5 — Select signal GPIO7_IO06. |

36.4.175 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_DATA3)

Address: 20E_0000h base + 2CCh offset = 20E_02CCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_DATA3 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_DAT3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD3_DAT3. NOTE: Pad SD3_DAT3 is involved in Daisy Chain. 000 ALT0 — Select signal SD3_DATA3. 001 ALT1 — Select signal UART3_CTS_B. - Configure register IOMUXC_UART3_UART_RTS_B_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO7_IO07. |

36.4.176 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD3_RESET)

Address: 20E_0000h base + 2D0h offset = 20E_02D0h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | 0 | | | |
| W | | | | | | | | | | | | | | 0 | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD3_RESET field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD3_RST. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |

Table continues on the next page...

IOMUXC_SW_MUX_CTL_PAD_SD3_RESET field descriptions (continued)

| Field | Description |
|------------|--|
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD3_RST. NOTE: Pad SD3_RST is involved in Daisy Chain. 000 ALT0 — Select signal SD3_RESET. 001 ALT1 — Select signal UART3_RTS_B. - Configure register IOMUXC_UART3_UART_RTS_B_SELECT_INPUT for mode ALT1. 101 ALT5 — Select signal GPIO7_IO08. |

36.4.177 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CLE)

Address: 20E_0000h base + 2D4h offset = 20E_02D4h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|------|----|----|----------|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_CLE field descriptions

| Field | Description |
|---------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_CLE. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: NANDF_CLE. 000 ALT0 — Select signal NAND_CLE. 001 ALT1 — Select signal IPU2_SISG4. 101 ALT5 — Select signal GPIO6_IO07. |

36.4.178 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_ALE)

Address: 20E_0000h base + 2D8h offset = 20E_02D8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_ALE field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_ALE. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: NANDF_ALE. 000 ALT0 — Select signal NAND_ALE. 001 ALT1 — Select signal SD4_RESET. 101 ALT5 — Select signal GPIO6_IO08. |

36.4.179 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_WP_B)

Address: 20E_0000h base + 2DCh offset = 20E_02DCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_WP_B field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_WP_B. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: NANDF_WP_B. 000 ALT0 — Select signal NAND_WP_B. 001 ALT1 — Select signal IPU2_SISG5. 101 ALT5 — Select signal GPIO6_IO09. |

36.4.180 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_READY_B)

Address: 20E_0000h base + 2E0h offset = 20E_02E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_READY_B field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_RB0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: NANDF_RB0. 000 ALT0 — Select signal NAND_READY_B. 001 ALT1 — Select signal IPU2_DI0_PIN01. 101 ALT5 — Select signal GPIO6_IO10. |

36.4.181 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CS0_B)

Address: 20E_0000h base + 2E4h offset = 20E_02E4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | |
| W | | | | | | | | | | | | | | | MUX_MODE | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_CS0_B field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_CS0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 2 iomux modes to be used for pad: NANDF_CS0. 000 ALT0 — Select signal NAND_CE0_B. 101 ALT5 — Select signal GPIO6_IO11. |

36.4.182 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CS1_B)

Address: 20E_0000h base + 2E8h offset = 20E_02E8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | |
| W | | | | | | | | | | | | | | | MUX_MODE | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_CS1_B field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_CS1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: NANDF_CS1. 000 ALT0 — Select signal NAND_CE1_B. 001 ALT1 — Select signal SD4_VSELECT. 010 ALT2 — Select signal SD3_VSELECT. 101 ALT5 — Select signal GPIO6_IO14. |

36.4.183 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CS2_B)

Address: 20E_0000h base + 2ECh offset = 20E_02ECh

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|------|----|----|----------|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | SION | 0 | | MUX_MODE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_CS2_B field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_CS2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_MUX_CTL_PAD_NAND_CS2_B field descriptions (continued)

| Field | Description |
|----------|--|
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 7 iomux modes to be used for pad: NANDF_CS2.</p> <p>NOTE: Pad NANDF_CS2 is involved in Daisy Chain.</p> <p>000 ALT0 — Select signal NAND_CE2_B. 001 ALT1 — Select signal IPU1_SISG0. 010 ALT2 — Select signal ESAI_TX0. - Configure register IOMUXC_ESAI_SDO0_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal EIM_CRE. 100 ALT4 — Select signal CCM_CLKO2. 101 ALT5 — Select signal GPIO6_IO15. 110 ALT6 — Select signal IPU2_SISG0.</p> |

36.4.184 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_CS3_B)

Address: 20E_0000h base + 2F0h offset = 20E_02F0h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|------|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | SION | 0 | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_CS3_B field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad NANDF_CS3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 6 iomux modes to be used for pad: NANDF_CS3.</p> <p>NOTE: Pad NANDF_CS3 is involved in Daisy Chain.</p> |

Table continues on the next page...

IOMUXC_SW_MUX_CTL_PAD_NAND_CS3_B field descriptions (continued)

| Field | Description |
|-------|---|
| | 000 ALT0 — Select signal NAND_CE3_B. 001 ALT1 — Select signal IPU1_SISG1. 010 ALT2 — Select signal ESAI_TX1. - Configure register IOMUXC_ESAI_SDO1_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal EIM_ADDR26. 101 ALT5 — Select signal GPIO6_IO16. 110 ALT6 — Select signal IPU2_SISG1. |

36.4.185 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_CMD)

Address: 20E_0000h base + 2F4h offset = 20E_02F4h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|------|----|----|----------|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | 0 | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_CMD field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_CMD. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: SD4_CMD. NOTE: Pad SD4_CMD is involved in Daisy Chain. 000 ALT0 — Select signal SD4_CMD. 001 ALT1 — Select signal NAND_RE_B. 010 ALT2 — Select signal UART3_TX_DATA. - Configure register IOMUXC_UART3_UART_RX_DATA_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO7_IO09. |

36.4.186 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_CLK)

Address: 20E_0000h base + 2F8h offset = 20E_02F8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_CLK field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_CLK. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: SD4_CLK. NOTE: Pad SD4_CLK is involved in Daisy Chain. 000 ALT0 — Select signal SD4_CLK. 001 ALT1 — Select signal NAND_WE_B. 010 ALT2 — Select signal UART3_RX_DATA. - Configure register IOMUXC_UART3_UART_RX_DATA_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO7_IO10. |

36.4.187 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA00)

Address: 20E_0000h base + 2FCh offset = 20E_02FCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_DATA00 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_D0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: NANDF_D0. 000 ALT0 — Select signal NAND_DATA00. 001 ALT1 — Select signal SD1_DATA4. 101 ALT5 — Select signal GPIO2_IO00. |

36.4.188 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA01)

Address: 20E_0000h base + 300h offset = 20E_0300h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_DATA01 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad NANDF_D1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 3 iomux modes to be used for pad: NANDF_D1.</p> <p>000 ALT0 — Select signal NAND_DATA01. 001 ALT1 — Select signal SD1_DATA5. 101 ALT5 — Select signal GPIO2_IO01.</p> |

36.4.189 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA02)

Address: 20E_0000h base + 304h offset = 20E_0304h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_DATA02 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_D2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: NANDF_D2. 000 ALT0 — Select signal NAND_DATA02. 001 ALT1 — Select signal SD1_DATA6. 101 ALT5 — Select signal GPIO2_IO02. |

36.4.190 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA03)

Address: 20E_0000h base + 308h offset = 20E_0308h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_DATA03 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad NANDF_D3.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 3 iomux modes to be used for pad: NANDF_D3.</p> <p>000 ALT0 — Select signal NAND_DATA03. 001 ALT1 — Select signal SD1_DATA7. 101 ALT5 — Select signal GPIO2_IO03.</p> |

36.4.191 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA04)

Address: 20E_0000h base + 30Ch offset = 20E_030Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_DATA04 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_D4. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: NANDF_D4. 000 ALT0 — Select signal NAND_DATA04. 001 ALT1 — Select signal SD2_DATA4. 101 ALT5 — Select signal GPIO2_IO04. |

36.4.192 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA05)

Address: 20E_0000h base + 310h offset = 20E_0310h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_DATA05 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad NANDF_D5.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 3 iomux modes to be used for pad: NANDF_D5.</p> <p>000 ALT0 — Select signal NAND_DATA05. 001 ALT1 — Select signal SD2_DATA5. 101 ALT5 — Select signal GPIO2_IO05.</p> |

36.4.193 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA06)

Address: 20E_0000h base + 314h offset = 20E_0314h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_DATA06 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad NANDF_D6. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: NANDF_D6. 000 ALT0 — Select signal NAND_DATA06. 001 ALT1 — Select signal SD2_DATA6. 101 ALT5 — Select signal GPIO2_IO06. |

36.4.194 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_NAND_DATA07)

Address: 20E_0000h base + 318h offset = 20E_0318h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_NAND_DATA07 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | <p>Software Input On Field.</p> <p>Force the selected mux mode input path no matter of MUX_MODE functionality.</p> <p>1 ENABLED — Force input path of pad NANDF_D7.</p> <p>0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular).</p> |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | <p>MUX Mode Select Field.</p> <p>Select 1 of 3 iomux modes to be used for pad: NANDF_D7.</p> <p>000 ALT0 — Select signal NAND_DATA07.</p> <p>001 ALT1 — Select signal SD2_DATA7.</p> <p>101 ALT5 — Select signal GPIO2_IO07.</p> |

36.4.195 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA0)

Address: 20E_0000h base + 31Ch offset = 20E_031Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|------|----|----------|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | SION | 0 | MUX_MODE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA0 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_DATA0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD4_DATA0. 001 ALT1 — Select signal SD4_DATA0. 010 ALT2 — Select signal NAND_DQS. 101 ALT5 — Select signal GPIO2_IO08. |

36.4.196 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA1)

Address: 20E_0000h base + 320h offset = 20E_0320h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA1 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_DAT1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD4_DAT1. 001 ALT1 — Select signal SD4_DATA1. 010 ALT2 — Select signal PWM3_OUT. 101 ALT5 — Select signal GPIO2_IO09. |

36.4.197 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA2)

Address: 20E_0000h base + 324h offset = 20E_0324h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|------|----|----|----------|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | SION | | 0 | MUX_MODE | | | | |
| W | | | | | | | | | | | 0 | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA2 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_DAT2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD4_DAT2. 001 ALT1 — Select signal SD4_DATA2. 010 ALT2 — Select signal PWM4_OUT. 101 ALT5 — Select signal GPIO2_IO10. |

36.4.198 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA3)

Address: 20E_0000h base + 328h offset = 20E_0328h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | 0 | | | |
| W | | | | | | | | | | | | | 0 | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA3 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_DAT3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 2 iomux modes to be used for pad: SD4_DAT3. 001 ALT1 — Select signal SD4_DATA3. 101 ALT5 — Select signal GPIO2_IO11. |

36.4.199 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA4)

Address: 20E_0000h base + 32Ch offset = 20E_032Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | 0 | | | |
| W | | | | | | | | | | | | | 0 | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA4 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_DAT4. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD4_DAT4. NOTE: Pad SD4_DAT4 is involved in Daisy Chain. 001 ALT1 — Select signal SD4_DATA4. 010 ALT2 — Select signal UART2_RX_DATA. - Configure register IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO12. |

36.4.200 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA5)

Address: 20E_0000h base + 330h offset = 20E_0330h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | 0 | | | |
| W | | | | | | | | | | | | | | 0 | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA5 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_DAT5. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |

Table continues on the next page...

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA5 field descriptions (continued)

| Field | Description |
|------------|--|
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD4_DAT5. NOTE: Pad SD4_DAT5 is involved in Daisy Chain. 001 ALT1 — Select signal SD4_DATA5. 010 ALT2 — Select signal UART2_RTS_B. - Configure register IOMUXC_UART2_UART_RTS_B_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO13. |

36.4.201 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA6)

Address: 20E_0000h base + 334h offset = 20E_0334h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|------|----|----|----------|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA6 field descriptions

| Field | Description |
|---------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_DAT6. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD4_DAT6. NOTE: Pad SD4_DAT6 is involved in Daisy Chain. 001 ALT1 — Select signal SD4_DATA6. 010 ALT2 — Select signal UART2_CTS_B. |

Table continues on the next page...

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA6 field descriptions (continued)

| Field | Description |
|-------|---|
| 101 | - Configure register IOMUXC_UART2_UART_RTS_B_SELECT_INPUT for mode ALT2. ALT5 — Select signal GPIO2_IO14. |

36.4.202 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD4_DATA7)

Address: 20E_0000h base + 338h offset = 20E_0338h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD4_DATA7 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD4_DAT7. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 3 iomux modes to be used for pad: SD4_DAT7. NOTE: Pad SD4_DAT7 is involved in Daisy Chain. 001 ALT1 — Select signal SD4_DATA7. 010 ALT2 — Select signal UART2_TX_DATA. - Configure register IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT for mode ALT2. 101 ALT5 — Select signal GPIO2_IO15. |

36.4.203 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_DATA1)

Address: 20E_0000h base + 33Ch offset = 20E_033Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD1_DATA1 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD1_DAT1. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: SD1_DAT1. NOTE: Pad SD1_DAT1 is involved in Daisy Chain. 000 ALT0 — Select signal SD1_DATA1. 001 ALT1 — Select signal ECSPi5_SS0. - Configure register IOMUXC_ECSPi5_SS0_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal PWM3_OUT. 011 ALT3 — Select signal GPT_CAPTURE2. 101 ALT5 — Select signal GPIO1_IO17. |

36.4.204 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_DATA0)

Address: 20E_0000h base + 340h offset = 20E_0340h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD1_DATA0 field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD1_DATA0. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: SD1_DATA0. NOTE: Pad SD1_DATA0 is involved in Daisy Chain. 000 ALT0 — Select signal SD1_DATA0. 001 ALT1 — Select signal ECSPI5_MISO. - Configure register IOMUXC_ECSPi5_MISO_SELECT_INPUT for mode ALT1. 011 ALT3 — Select signal GPT_CAPTURE1. 101 ALT5 — Select signal GPIO1_IO16. |

36.4.205 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_DATA3)

Address: 20E_0000h base + 344h offset = 20E_0344h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD1_DATA3 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD1_DAT3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: SD1_DAT3. 000 ALT0 — Select signal SD1_DATA3. 001 ALT1 — Select signal ECSPI5_SS2. 010 ALT2 — Select signal GPT_COMPARE3. 011 ALT3 — Select signal PWM1_OUT. 100 ALT4 — Select signal WDOG2_B. 101 ALT5 — Select signal GPIO1_IO21. 110 ALT6 — Select signal WDOG2_RESET_B_DEB. |

36.4.206 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_CMD)

Address: 20E_0000h base + 348h offset = 20E_0348h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD1_CMD field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD1_CMD. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: SD1_CMD. NOTE: Pad SD1_CMD is involved in Daisy Chain. 000 ALT0 — Select signal SD1_CMD. 001 ALT1 — Select signal ECSPI5_MOSI. - Configure register IOMUXC_ECSPi5_MOSI_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal PWM4_OUT. 011 ALT3 — Select signal GPT_COMPARE1. 101 ALT5 — Select signal GPIO1_IO18. |

36.4.207 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_DATA2)

Address: 20E_0000h base + 34Ch offset = 20E_034Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD1_DATA2 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD1_DAT2. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: SD1_DAT2. NOTE: Pad SD1_DAT2 is involved in Daisy Chain. 000 ALT0 — Select signal SD1_DATA2. 001 ALT1 — Select signal ECSPI5_SS1. - Configure register IOMUXC_ECSPi5_SS1_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal GPT_COMPARE2. 011 ALT3 — Select signal PWM2_OUT. 100 ALT4 — Select signal WDOG1_B. 101 ALT5 — Select signal GPIO1_IO19. 110 ALT6 — Select signal WDOG1_RESET_B_DEB. |

36.4.208 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD1_CLK)

Address: 20E_0000h base + 350h offset = 20E_0350h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD1_CLK field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD1_CLK. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: SD1_CLK. NOTE: Pad SD1_CLK is involved in Daisy Chain. 000 ALT0 — Select signal SD1_CLK. 001 ALT1 — Select signal ECSPi5_SCLK. - Configure register IOMUXC_ECSPi5_CSPI_CLK_IN_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal XTALOSC_OSC32K_32K_OUT. 011 ALT3 — Select signal GPT_CLKIN. 101 ALT5 — Select signal GPIO1_IO20. |

36.4.209 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_CLK)

Address: 20E_0000h base + 354h offset = 20E_0354h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD2_CLK field descriptions

| Field | Description |
|------------------|--|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD2_CLK. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: SD2_CLK. NOTE: Pad SD2_CLK is involved in Daisy Chain. 000 ALT0 — Select signal SD2_CLK. 001 ALT1 — Select signal ECSPi5_SCLK. - Configure register IOMUXC_ECSPi5_CSPI_CLK_IN_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal KEY_COL5. - Configure register IOMUXC_KEY_COL5_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD4_RXFS. - Configure register IOMUXC_AUD4_INPUT_RXFS_AMX_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO1_IO10. |

36.4.210 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_CMD)

Address: 20E_0000h base + 358h offset = 20E_0358h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD2_CMD field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD2_CMD. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: SD2_CMD. NOTE: Pad SD2_CMD is involved in Daisy Chain. 000 ALT0 — Select signal SD2_CMD. 001 ALT1 — Select signal ECSP15_MOSI. - Configure register IOMUXC_ECSP15_MOSI_SELECT_INPUT for mode ALT1. 010 ALT2 — Select signal KEY_ROW5. - Configure register IOMUXC_KEY_ROW5_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD4_RXC. - Configure register IOMUXC_AUD4_INPUT_RXCLK_AMX_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO1_IO11. |

36.4.211 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_SD2_DATA3)

Address: 20E_0000h base + 35Ch offset = 20E_035Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | SION | 0 | | MUX_MODE |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

IOMUXC_SW_MUX_CTL_PAD_SD2_DATA3 field descriptions

| Field | Description |
|------------------|---|
| 31–5 Reserved | This read-only field is reserved and always has the value 0. |
| 4 SION | Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 ENABLED — Force input path of pad SD2_DAT3. 0 DISABLED — Input Path is determined by functionality of the selected mux mode (regular). |
| 3 Reserved | This read-only field is reserved and always has the value 0. |
| MUX_MODE | MUX Mode Select Field. Select 1 of 5 iomux modes to be used for pad: SD2_DAT3. NOTE: Pad SD2_DAT3 is involved in Daisy Chain. 000 ALT0 — Select signal SD2_DATA3. 001 ALT1 — Select signal ECSPI5_SS3. 010 ALT2 — Select signal KEY_COL6. - Configure register IOMUXC_KEY_COL6_SELECT_INPUT for mode ALT2. 011 ALT3 — Select signal AUD4_TXC. - Configure register IOMUXC_AUD4_INPUT_TXCLK_AMX_SELECT_INPUT for mode ALT3. 101 ALT5 — Select signal GPIO1_IO12. |

36.4.212 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_DATA1)

Address: 20E_0000h base + 360h offset = 20E_0360h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD2_DATA1 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD2_DAT1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD2_DAT1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD2_DAT1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD2_DAT1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD2_DATA1 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: SD2_DAT1.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.213 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_DATA2)

Address: 20E_0000h base + 364h offset = 20E_0364h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD2_DATA2 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD2_DAT2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD2_DAT2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD2_DAT2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD2_DAT2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD2_DAT2. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD2_DATA2 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.214 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_DATA0)

Address: 20E_0000h base + 368h offset = 20E_0368h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD2_DATA0 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD2_DAT0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD2_DAT0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD2_DATA0 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD2_DAT0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD2_DAT0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD2_DAT0. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD2_DATA0 field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | |
|-------|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| | 0 SLOW — Slow Slew Rate | | | | | | | | | | | | | | |
| | 1 FAST — Fast Slew Rate | | | | | | | | | | | | | | |

36.4.215 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TXC)

Address: 20E_0000h base + 36Ch offset = 20E_036Ch

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|----|-----|----|----|----|----|-----|----|----|---------|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | DDR_SEL | 0 | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | ODT | | | 0 | | DSE | | | 0 | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_TXC field descriptions

| Field | Description | | | | | | | | | | | | | | | |
|-------------------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. | | | | | | | | | | | | | | | |
| 17 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_TXC. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input | | | | | | | | | | | | | | | |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_TXC. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up | | | | | | | | | | | | | | | |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_TXC field descriptions (continued)

| Field | Description |
|-----------------|--|
| 13 PUE | <p>Pull / Keep Select Field</p> <p>Select one of next values for pad: RGMII_TXC.</p> <p>0 KEEP — Keeper Enabled 1 PULL — Pull Enabled</p> |
| 12 PKE | <p>Pull / Keep Enable Field</p> <p>Select one of next values for pad: RGMII_TXC.</p> <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Read Only Field</p> <p>The value of this field is fixed and cannot be changed.</p> <p>000 DISABLED — Disabled</p> |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: RGMII_TXC.</p> <p>000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V</p> |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.216 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TD0)

Address: 20E_0000h base + 370h offset = 20E_0370h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|-----|----|----|----|-----|----|----|----|---------|----|----|-----|
| R | 0 | | | | | | | | | | | | DDR_SEL | 0 | 0 | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | ODT | | | 0 | DSE | | | 0 | 0 | | | |
| W | | | | 0 | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_TD0 field descriptions

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_TD0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_TD0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_TD0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_TD0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_TD0 field descriptions (continued)

| Field | Description |
|--------------|--|
| | 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Read Only Field The value of this field is fixed and cannot be changed. 000 DISABLED — Disabled |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_TD0. 000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.217 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TD1)

Address: 20E_0000h base + 374h offset = 20E_0374h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | 0 | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | 0 | ODT | | 0 | | DSE | | 0 | | 0 | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_TD1 field descriptions

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_TD1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_TD1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_TD1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_TD1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Read Only Field The value of this field is fixed and cannot be changed. 000 DISABLED — Disabled |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_TD1. 000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_TD1 field descriptions (continued)

| Field | Description |
|----------|---|
| | 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.218 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TD2)

Address: 20E_0000h base + 378h offset = 20E_0378h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | 0 | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | | ODT | | 0 | | DSE | | | 0 | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_TD2 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_TD2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_TD2. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_TD2 field descriptions (continued)

| Field | Description |
|--------------|---|
| | <p>00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up</p> |
| 13 PUE | <p>Pull / Keep Select Field Select one of next values for pad: RGMII_TD2.</p> <p>0 KEEP — Keeper Enabled 1 PULL — Pull Enabled</p> |
| 12 PKE | <p>Pull / Keep Enable Field Select one of next values for pad: RGMII_TD2.</p> <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | <p>On Die Termination Field Read Only Field The value of this field is fixed and cannot be changed.</p> <p>000 DISABLED — Disabled</p> |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: RGMII_TD2.</p> <p>000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V</p> |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.219 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TD3)

Address: 20E_0000h base + 37Ch offset = 20E_037Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|-----|----|----|----|-----|----|----|----|---------|----|-----|----|
| R | 0 | | | | | | | | | | | | DDR_SEL | 0 | HYS | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | ODT | | | 0 | DSE | | | 0 | | | | |
| W | | | | 0 | | | | 0 | | | | 1 | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_TD3 field descriptions

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_TD3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_TD3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_TD3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_TD3. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_TD3 field descriptions (continued)

| Field | Description |
|--------------|---|
| | 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Read Only Field The value of this field is fixed and cannot be changed. 000 DISABLED — Disabled |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_TD3. 000 HI_Z — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.220 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RX_CTL)

Address: 20E_0000h base + 380h offset = 20E_0380h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | 0 | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | 0 | ODT | | 0 | | DSE | | 0 | | 0 | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_RX_CTL field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_RX_CTL. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_RX_CTL. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_RX_CTL. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_RX_CTL. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM Note: The value of this field does not reflect the value of the Group Control Register. |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_RX_CTL. 000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_RX_CTL field descriptions (continued)

| Field | Description |
|----------|--|
| | 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.221 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RD0)

Address: 20E_0000h base + 384h offset = 20E_0384h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|-----|----|----|----|----|----|-----|----|---------|----|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | 0 | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | ODT | | | 0 | | | DSE | | | 0 | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_RD0 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_RD0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_RD0. 00 100K_OHM_PD — 100K Ohm Pull Down |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_RD0 field descriptions (continued)

| Field | Description |
|--------------|--|
| | 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_RD0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_RD0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM Note: The value of this field does not reflect the value of the Group Control Register. |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_RD0. 000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.222 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_TX_CTL)

Address: 20E_0000h base + 388h offset = 20E_0388h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|-----|----|----|----|-----|----|----|----|---------|----|----|-----|
| R | 0 | | | | | | | | | | | | DDR_SEL | 0 | 0 | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | ODT | | | 0 | DSE | | | 0 | 0 | | | |
| W | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_TX_CTL field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_TX_CTL. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_TX_CTL. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_TX_CTL. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_TX_CTL. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_TX_CTL field descriptions (continued)

| Field | Description |
|--------------|---|
| | 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Read Only Field The value of this field is fixed and cannot be changed. 000 DISABLED — Disabled |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_TX_CTL. 000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.223 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RD1)

Address: 20E_0000h base + 38Ch offset = 20E_038Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | 0 | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | 0 | ODT | | 0 | 0 | DSE | | 0 | | 0 | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_RD1 field descriptions

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_RD1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_RD1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_RD1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_RD1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM Note: The value of this field does not reflect the value of the Group Control Register. |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_RD1. 000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_RD1 field descriptions (continued)

| Field | Description |
|----------|--|
| | 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.224 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RD2)

Address: 20E_0000h base + 390h offset = 20E_0390h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|-----|----|----|----|----|----|----|----|---------|----|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | 0 | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | ODT | | | | 0 | | | | DSE | | 0 | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_RD2 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_RD2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_RD2. 00 100K_OHM_PD — 100K Ohm Pull Down |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_RD2 field descriptions (continued)

| Field | Description |
|--------------|--|
| | 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_RD2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_RD2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM Note: The value of this field does not reflect the value of the Group Control Register. |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_RD2. 000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.225 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RD3)

Address: 20E_0000h base + 394h offset = 20E_0394h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|-----|----|----|----|-----|----|----|----|---------|----|-----|----|
| R | 0 | | | | | | | | | | | | DDR_SEL | 0 | HYS | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | ODT | | | 0 | DSE | | | 0 | | | | |
| W | | | | 0 | | | | 0 | | | | 1 | 0 | 0 | 0 | 0 |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_RD3 field descriptions

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_RD3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_RD3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_RD3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_RD3. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_RD3 field descriptions (continued)

| Field | Description |
|--------------|--|
| | 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM Note: The value of this field does not reflect the value of the Group Control Register. |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_RD3. 000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.226 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_RGMII_RXC)

Address: 20E_0000h base + 398h offset = 20E_0398h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|-----|----|----|----|----|-----|----|----|---------|----|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | 0 | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | ODT | | | | 0 | DSE | | | | 0 | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_RGMII_RXC field descriptions

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: RGMII_RXC. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: RGMII_RXC. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: RGMII_RXC. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: RGMII_RXC. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM Note: The value of this field does not reflect the value of the Group Control Register. |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: RGMII_RXC. 000 HIZ — HI-Z 001 287_OHM — 287/174 Ohm @ 2.5V, 247/201 Ohm pd/pu @ 1.8V 010 121_OHM — 121/85 Ohm @ 2.5V, 113/96 Ohm pd/pu @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_RGMII_RXC field descriptions (continued)

| Field | Description |
|----------|--|
| | 011 76_OHM — 76/56 Ohm @ 2.5V, 73/63 Ohm pd/pu @ 1.8V 100 57_OHM — 57/43 Ohm @ 2.5V, 55/48 Ohm pd/pu @ 1.8V 101 45_OHM — 45/34 Ohm @ 2.5V, 43/38 Ohm pd/pu @ 1.8V 110 37_OHM — 37/28 Ohm @ 2.5V, 36/32 Ohm pd/pu @ 1.8V 111 31_OHM — 31/24 Ohm @ 2.5V, 30/27 Ohm pd/pu @ 1.8V |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.227 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR25)

Address: 20E_0000h base + 39Ch offset = 20E_039Ch

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR25 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A25. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A25. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A25. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR25 field descriptions (continued)

| Field | Description |
|------------------|---|
| 12 PKE | <p>Pull / Keep Enable Field</p> <p>Select one of next values for pad: EIM_A25.</p> <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field</p> <p>Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_A25.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.228 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_EB2_B)

Address: 20E_0000h base + 3A0h offset = 20E_03A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_EB2_B field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_EB2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_EB2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_EB2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_EB2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_EB2_B field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_EB2.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.229 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA16)

Address: 20E_0000h base + 3A4h offset = 20E_03A4h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA16 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D16. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D16. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D16. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D16. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_D16. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA16 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.230 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA17)

Address: 20E_0000h base + 3A8h offset = 20E_03A8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA17 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D17. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D17. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA17 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D17. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D17. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_D17. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA17 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.231 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA18)

Address: 20E_0000h base + 3ACh offset = 20E_03ACh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA18 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D18. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D18. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D18. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D18. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA18 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_D18.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.232 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA19)

Address: 20E_0000h base + 3B0h offset = 20E_03B0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA19 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D19. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D19. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D19. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D19. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA19 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_D19.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.233 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA20)

Address: 20E_0000h base + 3B4h offset = 20E_03B4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA20 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D20. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D20. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D20. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D20. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_D20. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA20 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.234 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA21)

Address: 20E_0000h base + 3B8h offset = 20E_03B8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA21 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D21. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D21. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA21 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D21. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D21. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_D21. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA21 field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | |
|-------|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| | 0 SLOW — Slow Slew Rate | | | | | | | | | | | | | | |
| | 1 FAST — Fast Slew Rate | | | | | | | | | | | | | | |

36.4.235 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA22)

Address: 20E_0000h base + 3BCh offset = 20E_03BCh

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|-------|--|----|-----|----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | 0 | | | | | | | | | | | | | | | HYS | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | 0 | | | SPEED | | | DSE | | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA22 field descriptions

| Field | Description | | | | | | | | | | | | | | | | |
|-------------------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D22. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input | | | | | | | | | | | | | | | | |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D22. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up | | | | | | | | | | | | | | | | |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D22. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled | | | | | | | | | | | | | | | | |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D22. | | | | | | | | | | | | | | | | |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA22 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_D22.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.236 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA23)

Address: 20E_0000h base + 3C0h offset = 20E_03C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA23 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D23. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D23. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D23. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D23. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA23 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_D23.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.237 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_EB3_B)

Address: 20E_0000h base + 3C4h offset = 20E_03C4h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_EB3_B field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_EB3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_EB3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_EB3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_EB3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_EB3. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_EB3_B field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.238 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA24)

Address: 20E_0000h base + 3C8h offset = 20E_03C8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA24 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D24. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D24. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA24 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D24. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D24. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_D24. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA24 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.239 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA25)

Address: 20E_0000h base + 3CCh offset = 20E_03CCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA25 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D25. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D25. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D25. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D25. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA25 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_D25.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.240 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA26)

Address: 20E_0000h base + 3D0h offset = 20E_03D0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA26 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D26. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D26. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D26. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D26. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA26 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_D26.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.241 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA27)

Address: 20E_0000h base + 3D4h offset = 20E_03D4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA27 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D27. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D27. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D27. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D27. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_D27. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA27 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.242 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA28)

Address: 20E_0000h base + 3D8h offset = 20E_03D8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA28 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D28. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D28. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA28 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D28. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D28. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_D28. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA28 field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | |
|-------|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| | 0 SLOW — Slow Slew Rate | | | | | | | | | | | | | | |
| | 1 FAST — Fast Slew Rate | | | | | | | | | | | | | | |

36.4.243 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA29)

Address: 20E_0000h base + 3DCh offset = 20E_03DCh

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|-------|--|----|-----|----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | 0 | | | | | | | | | | | | | | | HYS | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | 0 | | | SPEED | | | DSE | | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA29 field descriptions

| Field | Description | | | | | | | | | | | | | | | | |
|-------------------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D29. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input | | | | | | | | | | | | | | | | |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D29. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up | | | | | | | | | | | | | | | | |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D29. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled | | | | | | | | | | | | | | | | |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D29. | | | | | | | | | | | | | | | | |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA29 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_D29.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.244 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA30)

Address: 20E_0000h base + 3E0h offset = 20E_03E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA30 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D30. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D30. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D30. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D30. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA30 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_D30.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.245 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_DATA31)

Address: 20E_0000h base + 3E4h offset = 20E_03E4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA31 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_D31. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_D31. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_D31. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_D31. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_D31. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_DATA31 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.246 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR24)

Address: 20E_0000h base + 3E8h offset = 20E_03E8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | | 0 | | SPEED | | DSE | | 0 | | 0 | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR24 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A24. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A24. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR24 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A24. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_A24. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_A24. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR24 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.247 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR23)

Address: 20E_0000h base + 3ECh offset = 20E_03ECh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR23 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A23. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A23. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A23. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_A23. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR23 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_A23.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.248 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR22)

Address: 20E_0000h base + 3F0h offset = 20E_03F0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR22 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A22. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A22. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A22. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_A22. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR22 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_A22.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.249 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR21)

Address: 20E_0000h base + 3F4h offset = 20E_03F4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR21 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A21. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A21. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A21. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_A21. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_A21. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR21 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.250 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR20)

Address: 20E_0000h base + 3F8h offset = 20E_03F8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR20 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A20. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A20. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR20 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A20. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_A20. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_A20. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR20 field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | |
|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| | 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | |

36.4.251 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR19)

Address: 20E_0000h base + 3FCh offset = 20E_03FCh

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|-------|--|----|-----|----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | 0 | | | | | | | | | | | | | | | HYS | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | 0 | | | SPEED | | | DSE | | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR19 field descriptions

| Field | Description | | | | | | | | | | | | | | | | |
|-------------------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A19. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input | | | | | | | | | | | | | | | | |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A19. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up | | | | | | | | | | | | | | | | |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A19. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled | | | | | | | | | | | | | | | | |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_A19. | | | | | | | | | | | | | | | | |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR19 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_A19.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.252 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR18)

Address: 20E_0000h base + 400h offset = 20E_0400h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR18 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A18. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A18. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A18. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_A18. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR18 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_A18.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.253 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR17)

Address: 20E_0000h base + 404h offset = 20E_0404h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR17 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A17. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A17. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A17. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_A17. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_A17. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR17 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.254 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR16)

Address: 20E_0000h base + 408h offset = 20E_0408h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR16 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_A16. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_A16. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR16 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_A16. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_A16. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_A16. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR16 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.255 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_CS0_B)

Address: 20E_0000h base + 40Ch offset = 20E_040Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_CS0_B field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_CS0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_CS0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_CS0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_CS0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_CS0_B field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_CS0.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.256 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_CS1_B)

Address: 20E_0000h base + 410h offset = 20E_0410h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_CS1_B field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_CS1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_CS1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_CS1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_CS1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_CS1_B field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_CS1.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.257 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_OE_B)

Address: 20E_0000h base + 414h offset = 20E_0414h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_OE_B field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_OE. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_OE. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_OE. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_OE. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_OE. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_OE_B field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.258 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_RW)

Address: 20E_0000h base + 418h offset = 20E_0418h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_RW field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_RW. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_RW. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_RW field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_RW. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_RW. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_RW. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_RW field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.259 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_LBA_B)

Address: 20E_0000h base + 41Ch offset = 20E_041Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_LBA_B field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_LBA. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_LBA. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_LBA. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_LBA. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_LBA_B field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_LBA.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.260 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_EB0_B)

Address: 20E_0000h base + 420h offset = 20E_0420h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_EB0_B field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_EB0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_EB0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_EB0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_EB0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_EB0_B field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_EB0.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.261 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_EB1_B)

Address: 20E_0000h base + 424h offset = 20E_0424h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_EB1_B field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_EB1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_EB1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_EB1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_EB1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_EB1. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_EB1_B field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.262 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD00)

Address: 20E_0000h base + 428h offset = 20E_0428h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD00 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD00 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_DA0. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD00 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.263 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD01)

Address: 20E_0000h base + 42Ch offset = 20E_042Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD01 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD01 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_DA1.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.264 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD02)

Address: 20E_0000h base + 430h offset = 20E_0430h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD02 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD02 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_DA2.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.265 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD03)

Address: 20E_0000h base + 434h offset = 20E_0434h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD03 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_DA3. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD03 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.266 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD04)

Address: 20E_0000h base + 438h offset = 20E_0438h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD04 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD04 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA4. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_DA4. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD04 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.267 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD05)

Address: 20E_0000h base + 43Ch offset = 20E_043Ch

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD05 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA5. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA5. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA5. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA5. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD05 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_DA5.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.268 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD06)

Address: 20E_0000h base + 440h offset = 20E_0440h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD06 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA6. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA6. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA6. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA6. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD06 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_DA6.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.269 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD07)

Address: 20E_0000h base + 444h offset = 20E_0444h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD07 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA7. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA7. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA7. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA7. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_DA7. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD07 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.270 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD08)

Address: 20E_0000h base + 448h offset = 20E_0448h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD08 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA8. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA8. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD08 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA8. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA8. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_DA8. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD08 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.271 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD09)

Address: 20E_0000h base + 44Ch offset = 20E_044Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD09 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA9. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA9. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA9. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA9. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD09 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_DA9.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.272 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD10)

Address: 20E_0000h base + 450h offset = 20E_0450h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD10 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA10. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA10. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA10. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA10. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD10 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_DA10.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.273 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD11)

Address: 20E_0000h base + 454h offset = 20E_0454h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD11 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA11. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA11. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA11. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA11. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_DA11. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD11 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.274 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD12)

Address: 20E_0000h base + 458h offset = 20E_0458h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD12 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA12. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA12. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD12 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA12. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA12. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_DA12. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD12 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.275 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD13)

Address: 20E_0000h base + 45Ch offset = 20E_045Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD13 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA13. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA13. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA13. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA13. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD13 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_DA13.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.276 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD14)

Address: 20E_0000h base + 460h offset = 20E_0460h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD14 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA14. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA14. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA14. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA14. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD14 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: EIM_DA14.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.277 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_AD15)

Address: 20E_0000h base + 464h offset = 20E_0464h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_AD15 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_DA15. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_DA15. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_DA15. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_DA15. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_DA15. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_AD15 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.278 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_WAIT_B)

Address: 20E_0000h base + 468h offset = 20E_0468h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | | 0 | | SPEED | | DSE | | 0 | | 0 | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_EIM_WAIT_B field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_WAIT. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_WAIT. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_WAIT_B field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_WAIT. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_WAIT. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: EIM_WAIT. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_WAIT_B field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.279 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_BCLK)

Address: 20E_0000h base + 46Ch offset = 20E_046Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_EIM_BCLK field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: EIM_BCLK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: EIM_BCLK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: EIM_BCLK. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: EIM_BCLK. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_BCLK field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: EIM_BCLK.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.280 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DI0_DISP_CLK)

Address: 20E_0000h base + 470h offset = 20E_0470h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DI0_DISP_CLK field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DI0_DISP_CLK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DI0_DISP_CLK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DI0_DISP_CLK. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DI0_DISP_CLK. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DI0_DISP_CLK field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DI0_DISP_CLK.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.281 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DI0_PIN15)

Address: 20E_0000h base + 474h offset = 20E_0474h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN15 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DI0_PIN15. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DI0_PIN15. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DI0_PIN15. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DI0_PIN15. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DI0_PIN15. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN15 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.282 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DI0_PIN02)

Address: 20E_0000h base + 478h offset = 20E_0478h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN02 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DI0_PIN2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DI0_PIN2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN02 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DI0_PIN2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DI0_PIN2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DI0_PIN2. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN02 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.283 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DI0_PIN03)

Address: 20E_0000h base + 47Ch offset = 20E_047Ch

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN03 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DI0_PIN3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DI0_PIN3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DI0_PIN3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DI0_PIN3. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN03 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DI0_PIN3.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.284 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DI0_PIN04)

Address: 20E_0000h base + 480h offset = 20E_0480h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN04 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DI0_PIN4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DI0_PIN4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DI0_PIN4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DI0_PIN4. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN04 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DI0_PIN4.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.285 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA00)

Address: 20E_0000h base + 484h offset = 20E_0484h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA00 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT0. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA00 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.286 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA01)

Address: 20E_0000h base + 488h offset = 20E_0488h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA01 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA01 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT1. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA01 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.287 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA02)

Address: 20E_0000h base + 48Ch offset = 20E_048Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA02 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT2. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA02 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DISP0_DAT2.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.288 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA03)

Address: 20E_0000h base + 490h offset = 20E_0490h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA03 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA03 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DISP0_DAT3.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.289 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA04)

Address: 20E_0000h base + 494h offset = 20E_0494h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA04 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT4. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT4. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA04 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.290 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA05)

Address: 20E_0000h base + 498h offset = 20E_0498h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA05 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT5. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT5. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA05 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT5. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT5. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT5. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA05 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.291 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA06)

Address: 20E_0000h base + 49Ch offset = 20E_049Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA06 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT6. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT6. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT6. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT6. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA06 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DISP0_DAT6.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.292 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA07)

Address: 20E_0000h base + 4A0h offset = 20E_04A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA07 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT7. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT7. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT7. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT7. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA07 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DISP0_DAT7.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.293 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA08)

Address: 20E_0000h base + 4A4h offset = 20E_04A4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA08 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT8. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT8. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT8. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT8. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT8. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA08 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.294 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA09)

Address: 20E_0000h base + 4A8h offset = 20E_04A8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA09 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT9. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT9. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA09 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT9. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT9. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT9. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA09 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.295 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA10)

Address: 20E_0000h base + 4ACh offset = 20E_04ACh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA10 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT10. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT10. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT10. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT10. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA10 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DISP0_DAT10.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.296 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA11)

Address: 20E_0000h base + 4B0h offset = 20E_04B0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA11 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT11. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT11. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT11. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT11. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA11 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DISP0_DAT11.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.297 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA12)

Address: 20E_0000h base + 4B4h offset = 20E_04B4h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA12 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT12. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT12. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT12. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT12. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT12. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA12 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.298 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA13)

Address: 20E_0000h base + 4B8h offset = 20E_04B8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA13 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT13. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT13. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA13 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT13. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT13. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT13. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA13 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.299 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA14)

Address: 20E_0000h base + 4BCh offset = 20E_04BCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA14 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT14. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT14. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT14. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT14. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA14 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DISP0_DAT14.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.300 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA15)

Address: 20E_0000h base + 4C0h offset = 20E_04C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA15 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT15. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT15. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT15. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT15. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA15 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DISP0_DAT15.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.301 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA16)

Address: 20E_0000h base + 4C4h offset = 20E_04C4h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA16 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT16. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT16. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT16. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT16. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT16. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA16 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.302 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA17)

Address: 20E_0000h base + 4C8h offset = 20E_04C8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA17 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT17. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT17. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA17 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT17. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT17. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT17. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA17 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.303 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA18)

Address: 20E_0000h base + 4CCh offset = 20E_04CCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA18 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT18. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT18. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT18. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT18. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA18 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DISP0_DAT18.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.304 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA19)

Address: 20E_0000h base + 4D0h offset = 20E_04D0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA19 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT19. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT19. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT19. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT19. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA19 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DISP0_DAT19.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.305 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA20)

Address: 20E_0000h base + 4D4h offset = 20E_04D4h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA20 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT20. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT20. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT20. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT20. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT20. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA20 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.306 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA21)

Address: 20E_0000h base + 4D8h offset = 20E_04D8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA21 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT21. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT21. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA21 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT21. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT21. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DISP0_DAT21. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA21 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.307 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA22)

Address: 20E_0000h base + 4DCh offset = 20E_04DCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA22 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT22. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT22. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT22. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT22. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA22 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DISP0_DAT22.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.308 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA23)

Address: 20E_0000h base + 4E0h offset = 20E_04E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA23 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DISP0_DAT23. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DISP0_DAT23. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DISP0_DAT23. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DISP0_DAT23. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DISP0_DATA23 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DISP0_DAT23.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.309 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_MDIO)

Address: 20E_0000h base + 4E4h offset = 20E_04E4h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_MDIO field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_MDIO. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_MDIO. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_MDIO. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_MDIO. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: ENET_MDIO. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_MDIO field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.310 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_REF_CLK)

Address: 20E_0000h base + 4E8h offset = 20E_04E8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_REF_CLK field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_REF_CLK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_REF_CLK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_REF_CLK field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_REF_CLK. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_REF_CLK. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: ENET_REF_CLK. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_REF_CLK field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.311 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_RX_ER)

Address: 20E_0000h base + 4ECh offset = 20E_04ECh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_RX_ER field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_RX_ER. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_RX_ER. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_RX_ER. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_RX_ER. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_RX_ER field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: ENET_RX_ER.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.312 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_CRS_DV)

Address: 20E_0000h base + 4F0h offset = 20E_04F0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|-------|----|-----|----|----|----|----|-----|----|-----|
| R | 0 | | | | | | | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | 0 | | SPEED | | DSE | | | 0 | | SRE | | |
| W | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_CRS_DV field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_CRS_DV. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_CRS_DV. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_CRS_DV. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_CRS_DV. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_CRS_DV field descriptions (continued)

| Field | Description |
|------------------|---|
| | 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. Read Only Field The value of this field is fixed and cannot be changed. 10 MEDIUM — Medium frequency (100, 150 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: ENET_CRS_DV. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.313 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_RX_DATA1)

Address: 20E_0000h base + 4F4h offset = 20E_04F4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|-------|----|----|-----|----|----|----|-----|----|-----|
| R | 0 | | | | | | | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | 0 | | SPEED | | | DSE | | | 0 | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_RX_DATA1 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_RXD1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_RXD1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_RXD1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_RXD1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: ENET_RXD1. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_RX_DATA1 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.314 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_RX_DATA0)

Address: 20E_0000h base + 4F8h offset = 20E_04F8h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_RX_DATA0 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_RXD0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_RXD0. 00 100K_OHM_PD — 100K Ohm Pull Down |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_RX_DATA0 field descriptions (continued)

| Field | Description |
|---------------|---|
| | 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_RXD0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_RXD0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. Read Only Field The value of this field is fixed and cannot be changed. 10 MEDIUM — Medium frequency (100, 150 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: ENET_RXD0. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_RX_DATA0 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.315 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_TX_EN)

Address: 20E_0000h base + 4FCh offset = 20E_04FCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_TX_EN field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_TX_EN. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_TX_EN. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_TX_EN. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_TX_EN. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_TX_EN field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: ENET_TX_EN.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.316 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_TX_DATA1)

Address: 20E_0000h base + 500h offset = 20E_0500h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_TX_DATA1 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_TXD1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_TXD1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_TXD1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_TXD1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_TX_DATA1 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: ENET_TXD1.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.317 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_TX_DATA0)

Address: 20E_0000h base + 504h offset = 20E_0504h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_TX_DATA0 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_TXD0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_TXD0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_TXD0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_TXD0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: ENET_TXD0. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_TX_DATA0 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.318 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_ENET_MDC)

Address: 20E_0000h base + 508h offset = 20E_0508h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_ENET_MDC field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: ENET_MDC. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: ENET_MDC. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_MDC field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: ENET_MDC. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: ENET_MDC. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: ENET_MDC. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_ENET_MDC field descriptions (continued)

| Field | Description |
|-------|------------------------------|
| 0 | SLOW — Slow Slew Rate |
| 1 | FAST — Fast Slew Rate |

36.4.319 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS5_P)

Address: 20E_0000h base + 50Ch offset = 20E_050Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|-----|----|----|----|----|----|----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | DDR_INPUT | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | 0 | | | | | 0 | | | | DSE | 0 | | |
| W | | | | | ODT | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS5_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS5_P field descriptions (continued)

| Field | Description |
|-----------------|--|
| | <p>This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE</p> <p>Note: The value of this field does not reflect the value of the Group Control Register.</p> |
| 17 DDR_INPUT | <p>DDR / CMOS Input Mode Field</p> <p>This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRMODE_CTL</p> <p>Note: The value of this field does not reflect the value of the Group Control Register.</p> |
| 16 HYS | <p>Hysteresis Enable Field</p> <p>This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRHYS</p> <p>Note: The value of this field does not reflect the value of the Group Control Register.</p> |
| 15–14 PUS | <p>Pull Up / Down Config. Field</p> <p>Select one of next values for pad: DRAM_SDQS5.</p> <ul style="list-style-type: none"> 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | <p>Pull / Keep Select Field</p> <p>Select one of next values for pad: DRAM_SDQS5.</p> <ul style="list-style-type: none"> 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | <p>Pull / Keep Enable Field</p> <p>Select one of next values for pad: DRAM_SDQS5.</p> <ul style="list-style-type: none"> 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for pad: DRAM_SDQS5.</p> <ul style="list-style-type: none"> 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field |

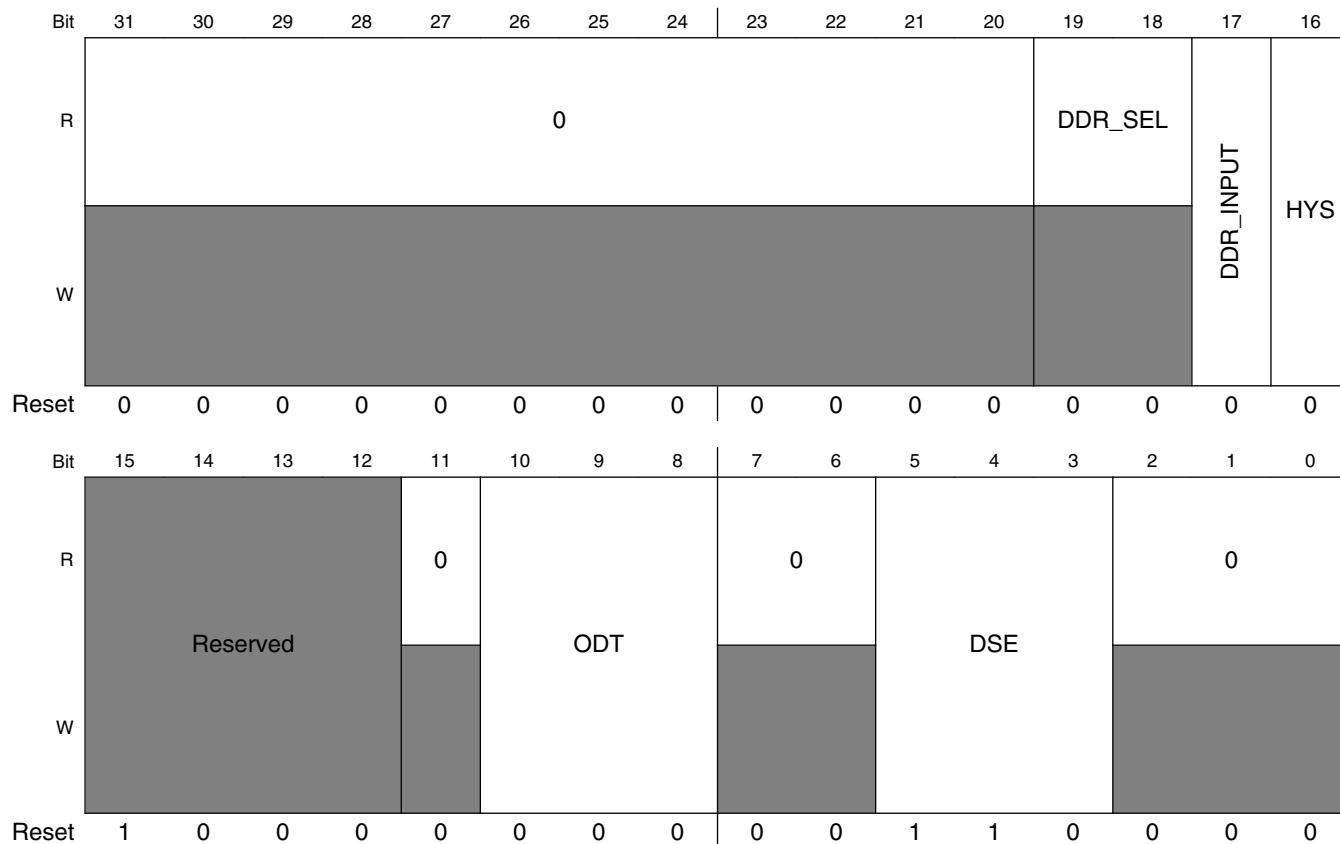
Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS5_P field descriptions (continued)

| Field | Description |
|----------|---|
| | Select one of next values for pad: DRAM_SDQS5. 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.320 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM5)

Address: 20E_0000h base + 510h offset = 20E_0510h



IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM5 field descriptions

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_DQM5. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_DQM5. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_DQM5. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_DQM5. 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.321 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM4)

Address: 20E_0000h base + 514h offset = 20E_0514h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|-----|----|----|-----------|----|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | DDR_INPUT | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | 0 | | | 0 | | |
| W | | | | Reserved | | ODT | | | | DSE | | | | 0 | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM4 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_DQM4. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_DQM4. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM4 field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|--|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field Select one of next values for pad: DRAM_DQM4.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DRAM_DQM4.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.322 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS4_P)

Address: 20E_0000h base + 518h offset = 20E_0518h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|-----------|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | DDR_INPUT | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | | | 0 | |
| | PUS | PUE | PKE | | | ODT | | | | DSE | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS4_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRCODE_CTL |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS4_P field descriptions (continued)

| Field | Description |
|-----------------|--|
| | Note: The value of this field does not reflect the value of the Group Control Register. |
| 16 HYS | Hysteresis Enable Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRHYS Note: The value of this field does not reflect the value of the Group Control Register. |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DRAM_SDQS4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DRAM_SDQS4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DRAM_SDQS4. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDQS4. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_SDQS4. 000 HIZ — Hi-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS4_P field descriptions (continued)

| Field | Description |
|----------|--|
| | 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.323 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS3_P)

Address: 20E_0000h base + 51Ch offset = 20E_051Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|-----|-----|----|----|----|-----|----|----|-----|----|---------|----|-----------|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | DDR_INPUT | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | 0 | | | |
| PUS | | | PUE | PKE | | | | ODT | | | DSE | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS3_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRMODE_CTL Note: The value of this field does not reflect the value of the Group Control Register. |
| 16 HYS | Hysteresis Enable Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRHYS Note: The value of this field does not reflect the value of the Group Control Register. |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DRAM_SDQS3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DRAM_SDQS3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DRAM_SDQS3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDQS3. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |

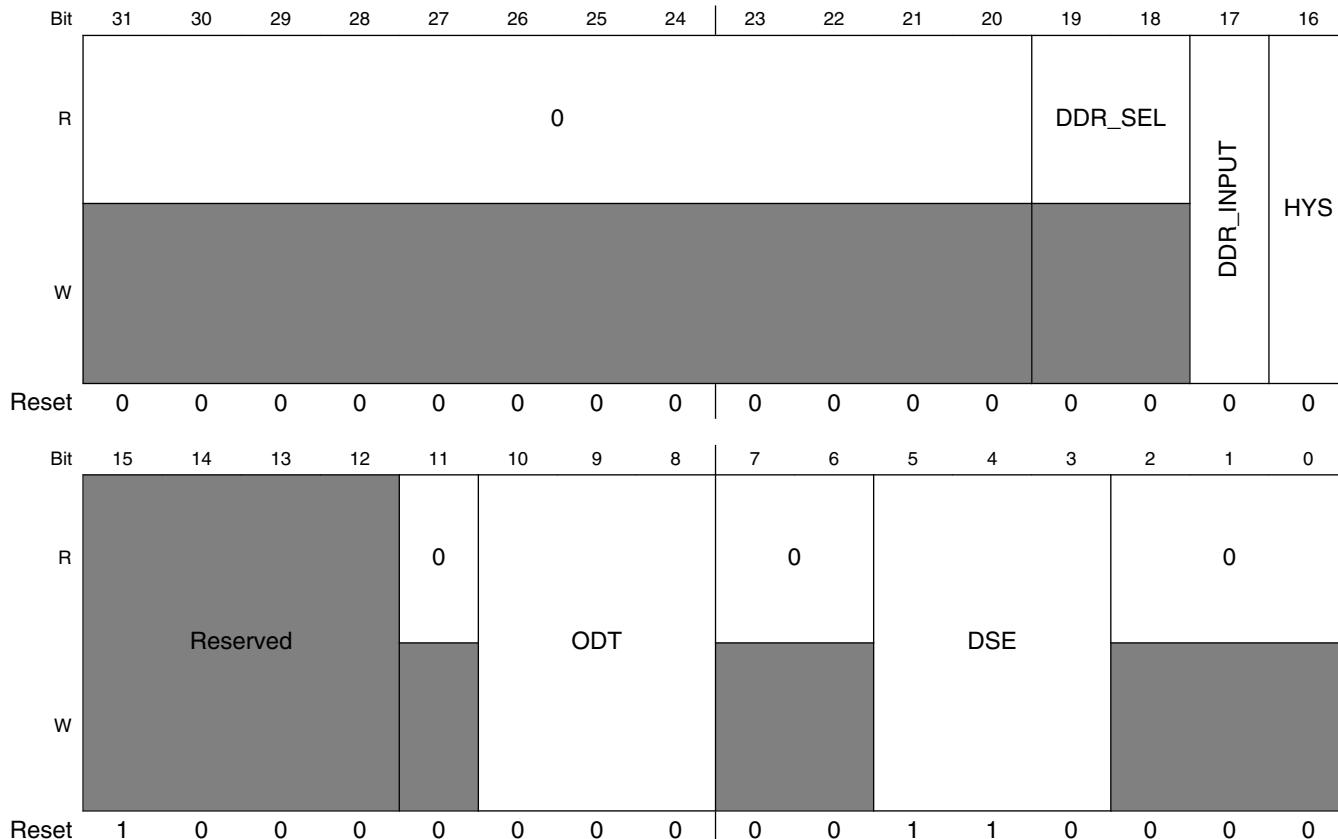
Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS3_P field descriptions (continued)

| Field | Description |
|-----------------|---|
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_SDQS3. 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.324 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM3)

Address: 20E_0000h base + 520h offset = 20E_0520h



IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM3 field descriptions

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_DQM3. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_DQM3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_DQM3. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_DQM3. 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.325 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS2_P)

Address: 20E_0000h base + 524h offset = 20E_0524h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|-----------|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | DDR_INPUT | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | | | 0 | |
| | PUS | PUE | PKE | | | ODT | | | | DSE | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS2_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRCODE_CTL |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS2_P field descriptions (continued)

| Field | Description |
|-----------------|--|
| | Note: The value of this field does not reflect the value of the Group Control Register. |
| 16 HYS | Hysteresis Enable Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRHYS Note: The value of this field does not reflect the value of the Group Control Register. |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DRAM_SDQS2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DRAM_SDQS2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DRAM_SDQS2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDQS2. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_SDQS2. 000 HIZ — Hi-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm |

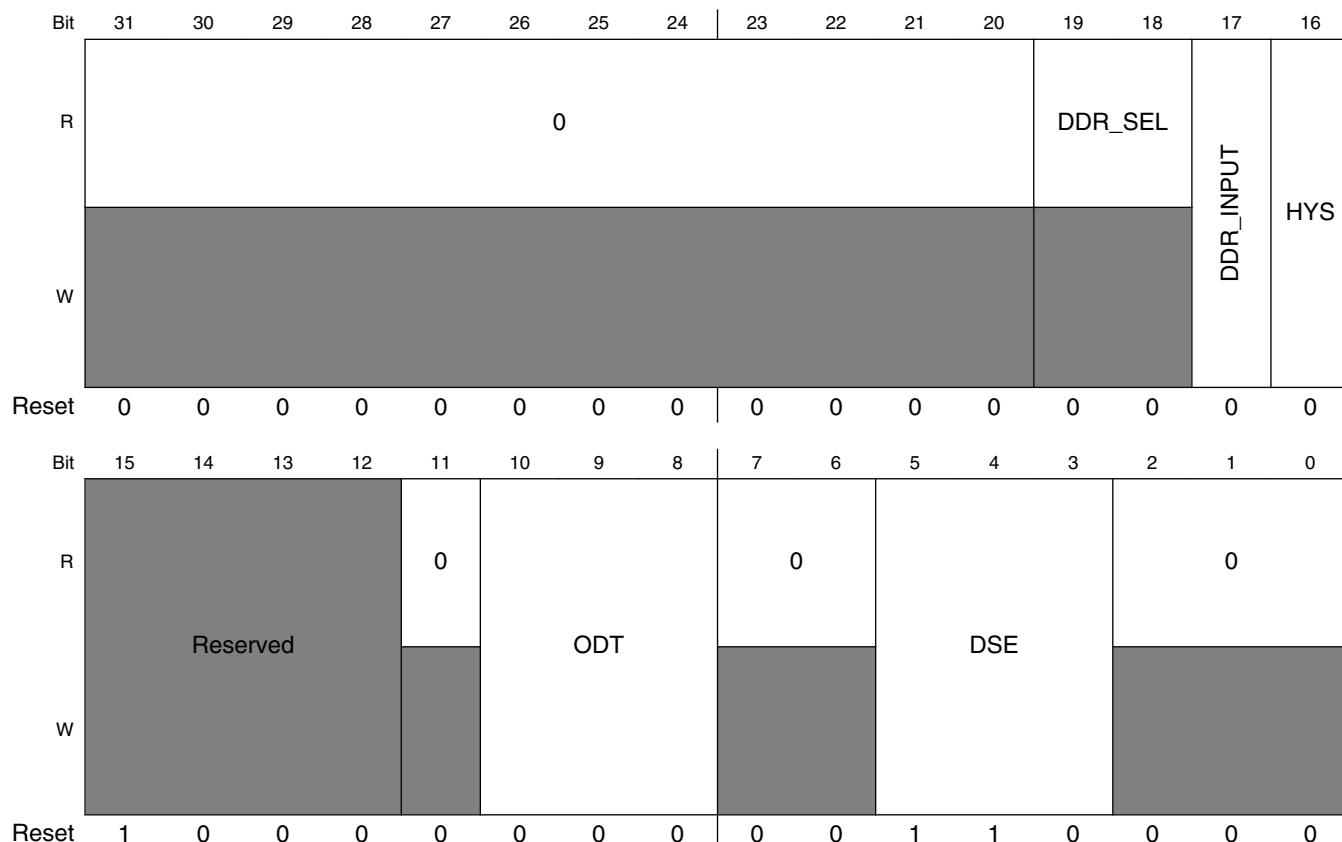
Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS2_P field descriptions (continued)

| Field | Description |
|----------|--|
| | 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.326 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM2)

Address: 20E_0000h base + 528h offset = 20E_0528h

**IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM2 field descriptions**

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM2 field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | Note: The value of this field does not reflect the value of the Group Control Register. | | | | | | | | | | | | | | | | |
| 17 DDR_INPUT | <p>DDR / CMOS Input Mode Field</p> <p>Select one of next values for pad: DRAM_DQM2.</p> <p>0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode.</p> | | | | | | | | | | | | | | | | |
| 16 HYS | <p>Hysteresis Enable Field</p> <p>Select one of next values for pad: DRAM_DQM2.</p> <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for pad: DRAM_DQM2.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DRAM_DQM2.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.327 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR00)

Address: 20E_0000h base + 52Ch offset = 20E_052Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----------|----|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | Reserved | | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR00 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A0. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR00 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A0. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.328 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR01)

Address: 20E_0000h base + 530h offset = 20E_0530h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR01 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A1. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR01 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A1. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.329 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR02)

Address: 20E_0000h base + 534h offset = 20E_0534h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR02 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A2. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A2. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR02 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A2. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.330 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR03)

Address: 20E_0000h base + 538h offset = 20E_0538h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR03 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A3. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A3. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR03 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A3. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.331 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR04)

Address: 20E_0000h base + 53Ch offset = 20E_053Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR04 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A4. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A4. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR04 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A4. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.332 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR05)

Address: 20E_0000h base + 540h offset = 20E_0540h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|---|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR05 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A5. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A5. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR05 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A5. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.333 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR06)

Address: 20E_0000h base + 544h offset = 20E_0544h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR06 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A6. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A6. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR06 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A6. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.334 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR07)

Address: 20E_0000h base + 548h offset = 20E_0548h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----------|----|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | Reserved | | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR07 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A7. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A7. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR07 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A7. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.335 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR08)

Address: 20E_0000h base + 54Ch offset = 20E_054Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR08 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A8. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A8. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR08 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A8. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.336 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR09)

Address: 20E_0000h base + 550h offset = 20E_0550h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----------|----|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | Reserved | | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR09 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A9. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A9. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR09 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A9. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.337 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR10)

Address: 20E_0000h base + 554h offset = 20E_0554h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR10 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A10. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A10. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR10 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A10. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.338 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR11)

Address: 20E_0000h base + 558h offset = 20E_0558h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR11 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A11. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A11. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR11 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A11. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.339 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR12)

Address: 20E_0000h base + 55Ch offset = 20E_055Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR12 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A12. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A12. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR12 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A12. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.340 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR13)

Address: 20E_0000h base + 560h offset = 20E_0560h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----------|----|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | Reserved | | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR13 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A13. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A13. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR13 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A13. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.341 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR14)

Address: 20E_0000h base + 564h offset = 20E_0564h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|---|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR14 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A14. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A14. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR14 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A14. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.342 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR15)

Address: 20E_0000h base + 568h offset = 20E_0568h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR15 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_A15. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_A15. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ADDR15 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_A15. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.343 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_CAS_B)

Address: 20E_0000h base + 56Ch offset = 20E_056Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|-----|----|----|-----------|----|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | DDR_INPUT | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | | 0 | | |
| W | | | | Reserved | | ODT | | | | DSE | | | | 0 | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_CAS_B field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_CAS. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_CAS. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_CAS_B field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field Select one of next values for pad: DRAM_CAS.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DRAM_CAS.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.344 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_CS0_B)

Address: 20E_0000h base + 570h offset = 20E_0570h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|---|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_CS0_B field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_CS0. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_CS0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_CS0_B field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_CS0. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_CTLDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.345 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_CS1_B)

Address: 20E_0000h base + 574h offset = 20E_0574h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|---|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_CS1_B field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_CS1. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_CS1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_CS1_B field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_CS1. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_CTLDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.346 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_RAS_B)

Address: 20E_0000h base + 578h offset = 20E_0578h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|---|----|-----|----|----|-----------|----|----|-----|
| R | | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | | 0 | | | | | 0 | | |
| W | | | | Reserved | | ODT | | | | | DSE | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_RAS_B field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_RAS. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_RAS. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_RAS_B field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field Select one of next values for pad: DRAM_RAS.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DRAM_RAS.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.347 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_RESET)

Address: 20E_0000h base + 57Ch offset = 20E_057Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|-----|----|---------|----|-----------|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | DDR_SEL | | DDR_INPUT | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | 0 | | 0 | |
| W | | | | Reserved | | ODT | | | 0 | | DSE | | | 0 | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_RESET field descriptions

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field Select one of next values for pad: DRAM_RESET. 00 DDR3_LPDDR2 — DDR3 and LPDDR2 mode. 01 RESERVED1 — Reserved 10 RESERVED2 — Reserved 11 RESERVED3 — Reserved |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_RESET. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_RESET. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_RESET field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|--|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for pad: DRAM_RESET.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DRAM_RESET.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.348 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA0)

Address: 20E_0000h base + 580h offset = 20E_0580h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|---|----|----|----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | | 0 | | | | DSE | | 0 | |
| W | | | | Reserved | | ODT | | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA0 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDBA0. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDBA0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA0 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDBA0. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.349 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA1)

Address: 20E_0000h base + 584h offset = 20E_0584h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|---|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA1 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDBA1. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDBA1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA1 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDBA1. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_ADDDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.350 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK0_P)

Address: 20E_0000h base + 588h offset = 20E_0588h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|-----|----|----|---------|-----------|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | | 0 | | |
| W | | | | Reserved | | ODT | | | | DSE | | | | 0 | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK0_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDCLK_0. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDCLK_0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK0_P field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field Select one of next values for pad: DRAM_SDCLK_0.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DRAM_SDCLK_0.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.351 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA2)

Address: 20E_0000h base + 58Ch offset = 20E_058Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|---|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA2 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDBA2. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDBA2. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDBA2 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDBA2. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_CTLDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.352 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE0)

Address: 20E_0000h base + 590h offset = 20E_0590h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|-----|----|---------|-----------|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | DSE | | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE0 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDCKE0. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDCKE0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE0 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDCKE0. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_CTLDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.353 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK1_P)

Address: 20E_0000h base + 594h offset = 20E_0594h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|-----|----|----|---------|-----------|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | | 0 | | |
| W | | | | Reserved | | ODT | | | | DSE | | | | 0 | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK1_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDCLK_1. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDCLK_1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK1_P field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field Select one of next values for pad: DRAM_SDCLK_1.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: DRAM_SDCLK_1.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.354 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE1)

Address: 20E_0000h base + 598h offset = 20E_0598h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE1 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDCKE1. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDCKE1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE1 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDCKE1. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_CTLDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.355 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ODT0)

Address: 20E_0000h base + 59Ch offset = 20E_059Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|-----|----|----|-----------|----|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | DDR_INPUT | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | 0 | | | 0 | | |
| W | | | | Reserved | | ODT | | | | DSE | | | | 0 | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ODT0 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDODT0. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDODT0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ODT0 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDODT0. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_SDODT0. 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.356 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_ODT1)

Address: 20E_0000h base + 5A0h offset = 20E_05A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|-----|----|----|-----------|----|----|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | DDR_INPUT | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | 0 | | | 0 | | |
| W | | | | Reserved | | ODT | | | | DSE | | | | 0 | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_ODT1 field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDODT1. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDODT1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_ODT1 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDODT1. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_SDODT1. 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.357 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDWE_B)

Address: 20E_0000h base + 5A4h offset = 20E_05A4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----------|----|-----|----|----|----|----|----|-----|---------|-----------|----|-----|
| R | | | | | | | | 0 | | | | | DDR_SEL | | | |
| W | | | | | | | | | | | | | | DDR_INPUT | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | DSE | | 0 | | |
| W | | | | Reserved | | ODT | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDWE_B field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field Select one of next values for pad: DRAM_SDWE. 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: DRAM_SDWE. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDWE_B field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–12 - | This field is reserved. Reserved |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDWE. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_CTLDS Note: The value of this field does not reflect the value of the Group Control Register. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.358 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS0_P)

Address: 20E_0000h base + 5A8h offset = 20E_05A8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|-----------|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | DDR_INPUT | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | | | 0 | |
| | PUS | PUE | PKE | | | ODT | | | | DSE | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS0_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRCODE_CTL |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS0_P field descriptions (continued)

| Field | Description |
|-----------------|--|
| | Note: The value of this field does not reflect the value of the Group Control Register. |
| 16 HYS | Hysteresis Enable Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRHYS Note: The value of this field does not reflect the value of the Group Control Register. |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DRAM_SDQS0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DRAM_SDQS0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DRAM_SDQS0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDQS0. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_SDQS0. 000 HIZ — Hi-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm |

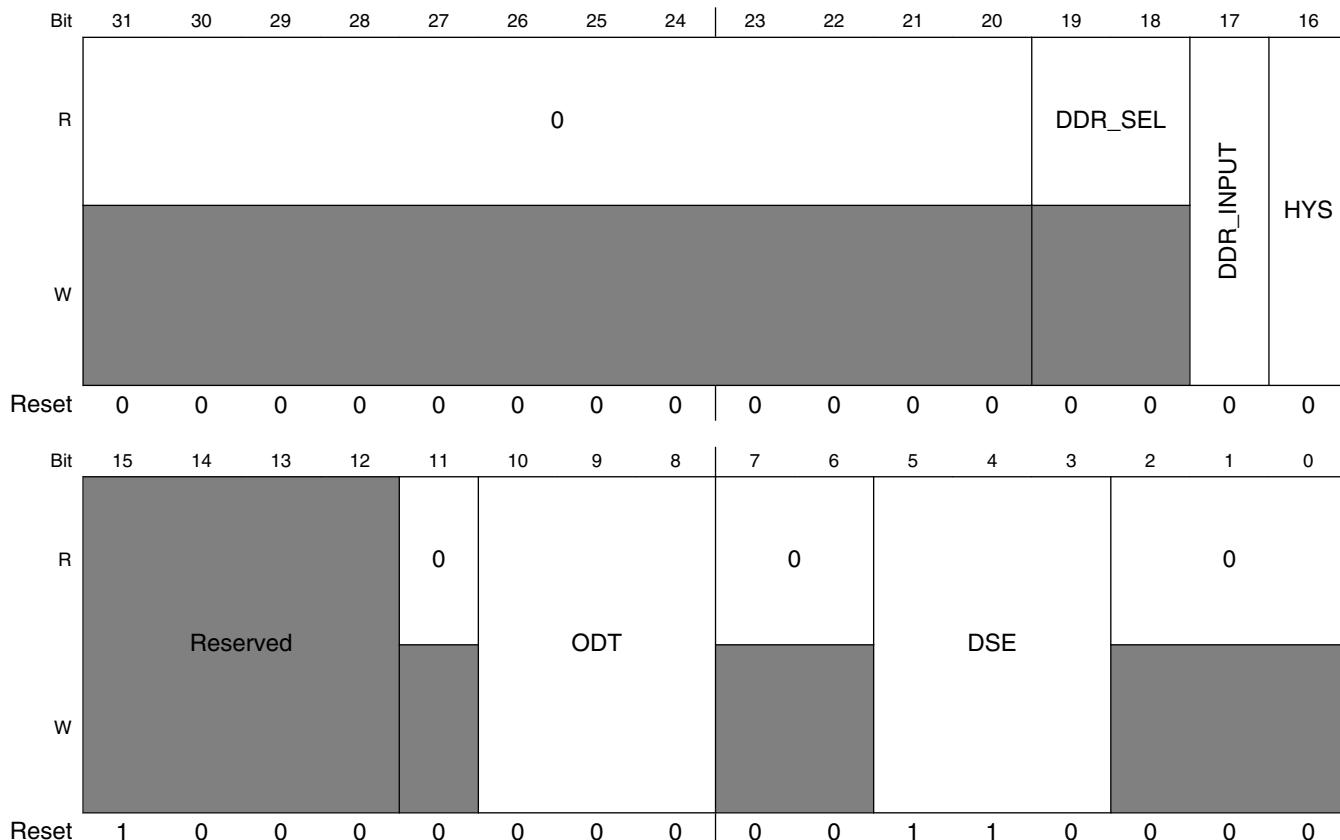
Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS0_P field descriptions (continued)

| Field | Description |
|----------|--|
| | 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.359 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM0)

Address: 20E_0000h base + 5ACh offset = 20E_05ACh

**IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM0 field descriptions**

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_DQMO field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | Note: The value of this field does not reflect the value of the Group Control Register. | | | | | | | | | | | | | | | | |
| 17 DDR_INPUT | <p>DDR / CMOS Input Mode Field</p> <p>Select one of next values for pad: DRAM_DQMO.</p> <p>0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode.</p> | | | | | | | | | | | | | | | | |
| 16 HYS | <p>Hysteresis Enable Field</p> <p>Select one of next values for pad: DRAM_DQMO.</p> <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for pad: DRAM_DQMO.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DRAM_DQMO.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.360 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS1_P)

Address: 20E_0000h base + 5B0h offset = 20E_05B0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|-----------|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | DDR_INPUT | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | | | 0 | |
| | PUS | PUE | PKE | | | ODT | | | | DSE | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS1_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRCODE_CTL |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS1_P field descriptions (continued)

| Field | Description |
|-----------------|--|
| | Note: The value of this field does not reflect the value of the Group Control Register. |
| 16 HYS | Hysteresis Enable Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRHYS Note: The value of this field does not reflect the value of the Group Control Register. |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DRAM_SDQS1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DRAM_SDQS1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DRAM_SDQS1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDQS1. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_SDQS1. 000 HIZ — Hi-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm |

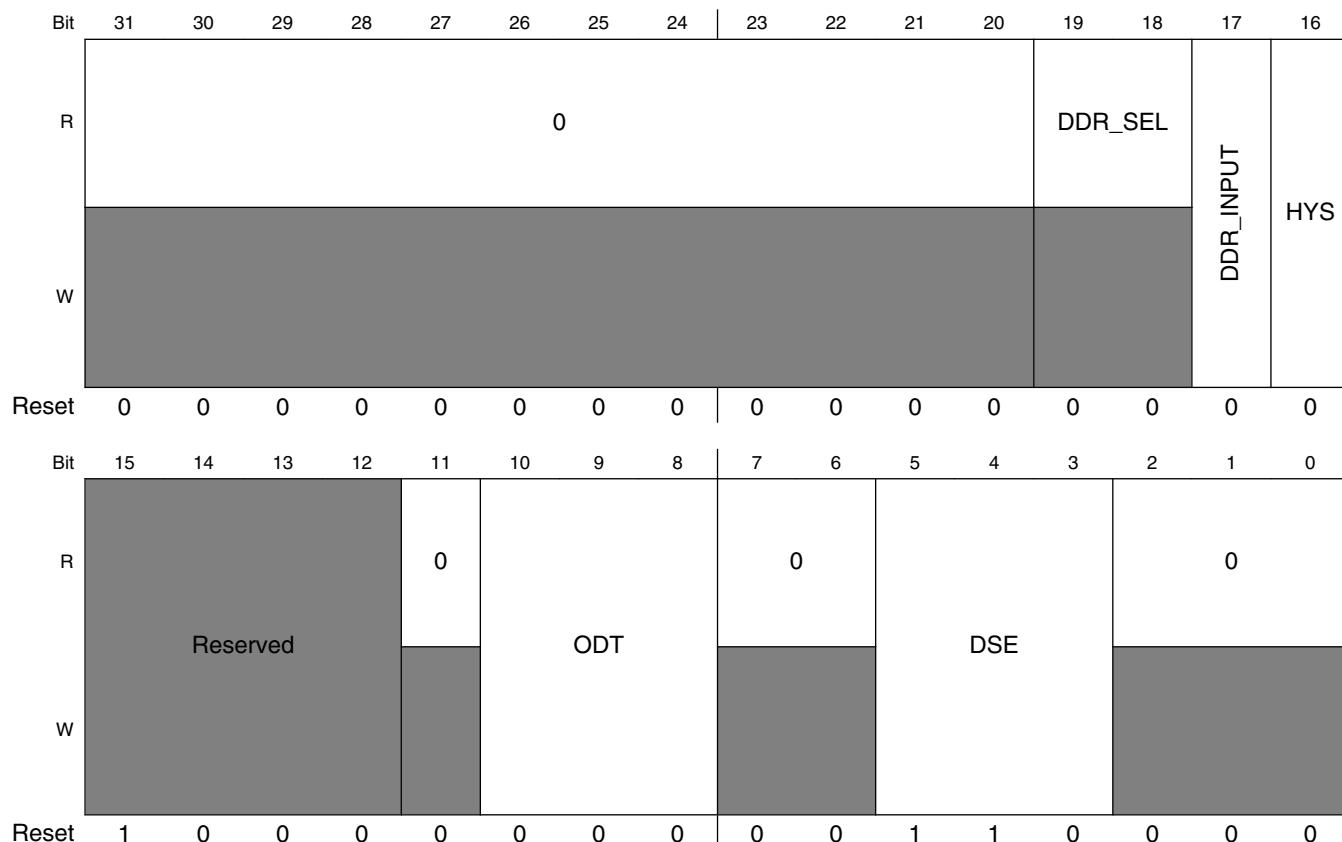
Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS1_P field descriptions (continued)

| Field | Description |
|----------|--|
| | 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.361 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM1)

Address: 20E_0000h base + 5B4h offset = 20E_05B4h

**IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM1 field descriptions**

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM1 field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | Note: The value of this field does not reflect the value of the Group Control Register. | | | | | | | | | | | | | | | | |
| 17 DDR_INPUT | <p>DDR / CMOS Input Mode Field</p> <p>Select one of next values for pad: DRAM_DQM1.</p> <p>0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode.</p> | | | | | | | | | | | | | | | | |
| 16 HYS | <p>Hysteresis Enable Field</p> <p>Select one of next values for pad: DRAM_DQM1.</p> <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for pad: DRAM_DQM1.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DRAM_DQM1.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.362 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS6_P)

Address: 20E_0000h base + 5B8h offset = 20E_05B8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|-----------|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | DDR_INPUT | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | | | 0 | |
| | PUS | PUE | PKE | | | ODT | | | | DSE | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS6_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRCODE_CTL |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS6_P field descriptions (continued)

| Field | Description |
|-----------------|--|
| | Note: The value of this field does not reflect the value of the Group Control Register. |
| 16 HYS | Hysteresis Enable Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRHYS Note: The value of this field does not reflect the value of the Group Control Register. |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DRAM_SDQS6. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DRAM_SDQS6. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DRAM_SDQS6. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDQS6. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_SDQS6. 000 HIZ — Hi-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm |

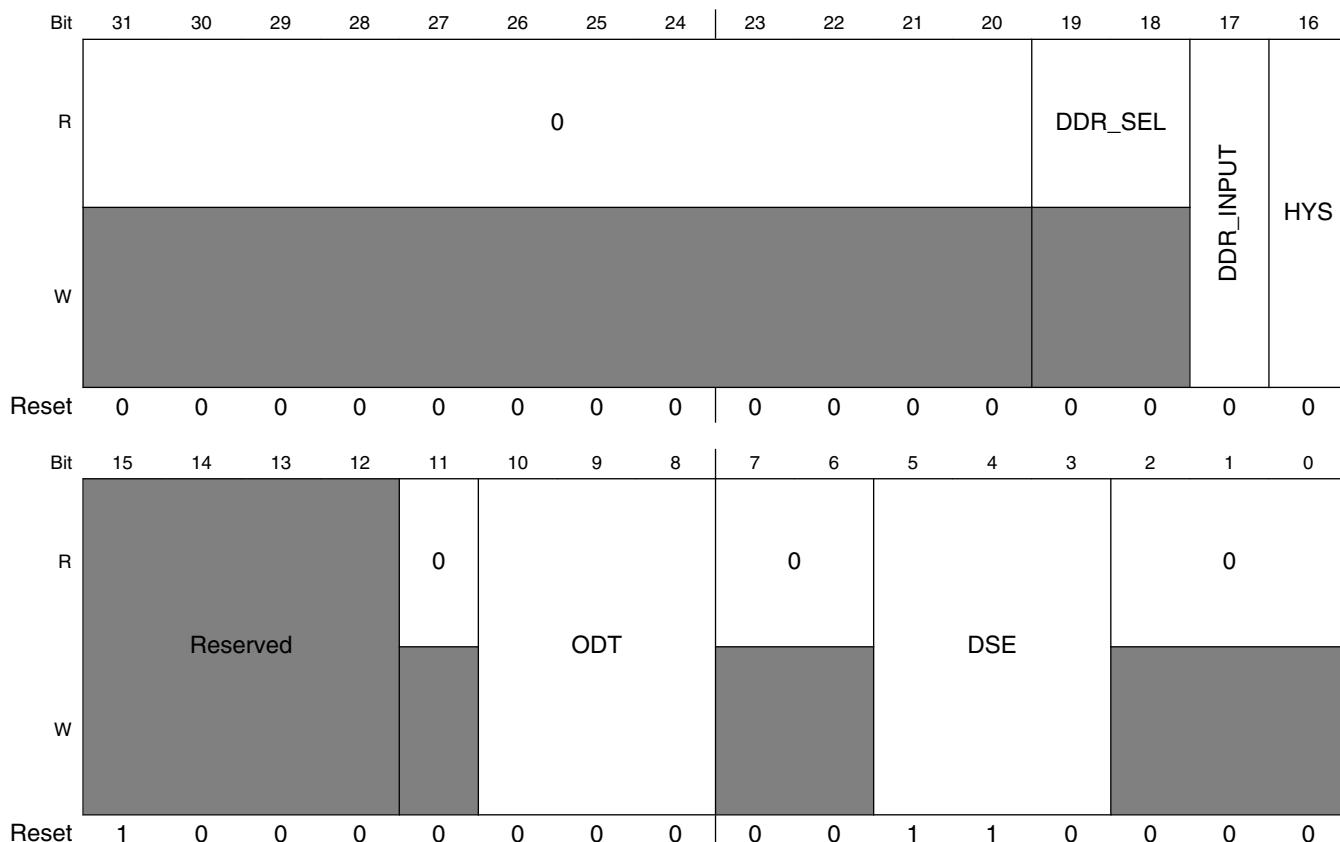
Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS6_P field descriptions (continued)

| Field | Description |
|----------|--|
| | 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.363 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM6)

Address: 20E_0000h base + 5BCh offset = 20E_05BCh

**IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM6 field descriptions**

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM6 field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | Note: The value of this field does not reflect the value of the Group Control Register. | | | | | | | | | | | | | | | | |
| 17 DDR_INPUT | <p>DDR / CMOS Input Mode Field</p> <p>Select one of next values for pad: DRAM_DQM6.</p> <p>0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode.</p> | | | | | | | | | | | | | | | | |
| 16 HYS | <p>Hysteresis Enable Field</p> <p>Select one of next values for pad: DRAM_DQM6.</p> <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for pad: DRAM_DQM6.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DRAM_DQM6.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.364 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS7_P)

Address: 20E_0000h base + 5C0h offset = 20E_05C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|----|----|-----|----|----|----|-----|----|----|---------|----|-----------|-----|
| R | | | | | | | | | 0 | | | | DDR_SEL | | DDR_INPUT | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | 0 | | | | 0 | | | | | | 0 | |
| | PUS | PUE | PKE | | | ODT | | | | DSE | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS7_P field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE Note: The value of this field does not reflect the value of the Group Control Register. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRCODE_CTL |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS7_P field descriptions (continued)

| Field | Description |
|-----------------|--|
| | Note: The value of this field does not reflect the value of the Group Control Register. |
| 16 HYS | Hysteresis Enable Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDRHYS Note: The value of this field does not reflect the value of the Group Control Register. |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: DRAM_SDQS7. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: DRAM_SDQS7. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: DRAM_SDQS7. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for pad: DRAM_SDQS7. 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: DRAM_SDQS7. 000 HIZ — Hi-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm |

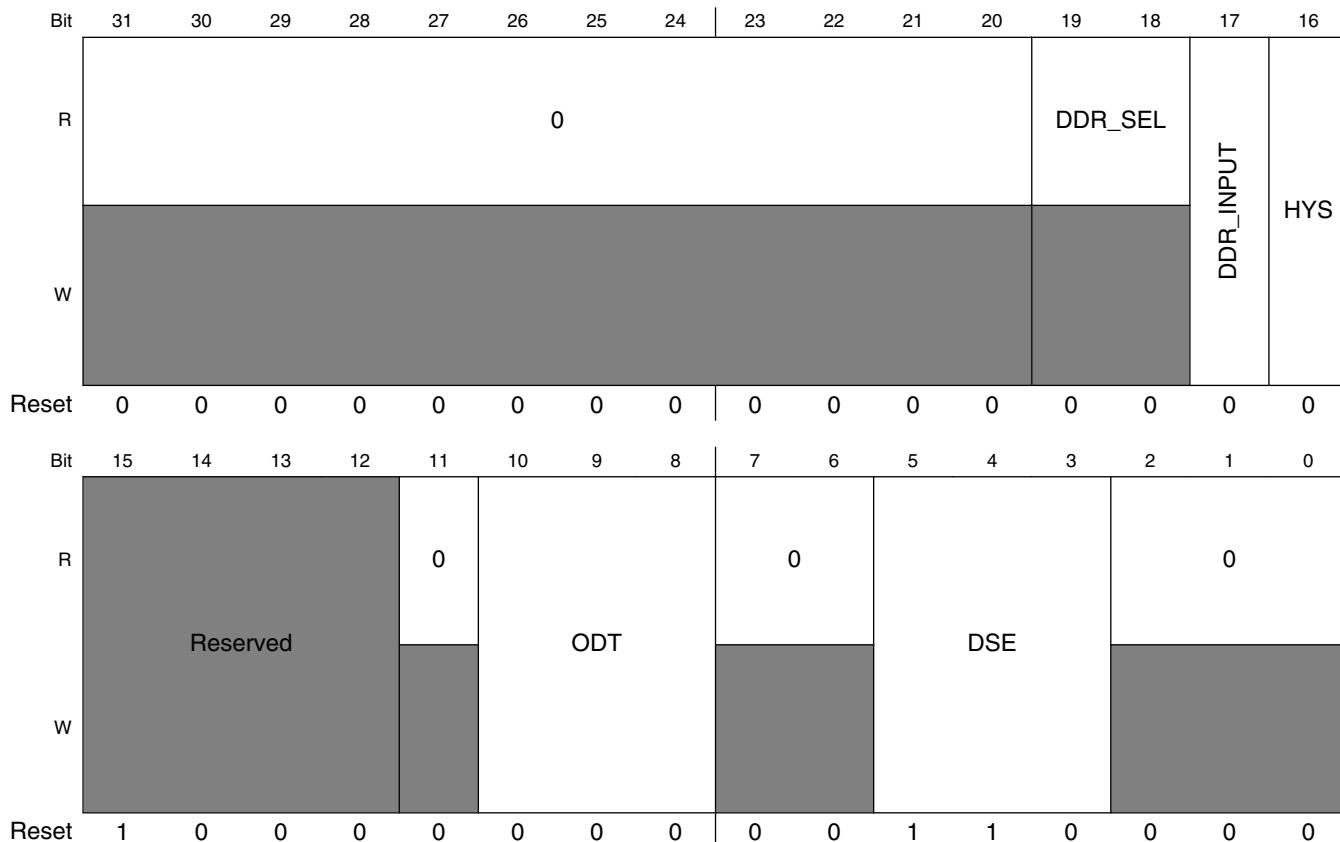
Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS7_P field descriptions (continued)

| Field | Description |
|----------|--|
| | 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.365 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM7)

Address: 20E_0000h base + 5C4h offset = 20E_05C4h

**IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM7 field descriptions**

| Field | Description |
|-------------------|---|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | DDR Select Field This property can be configured using Group Control Register: IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_DRAM_DQM7 field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|-----------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| | Note: The value of this field does not reflect the value of the Group Control Register. | | | | | | | | | | | | | | | | |
| 17 DDR_INPUT | <p>DDR / CMOS Input Mode Field</p> <p>Select one of next values for pad: DRAM_DQM7.</p> <p>0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode.</p> | | | | | | | | | | | | | | | | |
| 16 HYS | <p>Hysteresis Enable Field</p> <p>Select one of next values for pad: DRAM_DQM7.</p> <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> | | | | | | | | | | | | | | | | |
| 15–12 - | This field is reserved. Reserved | | | | | | | | | | | | | | | | |
| 11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for pad: DRAM_DQM7.</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| 7–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: DRAM_DQM7.</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.366 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_COL0)

Address: 20E_0000h base + 5C8h offset = 20E_05C8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_COL0 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_COL0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_COL0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_COL0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_COL0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_COL0 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: KEY_COL0.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.367 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW0)

Address: 20E_0000h base + 5CCh offset = 20E_05CCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW0 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_ROW0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_ROW0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_ROW0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_ROW0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: KEY_ROW0. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW0 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.368 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_COL1)

Address: 20E_0000h base + 5D0h offset = 20E_05D0h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_COL1 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_COL1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_COL1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_COL1 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_COL1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_COL1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: KEY_COL1. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_COL1 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.369 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW1)

Address: 20E_0000h base + 5D4h offset = 20E_05D4h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW1 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_ROW1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_ROW1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_ROW1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_ROW1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW1 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: KEY_ROW1.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.370 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_COL2)

Address: 20E_0000h base + 5D8h offset = 20E_05D8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_COL2 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_COL2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_COL2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_COL2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_COL2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_COL2 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: KEY_COL2.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.371 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW2)

Address: 20E_0000h base + 5DCh offset = 20E_05DCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW2 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_ROW2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_ROW2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_ROW2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_ROW2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: KEY_ROW2. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW2 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

**36.4.372 Pad Control Register
(IOMUXC_SW_PAD_CTL_PAD_KEY_COL3)**

Address: 20E_0000h base + 5E0h offset = 20E_05E0h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_COL3 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_COL3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_COL3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_COL3 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_COL3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_COL3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: KEY_COL3. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_COL3 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.373 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW3)

Address: 20E_0000h base + 5E4h offset = 20E_05E4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW3 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_ROW3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_ROW3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_ROW3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_ROW3. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW3 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: KEY_ROW3.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.374 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_COL4)

Address: 20E_0000h base + 5E8h offset = 20E_05E8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_COL4 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_COL4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_COL4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_COL4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_COL4. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_COL4 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: KEY_COL4.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.375 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_KEY_ROW4)

Address: 20E_0000h base + 5ECh offset = 20E_05ECh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW4 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: KEY_ROW4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: KEY_ROW4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: KEY_ROW4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: KEY_ROW4. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: KEY_ROW4. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_KEY_ROW4 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.376 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO00)

Address: 20E_0000h base + 5F0h offset = 20E_05F0h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO00 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_0. 00 100K_OHM_PD — 100K Ohm Pull Down |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO00 field descriptions (continued)

| Field | Description |
|---------------|---|
| | <p>01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up</p> |
| 13 PUE | <p>Pull / Keep Select Field Select one of next values for pad: GPIO_0.</p> <p>0 KEEP — Keeper Enabled 1 PULL — Pull Enabled</p> |
| 12 PKE | <p>Pull / Keep Enable Field Select one of next values for pad: GPIO_0.</p> <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>Read Only Field The value of this field is fixed and cannot be changed.</p> <p>10 MEDIUM — Medium frequency (100, 150 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: GPIO_0.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO00 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.377 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO01)

Address: 20E_0000h base + 5F4h offset = 20E_05F4h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO01 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO01 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: GPIO_1.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.378 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO09)

Address: 20E_0000h base + 5F8h offset = 20E_05F8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO09 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_9. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_9. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_9. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_9. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO09 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: GPIO_9.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.379 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO03)

Address: 20E_0000h base + 5FCh offset = 20E_05FCh

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO03 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: GPIO_3. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO03 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.380 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO06)

Address: 20E_0000h base + 600h offset = 20E_0600h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO06 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_6. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_6. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO06 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_6. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_6. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: GPIO_6. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO06 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.381 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO02)

Address: 20E_0000h base + 604h offset = 20E_0604h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO02 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_2. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO02 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: GPIO_2.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.382 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO04)

Address: 20E_0000h base + 608h offset = 20E_0608h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO04 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_4. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO04 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: GPIO_4.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.383 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO05)

Address: 20E_0000h base + 60Ch offset = 20E_060Ch

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO05 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_5. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_5. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_5. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_5. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: GPIO_5. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO05 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.384 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO07)

Address: 20E_0000h base + 610h offset = 20E_0610h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO07 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_7. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_7. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO07 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_7. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_7. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: GPIO_7. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO07 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.385 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO08)

Address: 20E_0000h base + 614h offset = 20E_0614h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO08 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_8. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_8. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_8. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_8. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO08 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: GPIO_8.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.386 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO16)

Address: 20E_0000h base + 618h offset = 20E_0618h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO16 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_16. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_16. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_16. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_16. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO16 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: GPIO_16.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.387 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO17)

Address: 20E_0000h base + 61Ch offset = 20E_061Ch

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|-------|--|-----|----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | 0 | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO17 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_17. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_17. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_17. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_17. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. Read Only Field The value of this field is fixed and cannot be changed. 10 MEDIUM — Medium frequency (100, 150 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: GPIO_17. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO17 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

**36.4.388 Pad Control Register
(IOMUXC_SW_PAD_CTL_PAD_GPIO18)**

Address: 20E_0000h base + 620h offset = 20E_0620h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO18 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_18. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_18. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO18 field descriptions (continued)

| Field | Description |
|------------------|---|
| 13 PUE | <p>Pull / Keep Select Field</p> <p>Select one of next values for pad: GPIO_18.</p> <p>0 KEEP — Keeper Enabled 1 PULL — Pull Enabled</p> |
| 12 PKE | <p>Pull / Keep Enable Field</p> <p>Select one of next values for pad: GPIO_18.</p> <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field</p> <p>Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: GPIO_18.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.389 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_GPIO19)

Address: 20E_0000h base + 624h offset = 20E_0624h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_GPIO19 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: GPIO_19. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: GPIO_19. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: GPIO_19. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: GPIO_19. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_GPIO19 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: GPIO_19.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.390 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_PIXCLK)

Address: 20E_0000h base + 628h offset = 20E_0628h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_PIXCLK field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_PIXCLK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_PIXCLK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_PIXCLK. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_PIXCLK. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_PIXCLK. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_PIXCLK field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.391 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_HSYNC)

Address: 20E_0000h base + 62Ch offset = 20E_062Ch

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_HSYNC field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_MCLK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_MCLK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_HSYNC field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_MCLK. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_MCLK. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_MCLK. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_HSYNC field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | |
|-------|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| | 0 SLOW — Slow Slew Rate | | | | | | | | | | | | | | |
| | 1 FAST — Fast Slew Rate | | | | | | | | | | | | | | |

36.4.392 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA_EN)

Address: 20E_0000h base + 630h offset = 20E_0630h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA_EN field descriptions

| Field | Description | | | | | | | | | | | | | | | |
|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DATA_EN. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input | | | | | | | | | | | | | | | |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DATA_EN. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up | | | | | | | | | | | | | | | |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DATA_EN. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled | | | | | | | | | | | | | | | |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DATA_EN. | | | | | | | | | | | | | | | |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA_EN field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: CSI0_DATA_EN.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.393 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_VSYNC)

Address: 20E_0000h base + 634h offset = 20E_0634h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_VSYNC field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_VSYNC. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_VSYNC. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_VSYNC. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_VSYNC. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_VSYNC field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: CSI0_VSYNC.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.394 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA04)

Address: 20E_0000h base + 638h offset = 20E_0638h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA04 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT4. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_DAT4. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA04 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.395 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA05)

Address: 20E_0000h base + 63Ch offset = 20E_063Ch

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA05 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT5. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT5. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA05 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT5. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT5. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_DAT5. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA05 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.396 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA06)

Address: 20E_0000h base + 640h offset = 20E_0640h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA06 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT6. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT6. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT6. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT6. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA06 field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: CSI0_DAT6.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.397 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA07)

Address: 20E_0000h base + 644h offset = 20E_0644h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA07 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT7. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT7. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT7. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT7. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA07 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: CSI0_DAT7.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.398 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA08)

Address: 20E_0000h base + 648h offset = 20E_0648h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA08 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT8. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT8. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT8. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT8. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_DAT8. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA08 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.399 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA09)

Address: 20E_0000h base + 64Ch offset = 20E_064Ch

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA09 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT9. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT9. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA09 field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT9. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT9. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_DAT9. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA09 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.400 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA10)

Address: 20E_0000h base + 650h offset = 20E_0650h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA10 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT10. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT10. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT10. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT10. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA10 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: CSI0_DAT10.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.401 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA11)

Address: 20E_0000h base + 654h offset = 20E_0654h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA11 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT11. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT11. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT11. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT11. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA11 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: CSI0_DAT11.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.402 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA12)

Address: 20E_0000h base + 658h offset = 20E_0658h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA12 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT12. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT12. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT12. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT12. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_DAT12. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA12 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.403 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA13)

Address: 20E_0000h base + 65Ch offset = 20E_065Ch

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA13 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT13. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT13. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA13 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT13. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT13. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_DAT13. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA13 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.404 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA14)

Address: 20E_0000h base + 660h offset = 20E_0660h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA14 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT14. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT14. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT14. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT14. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA14 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: CSI0_DAT14.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.405 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA15)

Address: 20E_0000h base + 664h offset = 20E_0664h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA15 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT15. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT15. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT15. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT15. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA15 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: CSI0_DAT15.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.406 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA16)

Address: 20E_0000h base + 668h offset = 20E_0668h

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA16 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT16. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT16. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT16. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT16. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_DAT16. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA16 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.407 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA17)

Address: 20E_0000h base + 66Ch offset = 20E_066Ch

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA17 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT17. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT17. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA17 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT17. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT17. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: CSI0_DAT17. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA17 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.408 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA18)

Address: 20E_0000h base + 670h offset = 20E_0670h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA18 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT18. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT18. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT18. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT18. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA18 field descriptions (continued)

| Field | Description |
|---------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: CSI0_DAT18.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.409 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA19)

Address: 20E_0000h base + 674h offset = 20E_0674h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA19 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: CSI0_DAT19. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: CSI0_DAT19. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: CSI0_DAT19. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: CSI0_DAT19. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_CSI0_DATA19 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: CSI0_DAT19.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.410 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TMS)

Address: 20E_0000h base + 678h offset = 20E_0678h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|----|-----|-----|----|----|----|--|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_JTAG_TMS field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: JTAG_TMS. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: JTAG_TMS. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Read Only Field The value of this field is fixed and cannot be changed. 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: JTAG_TMS. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. Read Only Field The value of this field is fixed and cannot be changed. 0 DISABLED — Output is CMOS. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field Read Only Field The value of this field is fixed and cannot be changed. 01 50MHZ — Low (50 MHz) |
| 5–3 DSE | Drive Strength Field Read Only Field The value of this field is fixed and cannot be changed. 100 60_OHM — 60 Ohm |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_JTAG_TMS field descriptions (continued)

| Field | Description |
|----------|---|
| 0 SRE | Slew Rate Field Slew rate control. Read Only Field The value of this field is fixed and cannot be changed. 0 SLOW — Slow Slew Rate |

36.4.411 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_MOD)

Address: 20E_0000h base + 67Ch offset = 20E_067Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_JTAG_MOD field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: JTAG_MOD. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: JTAG_MOD. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Read Only Field |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_JTAG_MOD field descriptions (continued)

| Field | Description |
|------------------|--|
| | The value of this field is fixed and cannot be changed. 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: JTAG_MOD. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. Read Only Field The value of this field is fixed and cannot be changed. 0 DISABLED — Output is CMOS. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field Read Only Field The value of this field is fixed and cannot be changed. 01 50MHZ — Low (50 MHz) |
| 5–3 DSE | Drive Strength Field Read Only Field The value of this field is fixed and cannot be changed. 100 60_OHM — 60 Ohm |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. Read Only Field The value of this field is fixed and cannot be changed. 0 SLOW — Slow Slew Rate |

36.4.412 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TRSTB)

Address: 20E_0000h base + 680h offset = 20E_0680h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|-------|----|-----|----|----|----|-----|----|----|-----|
| R | 0 | | | | | | | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | 0 | | SPEED | | DSE | | 0 | | SRE | | | |
| W | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Reset | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_JTAG_TRSTB field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: JTAG_TRSTB. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: JTAG_TRSTB. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Read Only Field The value of this field is fixed and cannot be changed. 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: JTAG_TRSTB. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. Read Only Field |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_JTAG_TRSTB field descriptions (continued)

| Field | Description |
|------------------|---|
| | The value of this field is fixed and cannot be changed. 0 DISABLED — Output is CMOS. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field Read Only Field The value of this field is fixed and cannot be changed. 01 50MHZ — Low (50 MHz) |
| 5–3 DSE | Drive Strength Field Read Only Field The value of this field is fixed and cannot be changed. 100 60_OHM — 60 Ohm |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. Read Only Field The value of this field is fixed and cannot be changed. 0 SLOW — Slow Slew Rate |

36.4.413 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TDI)

Address: 20E_0000h base + 684h offset = 20E_0684h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|-------|----|-----|----|----|----|-----|----|----|-----|
| R | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | 0 | | SPEED | | DSE | | 0 | | SRE | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_JTAG_TDI field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: JTAG_TDI. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: JTAG_TDI. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Read Only Field The value of this field is fixed and cannot be changed. 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: JTAG_TDI. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. Read Only Field The value of this field is fixed and cannot be changed. 0 DISABLED — Output is CMOS. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field Read Only Field The value of this field is fixed and cannot be changed. 01 50MHZ — Low (50 MHz) |
| 5–3 DSE | Drive Strength Field Read Only Field The value of this field is fixed and cannot be changed. 100 60_OHM — 60 Ohm |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_JTAG_TDI field descriptions (continued)

| Field | Description |
|----------|---|
| 0 SRE | Slew Rate Field Slew rate control. Read Only Field The value of this field is fixed and cannot be changed. 0 SLOW — Slow Slew Rate |

36.4.414 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TCK)

Address: 20E_0000h base + 688h offset = 20E_0688h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_JTAG_TCK field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: JTAG_TCK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: JTAG_TCK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Read Only Field |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_JTAG_TCK field descriptions (continued)

| Field | Description |
|------------------|--|
| | The value of this field is fixed and cannot be changed. 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: JTAG_TCK. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. Read Only Field The value of this field is fixed and cannot be changed. 0 DISABLED — Output is CMOS. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field Read Only Field The value of this field is fixed and cannot be changed. 01 50MHZ — Low (50 MHz) |
| 5–3 DSE | Drive Strength Field Read Only Field The value of this field is fixed and cannot be changed. 100 60_OHM — 60 Ohm |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. Read Only Field The value of this field is fixed and cannot be changed. 0 SLOW — Slow Slew Rate |

36.4.415 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_JTAG_TDO)

Address: 20E_0000h base + 68Ch offset = 20E_068Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|-----|----|
| R | 0 | | | | | | | | | | | | | | HYS | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | 0 | | | SPEED | | DSE | | | 0 | SRE | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

IOMUXC_SW_PAD_CTL_PAD_JTAG_TDO field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Read Only Field The value of this field is fixed and cannot be changed. 0 DISABLED — CMOS input |
| 15–14 PUS | Pull Up / Down Config. Field Read Only Field The value of this field is fixed and cannot be changed. 10 100K_OHM_PU — 100K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Read Only Field The value of this field is fixed and cannot be changed. 0 KEEP — Keeper Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: JTAG_TDO. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. Read Only Field The value of this field is fixed and cannot be changed. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_JTAG_TDO field descriptions (continued)

| Field | Description |
|------------------|---|
| 0 | DISABLED — Output is CMOS. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field Read Only Field The value of this field is fixed and cannot be changed. 10 100MHZ — Medium (100 MHz) |
| 5–3 DSE | Drive Strength Field Read Only Field The value of this field is fixed and cannot be changed. 110 40_OHM — 40 Ohm |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. Read Only Field The value of this field is fixed and cannot be changed. 1 FAST — Fast Slew Rate |

36.4.416 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA7)

Address: 20E_0000h base + 690h offset = 20E_0690h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA7 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA7 field descriptions (continued)

| Field | Description |
|------------------|--|
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_DAT7. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_DAT7. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_DAT7. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_DAT7. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD3_DAT7. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA7 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

**36.4.417 Pad Control Register
(IOMUXC_SW_PAD_CTL_PAD_SD3_DATA6)**

Address: 20E_0000h base + 694h offset = 20E_0694h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA6 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_DAT6. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_DAT6. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA6 field descriptions (continued)

| Field | Description |
|------------------|--|
| 13 PUE | <p>Pull / Keep Select Field</p> <p>Select one of next values for pad: SD3_DAT6.</p> <p>0 KEEP — Keeper Enabled 1 PULL — Pull Enabled</p> |
| 12 PKE | <p>Pull / Keep Enable Field</p> <p>Select one of next values for pad: SD3_DAT6.</p> <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field</p> <p>Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: SD3_DAT6.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.418 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA5)

Address: 20E_0000h base + 698h offset = 20E_0698h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA5 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_DAT5. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_DAT5. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_DAT5. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_DAT5. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA5 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: SD3_DAT5.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.419 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA4)

Address: 20E_0000h base + 69Ch offset = 20E_069Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA4 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_DAT4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_DAT4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_DAT4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_DAT4. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD3_DAT4. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA4 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.420 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_CMD)

Address: 20E_0000h base + 6A0h offset = 20E_06A0h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_CMD field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_CMD. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_CMD. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_CMD field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_CMD. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_CMD. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD3_CMD. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_CMD field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.421 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_CLK)

Address: 20E_0000h base + 6A4h offset = 20E_06A4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_CLK field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_CLK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_CLK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_CLK. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_CLK. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_CLK field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: SD3_CLK.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.422 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA0)

Address: 20E_0000h base + 6A8h offset = 20E_06A8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA0 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_DAT0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_DAT0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_DAT0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_DAT0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA0 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: SD3_DAT0.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.423 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA1)

Address: 20E_0000h base + 6ACh offset = 20E_06ACh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA1 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_DAT1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_DAT1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_DAT1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_DAT1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD3_DAT1. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA1 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.424 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA2)

Address: 20E_0000h base + 6B0h offset = 20E_06B0h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA2 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_DAT2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_DAT2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA2 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_DAT2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_DAT2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD3_DAT2. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA2 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.425 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_DATA3)

Address: 20E_0000h base + 6B4h offset = 20E_06B4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA3 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_DAT3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_DAT3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_DAT3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_DAT3. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_DATA3 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: SD3_DAT3.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.426 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD3_RESET)

Address: 20E_0000h base + 6B8h offset = 20E_06B8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD3_RESET field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD3_RST. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD3_RST. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD3_RST. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD3_RST. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD3_RESET field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: SD3_RST.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.427 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CLE)

Address: 20E_0000h base + 6BCh offset = 20E_06BCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_CLE field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_CLE. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_CLE. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_CLE. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_CLE. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: NANDF_CLE. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_CLE field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.428 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_ALE)

Address: 20E_0000h base + 6C0h offset = 20E_06C0h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_ALE field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_ALE. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_ALE. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_ALE field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_ALE. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_ALE. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: NANDF_ALE. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_ALE field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.429 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_WP_B)

Address: 20E_0000h base + 6C4h offset = 20E_06C4h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_WP_B field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_WP_B. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_WP_B. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_WP_B. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_WP_B. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_WP_B field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: NANDF_WP_B.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.430 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_READY_B)

Address: 20E_0000h base + 6C8h offset = 20E_06C8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_READY_B field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_RB0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_RB0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_RB0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_RB0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_READY_B field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: NANDF_RB0.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.431 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CS0_B)

Address: 20E_0000h base + 6CCh offset = 20E_06CCh

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_CS0_B field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_CS0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_CS0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_CS0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_CS0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: NANDF_CS0. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_CS0_B field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.432 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CS1_B)

Address: 20E_0000h base + 6D0h offset = 20E_06D0h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_CS1_B field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_CS1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_CS1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_CS1_B field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_CS1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_CS1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: NANDF_CS1. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_CS1_B field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.433 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CS2_B)

Address: 20E_0000h base + 6D4h offset = 20E_06D4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_CS2_B field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_CS2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_CS2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_CS2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_CS2. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_CS2_B field descriptions (continued)

| Field | Description |
|------------------|--|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: NANDF_CS2.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.434 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_CS3_B)

Address: 20E_0000h base + 6D8h offset = 20E_06D8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_CS3_B field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_CS3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_CS3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_CS3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_CS3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_CS3_B field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: NANDF_CS3.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.435 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_CMD)

Address: 20E_0000h base + 6DCh offset = 20E_06DCh

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_CMD field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_CMD. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_CMD. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_CMD. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_CMD. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD4_CMD. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_CMD field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.436 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_CLK)

Address: 20E_0000h base + 6E0h offset = 20E_06E0h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_CLK field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_CLK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_CLK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_CLK field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_CLK. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_CLK. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD4_CLK. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_CLK field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.437 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA00)

Address: 20E_0000h base + 6E4h offset = 20E_06E4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA00 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_D0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_D0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_D0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_D0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA00 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: NANDF_D0.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.438 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA01)

Address: 20E_0000h base + 6E8h offset = 20E_06E8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA01 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_D1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_D1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_D1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_D1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA01 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: NANDF_D1.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.439 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA02)

Address: 20E_0000h base + 6ECH offset = 20E_06ECH

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA02 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_D2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_D2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_D2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_D2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: NANDF_D2. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA02 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.440 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA03)

Address: 20E_0000h base + 6F0h offset = 20E_06F0h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA03 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_D3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_D3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA03 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_D3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_D3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: NANDF_D3. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA03 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.441 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA04)

Address: 20E_0000h base + 6F4h offset = 20E_06F4h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|--|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA04 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_D4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_D4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_D4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_D4. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA04 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: NANDF_D4.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.442 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA05)

Address: 20E_0000h base + 6F8h offset = 20E_06F8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA05 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_D5. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_D5. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_D5. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_D5. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA05 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: NANDF_D5.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.443 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA06)

Address: 20E_0000h base + 6FCh offset = 20E_06FCh

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA06 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_D6. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_D6. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_D6. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_D6. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: NANDF_D6. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA06 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.444 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_NAND_DATA07)

Address: 20E_0000h base + 700h offset = 20E_0700h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA07 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: NANDF_D7. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: NANDF_D7. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA07 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: NANDF_D7. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: NANDF_D7. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: NANDF_D7. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_NAND_DATA07 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.445 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA0)

Address: 20E_0000h base + 704h offset = 20E_0704h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA0 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_DAT0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_DAT0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_DAT0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_DAT0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA0 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: SD4_DAT0.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.446 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA1)

Address: 20E_0000h base + 708h offset = 20E_0708h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA1 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_DAT1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_DAT1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_DAT1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_DAT1. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA1 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: SD4_DAT1.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.447 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA2)

Address: 20E_0000h base + 70Ch offset = 20E_070Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA2 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_DAT2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_DAT2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_DAT2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_DAT2. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD4_DAT2. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA2 field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

**36.4.448 Pad Control Register
(IOMUXC_SW_PAD_CTL_PAD_SD4_DATA3)**

Address: 20E_0000h base + 710h offset = 20E_0710h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA3 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_DAT3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_DAT3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA3 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_DAT3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_DAT3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD4_DAT3. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA3 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.449 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA4)

Address: 20E_0000h base + 714h offset = 20E_0714h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA4 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_DAT4. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_DAT4. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_DAT4. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_DAT4. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA4 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: SD4_DAT4.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.450 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA5)

Address: 20E_0000h base + 718h offset = 20E_0718h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA5 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_DAT5. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_DAT5. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_DAT5. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_DAT5. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA5 field descriptions (continued)

| Field | Description |
|------------------|--|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: SD4_DAT5.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.451 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA6)

Address: 20E_0000h base + 71Ch offset = 20E_071Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA6 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_DAT6. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_DAT6. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_DAT6. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_DAT6. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD4_DAT6. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA6 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.452 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD4_DATA7)

Address: 20E_0000h base + 720h offset = 20E_0720h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA7 field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD4_DAT7. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD4_DAT7. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA7 field descriptions (continued)

| Field | Description |
|------------------|--|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD4_DAT7. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD4_DAT7. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD4_DAT7. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD4_DATA7 field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.453 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_DATA1)

Address: 20E_0000h base + 724h offset = 20E_0724h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD1_DATA1 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD1_DAT1. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD1_DAT1. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD1_DAT1. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD1_DAT1. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD1_DATA1 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: SD1_DAT1.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.454 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_DATA0)

Address: 20E_0000h base + 728h offset = 20E_0728h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD1_DATA0 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD1_DAT0. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD1_DAT0. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD1_DAT0. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD1_DAT0. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD1_DATA0 field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: SD1_DAT0.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.455 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_DATA3)

Address: 20E_0000h base + 72Ch offset = 20E_072Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|-----|-----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD1_DATA3 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD1_DAT3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD1_DAT3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD1_DAT3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD1_DAT3. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD1_DAT3. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD1_DATA3 field descriptions (continued)

| Field | Description |
|-----------------|---|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.456 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_CMD)

Address: 20E_0000h base + 730h offset = 20E_0730h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | | | SRE |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD1_CMD field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD1_CMD. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD1_CMD. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD1_CMD field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD1_CMD. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD1_CMD. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD1_CMD. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD1_CMD field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.457 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_DATA2)

Address: 20E_0000h base + 734h offset = 20E_0734h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD1_DATA2 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD1_DAT2. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD1_DAT2. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD1_DAT2. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD1_DAT2. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD1_DATA2 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: SD1_DAT2.</p> <p>000 HIZ — Hi-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.458 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD1_CLK)

Address: 20E_0000h base + 738h offset = 20E_0738h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | SRE | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD1_CLK field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD1_CLK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD1_CLK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD1_CLK. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD1_CLK. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD1_CLK field descriptions (continued)

| Field | Description |
|------------------|---|
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field</p> <p>The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for pad: SD1_CLK.</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field</p> <p>Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <ul style="list-style-type: none"> 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.459 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_CLK)

Address: 20E_0000h base + 73Ch offset = 20E_073Ch

| | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|----|----|----|----|-------|----|-----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | HYS |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | | SPEED | | DSE | | 0 | | | SRE |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD2_CLK field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD2_CLK. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD2_CLK. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD2_CLK. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD2_CLK. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD2_CLK. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD2_CLK field descriptions (continued)

| Field | Description |
|-----------------|--|
| | 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate |

36.4.460 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_CMD)

Address: 20E_0000h base + 740h offset = 20E_0740h

| | | | | | | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|-----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | OKE | ODE | 0 | | | SPEED | | DSE | | 0 | | SRE | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD2_CMD field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD2_CMD. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD2_CMD. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD2_CMD field descriptions (continued)

| Field | Description |
|------------------|---|
| | 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD2_CMD. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD2_CMD. 0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled |
| 11 ODE | Open Drain Enable Field Enables open drain of the pin. 0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain. |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. 00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz) |
| 5–3 DSE | Drive Strength Field Select one of next values for pad: SD2_CMD. 000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD2_CMD field descriptions (continued)

| Field | Description |
|-------|--------------------------------|
| | 0 SLOW — Slow Slew Rate |
| | 1 FAST — Fast Slew Rate |

36.4.461 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_SD2_DATA3)

Address: 20E_0000h base + 744h offset = 20E_0744h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|-----|-----|-----|----|----|----|-------|----|-----|----|----|----|----|-----|-----|
| R | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | PUS | PUE | PKE | ODE | | 0 | | SPEED | | DSE | | 0 | | | SRE | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_PAD_SD2_DATA3 field descriptions

| Field | Description |
|-------------------|--|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | Hysteresis Enable Field Select one of next values for pad: SD2_DAT3. 0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input |
| 15–14 PUS | Pull Up / Down Config. Field Select one of next values for pad: SD2_DAT3. 00 100K_OHM_PD — 100K Ohm Pull Down 01 47K_OHM_PU — 47K Ohm Pull Up 10 100K_OHM_PU — 100K Ohm Pull Up 11 22K_OHM_PU — 22K Ohm Pull Up |
| 13 PUE | Pull / Keep Select Field Select one of next values for pad: SD2_DAT3. 0 KEEP — Keeper Enabled 1 PULL — Pull Enabled |
| 12 PKE | Pull / Keep Enable Field Select one of next values for pad: SD2_DAT3. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_SD2_DATA3 field descriptions (continued)

| Field | Description |
|------------------|---|
| | <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| 11 ODE | <p>Open Drain Enable Field Enables open drain of the pin.</p> <p>0 DISABLED — Output is CMOS. 1 ENABLED — Output is Open Drain.</p> |
| 10–8 Reserved | This read-only field is reserved and always has the value 0. |
| 7–6 SPEED | <p>Speed Field The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>00 LOW — Low frequency (50 MHz) 01 MEDIUM — Medium frequency (100, 150 MHz) 10 MEDIUM — Medium frequency (100, 150 MHz) 11 MAXIMUM — Maximum frequency (100, 150, 200 MHz)</p> |
| 5–3 DSE | <p>Drive Strength Field Select one of next values for pad: SD2_DAT3.</p> <p>000 HIZ — HI-Z 001 260_OHM — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 130_OHM — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 90_OHM — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V 100 60_OHM — 37 Ohm @ 3.3V, 60 Ohm @ 1.8V 101 50_OHM — 30 Ohm @ 3.3V, 50 Ohm @ 1.8V 110 40_OHM — 25 Ohm @ 3.3V, 40 Ohm @ 1.8V 111 33_OHM — 20 Ohm @ 3.3V, 33 Ohm @ 1.8V</p> |
| 2–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 SRE | <p>Slew Rate Field Slew rate control. The operational frequency on GPIO pads is dependent on slew rate (SRE), speed (SPEED), and supply voltage (OVDD). Please see for more details.</p> <p>0 SLOW — Slow Slew Rate 1 FAST — Fast Slew Rate</p> |

36.4.462 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B7DS)

Address: 20E_0000h base + 748h offset = 20E_0748h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |

IOMUXC_SW_PAD_CTL_GRP_B7DS field descriptions

| Field | Description |
|------------------|--|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for group: Affected pads: DRAM_DATA56, DRAM_DATA57, DRAM_DATA58, DRAM_DATA59, DRAM_DATA60, DRAM_DATA61, DRAM_DATA62, DRAM_DATA63 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHMHM — 60 Ohm 101 48_OHMHM — 48 Ohm 110 40_OHMHM — 40 Ohm 111 34_OHMHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.463 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_ADDDS)

Address: 20E_0000h base + 74Ch offset = 20E_074Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |

IOMUXC_SW_PAD_CTL_GRP_ADDDS field descriptions

| Field | Description |
|------------------|--|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_ADDDS field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|------------|--|-----|-------------------|-----|--------------------------|-----|--------------------------|-----|------------------------|-----|------------------------|-----|------------------------|-----|------------------------|-----|------------------------|
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_ADDR00, DRAM_ADDR01, DRAM_ADDR02, DRAM_ADDR03, DRAM_ADDR04, DRAM_ADDR05, DRAM_ADDR06, DRAM_ADDR07, DRAM_ADDR08, DRAM_ADDR09, DRAM_ADDR10, DRAM_ADDR11, DRAM_ADDR12, DRAM_ADDR13, DRAM_ADDR14, DRAM_ADDR15, DRAM_SDBA0, DRAM_SDBA1</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.464 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRMODE_CTL)

Address: 20E_0000h base + 750h offset = 20E_0750h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|
| R | | | | | | | | | 0 | | | | | | DDR_INPUT | 0 |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_GRP_DDRMODE_CTL field descriptions

| Field | Description |
|-------------------|--|
| 31–18 Reserved | This read-only field is reserved and always has the value 0. |
| 17 DDR_INPUT | DDR / CMOS Input Mode Field |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_DDRMODE_CTL field descriptions (continued)

| Field | Description |
|----------|---|
| | Select one of next values for group: . Affected pads: DRAM_SDQS0_P, DRAM_SDQS1_P, DRAM_SDQS2_P, DRAM_SDQS3_P, DRAM_SDQS4_P, DRAM_SDQS5_P, DRAM_SDQS6_P, DRAM_SDQS7_P 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.465 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL0)

Address: 20E_0000h base + 754h offset = 20E_0754h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|-----|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | ODT | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL0 field descriptions

| Field | Description |
|-------------------|---|
| 31–11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for group: . Affected pads: DRAM_DATA00, DRAM_DATA01, DRAM_DATA02, DRAM_DATA03, DRAM_DATA04, DRAM_DATA05, DRAM_DATA06, DRAM_DATA07 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHMHM — 30 Ohm ODT 101 24_OHMHM — 24 Ohm ODT 110 20_OHMHM — 20 Ohm ODT 111 17_OHMHM — 17 Ohm ODT |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.466 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRPKE)

Address: 20E_0000h base + 758h offset = 20E_0758h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | |
|-------|----|----|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|
| R | 0 | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| R | 0 | | PKE | | 0 | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

IOMUXC_SW_PAD_CTL_GRP_DDRPKE field descriptions

| Field | Description |
|-------------------|---|
| 31–13 Reserved | This read-only field is reserved and always has the value 0. |
| 12 PKE | <p>Pull / Keep Enable Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA00, DRAM_DATA01, DRAM_DATA02, DRAM_DATA03, DRAM_DATA04, DRAM_DATA05, DRAM_DATA06, DRAM_DATA07, DRAM_DATA08, DRAM_DATA09, DRAM_DATA10, DRAM_DATA11, DRAM_DATA12, DRAM_DATA13, DRAM_DATA14, DRAM_DATA15, DRAM_DATA16, DRAM_DATA17, DRAM_DATA18, DRAM_DATA19, DRAM_DATA20, DRAM_DATA21, DRAM_DATA22, DRAM_DATA23, DRAM_DATA24, DRAM_DATA25, DRAM_DATA26, DRAM_DATA27, DRAM_DATA28, DRAM_DATA29, DRAM_DATA30, DRAM_DATA31, DRAM_DATA32, DRAM_DATA33, DRAM_DATA34, DRAM_DATA35, DRAM_DATA36, DRAM_DATA37, DRAM_DATA38, DRAM_DATA39, DRAM_DATA40, DRAM_DATA41, DRAM_DATA42, DRAM_DATA43, DRAM_DATA44, DRAM_DATA45, DRAM_DATA46, DRAM_DATA47, DRAM_DATA48, DRAM_DATA49, DRAM_DATA50, DRAM_DATA51, DRAM_DATA52, DRAM_DATA53, DRAM_DATA54, DRAM_DATA55, DRAM_DATA56, DRAM_DATA57, DRAM_DATA58, DRAM_DATA59, DRAM_DATA60, DRAM_DATA61, DRAM_DATA62, DRAM_DATA63</p> <p>0 DISABLED — Pull/Keeper Disabled 1 ENABLED — Pull/Keeper Enabled</p> |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.467 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL1)

Address: 20E_0000h base + 75Ch offset = 20E_075Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R | 0 | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL1 field descriptions

| Field | Description | | | | | | | | | | | | | | | | |
|-------------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| 31–11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA08, DRAM_DATA09, DRAM_DATA10, DRAM_DATA11, DRAM_DATA12, DRAM_DATA13, DRAM_DATA14, DRAM_DATA15</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.468 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL2)

Address: 20E_0000h base + 760h offset = 20E_0760h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL2 field descriptions

| Field | Description | | | | | | | | | | | | |
|-------------------|---|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| 31–11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA16, DRAM_DATA17, DRAM_DATA18, DRAM_DATA19, DRAM_DATA20, DRAM_DATA21, DRAM_DATA22, DRAM_DATA23</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL2 field descriptions (continued)

| Field | Description |
|----------|--|
| | 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.469 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL3)

Address: 20E_0000h base + 764h offset = 20E_0764h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| R | | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL3 field descriptions

| Field | Description |
|-------------------|---|
| 31–11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for group: . Affected pads: DRAM_DATA24, DRAM_DATA25, DRAM_DATA26, DRAM_DATA27, DRAM_DATA28, DRAM_DATA29, DRAM_DATA30, DRAM_DATA31 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.470 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRPK)

Address: 20E_0000h base + 768h offset = 20E_0768h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | PUE | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_GRP_DDRPK field descriptions

| Field | Description |
|-------------------|---|
| 31–14 Reserved | This read-only field is reserved and always has the value 0. |
| 13 PUE | <p>Pull / Keep Select Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA00, DRAM_DATA01, DRAM_DATA02, DRAM_DATA03, DRAM_DATA04, DRAM_DATA05, DRAM_DATA06, DRAM_DATA07, DRAM_DATA08, DRAM_DATA09, DRAM_DATA10, DRAM_DATA11, DRAM_DATA12, DRAM_DATA13, DRAM_DATA14, DRAM_DATA15, DRAM_DATA16, DRAM_DATA17, DRAM_DATA18, DRAM_DATA19, DRAM_DATA20, DRAM_DATA21, DRAM_DATA22, DRAM_DATA23, DRAM_DATA24, DRAM_DATA25, DRAM_DATA26, DRAM_DATA27, DRAM_DATA28, DRAM_DATA29, DRAM_DATA30, DRAM_DATA31, DRAM_DATA32, DRAM_DATA33, DRAM_DATA34, DRAM_DATA35, DRAM_DATA36, DRAM_DATA37, DRAM_DATA38, DRAM_DATA39, DRAM_DATA40, DRAM_DATA41, DRAM_DATA42, DRAM_DATA43, DRAM_DATA44, DRAM_DATA45, DRAM_DATA46, DRAM_DATA47, DRAM_DATA48, DRAM_DATA49, DRAM_DATA50, DRAM_DATA51, DRAM_DATA52, DRAM_DATA53, DRAM_DATA54, DRAM_DATA55, DRAM_DATA56, DRAM_DATA57, DRAM_DATA58, DRAM_DATA59, DRAM_DATA60, DRAM_DATA61, DRAM_DATA62, DRAM_DATA63</p> <p>0 KEEP — Keeper Enabled 1 PULL — Pull Enabled</p> |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.471 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL4)

Address: 20E_0000h base + 76Ch offset = 20E_076Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL4 field descriptions

| Field | Description | | | | | | | | | | | | | | | | |
|-------------------|---|-----|----------------------------|-----|------------------------------|-----|-----------------------------|-----|-----------------------------|-----|-----------------------------|-----|-----------------------------|-----|-----------------------------|-----|-----------------------------|
| 31–11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA32, DRAM_DATA33, DRAM_DATA34, DRAM_DATA35, DRAM_DATA36, DRAM_DATA37, DRAM_DATA38, DRAM_DATA39</p> <table> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHMM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHMM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHMM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHMM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHMM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHMM — 17 Ohm ODT</td></tr> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHMM — 60 Ohm ODT | 011 | 40_OHMM — 40 Ohm ODT | 100 | 30_OHMM — 30 Ohm ODT | 101 | 24_OHMM — 24 Ohm ODT | 110 | 20_OHMM — 20 Ohm ODT | 111 | 17_OHMM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHMM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHMM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHMM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHMM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHMM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHMM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.472 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRHYS)

Address: 20E_0000h base + 770h offset = 20E_0770h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|-----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | HYS |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_GRP_DDRHYS field descriptions

| Field | Description |
|-------------------|---|
| 31–17 Reserved | This read-only field is reserved and always has the value 0. |
| 16 HYS | <p>Hysteresis Enable Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA00, DRAM_DATA01, DRAM_DATA02, DRAM_DATA03, DRAM_DATA04, DRAM_DATA05, DRAM_DATA06, DRAM_DATA07, DRAM_DATA08, DRAM_DATA09, DRAM_DATA10, DRAM_DATA11, DRAM_DATA12, DRAM_DATA13, DRAM_DATA14, DRAM_DATA15, DRAM_DATA16, DRAM_DATA17, DRAM_DATA18, DRAM_DATA19, DRAM_DATA20, DRAM_DATA21, DRAM_DATA22, DRAM_DATA23, DRAM_DATA24, DRAM_DATA25, DRAM_DATA26, DRAM_DATA27, DRAM_DATA28, DRAM_DATA29, DRAM_DATA30, DRAM_DATA31, DRAM_DATA32, DRAM_DATA33, DRAM_DATA34,</p> |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_DDRHYS field descriptions (continued)

| Field | Description |
|----------|---|
| | <p>DRAM_DATA35, DRAM_DATA36, DRAM_DATA37, DRAM_DATA38, DRAM_DATA39, DRAM_DATA40, DRAM_DATA41, DRAM_DATA42, DRAM_DATA43, DRAM_DATA44, DRAM_DATA45, DRAM_DATA46, DRAM_DATA47, DRAM_DATA48, DRAM_DATA49, DRAM_DATA50, DRAM_DATA51, DRAM_DATA52, DRAM_DATA53, DRAM_DATA54, DRAM_DATA55, DRAM_DATA56, DRAM_DATA57, DRAM_DATA58, DRAM_DATA59, DRAM_DATA60, DRAM_DATA61, DRAM_DATA62, DRAM_DATA63, DRAM_SDQS0_P, DRAM_SDQS1_P, DRAM_SDQS2_P, DRAM_SDQS3_P, DRAM_SDQS4_P, DRAM_SDQS5_P, DRAM_SDQS6_P, DRAM_SDQS7_P</p> <p>0 DISABLED — CMOS input 1 ENABLED — Schmitt trigger input</p> |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.473 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDRMODE)

Address: 20E_0000h base + 774h offset = 20E_0774h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|
| R | | | | | | | | | 0 | | | | | | | 0 |
| W | | | | | | | | | | | | | | | | DDR_INPUT |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_GRP_DDRMODE field descriptions

| Field | Description |
|-------------------|---|
| 31–18 Reserved | This read-only field is reserved and always has the value 0. |
| 17 DDR_INPUT | <p>DDR / CMOS Input Mode Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA00, DRAM_DATA01, DRAM_DATA02, DRAM_DATA03, DRAM_DATA04, DRAM_DATA05, DRAM_DATA06, DRAM_DATA07, DRAM_DATA08, DRAM_DATA09, DRAM_DATA10, DRAM_DATA11, DRAM_DATA12, DRAM_DATA13, DRAM_DATA14, DRAM_DATA15, DRAM_DATA16, DRAM_DATA17, DRAM_DATA18, DRAM_DATA19, DRAM_DATA20, DRAM_DATA21, DRAM_DATA22, DRAM_DATA23, DRAM_DATA24, DRAM_DATA25, DRAM_DATA26, DRAM_DATA27, DRAM_DATA28, DRAM_DATA29, DRAM_DATA30, DRAM_DATA31, DRAM_DATA32, DRAM_DATA33, DRAM_DATA34,</p> |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_DDRMODE field descriptions (continued)

| Field | Description |
|----------|---|
| | DRAM_DATA35, DRAM_DATA36, DRAM_DATA37, DRAM_DATA38, DRAM_DATA39, DRAM_DATA40, DRAM_DATA41, DRAM_DATA42, DRAM_DATA43, DRAM_DATA44, DRAM_DATA45, DRAM_DATA46, DRAM_DATA47, DRAM_DATA48, DRAM_DATA49, DRAM_DATA50, DRAM_DATA51, DRAM_DATA52, DRAM_DATA53, DRAM_DATA54, DRAM_DATA55, DRAM_DATA56, DRAM_DATA57, DRAM_DATA58, DRAM_DATA59, DRAM_DATA60, DRAM_DATA61, DRAM_DATA62, DRAM_DATA63 0 CMOS — CMOS input mode. 1 DIFFERENTIAL — Differential input mode. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.474 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL5)

Address: 20E_0000h base + 778h offset = 20E_0778h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| R | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL5 field descriptions

| Field | Description |
|-------------------|---|
| 31–11 Reserved | This read-only field is reserved and always has the value 0. |
| 10–8 ODT | On Die Termination Field Select one of next values for group: . Affected pads: DRAM_DATA40, DRAM_DATA41, DRAM_DATA42, DRAM_DATA43, DRAM_DATA44, DRAM_DATA45, DRAM_DATA46, DRAM_DATA47 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHMF — 60 Ohm ODT 011 40_OHMF — 40 Ohm ODT 100 30_OHMF — 30 Ohm ODT 101 24_OHMF — 24 Ohm ODT 110 20_OHMF — 20 Ohm ODT 111 17_OHMF — 17 Ohm ODT |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.475 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL6)

Address: 20E_0000h base + 77Ch offset = 20E_077Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL6 field descriptions

| Field | Description | | | | | | | | | | | | | | | | |
|-------------------|--|-----|----------------------------|-----|------------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|-----|----------------------------|
| 31–11 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for group:</p> <p>Affected pads: DRAM_DATA48, DRAM_DATA49, DRAM_DATA50, DRAM_DATA51, DRAM_DATA52, DRAM_DATA53, DRAM_DATA54, DRAM_DATA55</p> <table> <tbody> <tr><td>000</td><td>DISABLED — Disabled</td></tr> <tr><td>001</td><td>120_OHM — 120 Ohm ODT</td></tr> <tr><td>010</td><td>60_OHM — 60 Ohm ODT</td></tr> <tr><td>011</td><td>40_OHM — 40 Ohm ODT</td></tr> <tr><td>100</td><td>30_OHM — 30 Ohm ODT</td></tr> <tr><td>101</td><td>24_OHM — 24 Ohm ODT</td></tr> <tr><td>110</td><td>20_OHM — 20 Ohm ODT</td></tr> <tr><td>111</td><td>17_OHM — 17 Ohm ODT</td></tr> </tbody> </table> | 000 | DISABLED — Disabled | 001 | 120_OHM — 120 Ohm ODT | 010 | 60_OHM — 60 Ohm ODT | 011 | 40_OHM — 40 Ohm ODT | 100 | 30_OHM — 30 Ohm ODT | 101 | 24_OHM — 24 Ohm ODT | 110 | 20_OHM — 20 Ohm ODT | 111 | 17_OHM — 17 Ohm ODT |
| 000 | DISABLED — Disabled | | | | | | | | | | | | | | | | |
| 001 | 120_OHM — 120 Ohm ODT | | | | | | | | | | | | | | | | |
| 010 | 60_OHM — 60 Ohm ODT | | | | | | | | | | | | | | | | |
| 011 | 40_OHM — 40 Ohm ODT | | | | | | | | | | | | | | | | |
| 100 | 30_OHM — 30 Ohm ODT | | | | | | | | | | | | | | | | |
| 101 | 24_OHM — 24 Ohm ODT | | | | | | | | | | | | | | | | |
| 110 | 20_OHM — 20 Ohm ODT | | | | | | | | | | | | | | | | |
| 111 | 17_OHM — 17 Ohm ODT | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.476 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_TERM_CTL7)

Address: 20E_0000h base + 780h offset = 20E_0780h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL7 field descriptions

| Field | Description |
|-------------------|--|
| 31–11 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_TERM_CTL7 field descriptions (continued)

| Field | Description |
|-------------|---|
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA56, DRAM_DATA57, DRAM_DATA58, DRAM_DATA59, DRAM_DATA60, DRAM_DATA61, DRAM_DATA62, DRAM_DATA63</p> <ul style="list-style-type: none"> 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.477 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B0DS)

Address: 20E_0000h base + 784h offset = 20E_0784h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|-----|---|---|---|---|
| R | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | DSE | | 0 | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | |

IOMUXC_SW_PAD_CTL_GRP_B0DS field descriptions

| Field | Description |
|------------------|--|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA00, DRAM_DATA01, DRAM_DATA02, DRAM_DATA03, DRAM_DATA04, DRAM_DATA05, DRAM_DATA06, DRAM_DATA07</p> <ul style="list-style-type: none"> 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.478 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B1DS)

Address: 20E_0000h base + 788h offset = 20E_0788h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | |

IOMUXC_SW_PAD_CTL_GRP_B1DS field descriptions

| Field | Description |
|------------------|--|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for group: Affected pads: DRAM_DATA08, DRAM_DATA09, DRAM_DATA10, DRAM_DATA11, DRAM_DATA12, DRAM_DATA13, DRAM_DATA14, DRAM_DATA15 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHMHM — 60 Ohm 101 48_OHMHM — 48 Ohm 110 40_OHMHM — 40 Ohm 111 34_OHMHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.479 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_CTLDS)

Address: 20E_0000h base + 78Ch offset = 20E_078Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | |

IOMUXC_SW_PAD_CTL_GRP_CTLDS field descriptions

| Field | Description |
|------------------|--|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_CTLDS field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|------------|---|-----|-------------------|-----|--------------------------|-----|--------------------------|-----|------------------------|-----|------------------------|-----|------------------------|-----|------------------------|-----|------------------------|
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_CS0_B, DRAM_CS1_B, DRAM_SDBA2, DRAM_SDCKE0, DRAM_SDCKE1, DRAM_SDWE_B</p> <table> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.480 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII)

Address: 20E_0000h base + 790h offset = 20E_0790h

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | 0 | | | | | | | DDR_SEL | 0 |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII field descriptions

| Field | Description | | | | |
|-------------------|---|----|-----------------------------|----|-----------------------------|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. | | | | |
| 19–18 DDR_SEL | <p>DDR Select Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: RGMII_RD0, RGMII_RD1, RGMII_RD2, RGMII_RD3, RGMII_RXC, RGMII_RX_CTL, RGMII_TD0, RGMII_TD1, RGMII_TD2, RGMII_TD3, RGMII_TXC, RGMII_TX_CTL</p> <table> <tr><td>00</td><td>RESERVED0 — Reserved</td></tr> <tr><td>01</td><td>RESERVED1 — Reserved</td></tr> </table> | 00 | RESERVED0 — Reserved | 01 | RESERVED1 — Reserved |
| 00 | RESERVED0 — Reserved | | | | |
| 01 | RESERVED1 — Reserved | | | | |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE_RGMII field descriptions (continued)

| Field | Description |
|----------|--|
| | 10 1P2V_IO — 1.2V I/O interfaces including USB HSIC and MIPI_HSI. Provides calibrated drive strengths for signals ranging from 1.0V up to 1.3V. 11 1P5V_IO — 1.5V I/O interfaces including ENET. Provides calibrated drive strengths for signals ranging from 1.3V to 2.5V. |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.481 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B2DS)

Address: 20E_0000h base + 794h offset = 20E_0794h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|-----|---|---|---|---|
| R | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | DSE | | 0 | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |

IOMUXC_SW_PAD_CTL_GRP_B2DS field descriptions

| Field | Description |
|------------------|--|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for group: . Affected pads: DRAM_DATA16, DRAM_DATA17, DRAM_DATA18, DRAM_DATA19, DRAM_DATA20, DRAM_DATA21, DRAM_DATA22, DRAM_DATA23 000 HIZ — Hi-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.482 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE)

Address: 20E_0000h base + 798h offset = 20E_0798h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|---------|----|----|----|
| R | | | | | | | | | 0 | | | | | DDR_SEL | | 0 | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE field descriptions

| Field | Description |
|-------------------|--|
| 31–20 Reserved | This read-only field is reserved and always has the value 0. |
| 19–18 DDR_SEL | <p>DDR Select Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_ADDR00, DRAM_ADDR01, DRAM_ADDR02, DRAM_ADDR03, DRAM_ADDR04, DRAM_ADDR05, DRAM_ADDR06, DRAM_ADDR07, DRAM_ADDR08, DRAM_ADDR09, DRAM_ADDR10, DRAM_ADDR11, DRAM_ADDR12, DRAM_ADDR13, DRAM_ADDR14, DRAM_ADDR15, DRAM_CAS_B, DRAM_CS0_B, DRAM_CS1_B, DRAM_DATA00, DRAM_DATA01, DRAM_DATA02, DRAM_DATA03, DRAM_DATA04, DRAM_DATA05, DRAM_DATA06, DRAM_DATA07, DRAM_DATA08, DRAM_DATA09, DRAM_DATA10, DRAM_DATA11, DRAM_DATA12, DRAM_DATA13, DRAM_DATA14, DRAM_DATA15, DRAM_DATA16, DRAM_DATA17, DRAM_DATA18, DRAM_DATA19, DRAM_DATA20, DRAM_DATA21, DRAM_DATA22, DRAM_DATA23, DRAM_DATA24, DRAM_DATA25, DRAM_DATA26, DRAM_DATA27, DRAM_DATA28, DRAM_DATA29, DRAM_DATA30, DRAM_DATA31, DRAM_DATA32, DRAM_DATA33, DRAM_DATA34, DRAM_DATA35, DRAM_DATA36, DRAM_DATA37, DRAM_DATA38, DRAM_DATA39, DRAM_DATA40, DRAM_DATA41, DRAM_DATA42, DRAM_DATA43, DRAM_DATA44, DRAM_DATA45, DRAM_DATA46, DRAM_DATA47, DRAM_DATA48, DRAM_DATA49, DRAM_DATA50, DRAM_DATA51, DRAM_DATA52, DRAM_DATA53, DRAM_DATA54, DRAM_DATA55, DRAM_DATA56, DRAM_DATA57, DRAM_DATA58, DRAM_DATA59, DRAM_DATA60, DRAM_DATA61, DRAM_DATA62, DRAM_DATA63, DRAM_DQM0, DRAM_DQM1, DRAM_DQM2, DRAM_DQM3, DRAM_DQM4, DRAM_DQM5, DRAM_DQM6, DRAM_DQM7, DRAM_ODT0, DRAM_ODT1, DRAM_RAS_B, DRAM_SDBA0, DRAM_SDBA1, DRAM_SDBA2, DRAM_SDCKE0, DRAM_SDCKE1, DRAM_SDCLK0_P, DRAM_SDCLK1_P, DRAM_SDQS0_P, DRAM_SDQS1_P, DRAM_SDQS2_P, DRAM_SDQS3_P, DRAM_SDQS4_P, DRAM_SDQS5_P, DRAM_SDQS6_P, DRAM_SDQS7_P, DRAM_SDWE_B</p> <ul style="list-style-type: none"> 00 RESERVED0 — Reserved 01 RESERVED1 — Reserved 10 LPDDR2 — LPDDR2 mode (240 Ohm driver unit calibration, 240, 120, 80, 60, 48, 40, 32 Ohm drive strengths at 1.2V) 11 DDR3 — DDR3 mode (240 Ohm driver unit calibration, 240, 120, 80, 60, 48, 40, 32 Ohm drive strengths at 1.5V) |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.483 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B3DS)

Address: 20E_0000h base + 79Ch offset = 20E_079Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | | |

IOMUXC_SW_PAD_CTL_GRP_B3DS field descriptions

| Field | Description |
|------------------|--|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for group: Affected pads: DRAM_DATA24, DRAM_DATA25, DRAM_DATA26, DRAM_DATA27, DRAM_DATA28, DRAM_DATA29, DRAM_DATA30, DRAM_DATA31 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.484 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B4DS)

Address: 20E_0000h base + 7A0h offset = 20E_07A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | | |

IOMUXC_SW_PAD_CTL_GRP_B4DS field descriptions

| Field | Description |
|------------------|--|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_B4DS field descriptions (continued)

| Field | Description | | | | | | | | | | | | | | | | |
|------------|---|-----|-------------------|-----|--------------------------|-----|--------------------------|-----|------------------------|-----|------------------------|-----|------------------------|-----|------------------------|-----|------------------------|
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA32, DRAM_DATA33, DRAM_DATA34, DRAM_DATA35, DRAM_DATA36, DRAM_DATA37, DRAM_DATA38, DRAM_DATA39</p> <table> <tbody> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </tbody> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.485 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B5DS)

Address: 20E_0000h base + 7A4h offset = 20E_07A4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-----|---|---|---|--|
| R | | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | DSE | | 0 | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |

IOMUXC_SW_PAD_CTL_GRP_B5DS field descriptions

| Field | Description | | | | | | | | | | | | | | | | |
|------------------|---|-----|-------------------|-----|--------------------------|-----|--------------------------|-----|------------------------|-----|------------------------|-----|------------------------|-----|------------------------|-----|------------------------|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |
| 5–3 DSE | <p>Drive Strength Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: DRAM_DATA40, DRAM_DATA41, DRAM_DATA42, DRAM_DATA43, DRAM_DATA44, DRAM_DATA45, DRAM_DATA46, DRAM_DATA47</p> <table> <tbody> <tr><td>000</td><td>HIZ — HI-Z</td></tr> <tr><td>001</td><td>240_OHM — 240 Ohm</td></tr> <tr><td>010</td><td>120_OHM — 120 Ohm</td></tr> <tr><td>011</td><td>80_OHM — 80 Ohm</td></tr> <tr><td>100</td><td>60_OHM — 60 Ohm</td></tr> <tr><td>101</td><td>48_OHM — 48 Ohm</td></tr> <tr><td>110</td><td>40_OHM — 40 Ohm</td></tr> <tr><td>111</td><td>34_OHM — 34 Ohm</td></tr> </tbody> </table> | 000 | HIZ — HI-Z | 001 | 240_OHM — 240 Ohm | 010 | 120_OHM — 120 Ohm | 011 | 80_OHM — 80 Ohm | 100 | 60_OHM — 60 Ohm | 101 | 48_OHM — 48 Ohm | 110 | 40_OHM — 40 Ohm | 111 | 34_OHM — 34 Ohm |
| 000 | HIZ — HI-Z | | | | | | | | | | | | | | | | |
| 001 | 240_OHM — 240 Ohm | | | | | | | | | | | | | | | | |
| 010 | 120_OHM — 120 Ohm | | | | | | | | | | | | | | | | |
| 011 | 80_OHM — 80 Ohm | | | | | | | | | | | | | | | | |
| 100 | 60_OHM — 60 Ohm | | | | | | | | | | | | | | | | |
| 101 | 48_OHM — 48 Ohm | | | | | | | | | | | | | | | | |
| 110 | 40_OHM — 40 Ohm | | | | | | | | | | | | | | | | |
| 111 | 34_OHM — 34 Ohm | | | | | | | | | | | | | | | | |
| Reserved | This read-only field is reserved and always has the value 0. | | | | | | | | | | | | | | | | |

36.4.486 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_B6DS)

Address: 20E_0000h base + 7A8h offset = 20E_07A8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |

IOMUXC_SW_PAD_CTL_GRP_B6DS field descriptions

| Field | Description |
|------------------|--|
| 31–6 Reserved | This read-only field is reserved and always has the value 0. |
| 5–3 DSE | Drive Strength Field Select one of next values for group: Affected pads: DRAM_DATA48, DRAM_DATA49, DRAM_DATA50, DRAM_DATA51, DRAM_DATA52, DRAM_DATA53, DRAM_DATA54, DRAM_DATA55 000 HIZ — HI-Z 001 240_OHM — 240 Ohm 010 120_OHM — 120 Ohm 011 80_OHM — 80 Ohm 100 60_OHM — 60 Ohm 101 48_OHM — 48 Ohm 110 40_OHM — 40 Ohm 111 34_OHM — 34 Ohm |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.487 Pad Group Control Register (IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM)

Address: 20E_0000h base + 7ACh offset = 20E_07ACh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| R | | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM field descriptions

| Field | Description |
|-------------------|--|
| 31–11 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_SW_PAD_CTL_GRP_RGMII_TERM field descriptions (continued)

| Field | Description |
|-------------|--|
| 10–8 ODT | <p>On Die Termination Field</p> <p>Select one of next values for group: .</p> <p>Affected pads: RGMII_RD0, RGMII_RD1, RGMII_RD2, RGMII_RD3, RGMII_RXC, RGMII_RX_CTL</p> <ul style="list-style-type: none"> 000 DISABLED — Disabled 001 120_OHM — 120 Ohm ODT 010 60_OHM — 60 Ohm ODT 011 40_OHM — 40 Ohm ODT 100 30_OHM — 30 Ohm ODT 101 24_OHM — 24 Ohm ODT 110 20_OHM — 20 Ohm ODT 111 17_OHM — 17 Ohm ODT |
| Reserved | This read-only field is reserved and always has the value 0. |

36.4.488 Select Input Register (IOMUXC_ASRC_ASRCK_CLOCK_6_SELECT_INPUT)

Address: 20E_0000h base + 7B0h offset = 20E_07B0h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ASRC_ASRCK_CLOCK_6_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <ul style="list-style-type: none"> 00 KEY_ROW3_ALT1 — Selecting ALT1 mode of pad KEY_ROW3 for ASRC_EXT_CLK. 01 GPIO00_ALT3 — Selecting ALT3 mode of pad GPIO_0 for ASRC_EXT_CLK. 10 GPIO18_ALT4 — Selecting ALT4 mode of pad GPIO_18 for ASRC_EXT_CLK. |

36.4.489 Select Input Register (IOMUXC_AUD4_INPUT_DA_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7B4h offset = 20E_07B4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_AUD4_INPUT_DA_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 SD2_DATA0_ALT3 — Selecting ALT3 mode of pad SD2_DAT0 for AUD4_RXD. 1 DISP0_DATA23_ALT3 — Selecting ALT3 mode of pad DISP0_DAT23 for AUD4_RXD. |

36.4.490 Select Input Register (IOMUXC_AUD4_INPUT_DB_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7B8h offset = 20E_07B8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_AUD4_INPUT_DB_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 SD2_DATA2_ALT3 — Selecting ALT3 mode of pad SD2_DAT2 for AUD4_TXD. 1 DISP0_DATA21_ALT3 — Selecting ALT3 mode of pad DISP0_DAT21 for AUD4_TXD. |

36.4.491 Select Input Register (IOMUXC_AUD4_INPUT_RXCLK_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7BCh offset = 20E_07BCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_AUD4_INPUT_RXCLK_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 DISP0_DATA19_ALT4 — Selecting ALT4 mode of pad DISP0_DAT19 for AUD4_RXC. 1 SD2_CMD_ALT3 — Selecting ALT3 mode of pad SD2_CMD for AUD4_RXC. |

36.4.492 Select Input Register (IOMUXC_AUD4_INPUT_RXFS_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7C0h offset = 20E_07C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_AUD4_INPUT_RXFS_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 DISP0_DATA18_ALT4 — Selecting ALT4 mode of pad DISP0_DAT18 for AUD4_RXFS. 1 SD2_CLK_ALT3 — Selecting ALT3 mode of pad SD2_CLK for AUD4_RXFS. |

36.4.493 Select Input Register (IOMUXC_AUD4_INPUT_TXCLK_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7C4h offset = 20E_07C4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_AUD4_INPUT_TXCLK_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 DISP0_DATA20_ALT3 — Selecting ALT3 mode of pad DISP0_DAT20 for AUD4_TXC. 1 SD2_DATA3_ALT3 — Selecting ALT3 mode of pad SD2_DAT3 for AUD4_TXC. |

36.4.494 Select Input Register (IOMUXC_AUD4_INPUT_TXFS_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7C8h offset = 20E_07C8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_AUD4_INPUT_TXFS_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 SD2_DATA1_ALT3 — Selecting ALT3 mode of pad SD2_DAT1 for AUD4_TXFS. 1 DISP0_DATA22_ALT3 — Selecting ALT3 mode of pad DISP0_DAT22 for AUD4_TXFS. |

36.4.495 Select Input Register (IOMUXC_AUD5_INPUT_DA_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7CCh offset = 20E_07CCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_AUD5_INPUT_DA_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 DISP0_DATA19_ALT3 — Selecting ALT3 mode of pad DISP0_DAT19 for AUD5_RXD. 1 KEY_ROW1_ALT2 — Selecting ALT2 mode of pad KEY_ROW1 for AUD5_RXD. |

36.4.496 Select Input Register (IOMUXC_AUD5_INPUT_DB_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7D0h offset = 20E_07D0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_AUD5_INPUT_DB_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 DISP0_DATA17_ALT3 — Selecting ALT3 mode of pad DISP0_DAT17 for AUD5_TXD. 1 KEY_ROW0_ALT2 — Selecting ALT2 mode of pad KEY_ROW0 for AUD5_TXD. |

36.4.497 Select Input Register (IOMUXC_AUD5_INPUT_RXCLK_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7D4h offset = 20E_07D4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_AUD5_INPUT_RXCLK_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA25_ALT6 — Selecting ALT6 mode of pad EIM_D25 for AUD5_RXC. 1 DISP0_DATA14_ALT3 — Selecting ALT3 mode of pad DISP0_DAT14 for AUD5_RXC. |

36.4.498 Select Input Register (IOMUXC_AUD5_INPUT_RXFS_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7D8h offset = 20E_07D8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_AUD5_INPUT_RXFS_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA24_ALT6 — Selecting ALT6 mode of pad EIM_D24 for AUD5_RXFS. 1 DISP0_DATA13_ALT3 — Selecting ALT3 mode of pad DISP0_DAT13 for AUD5_RXFS. |

36.4.499 Select Input Register (IOMUXC_AUD5_INPUT_TXCLK_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7DCh offset = 20E_07DCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_AUD5_INPUT_TXCLK_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 DISP0_DATA16_ALT3 — Selecting ALT3 mode of pad DISP0_DAT16 for AUD5_TXC. 1 KEY_COL0_ALT2 — Selecting ALT2 mode of pad KEY_COL0 for AUD5_TXC. |

36.4.500 Select Input Register (IOMUXC_AUD5_INPUT_TXFS_AMX_SELECT_INPUT)

Address: 20E_0000h base + 7E0h offset = 20E_07E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | |

IOMUXC_AUD5_INPUT_TXFS_AMX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 DISP0_DATA18_ALT3 — Selecting ALT3 mode of pad DISP0_DAT18 for AUD5_TXFS. 1 KEY_COL1_ALT2 — Selecting ALT2 mode of pad KEY_COL1 for AUD5_TXFS. |

36.4.501 Select Input Register (IOMUXC_FLEXCAN1_RX_SELECT_INPUT)

Address: 20E_0000h base + 7E4h offset = 20E_07E4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | |

IOMUXC_FLEXCAN1_RX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 KEY_ROW2_ALT2 — Selecting ALT2 mode of pad KEY_ROW2 for FLEXCAN1_RX.</p> <p>01 GPIO08_ALT3 — Selecting ALT3 mode of pad GPIO_8 for FLEXCAN1_RX.</p> <p>10 SD3_CLK_ALT2 — Selecting ALT2 mode of pad SD3_CLK for FLEXCAN1_RX.</p> |

36.4.502 Select Input Register (IOMUXC_FLEXCAN2_RX_SELECT_INPUT)

Address: 20E_0000h base + 7E8h offset = 20E_07E8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_FLEXCAN2_RX_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>0 KEY_ROW4_ALT0 — Selecting ALT0 mode of pad KEY_ROW4 for FLEXCAN2_RX.</p> <p>1 SD3_DATA1_ALT2 — Selecting ALT2 mode of pad SD3_DAT1 for FLEXCAN2_RX.</p> |

36.4.503 Select Input Register (IOMUXC_CCM_PMIC_READY_SELECT_INPUT)

Address: 20E_0000h base + 7F0h offset = 20E_07F0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | DAISY | | | | | | | |

IOMUXC_CCM_PMIC_READY_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_EB0_B_ALT4 — Selecting ALT4 mode of pad EIM_EB0 for CCM_PMIC_READY. 1 GPIO17_ALT2 — Selecting ALT2 mode of pad GPIO_17 for CCM_PMIC_READY. |

36.4.504 Select Input Register (IOMUXC_ECSP1_CSPI_CLK_IN_SELECT_INPUT)

Address: 20E_0000h base + 7F4h offset = 20E_07F4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | DAISY | | | | | | | |

IOMUXC_ECSPI1_CSPI_CLK_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_DATA16_ALT1 — Selecting ALT1 mode of pad EIM_D16 for ECSPI1_SCLK. 01 DISP0_DATA20_ALT2 — Selecting ALT2 mode of pad DISP0_DAT20 for ECSPI1_SCLK. 10 KEY_COL0_ALT0 — Selecting ALT0 mode of pad KEY_COL0 for ECSPI1_SCLK. 11 CSI0_DATA04_ALT2 — Selecting ALT2 mode of pad CSI0_DAT4 for ECSPI1_SCLK.</p> |

36.4.505 Select Input Register (IOMUXC_ECSPI1_MISO_SELECT_INPUT)

Address: 20E_0000h base + 7F8h offset = 20E_07F8h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ECSPI1_MISO_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_DATA17_ALT1 — Selecting ALT1 mode of pad EIM_D17 for ECSPI1_MISO. 01 DISP0_DATA22_ALT2 — Selecting ALT2 mode of pad DISP0_DAT22 for ECSPI1_MISO. 10 KEY_COL1_ALT0 — Selecting ALT0 mode of pad KEY_COL1 for ECSPI1_MISO. 11 CSI0_DATA06_ALT2 — Selecting ALT2 mode of pad CSI0_DAT6 for ECSPI1_MISO.</p> |

36.4.506 Select Input Register (IOMUXC_ECSPI1_MOSI_SELECT_INPUT)

Address: 20E_0000h base + 7FCh offset = 20E_07FCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ECSPI1_MOSI_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_DATA18_ALT1 — Selecting ALT1 mode of pad EIM_D18 for ECSPI1_MOSI. 01 DISP0_DATA21_ALT2 — Selecting ALT2 mode of pad DISP0_DAT21 for ECSPI1_MOSI. 10 KEY_ROW0_ALT0 — Selecting ALT0 mode of pad KEY_ROW0 for ECSPI1_MOSI. 11 CSI0_DATA05_ALT2 — Selecting ALT2 mode of pad CSI0_DAT5 for ECSPI1_MOSI.</p> |

36.4.507 Select Input Register (IOMUXC_ECSPI1_SS0_SELECT_INPUT)

Address: 20E_0000h base + 800h offset = 20E_0800h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ECSPI1_SS0_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_EB2_B_ALT1 — Selecting ALT1 mode of pad EIM_EB2 for ECSPI1_SS0.</p> <p>01 DISP0_DATA23_ALT2 — Selecting ALT2 mode of pad DISP0_DAT23 for ECSPI1_SS0.</p> <p>10 KEY_ROW1_ALT0 — Selecting ALT0 mode of pad KEY_ROW1 for ECSPI1_SS0.</p> <p>11 CSI0_DATA07_ALT2 — Selecting ALT2 mode of pad CSI0_DAT7 for ECSPI1_SS0.</p> |

36.4.508 Select Input Register (IOMUXC_ECSPI1_SS1_SELECT_INPUT)

Address: 20E_0000h base + 804h offset = 20E_0804h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ECSPI1_SS1_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_DATA19_ALT1 — Selecting ALT1 mode of pad EIM_D19 for ECSPI1_SS1.</p> <p>01 DISP0_DATA15_ALT2 — Selecting ALT2 mode of pad DISP0_DAT15 for ECSPI1_SS1.</p> <p>10 KEY_COL2_ALT0 — Selecting ALT0 mode of pad KEY_COL2 for ECSPI1_SS1.</p> |

36.4.509 Select Input Register (IOMUXC_ECSPI1_SS2_SELECT_INPUT)

Address: 20E_0000h base + 808h offset = 20E_0808h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |

IOMUXC_ECSPI1_SS2_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA24_ALT3 — Selecting ALT3 mode of pad EIM_D24 for ECSPI1_SS2. 1 KEY_ROW2_ALT0 — Selecting ALT0 mode of pad KEY_ROW2 for ECSPI1_SS2. |

36.4.510 Select Input Register (IOMUXC_ECSPI1_SS3_SELECT_INPUT)

Address: 20E_0000h base + 80Ch offset = 20E_080Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | DAISY | | | | | | | |

IOMUXC_ECSPI1_SS3_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA25_ALT3 — Selecting ALT3 mode of pad EIM_D25 for ECSPI1_SS3. 1 KEY_COL3_ALT0 — Selecting ALT0 mode of pad KEY_COL3 for ECSPI1_SS3. |

36.4.511 Select Input Register (IOMUXC_ECSPI2_CSPI_CLK_IN_SELECT_INPUT)

Address: 20E_0000h base + 810h offset = 20E_0810h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | DAISY | | | | | | | |

IOMUXC_ECSPI2_CSPI_CLK_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_CS0_B_ALT2 — Selecting ALT2 mode of pad EIM_CS0 for ECSPI2_SCLK. 01 DISP0_DATA19_ALT2 — Selecting ALT2 mode of pad DISP0_DAT19 for ECSPI2_SCLK. 10 CSI0_DATA08_ALT2 — Selecting ALT2 mode of pad CSI0_DAT8 for ECSPI2_SCLK.</p> |

36.4.512 Select Input Register (IOMUXC_ECSPI2_MISO_SELECT_INPUT)

Address: 20E_0000h base + 814h offset = 20E_0814h

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ECSPI2_MISO_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_OE_B_ALT2 — Selecting ALT2 mode of pad EIM_OE for ECSPI2_MISO. 01 DISP0_DATA17_ALT2 — Selecting ALT2 mode of pad DISP0_DAT17 for ECSPI2_MISO. 10 CSI0_DATA10_ALT2 — Selecting ALT2 mode of pad CSI0_DAT10 for ECSPI2_MISO.</p> |

36.4.513 Select Input Register (IOMUXC_ECSPI2_MOSI_SELECT_INPUT)

Address: 20E_0000h base + 818h offset = 20E_0818h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ECSPI2_MOSI_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 00 EIM_CS1_B_ALT2 — Selecting ALT2 mode of pad EIM_CS1 for ECSPI2_MOSI. 01 DISP0_DATA16_ALT2 — Selecting ALT2 mode of pad DISP0_DAT16 for ECSPI2_MOSI. 10 CSI0_DATA09_ALT2 — Selecting ALT2 mode of pad CSI0_DAT9 for ECSPI2_MOSI. |

36.4.514 Select Input Register (IOMUXC_ECSPI2_SS0_SELECT_INPUT)

Address: 20E_0000h base + 81Ch offset = 20E_081Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ECSPI2_SS0_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_ECSPI2_SS0_SELECT_INPUT field descriptions (continued)

| Field | Description |
|-------|--|
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_RW_ALT2 — Selecting ALT2 mode of pad EIM_RW for ECSPI2_SS0.</p> <p>01 DISP0_DATA18_ALT2 — Selecting ALT2 mode of pad DISP0_DAT18 for ECSPI2_SS0.</p> <p>10 CSI0_DATA11_ALT2 — Selecting ALT2 mode of pad CSI0_DAT11 for ECSPI2_SS0.</p> |

36.4.515 Select Input Register (IOMUXC_ECSPI2_SS1_SELECT_INPUT)

Address: 20E_0000h base + 820h offset = 20E_0820h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ECSPI2_SS1_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>0 EIM_LBA_B_ALT2 — Selecting ALT2 mode of pad EIM_LBA for ECSPI2_SS1.</p> <p>1 DISP0_DATA15_ALT3 — Selecting ALT3 mode of pad DISP0_DAT15 for ECSPI2_SS1.</p> |

36.4.516 Select Input Register (IOMUXC_ECSPI4_SS0_SELECT_INPUT)

Address: 20E_0000h base + 824h offset = 20E_0824h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ECSPI4_SS0_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA20_ALT1 — Selecting ALT1 mode of pad EIM_D20 for ECSPI4_SS0. 1 EIM_DATA29_ALT2 — Selecting ALT2 mode of pad EIM_D29 for ECSPI4_SS0. |

36.4.517 Select Input Register (IOMUXC_ECSPI5_CSPI_CLK_IN_SELECT_INPUT)

Address: 20E_0000h base + 828h offset = 20E_0828h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |

IOMUXC_ECSPI5_CSPI_CLK_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 SD1_CLK_ALT1 — Selecting ALT1 mode of pad SD1_CLK for ECSPi5_SCLK. 1 SD2_CLK_ALT1 — Selecting ALT1 mode of pad SD2_CLK for ECSPi5_SCLK. |

36.4.518 Select Input Register (IOMUXC_ECSPI5_MISO_SELECT_INPUT)

Address: 20E_0000h base + 82Ch offset = 20E_082Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_ECSPI5_MISO_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 SD2_DATA0_ALT1 — Selecting ALT1 mode of pad SD2_DAT0 for ECSPI5_MISO. 1 SD1_DATA0_ALT1 — Selecting ALT1 mode of pad SD1_DAT0 for ECSPI5_MISO. |

36.4.519 Select Input Register (IOMUXC_ECSPI5_MOSI_SELECT_INPUT)

Address: 20E_0000h base + 830h offset = 20E_0830h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_ECSPI5_MOSI_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 SD1_CMD_ALT1 — Selecting ALT1 mode of pad SD1_CMD for ECSPI5_MOSI. 1 SD2_CMD_ALT1 — Selecting ALT1 mode of pad SD2_CMD for ECSPI5_MOSI. |

36.4.520 Select Input Register (IOMUXC_ECSPI5_SS0_SELECT_INPUT)

Address: 20E_0000h base + 834h offset = 20E_0834h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ECSPI5_SS0_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 SD2_DATA1_ALT1 — Selecting ALT1 mode of pad SD2_DAT1 for ECSPI5_SS0. 1 SD1_DATA1_ALT1 — Selecting ALT1 mode of pad SD1_DAT1 for ECSPI5_SS0. |

36.4.521 Select Input Register (IOMUXC_ECSPI5_SS1_SELECT_INPUT)

Address: 20E_0000h base + 838h offset = 20E_0838h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |

IOMUXC_ECSPI5_SS1_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 SD2_DATA2_ALT1 — Selecting ALT1 mode of pad SD2_DAT2 for ECSPI5_SS1. 1 SD1_DATA2_ALT1 — Selecting ALT1 mode of pad SD1_DAT2 for ECSPI5_SS1. |

36.4.522 Select Input Register (IOMUXC_ENET_REF_CLK_SELECT_INPUT)

Address: 20E_0000h base + 83Ch offset = 20E_083Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_ENET_REF_CLK_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 RGMII_TX_CTL_ALT7 — Selecting ALT7 mode of pad RGMII_TX_CTL for ENET_REF_CLK. 1 GPIO16_ALT2 — Selecting ALT2 mode of pad GPIO_16 for ENET_REF_CLK. |

36.4.523 Select Input Register (IOMUXC_ENET_MAC0_MDIO_SELECT_INPUT)

Address: 20E_0000h base + 840h offset = 20E_0840h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ENET_MAC0_MDIO_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_MDIO_ALT1 — Selecting ALT1 mode of pad ENET_MDIO for ENET_MDIO. 1 KEY_COL1_ALT1 — Selecting ALT1 mode of pad KEY_COL1 for ENET_MDIO. |

36.4.524 Select Input Register (IOMUXC_ENET_MAC0_RX_CLK_SELECT_INPUT)

Address: 20E_0000h base + 844h offset = 20E_0844h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ENET_MAC0_RX_CLK_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 RGMII_RXC_ALT1 — Selecting ALT1 mode of pad RGMII_RXC for RGMII_RXC. 1 GPIO18_ALT1 — Selecting ALT1 mode of pad GPIO_18 for ENET_RX_CLK. |

36.4.525 Select Input Register (IOMUXC_ENET_MAC0_RX_DATA0_SELECT_INPUT)

Address: 20E_0000h base + 848h offset = 20E_0848h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ENET_MAC0_RX_DATA0_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 RGMII_RD0_ALT1 — Selecting ALT1 mode of pad RGMII_RD0 for RGMII_RD0. 1 ENET_RX_DATA0_ALT1 — Selecting ALT1 mode of pad ENET_RXD0 for ENET_RX_DATA0. |

36.4.526 Select Input Register (IOMUXC_ENET_MAC0_RX_DATA1_SELECT_INPUT)

Address: 20E_0000h base + 84Ch offset = 20E_084Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_ENET_MAC0_RX_DATA1_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 RGMII_RD1_ALT1 — Selecting ALT1 mode of pad RGMII_RD1 for RGMII_RD1. 1 ENET_RX_DATA1_ALT1 — Selecting ALT1 mode of pad ENET_RXD1 for ENET_RX_DATA1. |

36.4.527 Select Input Register (IOMUXC_ENET_MAC0_RX_DATA2_SELECT_INPUT)

Address: 20E_0000h base + 850h offset = 20E_0850h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ENET_MAC0_RX_DATA2_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 RGMII_RD2_ALT1 — Selecting ALT1 mode of pad RGMII_RD2 for RGMII_RD2. 1 KEY_COL2_ALT1 — Selecting ALT1 mode of pad KEY_COL2 for ENET_RX_DATA2. |

36.4.528 Select Input Register (IOMUXC_ENET_MAC0_RX_DATA3_SELECT_INPUT)

Address: 20E_0000h base + 854h offset = 20E_0854h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_ENET_MAC0_RX_DATA3_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 RGMII_RD3_ALT1 — Selecting ALT1 mode of pad RGMII_RD3 for RGMII_RD3. 1 KEY_COL0_ALT1 — Selecting ALT1 mode of pad KEY_COL0 for ENET_RX_DATA3. |

36.4.529 Select Input Register (IOMUXC_ENET_MAC0_RX_EN_SELECT_INPUT)

Address: 20E_0000h base + 858h offset = 20E_0858h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ENET_MAC0_RX_EN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 RGMII_RX_CTL_ALT1 — Selecting ALT1 mode of pad RGMII_RX_CTL for RGMII_RX_CTL. 1 ENET_CRS_DV_ALT1 — Selecting ALT1 mode of pad ENET_CRS_DV for ENET_RX_EN. |

36.4.530 Select Input Register (IOMUXC_ESAI_RX_FS_SELECT_INPUT)

Address: 20E_0000h base + 85Ch offset = 20E_085Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_ESAI_RX_FS_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_REF_CLK_ALT2 — Selecting ALT2 mode of pad ENET_REF_CLK for ESAI_RX_FS. 1 GPIO09_ALT0 — Selecting ALT0 mode of pad GPIO_9 for ESAI_RX_FS. |

36.4.531 Select Input Register (IOMUXC_ESAI_TX_FS_SELECT_INPUT)

Address: 20E_0000h base + 860h offset = 20E_0860h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ESAI_TX_FS_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_RX_DATA1_ALT2 — Selecting ALT2 mode of pad ENET_RXD1 for ESAI_TX_FS. 1 GPIO02_ALT0 — Selecting ALT0 mode of pad GPIO_2 for ESAI_TX_FS. |

36.4.532 Select Input Register (IOMUXC_ESAI_RX_HF_CLK_SELECT_INPUT)

Address: 20E_0000h base + 864h offset = 20E_0864h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ESAI_RX_HF_CLK_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_RX_ER_ALT2 — Selecting ALT2 mode of pad ENET_RX_ER for ESAI_RX_HF_CLK. 1 GPIO03_ALT0 — Selecting ALT0 mode of pad GPIO_3 for ESAI_RX_HF_CLK. |

36.4.533 Select Input Register (IOMUXC_ESAI_TX_HF_CLK_SELECT_INPUT)

Address: 20E_0000h base + 868h offset = 20E_0868h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ESAI_TX_HF_CLK_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_RX_DATA0_ALT2 — Selecting ALT2 mode of pad ENET_RXD0 for ESAI_TX_HF_CLK. 1 GPIO04_ALT0 — Selecting ALT0 mode of pad GPIO_4 for ESAI_TX_HF_CLK. |

36.4.534 Select Input Register (IOMUXC_ESAI_RX_CLK_SELECT_INPUT)

Address: 20E_0000h base + 86Ch offset = 20E_086Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ESAI_RX_CLK_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_MDIO_ALT2 — Selecting ALT2 mode of pad ENET_MDIO for ESAI_RX_CLK. 1 GPIO01_ALT0 — Selecting ALT0 mode of pad GPIO_1 for ESAI_RX_CLK. |

36.4.535 Select Input Register (IOMUXC_ESAI_TX_CLK_SELECT_INPUT)

Address: 20E_0000h base + 870h offset = 20E_0870h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ESAI_TX_CLK_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_CRS_DV_ALT2 — Selecting ALT2 mode of pad ENET_CRS_DV for ESAI_TX_CLK. 1 GPIO06_ALT0 — Selecting ALT0 mode of pad GPIO_6 for ESAI_TX_CLK. |

36.4.536 Select Input Register (IOMUXC_ESAI_SDO0_SELECT_INPUT)

Address: 20E_0000h base + 874h offset = 20E_0874h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_ESAI_SDO0_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 GPIO17_ALT0 — Selecting ALT0 mode of pad GPIO_17 for ESAI_TX0. 1 NAND_CS2_B_ALT2 — Selecting ALT2 mode of pad NANDF_CS2 for ESAI_TX0. |

36.4.537 Select Input Register (IOMUXC_ESAI_SDO1_SELECT_INPUT)

Address: 20E_0000h base + 878h offset = 20E_0878h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_ESAI_SDO1_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 GPIO18_ALT0 — Selecting ALT0 mode of pad GPIO_18 for ESAI_TX1. 1 NAND_CS3_B_ALT2 — Selecting ALT2 mode of pad NANDF_CS3 for ESAI_TX1. |

36.4.538 Select Input Register (IOMUXC_ESAI_SDO2_SD13_SELECT_INPUT)

Address: 20E_0000h base + 87Ch offset = 20E_087Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ESAI_SDO2_SD13_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_TX_DATA1_ALT2 — Selecting ALT2 mode of pad ENET_TXD1 for ESAI_RX2. 1 GPIO05_ALT0 — Selecting ALT0 mode of pad GPIO_5 for ESAI_RX2. |

36.4.539 Select Input Register (IOMUXC_ESAI_SDO3_SD12_SELECT_INPUT)

Address: 20E_0000h base + 880h offset = 20E_0880h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ESAI_SDO3_SD12_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_TX_EN_ALT2 — Selecting ALT2 mode of pad ENET_TX_EN for ESAI_TX3_RX2. 1 GPIO16_ALT0 — Selecting ALT0 mode of pad GPIO_16 for ESAI_TX3_RX2. |

36.4.540 Select Input Register (IOMUXC_ESAI_SDO4_SD1_SELECT_INPUT)

Address: 20E_0000h base + 884h offset = 20E_0884h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_ESAI_SDO4_SD1_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_TX_DATA0_ALT2 — Selecting ALT2 mode of pad ENET_TXD0 for ESAI_RX1. 1 GPIO07_ALT0 — Selecting ALT0 mode of pad GPIO_7 for ESAI_RX1. |

36.4.541 Select Input Register (IOMUXC_ESAI_SDO5_SDIO_SELECT_INPUT)

Address: 20E_0000h base + 888h offset = 20E_0888h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_ESAI_SDO5_SDIO_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_MDC_ALT2 — Selecting ALT2 mode of pad ENET_MDC for ESAI_TX5_RX0. 1 GPIO08_ALT0 — Selecting ALT0 mode of pad GPIO_8 for ESAI_TX5_RX0. |

36.4.542 Select Input Register (IOMUXC_HDMI_ICECIN_SELECT_INPUT)

Address: 20E_0000h base + 88Ch offset = 20E_088Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_HDMI_ICECIN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_ADDR25_ALT6 — Selecting ALT6 mode of pad EIM_A25 for HDMI_TX_CEC_LINE. 1 KEY_ROW2_ALT6 — Selecting ALT6 mode of pad KEY_ROW2 for HDMI_TX_CEC_LINE. |

36.4.543 Select Input Register (IOMUXC_HDMI_I2C_CLKIN_SELECT_INPUT)

Address: 20E_0000h base + 890h offset = 20E_0890h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_HDMI_I2C_CLKIN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_EB2_B_ALT4 — Selecting ALT4 mode of pad EIM_EB2 for HDMI_TX_DDC_SCL. 1 KEY_COL3_ALT2 — Selecting ALT2 mode of pad KEY_COL3 for HDMI_TX_DDC_SCL. |

36.4.544 Select Input Register (IOMUXC_HDMI_I2C_DATAIN_SELECT_INPUT)

Address: 20E_0000h base + 894h offset = 20E_0894h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_HDMI_I2C_DATAIN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA16_ALT4 — Selecting ALT4 mode of pad EIM_D16 for HDMI_TX_DDC_SDA. 1 KEY_ROW3_ALT2 — Selecting ALT2 mode of pad KEY_ROW3 for HDMI_TX_DDC_SDA. |

36.4.545 Select Input Register (IOMUXC_I2C1_SCL_IN_SELECT_INPUT)

Address: 20E_0000h base + 898h offset = 20E_0898h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |

IOMUXC_I2C1_SCL_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA21_ALT6 — Selecting ALT6 mode of pad EIM_D21 for I2C1_SCL. 1 CSI0_DATA09_ALT4 — Selecting ALT4 mode of pad CSI0_DAT9 for I2C1_SCL. |

36.4.546 Select Input Register (IOMUXC_I2C1_SDA_IN_SELECT_INPUT)

Address: 20E_0000h base + 89Ch offset = 20E_089Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_I2C1_SDA_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA28_ALT1 — Selecting ALT1 mode of pad EIM_D28 for I2C1_SDA. 1 CSI0_DATA08_ALT4 — Selecting ALT4 mode of pad CSI0_DAT8 for I2C1_SDA. |

36.4.547 Select Input Register (IOMUXC_I2C2_SCL_IN_SELECT_INPUT)

Address: 20E_0000h base + 8A0h offset = 20E_08A0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_I2C2_SCL_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_EB2_B_ALT6 — Selecting ALT6 mode of pad EIM_EB2 for I2C2_SCL. 1 KEY_COL3_ALT4 — Selecting ALT4 mode of pad KEY_COL3 for I2C2_SCL. |

36.4.548 Select Input Register (IOMUXC_I2C2_SDA_IN_SELECT_INPUT)

Address: 20E_0000h base + 8A4h offset = 20E_08A4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | DAISY | | | | | | | |

IOMUXC_I2C2_SDA_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA16_ALT6 — Selecting ALT6 mode of pad EIM_D16 for I2C2_SDA. 1 KEY_ROW3_ALT4 — Selecting ALT4 mode of pad KEY_ROW3 for I2C2_SDA. |

36.4.549 Select Input Register (IOMUXC_I2C3_SCL_IN_SELECT_INPUT)

Address: 20E_0000h base + 8A8h offset = 20E_08A8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | DAISY | | | | | | | |

IOMUXC_I2C3_SCL_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_DATA17_ALT6 — Selecting ALT6 mode of pad EIM_D17 for I2C3_SCL. 01 GPIO03_ALT2 — Selecting ALT2 mode of pad GPIO_3 for I2C3_SCL. 10 GPIO05_ALT6 — Selecting ALT6 mode of pad GPIO_5 for I2C3_SCL.</p> |

36.4.550 Select Input Register (IOMUXC_I2C3_SDA_IN_SELECT_INPUT)

Address: 20E_0000h base + 8ACh offset = 20E_08ACh

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | R | | | | | | | | 0 | | | | | | | |
| | W | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | R | | | | | | | | 0 | | | | | | | |
| | W | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_I2C3_SDA_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_DATA18_ALT6 — Selecting ALT6 mode of pad EIM_D18 for I2C3_SDA. 01 GPIO06_ALT2 — Selecting ALT2 mode of pad GPIO_6 for I2C3_SDA. 10 GPIO16_ALT6 — Selecting ALT6 mode of pad GPIO_16 for I2C3_SDA.</p> |

36.4.551 Select Input Register (IOMUXC_IPU2_SENS1_DATA10_SELECT_INPUT)

Address: 20E_0000h base + 8B0h offset = 20E_08B0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_IPU2_SENS1_DATA10_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA22_ALT3 — Selecting ALT3 mode of pad EIM_D22 for IPU2_CSI1_DATA10. 1 EIM_EB1_B_ALT2 — Selecting ALT2 mode of pad EIM_EB1 for IPU2_CSI1_DATA10. |

36.4.552 Select Input Register (IOMUXC_IPU2_SENS1_DATA11_SELECT_INPUT)

Address: 20E_0000h base + 8B4h offset = 20E_08B4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_IPU2_SENS1_DATA11_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA21_ALT3 — Selecting ALT3 mode of pad EIM_D21 for IPU2_CSI1_DATA11. 1 EIM_EB0_B_ALT2 — Selecting ALT2 mode of pad EIM_EB0 for IPU2_CSI1_DATA11. |

36.4.553 Select Input Register (IOMUXC_IPU2_SENS1_DATA12_SELECT_INPUT)

Address: 20E_0000h base + 8B8h offset = 20E_08B8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_IPU2_SENS1_DATA12_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA28_ALT3 — Selecting ALT3 mode of pad EIM_D28 for IPU2_CSI1_DATA12. 1 EIM_ADDR17_ALT2 — Selecting ALT2 mode of pad EIM_A17 for IPU2_CSI1_DATA12. |

36.4.554 Select Input Register (IOMUXC_IPU2_SENS1_DATA13_SELECT_INPUT)

Address: 20E_0000h base + 8BCh offset = 20E_08BCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_IPU2_SENS1_DATA13_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA27_ALT3 — Selecting ALT3 mode of pad EIM_D27 for IPU2_CSI1_DATA13. 1 EIM_ADDR18_ALT2 — Selecting ALT2 mode of pad EIM_A18 for IPU2_CSI1_DATA13. |

36.4.555 Select Input Register (IOMUXC_IPU2_SENS1_DATA14_SELECT_INPUT)

Address: 20E_0000h base + 8C0h offset = 20E_08C0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_IPU2_SENS1_DATA14_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA26_ALT3 — Selecting ALT3 mode of pad EIM_D26 for IPU2_CSI1_DATA14. 1 EIM_ADDR19_ALT2 — Selecting ALT2 mode of pad EIM_A19 for IPU2_CSI1_DATA14. |

36.4.556 Select Input Register (IOMUXC_IPU2_SENS1_DATA15_SELECT_INPUT)

Address: 20E_0000h base + 8C4h offset = 20E_08C4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_IPU2_SENS1_DATA15_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA20_ALT3 — Selecting ALT3 mode of pad EIM_D20 for IPU2_CSI1_DATA15. 1 EIM_ADDR20_ALT2 — Selecting ALT2 mode of pad EIM_A20 for IPU2_CSI1_DATA15. |

36.4.557 Select Input Register (IOMUXC_IPU2_SENS1_DATA16_SELECT_INPUT)

Address: 20E_0000h base + 8C8h offset = 20E_08C8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_IPU2_SENS1_DATA16_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA19_ALT3 — Selecting ALT3 mode of pad EIM_D19 for IPU2_CSI1_DATA16. 1 EIM_ADDR21_ALT2 — Selecting ALT2 mode of pad EIM_A21 for IPU2_CSI1_DATA16. |

36.4.558 Select Input Register (IOMUXC_IPU2_SENS1_DATA17_SELECT_INPUT)

Address: 20E_0000h base + 8CCh offset = 20E_08CCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_IPU2_SENS1_DATA17_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA18_ALT3 — Selecting ALT3 mode of pad EIM_D18 for IPU2_CSI1_DATA17. 1 EIM_ADDR22_ALT2 — Selecting ALT2 mode of pad EIM_A22 for IPU2_CSI1_DATA17. |

36.4.559 Select Input Register (IOMUXC_IPU2_SENS1_DATA18_SELECT_INPUT)

Address: 20E_0000h base + 8D0h offset = 20E_08D0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_IPU2_SENS1_DATA18_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA16_ALT3 — Selecting ALT3 mode of pad EIM_D16 for IPU2_CSI1_DATA18. 1 EIM_ADDR23_ALT2 — Selecting ALT2 mode of pad EIM_A23 for IPU2_CSI1_DATA18. |

36.4.560 Select Input Register (IOMUXC_IPU2_SENS1_DATA19_SELECT_INPUT)

Address: 20E_0000h base + 8D4h offset = 20E_08D4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_IPU2_SENS1_DATA19_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_EB2_B_ALT3 — Selecting ALT3 mode of pad EIM_EB2 for IPU2_CSI1_DATA19. 1 EIM_ADDR24_ALT2 — Selecting ALT2 mode of pad EIM_A24 for IPU2_CSI1_DATA19. |

36.4.561 Select Input Register (IOMUXC_IPU2_SENS1_DATA_EN_SELECT_INPUT)

Address: 20E_0000h base + 8D8h offset = 20E_08D8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_IPU2_SENS1_DATA_EN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA23_ALT4 — Selecting ALT4 mode of pad EIM_D23 for IPU2_CSI1_DATA_EN. 1 EIM_AD10_ALT2 — Selecting ALT2 mode of pad EIM_DA10 for IPU2_CSI1_DATA_EN. |

36.4.562 Select Input Register (IOMUXC_IPU2_SENS1_HSYNC_SELECT_INPUT)

Address: 20E_0000h base + 8DCh offset = 20E_08DCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_IPU2_SENS1_HSYNC_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_EB3_B_ALT4 — Selecting ALT4 mode of pad EIM_EB3 for IPU2_CSI1_HSYNC. 1 EIM_AD11_ALT2 — Selecting ALT2 mode of pad EIM_DA11 for IPU2_CSI1_HSYNC. |

36.4.563 Select Input Register (IOMUXC_IPU2_SENS1_PIX_CLK_SELECT_INPUT)

Address: 20E_0000h base + 8E0h offset = 20E_08E0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_IPU2_SENS1_PIX_CLK_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA17_ALT3 — Selecting ALT3 mode of pad EIM_D17 for IPU2_CSI1_PIXCLK. 1 EIM_ADDR16_ALT2 — Selecting ALT2 mode of pad EIM_A16 for IPU2_CSI1_PIXCLK. |

36.4.564 Select Input Register (IOMUXC_IPU2_SENS1_VSYNC_SELECT_INPUT)

Address: 20E_0000h base + 8E4h offset = 20E_08E4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_IPU2_SENS1_VSYNC_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA29_ALT6 — Selecting ALT6 mode of pad EIM_D29 for IPU2_CSI1_VSYNC. 1 EIM_AD12_ALT2 — Selecting ALT2 mode of pad EIM_DA12 for IPU2_CSI1_VSYNC. |

36.4.565 Select Input Register (IOMUXC_KEY_COL5_SELECT_INPUT)

Address: 20E_0000h base + 8E8h offset = 20E_08E8h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_KEY_COL5_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 GPIO00_ALT2 — Selecting ALT2 mode of pad GPIO_0 for KEY_COL5. 01 GPIO19_ALT0 — Selecting ALT0 mode of pad GPIO_19 for KEY_COL5. 10 CSI0_DATA04_ALT3 — Selecting ALT3 mode of pad CSI0_DAT4 for KEY_COL5. 11 SD2_CLK_ALT2 — Selecting ALT2 mode of pad SD2_CLK for KEY_COL5.</p> |

36.4.566 Select Input Register (IOMUXC_KEY_COL6_SELECT_INPUT)

Address: 20E_0000h base + 8ECh offset = 20E_08ECh

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_KEY_COL6_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 GPIO09_ALT2 — Selecting ALT2 mode of pad GPIO_9 for KEY_COL6. 01 CSI0_DATA06_ALT3 — Selecting ALT3 mode of pad CSI0_DAT6 for KEY_COL6. 10 SD2_DATA3_ALT2 — Selecting ALT2 mode of pad SD2_DAT3 for KEY_COL6.</p> |

36.4.567 Select Input Register (IOMUXC_KEY_COL7_SELECT_INPUT)

Address: 20E_0000h base + 8F0h offset = 20E_08F0h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_KEY_COL7_SELECT_INPUT field descriptions

| Field | Description |
|---------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 00 SD2_DATA1_ALT4 — Selecting ALT4 mode of pad SD2_DAT1 for KEY_COL7. 01 GPIO04_ALT2 — Selecting ALT2 mode of pad GPIO_4 for KEY_COL7. 10 CSI0_DATA08_ALT3 — Selecting ALT3 mode of pad CSI0_DAT8 for KEY_COL7. |

36.4.568 Select Input Register (IOMUXC_KEY_ROW5_SELECT_INPUT)

Address: 20E_0000h base + 8F4h offset = 20E_08F4h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_KEY_ROW5_SELECT_INPUT field descriptions

| Field | Description |
|---------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |

Table continues on the next page...

IOMUXC_KEY_ROW5_SELECT_INPUT field descriptions (continued)

| Field | Description |
|-------|--|
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 GPIO01_ALT2 — Selecting ALT2 mode of pad GPIO_1 for KEY_ROW5.</p> <p>01 CSI0_DATA05_ALT3 — Selecting ALT3 mode of pad CSI0_DAT5 for KEY_ROW5.</p> <p>10 SD2_CMD_ALT2 — Selecting ALT2 mode of pad SD2_CMD for KEY_ROW5.</p> |

36.4.569 Select Input Register (IOMUXC_KEY_ROW6_SELECT_INPUT)

Address: 20E_0000h base + 8F8h offset = 20E_08F8h

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_KEY_ROW6_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 SD2_DATA2_ALT4 — Selecting ALT4 mode of pad SD2_DAT2 for KEY_ROW6.</p> <p>01 GPIO02_ALT2 — Selecting ALT2 mode of pad GPIO_2 for KEY_ROW6.</p> <p>10 CSI0_DATA07_ALT3 — Selecting ALT3 mode of pad CSI0_DAT7 for KEY_ROW6.</p> |

36.4.570 Select Input Register (IOMUXC_KEY_ROW7_SELECT_INPUT)

Address: 20E_0000h base + 8FCh offset = 20E_08FCh

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_KEY_ROW7_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 00 SD2_DATA0_ALT4 — Selecting ALT4 mode of pad SD2_DAT0 for KEY_ROW7. 01 GPIO05_ALT2 — Selecting ALT2 mode of pad GPIO_5 for KEY_ROW7. 10 CSI0_DATA09_ALT3 — Selecting ALT3 mode of pad CSI0_DAT9 for KEY_ROW7. |

36.4.571 Select Input Register (IOMUXC_MLB_MLB_CLK_IN_SELECT_INPUT)

Address: 20E_0000h base + 900h offset = 20E_0900h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_MLB_MLB_CLK_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>0 ENET_TX_DATA1_ALT0 — Selecting ALT0 mode of pad ENET_TXD1 for MLB_CLK. 1 GPIO03_ALT7 — Selecting ALT7 mode of pad GPIO_3 for MLB_CLK.</p> |

36.4.572 Select Input Register (IOMUXC_MLB_MLB_DATA_IN_SELECT_INPUT)

Address: 20E_0000h base + 904h offset = 20E_0904h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_MLB_MLB_DATA_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>0 ENET_MDC_ALT0 — Selecting ALT0 mode of pad ENET_MDC for MLB_DATA. 1 GPIO02_ALT7 — Selecting ALT7 mode of pad GPIO_2 for MLB_DATA.</p> |

36.4.573 Select Input Register (IOMUXC_MLB_MLB_SIG_IN_SELECT_INPUT)

Address: 20E_0000h base + 908h offset = 20E_0908h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | DAISY | | | | | | | |
| W | | | | | | | | | | | | | | | | |

IOMUXC_MLB_MLB_SIG_IN_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 ENET_RX_DATA1_ALT0 — Selecting ALT0 mode of pad ENET_RXD1 for MLB_SIG. 1 GPIO06_ALT7 — Selecting ALT7 mode of pad GPIO_6 for MLB_SIG. |

36.4.574 Select Input Register (IOMUXC_SDMA_EVENTS14_SELECT_INPUT)

Address: 20E_0000h base + 90Ch offset = 20E_090Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|-------|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | DAISY | | | | | | | |

IOMUXC_SDMA_EVENTS14_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>0 DISP0_DATA16_ALT4 — Selecting ALT4 mode of pad DISP0_DAT16 for SDMA_EXT_EVENT0.</p> <p>1 GPIO17_ALT3 — Selecting ALT3 mode of pad GPIO_17 for SDMA_EXT_EVENT0.</p> |

36.4.575 Select Input Register (IOMUXC_SDMA_EVENTS15_SELECT_INPUT)

Address: 20E_0000h base + 910h offset = 20E_0910h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | DAISY | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SDMA_EVENTS15_SELECT_INPUT field descriptions

| Field | Description |
|------------------|---|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 DISP0_DATA17_ALT4 — Selecting ALT4 mode of pad DISP0_DAT17 for SDMA_EXT_EVENT1. 1 GPIO18_ALT3 — Selecting ALT3 mode of pad GPIO_18 for SDMA_EXT_EVENT1. |

36.4.576 Select Input Register (IOMUXC_SPDIF_SPDIF_IN1_SELECT_INPUT)

Address: 20E_0000h base + 914h offset = 20E_0914h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | DAISY | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SPDIF_SPDIF_IN1_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>00 EIM_DATA21_ALT7 — Selecting ALT7 mode of pad EIM_D21 for SPDIF_IN.</p> <p>01 ENET_RX_ER_ALT3 — Selecting ALT3 mode of pad ENET_RX_ER for SPDIF_IN.</p> <p>10 KEY_COL3_ALT6 — Selecting ALT6 mode of pad KEY_COL3 for SPDIF_IN.</p> <p>11 GPIO16_ALT4 — Selecting ALT4 mode of pad GPIO_16 for SPDIF_IN.</p> |

36.4.577 Select Input Register (IOMUXC_SPDIF_TX_CLK2_SELECT_INPUT)

Address: 20E_0000h base + 918h offset = 20E_0918h

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|-------|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | DAISY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_SPDIF_TX_CLK2_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>0 RGMII_TXC_ALT2 — Selecting ALT2 mode of pad RGMII_TXC for SPDIF_EXT_CLK.</p> <p>1 ENET_CRS_DV_ALT3 — Selecting ALT3 mode of pad ENET_CRS_DV for SPDIF_EXT_CLK.</p> |

36.4.578 Select Input Register (IOMUXC_UART1_UART_RTS_B_SELECT_INPUT)

Address: 20E_0000h base + 91Ch offset = 20E_091Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_UART1_UART_RTS_B_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>Route RTS_B signal to pad when UART is in DCE mode. Route CTS_B signal to pad when UART is in DTE mode.</p> <ul style="list-style-type: none"> 00 EIM_DATA19_ALT4 — Selecting ALT4 mode of pad EIM_D19 for UART1_CTS_B. 01 EIM_DATA20_ALT4 — Selecting ALT4 mode of pad EIM_D20 for UART1_RTS_B. 10 SD3_DATA0_ALT1 — Selecting ALT1 mode of pad SD3_DAT0 for UART1_CTS_B. 11 SD3_DATA1_ALT1 — Selecting ALT1 mode of pad SD3_DAT1 for UART1_RTS_B. |

36.4.579 Select Input Register (IOMUXC_UART1_UART_RX_DATA_SELECT_INPUT)

Address: 20E_0000h base + 920h offset = 20E_0920h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_UART1_UART_RX_DATA_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>Route RX_DATA signal to pad when UART is in DCE mode. Route TX_DATA signal to pad when UART is in DTE mode.</p> <ul style="list-style-type: none"> 00 CSI0_DATA10_ALT3 — Selecting ALT3 mode of pad CSI0_DAT10 for UART1_TX_DATA. 01 CSI0_DATA11_ALT3 — Selecting ALT3 mode of pad CSI0_DAT11 for UART1_RX_DATA. 10 SD3_DATA7_ALT1 — Selecting ALT1 mode of pad SD3_DAT7 for UART1_TX_DATA. 11 SD3_DATA6_ALT1 — Selecting ALT1 mode of pad SD3_DAT6 for UART1_RX_DATA. |

36.4.580 Select Input Register (IOMUXC_UART2_UART_RTS_B_SELECT_INPUT)

Address: 20E_0000h base + 924h offset = 20E_0924h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| R | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | DAISY |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |

IOMUXC_UART2_UART_RTS_B_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–3 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>Route RTS_B signal to pad when UART is in DCE mode. Route CTS_B signal to pad when UART is in DTE mode.</p> <ul style="list-style-type: none"> 000 EIM_DATA28_ALT4 — Selecting ALT4 mode of pad EIM_D28 for UART2_CTS_B. 001 EIM_DATA29_ALT4 — Selecting ALT4 mode of pad EIM_D29 for UART2_RTS_B. 010 SD3_CMD_ALT1 — Selecting ALT1 mode of pad SD3_CMD for UART2_CTS_B. 011 SD3_CLK_ALT1 — Selecting ALT1 mode of pad SD3_CLK for UART2_RTS_B. 100 SD4_DATA5_ALT2 — Selecting ALT2 mode of pad SD4_DAT5 for UART2_RTS_B. 101 SD4_DATA6_ALT2 — Selecting ALT2 mode of pad SD4_DAT6 for UART2_CTS_B. |

36.4.581 Select Input Register (IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT)

Address: 20E_0000h base + 928h offset = 20E_0928h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| R | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | DAISY |

Reset 0

IOMUXC_UART2_UART_RX_DATA_SELECT_INPUT field descriptions

| Field | Description |
|---------------|--|
| 31–3 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>Route RX_DATA signal to pad when UART is in DCE mode. Route TX_DATA signal to pad when UART is in DTE mode.</p> <ul style="list-style-type: none"> 000 EIM_DATA26_ALT4 — Selecting ALT4 mode of pad EIM_D26 for UART2_TX_DATA. 001 EIM_DATA27_ALT4 — Selecting ALT4 mode of pad EIM_D27 for UART2_RX_DATA. 010 GPIO07_ALT4 — Selecting ALT4 mode of pad GPIO_7 for UART2_TX_DATA. 011 GPIO08_ALT4 — Selecting ALT4 mode of pad GPIO_8 for UART2_RX_DATA. 100 SD3_DATA5_ALT1 — Selecting ALT1 mode of pad SD3_DAT5 for UART2_TX_DATA. 101 SD3_DATA4_ALT1 — Selecting ALT1 mode of pad SD3_DAT4 for UART2_RX_DATA. 110 SD4_DATA4_ALT2 — Selecting ALT2 mode of pad SD4_DAT4 for UART2_RX_DATA. 111 SD4_DATA7_ALT2 — Selecting ALT2 mode of pad SD4_DAT7 for UART2_TX_DATA. |

36.4.582 Select Input Register (IOMUXC_UART3_UART_RTS_B_SELECT_INPUT)

Address: 20E_0000h base + 92Ch offset = 20E_092Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| R | | | | | | | | | | | | | | | | 0 | | | | | | | | | | | | | | | | DAISY |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Reset 0

IOMUXC_UART3_UART_RTS_B_SELECT_INPUT field descriptions

| Field | Description |
|---------------|--|
| 31–3 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | Input Select (DAISY) Field |

Table continues on the next page...

IOMUXC_UART3_UART_RTS_B_SELECT_INPUT field descriptions (continued)

| Field | Description |
|-------|--|
| | Selecting Pads Involved in Daisy Chain. Route RTS_B signal to pad when UART is in DCE mode. Route CTS_B signal to pad when UART is in DTE mode. 000 EIM_DATA23_ALT2 — Selecting ALT2 mode of pad EIM_D23 for UART3_CTS_B. 001 EIM_EB3_B_ALT2 — Selecting ALT2 mode of pad EIM_EB3 for UART3_RTS_B. 010 EIM_DATA30_ALT4 — Selecting ALT4 mode of pad EIM_D30 for UART3_CTS_B. 011 EIM_DATA31_ALT4 — Selecting ALT4 mode of pad EIM_D31 for UART3_RTS_B. 100 SD3_DATA3_ALT1 — Selecting ALT1 mode of pad SD3_DAT3 for UART3_CTS_B. 101 SD3_RESET_ALT1 — Selecting ALT1 mode of pad SD3_RST for UART3_RTS_B. |

36.4.583 Select Input Register (IOMUXC_UART3_UART_RX_DATA_SELECT_INPUT)

Address: 20E_0000h base + 930h offset = 20E_0930h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_UART3_UART_RX_DATA_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. Route RX_DATA signal to pad when UART is in DCE mode. Route TX_DATA signal to pad when UART is in DTE mode. 00 EIM_DATA24_ALT2 — Selecting ALT2 mode of pad EIM_D24 for UART3_TX_DATA. 01 EIM_DATA25_ALT2 — Selecting ALT2 mode of pad EIM_D25 for UART3_RX_DATA. 10 SD4_CMD_ALT2 — Selecting ALT2 mode of pad SD4_CMD for UART3_TX_DATA. 11 SD4_CLK_ALT2 — Selecting ALT2 mode of pad SD4_CLK for UART3_RX_DATA. |

36.4.584 Select Input Register (IOMUXC_UART4_UART_RTS_B_SELECT_INPUT)

Address: 20E_0000h base + 934h offset = 20E_0934h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_UART4_UART_RTS_B_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>Route RTS_B signal to pad when UART is in DCE mode. Route CTS_B signal to pad when UART is in DTE mode.</p> <ul style="list-style-type: none"> 0 CSI0_DATA16_ALT3 — Selecting ALT3 mode of pad CSI0_DAT16 for UART4_RTS_B. 1 CSI0_DATA17_ALT3 — Selecting ALT3 mode of pad CSI0_DAT17 for UART4_CTS_B. |

36.4.585 Select Input Register (IOMUXC_UART4_UART_RX_DATA_SELECT_INPUT)

Address: 20E_0000h base + 938h offset = 20E_0938h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | 0 | | | | | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_UART4_UART_RX_DATA_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>Route RX_DATA signal to pad when UART is in DCE mode. Route TX_DATA signal to pad when UART is in DTE mode.</p> <ul style="list-style-type: none"> 00 KEY_COL0_ALT4 — Selecting ALT4 mode of pad KEY_COL0 for UART4_TX_DATA. 01 KEY_ROW0_ALT4 — Selecting ALT4 mode of pad KEY_ROW0 for UART4_RX_DATA. 10 CSI0_DATA12_ALT3 — Selecting ALT3 mode of pad CSI0_DAT12 for UART4_TX_DATA. 11 CSI0_DATA13_ALT3 — Selecting ALT3 mode of pad CSI0_DAT13 for UART4_RX_DATA. |

36.4.586 Select Input Register (IOMUXC_UART5_UART_RTS_B_SELECT_INPUT)

Address: 20E_0000h base + 93Ch offset = 20E_093Ch

| | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_UART5_UART_RTS_B_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>Route RTS_B signal to pad when UART is in DCE mode. Route CTS_B signal to pad when UART is in DTE mode.</p> <ul style="list-style-type: none"> 00 KEY_COL4_ALT4 — Selecting ALT4 mode of pad KEY_COL4 for UART5_RTS_B. 01 KEY_ROW4_ALT4 — Selecting ALT4 mode of pad KEY_ROW4 for UART5_CTS_B. 10 CSI0_DATA18_ALT3 — Selecting ALT3 mode of pad CSI0_DAT18 for UART5_RTS_B. 11 CSI0_DATA19_ALT3 — Selecting ALT3 mode of pad CSI0_DAT19 for UART5_CTS_B. |

36.4.587 Select Input Register (IOMUXC_UART5_UART_RX_DATA_SELECT_INPUT)

Address: 20E_0000h base + 940h offset = 20E_0940h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|
| R | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | | | | | | | | 0 | | | | | | | | |
| W | | | | | | | | | | | | | | | DAISY | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IOMUXC_UART5_UART_RX_DATA_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–2 Reserved | This read-only field is reserved and always has the value 0. |
| DAISY | <p>Input Select (DAISY) Field</p> <p>Selecting Pads Involved in Daisy Chain.</p> <p>Route RX_DATA signal to pad when UART is in DCE mode. Route TX_DATA signal to pad when UART is in DTE mode.</p> <ul style="list-style-type: none"> 00 KEY_COL1_ALT4 — Selecting ALT4 mode of pad KEY_COL1 for UART5_TX_DATA. 01 KEY_ROW1_ALT4 — Selecting ALT4 mode of pad KEY_ROW1 for UART5_RX_DATA. 10 CSI0_DATA14_ALT3 — Selecting ALT3 mode of pad CSI0_DAT14 for UART5_TX_DATA. 11 CSI0_DATA15_ALT3 — Selecting ALT3 mode of pad CSI0_DAT15 for UART5_RX_DATA. |

36.4.588 Select Input Register (IOMUXC_USB_OTG_OC_SELECT_INPUT)

Address: 20E_0000h base + 944h offset = 20E_0944h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_USB_OTG_OC_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA21_ALT4 — Selecting ALT4 mode of pad EIM_D21 for USB_OTG_OC. 1 KEY_COL4_ALT2 — Selecting ALT2 mode of pad KEY_COL4 for USB_OTG_OC. |

36.4.589 Select Input Register (IOMUXC_USB_H1_OC_SELECT_INPUT)

Address: 20E_0000h base + 948h offset = 20E_0948h

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |

IOMUXC_USB_H1_OC_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 EIM_DATA30_ALT6 — Selecting ALT6 mode of pad EIM_D30 for USB_H1_OC. 1 GPIO03_ALT6 — Selecting ALT6 mode of pad GPIO_3 for USB_H1_OC. |

36.4.590 Select Input Register (IOMUXC_USDHC1_WP_ON_SELECT_INPUT)

Address: 20E_0000h base + 94Ch offset = 20E_094Ch

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 0 | | | | | | | | | 0 | | | | | | | |
| W | | | | | | | | | | | | | | | | | |
| DAISY | | | | | | | | | | | | | | | | | |

IOMUXC_USDHC1_WP_ON_SELECT_INPUT field descriptions

| Field | Description |
|------------------|--|
| 31–1 Reserved | This read-only field is reserved and always has the value 0. |
| 0 DAISY | Input Select (DAISY) Field Selecting Pads Involved in Daisy Chain. 0 DI0_PIN04_ALT3 — Selecting ALT3 mode of pad DI0_PIN4 for SD1_WP. 1 GPIO09_ALT6 — Selecting ALT6 mode of pad GPIO_9 for SD1_WP. |