

Differential Low-Power Phase-Locked Loop in 45-nm STSCL Logic

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1 ABSTRACT

A Subthreshold Source Coupled Logic based Phase Locked Loop (PLL) is presented in this project. This topology was achieved by lowering the power supply down to $500mV$ and making every PLL component differential. To determine the benefits and drawbacks of this topology, a second PLL was built with CMOS technology with a supply voltage of $1V$. Both PLLs had an output frequency of $1.2GHz$ with a reference frequency of $150MHz$. The STSCL PLL locked frequencies around $1.2GHz$ while demonstrating an average power consumption $372 \mu W$ approximately. The STSCL PLL's LC VCO also demonstrated good phase noise performance, measuring -102 dBc/Hz at $1MHz$ offset. This system is also robust with an open-loop transfer function phase margin of 89° . The final lock time of the STSCL PLL is approximately $900ns$.

2 ACKNOWLEDGMENTS

We would like to thank Dr. Sotoudeh Hamedi-Hagh for his timely advice during this project. He was always there to give us a helping hand when we had trouble or technical difficulties.

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3 INTRODUCTION

Phase-Locked Loops (PLLs for short) are control systems that synchronize two signals with different phases, thereby making their frequencies the same. An essential part of RFICs and clock-data recovery, PLLs make a host of difficult problems comparatively easy. In RFIC chips, PLLs are used as frequency synthesizers, making modulation and demodulation in receivers and transmitters possible. In clock-data recovery, PLLs assist in recovery of the clock signal in receiver buffers during the transmission of serial data (in USB, UART, etc) [4]. As wireless communication becomes more ubiquitous in the modern age of information, PLLs have become a necessary part of integrated circuits.

The motivation behind this project is simple. PLLs have been known for quite some time now to consume substantial power. Therefore, low-power PLLs have long been an attractive choice as IC size keeps shrinking and more applications require lower power in the electronics market today. The importance of low power PLL design is clearly demonstrated by [5], [6], and [7]. Despite shrinking transistor sizes, resulting in overall lower power consumption, the PLL continues to be a power-hungry beast owing to its arduous tasks at hand. Our investigation was targeted at this problem, materializing in a low-power design for our PLL using a 45-nm process. Furthermore, a differential topology was chosen because of its noise immunity and practicality.

3.1 SUBTHRESHOLD OPERATION OF MOSFETS

Usually, the most common modes of operation of a MOS transistor taught in all universities today are - cut-off, triode and saturation. In the cut-off mode, the transistor is assumed to be completely turned off, allowing no current to flow through it. Using a

mechanical switch analogy, this would be like turning off your light switch and seeing your light bulb turn off completely. In the triode region, the transistor's gate-source voltage V_{gs} is higher than its threshold voltage, but its drain-source voltage V_{ds} is lower than $V_{gs} - V_{th}$. A channel is formed below the oxide layer and the gate terminal of the MOSFET. This makes the MOS transistor act like a resistor, with a linear I-V curve and constant slope representing its resistance. As the drain-source voltage V_{ds} is increased, the channel reaches a state where it gets pinched off towards the drain end; the current through the transistor reaches a state of saturation.

In analog integrated circuit theory, MOSFETs are always operated in the saturation region as this mode is most conducive to amplification. In digital integrated circuit theory, MOSFETs are usually operated as switches and so the triode region and cut-off regions are most ideal while the saturation region leads to meta-stability.

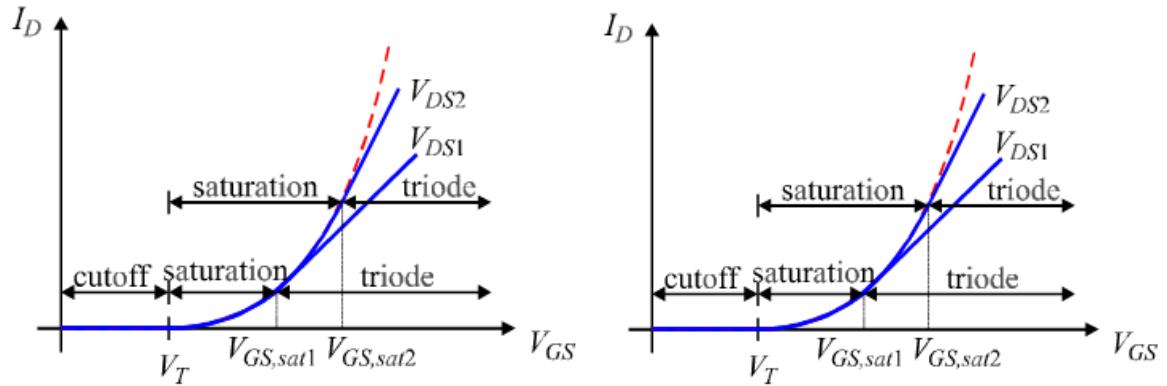


Figure 1. Conventional Regions of Operation of a MOSFET from [8]

The conventional models above have long been modified with newer models postulating the Subthreshold region in place of the conventional cut-off region. This is because in the real world, MOSFETs are not ideal switches. Even when they are completely turned off (i.e. $V_{gs} = 0$), there is some “leakage current” within MOSFETs owing to random fluctuations

in electron flow due to thermal noise. Similarly, when V_{gs} is finite but smaller than the threshold voltage V_{th} , the MOSFET is not going to be completely cut-off like an ideal switch; instead, it is going to allow a minuscule current to flow through it.

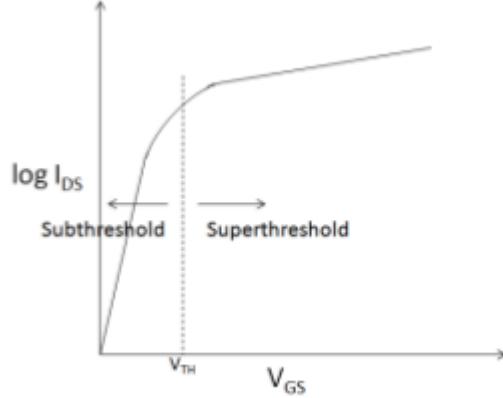


Figure 2. Subthreshold conduction in a MOSFET from [9]

In the subthreshold region, the MOSFET has an exponential relationship with V_{gs} . Thus, it is like a BJT in operation than a conventional MOSFET in triode or saturation (described in the above figure as “Super threshold”).

The defining equation relating the subthreshold current to the gate-source voltage of a MOSFET is given as follows:

$$I_{D-Sub} = \left(\frac{W}{L}\right) \mu_{eff} C_{ox} (n - 1) V_T^2 \cdot \exp\left(\frac{V_{gs} - V_{th}}{n V_T}\right) \left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right)$$

where n is called the “Subthreshold Slope Factor” ($n > 1$), VT is the thermal voltage, $\frac{W}{L}$ is the aspect ratio of the MOSFET, μ_{eff} is the effective mobility, and C_{ox} is the oxide capacitance.

An important parameter in the Subthreshold region is the MOSFET’s *Subthreshold Swing*. This parameter indicates how well a MOSFET can turn off once it goes from the super threshold to the subthreshold region. More technically, the subthreshold swing is defined as

the smallest change in V_{gs} which will cause a corresponding change in I_D by one order of magnitude [10].

$$S = \Delta V_{gs} = nV_T \cdot \ln(10)$$

$$n = 1 + \frac{C_{ox}}{C_{dep}}$$

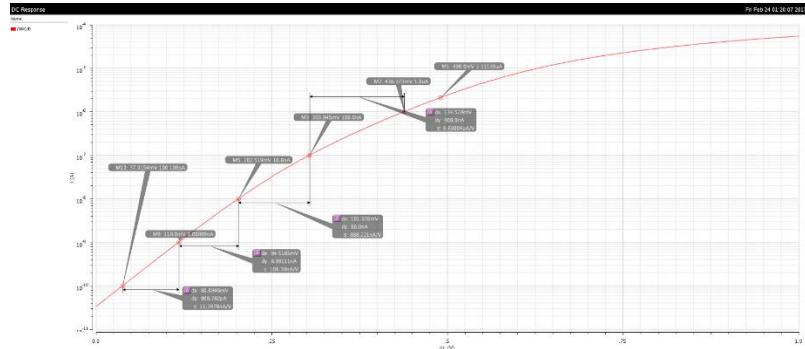


Figure 3. Subthreshold Swing for a 120-nm wide NMOS in the GPDK 45-nm process

For normal applications not requiring low-power, it is best if the subthreshold swing is kept low, which means there will be a sharp drop in current indicating better cut-off characteristics [10]. However, for low-power applications, the subthreshold swing can be made higher to reduce the marked differences between superthreshold and subthreshold currents.

Finally, it should be noted that the typical range of subthreshold current I_{D-sub} varies from 100 pA to $5\text{ }\mu\text{A}$ based on the experiments related to the design of the low-power STSCL PLL.

3.2 DIFFERENTIAL PAIRS AND SOURCE COUPLED LOGIC

Differential Pairs make up the building blocks of a robust, differential topology. They possess the ability to act as amplifiers, as comparators and as inverters when the transistors are

operated in the Subthreshold region. This versatility of the Differential Pair is what makes it an essential tool in our arsenal when building our PLL.

The workings of the Differential Pair are quite simple to explain. The two inputs are fed sinusoids that are out of phase by 180° . So, when one input is at a peak, the other will be at its trough. The peak of one input turns on the transistor it is fed to, thus letting current pass through that input's branch. The flow of current reduces the voltage at the drain of the transistor, thus making the output at that node LOW. On the other branch, the trough of the input turns off its respective transistor, letting no current pass through. Since no current flows, there is no voltage drop across the biasing transistor, therefore resulting in the respective output assuming a HIGH. If we take the difference between the two output nodes, we get a net value of HIGH or V_{dd} . As the input waves change with time, the outputs do the same and so we get a differential output at the drains of the two transistors, amplified by some finite value. If the two inputs assume the same value, both transistors will be on, thereby letting current pass through both. This will make both outputs at the drains of both transistors assume the same value - a logic LOW. When the outputs are differenced, the final output we get is a zero. This shows that when the inputs are the same, the differential pair responds with nothing i.e. it does not respond to a “common-mode” DC voltage.

Because of the differential pair's ability to reject DC “common-mode” voltages, it can reject noise that may seep in through the transistors at each individual input. The noise voltage on both inputs, which may end up amplified at the outputs, are essentially the same value. When they're amplified by the two transistors, they are still finite. However, due to the fact that we are taking our output between the two output terminals, the noise voltages are cancelled out and all we are left with is our final, desired, differential output. Therefore, we see that the

differential pair can cancel out noise, thereby resulting in its noise immunity, something that is highly desirable.

4 DESIGN

This section discusses the design and testing of each component used to create the Single-Ended and the Sub-Threshold Source-Coupled Logic Phase-Locked Loops. Each component will have two subsections; one will go into detail about the single-ended device and the other will talk about its STSCL counterpart. It is hoped that this method of information organization will help the reader understand both types of designs.

The process technology used for this project was the gpdk045. To fairly compare both PLLs that were built for this project, it was decided that using MOSFETS with the lowest threshold voltages (nmos1v_lvt and pmos1v_lvt) would be best for both. Due to this attribute, they will have the fastest switching speeds when compared to high threshold MOSFETS (nmos1v_hvt, and pmos1v_hvt) or the ones with characteristics in the middle (nmos1v, pmos1v). But this also becomes a disadvantage because they will have higher leakage currents which will lead to more power consumption. However, using low threshold devices is necessary to allow for the use of smaller devices. Details about transistor sizes will be addressed in appendix A.

4.1 PHASE-FREQUENCY FREQUENCY

The phase-frequency detector (PFD) is the first component of the PLL. It is a circuit that uses sequential logic to detect and measure the phase and frequency differences between the reference clock (ϕ_{ref}) and the feedback clock (ϕ_{fb}) and outputs a voltage pulse proportional to the difference detected.

4.1.1 Single-Ended PFD

The single-ended version of the PFD uses CMOS technology. It consists of two D Flip-flops with active-low reset capability and one two-input NAND gate. For PLL purposes, the data input for both flip-flops is tied to the power supply to allow for faster operation speeds and optimization of component sizes.

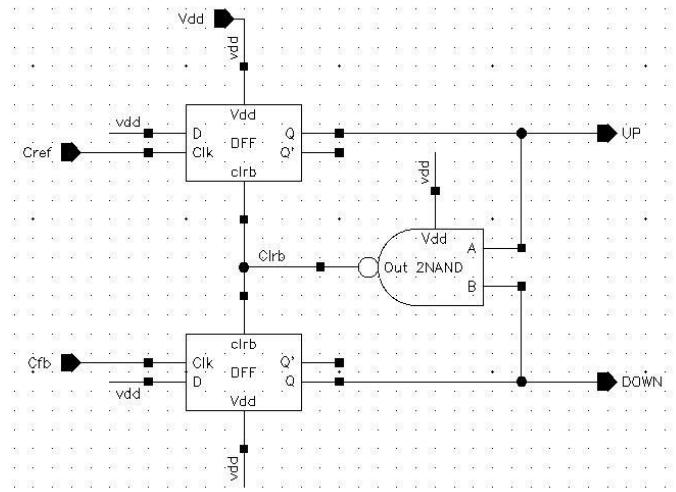


Figure 4. Phase-Frequency Detector Schematic

As shown in figure above, the outputs of the top and bottom flip-flops (“UP” and “DOWN”, respectively) are connected to the next component of the phase-locked loop and to the inputs of the NAND gate.

Table 1 NAND truth table

UP	DOWN	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Table 1 shows all the possible outputs from the NAND gate. The output is connected to the active-low reset input of both D flip-flops which means it must be LOW only when both UP and DOWN signals are high. This is indeed what happens; both flip-flops are reset which makes UP and DOWN go back to being LOW. This, in turn, sets the output of the NAND gate back to HIGH allowing the PFD to function normally.

PFD operation begins with the detection of the rising edge of ϕ_{ref} or ϕ_{fb} . Therefore, there are two scenarios that need to be examined. In the first one, ϕ_{ref} leads ϕ_{fb} .



Figure 5. waveform of ϕ_{ref} leading ϕ_{fb} .

In this situation, the UP signal goes HIGH at the falling edge of ϕ_{ref} and remains that way until the falling edge of ϕ_{fb} occurs. At this point, DOWN will be HIGH a very short time until the NAND gate resets both flip-flops. In this scenario, the PFD communicates to the rest of the circuit that ϕ_{fb} needs to speed up to catch up to the reference signal. The second scenario occurs when ϕ_{ref} lags ϕ_{fb} .

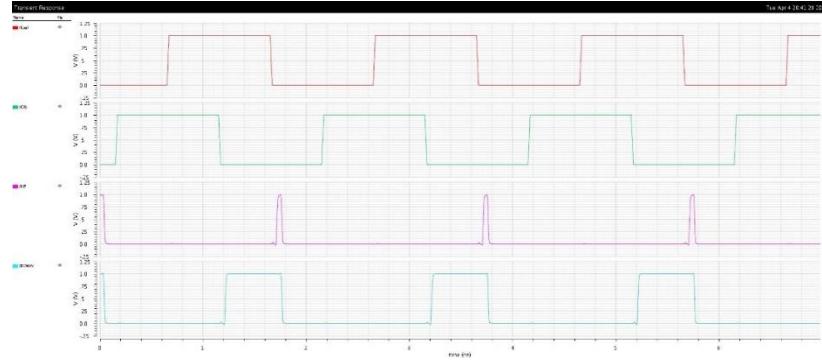


Figure 6. waveform of Φ_{ref} lagging Φ_{fb} .

In this situation, the UP and DOWN signals behave in the opposite way as the first scenario and the PFD communicates to the rest of the circuit that Φ_{fb} needs to slow down to be the same as the reference signal.

The nonidealities of the MOSFETS being used become apparent in both scenarios with the short pulse observed created by the lagging input. Whenever this signal becomes HIGH, its corresponding flip-flop will have a HIGH output for a very short time (46.49ps) before both flip-flops are reset. When both UP and DOWN signals are HIGH, the NAND gate transitions from HIGH to LOW, but this does not happen instantaneously. Also, once the reset signal becomes LOW, the rest of the PFD circuitry also takes time to be reset. To better understand how the PFD operates, a deeper look inside the D flip-flop is required. The D Flip-Flop is a storage device composed of two latches that have different functions at different edges of the clock.

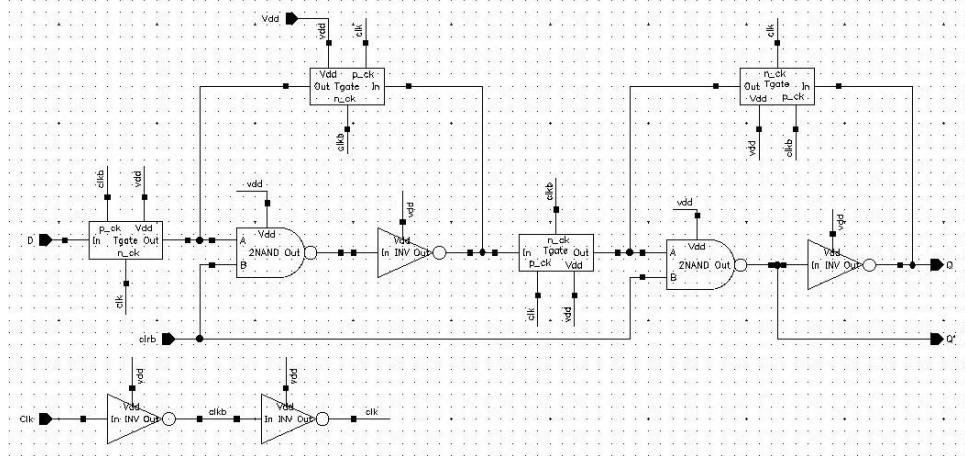


Figure 7. D Flip-flop schematic

Each latch is made up of two transmission gates (input and feedback), one NAND gate, and one inverter. When the clock is HIGH, the first latch takes in data while the second latch recirculates its previous value while remaining isolated from the first latch. When the clock goes LOW, the feedback and input transmission gates of the first and second latches, respectively, open; the feedback latch catches the value present at its input and sends it through to the second latch and consequently to the output. Two facts now become clear: the purpose of the feedback in each latch is to prevent the loss of data by recirculating it, and the data from the flip-flop comes out when the clock transitions from HIGH to LOW, which makes it a falling-edge D flip-flop.

Figure 4 shows one more aspect of the D flip-flop that needs to be addressed. The clock signal is inverted twice and the signals needed for flip-flop operation are taken from the outputs of these inverters. When the clock transitions from LOW to HIGH it is crucial that the data is present at the input and be stable, otherwise there is no guarantee the right value will be read. Inverting the clock twice introduces a delay to that signal so that data presence and stability is

insured before the clock reaches the transmission gates, this is referred as the setup time. The effect of the reset signal will be examined next.

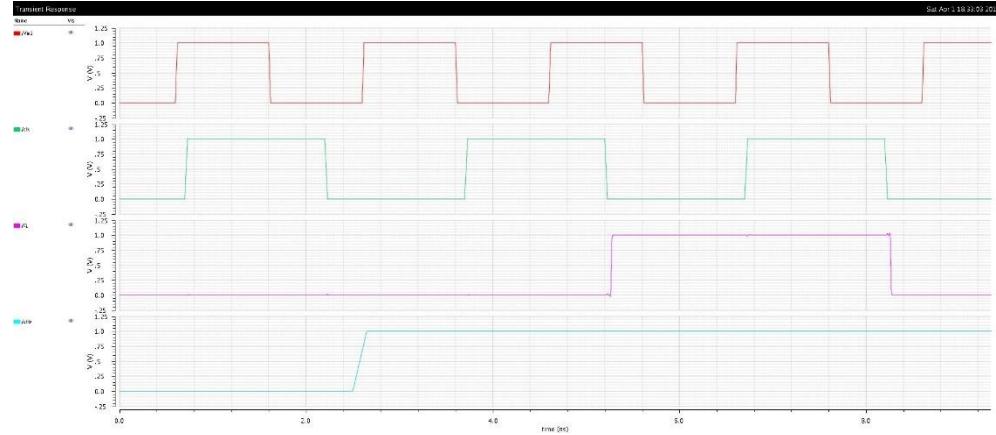


Figure 8. Waveform output of D flip-flop with toggling reset

Figure 8 shows that while the reset signal is LOW, data is not stored during the rising edge nor released during the falling edge. It is not until it goes HIGH that normal operations resume.

Lastly, small phase errors will cause the PFD to produce short output pulses which cannot be propagated effectively to control the charge pump. This results in a “dead zone” which could cause low loop gain and increased jitter [12]. A solution that is suggested is to introduce a delay in the reset path to create a minimum UP and DOWN pulse length. This approach was tested on the PFD in both situations. Figure 9 below is a repeat of figure 5 but the time when both signals are high is measured.

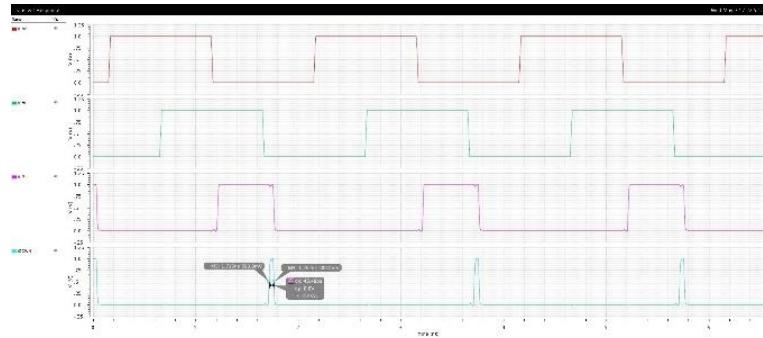


Figure 9. Measured delay without inverters

A delay cell made up of six inverters was attached to the output of the NAND gate. For simplicity, only one scenario was examined.

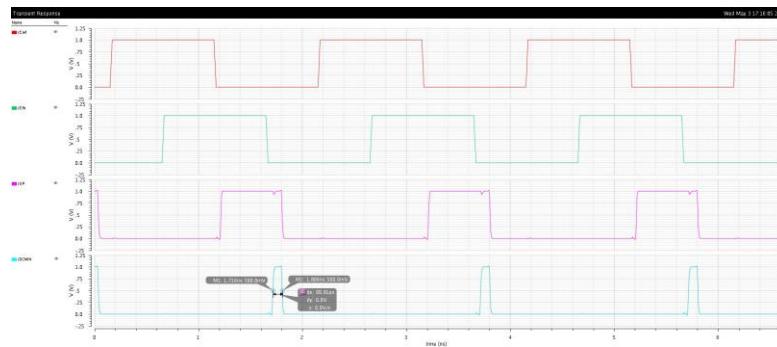


Figure 10. Measured delay with inverters

As we can see in figure 10, the time both UP and DOWN are HIGH is now 90.81ps which is larger than the 46.49ps without the delay cell. This makes sense because the reset signal will take longer to reach the reset inputs. Increasing the time both UP and DOWN are HIGH could be a problem which will be addressed in more detail in section 3.2. Furthermore, the single-ended PLL could properly lock without the delay cell so it was deemed unnecessary.

4.1.2 Differential PFD

The differential PFD performs the same task as its single-ended counterpart and they both have very similar block diagrams. However, the internal circuitry of the differential D flip-flop and AND gate is quite different.

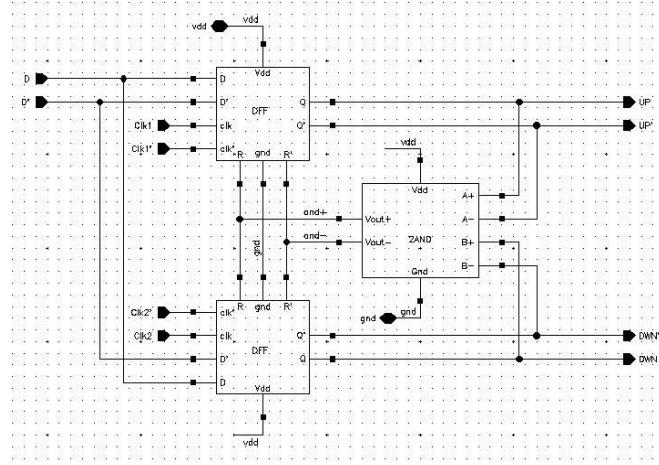


Figure 11. STSCL PFD schematic

Source-coupled logic circuits do not invert their outputs the way CMOS circuits do. Since each input or output has two terminals, a positive and negative one, obtaining an inverted or non-inverted signal depends on which of the two terminals is used as the positive one.

Just as in the single-ended PLL, the differential data input is set to HIGH: the positive data terminal is connected to the power supply and the negative one is grounded. Doing this provides the same advantages as with the single-ended PLL. Due to their similarities, there will also be two scenarios that must be examined. In the first one, ϕ_{ref} leads ϕ_{fb} .

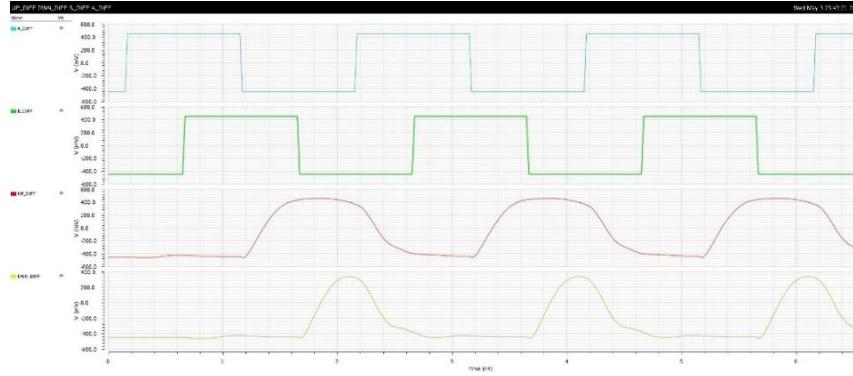


Figure 12. Waveform of Φ_{ref} leading Φ_{fb} .

The most apparent difference between figures 12 and 5 is the transition times. This is attributed to the low driving voltages for each MOSFET in the circuit. Due to the sub-threshold operation of the device, the depletion region generated by these driving voltages is very weak which causes slow transitions. This also holds true for the reset part of PFD operation; the AND gate used for this reset also experiences longer transition times which further contribute to what is seen in figure 12.

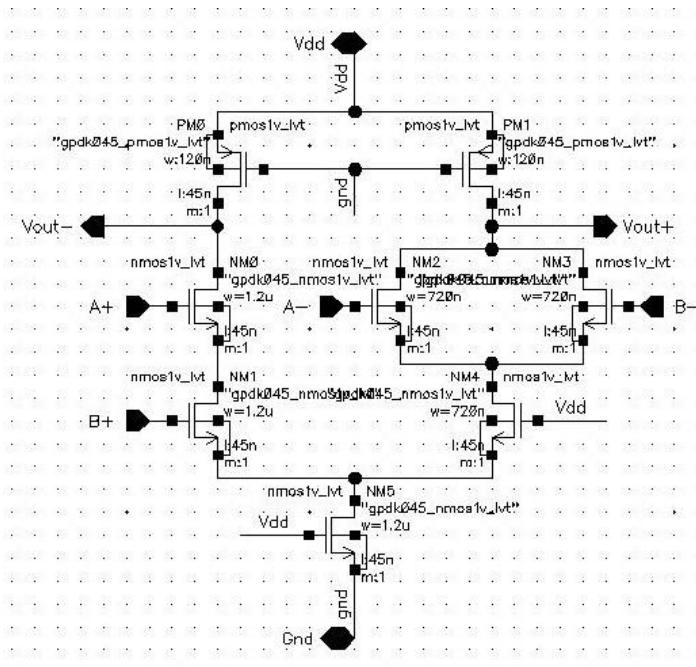


Figure 13. STSCL AND schematic

The second scenario occurs when ϕ_{ref} lags ϕ_{fb} .

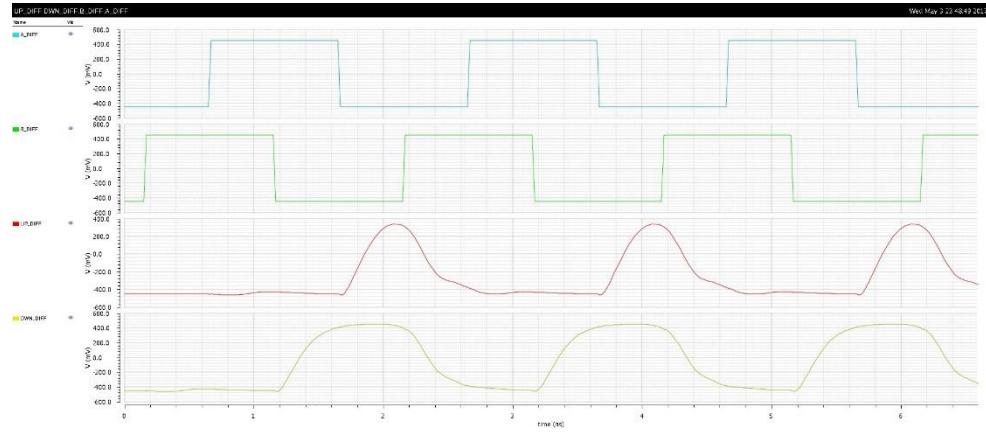


Figure 14. Waveform of ϕ_{ref} lagging ϕ_{fb} .

The figure above displays the same scenario as figure 6. The longer transition times are also observed in this figure. But despite the differences between both PFDs, the UP and DOWN signals go HIGH and LOW for the same reasons and both flip flops are active low. The non-idealities pointed out about the single-ended PFD are even more pronounced with the differential one. After much testing with different sized MOSFETs, it was not possible to create an output with the same transitions as the single-ended PFD. Increasing the size of each component did help decrease transition times but following this trend would make a STSCL too big for practical usage in modern circuits. To better understand how the differential PFD operates, a deeper look inside the latch is required.

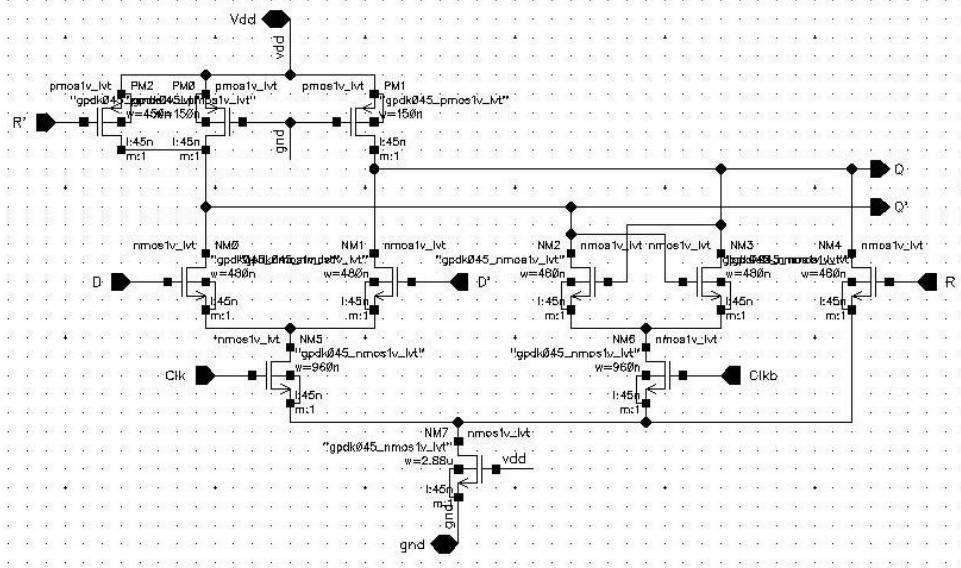


Figure 15. STSCL Latch schematic

As can be seen from figure above, the differential latch is quite different than its CMOS counterpart. Each latch has two sections; the data-set circuit on the left and data-store circuit on the right. The data inputs and the positive clock terminal are connected to the data set circuit. When the clock goes HIGH, the data present at the inputs gets set and this data becomes available as output of the master latch. The negative terminal of the clock is the only input to the data-store circuit. While the differential clock is HIGH, this circuit is deactivated because there is no path to ground.

The data store circuit becomes active when the clock goes from HIGH to LOW. Now the data becomes latched and stored in the data store section. The left MOSFET in the data-store section has a $V_{gs} = 0.5V$ and a $V_{ds} = 0V$ while the MOSFET on the right has the opposite voltages. Because of this, the data-store section will provide Q' with a connection to ground and Q will remain HIGH. Any changes in the input data will not affect the output of the latch at this stage since it has been successfully stored. If the data inputs were to change,

the already established V_{GS} of the left MOSFET will override any change in the data-store section, thereby providing stability for the next stage.

At the same time data is stored in the master latch, it is also being passed to the slave latch and becomes available as the output of the flip-flop.

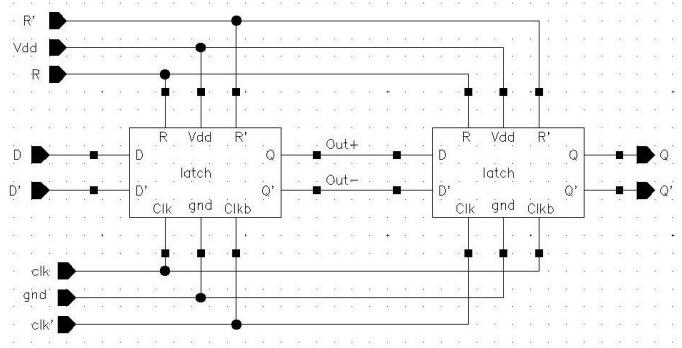


Figure 16. Block diagram of STSCL Flip-Flop

In the slave latch, the clock terminals are used in the opposite way which means the slave latch receives data when the clock is LOW. On the next clock transition from LOW to HIGH, the data becomes latched and stored in the data-store section of the slave latch which completes the data transfer from the input to the output of the d flip-flop.

Lastly, the differential reset signal can be asserted at any time during operation. A HIGH reset connects Q to ground and Q' to the supply voltage, creating differential LOW.

4.2 CHARGE PUMP

The charge pump converts the UP and DOWN input signals from the PFD that are digital in nature into currents that are sent to the Loop Filter. These currents eventually end up changing the control lines to the VCO, thereby giving rise to oscillations at the output of the PLL.

4.2.1 Single-Ended Charge Pump

The single-ended charge pump used is composed of a current source, current sink, and two switches with its inputs connected to the outputs of the PFD.

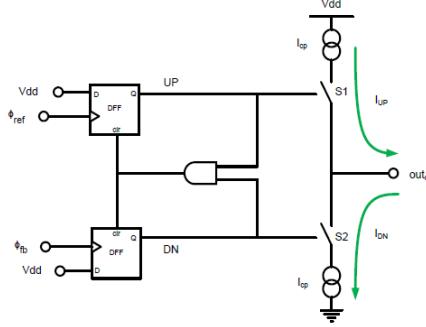


Figure 17. Block diagram of basic PFD-CP

The switches control when the current from the CP (I_{cp}) is sourced (I_{UP}) or sunk (I_{DOWN}) for a length of time proportional to phase error detected by the PFD. These switches, in turn, are controlled by the UP and DOWN outputs of the PFD.

In practice, the charge pump sections for I_{UP} and I_{DOWN} are made up of PMOS and NMOS MOSFETS, respectively. Ideally, these two currents will be the same but due to the differences between NMOS and PMOS MOSFETs, achieving this poses a challenge. Another design parameter to consider is how much current should the charge pump provide. A high current will allow for faster lock times but will consume more power. On the other hand, a current that is too small will increase the PLL lock time considerably. Also, based on the explanation given in section 3.1, both UP and DOWN signals will be high for a very short time. This will happen even when the PLL is locked creating a path from the power supply to ground. Therefore, it is imperative that this time is as short as possible and that I_{UP} and I_{DOWN}

be as equal as they can be made, otherwise the control voltage will change when it should remain the same. The current chosen was:

$$I_{cp} = 40\mu A$$

The last thing to consider for the charge pump is the inverse behaviors NMOS and PMOS MOSFETS exhibit. A HIGH voltage turns an NMOS on and an PMOS off. Therefore, an inverter must be connected to the UP output of the PFD for the charge pump to work properly.

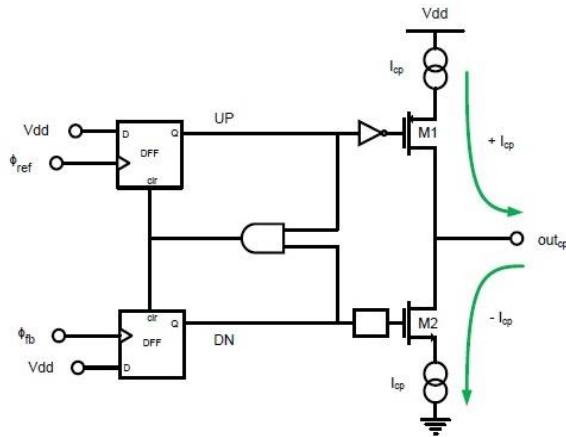


Figure 18. PFD and Charge Pump connected

Doing this introduces a small delay into that terminal that needs to be accounted for with the DOWN terminal. A transmission gate is added to create a delay like the inverter without changing the value of the output. The final charge pump setup is shown in figure 18. Despite not having the same delays, adding this transmission gate greatly reduces the difference in delays between both lines which leads to more stability.

Table 2 Delays from inverter and T-gate

	Inverter	T-gate	Difference

t_{pLH}	6.85ps	5.72ps	1.13ps
t_{pHL}	6.36ps	4.17ps	2.19ps

4.2.2 Differential Charge Pump

4.2.2.1 Design Methodology

The differential charge pump is designed based on the single-ended version. However, there are some slight differences between the two. Since we have two control voltages instead of one, the voltage between the two control lines must be regulated by the charge pump. If the differential input signal ‘UP’ is activated, then the positive control voltage line ‘Vout+’ will be increased, while the negative control voltage line ‘Vout-’ will be decreased. The opposite action occurs when the DOWN input signal is activated. When both UP and DOWN are activated at the same time, neither control voltage line will experience changes.

The main specification for the charge pump is to ensure that the currents going out of the charge pump are the same as the currents going into it. Another point to consider is the amount of current I_p passing through the charge pump when all inputs are activated. This current I_p is very useful in ensuring system stability (as will be seen in the Loop Filter sections).

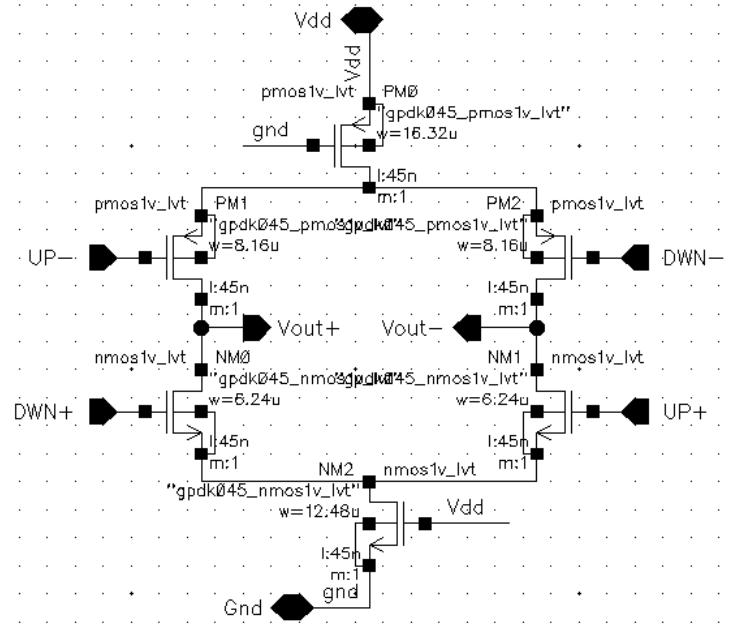


Figure 19. Differential Charge Pump schematic

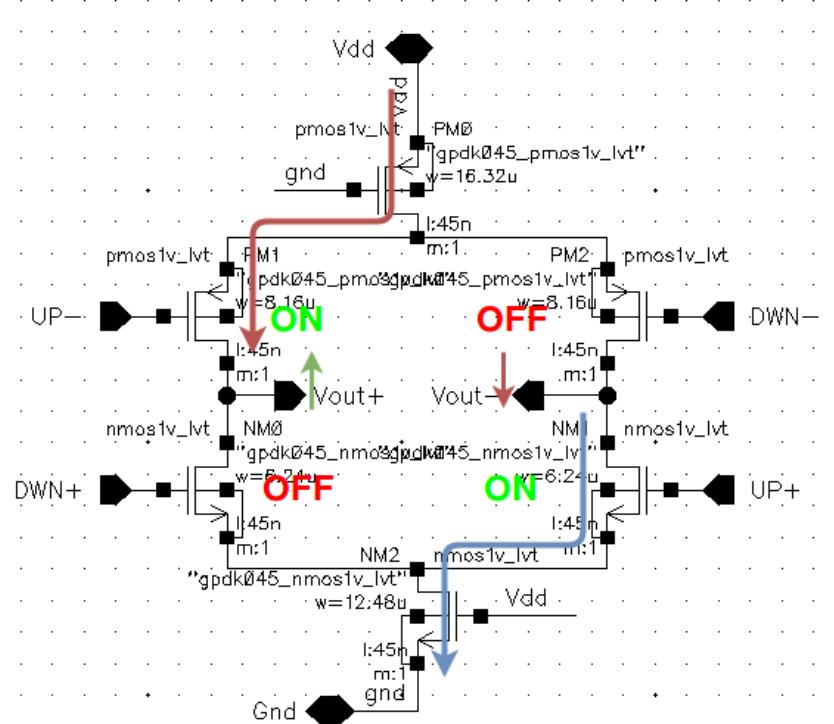


Figure 20. UP+ and UP- inputs activated in charge pump

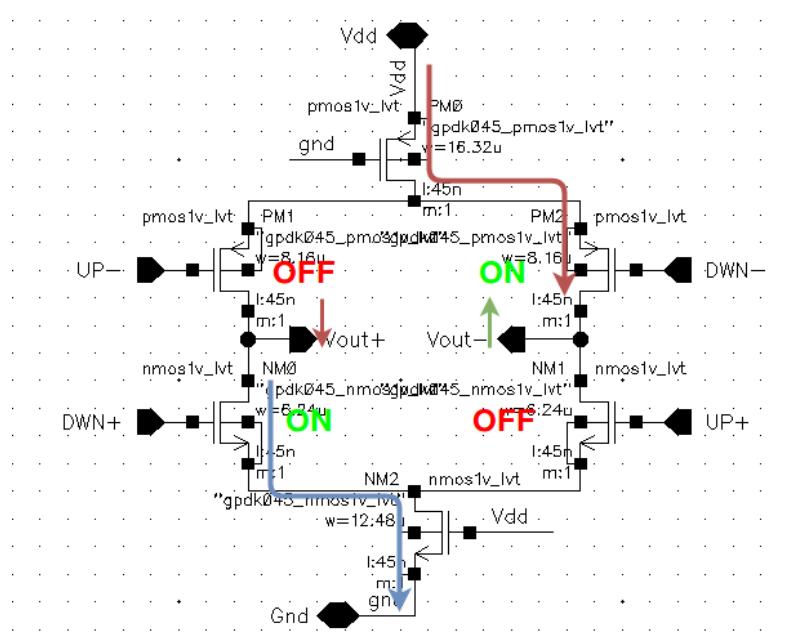


Figure 21. DOWN+ and DOWN- inputs activated in charge pump

When the UP+ and UP- inputs to the charge pump are activated, current flows through the transistors NM1 and PM1, into and out of the Vout+ and Vout- terminals respectively. This increases the previous voltage of Vout+ while decreasing the previous voltage of Vout- by the same amount. Similarly, when the DOWN+ and DOWN- inputs are activated, current flows through the transistors NM0 and PM2; this time the Vout+ value is decreased and the Vout- value is increased. In this way, the two loop filters connected to the Vout+ and Vout- terminals are charged and discharged accordingly.

The sizes of all transistors are kept large for two reasons - 1) This helps decrease the lock time of the PLL; 2) The damping factor (ζ) is increased, reducing unwanted overshoot. Concerning the first point, the amount of current I_p is critical in reducing the lock time through the relationship:

$$\frac{1}{\zeta w_n} = \frac{4\pi}{R_1 I_p K_{vco}}$$

So, as I_p is increased, the value $\frac{1}{\zeta w_n}$ (which is the time constant of the PLL closed-loop system), decreases, making the PLL lock faster.

Considering the second point, the damping factor is increased above a value of 1, making the PLL system overdamped and reducing any unwanted overshoot during lock.

$$\zeta = \frac{R_1}{2} \sqrt{\frac{I_p C_1 K_{vco}}{2\pi}}$$

If I_p is low, the damping factor becomes smaller and could end up with unwanted overshoot (if $\zeta < 1$) or even instability as it approaches 0. Although an underdamped system may lock faster and this is a tradeoff that is observed, the initial overshoot in control voltage not only affects locking capability of the PLL, but also results in greater peak power consumption. Therefore, I_p should be increased to a large enough value to ensure that the damping factor is greater than 1.

When all four inputs (UP+, UP-, DOWN+, DOWN-) are asserted, I_p is measured to be $84.5 \mu A$. A simple DC analysis in Cadence is used to achieve this result.

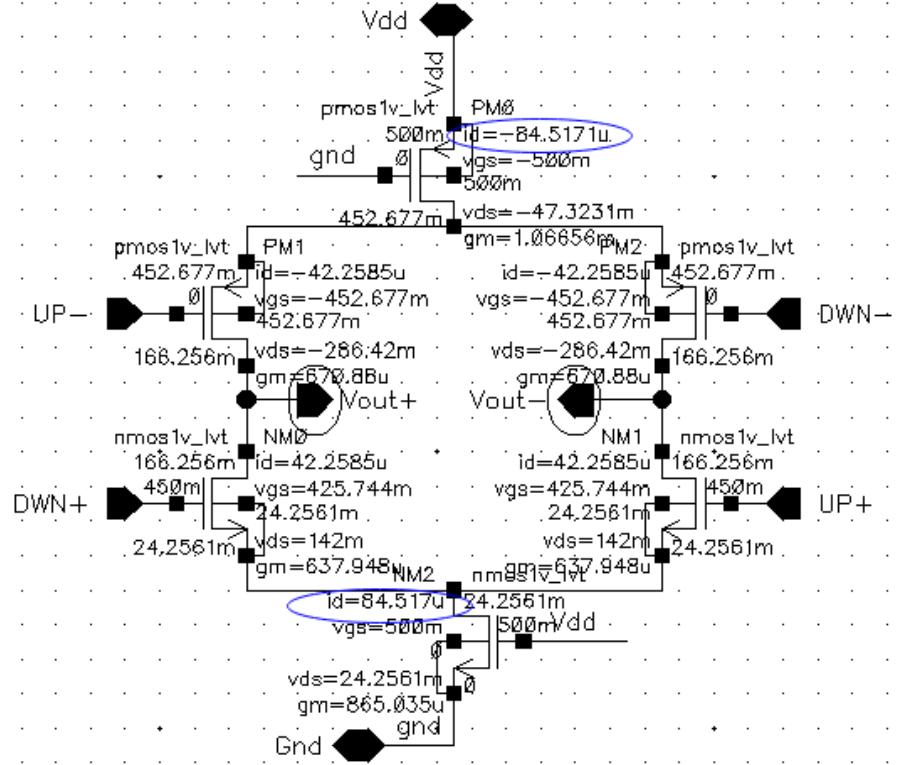


Figure 22. Charge pump DC analysis showing the value of I_p .

This value of I_p is used (as mentioned before) in the PLL's open-loop transfer function and is critical in providing closed-loop stability of the PLL.

4.2.2.2 Results

The charge pump's outputs must only receive or send currents when either UP or DOWN is activated (Note that UP and DOWN are differential in this context). When both UP and DOWN are activated, the charge pump outputs should see very little to no current, ensuring that the control voltage lines don't change. Furthermore, we also need to check whether the amount of current going out of the charge pump is approximately equal to the current coming in from the loop filter. These are the results that will determine whether the charge pump works properly or not.

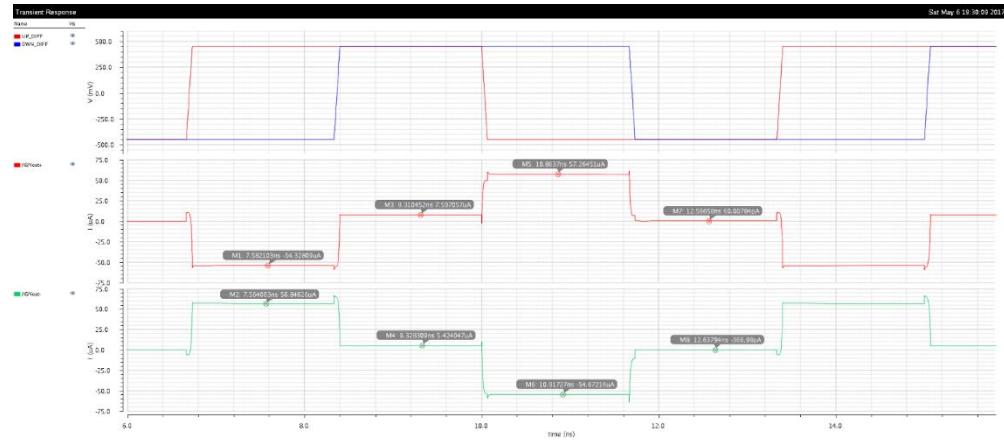


Figure 23. Charge pump current values as UP and DOWN inputs are switched

It should be noted from the above results that when both UP and DOWN differential inputs are asserted, the currents coming out of the charge pump are not small. In fact, they are in the order of a few microamps ($5\text{-}7 \mu\text{A}$). This, at first, may seem like a problem, but it must be emphasized that when the inputs UP and DOWN are asserted together, they are only done for a minuscule amount of time (in the order of picoseconds). Therefore, even though current is coming out of the charge pump terminals (Vout+ and Vout-), they don't pose an issue since this problem occurs for a small period.

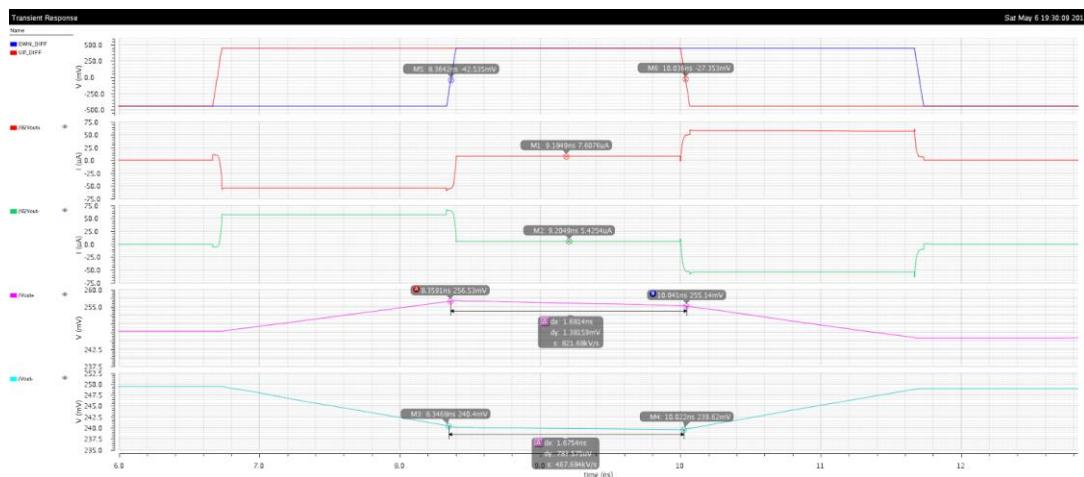


Figure 24. Changes in control voltages when both UP and DOWN are asserted for 1.67 ns

As a quick sanity check, the changes in the control lines are checked when the two inputs UP and DOWN are asserted together for a period of 1.67 ns. The V_{out+} output changes by 1.38 mV while the V_{out-} output changes by a mere 783.6 μ V. This gives us a good indication that even though current is entering and exiting the charge pump when both inputs are asserted, the voltage changes on the two control lines are minimal.

Having analyzed the functionality and potential problems in the differential charge pump, the charge pump's overall characteristics and performance are summarized.

Table 3 Differential Charge Pump Specifications

Specification	Value
DC Current ()	84.5uA
Peak Current (when UP or DOWN active)	$\sim 56\mu A$
Type	Differential

4.3 VOLTAGE CONTROLLED OSCILLATOR

A Voltage Controlled Oscillator or VCO produces a sinusoid with a frequency that is proportional to its input voltage. Usually, the higher the voltage, the higher the frequency of oscillations produced and vice versa.

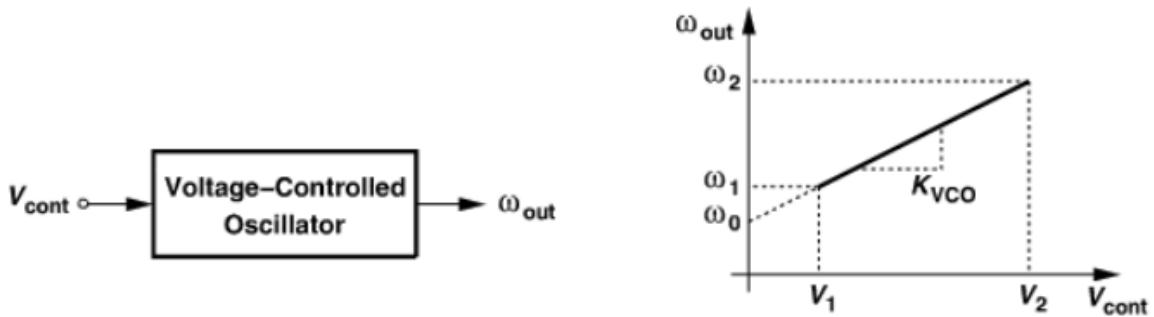


Figure 25. Voltage Controlled Oscillator Overview

A VCO converts a voltage into a sinusoid with a particular frequency. Its output can therefore be depicted by the following equation:

$$\omega_{out} = K_{vco}V_{cont} + \omega_0$$

This equation tells us that the VCO has some gain K_{vco} in $rad/s/V$, which should be ideally linear so that the output frequency of the VCO can change at a constant rate with any changes in control voltage.

There are two main types of VCOs used in integrated circuits - the LC VCO, which is built around an LC tank circuit; and the Ring VCO, which consists of an odd number of inverter stages connected in a loop.

An LC VCO usually has much better phase noise than the Ring VCO since the inductor chosen for an LC VCO has a high-quality factor. The Ring VCO usually covers a wider range of frequencies and has characteristically worse phase noise performance. The LC VCO operates on a much smaller range of frequencies and usually gives finer control.

As part of this project, we designed both types of VCOs and compared them. The Ring VCO was used in the single-ended CMOS PLL. The LC VCO was used in the differential STSCL PLL being a better fit because of the fine control it offered during lock.

The non-linear nature of the Frequency vs Control Voltage plot of the Ring VCO made it very difficult to lock the differential STSCL PLL we designed because a small change in control voltage corresponded to a huge change in frequency, most times of several magnitudes. Furthermore, it was difficult to stabilize the loop because our supply voltage was lowered from 1 V to 500 mV resulting in a much higher sensitivity offered by the Ring VCO.

4.3.1 Single-Ended VCO

A current-starved inverter was used as the basic delay cell for the VCO. Seven of these inverters were connected in series to create the voltage controlled oscillator and the output of the seventh one becomes the input of the first one.

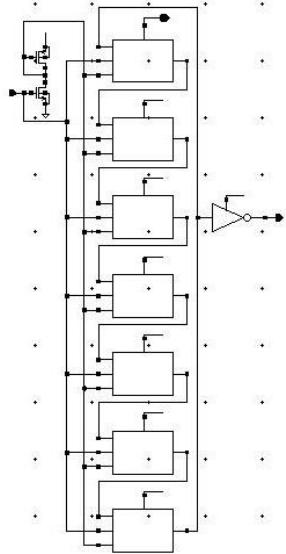


Figure 26. Schematic of Voltage Controlled Oscillator

The primary purpose of the VCO is to create an oscillating wave as an output. Therefore, an odd number of delay cells is needed; the output of the last delay cell will always be different which will cause the desired output. The amount of inverter cells is proportional to the possible output frequencies that can be achieved. Having less of these delay cells will create a shorter path from input to output which creates outputs with shorter periods. The minimum number of current starved-inverters that can be connected to achieve an acceptable output is three. This setup, however, will cause an output with a frequency that is too high for this project's purposes. Adding additional current-starved inverters slows the output down to a more appropriate frequency; this is how the conclusion of using seven delay cells was reached. Each current-starved inverter is made up of four MOSFETs in series.

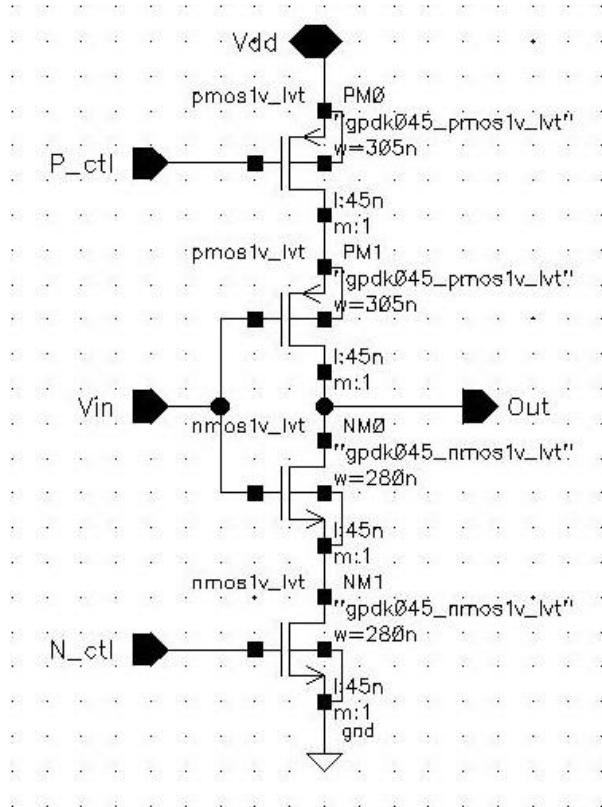


Figure 27. Current-Starved Inverter Schematic

As can be seen in figure 27, the middle section is basically an inverter. The MOSFETs at the very top and bottom are current sources which are controlled by the control voltage coming from the loop filter. However, this control voltage is single-ended so a circuit is needed to create two voltages.

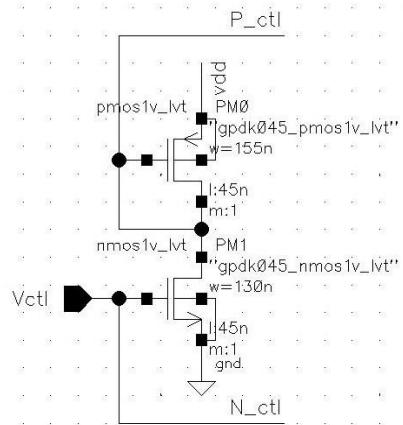


Figure 28. VCO current mirror

After examining figure 28, it can be deduced that as the control voltage increases, the voltage of the “P_ctl” line will decrease proportionally which will increase the V_{sg} of the PMOS MOSFET at the very top of the current-starved inverter. Finally, an inverter is added that functions as a buffer because the signal of the last current-starved inverter can have some distortion and uneven transitions. Testing the VCO required simulating with different control voltages. This allowed for the calculation of the VCO gain, K_{vco} .

Table 4 VCO output frequencies summary

V_{cnt}	frequency
0.10	0.00E+00
0.20	0.00E+00
0.30	2.94E+07
0.40	1.80E+08
0.50	7.18E+08
0.60	1.88E+09
0.70	3.30E+09
0.80	4.33E+09
0.90	4.87E+09
1.00	5.16E+09

A graph of the data from table 4 helps identify the linear region of operation for the VCO.

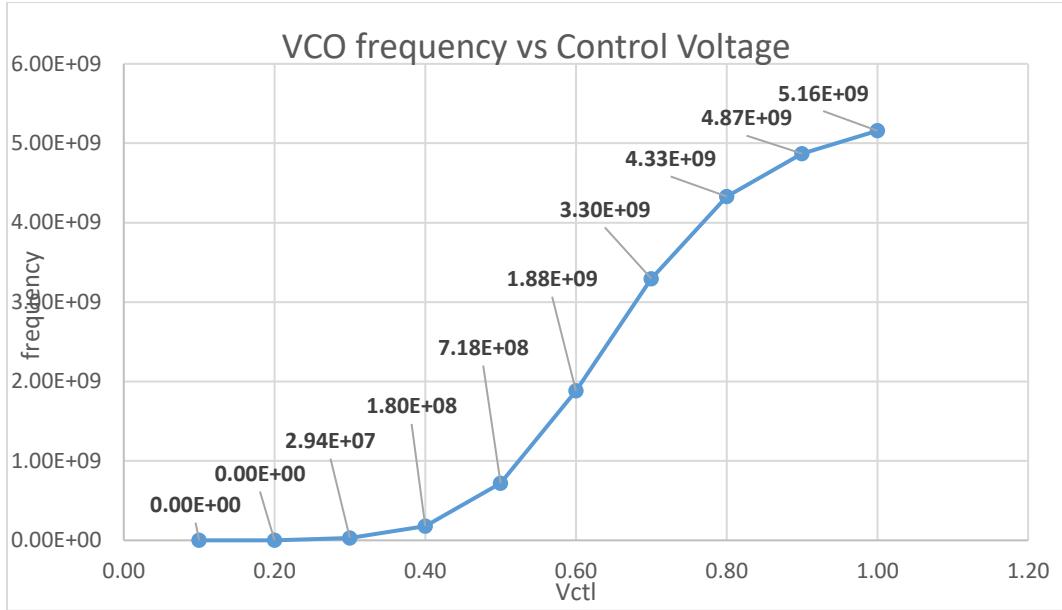


Figure 29. VCO output frequency vs control voltage

The linear region is observed to be between 0.4V and 0.8V. This area is desirable for its stability. With this information, the K_{VCO} can be obtained:

$$K_{VCO} = 2\pi \frac{f_{max} - f_{min}}{V_{max} - V_{min}} = 6.52E10 \text{ rad/v}$$

4.3.2 Differential VCO

4.3.2.1 Main Issues Faced with a Ring VCO versus an LC VCO

During the initial planning of the PLL design, the VCO was constructed using a Ring VCO topology. However, this VCO was highly sensitive to changes in the control voltage and so the PLL would never lock. It was therefore very important to create a finely tuned VCO and this was accomplished using an LC topology. Another reason the Ring VCO was not chosen for the design (even though it had a wide tuning range which was desirable) was that its high sensitivity was inversely related to the PLL stability and phase margin. As the sensitivity of the Ring VCO was increased, the phase margin degraded dramatically. Furthermore, since our

supply voltage was cut from 1 V to 500 mV, this meant that we needed a much higher K_{vco} to target a wider range of frequencies, increasing the instability in the system and degrading the phase margin as well.

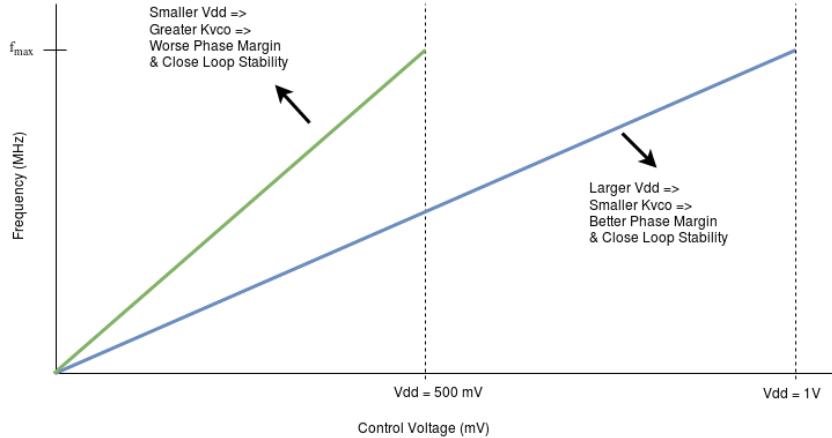


Figure 30. Explanation of tradeoff between K_{vco} , Phase Margin and Closed Loop Stability

On the other hand, an LC VCO, in addition to providing finer tuning and a smaller, more constant K_{vco} , also helped with stabilizing the system because of these characteristics. Furthermore, the LC VCO had better phase noise performance than the Ring VCO, this information being widely known in the AMS community. The LC VCO's phase noise was around -102 dBc/Hz at 1 MHz offset while the Ring VCO performed poorly at about -83 dBc/Hz at 1 MHz offset.

On the other hand, running an LC VCO in the subthreshold region of operation was incredibly problematic. The transistors needed to be enormous (a width of $20\mu\text{m}$ or more) when operated in subthreshold. However, when operated in saturation, the transistors were reasonably smaller ($6 \mu\text{m}$ or less) and still provided a large amount of current which is often required for the LC VCO to function well.

For the above reasons, the VCO for our PLL was the only block operated with a separate supply voltage of 1V instead of the usual 500mV for the other blocks.

4.3.2.2 LC VCO Topology

An LC VCO consists of an LC tank circuit (an inductor in parallel with a capacitor) along with two cross coupled NMOS transistors. “Cross coupled” here means that the gate (input) of one transistor is connected to the drain (output) of the other and likewise the same goes for the other transistor. The transistors create a total of 360° of phase shift which sustains the oscillations of the LC tank circuit. We can also say that the two transistors provide enough gain in the circuit to sustain these oscillations. It is for this reason that the transconductance of the two NMOS transistors is set as big as possible. Usually, a current source is connected below the two NMOS transistors to DC bias them.

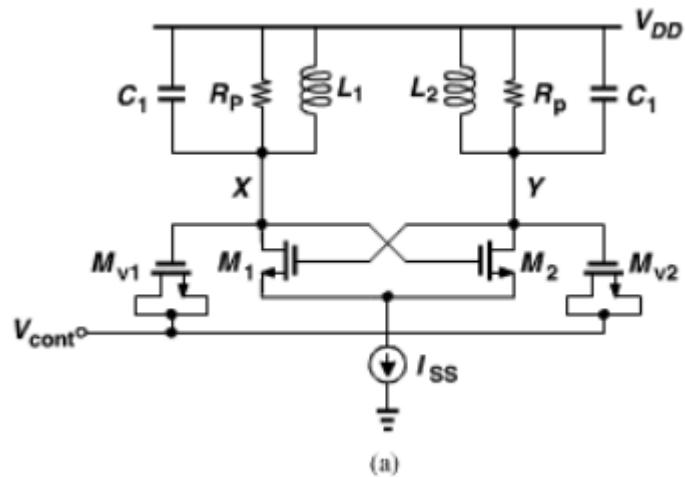


Figure 31. A typical LC VCO with cross-coupled transistors and current source at bottom

For oscillations to occur, the following criterion between the parallel resistance R_p used to model the loss in the inductor, and the transconductance gm of the NMOS transistors must be satisfied.

$$g_m R_p \gg 1$$

This means that the transconductance needs to be much greater than the reciprocal of the parallel loss resistor R_p to ensure that oscillations occur.

If the current source is at the bottom, the output will swing about V_{dd} (which in our case is 1V). The output peak-to-peak swing is related to the amount of current flowing through the current source and how big the resistance R_p is. The swing relationship is explained using the following equation:

$$V_{out|pp} = \frac{4}{\pi} I_{ss} R_p$$

Notice that increasing I_{ss} and R_p increases the output peak-to-peak swing. By setting the desired output peak-to-peak swing to 1V and the parallel loss resistance of the inductor accordingly, we can easily find the required amount of current I_{ss} .

R_p can be set using the desired quality factor of the inductor and is related to it by the following equation:

$$R_p = \omega L Q$$

Using the relationship between R_p , Q , L and ω , we can find R_p , therefore zeroing in on an I_{ss} tail current value and a transconductance (g_m) value for our transistors. The LC VCO as mentioned before, has a narrower tuning range compared to the Ring VCO

but much better phase noise performance. The tuning range is set by the two varactors connected to the outputs of the LC VCO.

$$\Delta\omega \approx \left(1 - \frac{C_{var2} - C_{var1}}{2C}\right) \frac{1}{\sqrt{LC}}$$

C_{var2} and C_{var1} are the maximum and minimum capacitance values of the varactor. The larger this difference between max and min, the wider the tuning range becomes.

The limitation of the LC VCO with the current source at the bottom is the control voltage range. This configuration only employs part of the total range of capacitance of the varactors.

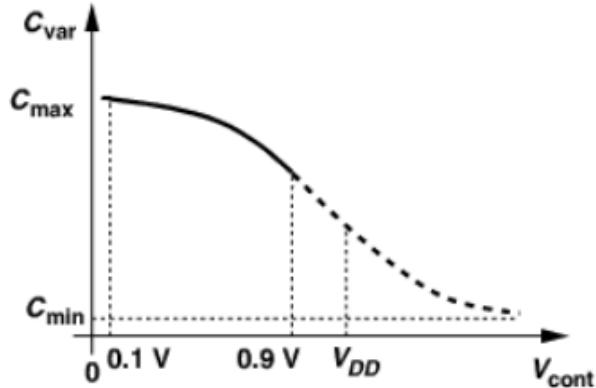


Figure 32. Limited range of varactor capacitances when current source at tail

Due to this fact, the tuning range is limited and the VCO only works for a small number of frequencies about the resonant frequency of the LC tank. Another problem with putting the current source at the bottom is the fact that since the outputs are DC biased at V_{dd} (1V in this case), they oscillate about V_{dd} . Furthermore, the outputs usually have tremendous swing, most times going all the way up to $2V_{dd}$. This puts stress on the varactors connected to the output, leading to their eventual damage with the passage of time.

The LC VCO for this project is designed with a current source (current mirror) at the top instead, which allows the outputs to swing about $\frac{V_{DD}}{2}$ rather than V_{DD} , thereby putting less stress on the varactors. It also allows for a wider tuning range than an LC VCO which has a current source at the bottom.

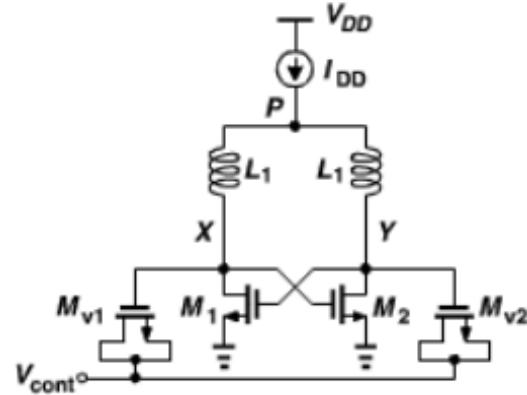


Figure 33. LC VCO with current source at the top

The current source being placed at the top can bias the voltage at point P to be $\frac{V_{DD}}{2}$. This helps reduce the stress on the varactors at the output and increase the range of usable capacitances of the varactors, effectively increasing the tuning range of the VCO.

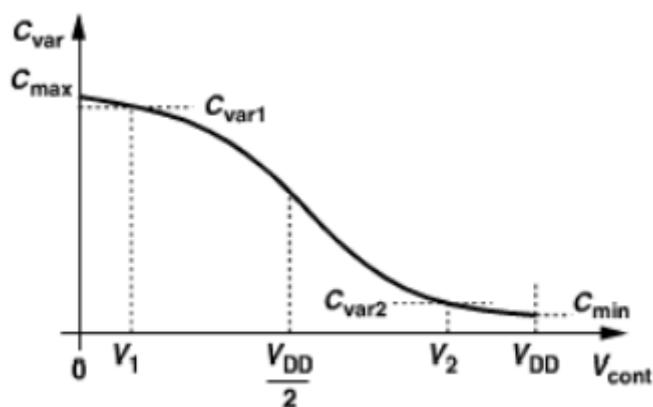


Figure 34. Capacitance range of varactors with current source at the top

How does this happen? The varactors now have a gate voltage of $\frac{V_{DD}}{2}$ instead of V_{DD} owing to the current source. The control voltage V_{cont} applied to the sources of the varactors goes from 0 to V_{DD} . This means that the voltage across the varactors will go from $-\frac{V_{DD}}{2}$ to $\frac{V_{DD}}{2}$, a wide range of usable capacitances. Compare this with when the varactor gate voltages were at V_{DD} when the current source was at the bottom. The control voltage goes from 0 to V_{DD} as usual, which makes the varactor gate-source voltages go from 0 to V_{DD} as well, covering only half the range of usable capacitances the varactor can offer. Therefore, placing the current source at the top ensures a wider range of varactor capacitances thereby allowing for a wider tuning range as well.

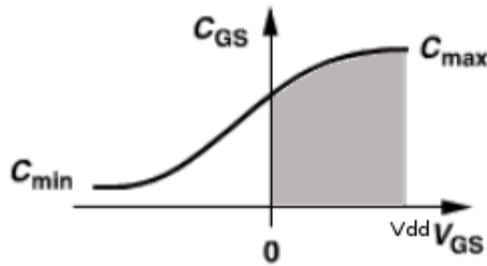


Figure 35. Capacitance range of varactor when current source at bottom

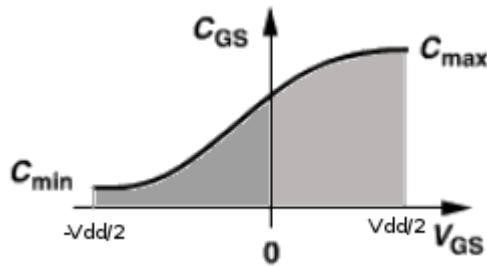


Figure 36. Capacitance range of varactor when current source at top

In sum, we can clearly see that placing the current source at the top is advantageous both in terms of tuning range and stress on varactors.

4.3.2.3 Schematic Diagram of LC VCO

Since our PLL is differential, the control voltages coming from the loop filter are differential. However, the LC VCO does not perform predictably when two control voltages are used. Hence, we decided to use only one input control voltage for the LC VCO. The differential control voltages are converted to a single-ended control voltage with the help of a balun (a 2-to-1 port device). The outputs of the LC VCO are connected to CMOS inverters instead of STSCL inverters because we are dealing with a $1V$ supply instead of a $500mV$ supply for the VCO. The inverters are also useful since they convert a sinusoid with lower swing into a square wave with higher swing (going from 0 all the way to $1V$).

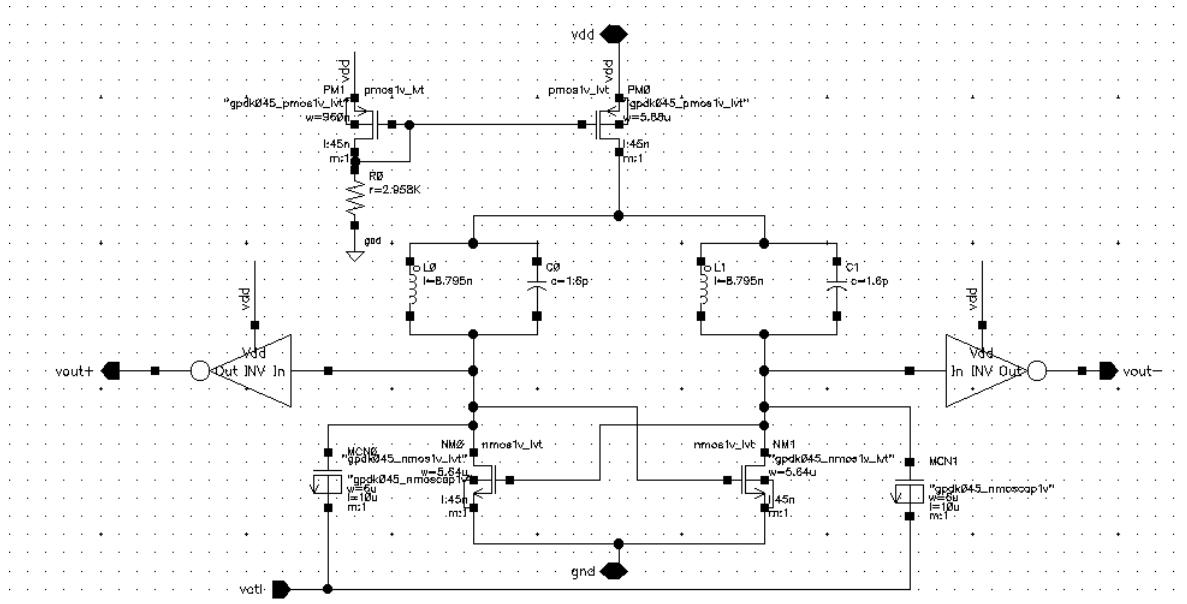


Figure 37. LC VCO Schematic with CMOS inverters at outputs

4.3.2.4 VCO Specifications and Design

To make a fully functional LC VCO, we begin with sizing the inductor and capacitor of the LC tank circuit. The desired resonant frequency of the tank is 1.2 GHz which is divided by the frequency divider to create a 150MHz feedback signal to the PFD. We also require the quality factor of the inductor to be 20, a reasonably low value chosen deliberately so that the

LC VCO can function properly with non-ideal inductors. An inductor value of $8.795nH$ and a capacitor value of $1.6pF$ result in a resonant frequency of 1.2 to 1.3GHz.

$$\omega = \frac{1}{\sqrt{LC}}$$

Using the inductor value and quality factor, we can determine the parallel resistance R_p modelling the loss in the inductor. The resulting R_p is $1.44k\Omega$; the reciprocal of R_p is $696 \mu A/V$. So, we need a gm much higher than this value for oscillations to occur. The cross-coupled NMOS transistors are set to a 120-nm finger width with 47 fingers each. This results in a gm of $1.842 mA/V$, a value much greater than the minimum mentioned above. Our required output peak-to-peak swing is 1 V, swinging about 500 mV. Given that we already know our required swing and R_p , we compute the current I_{ss} flowing through the current source above the tank circuit.

$$V_{out|pp} = \frac{4}{\pi} I_{ss} R_p \rightarrow \frac{\pi}{4} \frac{V_{out|pp}}{R_p}$$

The minimum required I_{ss} to sustain a high enough swing of 1 V peak-to-peak is 545.4 μA . This calculated current, however, is way too large and results in degraded phase noise (as will be seen in the following section). We therefore set the PMOS transistor which acts as our current source at 25 fingers with a finger width of 120 nm. This gives us a total width of 3 μm resulting in an I_{ss} of around 284 μA , nearly half the theoretical value above. Therefore, we see a smaller swing at the outputs of the VCO, but these can be converted into digital square waves by the two CMOS inverters connected to the outputs of the VCO.

$$V_{out|pp}(\text{theoretical}) = \frac{4}{\pi} I_{ss} R_p = \frac{4}{\pi} (284 \mu A)(1.44 k\Omega) \approx 520.7 mV$$

$$V_{out|pp}(\text{real}) = 656mV$$

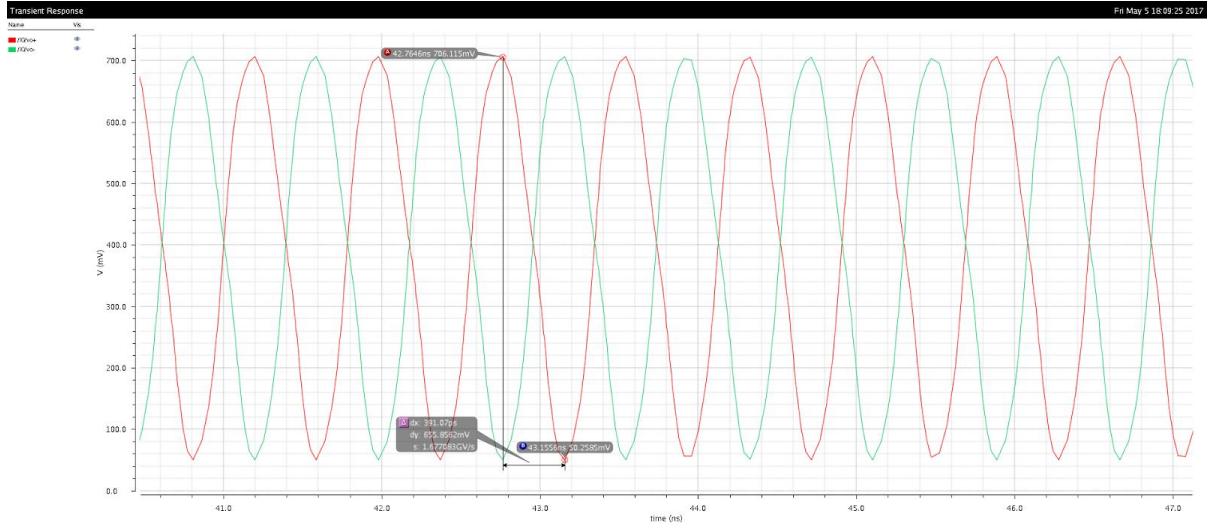


Figure 38. VCO output swing when I_{SS} is $284 \mu\text{A}$.

As mentioned before, the output of the VCO is rectified by the CMOS transistors, although the duty cycle of their outputs is slightly skewed because of the low swing of their inputs. This behavior is shown later to have little to no effect on the final output of the PLL.

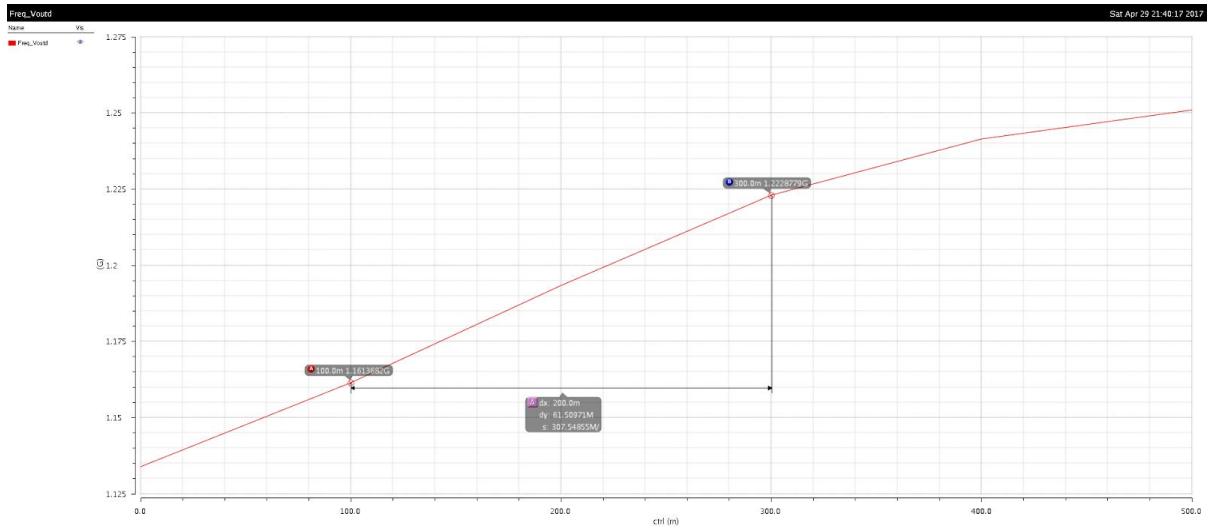


Figure 39. LC VCO Frequency (Hz) versus Control Voltage (mV)

The sensitivity of the LC VCO (K_{vco}) is 295 MHz/V with a tuning range going from 1.135 GHz to 1.25 GHz as the control voltage was increased from 0 to 500 mV.

As the sensitivity (K_{vco}) is increased, this leads to more instability in the system and so K_{vco} should be set to a range that is just large enough to allow the entire system to be stable, i.e. to allow the control voltages dictated by the loop filter to stabilize. It is therefore critical that K_{vco} is not too large and at the same time not too small as to create too narrow a tuning range.

As mentioned before about tuning range, the varactors were chosen such that we could achieve a tuning range from 1.135 GHz to 1.25 GHz. Theoretically, the difference $C_{max} - C_{min}$, would be given by the following equation:

$$C_{max} - C_{min} = 2C(1 - \Delta\omega\sqrt{LC})$$

As per the above equation, the theoretical value for the range of the varactors is 3.12 pF. This is an unusually high number and so is incorrect. The empirical range of the varactors used for the LC VCO is 904.8 fF, which provides the 115 MHz range from 1.135 GHz to 1.25 GHz for control voltages from 0 to 500 mV.

4.3.2.5 Phase Noise

The LC VCO can achieve excellent phase noise since its tuning range is narrow (the two are typically involved in a trade-off). It is for this very reason that Ring VCOs have poor phase noise as well. Another trade-off found in the LC VCO is between the source current I_{ss} and phase noise - as one is increased the other is reduced and vice versa. Initially, the I_{ss} of our LC VCO was set to 545.4 μ A (the current source PMOS was initially set to 49 fingers). Because of this, the phase noise was shown to degrade to -94.97 dBc/Hz.

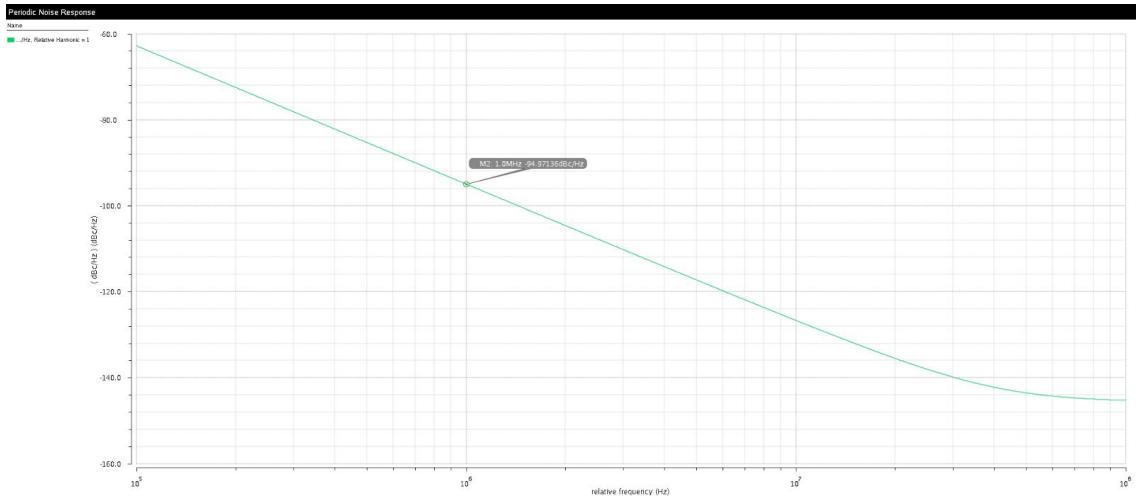


Figure 40. LC VCO phase noise when I_{ss} is $545.4 \mu\text{A}$

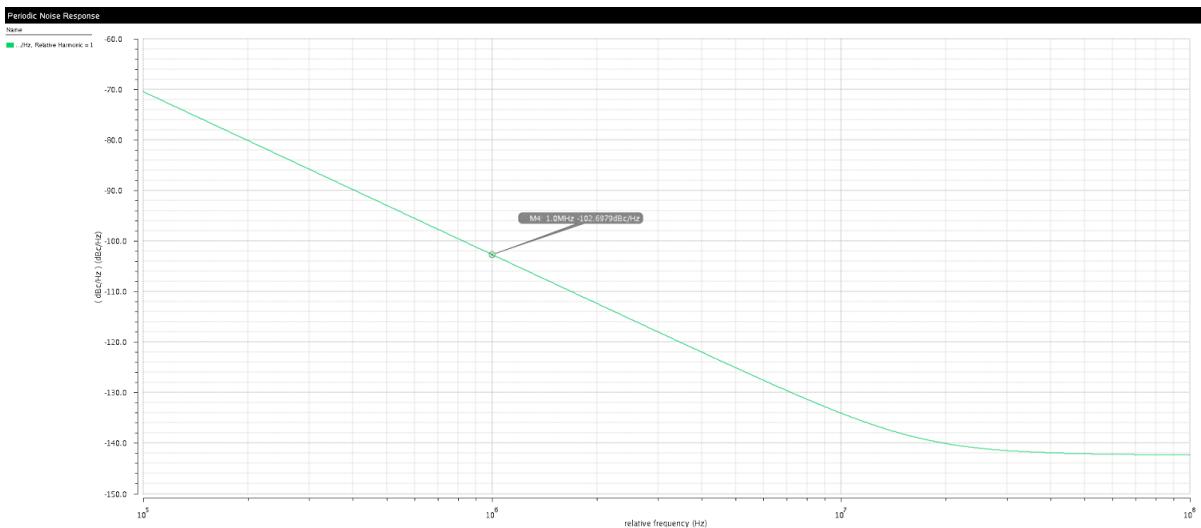


Figure 41. LC VCO phase noise when I_{ss} is reduced to $284 \mu\text{A}$

After the fingers of the current source PMOS were reduced to 25 (nearly half of the initial value of 49), the current I_{ss} came down to $284 \mu\text{A}$, which resulted in a phase noise of -102.7 dBc/Hz , a slightly better value. If the current were made any lower than this, the VCO output swing would start to drop even further, which results in the duty cycle of the square

wave outputs of the CMOS inverters to also degrade. Therefore, it was a judicious decision to keep current source I_{ss} at 284 μ A.

4.3.2.6 Summary

Finally, after having tackled all the above problems, the LC VCO specifications can be summarized in the table below.

Table 5 LC VCO final specifications

Specification	Value
Quality Factor	20
Parallel Resistance (R_p)	1.44 k Ω
Phase Noise	-102.7 dBc/Hz
Tuning Range	115 MHz
Output Swing	655 mV

4.4 FREQUENCY DIVIDER

The frequency divider reduces the frequency from the output of the VCO so that it is like the reference frequency when they are both compared in the PFD. This is a very important component because it allows the PLL to produce an output with a much higher frequency than the reference. For this project, the final frequency of the single-ended CMOS PLL is 1.2 GHz with a reference frequency of 150 MHz which means the VCO output must be divided by 8.

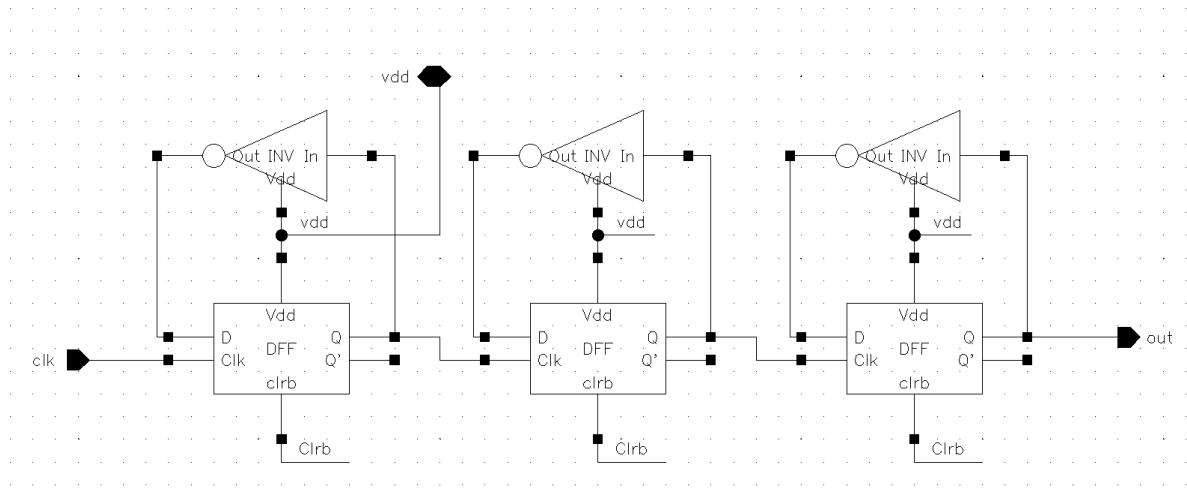


Figure 42 Single-ended Feedback Divider (Divide by 8)

The single-ended divider topology is simple; the output of each flip-flop becomes its own inverted input and the clock of the next one. Each D flip-flop divides the frequency of its input by two. Despite having an inverted output available from the flip flops, it was necessary to use the inverters to stabilize the outputs.

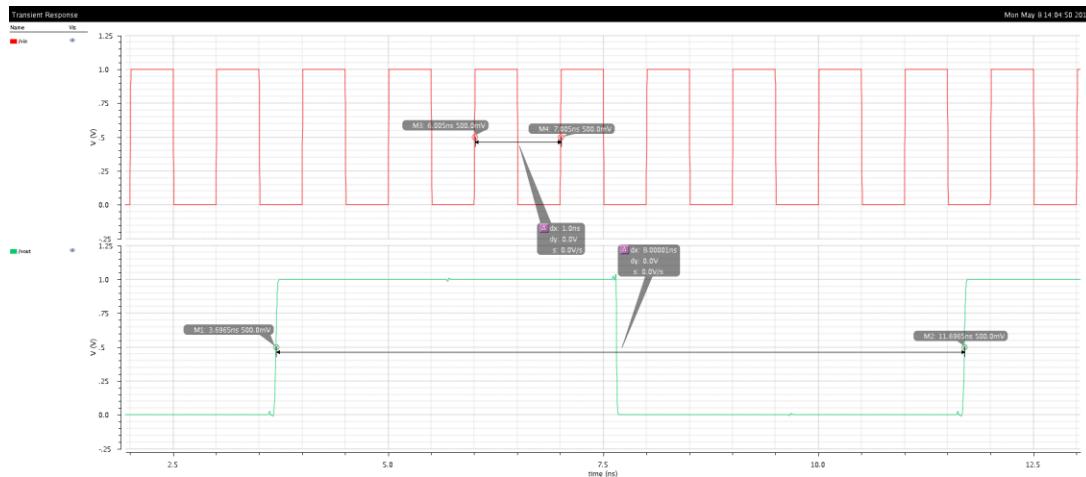


Figure 43 Results of single-ended Feedback Divider

The STSCL feedback divider is almost identical to its single-ended counterpart. The use of inverters was not necessary with this design.

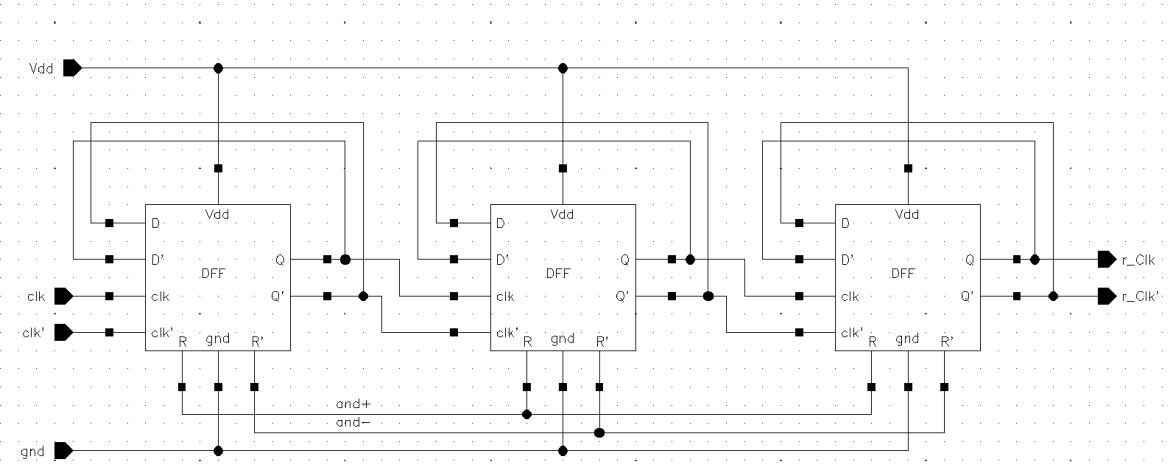


Figure 44 STSCL Feedback Divider (Divide by 8)

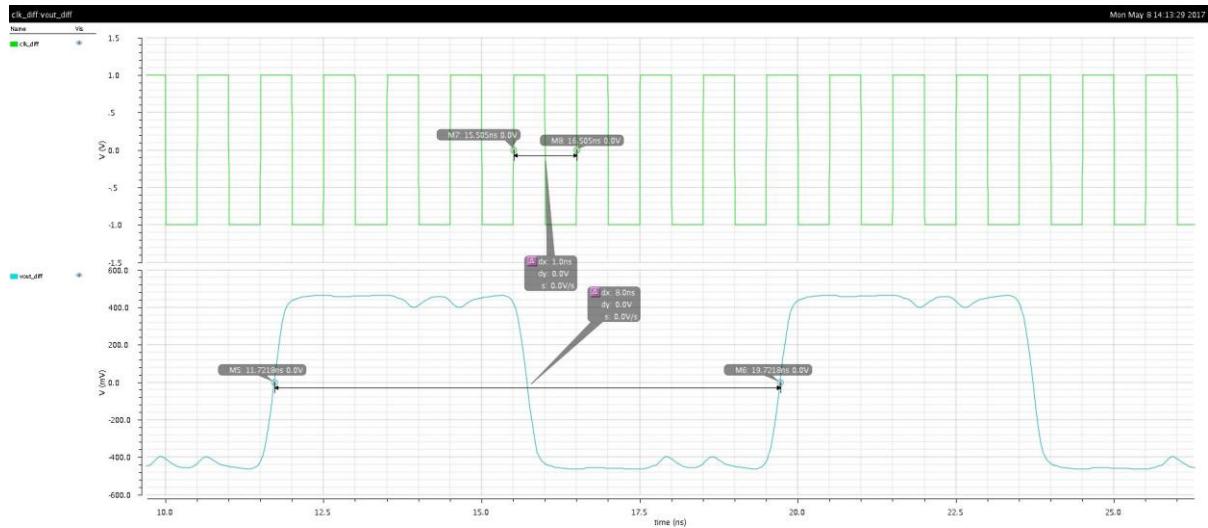


Figure 45 STSCL feedback divider results

4.5 LOOP FILTER

The loop filters used in the regular CMOS-based PLL and the STSCL low-power PLL are essentially identical. The only difference is that the STSCL PLL has two loop filters because there are two control voltages coming from the charge pump.

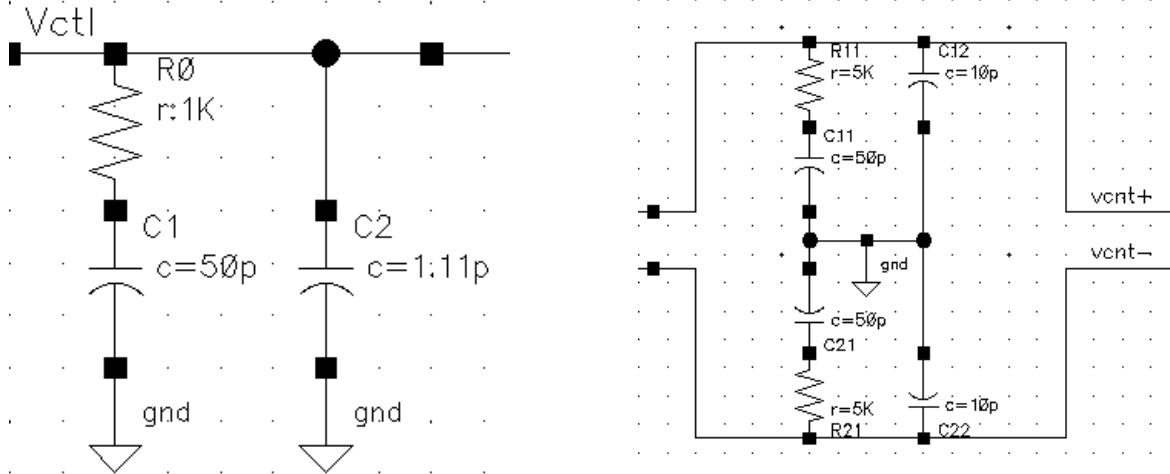


Figure 46. Single-ended Loop Filter (left) versus differential Loop Filter (right)

The differential loop filter ensures the stability of the entire PLL. Without this block, the PLL will not be able to lock the output frequency to the reference frequency. The loop filter does this by adding two poles and one zero to the system, ensuring zero steady-state error and closed-loop stability.

The loop filter is made up of a resistor and capacitor (R_1 and C_1) in series, followed by a second capacitor (C_2) in parallel. In the differential case, it is important to have two loop filters, one on each control line going to the VCO.

The transfer function of the loop filter is simple to derive based on its functionality. It converts a current coming from the charge pump into a voltage that controls the VCO. Based on this, we can see that the transfer function of the loop filter is of the form:

$$H_{LF} = \frac{V_{out}}{I_{in}}$$

It is quite self-evident that the loop filter's transfer function is its effective impedance.

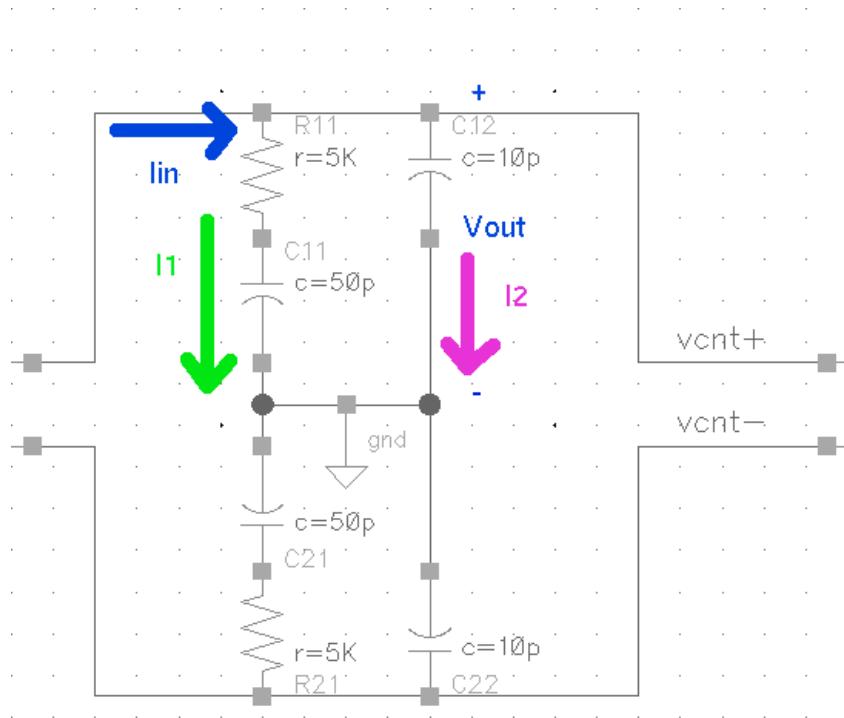


Figure 47. Currents coming from charge pump into the loop filter

We can see clearly that the total current I_{in} going into the loop filter is split (per KCL) into two currents I_1 and I_2 , charging the capacitors C_{11} and C_{12} (which represent C_1 and C_2) respectively. We can find the expressions for these two currents easily.

$$I_1 = \frac{V_{out}}{R_1 + \frac{1}{sC_1}}$$

$$I_2 = sC_2 V_{out}$$

$$I_{in} = I_1 + I_2 = V_{out} \left(\frac{1}{R_1 + \frac{1}{sC_1}} + sC_2 \right)$$

Using the above equations, we get our transfer function for the loop filter, which reduces to the following form:

$$H_{LF}(s) = \frac{V_{out}}{I_{in}} = \frac{1 + sR_1C_1}{s(C_1 + C_2)[1 + s\left(\frac{C_1C_2}{C_1 + C_2}\right)R_1]}$$

We see from the transfer function of the loop filter that it provides the system with two poles and one zero. The pole at zero turns the PLL into a Type-2 PLL which is essential for its functionality as this removes steady state errors for both step and ramp inputs [2].

After the transfer function of the loop filter was derived, it was time to do some Matlab modelling to figure out how much stability in terms of phase margin the loop filter provided. This was later combined with the VCO transfer function to understand how much overall phase margin the system had.

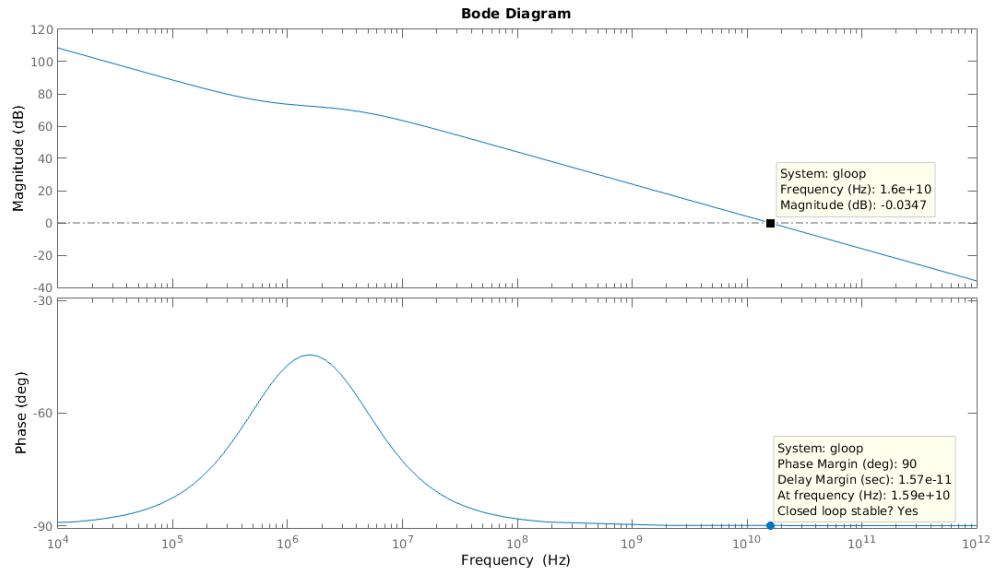


Figure 48. Loop filter Bode plot with gain crossover frequency and phase margin when $R_1 = 5k\Omega$, $C_1 = 50pF$, and $C_2 = 10pF$,

It is imperative to size the resistor and capacitors of the loop filter to satisfy two main issues within the PLL: 1) To make sure the current fed into the loop filter from the charge

pump is equal to the current going out of the loop filter back into the charge pump; 2) To make sure the PLL has enough phase margin and still lock.

Through experimentation with the charge pump and loop filter together, the resistor and capacitor values that provided equal currents in and out of the charge pump were $5k\Omega$ and $50pF$ respectively (R_1 and C_1 values). Using the transfer function of the loop filter derived earlier, we get a phase margin of 90° at a gain crossover frequency of 16 GHz for the loop filter. The value of C_2 was set to 10 pF because, at this value, the ripple was minimized to around 10 to 20 mV, reasonably small fluctuations on the control lines to the VCO.

After the loop filter's frequency response was characterized, it was time to see how much phase margin the open loop system had. This is a critical part of designing a PLL because without enough margin the PLL would be susceptible to instability, meaning that the overall, closed-loop gain of the PLL will be unbounded ($H(s) = \infty$). The output phase would therefore keep increasing indefinitely and the PLL would never lock.

To ensure that the closed-loop system is stable, we need to analyze the open-loop system first. The two are related as per the commonly known equation:

$$H(s) = \frac{G(s)}{1 + G(s)}$$

$G(s)$ is the open-loop system transfer function and $H(s)$ is the closed-loop system transfer function. Now, $H(s)$ will be unstable if its magnitude is unbounded, i.e., it goes to infinity. This can happen if the denominator $1 + G(s) = 0$. Therefore, $G(s) = -1$ makes the closed-loop system unstable.

$$G(s) = -1 \rightarrow |G(s)| = 1; \angle G(s) = 180^\circ$$

Because $G(s) = -1$ causes an instability, we need to find where this point occurs and make sure that we have enough margin built in so that our system can account for changes in functionality due to process variations. The loop filter is critical in making sure that we have enough phase margin in our PLL.

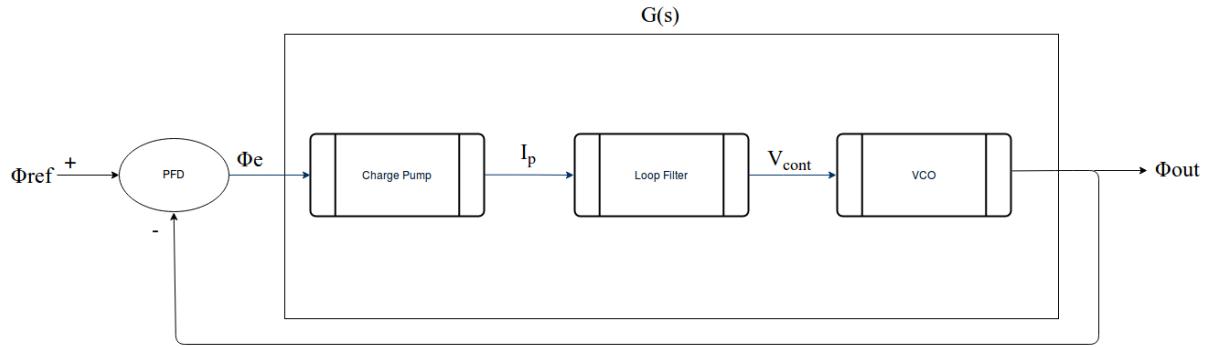


Figure 49. Closed loop PLL system with emphasis on $G(s)$, the open-loop transfer function

The open loop transfer function $G(s)$ comprises the charge pump, loop filter and VCO. The PFD is excluded as, for the sake of simplicity, it acts as a “difference” circuit. The open-loop system $G(s)$ takes the input phase error Φ_e and outputs Φ_{out} , the final output phase. $G(s)$ is given by:

$$G(s) = \frac{\Phi_{out}}{\Phi_e}(s) = \frac{K_{vco}I_p}{2\pi} \left(\frac{1 + sR_1(C_1 + C_2)}{(C_1 + C_2)s^2} \right)$$

K_{vco} as mentioned before assumes the value 295 MHz/V. The term I_p is the current going through the charge pump when the differential inputs UP and DOWN are turned on and is 84.5 μ A. Using the prior mentioned values of R_1 , C_1 , and C_2 , we can determine the open loop transfer function $G(s)$.

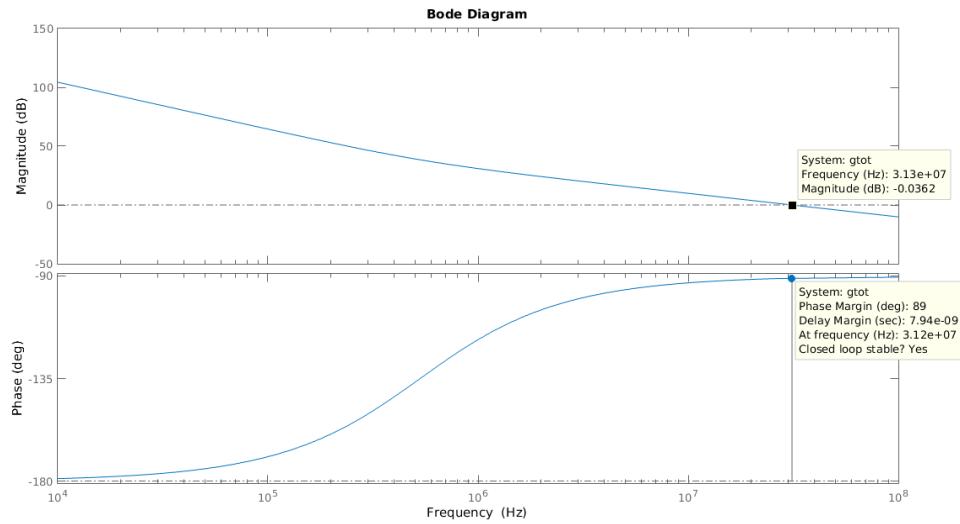


Figure 50. Bode plot of open-loop transfer function $G(s)$ with gain crossover frequency and phase margin

The phase margin of the open loop system $G(s)$ is 89° , quite a substantial amount of margin for the closed-loop system to be stable across process variations.

5 OVERALL DESIGN AND RESULTS

5.1 A Short Description on Design Methodology

After all the individual blocks were designed, it was time to put them all together and simulate the whole system. In a sense, this project employs a bottom-up approach instead of a top-down approach. The individual blocks were first designed, simulated, and characterized first instead of characterizing the whole system first and then going down to design the various blocks. The bottom-up approach, although it has problems of its own, was helpful because we could optimize each separate block (PFD, CP, etc.) and this helped us focus our efforts purely on each block first to make sure they function as per the assigned specifications.

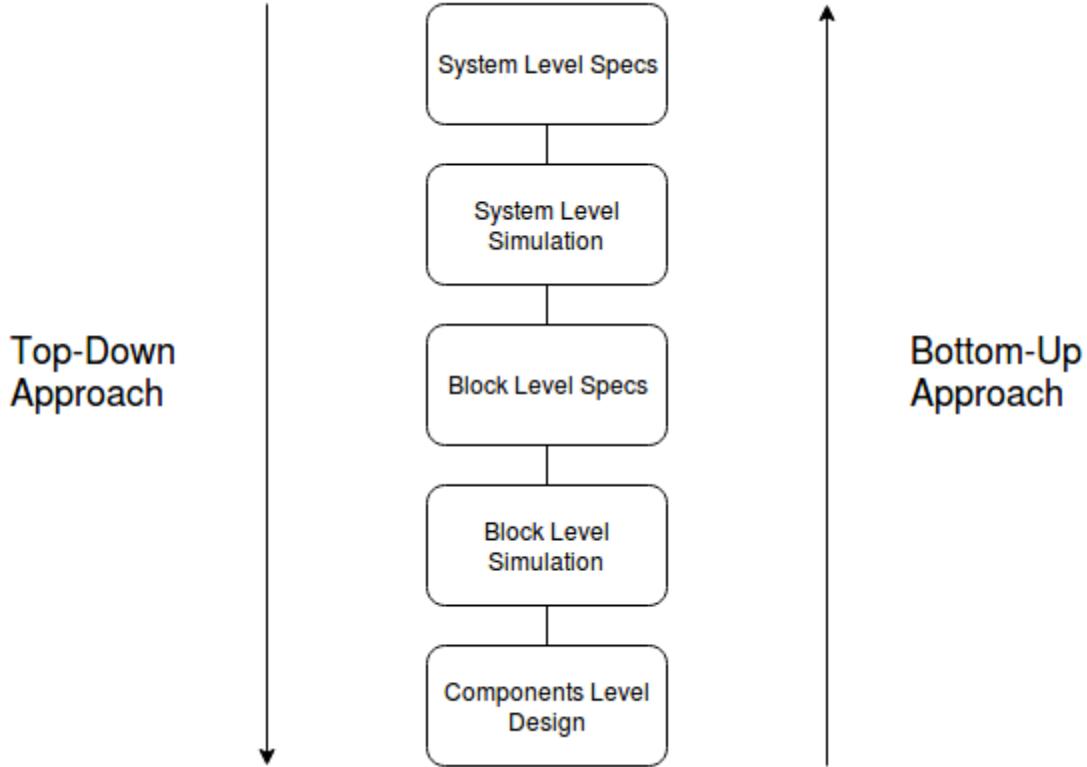


Figure 51. Top-down and Bottom-up design methodologies

In contrast, if we had gone with a top-down approach, we could've solved the design problems as well, but we would have had to keep iterating on a system level if our individual blocks didn't meet the overall system specifications. Instead, we focused on each individual block's specifications which were much easier to deal with. Furthermore, we wanted to understand each circuit block at a transistor level first and then build up on this knowledge to achieve each block's specified performance level.

5.2 Final System Level Design

With all blocks connected, the STSCL PLL was finally simulated and tested. The overall PLL design wasn't perfect right from the start so each individual block had to be readjusted, with the design and simulation process of each block being iterated.

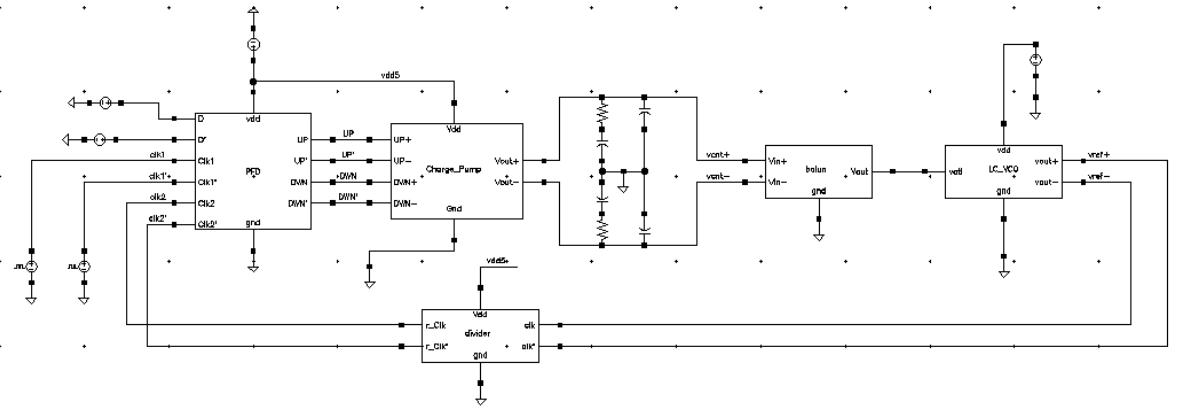


Figure 52. Final STSCL PLL system diagram

The PFD takes in a 150 MHz reference signal comparing it to the output from the frequency divider which is assumed to be close to this frequency range but out of phase. The PFD then computes the phase difference and hands this information to the charge pump which converts it to a current. The currents from the charge pump charge and discharge the two loop filters appropriately, changing the two differential control voltages. These control voltages in turn are converted to a single-ended control voltage by the balun (a 1:1 transformer) and sent to the VCO. The VCO's frequency, which is in the order of 1.2 GHz, changes accordingly and is sent back to be divided. This process goes on till the VCO output finally reaches a value very close to 1.2 GHz.

5.3 PLL Results and Comparisons

As mentioned before, both PLLs were tested under specific conditions to check whether it locked the output to the reference signal. To this end, a 150 MHz reference was used to

produce a 1.2 GHz output signal which was then fed back to the divider. The divider reduced the output, converting it in the range of 150 MHz.

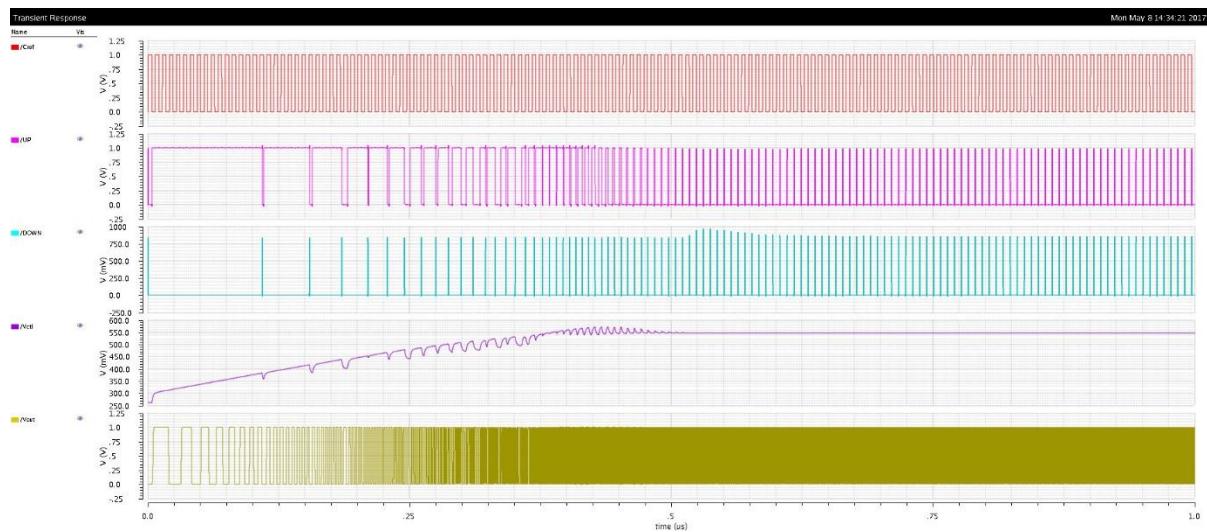


Figure 53 Single-ended CMOS PLL results

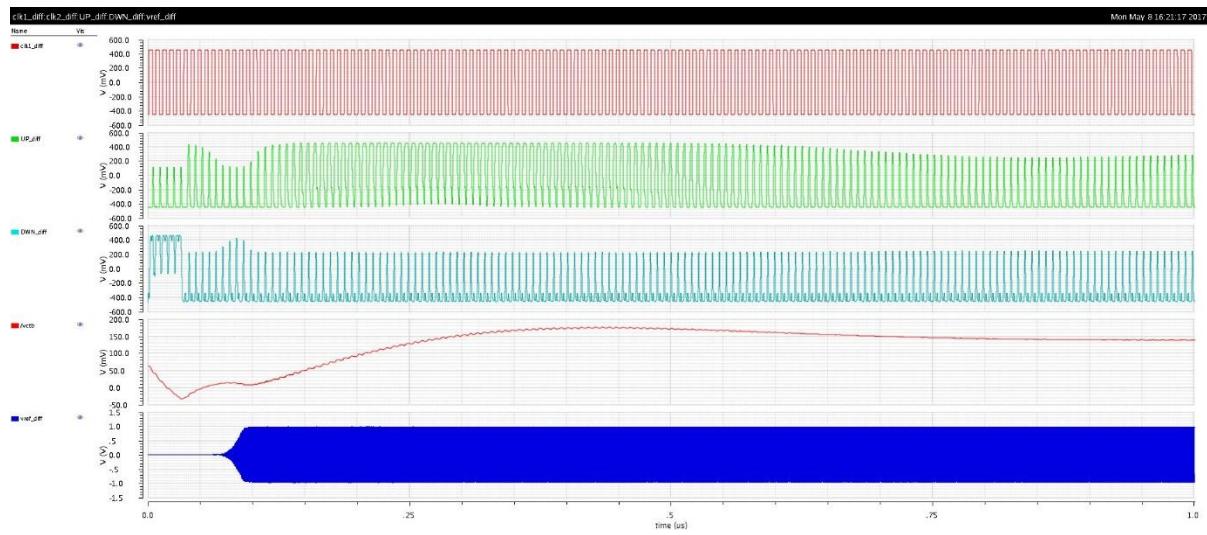


Figure 54 Differential STSCL PLL results

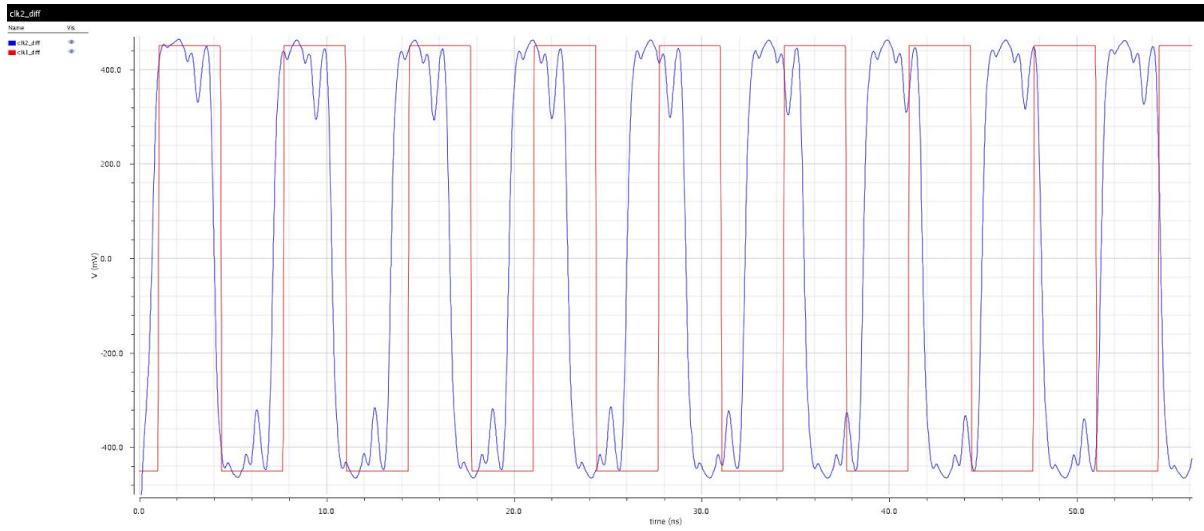


Figure 55. STSCL PLL output at the start of simulation from 0 to 50 ns

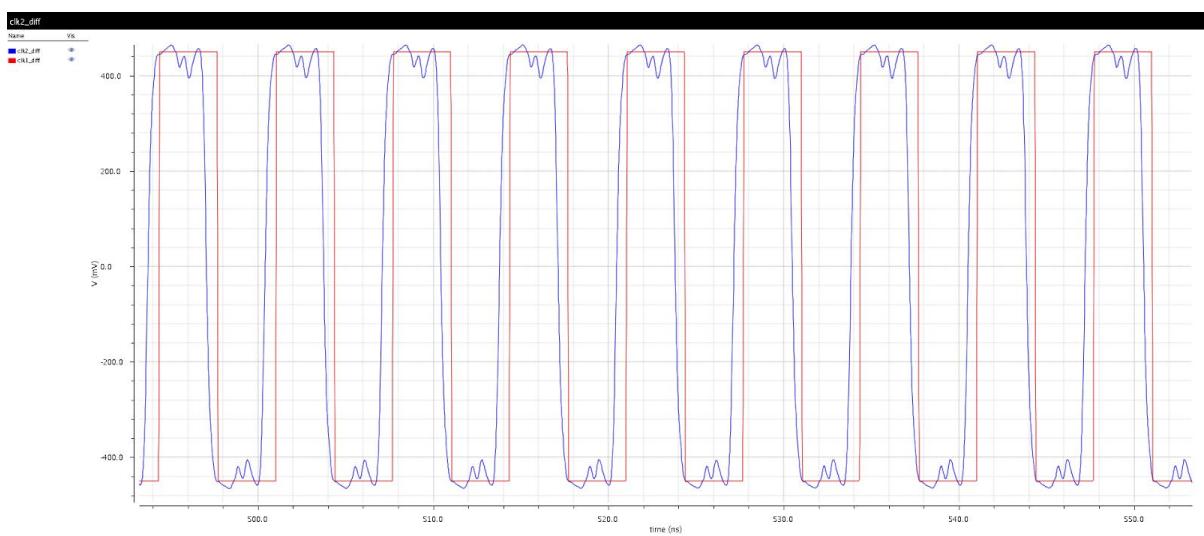


Figure 56. STSCL PLL output from 500 ns to 600 ns

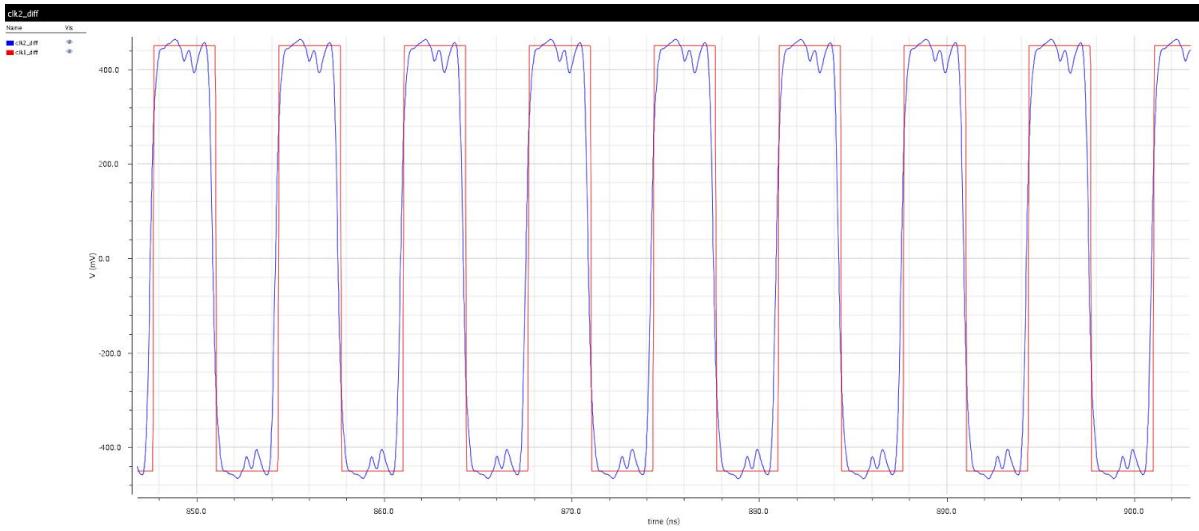


Figure 57. STSCL PLL output from 850 ns to 900 ns (approximate lock time)

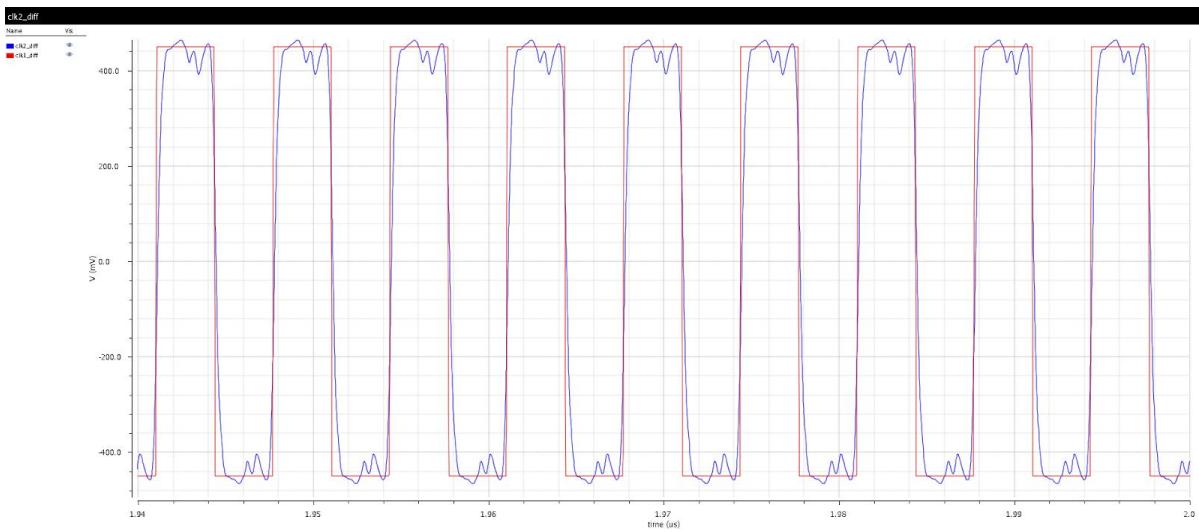


Figure 58. STSCL PLL output from 1.94 us to 2.0 us showing output still in lock

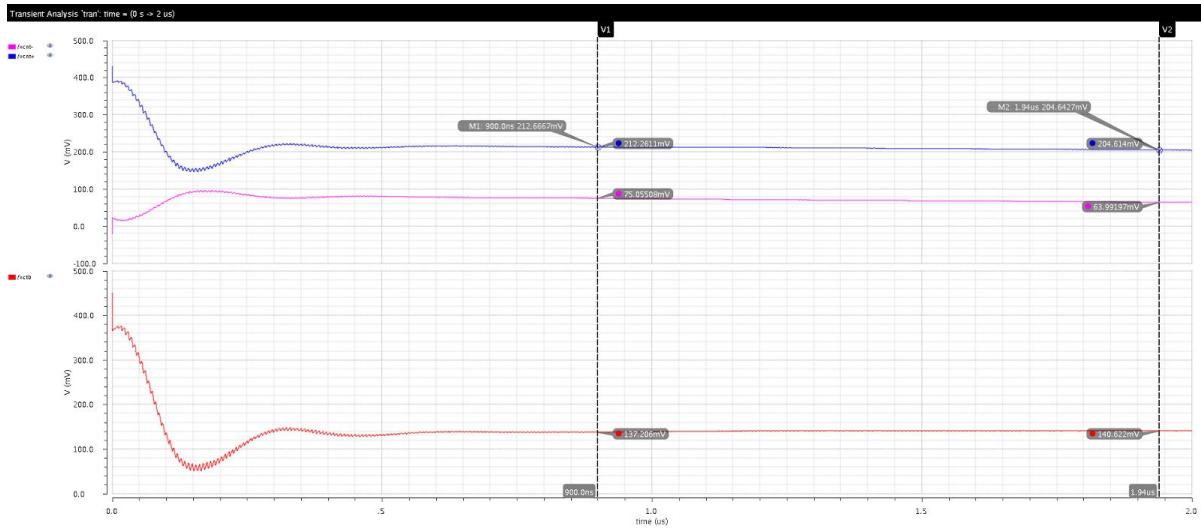


Figure 59. STSCL PLL control voltages showing stabilization at 900 ns and 1.94 us

We see that the STSCL PLL locks the output after about 900 ns. This can also be confirmed by observing the control voltages above. Finally, the table below summarizes the results of the differential STSCL PLL.

Table 6. STSCL low-power PLL Specification Summary

Specifications	Value
Supply Voltage	500 mV and 1 V (only for VCO)
Order	3
Type	2
Phase Margin	89°
Lock Time	~ 900 ns
Average Power Consumption	371.7 μ W
Reference frequency	150 MHz
Output frequency	1.2 GHz
Phase Noise	-102.7 dBc/Hz @ 1 MHz offset

The power consumption of the single-ended PLL is approximately $61.6 \mu\text{W}$, much lower than the STSCL PLL (which has an average power consumption of $371.7 \mu\text{W}$). This is because the latter uses an LC VCO while the former employs a Ring VCO. However, since the Ring VCO in STSCL has extremely high sensitivity and degraded phase noise, it is not used in this version.

6 CONCLUSION AND FUTURE WORK

6.1 Concluding Remarks

This report delineates the design and functionality of a low power differential Phase-Locked Loop constructed based on Subthreshold Source Coupled Logic (STSCL). The report goes over the introduction and motivations behind this design, mainly focusing on the importance of low power in many electronic applications today. The report then describes the bottom-up methodology used to design the differential PLL, starting from the component level, to the separate blocks of the PLL and all the way to the system level. Throughout the report, comparisons are made between the differential PLL and a single-ended CMOS PLL. The Phase-Frequency Detector, Charge Pump, Loop Filter, Voltage-Controlled Oscillator and Divider are all described in detail after which they are put together, simulated and fine-tuned to achieve the desired locking functionality. Both PLLs were shown to lock for a reference frequency of 150 MHz, with a final output of 1.2 GHz.

6.2 Future Work

We would like to continue to improve the PLL described in this report by exploring a wider range of frequencies. One idea is to sweep the reference frequency from 150 MHz to

300 MHz and above and to observe how the output responds. Now, the LC VCO has a narrow tuning range because we are using only two varactors. In the future, we would like to build a capacitor bank within the LC VCO which accounts for a much wider tuning range, thereby allowing the PLL to lock at a variety of frequencies. Our goal is to reach 1.2 GHz to 3.6 GHz if possible.

Another problem we want to tackle is layout. Due to time constraints, we could ascertain how the finished integrated circuit would look or how much space it would take up. One other reason that contributed to this problem was that the gpdk45 process didn't have corresponding layout elements and had to be done with a 65-nm process instead. Since we were working only with the 45-nm process, this would have been cumbersome to take on in the short period we had to design this PLL. Having said this, we would like to embark on the layout process as well in the future and try to come up with area constraints and optimize the design accordingly.

7 APPENDIX A: PHYSICAL DEVICE SPECIFICATIONS

In this section, the physical specification of each component in the CMOS-based PLL and STSCL PLL will be described.

7.1 A.1 SINGLE-ENDED PLL COMPONENTS

7.1.1 A.1.1 Inverter

instance name	cell name	device type	(W/L) (nm/nm)
PM0	pmos1v_lvt	PMOS	155/45
NM0	nmos1v_lvt	NMOS	130/45

Table A.1.1. Inverter

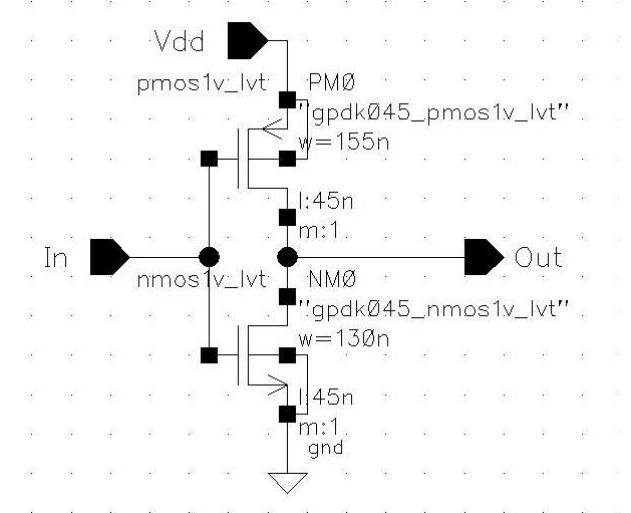


Figure A.1.1. Inverter

7.1.2 A.1.2 Transmission Gate

instance name	cell name	device type	(W/L) (nm/nm)
PM0	pmos1v_lvt	PMOS	155/45
NM0	nmos1v_lvt	NMOS	130/45

Table A.1.2. Transmission Gate

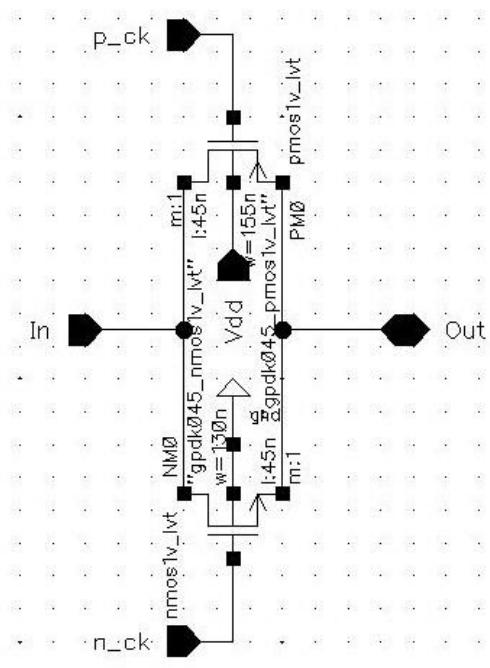


Figure A.1.2. Transmission Gate

7.1.3 A.1.3 NAND Gate

instance name	cell name	device type	(W/L) (nm/nm)
PM0	pmos1v_lvt	PMOS	155/45
PM1	pmos1v_lvt	PMOS	155/45
NM0	nmos1v_lvt	NMOS	260/45
NM1	nmos1v_lvt	NMOS	260/45

Table A.1.3. NAND Gate

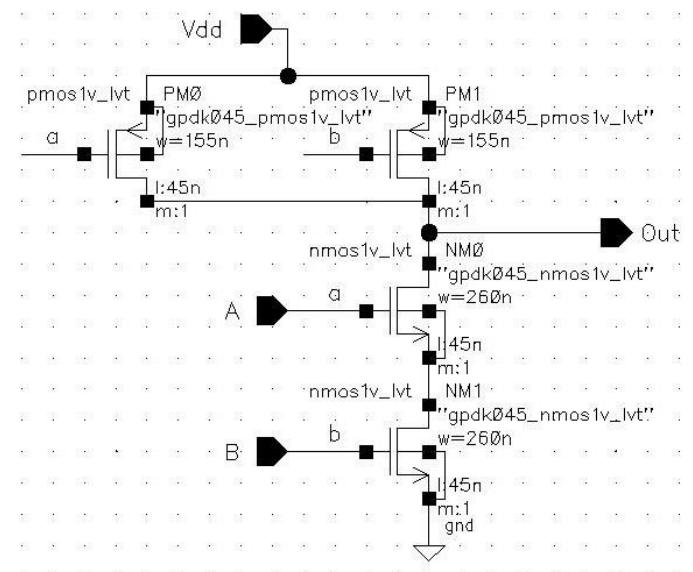


Figure A.1.3 NAND Gate

7.1.4 A.1.4 Charge Pump

instance name	cell name	device type	(W/L) (nm/nm)	instance name	device type	size
PM0	pmos1v_lvt	PMOS	1200/45	R0	resistor	30.38kΩ
PM1	pmos1v_lvt	PMOS	3100/45		resistor	40.52kΩ
PM2	pmos1v_lvt	PMOS	3100/45			
NM0	nmos1v_lvt	NMOS	480/45			
NM1	nmos1v_lvt	NMOS	3800/45			
NM2	nmos1v_lvt	NMOS	3800/45			

Table A.1.4. Charge Pump

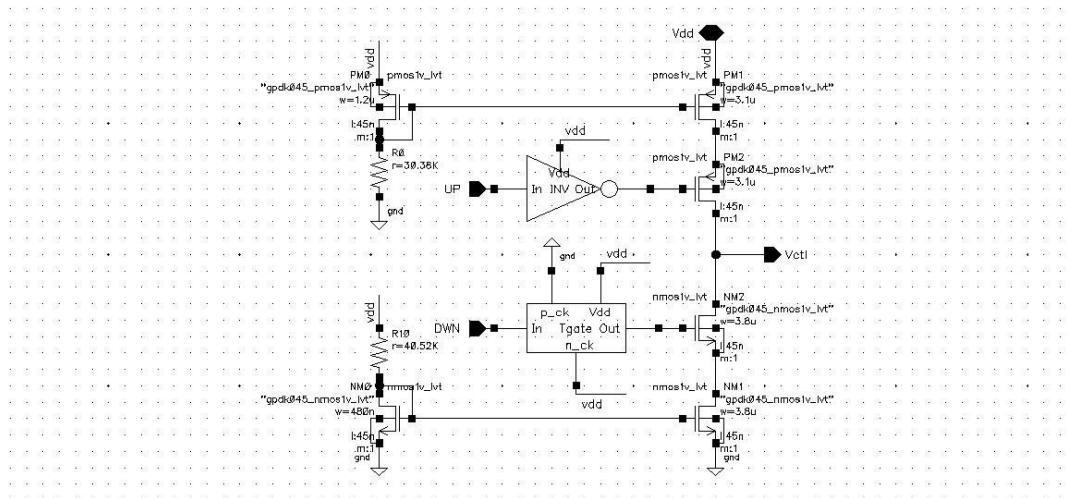


Figure A.1.4. Charge Pump

7.1.5 A.1.5 Loop Filter

instance name	device type	size
R1	resistor	$1k\Omega$
C1	capacitor	50pF
C2	capacitor	1.11pF

Table A.1.5. Loop Filter

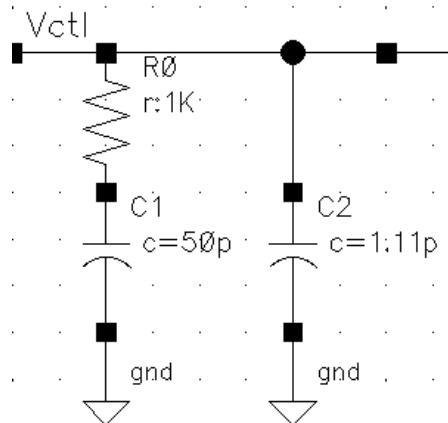


Figure A.1.5. Loop Filter

7.1.6 A.1.6 VCO Current Mirror

instance name	cell name	device type	(W/L) (nm/nm)
PM0	pmos1v_lvt	PMOS	155/45
NM1	nmos1v_lvt	NMOS	130/45

Table A.1.6. VCO Current Mirror

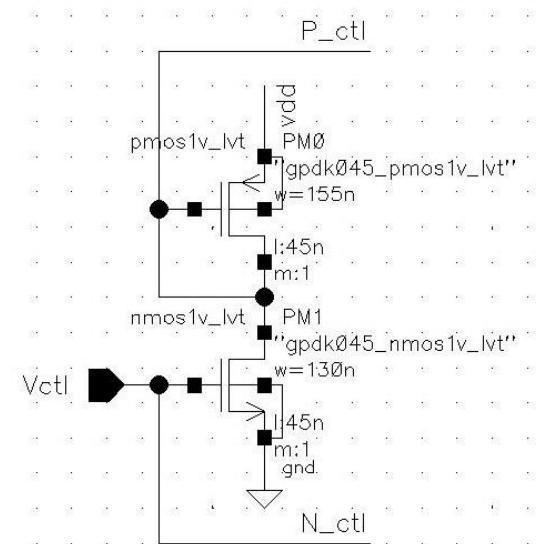


Figure A.1.6. VCO Current Mirror

7.1.7 A.1.7 Current-Starved Inverter

instance name	cell name	device type	(W/L) (nm/nm)
PM0	pmos1v_lvt	PMOS	305/45
PM1	pmos1v_lvt	PMOS	305/45
NM0	nmos1v_lvt	NMOS	280/45
NM1	nmos1v_lvt	NMOS	280/45

Table A.1.7. Current-Starved Inverter

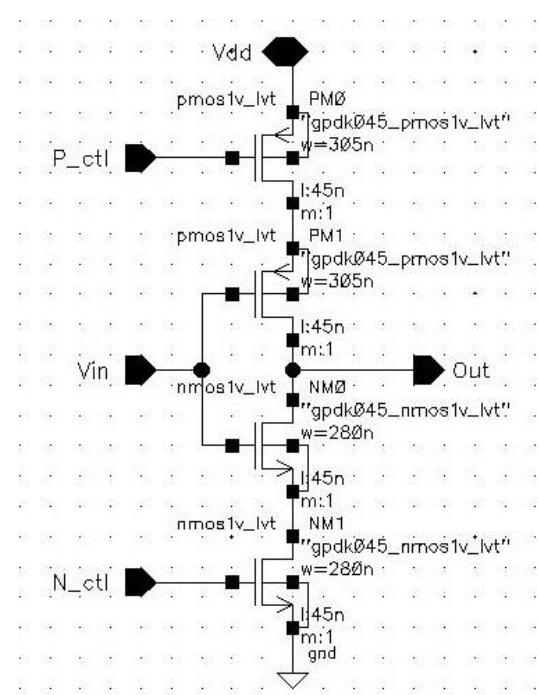


Figure A.1.7. Current-Starved Inverter

7.2 A.2 STSCL COMPONENT PARAMETERS

7.2.1 A.2.1 STSCL NAND Gate

instance name	cell name	device type	(W/L) (nm/nm)
PM0	pmos1v_lvt	PMOS	120/45
PM1	pmos1v_lvt	PMOS	120/45
NM0	nmos1v_lvt	NMOS	1200/45
NM1	nmos1v_lvt	NMOS	1200/45
NM2	nmos1v_lvt	NMOS	720/45
NM3	nmos1v_lvt	NMOS	720/45
NM4	nmos1v_lvt	NMOS	720/45
NM5	nmos1v_lvt	NMOS	1200/45

Table A.2.1. STSCL NAND Gate

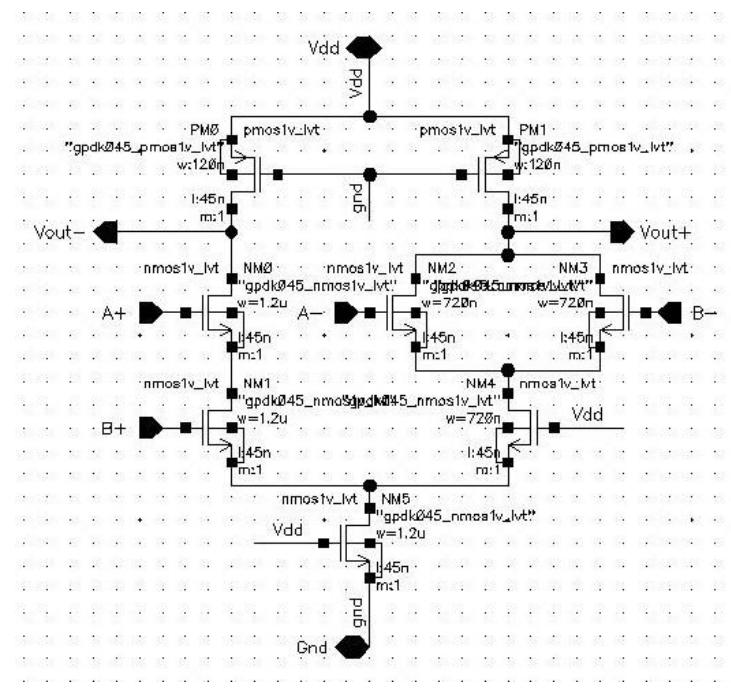


Figure A.2.1. STSCL NAND Gate

7.2.2 A.2.2 STSCL Latch

instance name	cell name	device type	(W/L) (nm/nm)	instance name	cell name	device type	(W/L) (nm/nm)
PM0	pmos1v_lvt	PMOS	150/45	NM3	nmos1v_lvt	NMOS	480/45
PM1	pmos1v_lvt	PMOS	150/45	NM4	nmos1v_lvt	NMOS	480/45
PM2	pmos1v_lvt	PMOS	450/45	NM5	nmos1v_lvt	NMOS	960/45
NM0	nmos1v_lvt	NMOS	480/45	NM6	nmos1v_lvt	NMOS	960/45
NM1	nmos1v_lvt	NMOS	480/45	NM7	nmos1v_lvt	NMOS	2888/45
NM2	nmos1v_lvt	NMOS	480/45				

Table A.2.2. STSCL Latch

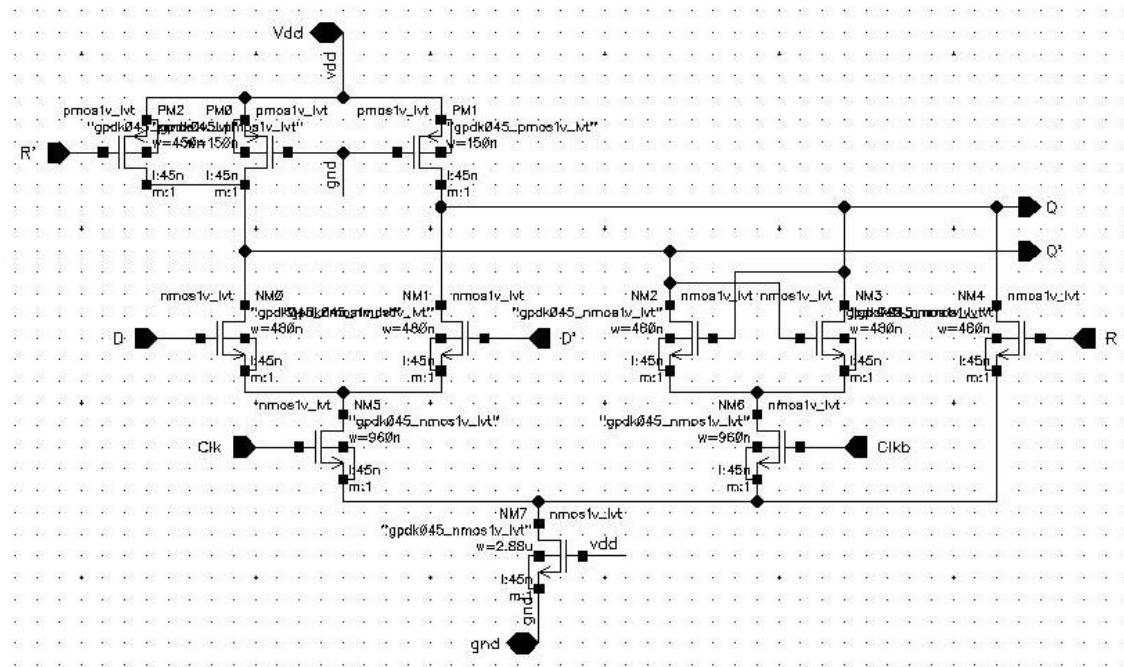


Figure A.2.2. STSCL Latch

7.2.3 A.2.3 STSCL Charge Pump

instance name	cell name	device type	(W/L) (nm/nm)
PM0	pmos1v_lvt	PMOS	16320/45
PM1	pmos1v_lvt	PMOS	8160/45
PM2	pmos1v_lvt	PMOS	8160/45
NM0	nmos1v_lvt	NMOS	6240/45
NM1	nmos1v_lvt	NMOS	6240/45
NM2	nmos1v_lvt	NMOS	12480/45

Table A.2.3. STSCL Charge Pump

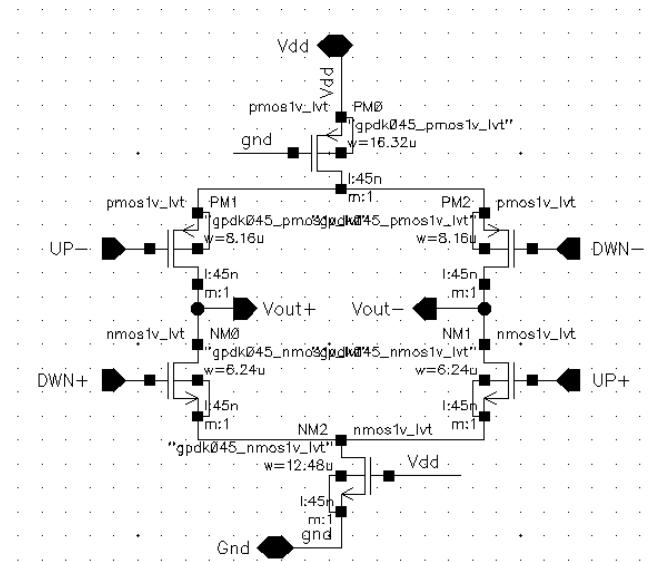


Figure A.2.3. STSCL Charge Pump

7.2.4 A.2.4 Differential Loop Filter

instance name	device type	size
R11	resistor	$5k\Omega$
C11	capacitor	$50pF$
C12	capacitor	$10pF$
R21	resistor	$5k\Omega$
C21	capacitor	$50pF$
C22	capacitor	$10pF$

Table A.2.4 Differential Loop

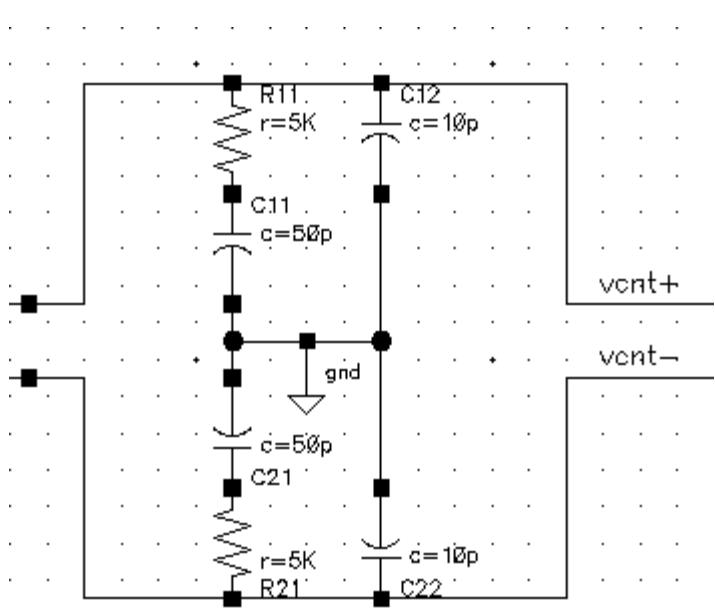


Figure A.2.4 Differential Loop Filter

7.2.5 A.2.4 Balun

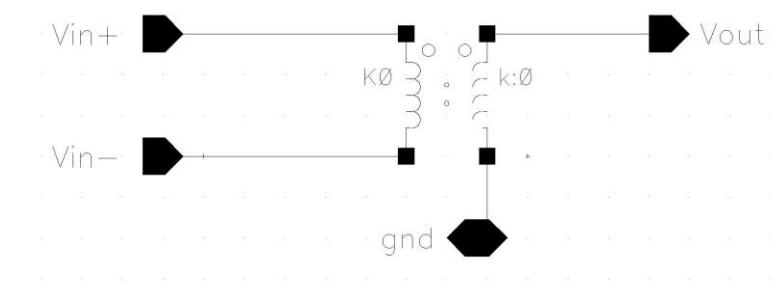


Figure A.2.4 Transformer acting as a Balun

7.2.6 A.2.5 LC VCO

instance name	device type	size	instance name	cell name	device type	(W/L) (nm/nm)
L0	resistor	8.795n	PM0	pmos1v_lvt	PMOS	5880/45
C0	capacitor	1.6p	PM1	pmos1v_lvt	PMOS	960/45
L1	capacitor	8.795n	NM0	nmos1v_lvt	NMOS	5640/45
C1	resistor	1.6p	NM1	nmos1v_lvt	NMOS	5640/45
MCN0	varactor	904.8f				
MCN1	varactor	904.8f				

Table A.2.5 LC VCO

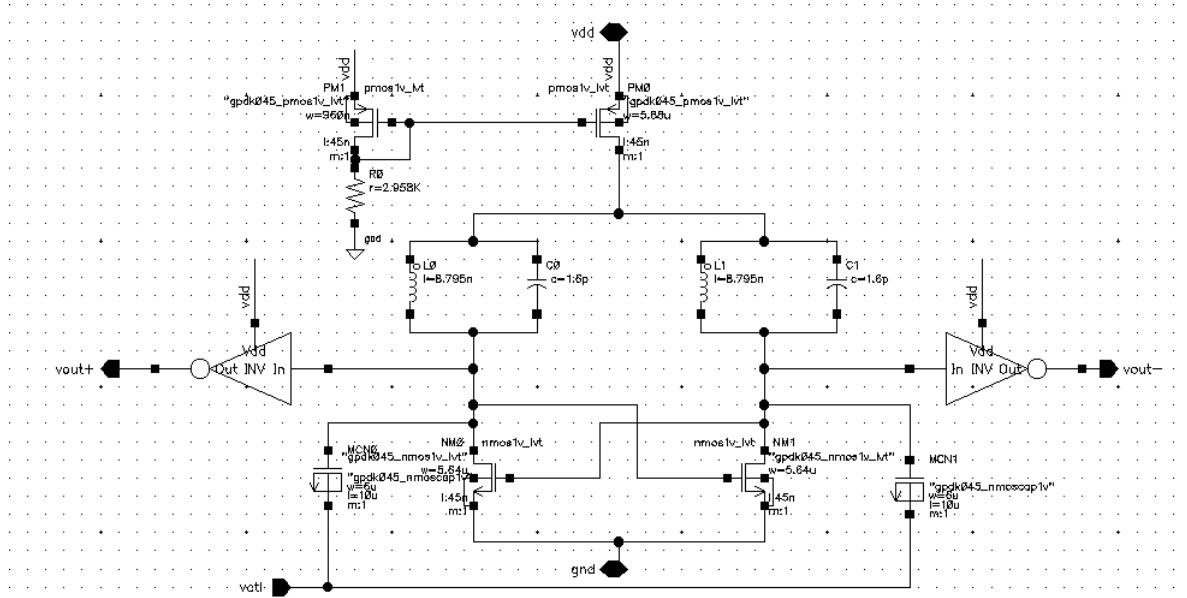


Figure A.2.5 LC VCO

8 APPENDIX B: K_{vco} DERIVATION

The following derivation is from [1]. The VCO's transfer function is simple to derive considering it takes in a voltage as an input and outputs a waveform with a particular phase. This waveform with said phase will oscillate at a frequency. We can define phase as the product of the angular frequency and time.

$$\varphi = \omega t$$

In broader terms, if the angular frequency varies with time and is therefore a function of time, the phase is defined as the area under the curve of (t) . Hence:

$$\varphi(t) = \int \omega(t) dt$$

From the defining equation of the output angular frequency of a VCO, we can get a transfer function like so:

$$\frac{\omega_{out}(t) - \omega_0}{V_{cont}(t)} = K_{vco}$$

Assuming $\omega_0 = 0$ and integrating the above equation, we can get our phase as follows:

$$\varphi(t) = \int \omega_{out}(t) dt = \int K_{vco} V_{cont}(t) dt$$

Taking the Laplace Transform of both sides, we can get something that looks like this:

$$\Phi(s) = \frac{K_{vco} V_{cont}(s)}{s}$$

Finally, this reduces to the more common transfer function form:

$$G_{vco}(s) = \frac{\Phi(s)}{V_{cont}(s)} = \frac{K_{vco}}{s}$$

9 REFERENCES

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