Ultra Low-Power Phase-Locked Loop using Subthreshold Source-Coupled Logic

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Introduction

Phase-Locked Loops (PLLs) are critical in numerous analog/mixed-signal applications such as clock-data recovery and frequency synthesizers in RFIC chips. Some of the main purposes of a PLL is to synchronize signals of different frequencies and to "lock" signals at desired frequencies.

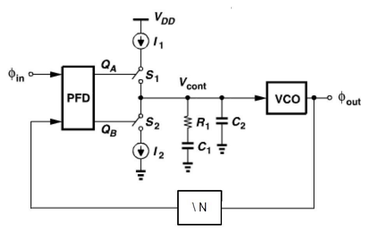
PLLs can be very power consumptive considering the aforementioned functions, and so the main focus of this project is to employ a low-power mode of operation with 45 nm MOSFETs to mitigate this problem. It has been known for a while that the Subthreshold (Weak Inversion) region of operation in modern day transistors is desirable for low-power applications and so was used during the design phase of this project. Furthermore, Source-Coupled Logic, a differential-based, current-steered logic family, was also used in order to create more robust, noise-immune, differential signals.

Design Approach

Key Points

- Low power consumption
- High voltage swing
- High locking frequency

System Diagram of a Phase Locked Loop



The PLL system can be summarized in the above block diagram. The PFD takes in a reference signal, comparing the VCO's output frequency with it. Depending on whether the VCO is running slower or faster compared to the reference, the PFD sends a "GO Faster" or "GO Slower" signal to the Charge Pump which then converts this into currents. These currents are used to charge and discharge the capacitors in the loop filter which in effect increases or decreases the control voltage to the VCO. This makes the VCO either speed up or slow down accordingly. This process is repeated until the output's frequency becomes equal to the input frequency.

Design Approach

Phase Frequency Detector

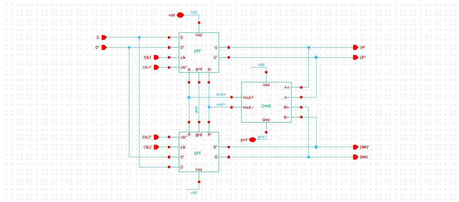


Figure 1: PFD Circuit Schematic

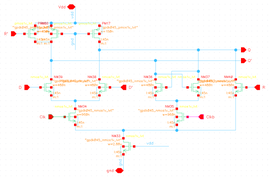


Figure 2: Latch circuit of DFF in PFD

The PFD uses sequential logic to detect and measure the phase difference between the reference clock (Φ_{ref}) and the feedback clock (Φ_{fb}) and outputs a voltage pulse proportional to the difference detected. The total DC power consumption of the PFD is 5 uW.

Charge Pump & Loop Filter

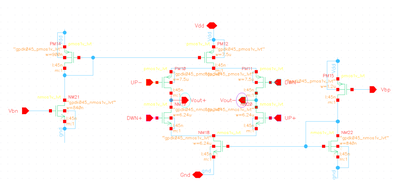


Figure 3: Charge Pump Schematic

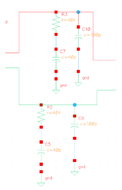


Figure 4: Loop Filter Schematic

The Charge Pump converts the differential signals from the PFD into currents that charge and discharge the loop filter placed between the positive and negative differential control voltage lines. The loop filter is based on a classic two-pole model, modified for differential signals. The total DC power consumption of the Charge Pump when in active mode is 18 uW

Voltage-Controlled LC Oscillator

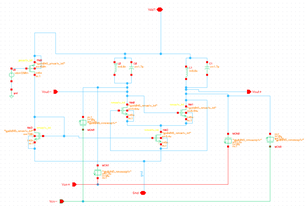


Figure 5: LC VCO Schematic

In order to test the PLL using a lower sensitivity VCO, an LC Oscillator operated at 1-V was used. This VCO has a small tuning range and so is less susceptible to changes in the control voltages. The sensitivity of the LC VCO is 41.96 MHz/V, and the phase noise is at -102 dBc/Hz. This LC VCO is not operated in Subthreshold region due to the enormous amounts of current required to sustain the oscillations at the outputs of the VCO. The total power consumption of the LC VCO is 489 uW.

Frequency Divider

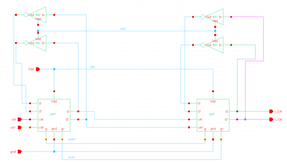


Figure 6: Frequency Divider Schematic

The frequency divider is made of three D-Flip Flops all operated in STSCL. It divides the output by a factor of 4. The total power consumption of the Frequency Divider is 224 uW. The divider was operated at 1 V like the VCO.

Results

The PLL locks reference frequencies of 150 to 300 MHz, outputting a 1.2 GHz square wave. The lock time is approximately 1-2 us. The total power consumption of the system is 750 uW. The final output swing was from 0 to 1 V single-ended (1 V swing peak-to-peak), and from -1 V to 1 V differential (2 V swing peak-to-peak).

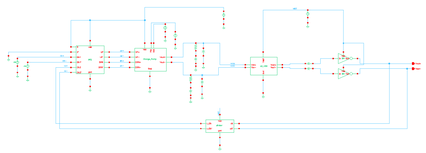


Figure 7: Complete Low Power PLL System Schematic

Main problems experienced during this project include fine-tuning of the charge pump, loop filter and VCO to accommodate proper locking with the PFD. The VCO sensitivity was adjusted in order to make the VCO lock at the correct output frequency of 1.2 GHz, which corresponded to a 300 MHz feedback from the frequency divider.

Summary

This project describes a low-power PLL which runs using STSCL logic using a standard 45-nm transistor process. The PLL provides high output frequency in the range of 1.2 GHz given low input reference frequencies in the range of 100-300 MHz. The total power consumption of the PLL is 750 uW with differential voltage swings of 1 V (-500 mV to 500 mV).

Key References

[1] Cheng, S. et al. "Design And Analysis Of An Ultrahigh-Speed Glitch-Free Fully Differential Charge Pump With Minimum Output Current Variation And Accurate Matching". *IEEE Transactions on Circuits and Systems II: Express Briefs* 53.9 (2006): 843-847. Web.

[2] Collins, Diarmuid. "A Fully Differential Phase-Locked Loop With Reduced Loop Bandwidth Variation". Graduate. National University of Ireland, Maynooth, 2011. Print.

[3] Razavi, Behzad. *RF Microelectronics*. 2nd ed. New York: Pearson Education, Inc, 2012. Print.

[4] Kanitkar, Hrishikesh. "Subthreshold Circuits: Design, Implementation, And Application". Master's of Science in Electrical Engineering. Rochester Institute of Technology, New York, 2009. Print.

[5] Magnelli, Luca et al. "Design Of A 75-Nw, 0.5-V Subthreshold Complementarymetal–Oxide–Semiconductor Operational Amplifier". *International Journal of Circuit Theory and Applications* (2012): 3. Web. 21 Apr. 2017.

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