# Design and Simulation of LC-VCO for Bluetooth in 45-nm CMOS

Victor Abarca and Raghav Kumar

Department of Electrical Engineering

San Jose State University

San Jose, CA

Abstract— This paper explores the design of a 2.35 to 2.55 GHz tunable, LC tank-based, voltage-controlled oscillator targeted at Bluetooth applications. The design operates on a 1-V power supply with 826  $\mu W$  DC power consumption, and has a 15-ns settling time, 2.4-V max peak-to-peak output swing with phase noise of -90.5 dBc/Hz.

Keywords— Voltage Controlled Oscillator, Bluetooth Radio, LC VCO, varactor, 45-nm

## I. Introduction

## A. General Definition and Operation

The VCO is a critical component in all radio designs. It is essential for use in upconversion and downconversion transceivers. It provides the "LO" signal to the mixers in both Heterodyne and Direct-conversion transceivers in order to perform up- and down-conversion. It is typically integrated into a phase locked loop. This allows it to be tuned to the desired frequency as needed, and feedback-controlled so it does not drift given noise due to thermal changes in the system.

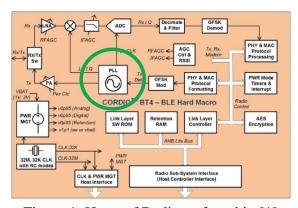


Figure 1. Heart of Radio as found in [1]

There are generally two types of VCOs that are commonly used - 1) LC-VCO (as depicted in

this paper), and 2) Ring VCO. The two have their respective advantages and disadvantages as described in [2] and are shown in the table below.

Table 1. Waveform oscillator (Ring) vs Resonant oscillator (LC) [2]

Oscillator type	Waveform oscillator	Resonant oscillator
Architecture	Ring	LC-tank
Power	Low	High
Area	Small	Large
Tuning range $^a$	Large	Small
Phase noise performance	Poor	Excellent

 $<sup>^{\</sup>rm a}$  The tuning range represents the frequency range covered by the VCO.

It is clear that the LC VCO (or the Resonant oscillator), although it consumes a lot more power and takes up more space, has excellent phase noise capability which is important for a VCO. The Ring oscillator has other advantages such as smaller area and less power consumption along with a high tuning range. However, the Ring VCO has poor phase noise which is often its greatest weakness.

Therefore, for the purpose of this paper, the design of the LC-VCO will be undertaken and described thoroughly.

## B. VCO Specifications

The **VCO** specifications have been following summarized in the table. These specifications will help design guide considerations and method by which the LC VCO will be designed.

Specification	Value
Tail current I <sub>ss</sub>	1 mA
Output peak-to-peak voltage $V_{o,pp}$	1 V
Tuning range $\Delta f_{osc}$	2.35 GHz - 2.55 GHz (200 MHz)
Center frequency	2.45 GHz
Supply Voltage $V_{DD}$	1 V
Quality Factor Q	40

# II. VCO Design Considerations

## A. Criterion for Oscillations in VCO

The most widely used VCO design for RF applications is the cross-coupled LC VCO. It consists of two LC tank circuits (an inductor in parallel with a capacitor) along with two cross coupled NMOS transistors. This is shown in Figure 2. The two transistors generate a phase shift of 360° which sustains the oscillations of the LC tank circuit. We can also say that the two transistors provide enough gain in the circuit to sustain these oscillations. It is for this reason that the transconductance of the two NMOS transistors is set as big as possible. Usually, a current source is connected below the two NMOS transistors to DC bias them. This VCO structure and description can be found in the detailed work provided in [3].

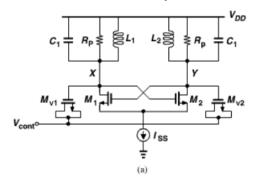


Figure 2. LC VCO with cross-coupled transistors

The parallel resistance  $R_p$ , which is the parallel loss resistance of the inductor, and the transconductance  $g_m$  of the amplifying transistors are related. They form an important criterion that, if not met, will lead to no oscillations at the output.

$$g_m R_p \gg 1$$
 (1)

$$g_m \gg \frac{1}{R_p}$$
 (2)

So, in order to ensure that oscillations do occur, the transconductance needs to be much greater than the reciprocal of the parallel loss resistor.

## B. Output Swing & Component Selection

When the current source is at the bottom, the output will swing about  $V_{DD}$  (in our case, this is 1 V). The output peak-to-peak swing is related to the amount of current  $I_{ss}$  flowing through the current source and how big the resistance  $R_p$  is. The swing relationship is explained using the following equation:

$$V_{o,pp} = \frac{4}{\pi} I_{SS} R_p \tag{3}$$

Given a specific peak-to-peak output voltage and  $I_{ss}$  current, this relationship can be used to determine the required parallel loss resistance  $R_p$ .

The requirement for  $I_{SS}$  is roughly 1 mA and the peak-to-peak voltage swing is 1  $V_{pp}$  differential or 0.5  $V_{pp}$  single-ended.

With such requirements, the theoretical value for  $R_n$  is as follows:

$$R_p = \frac{\pi}{4} \left( \frac{V_{pp}}{I_{ss}} \right) = \frac{\pi}{4} \left( \frac{1 V}{1 mA} \right) \approx 785.4 \Omega (4)$$

Using this value of  $R_p$ , we can estimate the inductance as well as the series resistance  $R_s$  in the LC tank.

$$R_p = \omega LQ \to L = \frac{R_p}{\omega Q}$$
 (5)

$$R_{S} = \frac{R_{p}}{Q^{2}} \tag{6}$$

Using the above equations, the values for Land  $R_s$  are 1.28 nH and 981.75 m $\Omega$  respectively.

To get the LC tank oscillating, we not only need the value of L but also the value of  $C_1$ . The center frequency is given as 2.45 GHz which is in the middle of the required tuning range of the LC VCO. This, along with the value of Lcan be used to find the capacitance  $C_1$ .

$$\omega_{osc} = \frac{1}{\sqrt{LC_1}} \rightarrow C_1 = \frac{1}{\omega^{-2}L} \tag{7}$$

The value of  $C_1$ , according to the above equation, is calculated to be 3.3 pF.

Lastly, from the first and second equations from subsection A, we can find the required transconductance  $g_m$  of the two amplifying transistors in the LC VCO.

$$g_m \gg \frac{1}{R_p} = \frac{1}{785.4 \,\Omega} = 1.273 \, mA/V(8)$$

Therefore, the transconductance of the two amplifying transistors need to be higher than 1.273 mA/V in order to provide sufficient oscillations.

## C. Tuning Range

As described in [2] and [3], the LC VCO has a narrower tuning range compared to the Ring VCO. The tuning range is set by the two varactors connected to the outputs of the LC VCO.

The varactors act as extra variable capacitors that add to the capacitance value of  $C_1$  in the LC tank circuit. By doing so, the varactors can change the output frequency of the VCO.

$$\omega_{osc} = \frac{1}{\sqrt{L(C_1 + C_{var})}} \tag{9}$$

If the varactors go from some minimum value  $C_{min}$  to a maximum value  $C_{max}$ , then we can estimate the tuning range of the LC VCO by manipulating equation (9) above.

$$\Delta\omega_{osc}\approx\frac{1}{\sqrt{LC_{1}}}\left(\frac{C_{max}-C_{min}}{2C_{1}}\right) \qquad (10)$$

The values of  $\Delta\omega_{osc}$ , Land  $C_1$  are given. Using these values, the varactor range can be calculated resulting in the required tuning range of 200 MHz.

$$C_{max} - C_{min} \approx \Delta \omega_{osc} 2C_1 \sqrt{LC_1}$$
 (11)

Using the above estimation, the varactor range comes out to be around 539.03 fF.

## D. Comparisons between Topologies

Placing the tail current at the bottom has certain disadvantages as explained thoroughly in [1] and [3]. These disadvantages are 1) The output oscillates about the supply voltage, putting stress on the varactors and eventually damaging them; 2) The tuning range is much smaller because the varactor capacitance range is not fully utilized.

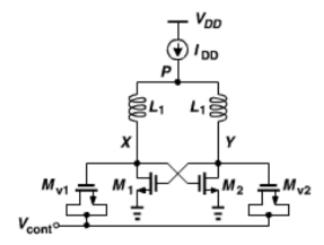


Figure 3. LC VCO with tail current at the top

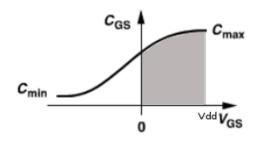


Figure 4. Usable range of varactor capacitance when tail current is at bottom

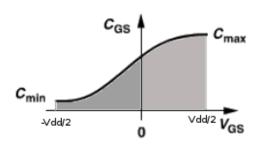


Figure 5. Usable range of varactor capacitance when tail current at top

The current source being placed at the top can bias the voltage at point P to be  $\frac{V_{dd}}{2}$ . This helps reduce the stress on the varactors at the output and increase the range of usable capacitances of the varactors, effectively increasing the tuning range of the VCO.

## III. VCO Design Method

The LC VCO was designed using the toptail topology described in the previous section due to its obvious advantages over the bottom-tail one.

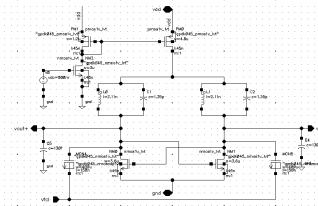


Figure 6. VCO Schematic from Cadence Virtuoso

The top-tail topology is realized by using a current mirror at the top of the LC tank circuit in order to sink a DC current of approximately 1 mA.

In addition to the capacitor  $C_1$ , the LC VCO also has a load capacitor of 130 fF which needs to be taken into account. As a result, the value of  $C_1$  will have to be changed from the original theoretical value to a smaller value in order for the

VCO to resonate at a center frequency of 2.45 GHz.

Contrary to the theoretical values for L and  $C_1$  derived in the previous section, the real values of the two are quite different. This is because the LC VCO had to be tweaked in order to get a linear frequency vs control voltage plot. In other words, the gain or sensitivity of the VCO needs to be, for the most part, constant over the tuning range. Another reason for this fine-tuning is to ensure the voltage at the top of the LC tank is set to a value very close to  $\frac{V_{DD}}{2}$  since the topology being used is with the tail current at the top.

For the above reasons, the inductor L is increased from 1.28 nH to 2.11 nH and the capacitor  $C_1$  is reduced to 1.35 pF from 3.3 pF. The varactor's value is also tweaked from the original, theoretical value of 539.03 fF to 904.8 fF.

The series resistance of the inductor is set to 812 m $\Omega$  instead of the theoretical value of 981.75 m $\Omega$ . Although the inductance and series resistance values are changed, the quality factor remains at 40.

The transistors are sized accordingly to provide a transconductance of 2.77 mA/V. This value is nearly twice as large as the theoretical value of 1.273 mA/V found in the previous section of this paper.

In the next section, it will be shown that these real values result in an output peak-to-peak roughly twice the calculated value. This is partly because a tail current of 1 mA is a substantial amount, which results in greater output excursions.

## IV. Results & Summary

The LC VCO was simulated to understand its behavior and to evaluate whether it meets or exceeds the specifications from section I of this paper.

## A. Gain $(K_{vco})$ Results

One of the most important criteria is the gain ( $K_{vco}$ ) of the LC VCO. We wanted to find out whether this specification was more or less constant over the tuning range. As described in the figure below, we see that the output frequency of the VCO is fairly linear from 0 to 0.5 V and only begins experiencing nonlinearities from 0.6 V to 1 V. This

shows that  $K_{vco}$  is fairly constant over the required range between 2.35 GHz and 2.55 GHz.

The gain can be expressed in the following way:

$$K_{vco} = \frac{\partial \omega_{out}}{\partial V_{cont}} \tag{12}$$

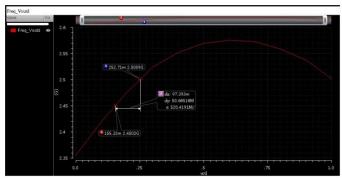


Figure 7. VCO frequency versus control voltage

The gain for this LC VCO is calculated to be roughly 520 MHz/V taking the above definition into consideration.

## B. Output Swing Results

A transient simulation was then conducted in order to determine whether the LC VCO oscillates with proper swing, meeting or exceeding the aforementioned requirements. The LC VCO settled pretty quickly from the trip point, sustaining constant amplitude oscillations at around 15 ns.

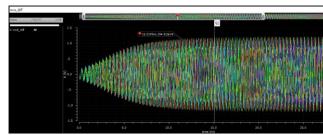


Figure 8. All outputs of LC VCO showing average settling time of 15 ns

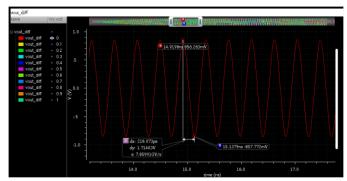


Figure 9. Lowest swing (1.71 V) at Vcont = 0 V

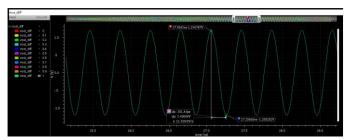


Figure 10. Highest swing (2.4 V) at V cont = 1 V

The output swing of the LC VCO based on the above figures is roughly double the requirement. From Figure 9 it is apparent that the lowest swing is around 1.71  $V_{pp}$  and the highest swing is around 2.4  $V_{pp}$  seen in Figure 10. The output swing clearly exceeds the specification outlined in Table 2, but this is expected since the LC VCO is sinking a large DC current (around 1 mA).

## C. Power Consumption Results

The DC power consumption of this VCO is fairly simple to obtain. It usually involves multiplying the supply voltage by all the branches drawing a DC current. It can be summarized as follows:

$$P_{DC} = V_{DD}I_{DC} \tag{13}$$

Now, in the case of this LC VCO, the supply voltage is 1 V and two branches exist - one for the tail current at the top of the LC tank, and one for the current mirror. The tail current is  $633.2~\mu A$  and the current mirror consumes  $193.0~\mu A$ . So the

total current sunk by the current source is (633.2 + 193.0)  $\mu A = 826.2~\mu A$ . Therefore, this translates to a DC power consumption of  $826.2~\mu A * 1~V = 826~\mu W$ . This can be confirmed by the DC power consumption report in Cadence.

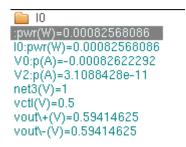


Figure 11. DC power consumption of LC VCO showing 0.826 mW

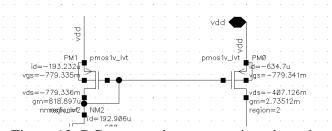


Figure 12. DC currents in current mirror branches

After DC power consumption came switching (or transient) power consumption. Once a transient analysis was conducted on the VCO, the transient power consumption graphs were viewed in the Results Browser option in Cadence Virtuoso. Using this feature, we found how much power the VCO consumes when oscillating.

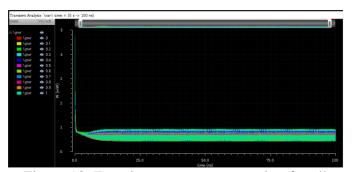


Figure 13. Transient power consumption for all values of Vcont

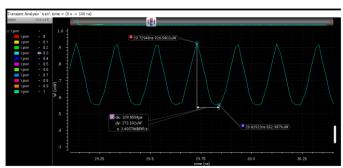


Figure 14. Maximum transient power consumption at Vcont = 300 mV

The switching power consumption was roughly between 0.4 mW to 0.9 mW as the control voltage  $V_{cont}$  was varied from 0 V to 1 V by 100 mV increments. The maximum peak power consumption was 0.93 mW which was reached when the control voltage was set to 300 mV.

#### D. Phase Noise Results

Although Phase Noise wasn't specified in Table 2, it tends to be vital for VCOs because they are typically the final block of a PLL. If the VCO's phase noise characteristics are poor, the output phase will be constantly disturbed, leading to jitter issues. This could also lead to locking problems in the PLL. Furthermore, in RFICs, phase noise in local oscillators (typically VCOs/PLLs) can corrupt the desired signal during downconversion from RF to IF during the presence of an interferer [1].

Keeping this in mind, the phase noise was simulated in order to understand the character of the LC VCO better.

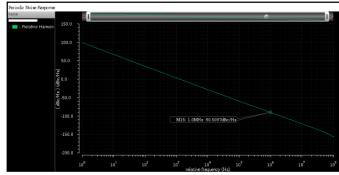


Figure 15. Phase Noise at 2.45 GHz beat frequency

For a beat frequency of 2.45 GHz, the phase noise was roughly -90.5 dBc/Hz at a relative frequency of 1 MHz. This amount of phase noise is poor considering the average LC VCO in the

market has upwards of -125 dBc/Hz or better. The phase noise will be improved in future revisions of this LC VCO design. However, phase noise depends on a few factors as outlined in [1]. These include - 1) the amount of noise different devices within the LC VCO inject (transistors, passives, etc); 2) the point in time when these devices inject noise (as during a transient simulation); 3) the output voltage swing (carrier power). Clearly, if the output peak-to-peak swing is reduced further, the phase noise can be improved beyond the current value.

## E. Design Summary

The complete design summary for the Bluetooth LC VCO can be seen in the table below. The LC VCO performed well in terms of settling time, tuning range and mostly constant sensitivity over the tuning range. The LC VCO can be improved in terms of phase noise along with reduced output swing and power consumption.

Table 3. Results Summary of LC VCO

Specification	Value
$K_{vco}$	520 MHz/V
Tuning Range $\Delta f_{osc}$	2.35 GHz - 2.55 GHz
Supply voltage $V_{DD}$	1 V
DC Power Consumption $P_{DC}$	826 μW
Max Switching Power Consumption $P_{trans max}$	930 μW
Tail Current $I_{ss}$ or $I_{DD}$	826 μΑ
Maximum output peak-to- peak Voltage $V_{pp}$	2.4 V
Phase Noise	-90.5 dBc/Hz

Settling time	15 ns
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## V. Conclusions

The LC VCO described in this paper is designed for the Bluetooth range of frequencies between 2.35 GHz to 2.55 GHz. This paper details the VCO's specifications, some vital design considerations, the design methods used and finally, the results of the design. The specifications for the LC VCO include a particular DC tail current, output voltage swing, tuning range and quality factor. Some of the main considerations include the gain/sensitivity ( $K_{vco}$ ), output swing ( $V_{pp}$ ), tuning (which is also a spec), and transconductance of the amplifying transistors to provide oscillations. Using these specifications and common considerations, the LC VCO was designed and adjusted for best results. The results of the design were finally discussed and summarized. Some of the results, such as phase noise, weren't optimized and therefore will be considered in more detail in future works.

## References

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- [2] D. Collins, "A Fully Differential Phase-Locked Loop With Reduced Loop Bandwidth Variation", Masters Thesis, National University of Ireland, Maynooth, 2011.
- [3] R. Kumar and V. Abarca, "Differential Low-Power Phase-Locked Loop in 45-nm STSCL Logic", Masters Thesis, San Jose State University, 2017.