High Figure-of-Merit Bluetooth LNA in 45nm CMOS

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***Abstract*— This paper details the design of an LNA using gpdk45 transistors as amplifiers along with ideal inductors with a quality factor of 10. The goal of the design was to meet certain specifications: linearity, gain, reflection, noise immunity, and DC power consumption. Once these specifications were met, the LNA performance was quantified using a "Figure of Merit" that combined all the above specifications.**

***Index Terms*— Low Noise Amplifier, common source, inductive source degeneration, quality factor, internal resistance, impedance matching, smith chart, noise figure, linearity.**

I. INTRODUCTION

The Low Noise Amplifier (LNA) is the first and most critical part of the transceiver chain in any RFIC. It is used to amplify very weak signals and add the least amount of noise possible. LNAs have many stringent specifications such as gain, linearity, power consumption, and noise figure to name a few and meeting them all includes many trade-offs between these parameters. Noise figure is a key parameter because adding too much noise to an already weak input signal would distort it beyond recognition.

Perhaps the most important design limitation is the power consumption which will place a limit on how much gain the LNA can produce as well as the size of the MOSFET used. The gpdk045 CMOS low voltage technology is used due to its advantageous qualities such as low power consumption, better relative noise and gain compared to larger technologies.

Matching the input signal to the LNA was a very critical objective of this project. Since the input signal is very weak, RF mismatch at the MOSFET gate will result in most of the signal being reflected and never being amplified by the LNA. This is why the reflection constraint is -10dB for an operating band of 100 MHz (from 2.4GHz to 2.5GHz).

The goal of this LNA is to achieve the following final parameters in the previously mentioned operating band.

Table 1. Low Noise Amplifier specifications

|S11|	< -10dB
Voltage Gain	>15dB
Noise Figure	<3.5dB
DC Power Consumption P_{dc}	<2mW
P_{1dB}	>-10dBm

Two widely used LNA configurations are the common-source and common gate. Common-source LNAs have a high gain, good noise performance, and a narrower bandwidth which is beneficial in isolating only desired signals to be amplified [1].

The basic common-source amplifier topology was required for this project with the freedom to make modifications if necessary.

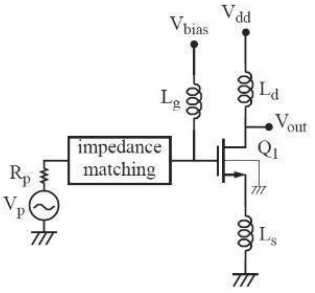

Figure 1. Common Source LNA topology

Placing an inductor at the source creates the commonly used Inductive Source Degeneration (SID) configuration. Source degeneration generates the real part at the input impedance which is important because there is no real part in there

without degeneration [2]. This inductor provides negative feedback to the amplifier which stabilizes the gain and reduces the noise figure [3]. It lessens the effects of nonlinear distortion by lowering V_{gs} relative to the input voltage. The major downside to this setup is the reduced gain for a given input voltage.

II. Proposed Final Design Schematic

The proposed LNA design is shown in figure 2. Adding a capacitive load was the only modification made to the basic design. This was done to shift the gain to the desired operating band.

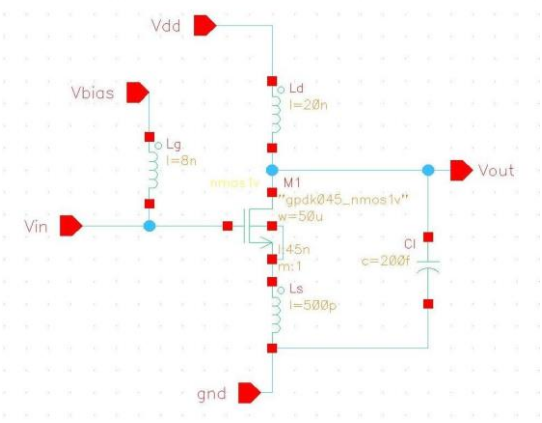

Figure 2. Final LNA design

The input to the LNA is a sine wave with an amplitude of 10mV and a frequency of 2.45GHz. The design was focused on this frequency (the middle of the operating band) to allow for the biggest margin of error in either direction.

The inductors used in this design were required to be real in order to design a realistic LNA so internal resistances had to be accounted for. Reactive components such as inductors are often described with a quality factor Q. It is described as:

$$Q = \frac{\omega\,(Energy\ Stored)}{Avg\ Power\ Dissipated}$$

The desired quality factor for this design is 10, and to obtain the internal resistance the following equation is used:

$$Q = \frac{\omega L}{R}$$

Since the value of Q is already known, this equation can be solved for resistance.

Table 2: LNA inductors and resistances

Inductor	Value	Internal Resistance
L_D	20 nH	30.8 Ω
L_S	500 pH	0.77 Ω
L_G	8 nH	12.3 Ω

The inductor at the drain has the largest value because this ensures a higher series resistance. Since the inductor is acting as a passive load element for the amplifying transistor, the series resistance plays an important role in setting up the necessary voltage drop across the transistor, thereby defining the best operating point. Ensuring a higher drain inductance also allows for the highest voltage drop across the transistor at the specified frequency which will cause the output to have a high swing, directly affecting the gain. Increasing this inductor value too much, however, will decrease the gain of the amplifier.

Due to the previously mentioned downside of the inductor at the source (lowering V_{gs}), L_S was chosen to have a small value so that it accomplishes its purpose without affecting V_{gs} too much. Lastly, the inductor at the gate was used to improve the linearity of the LNA. It also played a pivotal role in choosing the input matching network since it provided additional input impedance to the LNA.

A load capacitor of $200\,fF$ was placed at the output of the LNA to shift the desired gain to the

operating range This capacitor was also shown to improve the overall gain of the amplifier.

III. Gain Before Matching

The gain of any amplifier is a pivotal part of its functionality. It is quite obvious that an amplifier which fails to provide gain is an amplifier no more. It is for this reason that the LNA, being a type of amplifier, needs to provide gain to the signal in order to amplify it for better demodulation.

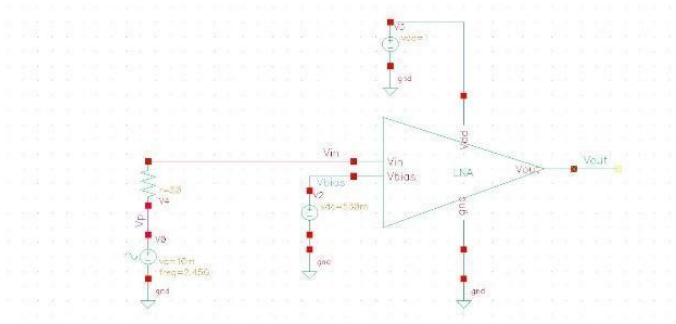

Figure 3. LNA block view before matching

The gain of this LNA was dictated by V_{gs} and the size of the MOSFET being used (50um, 40 fingers). Gain had to be maximized while at the same time taking power consumption into account. Different values of V_{bias} and transistor sizes were used with the focus of obtaining the minimum gain needed to meet specifications so as to avoid using too much power. The gain obtained without matching the input impedance was 15.78dB at 2.45GHz and it met specifications at 2.4GHz and 2.5GHz.

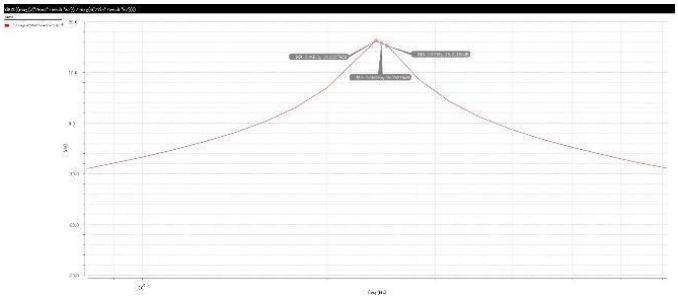

Figure 4. Gain (dB) before matching

Once the circuit is matched, the input voltage at the gate of the LNA will be higher which means the gain will be higher as well.

IV. Impedance Matching

After conducting the S-parameter simulation, we were able to find the S_{11} parameter and the input impedance of the LNA at the operating band frequency

$$S_{11} = 0.929554 \angle 42.8108$$

We found a very useful online tool that allowed us to plug in the values obtained from simulation and determined the components, values, and location to be used for the impedance matching circuit. A few different values for impedance and frequency were used until a satisfactory output was obtained.

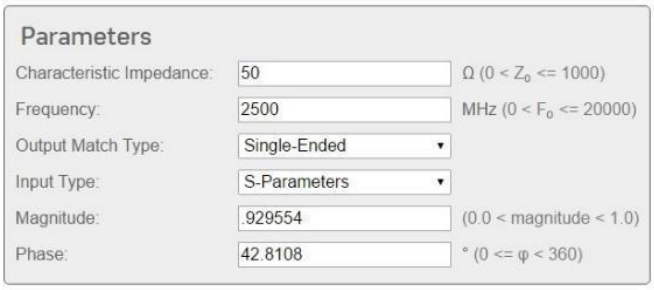

Figure 5. Input values to online tool

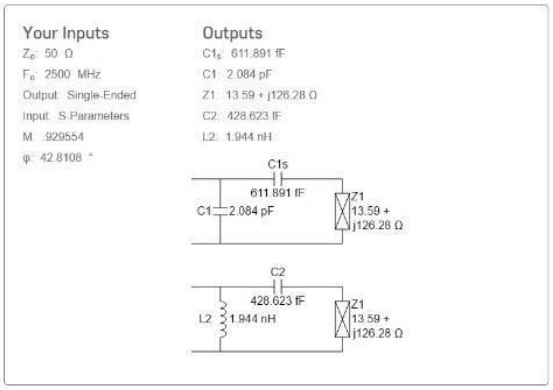

Figure 6. Possible matching networks

After obtaining these values a matching circuit was inserted into the LNA schematic to ensure it worked.

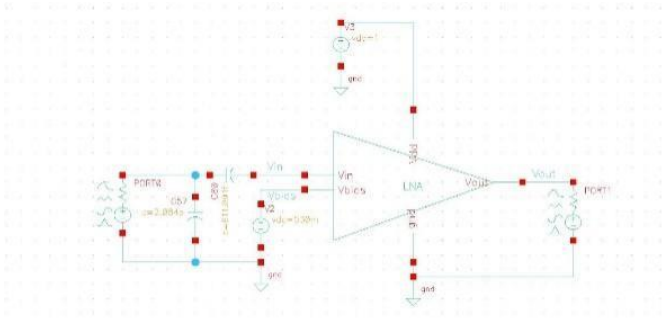

Figure 7. LNA schematic with matching network

Conducting the S-parameter simulation again produces a smith chart which will show if the added components work

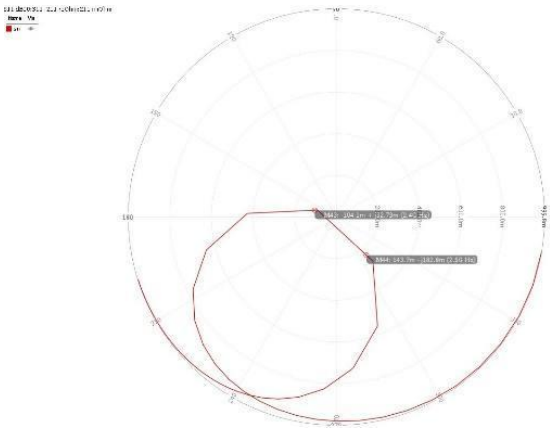

Figure 8. Smith Chart for S11 analysis

We can see that the impedance in the operating range is fairly close to 50 Ω which was the goal. Next a transient analysis was done to compare both input and output waves.

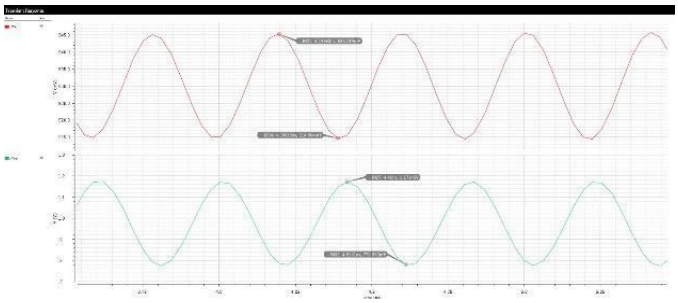

Figure 9. Input and Output Transient analysis graphs

Using the peak values from both waves we determine the gain:

$$A_v = \frac{1.171 - 0.780}{0.545 - 0.515} = 12.82$$

$$20log(12.82) = 22.16\,dB$$

AC analysis was also done as another way to check the new gain.

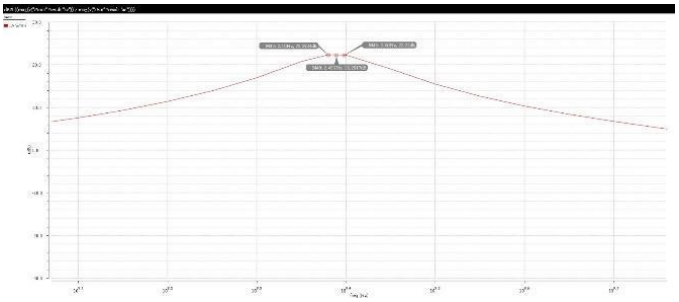

Figure 10. Gain after impedance matching

The gain of the LNA increased by about 6 dB after performing impedance matching. This was due to better noise immunity as a consequence of impedance matching. The maximum obtainable gain was 22.25 dB at 2.45 GHz which is very close the value obtained from transient analysis.

V. Noise Figure

The Noise Figure of the LNA was critical because this metric determined how noise immune the LNA would be. The Noise Figure is commonly represented by the following formula:

$$NF = \frac{SNR_{in}}{SNR_{out}}$$

The Noise Figure, we observed, improves through impedance matching and is also dependent on the amount of transistor gate resistance present. Therefore, the number of fingers in each MOSFET was increased to better distribute this gate resistance across a large number of smaller transistors connected in parallel.

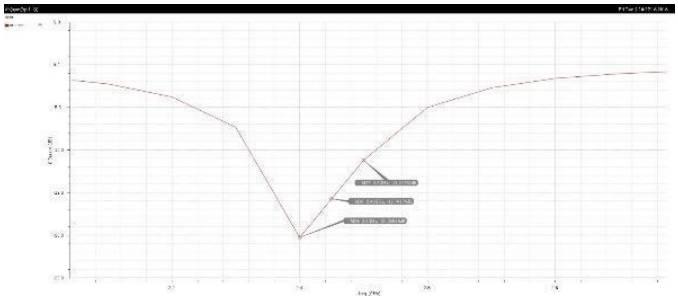

Figure 11. S11 value for operating frequency band

The S11 at 2.45 GHz was around -15.74 dB which is well below the requirement of -10 dB. This improvement of S11, as mentioned before, greatly improved the Noise Figure.

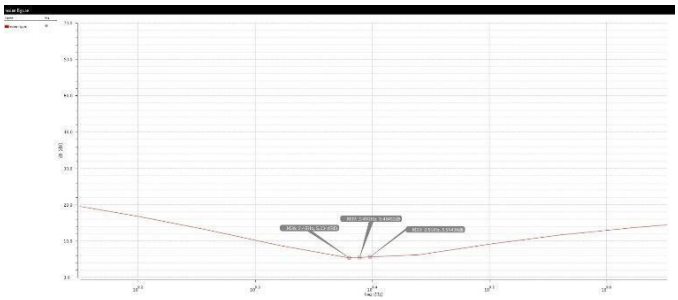

Figure 12. Noise Figure graph

The final Noise Figure that was obtained was 5.46 dB at 2.45 GHz. This figure was slightly higher than the required specification of 3.5 dB or below for the LNA. The main problem that we encountered involved a fine balance between acceptable linearity, reflections and noise immunity. It was observed that whenever the S11 parameter and Noise Figure were fine-tuned to the proper specifications (less than -10 dB and less than 3.5 dB respectively), this decreased linearity about 2 to 3 fold - linearity would drop from around -10 dBm to -20 dBm to -30 dBm.

Therefore, preserving linearity meant sacrificing 1-2 dB of Noise Figure - this was the main reason why the Noise Figure we obtained was 5.46 dB.

VI. Linearity

Linearity usually refers to how well an amplifier is able to amplify only the fundamental tone of a signal and suppress the harmonics or nonlinearities inherent in that signal. Linearity is often represented by either the 1-dB compression point (P1-dB for short) or the 3rd Input Intermodulation Point (IIP3). This design (and this paper) will deal with the 1-dB compression point to determine the linearity of the amplifier. The 1-dB compression point is defined as follows:

$$P_{1-dB} = \sqrt{0.145 \cdot \left|\frac{\alpha_1}{\alpha_3}\right|}$$

In the above equation, $A_{1\text{-}dB}$ is the amplitude of the input signal at the 1-dB compression point and α_1 and α_3 are the gains of the fundamental and third harmonic respectively. The power of the input $A_{1\text{-}dB}$, as shown below, is -3.5 dBm.

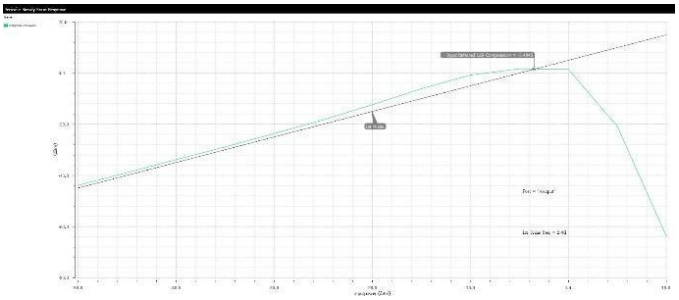

Figure 13. P-1dB graph

VII. DC Power Consumption

The DC power consumption for our LNA was minimal. In order to find out how much the entire design was consuming, we did a DC Analysis in Cadence and found that the total power drawn from the circuit is 0.81 mW. This is displayed in the figure below.

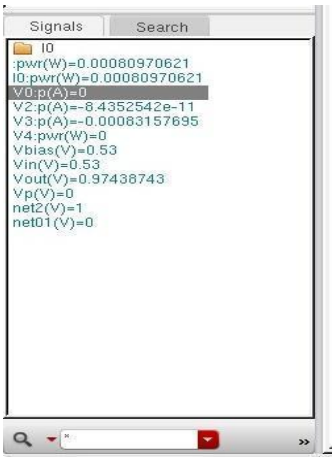

Figure 14. Power consumption

The specification for DC power consumption was 2 mW and clearly our LNA draws a much lower power value than this.

VIII. Final Calculations

The specifications used for the design of the LNA are - Gain, S11, Noise Figure, P1-dB, and DC Power Consumption. S11, although seen as a critical specification, is not included in the FOM formula used to evaluate the LNA.

Table 3. Final Simulated results for FoM

Gain	22.25 dB
S11	-15.74 dB
Noise Figure	5.46 dB
P1-dB	-3.5 dBm
DC Power Cons.	0.81 mW

$$FoM = \frac{A_v \, f \, P_{1-dB}}{(F - 1) \, P_{DC}}$$

$$FoM = \frac{12.82 \cdot 2.45\,GHz \cdot 0.447\,mW}{(3.516 - 1) \cdot 0.81\,mW} = 6.889\,GHz$$

IX. Conclusions

The Low Noise Amplifier (LNA) is a critical part of the Receiver subsystem of any RFIC chip. This paper took a detailed look at how to design an LNA and optimize certain key criteria for proper functionality of an LNA, namely: Gain, Reflection, Noise Immunity, Linearity and DC Power Consumption. The Gain of the LNA increased when the LNA was well matched to the 50 Ohm antenna while, at the same time, the reflections on the input were decreased. This improved noise immunity, represented by the Noise Figure, as wasted input power in the form of reflections was minimized. Linearity, represented by the 1-dB compression point (P1-dB) - another very important criterion - determined how well the LNA amplified only the fundamental tone of the input signal and suppressed non-linearities (2nd, 3rd harmonic etc). There were clear tradeoffs between the Noise Figure and the 1-dB compression point and so the LNA design was fine-tuned to get the best possible values for both specifications. The final FoM result was 6.889 GHz.

References

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