

EE220 RFIC DESIGN I DESIGN PROJECT

Design Project Title: High FoM Bluetooth LNA in 45nm

Team Size: One or two students per design project team

CAD tool: Use schematic composer, Spectre simulator in Cadence CAD tool for this assignment

Scope of the project:

The objective of this design project is to optimize the figure-of-merit (FoM) of a Bluetooth low-noise-amplifier (LNA). The FoM considers gain, frequency, P_{1dB} , noise figure, and DC power consumption. Its definition is given in equation (28) of the following paper:

$$FoM = \frac{Gain \cdot f \cdot P_{-1dB}}{(F - 1) \cdot P_{dc}} \quad (28)$$

S. Asgaran, M. Jamal Deen and C.H. Chen, "Design of the Input Matching Network of RF CMOS LNAs for Low-Power Operation," IEEE Transactions on Circuits and Systems—I, Vol. 54, No. 3, March 2007.

The LNA topology is given in Figure 1 with $V_{dd} = 1.0V$ and $R_p = 50\Omega$. All components should be selected from 45nm CMOS gpdk, with the exception of L_g which can be selected from analogLib.

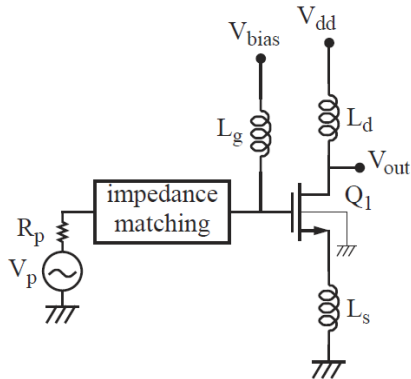


Figure 1: Common Source LNA topology

Design Specification:

While optimizing the FoM of the LNA design, the following specifications need to be met over the entire Bluetooth operating frequency range: 2.4GHz to 2.5GHz. (Consider room temp $T=25^\circ C$ only)

$ S_{11} $	$< -10dB$
Voltage Gain	$>15dB$
Noise Figure	$<3.5dB$
DC Power Consumption P_{dc}	$<2mW$
P_{1dB}	$>-10dBm$

Table 1: Bluetooth LNA Specification

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You are required to optimize the components of the matching network, L_s , L_d , biasing voltage, and the transistor size, in order to meet to the key specifications.

Report Requirements:

The final report should be 4-8 pages in overall and in two-column IEEE paper format. Describe the major design considerations and tradeoffs. Present all simulation results for parameters in Table1.

Submit your final report (in Microsoft Word file) electronically through SJSU email by Dec. 16, 2016.