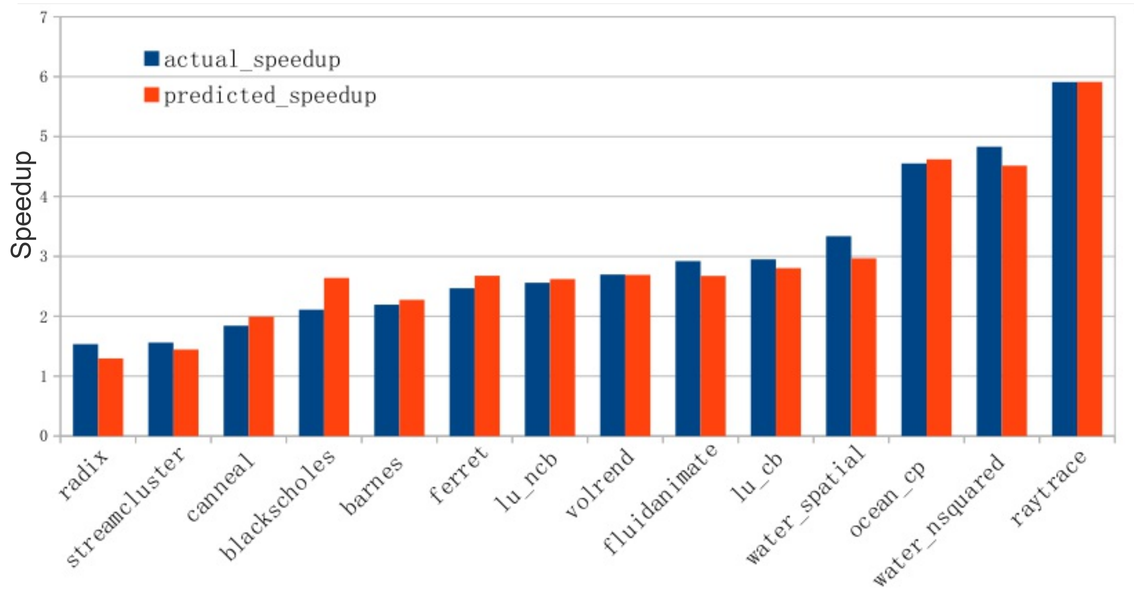
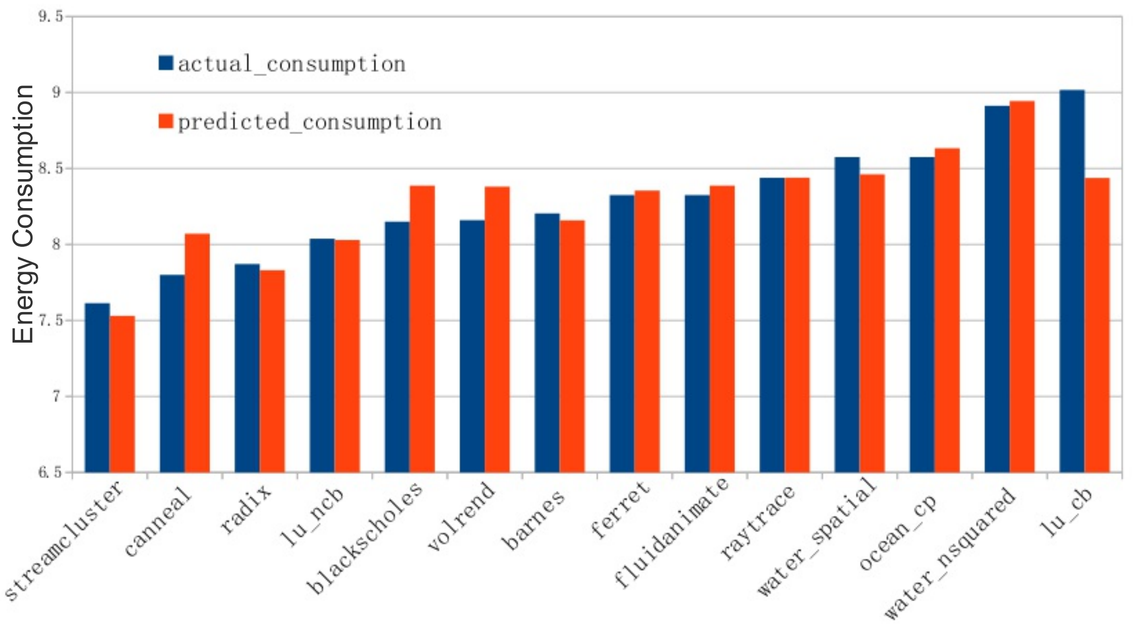
	L1D_CACHE_REFILL	SW_INCR	L2_CACHE	BR_IMMED_RETRIED	.....	Speedup	Energy
radix	247752621	0	590072810	1566821217	.....	1.534639	7.8714
ferret	48055269	0	196999342	2447940818	.....	2.468487	8.325
.....	.....	0	.....	.....	.....	.....	.....

(a) Abstract ARMv8 PMUs Selection Process

Index	Name	Description [1]
A:	L1D_CACHE_REFILL	# L1 data cache refill
B:	L1D_TLB_REFILL	# Attributable L1 data TLB refill
C:	L1D_CACHE_WB	# Attributable L1 data cache write-back
D:	L2D_CACHE	# L2 data cache access
E:	L2D_CACHE_WB	# Attributable L2 data cache write-back
F:	BUS_ACCESS	# Bus access
G:	Cycle	# Processor clock cycle
Linear predictive speedup model		
2.6185+((-7.8618*A)+(-25.7769*B)+ -34.2781*C)+(11.2167*D)+(44.3879*E)+(-10.1942*F))/G		
Linear predictive energy model		
2.3116+((-759.5873*A)+(13.9528*B)+ (5.9552*C)+(0.5631*D)+(760.8123*E)+(-14.1615*F))/G		

(b) PMU-based Performance and Energy Models





(c) Performance and Energy Models Validation