Topic: Voltage Multiplier

➢ Definition:

- The voltage multiplier is an electronic circuit that delivers the output voltage whose amplitude (peak value) is two, three, or more times greater than the amplitude (peak value) of the input voltage.
- The voltage multiplier is an electronic circuit that converts the low AC voltage into high DC voltage

or

- The voltage multiplier is an AC-to-DC converter, made up of diodes and capacitors that produce a high voltage DC output from a low voltage AC input.

➢ Types of voltage multipliers

Voltage multipliers are classified into four types:

- Half-wave voltage doubler
- Full-wave voltage doubler
- Voltage tripler
- Voltage quadrupler

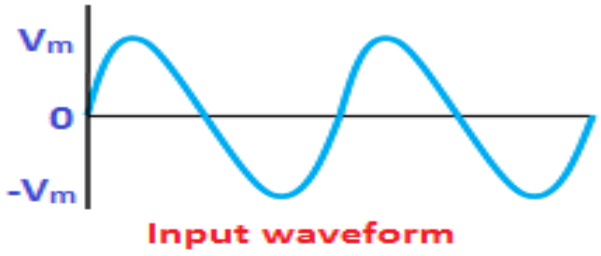
➢ Half-wave voltage doubler

As its name suggests, a half-wave voltage doubler is a voltage multiplier circuit whose output voltage amplitude is twice that of the input voltage amplitude. A half-wave voltage doubler drives the voltage to the output during either positive or negative half cycle. The half-wave voltage doubler circuit consists of two diodes, two capacitors, and AC input voltage source.

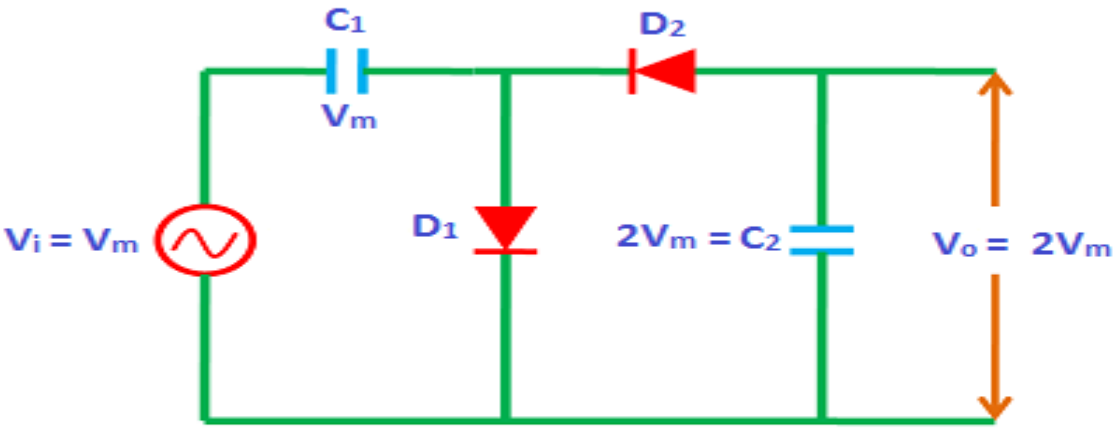
- **During positive half cycle:**

The circuit diagram of the half-wave voltage doubler is shown in the below figure. **During the positive half cycle, diode D_1 is forward biased.** So it allows electric current through it. This current will flows to the capacitor C_1 and charges it to the peak value of input voltage I.e. V_m.

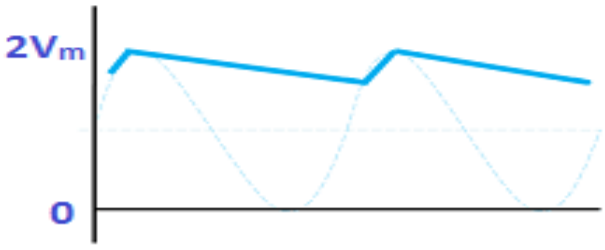
However, current does not flow to the capacitor C_2 because the diode **D_2 is reverse biased**. So the diode D_2 blocks the electric current flowing towards the capacitor C_2. Therefore, during the positive half cycle, capacitor C_1 is charged whereas capacitor C_2 is uncharged.



Input waveform



Half-wave voltage doubler



Output waveform

During negative half cycle:

- During the negative half cycle, diode D_1 is reverse biased. So the diode D_1 will not allow electric current through it. Therefore, during the negative half cycle, the capacitor C_1 will not be charged. However, the charge (V_m) stored in the capacitor C_1 is discharged (released).
- On the other hand, the diode D_2 is forward biased during the negative half cycle. So the diode D_2 allows electric current through it. This current will flows to the capacitor C_2 and charges it. The capacitor C_2 charges to a value $2V_m$ because the input voltage V_m and capacitor C_1 voltage V_m is added to the capacitor C_2. Hence, during the negative half cycle, the capacitor C_2 is charged by both input supply voltage V_m and capacitor C_1 voltage V_m. Therefore, the capacitor C_2 is charged to $2V_m$.
- If a load is connected to the circuit at the output side, the charge ($2V_m$) stored in the capacitor C_2 is discharged and flows to the output.
- During the next positive half cycle, diode D_1 is forward biased and diode D_2 is reverse biased. So the capacitor C_1 charges to V_m whereas capacitor C_2 will not be charged. However, the charge ($2V_m$) stored in the capacitor C_2 will be discharged and flows to the output load. Thus, the half-wave voltage doubler drives a voltage of $2V_m$ to the output load.

The capacitor C_2 gets charged again in the next half cycle.

The voltage ($2V_m$) obtained at the output side is twice that of the input voltage (V_m).

The capacitors C_1 and C_2 in half wave-voltage doubler charges in alternate half cycles.

The output waveform of the half-wave voltage doubler is almost similar to the half wave rectifier with filter. The only difference is the output voltage amplitude of the half-wave voltage doubler is twice that of the

input voltage amplitude but in half wave rectifier with filter, the output voltage amplitude is same as the input voltage amplitude.

The half-wave voltage doubler supplies the voltage to the output load in one cycle (either positive or negative half cycle). In our case, the half-wave voltage doubler supplies the voltage to the output load during positive half cycles. Therefore, the output signal regulation of the half-wave voltage doubler is poor.

- **<u>Advantages of half-wave voltage doubler</u>**
- High voltages are produced from the low input voltage source without using the expensive high voltage transformers.
- Disadvantages of half-wave voltage doubler
- Large ripples (unwanted fluctuations) are present in the output signal.

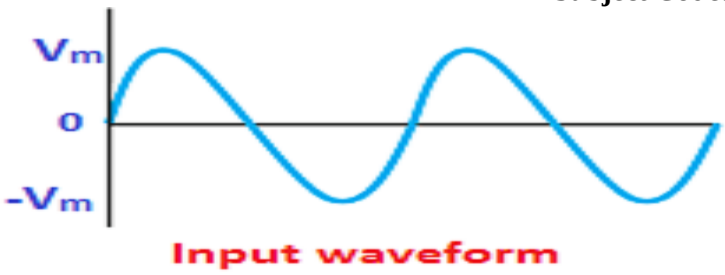
• Full-wave voltage doubler

The full-wave voltage doubler consists of two diodes, two capacitors, and input AC voltage source.

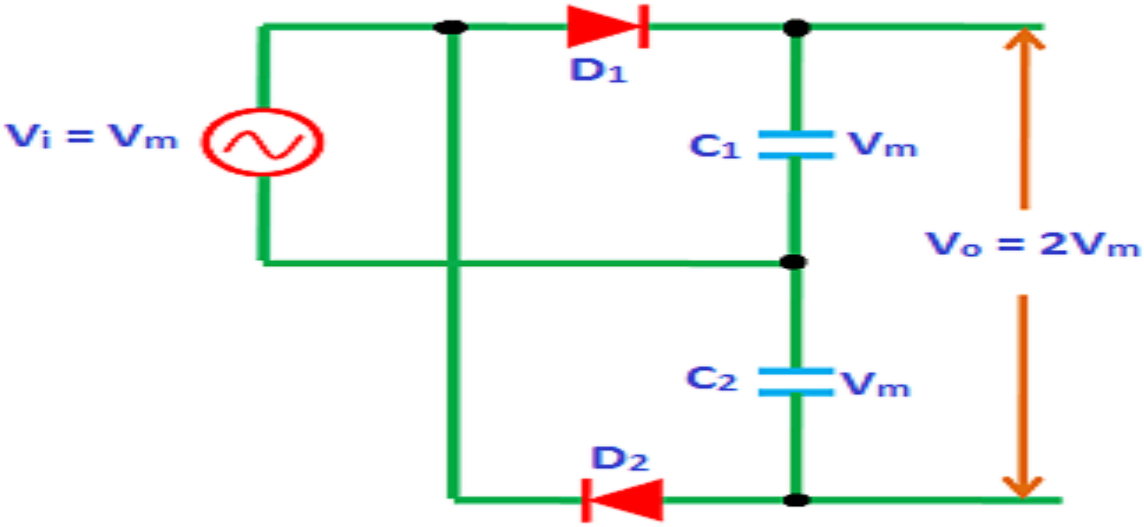
- **During positive half cycle:**

During the positive half cycle of the input AC signal, diode D_1 is forward biased. So the diode D_1 allows electric current through it. This current will flows to the capacitor C_1 and charges it to the peak value of input voltage I.e V_m.

On the other hand, diode D_2 is reverse biased during the positive half cycle. So the diode D_2 does not allow electric current through it. Therefore, the capacitor C_2 is uncharged.



Input waveform



Full-wave voltage doubler

Output waveform

During negative half cycle:

During the negative half cycle of the input AC signal, the diode D_2 is forward biased. So the diode D_2 allows electric current through it. This current will flows to the capacitor C_2 and charges it to the peak value of the input voltage I.e. V_m.

- On the other hand, diode D_1 is reverse biased during the negative half cycle. So the diode D_1 does not allow electric current through it.
- Thus, the capacitor C_1 and capacitor C_2 are charged during alternate half cycles.
- The output voltage is taken across the two series connected capacitors C_1 and C_2.
- If no load is connected, the output voltage is equal to the sum of capacitor C_1 voltage and capacitor C_2 voltage I.e. $C_1 + C_2 = V_m + V_m = 2V_m$. When a load is connected to the output terminals, the output voltage V_o will be somewhat less than $2V_m$.
- The circuit is called full-wave voltage doubler because one of the output capacitors is being charged during each half cycle of the input voltage.