

Unit-2

Bipolar Junction Transistor & it's Biasing

# Basic Electronics

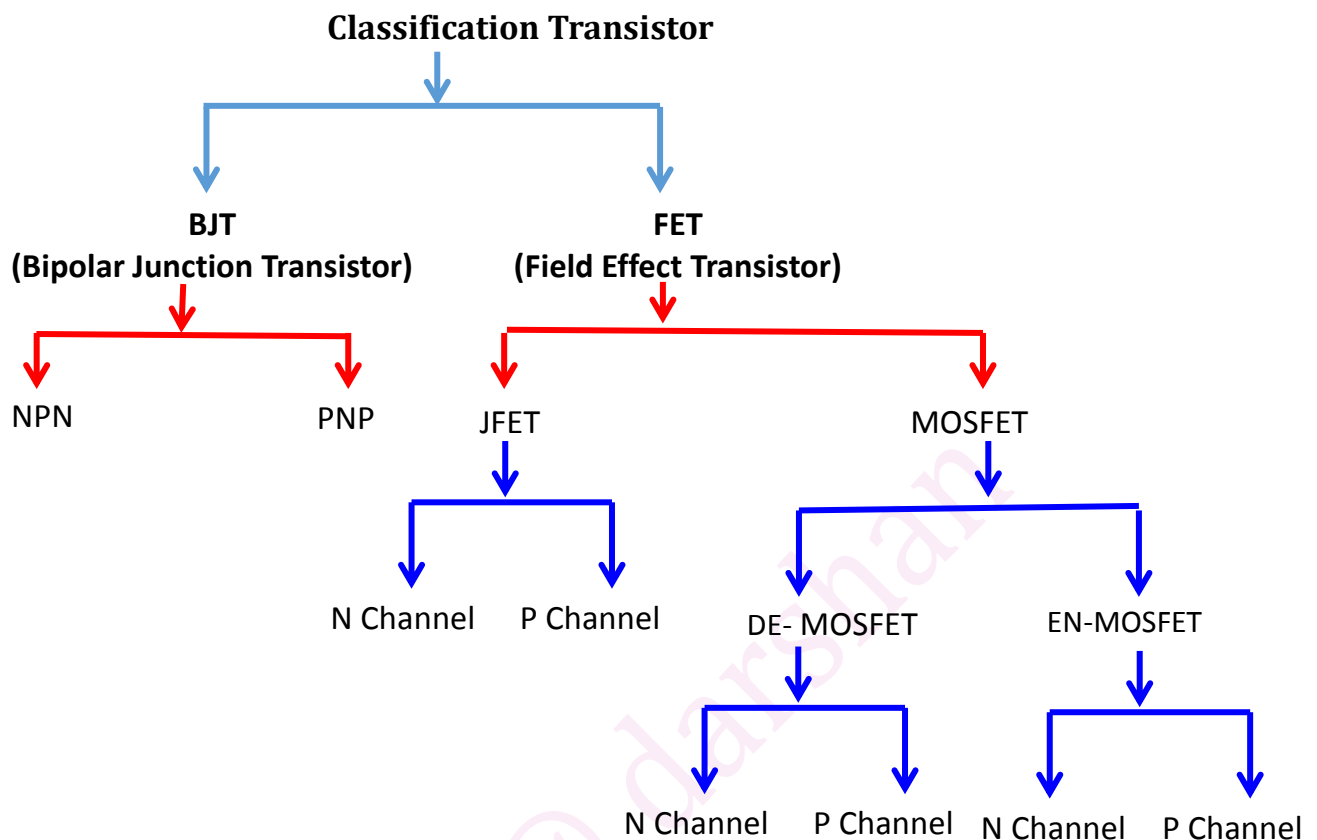
(3110016)

2<sup>nd</sup> Semester

Computer/Electrical Engineering

## 2.1 Classification of Transistor

Transistor can be classified as follow in different ways.



## 2.2 Construction of Bipolar Junction Transistor (BJT)

BJT is introduced in 1948 by Shockley, BJT is an electronic component mainly used for **switching** and **amplification** purpose.

BJT is called **bipolar** because the main flow of electrons through them takes place in two types of semiconductor material P type and N type, as the main current goes from emitter to collector (or vice versa). In other words, two types of charge carriers *electrons* and *holes* comprise this main current through the transistor so it is called bipolar.

Transistor implies *transfer of resistance* because it transfers current from low resistance input path to high resistance output path.

BJT is called a **current controlled device** where small current at the base side is used to control the large current at other terminals.

BJT comes in two types called

- NPN transistor and
- PNP transistor

This transistor comes with two PN junctions.

- PN junction exists between emitter and base is called **emitter-base junction**
- PN junction exists between collector and base is called **collector-base junction**.

It is composed of three terminals called Emitter (E), Base (B) and Collector(C)

All three terminals of the BJT are different in terms of their doping concentrations.

### Emitter:

- It is heavily doped
- Moderate in size
- It emits/injects charge carriers into base for conduction of current

### Base:

- It is lightly doped
- Small/Thin in size
- It passes most of charge carrier to collector. It provides channel/path to charge carrier between emitter & collector

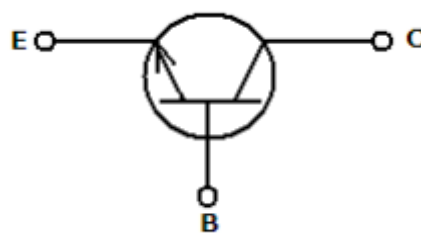
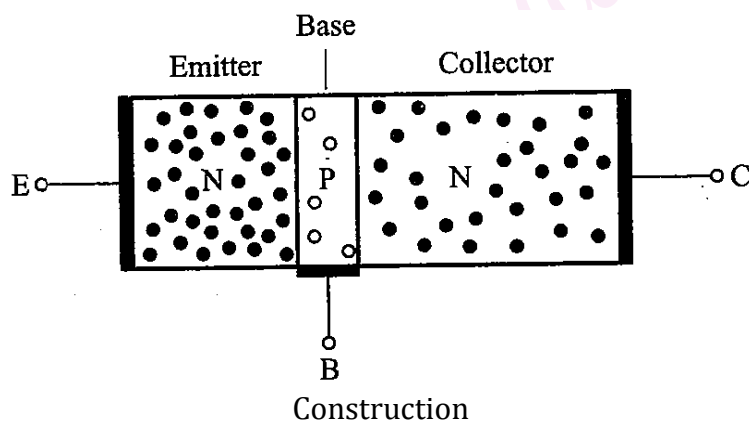
### Collector:

- It is moderately doped
- Large in size
- It collects charge carriers from base which has been emitted by emitter.

### Transistor Construction:

#### (1)NPN Transistor:

When single p-type semiconductor layer is sandwiched between two n-type semiconductor layers, an NPN transistor is formed.

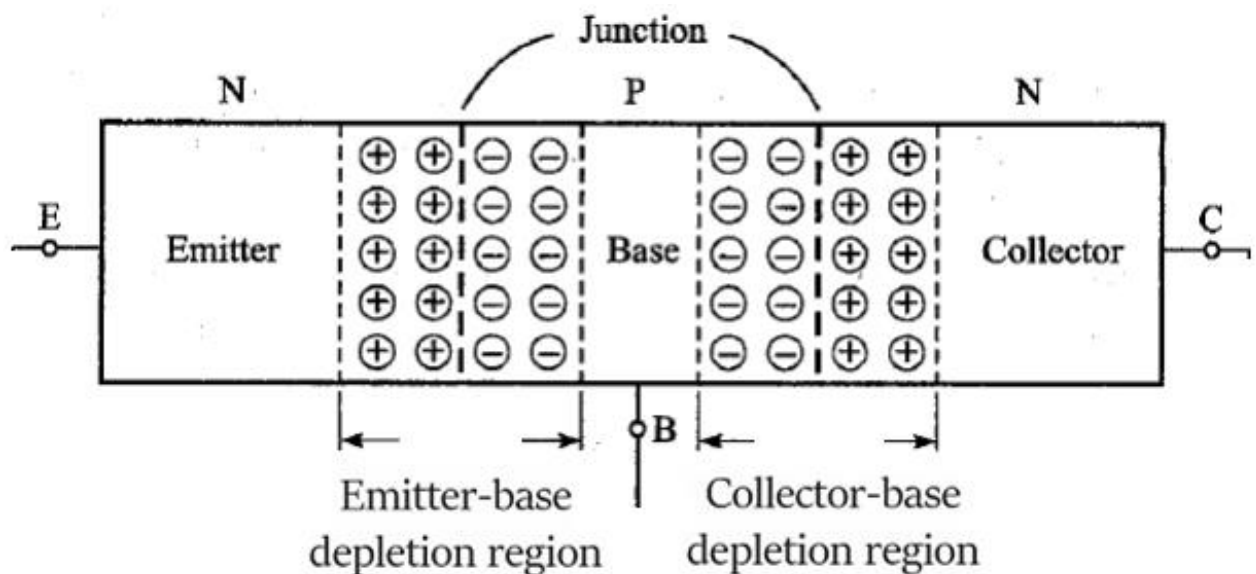


Symbol of NPN

#### Unbiased NPN transistor:

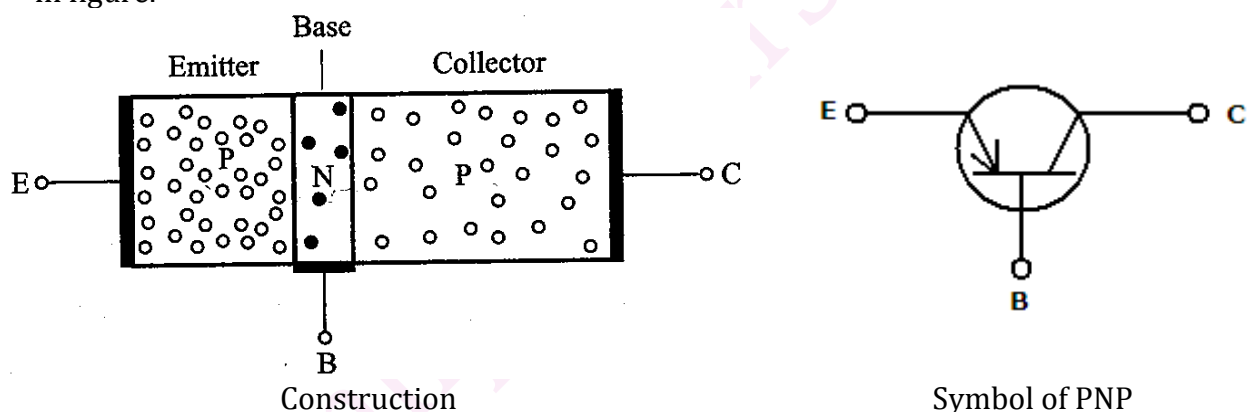
When no voltage is applied to a transistor, it is said to be an unbiased transistor. At the left side n-region (emitter) and right side n-region (collector), free electrons are the majority carriers and holes are the minority carriers whereas in p-region (base), holes are the majority carriers and free electrons are the minority carriers.

The free electrons in the n regions will spread in all directions. Some of the free electrons from the n region will diffuse across the junction and recombine with the holes in the p region. The result is two depletion layers, as shown in Figure.



### (2) PNP Transistor:

When single n-type semiconductor layer is sandwiched between two p-type semiconductor layers, an PNP transistor is formed. Construction and symbol of PNP transistor is as shown in figure.

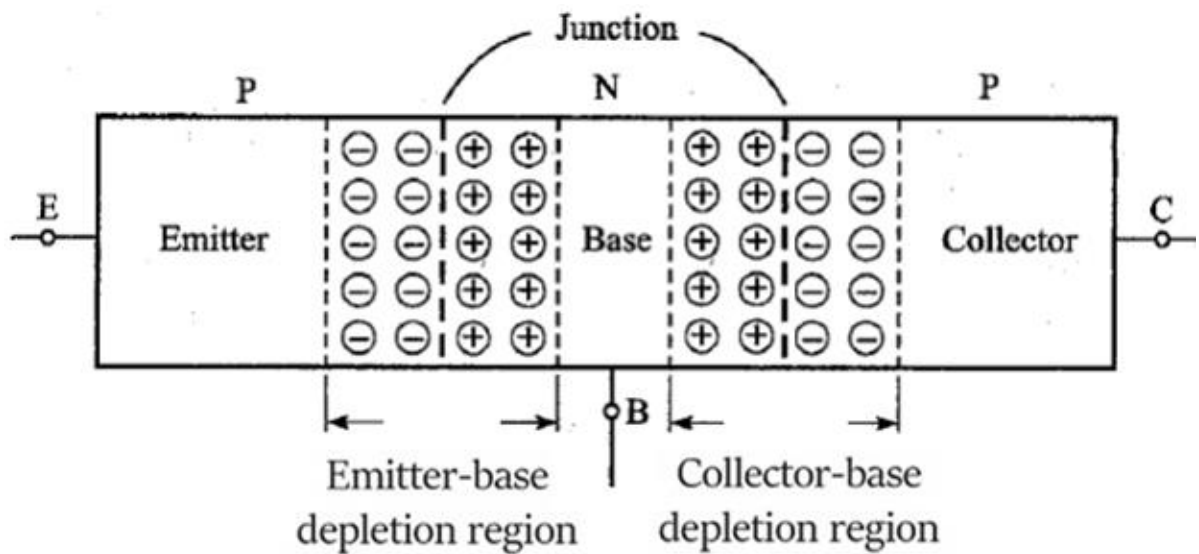


### Unbiased PNP transistor:

When no voltage is applied to a pnp transistor, it is said to be an unbiased pnp transistor. At the left side p-region (emitter) and right side p-region (collector), holes are the majority carriers and free electrons are the minority carriers whereas in n-region (base), free electrons are the majority carriers and holes are the minority carriers.

Therefore, the holes at the left side p-region (emitter) and right side p-region (collector) experience a repulsive force from each other. As a result, the holes at the left side and right side p-regions (emitter and collector) will move into the n-region (base).

During this process, the holes meet the free electrons in the n-region (base) and recombines with them. As a result, depletion region (positive and negative ions) is formed at the emitter to base junction and base to collector junction.



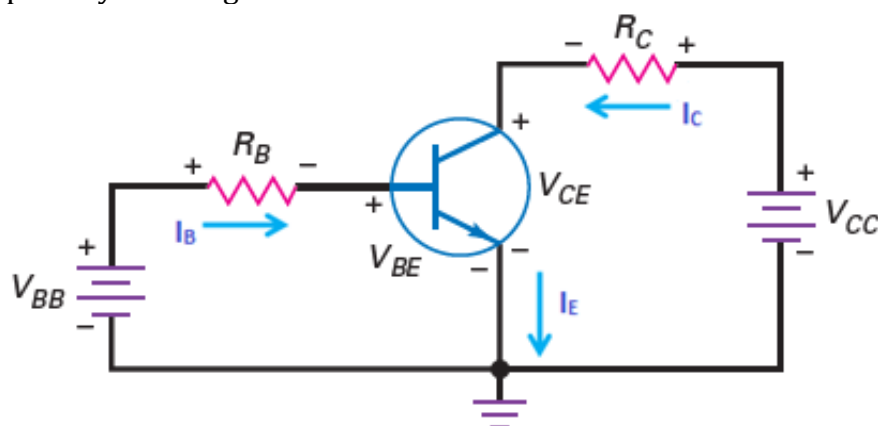
### 2.3 Operating region of Bipolar Junction Transistor (BJT)

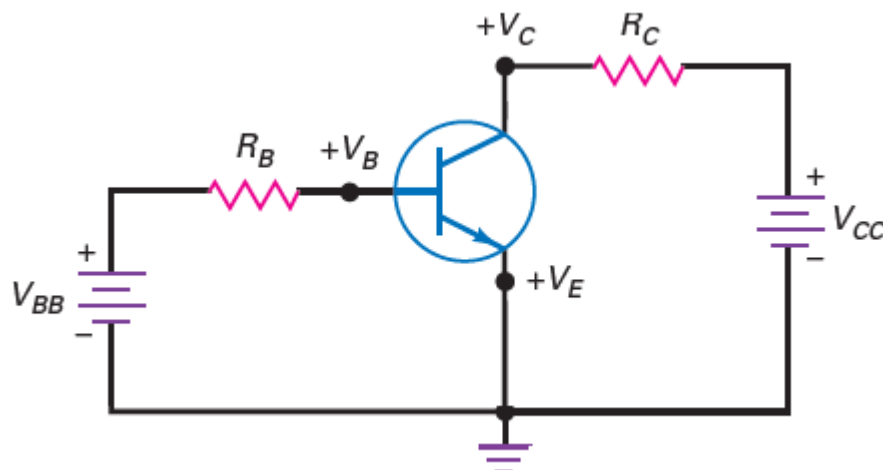
A transistor has two junctions, emitter-base junction and a collection-base junction. There are four possible ways of biasing these two junctions.

Condition		Emitter Base Junction (E-B Junction)	Collector base Junction (C-B Junction)	Operating Region
1	FR	<b>Forward Biased</b>	Reverse Biased	<b>Active</b>
2	FF	<b>Forward Biased</b>	<b>Forward Biased</b>	Saturation
3	RR	Reverse Biased	Reverse Biased	Cutoff
4	RF	Reverse Biased	<b>Forward Biased</b>	Inverted(Not Used)

### 2.4 Various Voltages and Currents in Bipolar Junction Transistor (BJT)

In transistor notation used for various voltages and currents as well as direction of various currents and polarity of voltages are as follows.



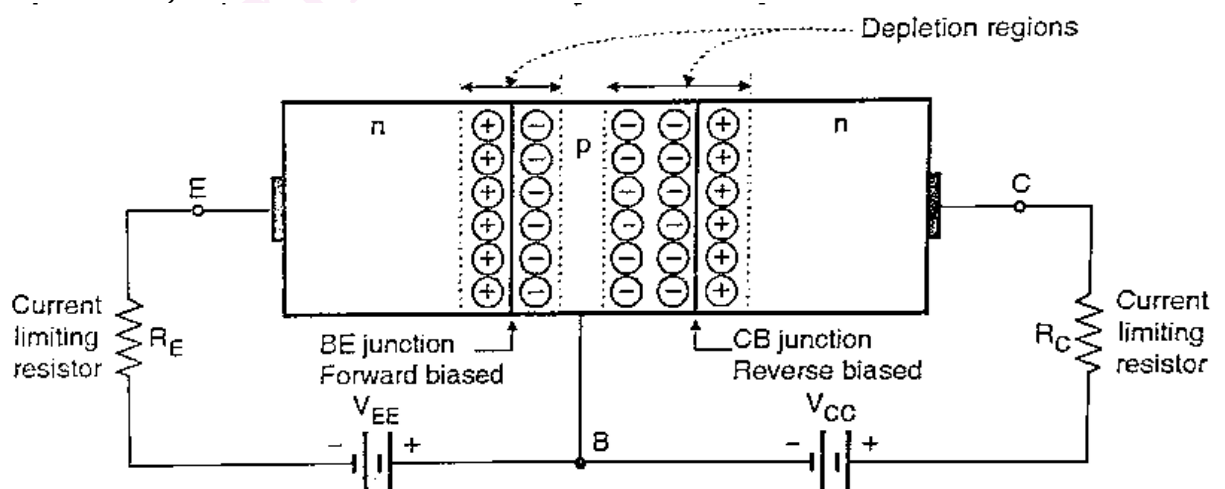


$V_{CC}$	Collector Battery Voltage	$I_C$	Collector Current
$V_{EE}$	Emitter Battery Voltage	$I_E$	Emitter Current
$V_{BB}$	Base Battery Voltage	$I_B$	Base Current
$V_C$	Collector Terminal Voltage	$V_{BE}$	Voltage across Emitter-Base Jn.
$V_E$	Emitter Terminal Voltage	$V_{CB}$	Voltage across Collector-Base Jn.
$V_B$	Base Terminal Voltage	$V_{CE}$	Voltage across Collector-Emitter Jn.

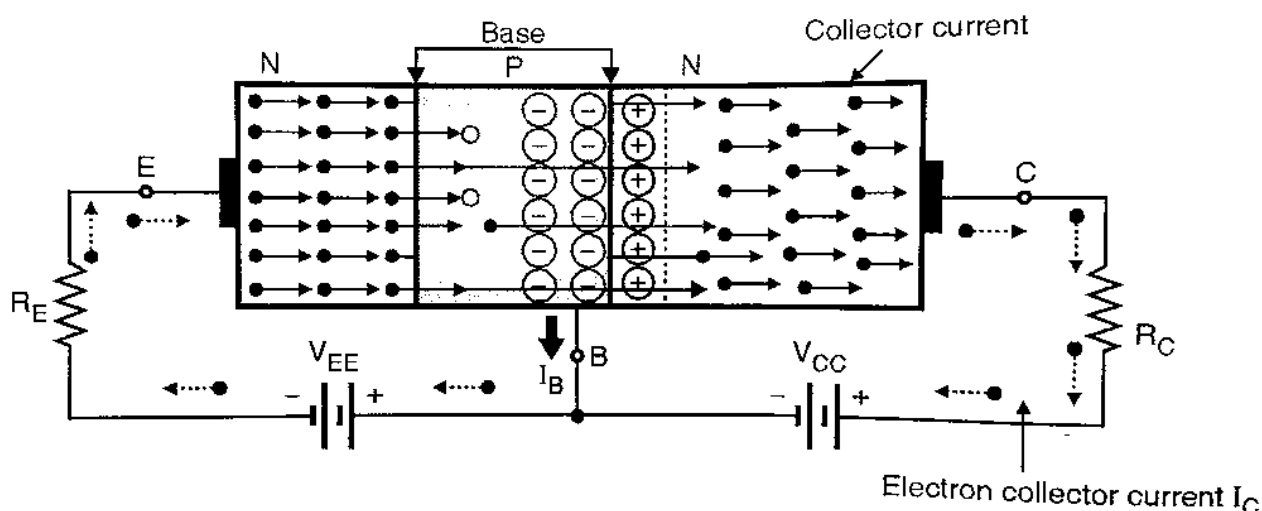
$$I_E = I_C + I_B$$

## 2.5 Working of Bipolar Junction Transistor (BJT) in Active region.

As shown in figure npn transistor is biased in Active region. **Emitter-Base junction is forward biased and collector base junction is reverse biased.** The left source  $V_{EE}$  forward-biases the emitter base junction and the right source  $V_{CC}$  reverse-biases the collector base junction.



The heavily doped emitter, emit or inject its free electrons into the base. The lightly doped base passes emitter-injected electrons on to the collector. The collector is so named because it collects or gathers most of the electrons from the base.



If  $V_{EE}$  is greater than the emitter-base barrier potential then emitter electrons will enter the base region, as shown in Figure. Theoretically, these free electrons can flow in either of two directions. Either they can flow through base and towards positive terminal of battery  $V_{EE}$ . Otherwise, the free electrons can flow into the collector.

But as the base is lightly doped and very thin, free electrons entered into base gets very less amount of time for recombination in the base region. For this reason almost all the emitter-injected electrons pass through the base to the collector. Only a few free electrons will recombine with holes in the lightly doped base and will flow through the base and toward the positive side of the  $V_{EE}$  supply.

Almost all the free electrons go into the collector, as shown in Figure. Once they are in the collector, they feel the attraction of the  $V_{CC}$  source voltage. Because of this, the free electrons flow through the collector and through  $R_C$  until they reach the positive terminal of the collector supply voltage.

Thus  $V_{EE}$  forward-biases the emitter diode, forcing the free electrons in emitter to enter the base. The thin and lightly doped base gives almost all these electrons enough time to diffuse into the collector. These electrons flow through the collector, through  $R_C$ , and into the positive terminal of the  $V_{CC}$  voltage source. Even though CB junction is reverse biased electron from emitter could able to reach to collector.

### **Emitter efficiency (emitter injection ratio):**

It is defined as the ration of charge carriers injected by emitter into the base to total emitter current. It is denoted by symbol  $\gamma$  (gamma).

$$\gamma = \frac{\text{charge carrier injected by emitter at EB junction}}{\text{Total emitter curremy}} = \frac{I_{nE}}{I_{nE} + I_{pE}} = \frac{I_{nE}}{I_E}$$

For NPN transistor total emitter current is due to emitted electrons  $I_{nE}$  as well as due to minority charge carrier hole  $I_{pE}$ . Current due to minority charge carriers is very small. Typical value of  $\gamma$  is 0.995

**Base Transportation factor  $\beta^*$ :**

It is defined as the ration of charge carriers reaching/arriving at collector to the number of emitted charge carriers. It is denoted by symbol  $\beta^*$  or  $\beta'$  (Beta).

$$\beta^* = \frac{\text{injected charge carriers reaching/arriving at collector}}{\text{charge carriers emitted by emitter}} = \frac{I_{nC}}{I_{nE}}$$

For NPN transistor charge carriers (electrons) emitted by emitter is  $I_{nE}$  and charge carriers (electrons) reaching at collector is  $I_{nC}$ . Typical value of  $\beta^*$  is 0.995.

**Large signal current gain  $\alpha^*$ :**

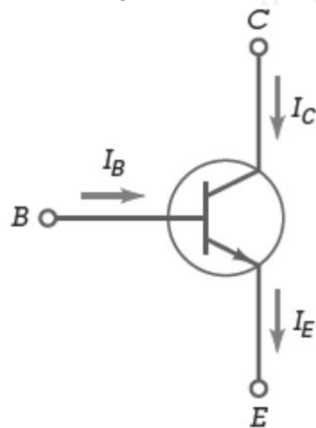
It is defined as the ration of collector current increment to total emitter current. It is denoted by symbol  $\alpha^*$  or  $\alpha'$  (Alpha).

$$\alpha^* = \frac{\text{collector current increment}}{\text{total emitter current}} = \frac{I_C - I_{CBO}}{I_{nE} + I_{pE}} = \frac{I_{nC}}{I_E}$$

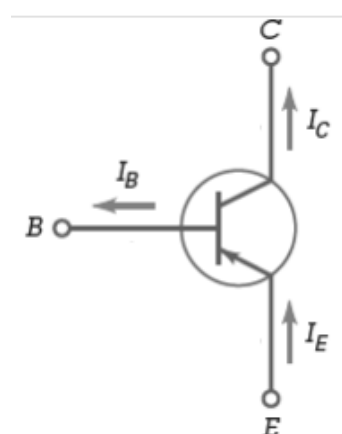
For NPN transistor total emitter current is due to emitted electrons  $I_{nE}$  as well as due to minority charge carrier hole  $I_{pE}$ . Increment in collector current is  $I_C - I_{CBO}$ , where  $I_{CBO}$  is collector to base leakage current when emitter is open (due to minority charge carrier in collector). Typical value of  $\alpha^*$  is 0.9 to 0.995.

**2.6 Different Current components in Transistor and their relationship:**

There are three different currents in a transistor: emitter current  $I_E$ , base current  $I_B$ , and collector current  $I_C$ .



Direction of currents in NPN transistor



Direction of currents in PNP transistor

Because the emitter is the source of the electrons, it has the largest current. Since most of the emitter electrons flow to the collector, the collector current is almost as large as the emitter current. The base current is very small by comparison, often less than 1 percent of the collector current.



**Relation of Currents:**

As per Kirchhoff's current law. It says that the sum of all currents into a point or junction equals the sum of all currents out of the point or junction. When applied to a transistor, Kirchhoff's current law gives us this important relationship:

$$I_E = I_B + I_C$$

This says that the emitter current is the sum of the collector current and the base current. Since the base current is so small, the collector current approximately equals the emitter current.

$$I_C \approx I_E$$

and the base current is much smaller than the collector current:

$$I_B \ll I_C$$

**Current Gain in transistor and it's relation:****Current Gain Alpha ( $\alpha_{dc}$ ) :**

The current gain alpha dc ( $\alpha_{dc}$ ) is defined as the ratio of dc collector current to dc emitter current.

$$\alpha_{dc} = \frac{I_C}{I_E}$$

Since the collector current almost equals the emitter current, the dc alpha is slightly less than 1. For instance, in a low-power transistor, the dc alpha is typically greater than 0.99. Even in a high-power transistor, the dc alpha is typically greater than 0.95.

**Current Gain Beta ( $\beta_{dc}$ ) :**

The current gain Beta dc ( $\beta_{dc}$ ) is defined as the ratio of dc collector current to dc base current.

$$\beta_{dc} = \frac{I_C}{I_B}$$

The dc beta is also known as the current gain because a small base current controls a much larger collector current. The current gain is a major advantage of a transistor and has led to all kinds of applications.

For low-power transistors (under 1 W), the current gain is typically 100 to 300. High-power transistors (over 1 W) usually have current gains of 20 to 100.

**Relation between current gain  $\alpha_{dc}$  and  $\beta_{dc}$** 

The emitter current equation is

$$I_E = I_B + I_C \quad \text{---- (1)}$$

Dividing equation (1) by  $I_C$

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1 \quad \text{---- (2)}$$

$$\frac{1}{\alpha_{dc}} = \frac{1 + \beta_{dc}}{\beta_{dc}}$$

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} \quad \text{---- (3)}$$

Equation (3) indicates  $\alpha_{dc}$  in terms of  $\beta_{dc}$

Rearranging equation (2) again

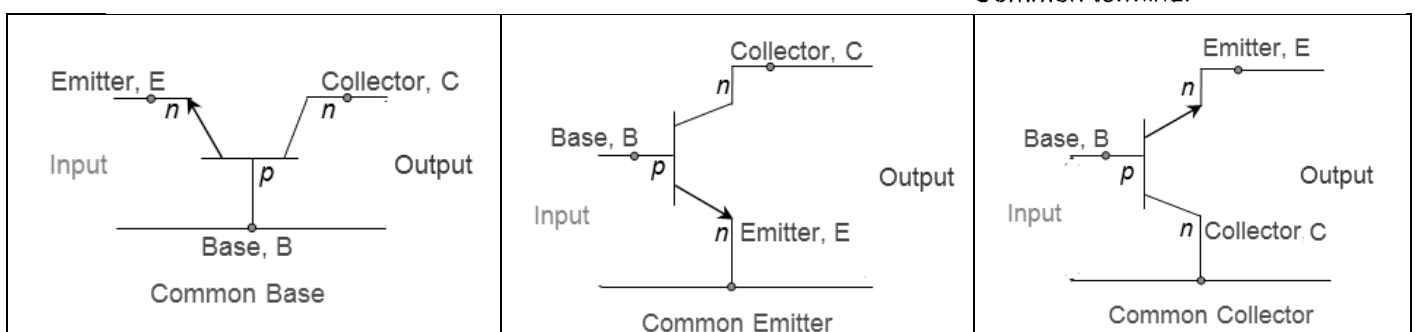
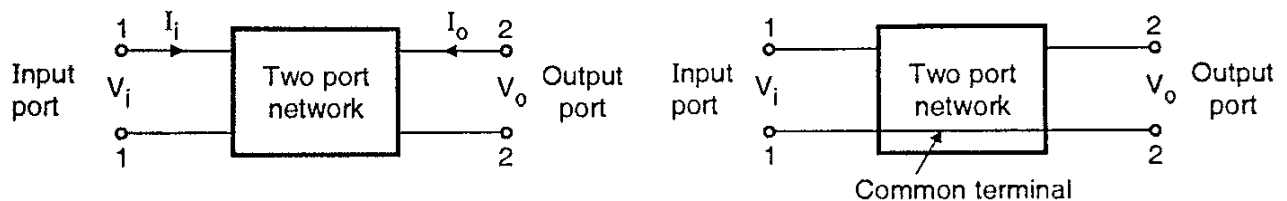
$$\frac{1}{\beta_{dc}} = \frac{1}{\alpha_{dc}} - 1$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} \quad \text{---- (4)}$$

Equation (4) indicates  $\beta_{dc}$  in terms of  $\alpha_{dc}$

## 2.7 Types of Transistor Configurations

Transistor has three terminals namely emitter (E), base (B), and collector (C). But to connect a transistor in the circuit, we need four terminals, two terminals for input and other two terminals for output. If one of the three terminals is used as common to both input and output then transistor can be considered as two port network.



When a transistor is to be connected in a circuit, one terminal is used as the input terminal, the other terminal is used as the output terminal and the third terminal is common to the input and output. That means here input is applied between the input terminal and common terminal, and the corresponding output is taken between the output terminal and common terminal.

Depending upon the terminal which is used as a common terminal to the input and output terminals, the transistor can be connected in the following three configurations. They are:

- (i) Common base (CB) configuration
- (ii) Common emitter (CE) configuration
- (iii) Common collector (CC) configuration

In every configuration, the base-emitter junction is always forward biased and the collector-base junction is always reverse biased to operate the transistor as a current amplifier.

### *Common base (CB) configuration*

In common base configuration, emitter is the input terminal, collector is the output terminal, and base is the common terminal. The base terminal is grounded in the common base configuration. So the common base configuration is also known as grounded base configuration.

### *Common emitter (CE) configuration*

In common emitter configuration, base is the input terminal, collector is the output terminal, and emitter is the common terminal. The emitter terminal is grounded in the common emitter configuration. So the common emitter configuration is also known as grounded emitter configuration.

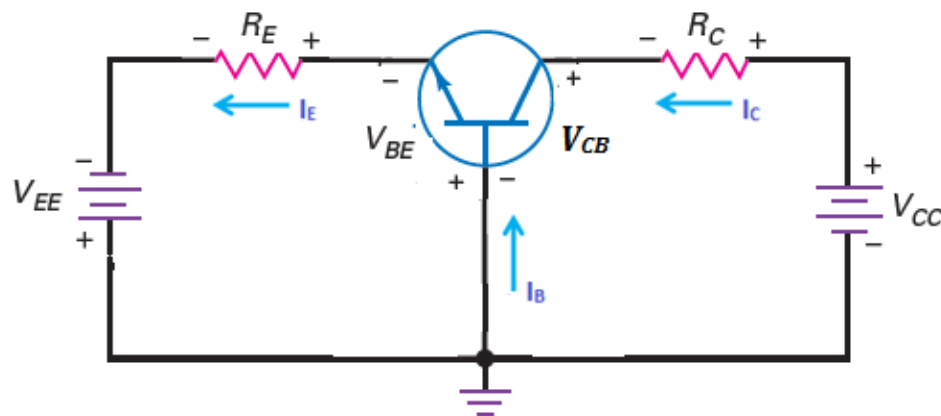
### *Common collector (CC) configuration*

In common collector configuration, base is the input terminal, emitter is the output terminal, and collector is the common terminal. The collector terminal is grounded in the common collector configuration. So the common collector configuration is also known as grounded collector configuration.

## **2.8 Common Base Configuration of Transistor (CB Configuration)**

In common base configuration, emitter is the input terminal, collector is the output terminal, and base is the common terminal between input and output.

As shown in figure EB junction is forward biased and CB junction is reverse biased. To forward bias EB junction  $V_{EE}$  battery is connected and to reverse bias CB junction  $V_{CC}$  battery is connected as shown in figure. Resistance  $R_E$  and  $R_C$  are current limiting resistors.



Current Gain and different current components in CB configuration:

**Current Gain  $\alpha_{dc}$  :**

It is defined as the ration of output current  $I_C$  to Input current  $I_E$ . it is dented by  $\alpha_{dc}$  or  $\alpha$ . It is represented by equation

$$\alpha_{dc} = \frac{I_C (inj)}{I_E} = \frac{I_C - I_{CBO}}{I_E} \quad \text{---- (1)}$$

In equation (1)

$I_C (inj)$  is injected charge carrier into the collector from emitter

$I_{CBO}$  is reverse leakage current between collector to base when emitter is open. Which is very small. If we neglect  $I_{CBO}$  then  $\alpha_{dc}$  is approximated to

$$\alpha_{dc} \cong \frac{I_C}{I_E} \quad \text{---- (2)}$$

**Collector current  $I_C$  :**

From equation (1), collector current can be written as

$$I_C = \alpha_{dc} I_E + I_{CBO} \quad \text{---- (3)}$$

as  $I_{CBO}$  is very small, If we neglect  $I_{CBO}$  then collector current  $I_C$  is approximated to

$$I_C \cong \alpha_{dc} I_E$$

**Emitter current  $I_E$  :**

Emitter current is sum of Base current  $I_B$  and collector current  $I_C$

$$I_E = I_C + I_B \quad \text{---- (4)}$$

**Base current  $I_B$  :**

$$I_B = I_E - I_C \quad \text{--- (5)}$$

Putting the value of  $I_C$  in equation (5) from equation (3)

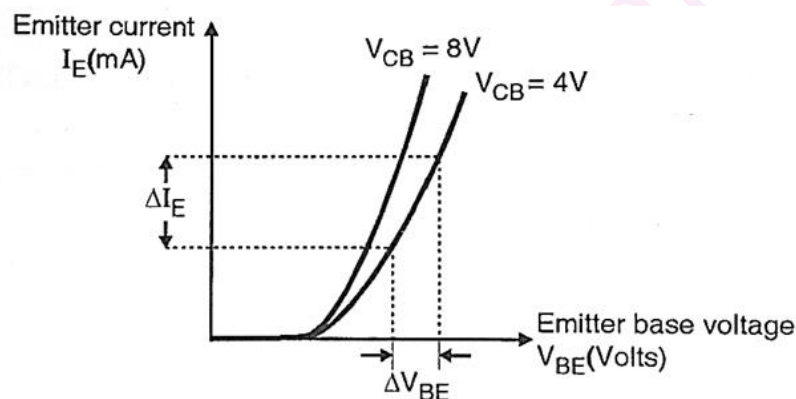
$$I_B = I_E - \alpha_{dc} I_E - I_{CBO}$$

$$I_B = I_E(1 - \alpha_{dc}) - I_{CBO} \quad \text{--- (6)}$$

$$I_B \cong I_E(1 - \alpha_{dc})$$

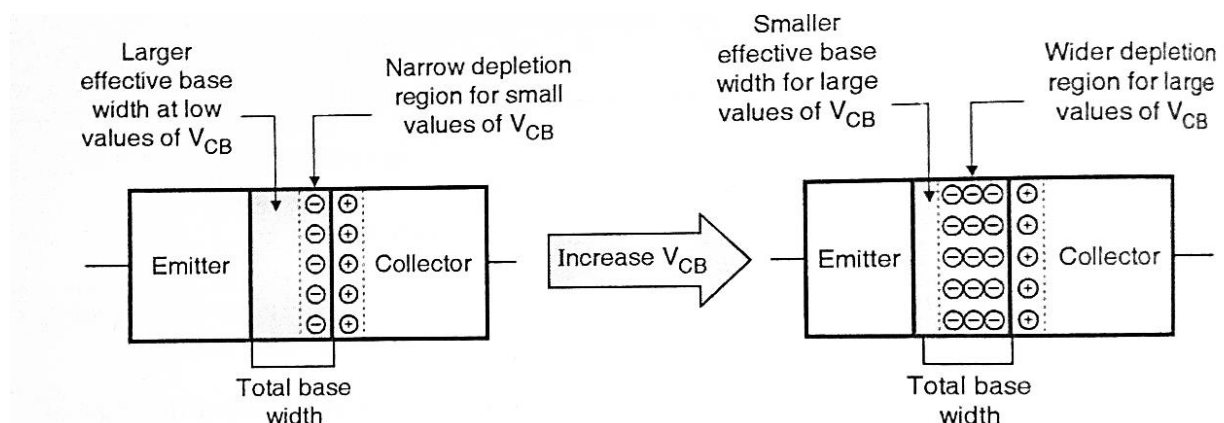
### Input Characteristic of CB configuration:

Input characteristic is the relation between transistors input current  $I_E$  and input voltage  $V_{BE}$ , keeping the output voltage  $V_{CB}$  constant.



### Base width modulation/Early effect:

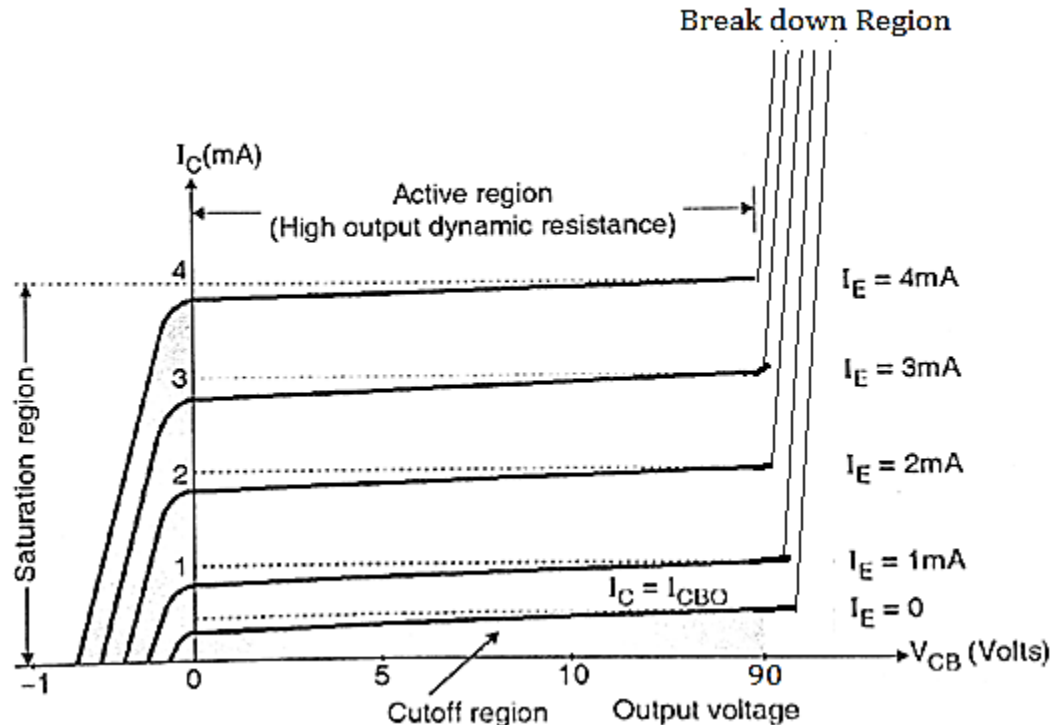
In CB configuration of transistor, if we increase  $V_{CB}$ , then depletion layer at CB junction will increase, which results in decrease in effective base width. Hence concentration gradient at EB junction will increase, which allows more electrons from emitter to diffuse into the base. So emitter current  $I_B$  will increase. Thus when collector base voltage  $V_{CB}$  is increases, emitter current  $I_E$  will also increases.



The change in effective base width due to change in  $V_{CB}$  is called Base width modulation or Early effect.

### Output Characteristic of CB configuration:

Output characteristic is the relation between transistors output current  $I_C$  and output voltage  $V_{CB}$ , keeping the input current  $I_E$  constant.

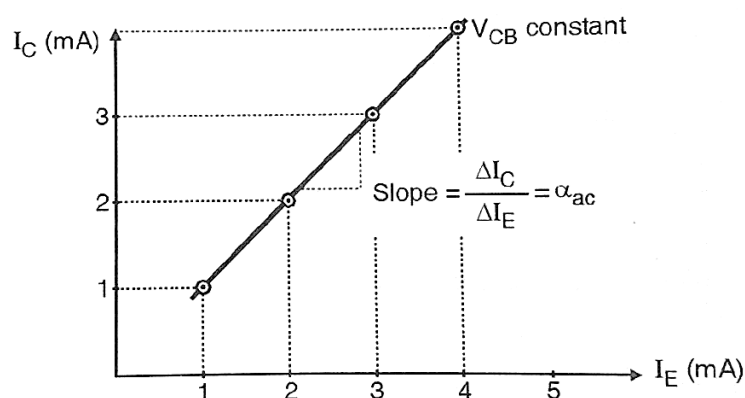


If an excessive reverse-bias voltage is applied to the collector-base junction, the device breakdown may occur.

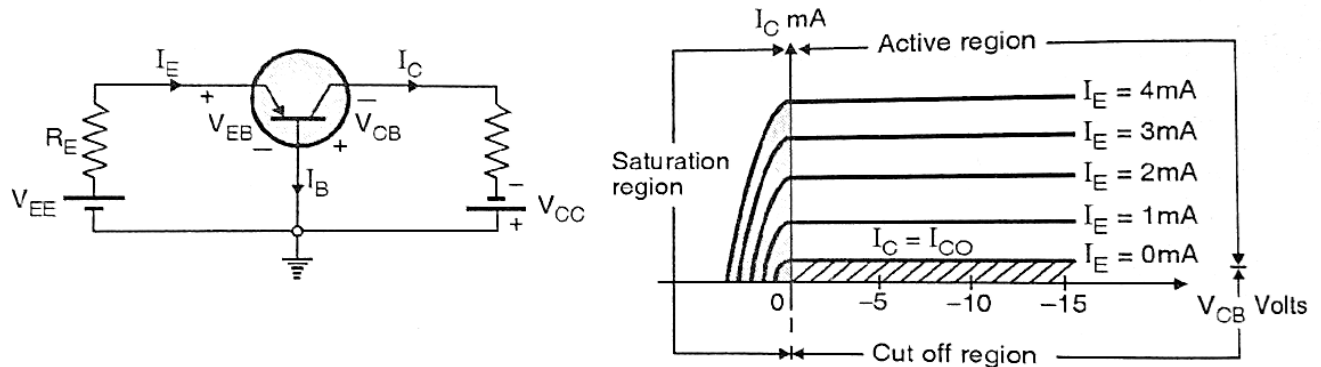
As reverse bias voltage  $V_{CB}$  is increases, collector-base depletion region also increases. If an excessive reverse-bias voltage is applied then collector-base depletion region penetrating into the base until it makes contact with emitter-base depletion region. This condition is known as *punch through* or *reach through* effect. A Very large currents can flow when it occurs and possible destroying the device.

### Transfer Characteristic of CB configuration

Transfer characteristic is the relation between transistors output current  $I_C$  and input current  $I_E$  for constant  $V_{CB}$  voltage. It is linear as shown in figure.



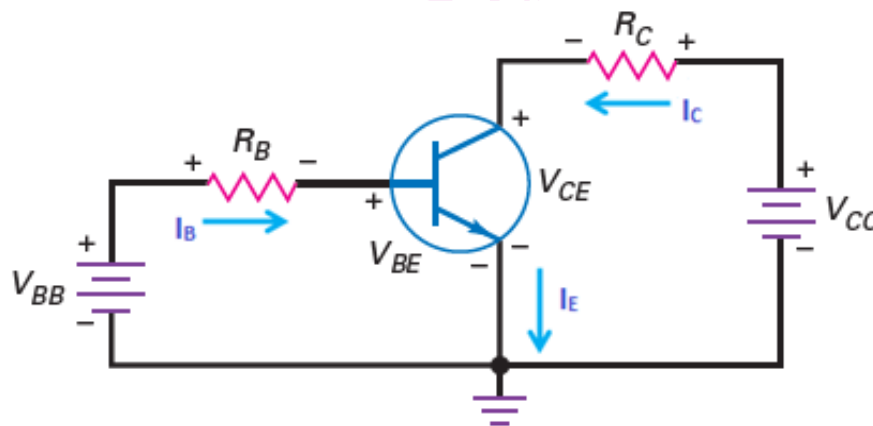
### Circuit diagram and output characteristic of CB configuration using PNP transistor:



## 2.9 Common Emitter Configuration of Transistor (CE Configuration)

In common emitter configuration, base is the input terminal, collector is the output terminal, and emitter is the common terminal between input and output.

As shown in figure EB junction is forward biased and CB junction is reverse biased. To forward bias EB junction  $V_{BB}$  battery is connected and to reverse bias CB junction  $V_{CC}$  battery is connected as shown in figure. Resistance  $R_B$  and  $R_C$  are current limiting resistors.



Current Gain and different current components in CE configuration:

### Current Gain $\beta_{dc}$ :

It is defined as the ration of output current  $I_C$  to Input current  $I_B$ . it is dented by  $\beta_{dc}$  or  $\beta$ . It is represented by equation

$$\beta_{dc} = \frac{I_C (inj)}{I_B} = \frac{I_C - I_{CEO}}{I_B} \quad \text{----- (1)}$$

In equation (1)

$I_C (inj)$  is injected charge carrier into the collector from emitter

$I_{CEO}$  is reverse leakage current between collector to emitter when base is open. Which is very small. If we neglect  $I_{CEO}$  then  $\beta_{dc}$  is approximated to

$$\beta_{dc} \cong \frac{I_C}{I_B}$$

---- (2)

**Collector current  $I_C$  :**

From equation (1), collector current can be written as

$$I_C = \beta_{dc} I_B + I_{CEO}$$

---- (3)

as  $I_{CEO}$  is very small, If we neglect  $I_{CEO}$  then collector current  $I_C$  is approximated to

$$I_C \cong \beta_{dc} I_B$$

**Emitter current  $I_E$  :**

Emitter current is sum of Base current  $I_B$  and collector current  $I_C$

$$I_E = I_C + I_B$$

---- (4)

Putting the value of  $I_C$  in equation (4) from equation (3)

$$I_E = \beta_{dc} I_B + I_{CEO} + I_B$$

$$I_E = I_B(1 + \beta_{dc}) + I_{CEO}$$

---- (5)

**Base current  $I_B$  :**

Base current  $I_B$  is

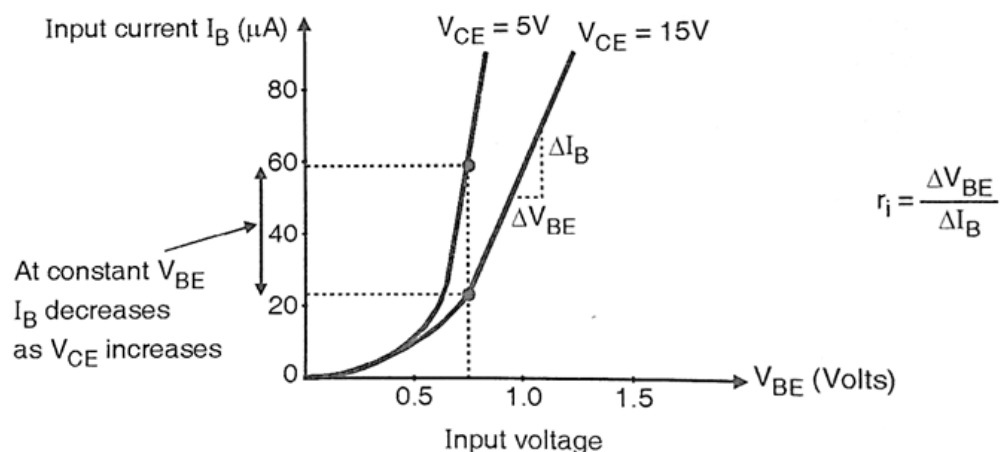
$$I_E \cong I_B(1 + \beta_{dc})$$

$$I_B = I_E - I_C$$

---- (6)

**Input Characteristic of CE configuration:**

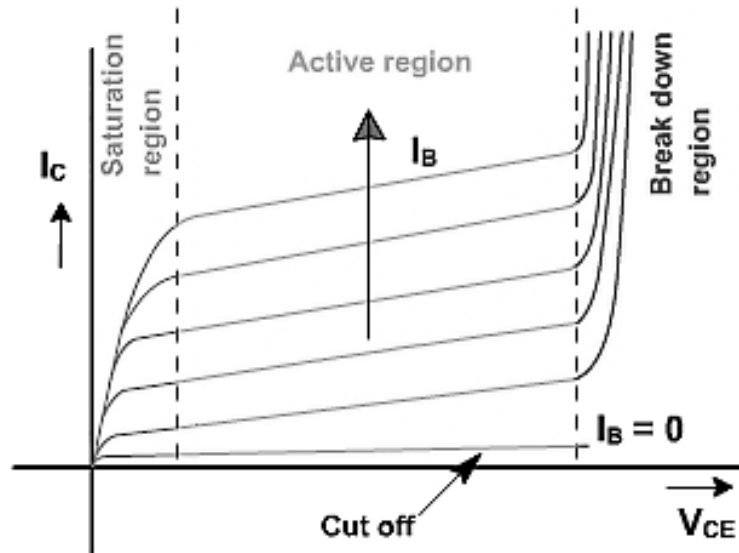
Input characteristic is the relation between transistors input current  $I_B$  and input voltage  $V_{BE}$ , keeping the output voltage  $V_{CE}$  constant.





### Output Characteristic of CE configuration:

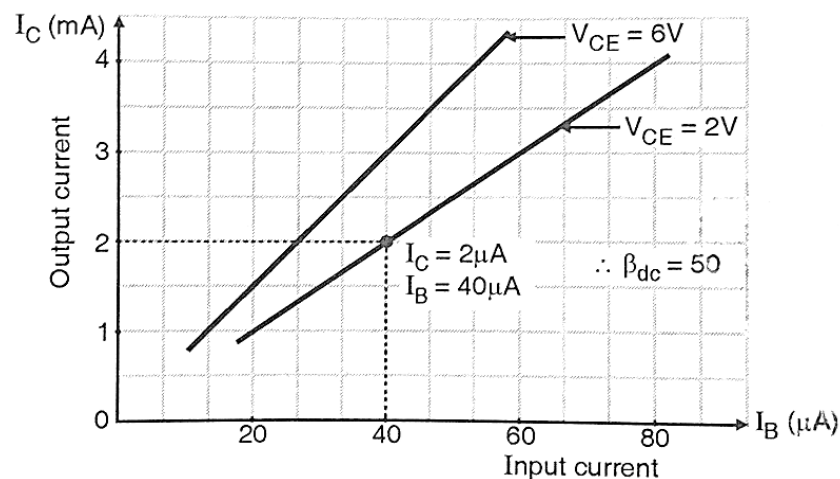
Output characteristic is the relation between transistors output current  $I_C$  and output voltage  $V_{CE}$ , keeping the input current  $I_B$  constant.



If an excessive reverse-bias voltage is applied to the collector-emitter junction, the device breakdown may occur.

### Transfer Characteristic of CE configuration

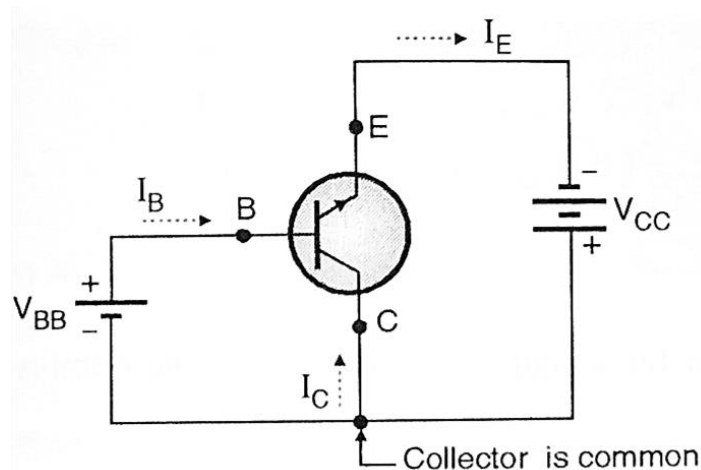
Transfer characteristic is the relation between transistors output current  $I_C$  and input current  $I_B$  for constant  $V_{CE}$  voltage. It is linear as shown in figure.



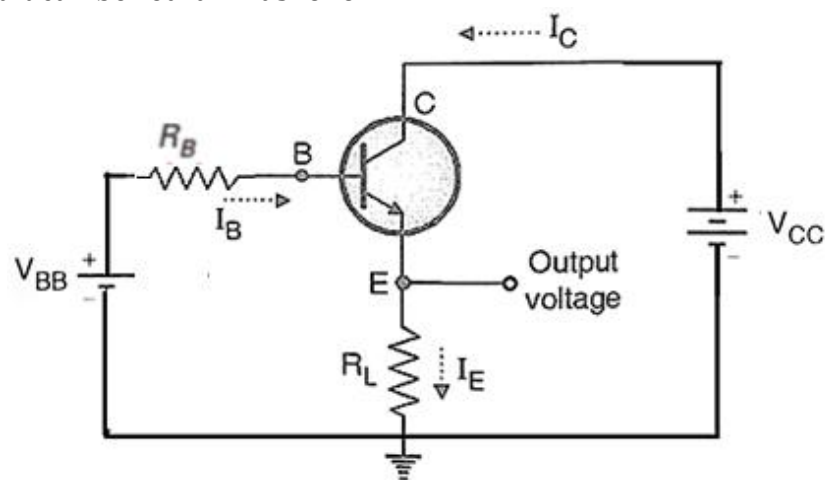
## 2.10 Common Collector Configuration of Transistor (CC Configuration)

In common collector configuration, base is the input terminal, emitter is the output terminal, and collector is the common terminal between input and output.

As shown in figure EB junction is forward biased and CB junction is reverse biased. To forward bias EB junction  $V_{BB}$  battery is connected and to reverse bias CB junction  $V_{CC}$  battery is connected as shown in figure. Resistance  $R_B$  and  $R_E$  are current limiting resistors.



The above circuit can be redrawn as follow:



Current Gain and different current components in CE configuration:

**Current Gain  $\gamma_{dc}$  :**

It is defined as the ration of output current  $I_E$  to Input current  $I_B$ . it is dented by  $\gamma_{dc}$  or  $\gamma$ . It is represented by equation

$$\gamma_{dc} = \frac{I_E}{I_B} = \frac{I_C + I_B}{I_B} \quad \text{----- (1)}$$

In equation (1)

$$I_C \cong \beta_{dc} I_B$$

Hence,

$$\gamma_{dc} \cong 1 + \beta_{dc} \quad \text{----- (2)}$$

**Collector current  $I_C$  :**

As we know that collector current can be written as

$$I_C = \alpha_{dc} I_E + I_{CBO}$$

or

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (3)}$$

as  $I_{CEO}$  is very small, If we neglect  $I_{CEO}$  then collector current  $I_C$  is approximated to

$$I_C \cong \beta_{dc} I_B$$

### Emitter current $I_E$ :

Emitter current is sum of Base current  $I_B$  and collector current  $I_C$

$$I_E = I_C + I_B \quad \text{--- (4)}$$

Putting the value of  $I_C$  in equation (4) from equation (3)

$$I_E = \beta_{dc} I_B + I_{CEO} + I_B$$

$$I_E = I_B (1 + \beta_{dc}) + I_{CEO} \quad \text{--- (5)}$$

$$I_E \cong I_B (1 + \beta_{dc})$$

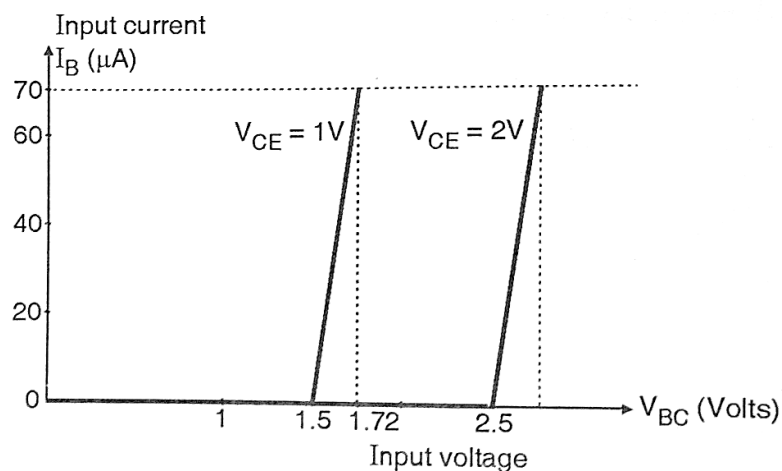
### Base current $I_B$ :

Base current  $I_B$  is

$$I_B = I_E - I_C \quad \text{--- (6)}$$

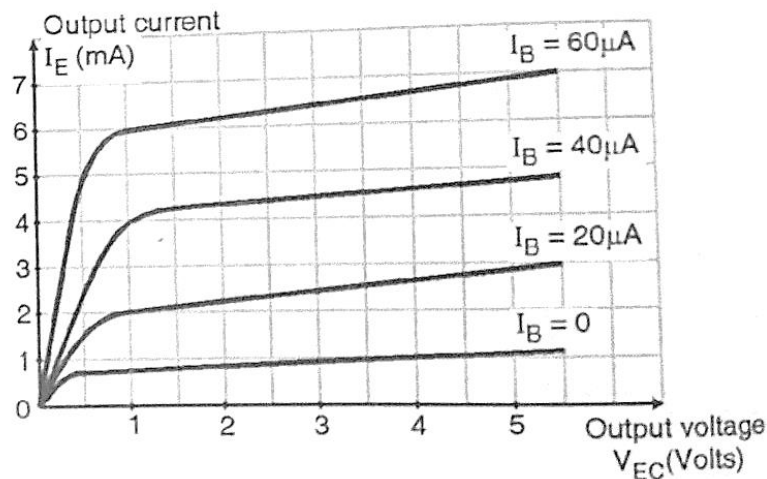
### Input Characteristic of CC configuration:

Input characteristic is the relation between transistors input current  $I_B$  and input voltage  $V_{BC}$ , keeping the output voltage  $V_{CE}$  constant.



### Output Characteristic of CC configuration:

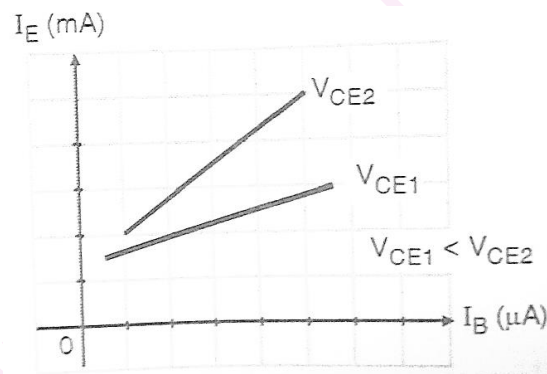
Output characteristic is the relation between transistors output current  $I_E$  and output voltage  $V_{EC}$ , keeping the input current  $I_B$  constant.



If an excessive reverse-bias voltage is applied to the collector-emitter junction, the device breakdown may occur.

### Transfer Characteristic of CC configuration

Transfer characteristic is the relation between transistors output current  $I_E$  and input current  $I_B$  for constant  $V_{CE}$  voltage. It is linear as shown in figure.



### 2.11 Relation between current gain $\alpha$ , $\beta$ and $\gamma$

The emitter current equation is

$$I_E = I_B + I_C \quad \text{---- (1)}$$

Dividing equation (1) by  $I_C$

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad \text{---- (2)}$$

$$\frac{1}{\alpha} = \frac{1 + \beta}{\beta}$$

$$\alpha = \frac{\beta}{1 + \beta}$$

---- (3)

Equation (3) indicates  $\alpha$  in terms of  $\beta$ 

Rearranging equation (2) again

$$\frac{1}{\beta} = \frac{1}{\alpha} - 1$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

---- (4)

Equation (4) indicates  $\beta$  in terms of  $\alpha$ 

Also the emitter current equation is

$$I_E = I_B + I_C \quad \text{---- (5)}$$

Dividing equation (7) by  $I_B$ 

$$\frac{I_E}{I_B} = \frac{I_B}{I_B} + \frac{I_C}{I_B}$$

$$\gamma = 1 + \beta$$

---- (6)

### 2.12 Relation between leakage current $I_{CBO}$ and $I_{CEO}$

Emitter current is

$$I_E = I_B + I_C$$

In CB configuration, collector current is

$$I_C = \alpha I_E + I_{CBO} \quad \text{--- (1)}$$

Putting the value of emitter current  $I_E = I_B + I_C$  in equation (1)

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$(1 - \alpha) I_C = \alpha I_B + I_{CBO}$$

Hence,

$$I_C = \left( \frac{\alpha}{1 - \alpha} \right) (I_B) + \left( \frac{I_{CBO}}{1 - \alpha} \right)$$

--- (2)

But in equation (2)

$$\frac{\alpha}{1 - \alpha} = \beta$$

and

$$1 - \alpha = 1 - \frac{\beta}{1 + \beta} = \frac{1}{1 + \beta}$$

$$\frac{1}{1 - \alpha} = 1 + \beta$$

Now, equation (2) can be written as

$$I_C = \beta I_B + (1 + \beta) I_{CBO} \quad \text{--- (3)}$$

In CE configuration, collector current is

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (4)}$$

Comparing equation (3) and (4)

$$I_{CEO} = (1 + \beta) I_{CBO} \quad \text{---- (5)}$$

### 2.13 Comparison between CB, CE and CC configuration of transistor

Sr. No.	Parameters	CB	CE	CC
1	Common terminal between input and output	Base	Emitter	Collector
2	Input current	$I_E$	$I_B$	$I_B$
3	Output current	$I_C$	$I_C$	$I_E$
4	Current Gain	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\gamma_{dc} = \frac{I_E}{I_B}$
		Low	High	High
5	Input voltage	$V_{EB}$	$V_{BE}$	$V_{CB}$
6	Output voltage	$V_{CB}$	$V_{CE}$	$V_{EC}$
7	Voltage gain	Medium	High	Low
8	Input Impedance	Very low (20 $\Omega$ )	Medium (1 K $\Omega$ )	Very high (1 M $\Omega$ )
9	Output impedance	Very high (1 M $\Omega$ )	High (40 K $\Omega$ )	Very low (50 $\Omega$ )
10	Power gain	Medium	Very High	Medium
11	Leakage current	Low	High	High
12	Signal Phase	In phase with input	Out of phase with input	In phase with input
13	Application	Preamplifier	Audio Amplifier	Impedance matching

### 2.14 Why CE configuration is most preferred?

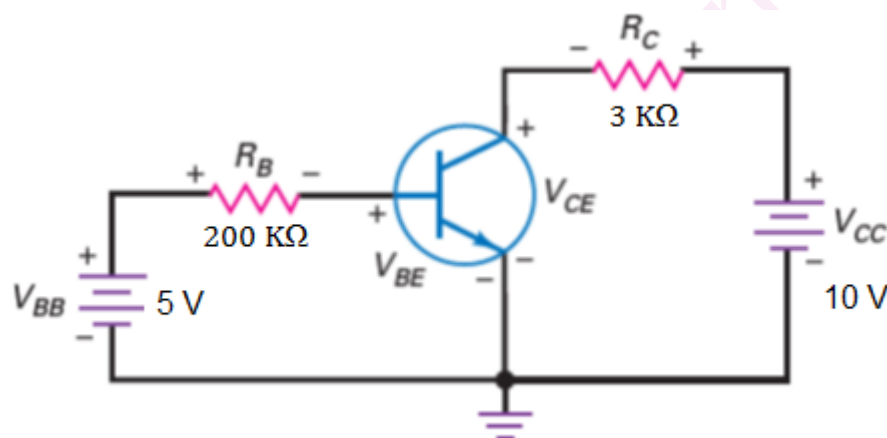
Out of three configuration of transistor, CE configuration is most popular and widely used because of following reason

- (i) It has high current and voltage gain.
- (ii) Power gain is high.
- (iii) Input and Output impedance are moderate/high. Hence many such stage of CE configuration can be coupled/cascaded to gather without any additional impedance matching circuit.

### 2.15 Examples

#### Example-1

For NPN transistor connected in CE configuration as shown in figure, calculate transistor currents and  $\alpha$ . Given data are  $\beta = 100$ ,  $I_{CO} = 2 \times 10^{-8}$  mA.



Base Current:

Apply KVL law at input loop.

$$V_{BB} = I_B R_B + V_{BE}$$

Assuming  $V_{BE} = 0.7$  V

$$5 = I_B (200 \times 10^3) + 0.7$$

$$I_B = 21.5 \mu\text{A} \quad \text{--- (1)}$$

Collector Current:

$$I_C = \beta I_B + I_{CO}$$

Putting the value of  $I_B$  from equation (1)

$$I_C = 100 \times (21.5 \times 10^{-6}) + 2 \times 10^{-8}$$

$$I_C = 2.15 \text{ mA} \quad \text{---- (2)}$$

Emitter Current:

$$I_E = I_B + I_C$$

Putting the value of  $I_B$  and  $I_C$  from equation (1) and (2)

$$I_E = (21.5 \times 10^{-6}) + 2.15 \times 10^{-3}$$

$$I_E = 2.17 \text{ mA} \quad \text{---- (3)}$$

Current Gain  $\alpha$ :

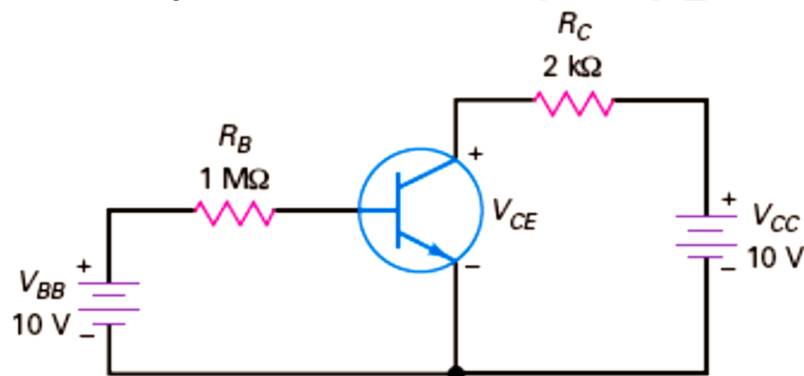
$$\alpha = \frac{I_C}{I_E} = \frac{2.15}{2.17} = 0.99 \quad \text{--- (4)}$$

Also

$$\alpha = \frac{\beta}{1 + \beta} = \frac{100}{1 + 100} = 0.99$$

### Example-2

For NPN transistor connected in CE configuration as shown in figure, calculate transistor currents  $I_B$ ,  $I_C$ ,  $V_{CE}$ , and  $P_D$  if  $\beta = 300$ .



Base Current:

Apply KVL law at input loop.

$$V_{BB} = I_B R_B + V_{BE}$$

Assuming  $V_{BE} = 0.7 \text{ V}$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10 - 0.7}{1 \times 10^6} = 9.3 \times 10^{-3}$$

$$I_B = 9.3 \text{ } \mu\text{A} \quad \text{--- (1)}$$

Collector Current:

$$I_C = \beta I_B$$

Putting the value of  $I_B$  from equation (1)

$$I_C = 300 \times (9.3 \times 10^{-6})$$

$$I_C = 2.79 \text{ mA} \quad \text{---- (2)}$$



Collector to Emitter voltage  $V_{CE}$ :

Apply KVL law at output loop.

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

Putting the value of  $I_B$  and  $I_C$  from equation (1) and (2)

$$V_{CE} = 10 - 2.79 \times 10^{-3} \times 2 \times 10^3$$

$$V_{CE} = \mathbf{4.42 \quad volt} \quad \text{---- (3)}$$

Power dissipation  $P_D$ :

$$P_D = V_{CE} I_C = 4.42 \times 2.79 \times 10^{-3} = \mathbf{12.3 \times 10^{-3}} \quad \text{--- (4)}$$

$$P_D = \mathbf{12.3 \quad mW}$$

## Transistor Biasing & Thermal Stability

### 2.16 Transistor Biasing & Need of biasing

What is Biasing?

Use of DC potential (DC Battery/power supply) to establish the operating condition of transistor is called biasing.

Transistor can be operated in either of three regions

Condition	(E-B Junction)	(C-B Junction)	Operating Region	Application
FR	<b>Forward Biased</b>	Reverse Biased	<b>Active</b>	<b>Amplifier</b>
FF	<b>Forward Biased</b>	<b>Forward Biased</b>	Saturation	Switch
RR	Reverse Biased	Reverse Biased	Cutoff	Switch

In order to operate in either of region, DC battery/power supply is required to be connected with correct polarity.

Biasing in electronics means establishing predetermined voltages or currents at various points of an electronic circuit for the purpose of establishing proper operating conditions in electronic components.

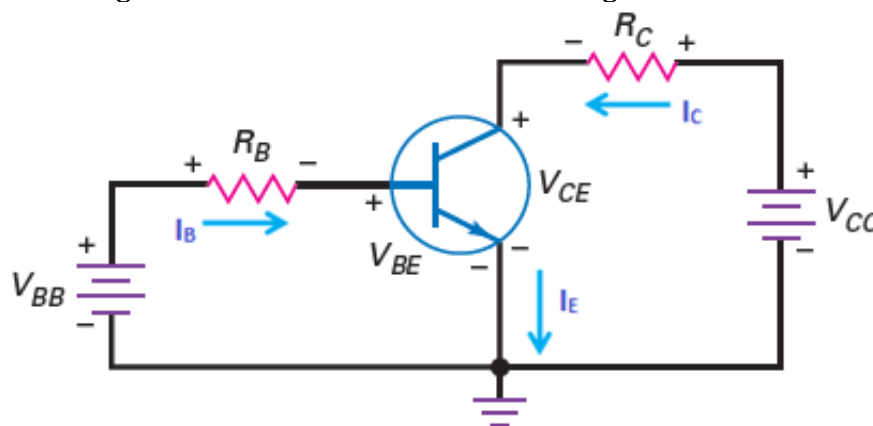
Need of Biasing :

- (i) To stabilize the operating point Q.
- (ii) To set operating point Q, at center of DC load line.
- (iii) To reduce the value of stability factor (S)
- (iv) Stabilize the collector current against temperature variations.
- (v) To operate the transistor in active region as an amplifier OR To operate the transistor as a switch

### 2.17 DC Load line and Operating point Q

The DC load line represents the desirable combinations of the collector current  $I_C$  and the collector-emitter voltage  $V_{CE}$ . It is drawn when no signal is given to the input, and the transistor biased with DC supply.

Consider the CE configuration of transistor as shown in figure.



For the given circuit, applying KVL low at output loop,

$$V_{CC} = I_C R_C + V_{CE} \quad \text{---- (1)}$$

Rearranging equation (1)

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = \left( -\frac{1}{R_C} \right) (V_{CE}) + \left( \frac{V_{CC}}{R_C} \right) \quad \text{---- (2)}$$

Equation (2) is like the equation of straight line i.e.  $y = mx + C$

The straight line represented by equation (2) is called **DC Load Line**.

In equation (2) when  $V_{CE} = 0$ ,

$$I_C = \frac{V_{CC}}{R_C}$$

This is maximum possible current through transistor. Hence

$$I_{C(max)} = \frac{V_{CC}}{R_C} \quad \text{---- (3)}$$

Equation (3) is maximum possible current through transistor. So it is called **Saturation** point. Hence

$$I_{C(saturation)} = \frac{V_{CC}}{R_C}$$

Now, in equation (2) when  $I_C = 0$ ,

$$V_{CE} = V_{CC}$$

This is maximum possible voltage across transistor. Hence

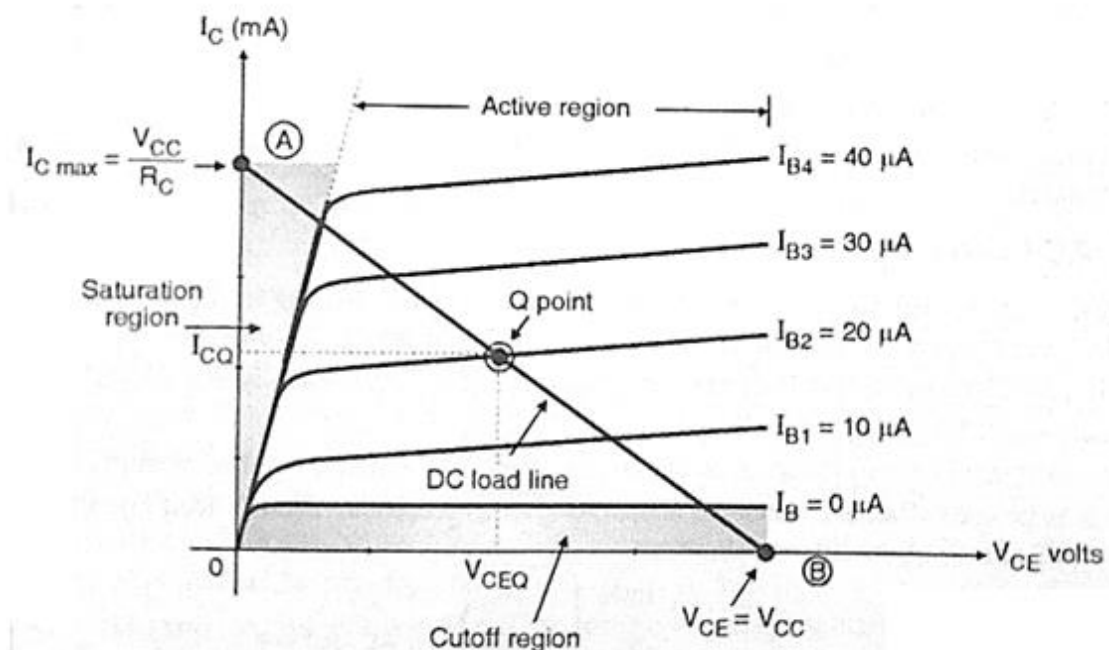
$$V_{CE(max)} = V_{CC} \quad \text{---- (4)}$$

Equation (4) is maximum possible voltage across transistor. So it is called **cut-off** point. Hence

$$V_{CE(cut-off)} = V_{CC}$$

Line joining the Saturation and cut-off point is called **DC Load Line**. it is a straight line as shown in figure. Any point/value corresponding to  $I_C$  and  $V_{CE}$  will be on this DC Load Line

The DC Load Line is shown with output characteristic of transistor.



### Q point (Quiescent point)

The Q point is also called **operating point** OR Bias point OR Quiescent point.

It is the point on DC Load Line, which represents the DC current  $I_{CQ}$  through transistor and voltage  $V_{CEQ}$  across transistor in quiescent or steady state/DC condition.

The co-ordinates of Q point are  $I_{CQ}$  and  $V_{CEQ}$ .

$$Q = (I_{CQ}, V_{CEQ})$$

The position of Q point on dc load line depends on application of transistor. When transistor is used as an amplifier, operating point Q should be set at the center of dc load line to avoid distortion in output waveform.

Position of Q point on dc load line is determined based on its application,

Application	Position of Q point
ON switch	At cut-off point/Region
OFF switch	At saturation point/Region
Amplifier	At center of dc load line/ In Active Region

### 2.18 Factors affecting the stability of Q point

Ideally Q point must be stable. It should not shift upward or downward on dc load line. But practically, Q point is unstable and changes its position on dc load line. The factors affecting the stability of Q point are

- (i) Change in temperature
- (ii) Change in value of  $\beta_{dc}$
- (iii) Variation in transistor parameters from one device to another.

#### (1) Q point instability due to Temperature.

As temperature changes, current through transistor will also change. Due to change in junction temperature of transistor its parameter like  $V_{BE}$ ,  $\beta_{dc}$  and  $I_{CBO}$  will change. Which in turn results in change in operating point Q ( $I_{CQ}$ ,  $V_{CEQ}$ ).

#### (2) Q point instability due to change in $\beta_{dc}$

Collector current of transistor is related with  $\beta_{dc}$ , as per equation  $I_C = \beta I_B$ . Hence if  $\beta_{dc}$  changes then collector current will also change. Which in turn results in change in operating point Q ( $I_{CQ}$ ,  $V_{CEQ}$ ).

#### (3) Q point instability due to variation in transistor parameter

Parameters like  $\beta_{dc}$  of two transistors with same number, type and manufacturer are slightly different in value. So when one transistor is replaced by another transistor, its collector current will also change. Which in turn results in change in operating point Q ( $I_{CQ}$ ,  $V_{CEQ}$ ).

### 2.19 Stability factor:

Stability factor indicates the stability of Q point against the variation/change in transistor parameters. Stability of Q point in transistor depends on following three parameters.

- (i) Reverse Leakage current  $I_{CO}$
- (ii) Current gain  $\beta_{dc}$
- (iii) Base to emitter voltage  $V_{BE}$

#### Stability factor S:

It is defined as the ratio of change in collector current due to change in reverse saturation current/leakage current  $I_{CO}$ , when  $\beta_{dc}$  and  $V_{BE}$  are constant.

$$S = \frac{\Delta I_C}{\Delta I_{CO}} \quad \text{For constant } \beta_{dc} \text{ and } V_{BE}$$

#### Stability factor S' :

It is defined as the ratio of change in collector current due to change in  $V_{BE}$ , when  $\beta_{dc}$  and  $I_{CO}$  are constant

$$S' = \frac{\Delta I_C}{\Delta V_{BE}} \quad \text{For constant } \beta_{dc} \text{ and } I_{CO}$$

#### Stability factor S'' :

It is defined as the ratio of change in collector current due to change in  $\beta_{dc}$ , when  $V_{BE}$  and  $I_{CO}$  are constant

$$S'' = \frac{\Delta I_C}{\Delta \beta_{dc}} \quad \text{For constant } V_{BE} \text{ and } I_{CO}$$

***Ideally the value of stability factor should be Zero. Practically it should be small as possible.***

### 2.20 Bias Stabilization Techniques/Biasing Circuits:

Bias stabilization is a process of stabilizing the Q point. Hence biasing circuit is required to be designed to keep operating point stable on dc load line.

Requirement of biasing circuits

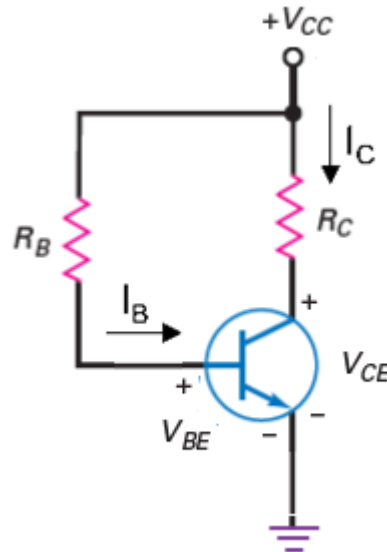
- (i) To establish the operating point Q at the middle of load line.
- (ii) Stabilize collector current against variation in temperature.
- (iii) To make operating point Q independent of transistor parameter.

Various biasing circuits

- (i) Fixed Bias circuit.
- (ii) Collector to Base Bias circuit.
- (iii) Voltage Divider Bias circuit.

### 2.21 Fixed Bias Circuit (Single Base Resistor Bias/Base Bias):

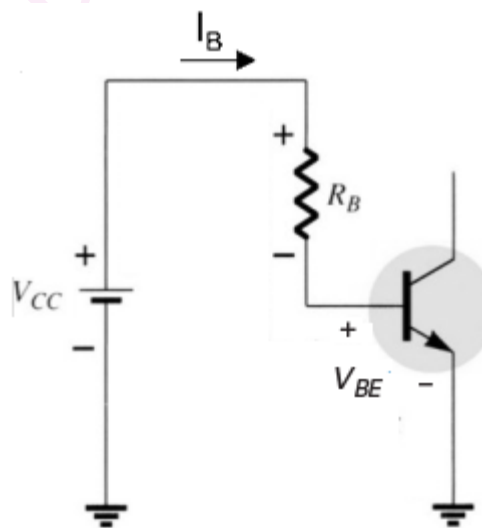
The fixed-bias configuration is the simplest of transistor biasing arrangement. Fixed bias circuit is as shown in figure



Steps to find Q point:

#### **Input section:**

DC equivalent circuit can be drawn as follow.  
Let us consider only the input section of circuit



If we apply KVL law at input loop then,

$$V_{CC} = I_B R_B + V_{BE} \quad \text{---- (1)}$$

from equation (1), base current is given as

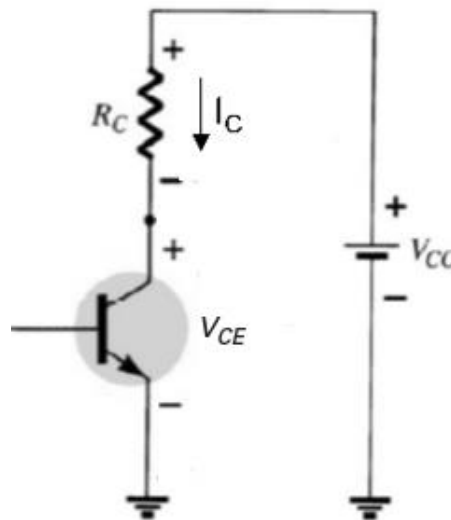
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \text{--- (2)}$$

Since  $V_{BE}$  is very small, it can be neglected compared to  $V_{CC}$  then equation (2) can be approximated to

$$I_B \cong \frac{V_{CC}}{R_B}$$

**Output section:**

Let us consider only the output section of circuit



The collector current in terms of Base current is derived by equation

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (3)}$$

If we apply KVL law at output loop then,

$$V_{CC} = I_C R_C + V_{CE} \quad \text{---- (4)}$$

from equation (4), collector to emitter voltage is given as

$$V_{CE} = V_{CC} - I_C R_C \quad \text{--- (5)}$$

Equation (3) and (5) are the equation of operating point Q

$$I_{CQ} = \beta_{dc} I_B + I_{CEO}$$

$$V_{CEQ} = V_{CC} - I_C R_C$$

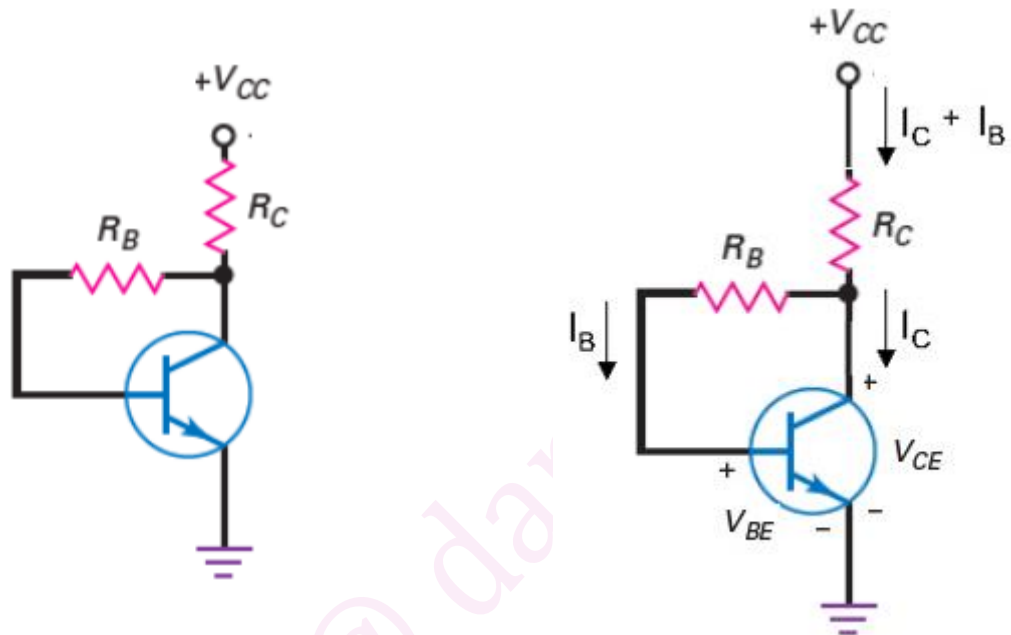
*Stabilization of Q point in Fixed bias circuit:*

- The fixed bias circuit is simple and easy to design. But still it is seldom used because it can not stabilize operating point Q.

- if temperature increases then leakage current  $I_{CEO}$  will change, which will result in change in  $I_{CQ}$  corresponding to Q point.
- Also if transistor is replaced by another transistor then  $\beta_{dc}$  may change which results in change in  $I_{CQ}$  corresponding to Q point.

### 2.22 Collector to Base Bias Circuit:

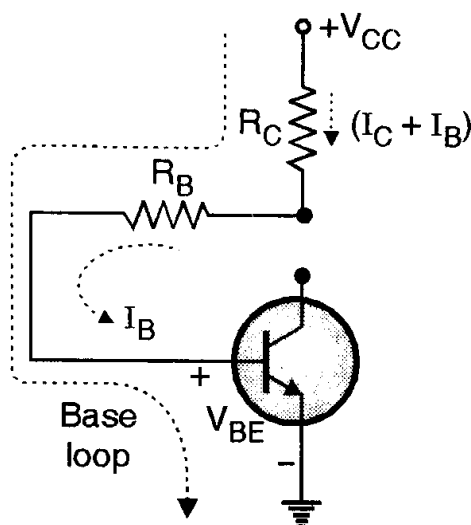
In collector to base bias configuration, base resistor  $R_B$  is connected to the collector terminal instead of battery  $V_{CC}$ . collector to base bias circuit is as shown in figure.



Steps to find Q point:

#### Input section:

Let us consider only the input loop/section of circuit



If we apply KVL law at input loop then,

$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE} \quad \text{---- (1)}$$



$$V_{CC} = I_C R_C + (R_C + R_B) I_B + V_{BE}$$

from equation (1), base current is given as

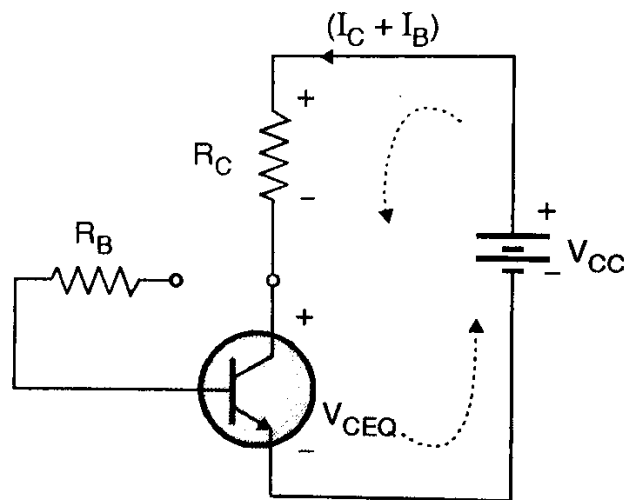
$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B} \quad \text{--- (2)}$$

Since  $V_{BE}$  is very small, it can be neglected compared to  $V_{CC}$  then equation (2) can be approximated to

$$I_B \cong \frac{V_{CC} - I_C R_C}{R_C + R_B}$$

### Output section:

Let us consider only the output section of circuit



The collector current in terms of Base current is derived by equation

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (3)}$$

If we apply KVL law at output loop then,

$$V_{CC} = (I_C + I_B) R_C + V_{CE} \quad \text{---- (4)}$$

from equation (4), collector to emitter voltage is given as

$$V_{CE} = V_{CC} - (I_C + I_B) R_C \quad \text{--- (5)}$$

Also,

$$V_{CE} = V_{CC} - I_C R_C - I_B R_C \quad \text{----- (6)}$$

As Current  $I_B \ll I_C$ , equation (6) can be approximated to

$$V_{CE} \cong V_{CC} - I_C R_C \quad \text{----- (7)}$$

If we replace the value of equation (7) in equation (2) then Base current can be written as

$$I_B \cong \frac{V_{CE} - V_{BE}}{R_C + R_B}$$

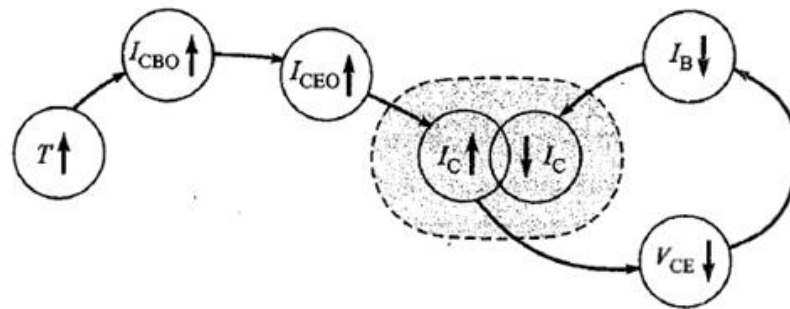
Equation (3) and (5) are the equation of operating point Q

$$I_{CQ} = \beta_{dc} I_B + I_{CEO}$$

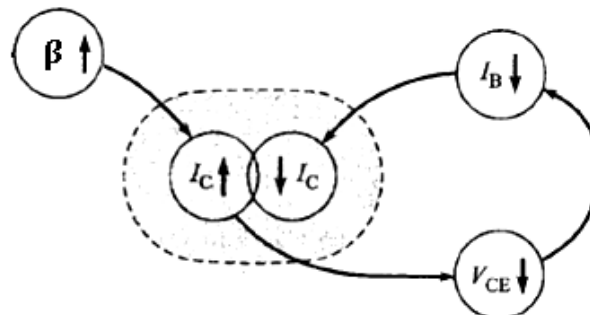
$$V_{CEQ} = V_{CC} - (I_C + I_B) R_C$$

*Stabilization of Q point in collector to base bias circuit:*

- if temperature increases then leakage current  $I_{CEO}$  will increase, which will result in increase in  $I_{CQ}$ . If collector current  $I_C$  increases then  $V_{CE}$  will decrease (because  $V_{CE} \cong V_{CC} - I_C R_C$ ). When  $V_{CE}$  decreases, it also decreases base current  $I_B$ . Decrease in base current forces collector current to decrease. Hence increase of collector current due to temperature will be stabilize by decrease in base current.



- if transistor is replaced by another transistor then  $\beta_{dc}$  may change which results in change in  $I_{CQ}$  corresponding to Q point. If collector current  $I_C$  increases then  $V_{CE}$  will decrease (because  $V_{CE} \cong V_{CC} - I_C R_C$ ). When  $V_{CE}$  decreases, it also decreases base current  $I_B$ . Decrease in base current forces collector current to decrease. Hence increase of collector current due to change in  $\beta_{dc}$  will be stabilize by decrease in base current.

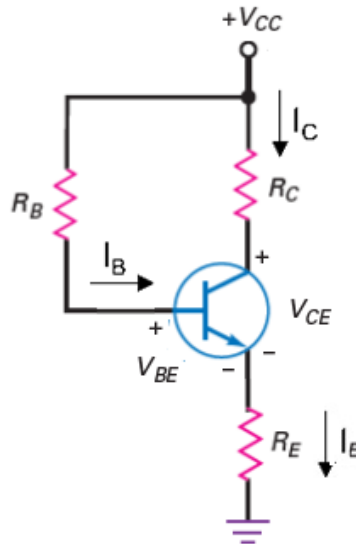


*Limitation of collector to base bias circuit:*

- Collector to base bias circuit is seldom used because base resistor provides negative feedback, which reduces the gain of not only DC but also AC input signal.

### 2.23 Emitter feedback Bias Circuit (Bias circuit with emitter resistor):

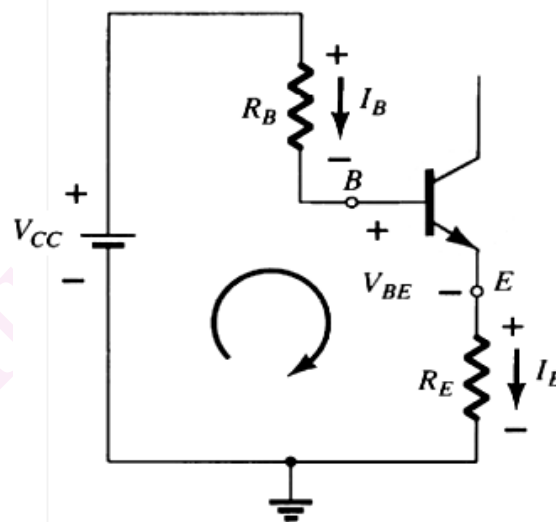
In emitter feedback bias three resistors  $R_B$ ,  $R_C$ , and  $R_E$  are connected as shown in figure. Emitter resistor provides negative feedback. This circuit can able to stabilize operating point Q..



Steps to find Q point:

#### Input section:

Let us consider only the input loop/section of circuit



If we apply KVL law at input loop then,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \quad \text{---- (1)}$$

from equation (1), base current is given as

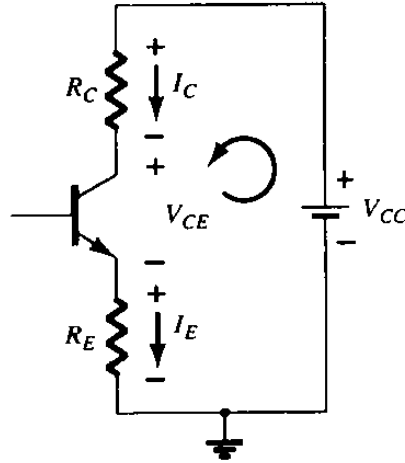
$$I_B = \frac{V_{CC} - I_E R_E - V_{BE}}{R_B} \quad \text{--- (2)}$$

Since  $V_{BE}$  is very small, it can be neglected compared to  $V_{CC}$  then equation (2) can be approximated to

$$I_B \cong \frac{V_{CC} - I_E R_E}{R_B}$$

### Output section:

Let us consider only the output section of circuit



The collector current in terms of Base current is derived by equation

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (3)}$$

If we apply KVL law at output loop then,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \quad \text{---- (4)}$$

from equation (4), collector to emitter voltage is given as

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \quad \text{--- (5)}$$

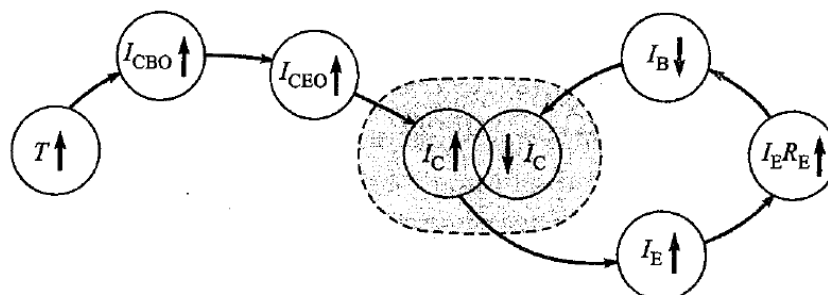
Equation (3) and (5) are the equation of operating point Q

$$I_{CQ} = \beta_{dc} I_B + I_{CEO}$$

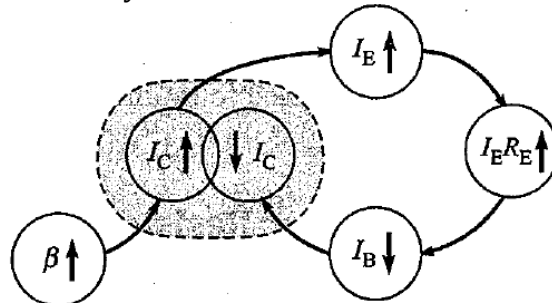
$$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$$

*Stabilization of Q point in collector to base bias circuit:*

- if temperature increases then leakage current  $I_{CEO}$  will increase, which will result in increase in  $I_{CQ}$ . If collector current  $I_C$  increases then  $I_E$  will increase. When  $I_E$  increases, it results in decreases in base current  $I_B$ . Decrease in base current forces collector current to decrease. Hence increase of collector current due to temperature will be stabilize by decrease in base current.



- if transistor is replaced by another transistor then  $\beta_{dc}$  may change which results in change in  $I_{CQ}$  corresponding to Q point. If collector current  $I_C$  increases then  $I_E$  will increase. When  $I_E$  increases, it results in decreases in base current  $I_B$ . Decrease in base current forces collector current to decrease. Hence increase of collector current due to change in  $\beta_{dc}$  will be stabilize by decrease in base current.

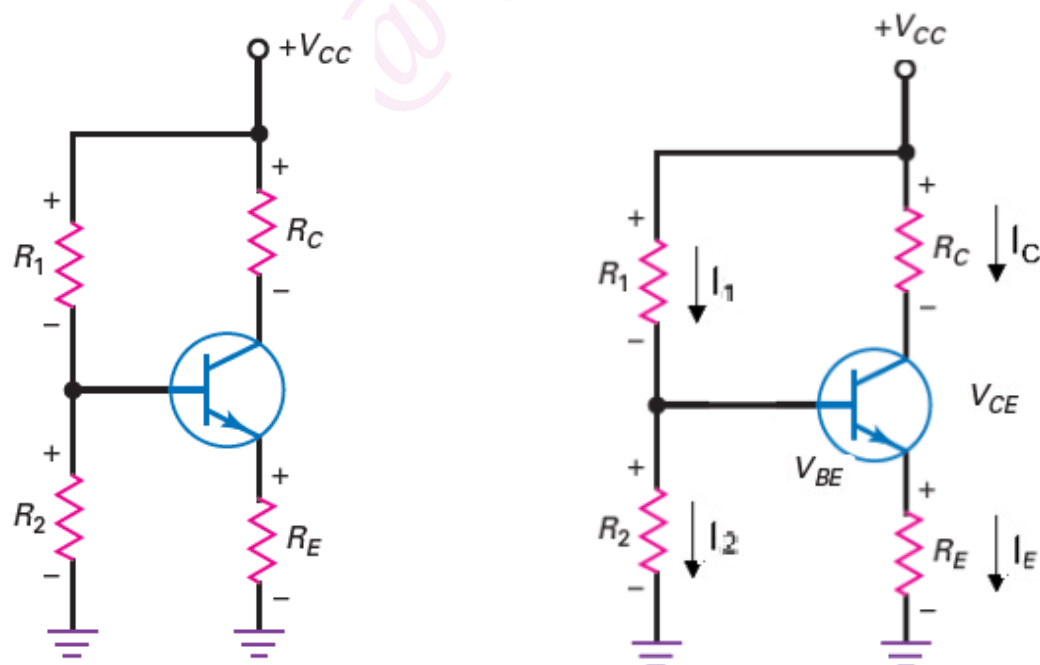


*Limitation of collector to base bias circuit:*

In emitter bias, emitter resistor provides negative feedback, which reduces the gain of not only DC but also AC input signal but reduction in AC gain can be avoided by connecting one capacitor in parallel with emitter resistor.

## 2.24 Voltage Divider Bias Circuit (Self Bias):

It is most widely used biasing circuit. It stabilize the operating point Q against change in temperature as well as transistor current gain  $\beta_{dc}$ . Voltage divider bias circuit is as shown in figure. The base circuit contains a voltage divider ( $R_1$  and  $R_2$ ). Because of this, the circuit is called voltage-divider bias.



Resistor  $R_1$  and  $R_2$  forms voltage divider network. To simplify the circuit, it can be converted to Thevenin's equivalent circuit.

Thevenin's equivalent circuit can be derived by finding out Thevenin equivalent Resistor  $R_{TH}$  and Voltage  $V_{TH}$ .

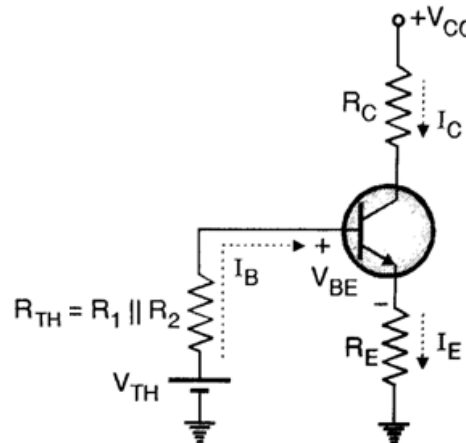
Thevenin's equivalent Resistor

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

Thevenin's equivalent Voltage

$$V_{TH} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

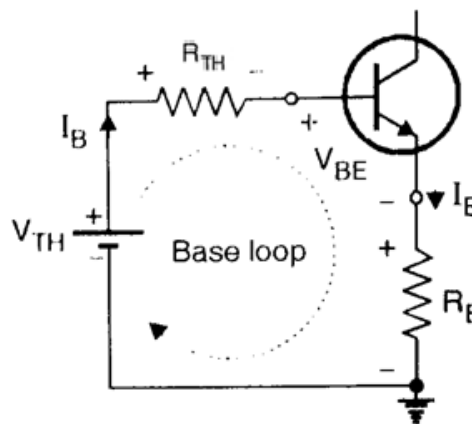
Now Thevenin's equivalent circuit is



Steps to find Q point:

### Input section:

Let us consider only the input loop/section of Thevenin's equivalent circuit



If we apply KVL law at input loop then,

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E \quad \text{---- (1)}$$

$$\text{But, } I_E = (1 + \beta_{dc}) I_B$$

$$V_{TH} = I_B R_{TH} + V_{BE} + (1 + \beta_{dc}) I_B R_E \quad \text{---- (2)}$$

from equation (2), base current is given as

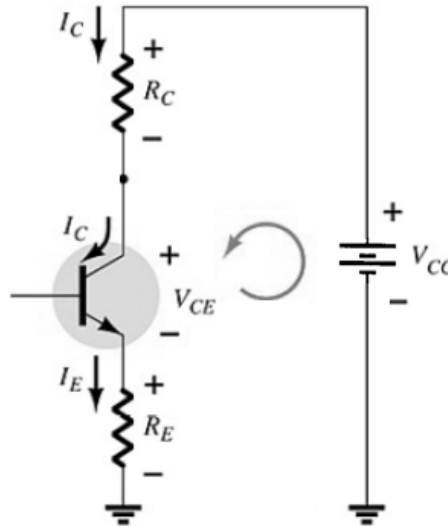
$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1 + \beta_{dc}) R_E} \quad \text{----- (3)}$$

Since  $V_{BE}$  is very small, it can be neglected compared to  $V_{TH}$ . Also  $\beta_{dc} \gg 1$ , then equation (3) can be approximated to

$$I_B \cong \frac{V_{TH}}{R_{TH} + \beta_{dc} R_E}$$

**Output section:**

Let us consider only the output section of circuit



The collector current in terms of Base current is derived by equation

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (4)}$$

If we apply KVL law at output loop then,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \quad \text{---- (5)}$$

from equation (5), collector to emitter voltage is given as

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \quad \text{--- (6)}$$

Equation (4) and (6) are the equation of operating point Q

$$I_{CQ} = \beta_{dc} I_B + I_{CEO}$$

$$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$$

**2.25 Bias Compensation Techniques:**

Bias stabilization and compensation techniques are used to stabilize the operating point Q against variation in Temperature,  $I_{CO}$ ,  $\beta_{dc}$ , and  $V_{BE}$ .

Stabilization techniques refer to the use of resistive biasing circuits.

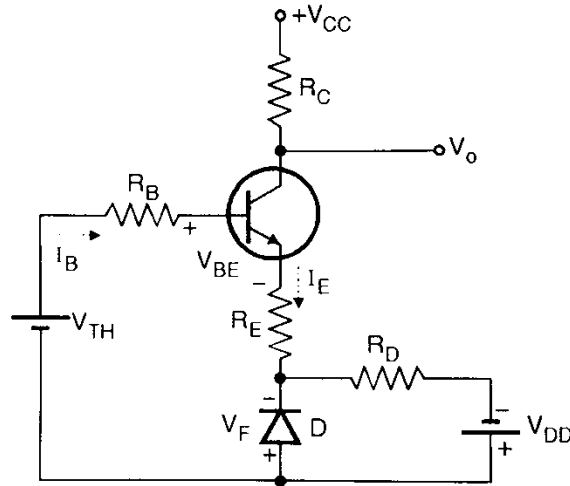
Compensation techniques refer to the use of temperature sensitive device such as Diode, Thermistor, Sensistor.

Types of bias compensation techniques includes

- (i) Compensation for changes in  $V_{BE}$ .
- (ii) Compensation for changes in  $I_{CO}$ .

### (1) Diode compensation for $V_{BE}$

As shown in figure Diode and transistor used are of same material and type. Also diode and transistor have same temperature co-efficient.



Applying KVL low at input base loop,

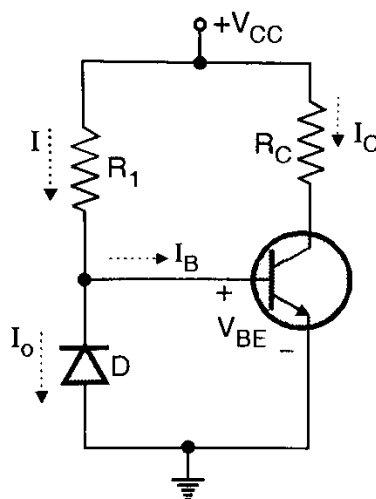
$$V_{TH} = I_B R_B + V_{BE} + I_E R_E - V_F \quad \text{---- (1)}$$

But material used for diode is same as that for transistor and have same temperature co-efficient. Hence change in voltage across diode  $V_F$  is same as change in  $V_{BE}$  across transistor due to change in Temperature. So in equation (1),  $V_F$  and  $V_{BE}$  will be cancel out.

Thus change in  $V_{BE}$  due to temperature is compensated by change in  $V_F$  and collector current corresponding to Q point, becomes insensitive to variation in transistor parameter  $V_{BE}$ .

### (2) Diode compensation for $I_{CO}$

The diode compensation circuit shown in figure offers stabilization against variation in  $I_{CO}$ . Diode and transistor are of same type and material. Therefore reverse saturation current of diode  $I_O$  will increase with temperature at the same rate as leakage current of transistor  $I_{CO}$  will change.





As diode is reverse biased, current through resistor  $R_1$  is

$$I_1 = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} = \text{constant}$$

The base current  $I_B = I - I_O$ . Now substitute the value of  $I_B$  in equation of collector current

$$I_C = \beta_{dc} I_B + (1 + \beta_{dc}) I_{CO}$$

$$I_C = \beta_{dc}(I - I_O) + (1 + \beta_{dc}) I_{CO}$$

$$I_C = \beta_{dc} I - \beta_{dc} I_O + (1 + \beta_{dc}) I_{CO} \quad \text{---(1)}$$

In equation (1), reverse leakage current of diode ( $I_O$ ) is same as leakage current of transistor ( $I_{CO}$ ), because material used for diode and transistor is same.

Also,

$$\beta_{dc} I_O \approx (1 + \beta_{dc}) I_{CO}$$

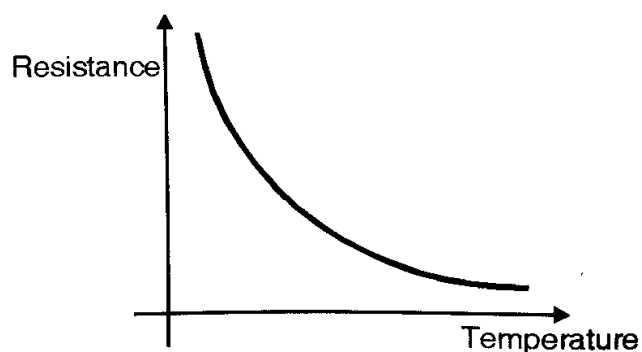
Hence equation (1) can be now written as

$$I_C = \beta_{dc} I$$

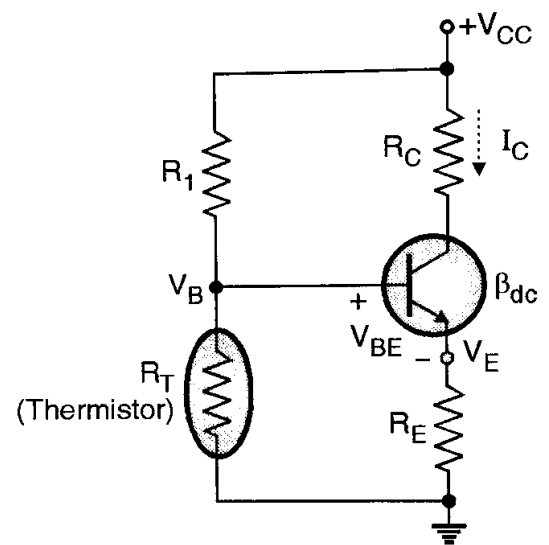
As current  $I$  is constant, collector current  $I_C$  will also remain constant irrespective of change in temperature. Thus compensation provided against change in  $I_{CO}$  due change in temperature.

### (3) Bias compensation using Thermistor

Thermistor is temperature dependent resistor. It's resistance decreases exponentially as temperature increases. So thermistor has negative temperature co-efficient of resistance. As shown in figure, thermistor  $R_T$  is connected along with  $R_1$  and forms voltage divider network.



Characteristic of Thermistor



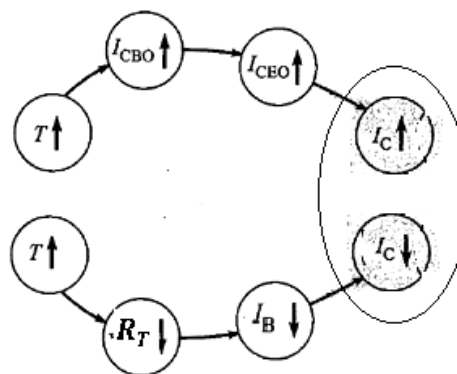
Now voltage  $V_B$  at base can be derived as

$$V_B = \frac{R_T V_{CC}}{R_1 + R_T}$$

Also,  $V_E = I_E R_E$  and  $V_{BE} = V_B - V_E$

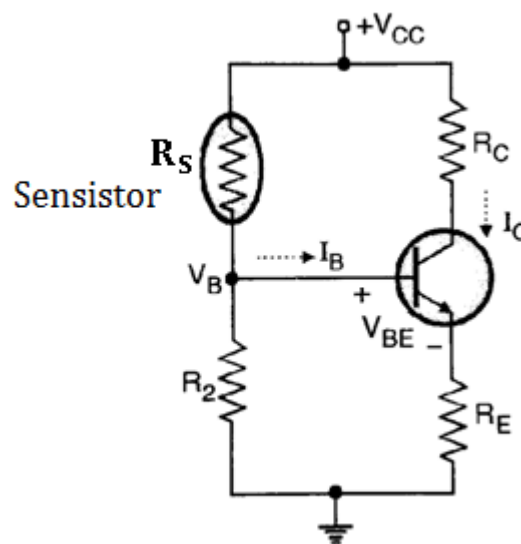
Now as temperature increase, collector current  $I_C$  tends to increase. At the same time increase in temperature, causes resistance of thermistor  $R_T$  to decrease. Hence base voltage  $V_B$  and  $V_{BE}$  decrease. This will force the base current  $I_B$  to decrease. Reduction in base current  $I_B$  will reduce collector current.

Hence increase in collector current due to temperature is compensated by decrease in collector current due to thermistor.



#### (4) Bias compensation using Sensistor

Sensistor is temperature dependent resistor. It's resistance increases exponentially as temperature increases. So sensistor has positive temperature co-efficient of resistance. As shown in figure, sensistor  $R_S$  is connected along with  $R_2$  and forms voltage divider network.



Now voltage  $V_B$  at base can be derived as

$$V_B = \frac{R_2 V_{CC}}{R_2 + R_T}$$

Also,  $V_F = I_F R_F$  and  $V_{BF} = V_B - V_F$

Now as temperature increase, collector current  $I_C$  tends to increase. At the same time increase in temperature, causes resistance of sensistor  $R_S$  to increase. Hence base voltage  $V_B$  and  $V_{BE}$  decrease. This will force the base current  $I_B$  to decrease. Reduction in base current  $I_B$  will reduce collector current.

Hence increase in collector current due to temperature is compensated by decrease in collector current due to sensistor.

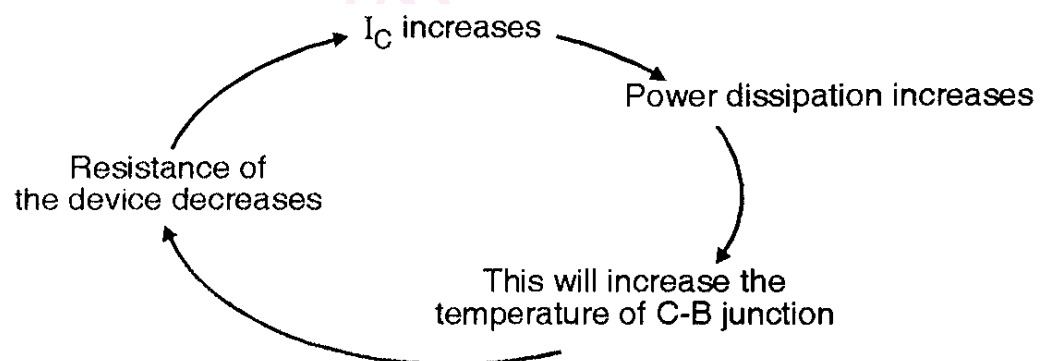
### 2.26 Thermal Runaway.

Maximum power a transistor can dissipate without getting damaged depends on the maximum temperature that a collector-base junction can withstand. Rise in temperature across collector –base junction can due to cumulative internal heating process.

The collector current in transistor is represented by equation

$$I_C = \beta_{dc} I_B + I_{CEO}$$

- If collector current increases, then power dissipation at collector-base junction also increases.
- Increase in power dissipation results in increase in temperature at C-B junction.
- As transistor has negative temperature co-efficient of resistance, increase in temperature at C-B junction, decreases resistance.
- The reduced resistance will increase the collector current.



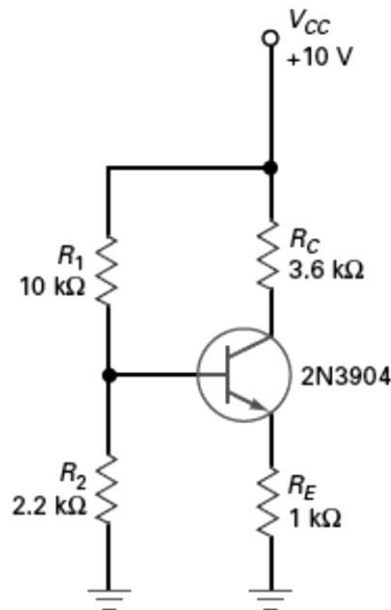
This becomes cumulative process which will finally results in damage/burning-off to transistor due to excessive internal heating. This process is known as **Thermal Runaway**.

Thermal runaway can be avoided by

- Limiting collector current beyond certain maximum rating level.
- Limiting power dissipation below maximum permissible level.
- Using Heat Sink.

**2.27 Example-3**

What is the collector-emitter voltage for transistor shown in figure.



For voltage divider bias circuit, to find out  $V_{CB}$ , we need to derive voltage  $V_C$  and  $V_E$

For voltage divider .

$$V_{BB} = \frac{2.2 \text{ K}\Omega \times V_{CC}}{2.2 \text{ K}\Omega + 10 \text{ K}\Omega}$$

$$V_{BB} = \frac{2.2 \times 10^3 \times 10}{12.2 \times 10^3} = 1.8 \text{ volt}$$

Assuming  $V_{BE} = 0.7 \text{ V}$

$$V_{BB} = V_{BE} + I_E R_E = V_{BE} + V_E$$

$$V_E = V_{BB} - V_{BE}$$

$$V_E = 1.8 - 0.7 = 1.1 \text{ volt}$$

Emitter current is

$$I_E = \frac{V_E}{R_E} = \frac{1.1}{1 \times 10^3} = 1.1 \text{ mA}$$

Collector Current is almost same as emitter current

Now collector voltage can be derived as

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 10 - 1.1 \times 10^{-3} \times 3.6 \times 10^3 = 10 - 3.96 = 6.04$$

Hence,

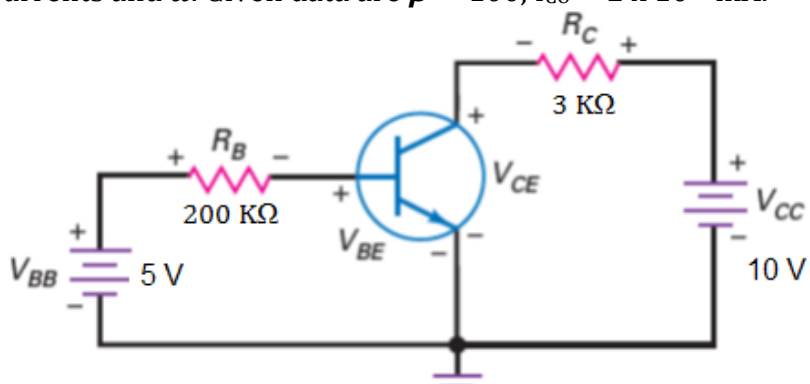
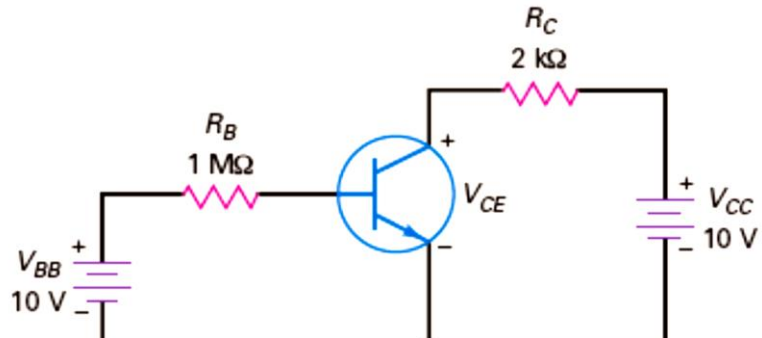
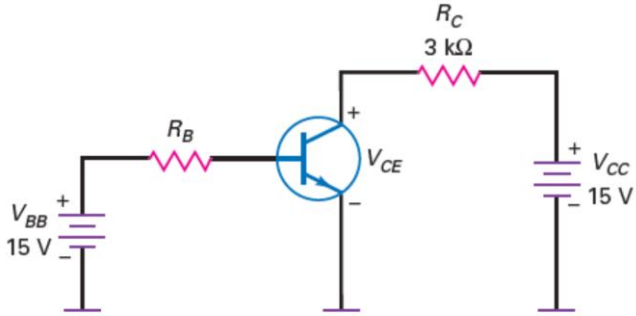
$$V_{CE} = V_C - V_E = 6.04 - 1.1 = 4.94 \text{ volt}$$

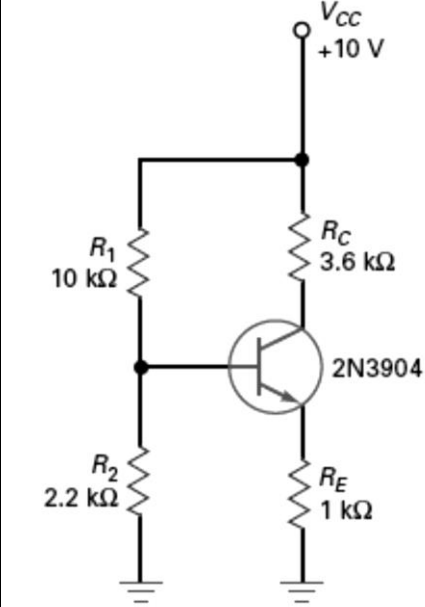
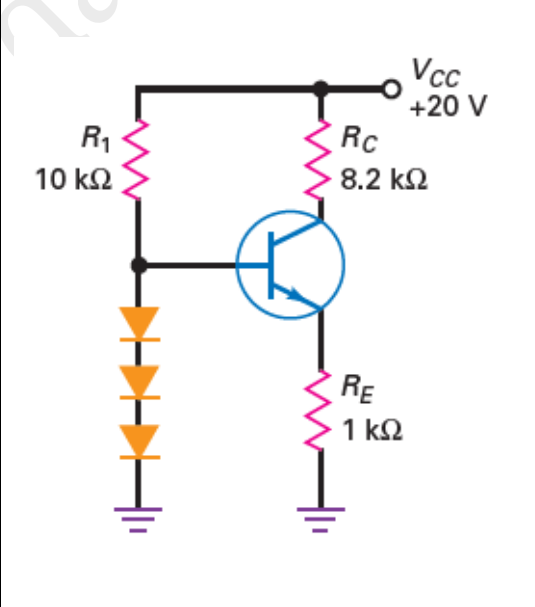
**Exercise: Question Bank Unit-2**

		<b>Marks</b>
Q:1	Classify the Transistors	4
Q:2	Draw the construction and symbol of NPN and PNP transistor and explain unbiased transistor in detail. Also give details of different operating region of transistor	7
Q:3	Explain working of Bipolar Junction Transistor in Active region	7
Q:4	Define following terms: (i) Emitter efficiency (ii) Base transportation factor (iii) Large signal current gain	3
Q:5	<b><i>Explain Common Base configuration (CB) of transistor in detail with necessary derivation, input characteristic and output characteristic.</i></b>	7
Q:6	<b><i>Using NPN transistor draw the circuit diagram of Common Emitter configuration (CE configuration) of transistor and explain it in detail with necessary derivation, input characteristic and output characteristic.</i></b>	7
Q:7	Explain Common Collector configuration (CC) of transistor in detail with necessary derivation, input characteristic and output characteristic.	7
Q:8	<b><i>What is Base width modulation or Early effect in transistor? Explain it in detail for CB configuration</i></b>	4
Q:9	Explain punch through or Reach through effect in transistor for CE configuration	4
Q:10	<b><i>Establish the relationship between current gain <math>\alpha</math>, <math>\beta</math> and <math>\gamma</math></i></b>	4
Q:11	Establish the relationship between leakage current $I_{CBO}$ and $I_{CEO}$	4
Q:12	<b><i>Compare CB, CE and CC configuration of transistor</i></b>	7
Q:13	<b><i>Why CE configuration of transistor is most preferred?</i></b>	3
Q:14	What do you mean by Biasing? What is the need of biasing circuits?	4
Q:15	<b><i>Explain the concept DC Load line and Operating point Q. Also derive the equation of operating point Q for CE configuration.</i></b>	7
Q:16	Which are the factors that affects the stability of Q point?	4
Q:17	Define Stability factor S, S' and S''	3
Q:18	Explain Base Bias OR Fixed Bias circuit in detail with necessary circuit diagram and also derive the equations of Q point for Fixed bias	7
Q:19	<b><i>Explain Collector to Base Bias circuit in detail with necessary circuit diagram and also derive the equations of Q point.</i></b>	7

Q:20	Explain Emitter feedback Bias circuit in detail with necessary circuit diagram and also derive the equations of Q point.	7
Q:21	<b>Explain Voltage Divider Bias OR Self Bias OR Universal Biasing circuit in detail with necessary circuit diagram and also derive the equations of Q</b>	7
Q:22	What is the difference between bias stabilization techniques and Bias Compensation Techniques. Explain different bias compensation techniques.	7
Q:23	<b>Write short note on Thermal Runaway</b>	4

**Tutorials/Examples**

		<b>Marks</b>
Q:1	<p>For NPN transistor connected in CE configuration as shown in figure, calculate transistor currents and <math>\alpha</math>. Given data are <math>\beta = 100</math>, <math>I_{CO} = 2 \times 10^{-8}</math> mA.</p> 	7
Q:2	<p>For NPN transistor connected in CE configuration as shown in figure, calculate transistor currents <math>I_B</math>, <math>I_C</math>, <math>V_{CE}</math>, and <math>P_D</math> if <math>\beta = 300</math>.</p> 	7
Q:3	Derive stability factor S for CB and CE configuration of transistor.	4
Q:4	<p>Find out ends of DC load line for the circuit shown in figure. Also draw the DC load line for given circuit</p> 	4

<b>Q:5</b>	Calculate the saturation and cutoff values for circuit shown in figure <i>and</i> Draw the load lines	<b>4</b>
<b>Q:6</b>	Calculate Q Point for given circuit. if $\beta = 100$ .	<b>7</b>
<b>Q:7</b>	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;">  <p>Figure . 7</p> </div> <div style="text-align: center;">  <p>Figure . 8</p> </div> </div>	<b>4</b>
<b>Q:8</b>	Calculate $I_C$ , $V_{CE}$ , $V_C$ and $V_E$ for the circuit shown in figure.8. all the diodes and transistor are made from silicon material	<b>7</b>
<b>Q:9</b>	Find out LED current for the circuit shown in figure.9.	<b>4</b>
<b>Q:10</b>	Find out LED current for the circuit shown in figure.10.	<b>4</b>

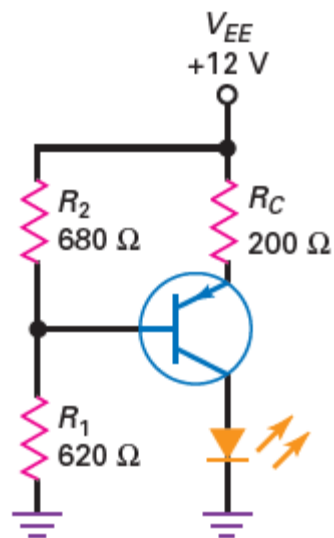


Figure . 9

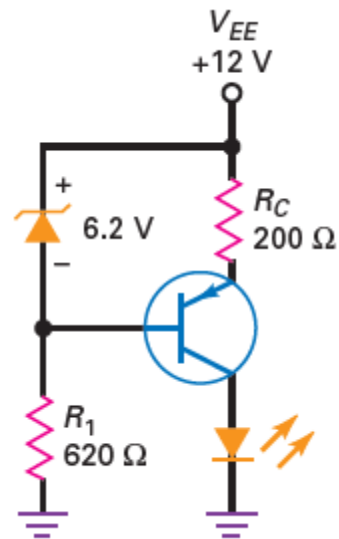


Figure . 10