Digital Electronics (303105220)

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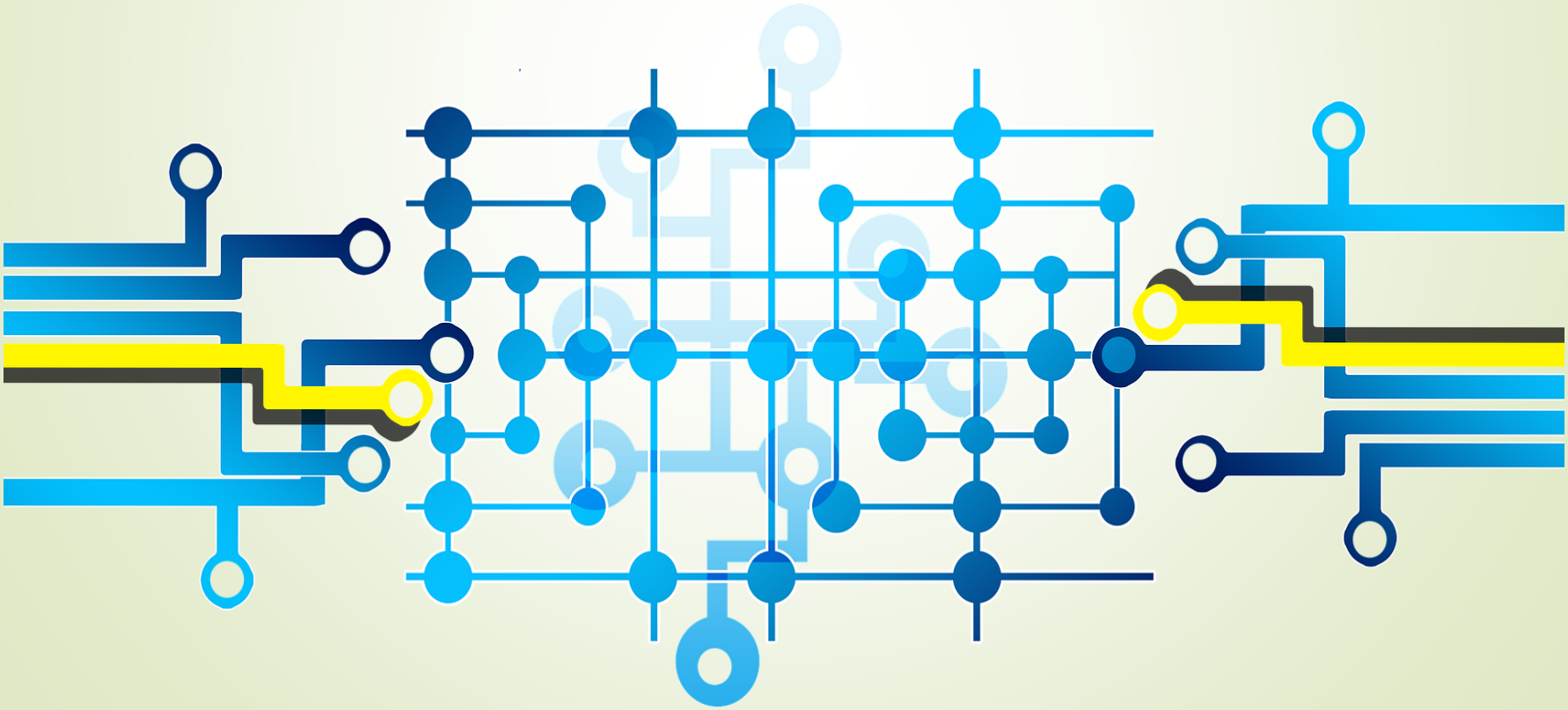


CHAPTER-6

Semiconductor Memories And Programmable Logic Devices

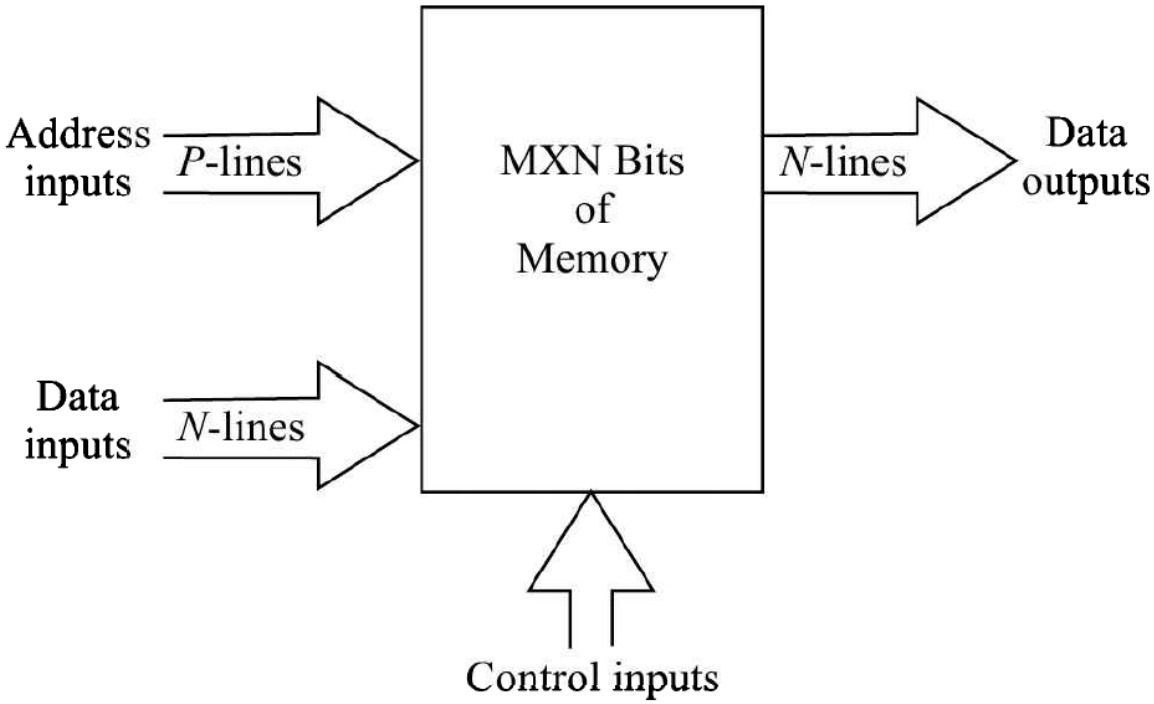
Classification and characteristics of memories, Content addressable memory (CAM), commonly used memory chips, Introduction of PLD, ROM as a PLD, Programmable logic array, Programmable array logic, Complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA)

Classification and characteristics of memories

- **Memory :** means for storing data (information) in the form of words. It is made of storage locations for storing numeric or alphanumeric information or program codes.
- Memory used to store data : **Data Memory**
- Memory used to store programs : **Program Memory**
- Usually, computers store programs in the form of machine language instructions, in binary codes.
- Each **memory location** is identified by an **address.** Each memory location can accommodate one or more bits **(word).**
- **Capacity** refers to the total number of bits (or bytes) a device computer can store.
- Memories are made of storage elements (FFs, capacitors, or magnetic domains).
- **Word** is the fundamental group of bits used to represent one entity of information (one numerical value, one alphanumeric value, etc.)
- The word size may be a multiple of 1 byte, e.g. 2 bytes (16-bit word), 4 bytes (32-bit word), etc.
- Each memory location holds one word of information.
- Size of memory is expressed as a multiple of 2^{10} = 1024 (K), e.g., memory of size 2048 represents 2K memory, 2^{16} = 65536 is 64 K, and so on.

Classification and characteristics of memories

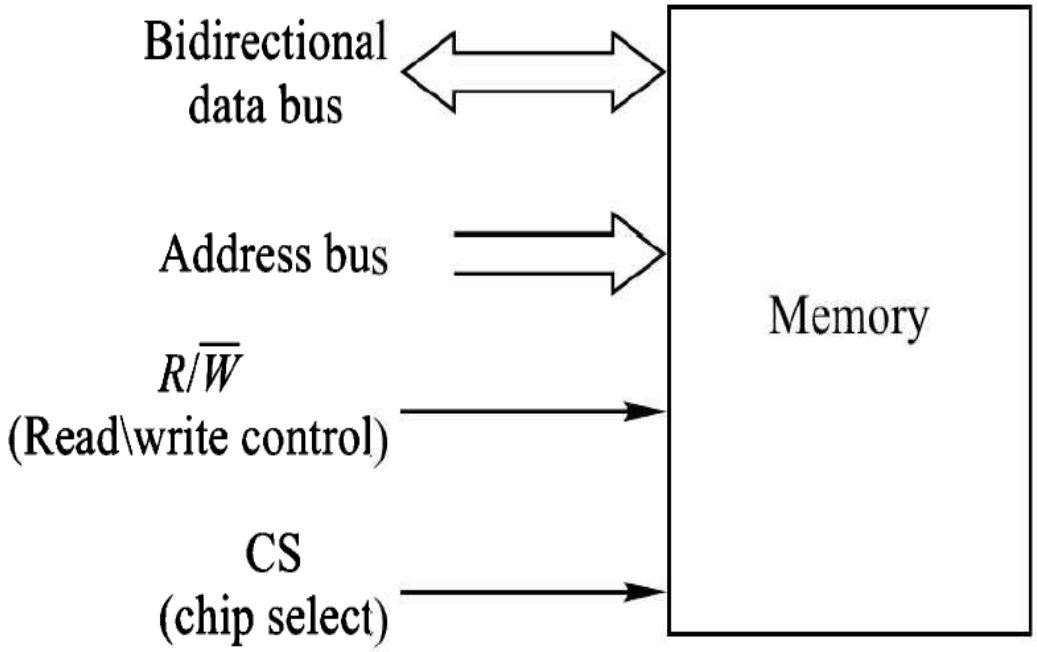
- There are a number of locations in a memory chip. Each location stores one word of information.
- The size of the memory chip is specified by two numbers M and N as MxN. M = number of locations available in the memory = 2^P; N = number of bits at the memory location.



Classification and characteristics of memories

Q. Determine the binary address of each memory location for a memory of size 16 words.

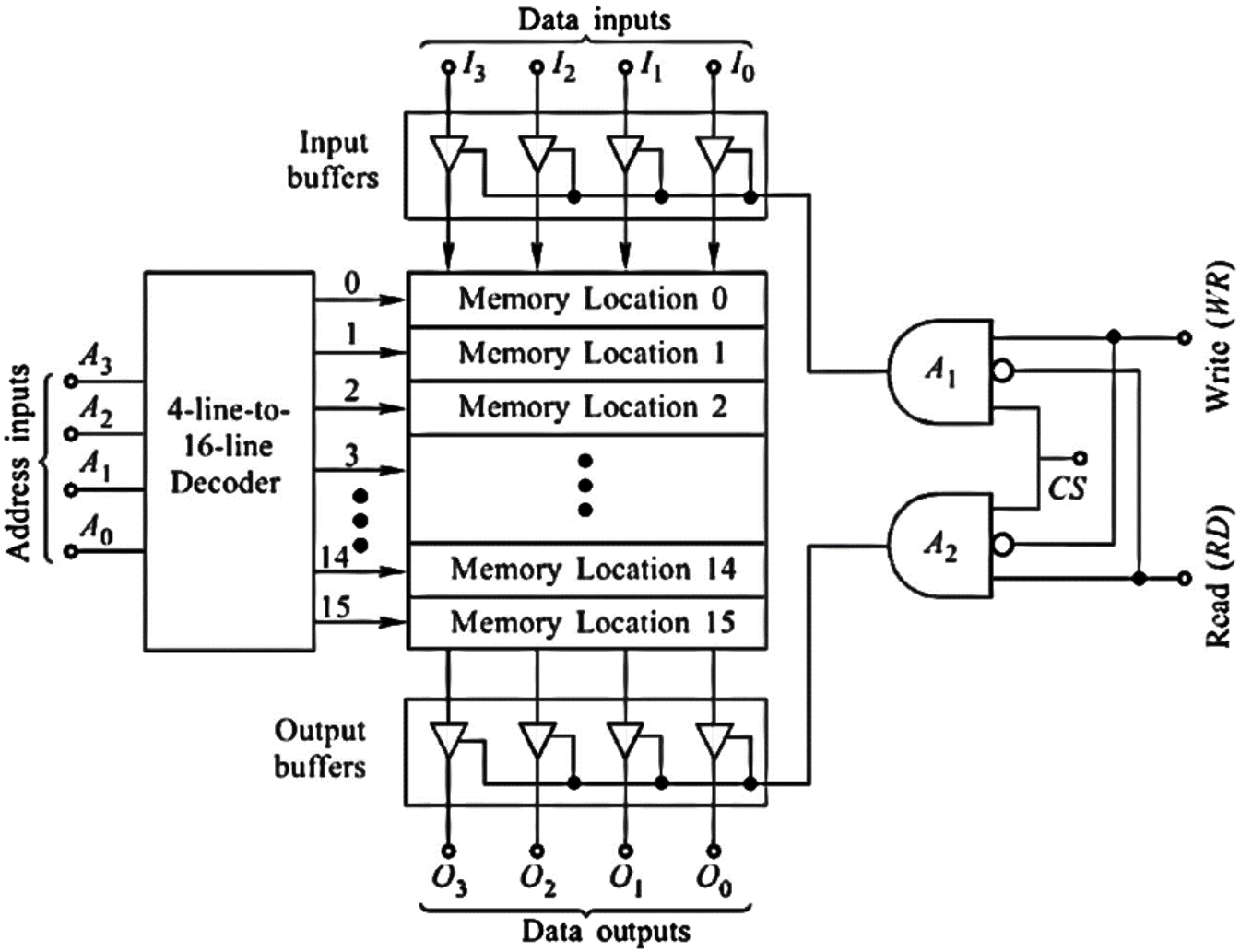
A. M=16 = 2^4. therefore, 4-bit addresses are required.



Word number	Binary Address			
	A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
14	1	1	1	0
15	1	1	1	1

Classification and characteristics of memories

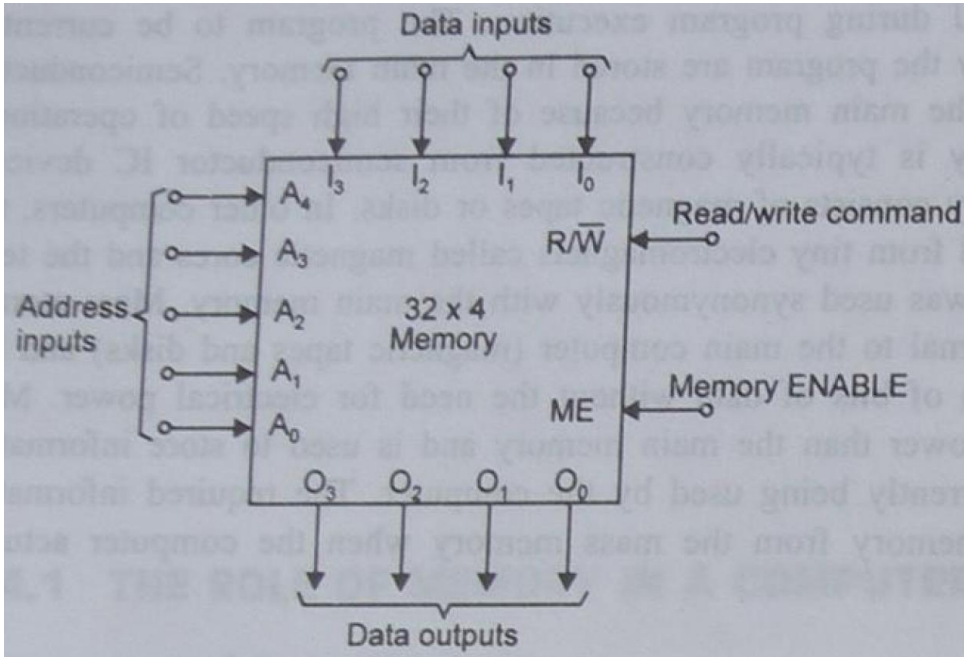
16x4 memory chip (organization)



Classification and characteristics of memories

Functions of a memory system:

1. Select the address in the memory for read/write operations.
2. Select either a read operation or a write operation.
3. Supply the input data to be stored during the write operation.
4. Hold the output data coming from memory during a read operation.
5. Enable or Disable the memory.

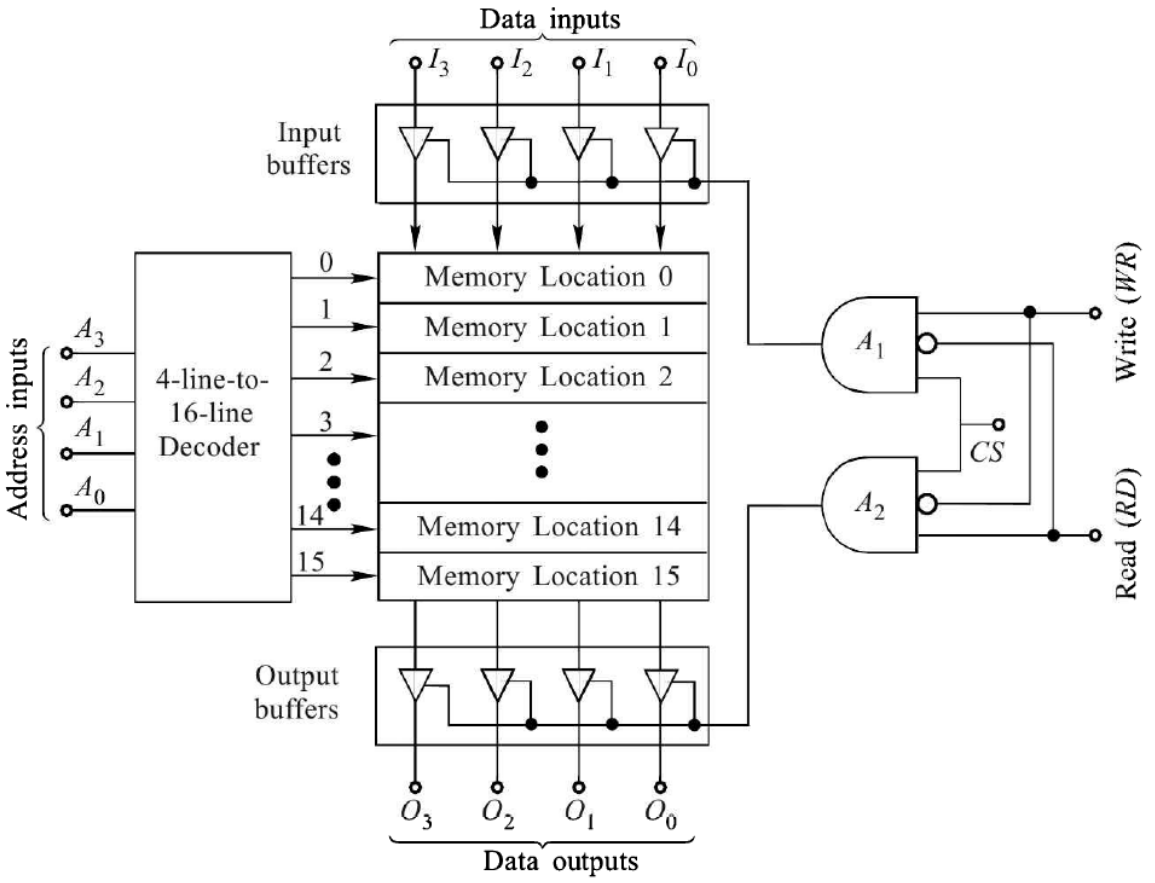


Classification and characteristics of memories

Read operation:

1. The chip-select signal is applied to the CS terminal.
2. The address of the desired memory location is applied to the address input terminals.
3. A read command signal is applied to the read-control input terminal.
4. The required data appears on the data-output terminals.

Read (RD) and Chip select (CS) signals must be high (1), and Write (WR) must be low (0).

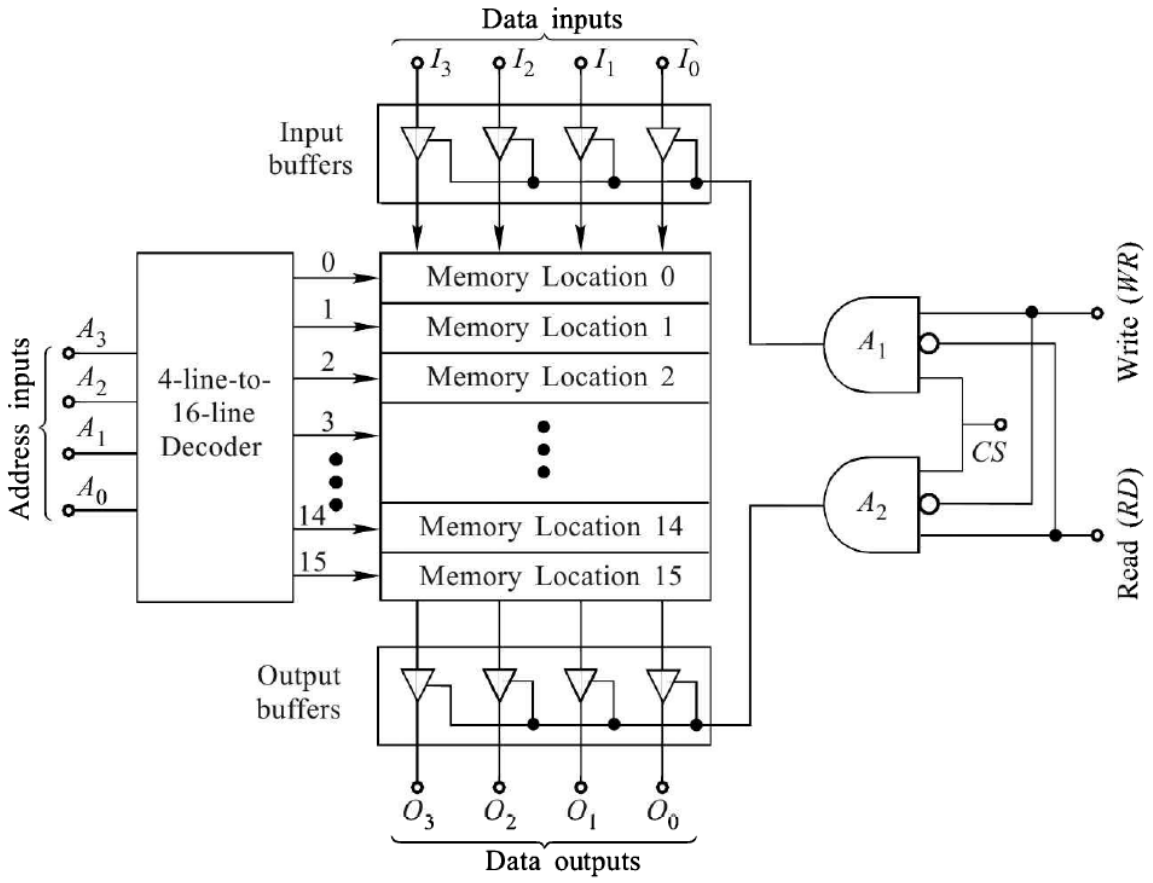


Classification and characteristics of memories

Write operation:

1. The chip-select signal is applied to the CS terminal.
2. The word to be stored is applied to the data terminal.
3. The address of the desired memory location is applied to the address input terminals.
4. A write command signal is applied to the write-control input terminal.

Write (WR) and Chip select (CS) signals must be high (1), and Read (RD) must be low (0).



Classification and characteristics of memories

Classification of Memories:

1. **Read Only Memories (ROMs):** Used to read the stored (fixed) information, such as function tables, fixed data, and instructions. Information is entered outside the system where it is to be read. Every memory location in ROM requires equal time in reading the already stored data.
   - **I. Read-only Memory (ROM)** is programmed at the time of manufacturing (custom programmed). The data stored can't be changed later. It is a costly process, so these are manufactured in large quantities. The chip can be fabricated with Bipolar or MOS Technology
   - **II. Programmable ROM (PROM):** Programmed by a user in a special device – PROM programmer. A PROM can be programmed only once. Suitable for data which is permanent in nature. The PROM chip is available without any data stored from vendor. The chip can be fabricated only with MOS Technology.
   - **III. Erasable and Programmable ROM:** These are programmable ROMs. They can be programmed again and again. When UV radiation is used to erase the data of ROM – erasable programmable ROM (EPROM), and when electrical voltage is used for erasure- electrically erasable and programmable ROM (EEPROM). The chip can be fabricated only with MOS Technology.

Classification and characteristics of memories

Classification of Memories:

2. **Random Access Memories (RWM or RAM).** Also called read-and write memory. Any memory location in RAM requires equal time for reading and writing operations.

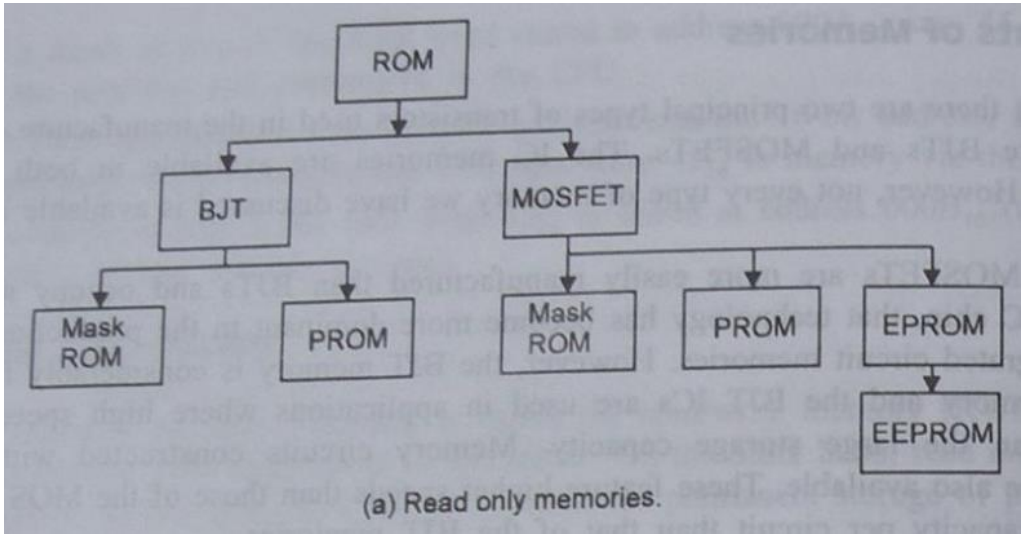
   I. **Can be Static or Dynamic –** Fabricated using unipolar (MOS RAMs are static/dynamic) or bipolar technologies (only static). Bipolar RAMs are faster than MOS RAMs.

   - **Static RAM (SRAM)** uses a bistable latch as a storage element.
   - **Dynamic RAM (DRAM)** uses a capacitor as a storage element (requires periodic refreshing)

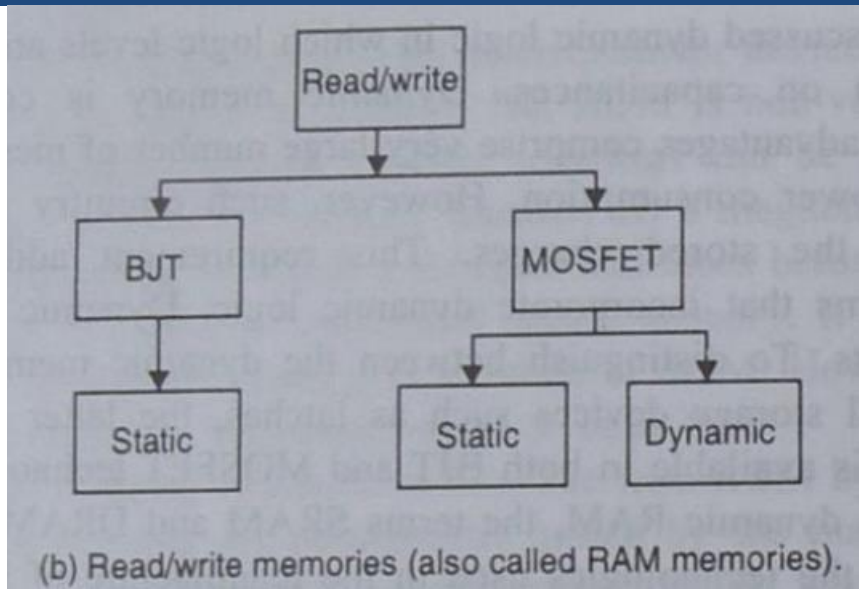
   SRAMs are faster than DRAMs but can store less data for a given size of memory. SRAMs can be fabricated using bipolar devices or MOSFETs, whereas DRAMs can be made only with MOSFETs.

   SRAMs can be Synchronous or Asynchronous (with the system clock). Synchronous RAM can have the ***burst*** feature (read or write upto 4 locations using a single address).

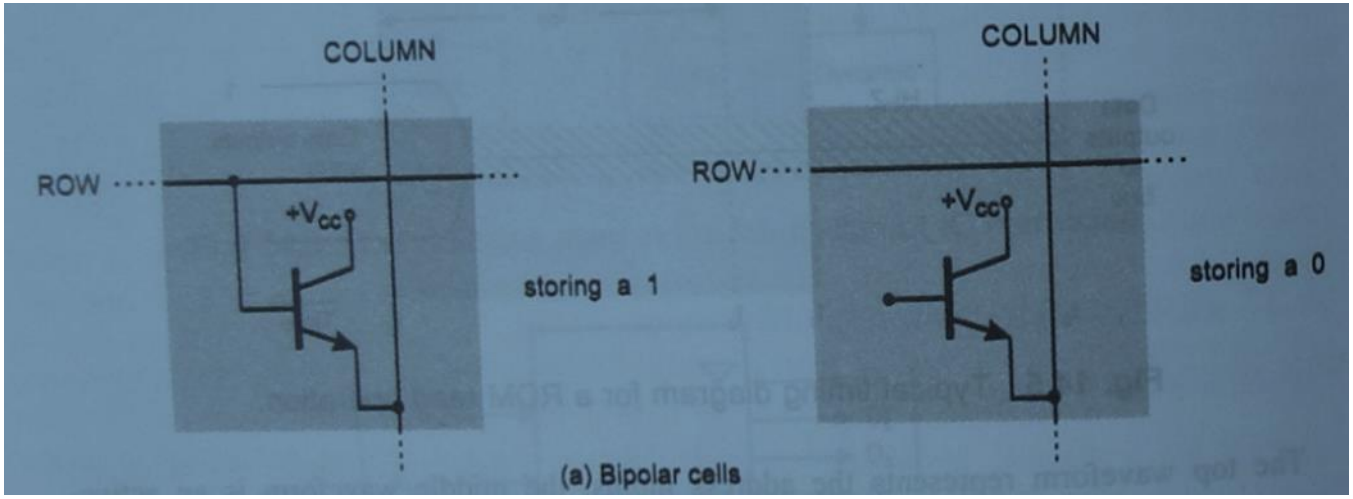
Classification and characteristics of memories



(a) Read only memories.



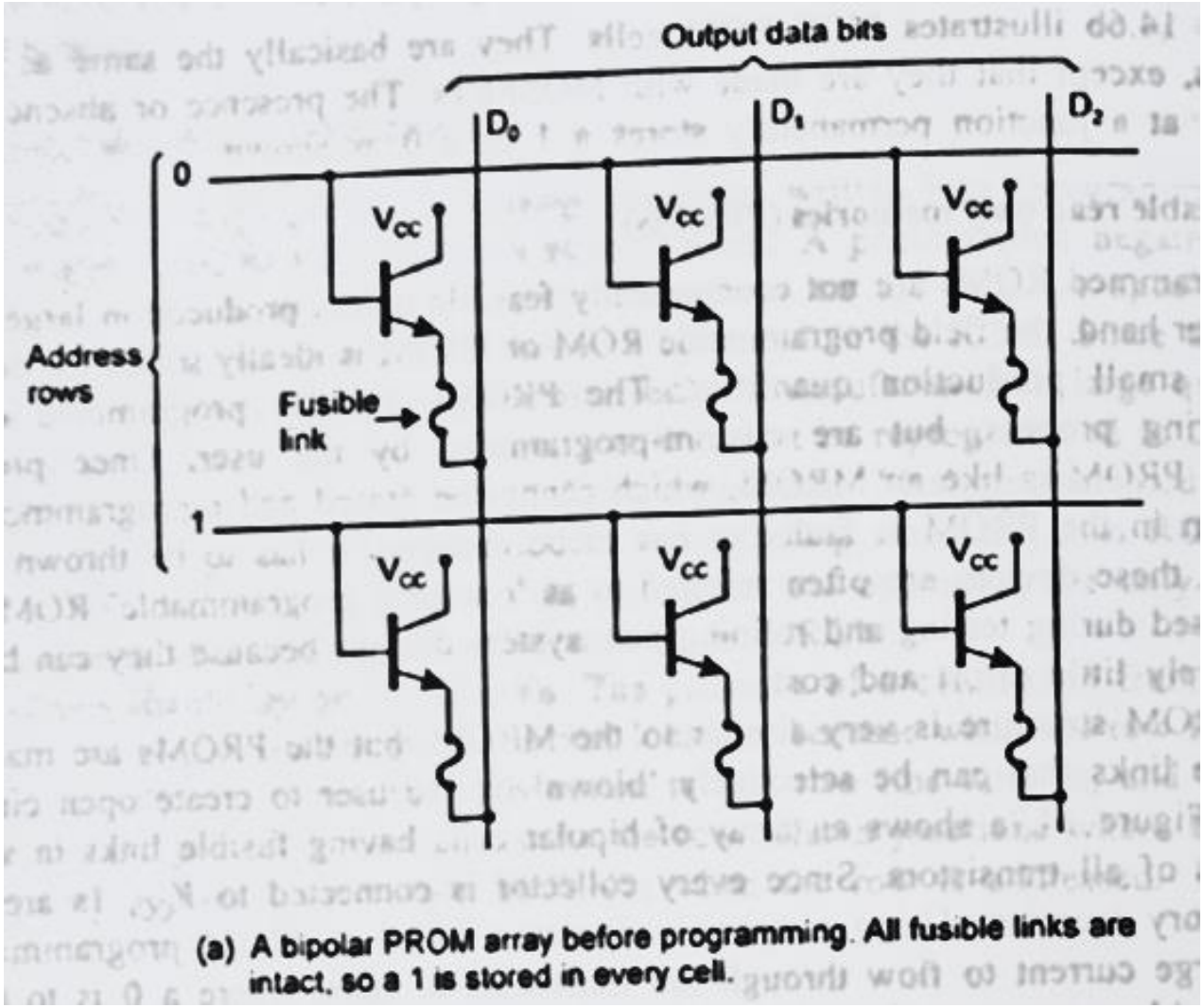
(b) Read/write memories (also called RAM memories).



(a) Bipolar cells

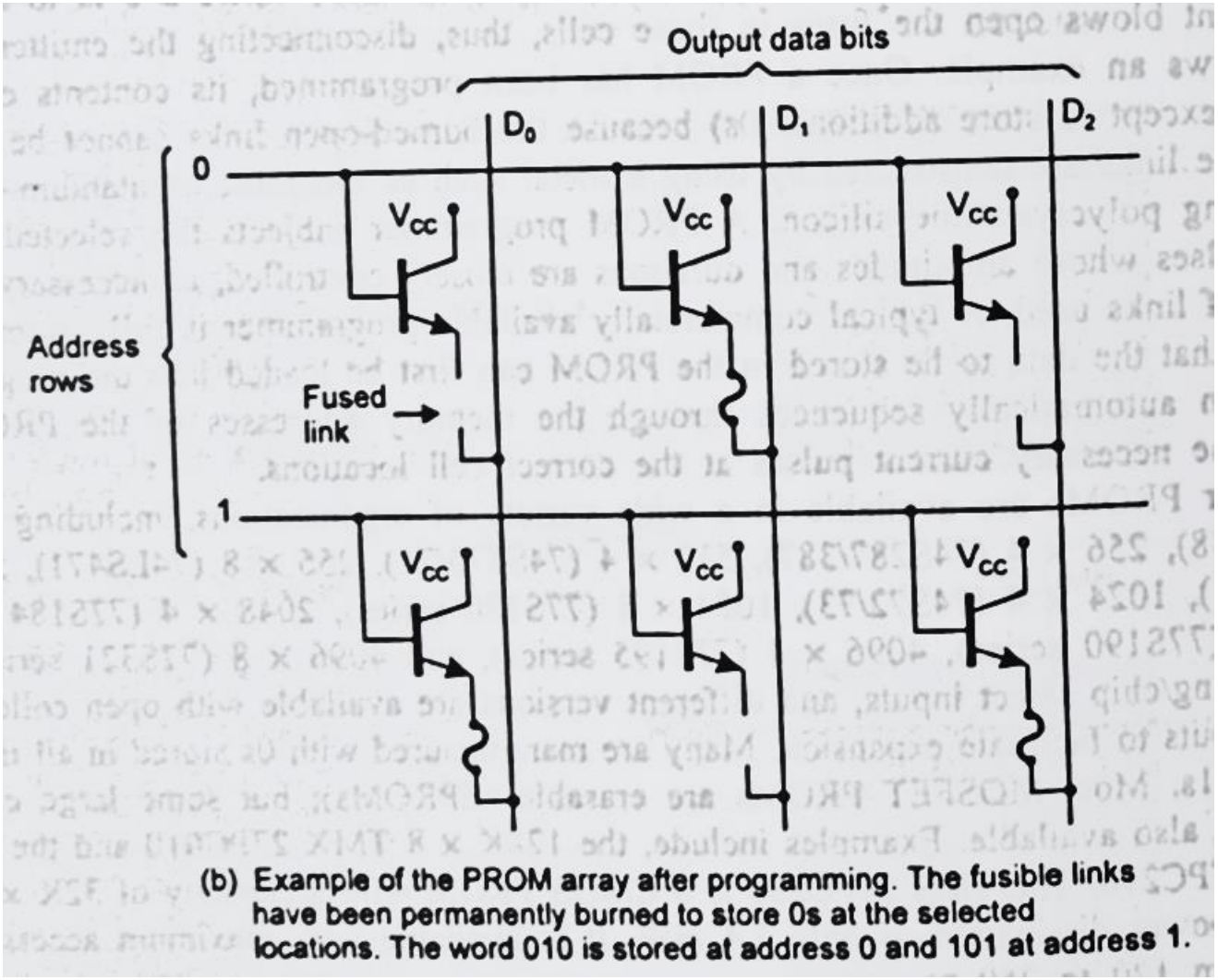
Bipolar ROM Cell

Classification and characteristics of memories



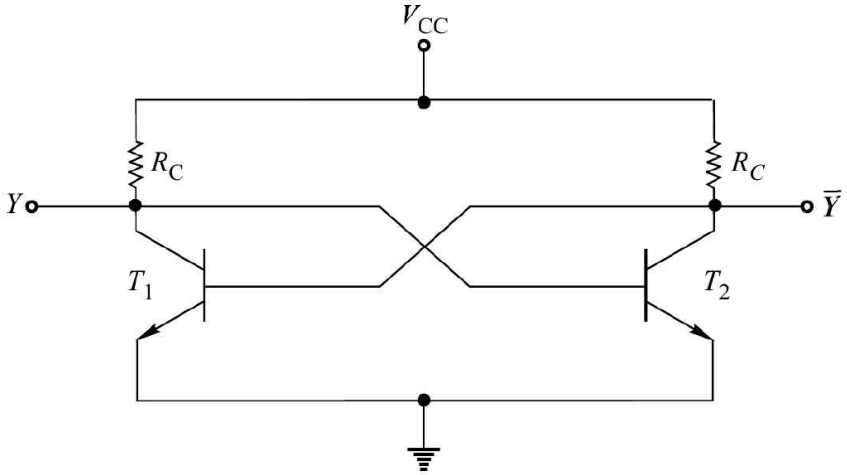
(a) A bipolar PROM array before programming. All fusible links are intact, so a 1 is stored in every cell.

Classification and characteristics of memories



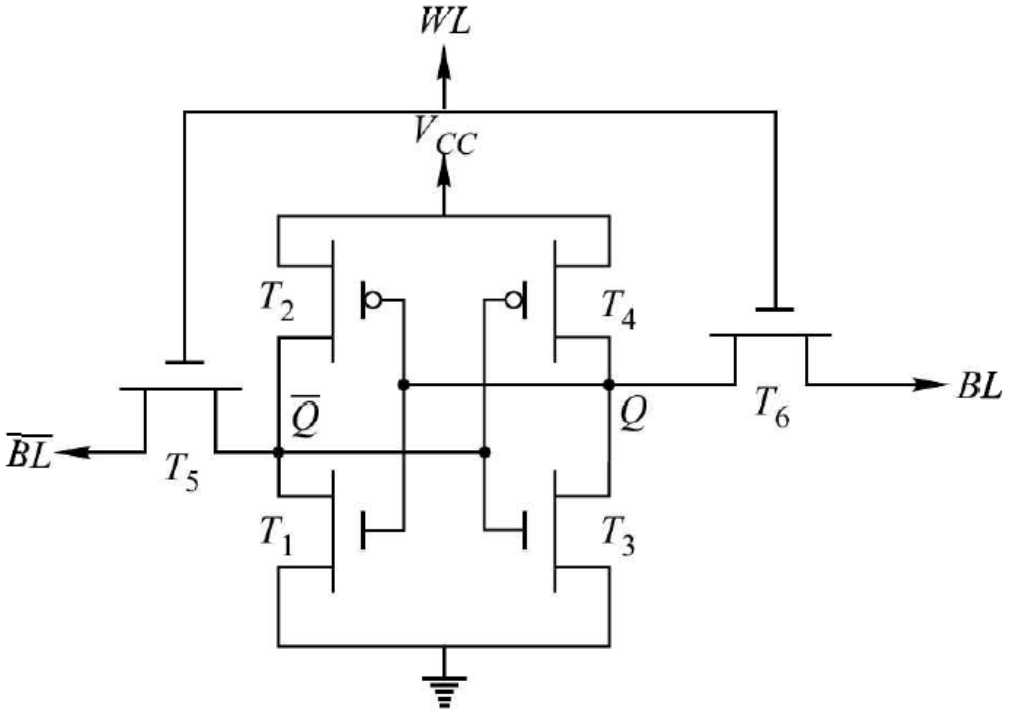
(b) Example of the PROM array after programming. The fusible links have been permanently burned to store 0s at the selected locations. The word 010 is stored at address 0 and 101 at address 1.

Classification and characteristics of memories



Bipolar RAM storage cell

Additional requirements of cell Addressing, and reading and writing onto the cell can be understood from pg. 486-487, sec. 11.6 of the book by R. P. Jain (Modern Digital Electronics), 4th Ed. , TMH.

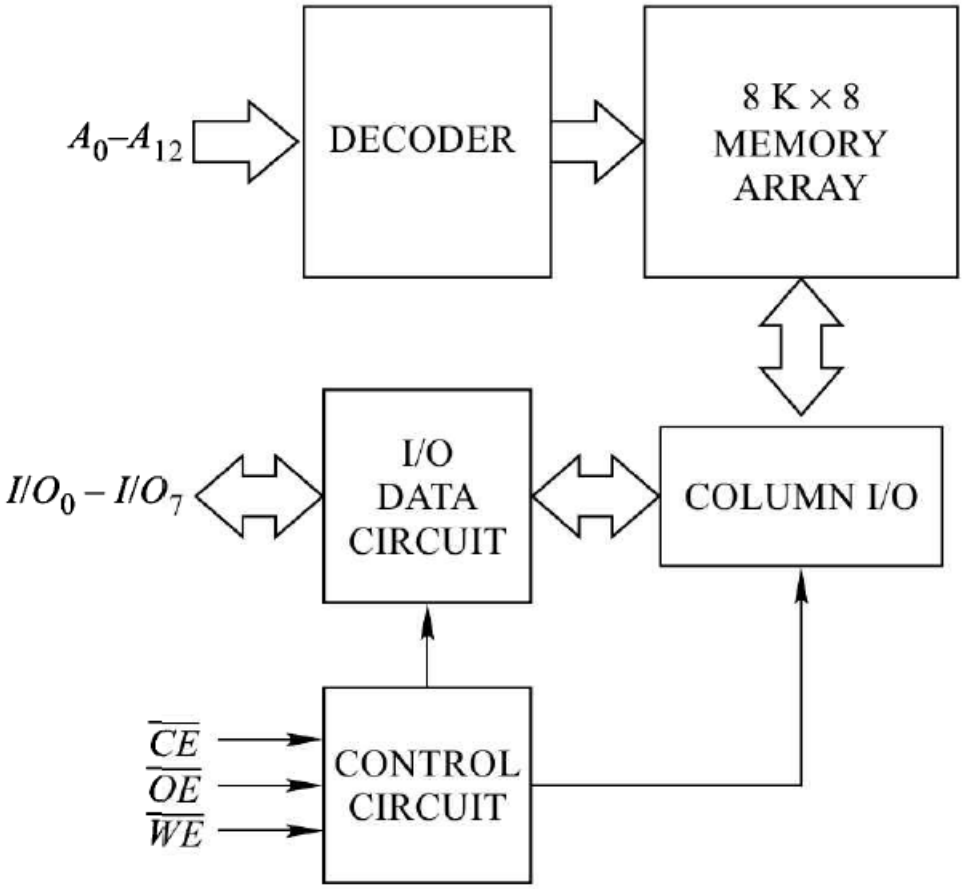


CMOS SRAM storage cell

Bit line (BL): Used to store data during a write operation and to read the stored data during a read operation.

Word line (WL): activates cells based on the address input both while reading and writing

Classification and characteristics of memories



Block diagram of Asynchronous SRAM

Single decoder circuit

3 control inputs: $\overline{CE}, \overline{OE}, \overline{WE}$

CE : Chip Enable
OE : Output Enable
WE : Write Enable

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	**I/O operation**
Not selected	X	H	X	High -Z
Output disabled	H	L	H	High- Z
Read	H	L	L	D_{out}
Write	L	L	X	D_{in}

Classification and characteristics of memories

SRAM	DRAM
It can store data as long as electricity is available.	It saves data for as long as the power is on or for a few moments if the power is turned off.
Because capacitors aren't utilized, there's no need to refresh.	The contents of the capacitor must be updated on a regular basis in order to store information for a longer amount of time.
SRAM has a storage capacity of 1 MB to 16 MB in most cases.	DRAM, which is often found in tablets and smartphones, has a capacity of 1 GB to 2 GB.
The storage capacity of SRAM is low.	The storage capacity of DRAM is higher than SRAM.
SRAM is more expensive than DRAM.	DRAM is less expensive than SRAM.
It is comparatively faster.	It is comparatively slower.
The power consumption is minimal, and the access speed is quick.	The cost of production is low, and the memory capacity is higher.
SRAM is used in cache memories.	DRAM is used in main memories.

Types of SRAM:

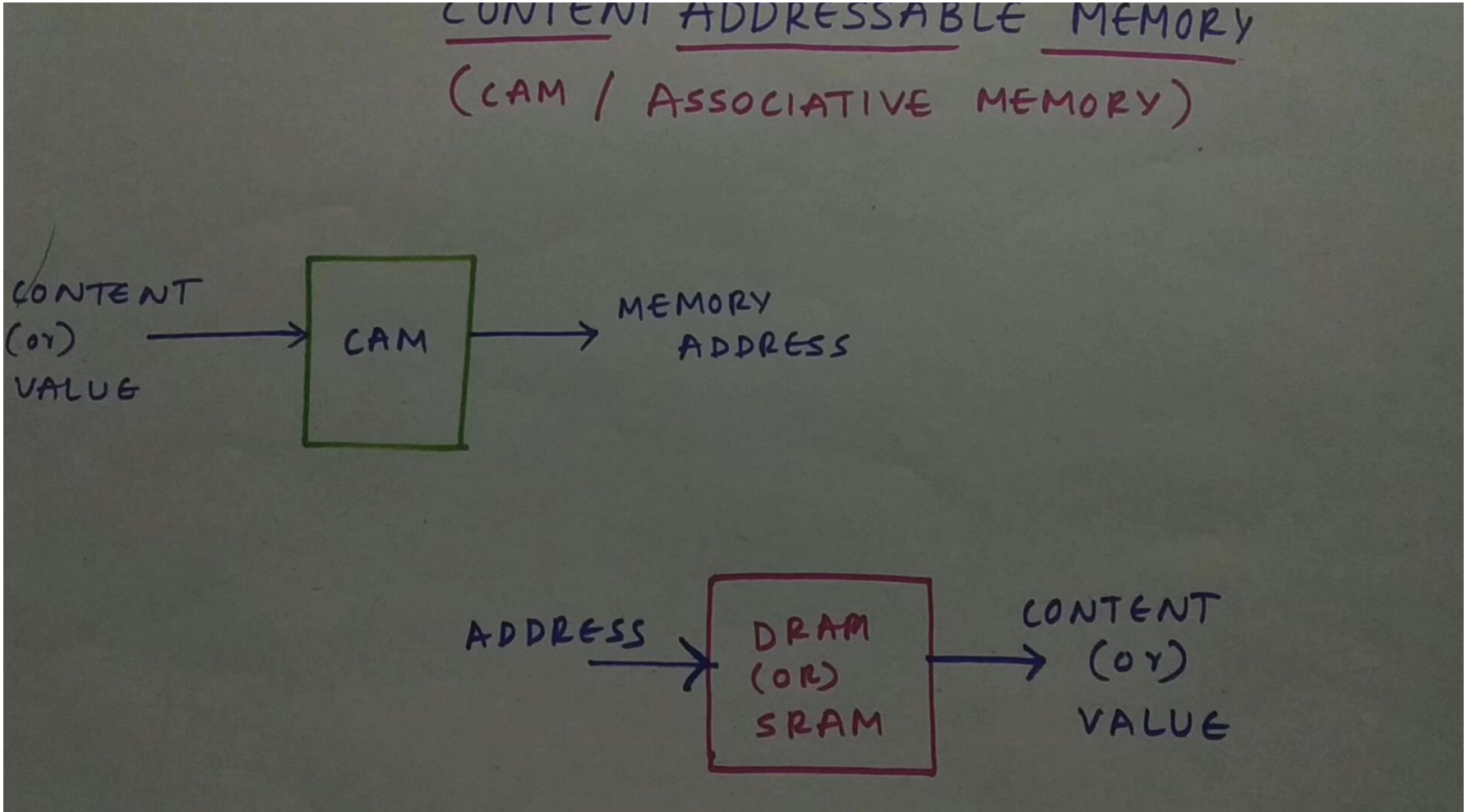
- **Bipolar SRAM**
- **MOSFET SRAM**

Types of DRAM:

- **Fast page mode DRAM (FPM DRAM)**
- **Extended data out DRAM (EDO DRAM)**
- **Burst EDO DRAM (BEDO DRAM)**
- **Synchronous DRAM**

Classification and characteristics of memories

Content Addressable Memory (CAM):



Classification and characteristics of memories

A **programmable logic device (PLD)** is an electronic component used to build reconfigurable digital circuits.

- Unlike digital logic constructed using discrete logic gates with fixed functions, a PLD has an undefined function at the time of manufacture.
- Before the PLD can be used in a circuit it must be programmed to implement the desired function.
- They contain an array of AND gates and another array of OR gates.
- Programming a PLD changes the connections made between the gates in the device.
- There are three kinds of PLDs based on the type of arrays which has programmable feature.

1. Programmable Read Only Memory
2. Programmable Array Logic (PAL)
3. Programmable Logic Array (PLA)

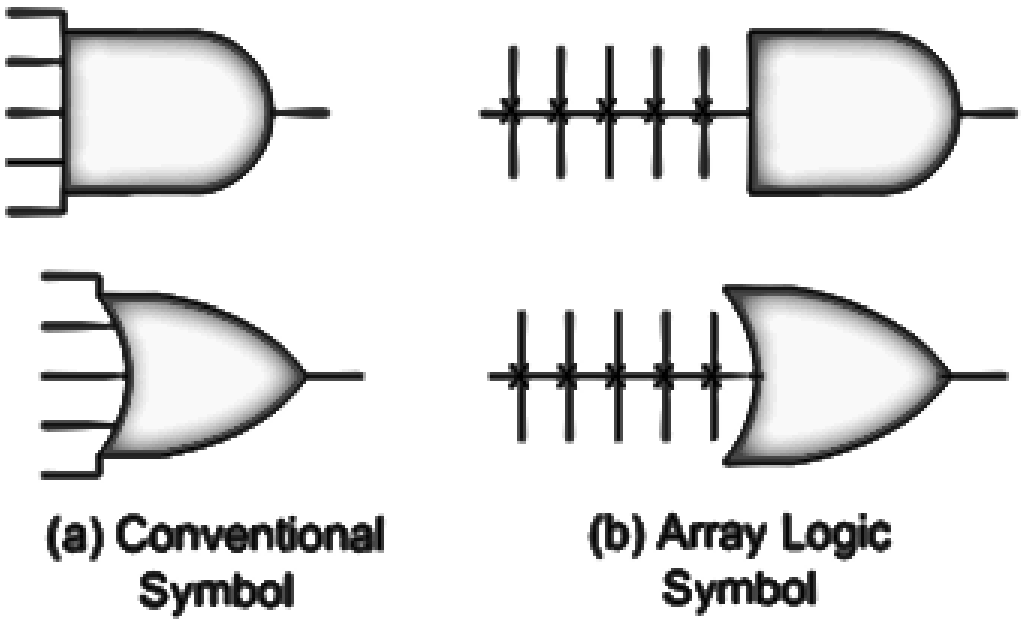
Classification and characteristics of memories

Programmable Read Only Memory (PROM) :

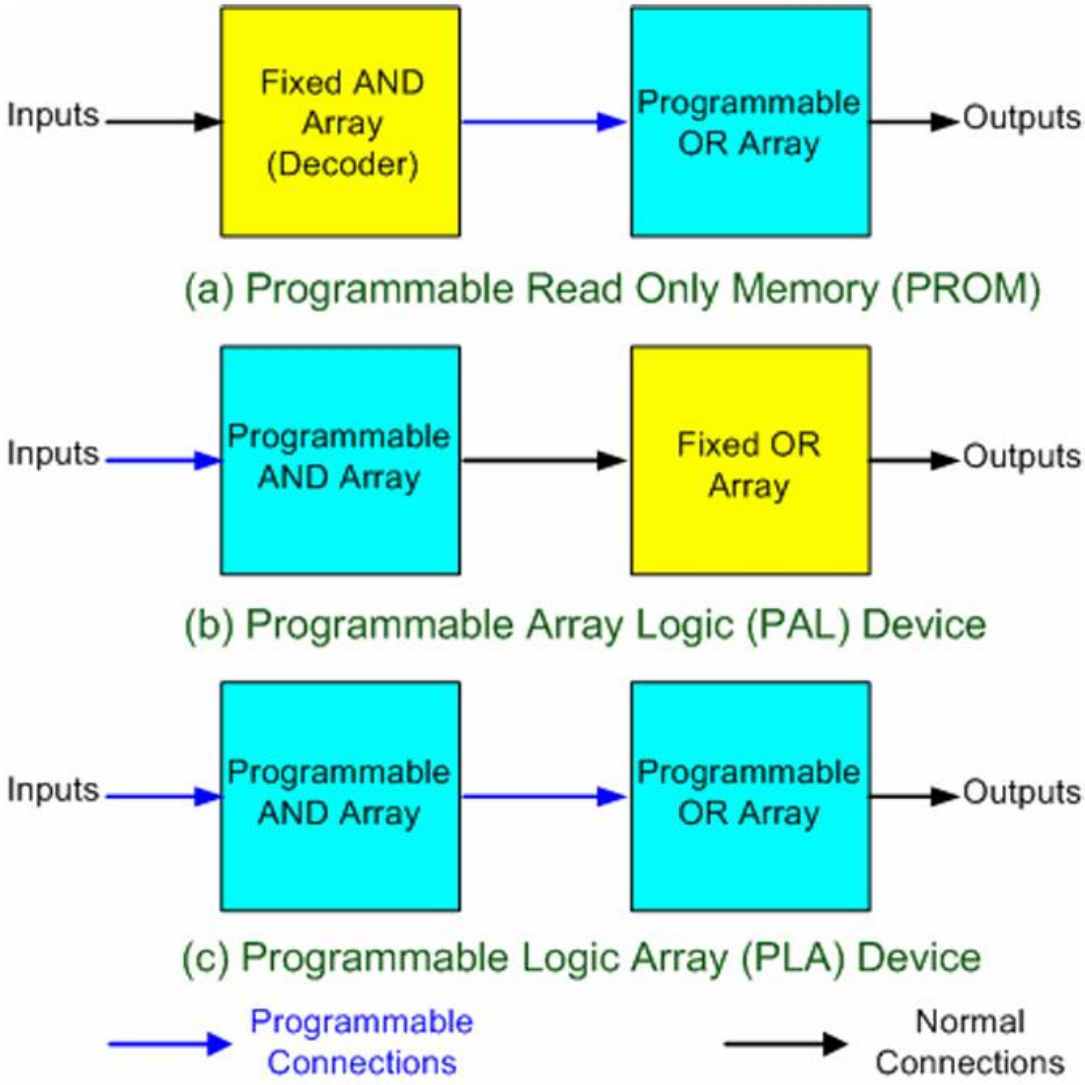
- The key difference from a standard ROM is that the data is written into a ROM during manufacture, while with a PROM the data is programmed into them after manufacture.
- Thus, ROMs tend to be used only for large production runs with well-verified data.
- PROMs may be used where the volume required does not make a factory-programmed ROM economical, or during the development of a system that may ultimately be converted to ROMs in a mass-produced version.
- PROMs are manufactured blank and, depending on the technology, can be programmed at the wafer, final test, or in the system.
- Blank PROM chips are programmed by plugging them into a device called a *PROM programmer*.
- These types of memories are frequently used in microcontrollers, video game consoles, mobile phones, radio-frequency identification (RFID) tags, implantable medical devices, high-definition multimedia interfaces (HDMI), and in many other consumer and automotive electronics products.

Classification and characteristics of memories

Programmable Logic Array (PLA) and Programmable Array Logic (PAL):



Classification and characteristics of memories

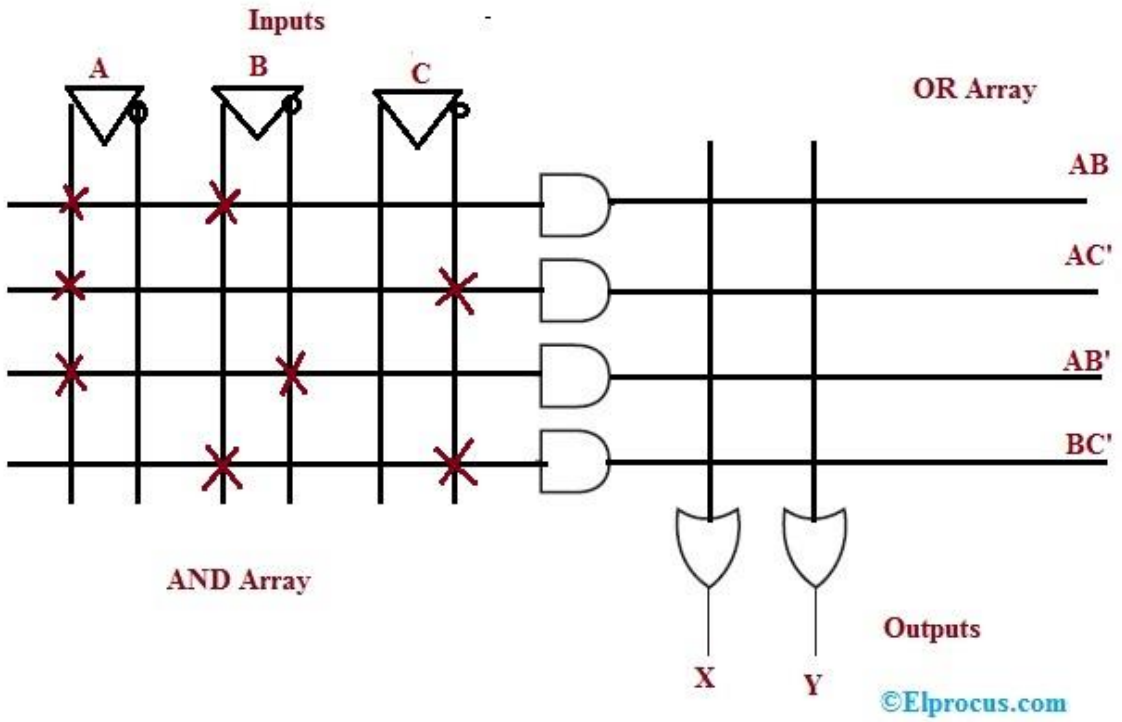


Classification and characteristics of memories

Implement the following **Boolean expression** with the help of **programmable array logic (PAL):**

$$X = AB + A\bar{C}$$
$$Y = A\bar{B} + B\bar{C}$$

The total required logic gates for generating the above two equations is AND gates-4, OR programmable gates-2.



Classification and characteristics of memories

Programmable Array Logic (PAL)	**Programmable Logic Array (PLA)**
The full form of PAL is programmable array logic	The full form of the PLA is a programmable logic array
The construction of PAL can be done using the programmable collection of AND & OR gates	The construction of PLA can be done using the programmable collection of AND & fixed collection of OR gates.
The availability of PAL is less prolific	The availability of PLA is more
The flexibility of PAL programming is more	The flexibility of PLA is less
PAL is expensive	PLA is not so costly (middle range)
The number of functions implemented in PAL is large	The number of functions implemented in PLA is limited
The speed of PAL is slow	The speed of PLA is high

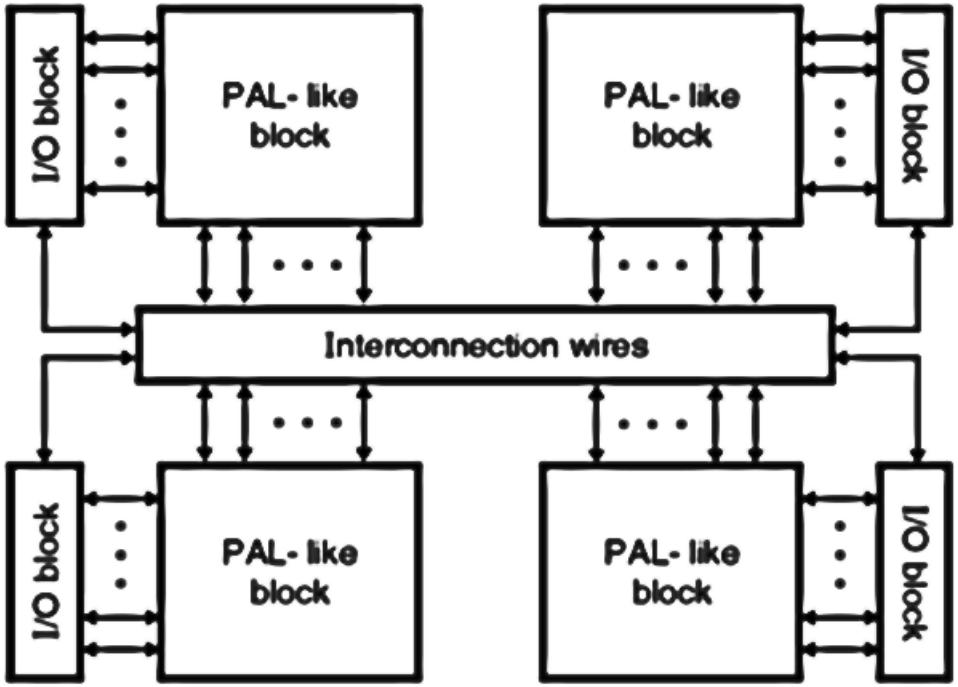
Classification and characteristics of memories

CPLD:

- CPLD stands for Complex Programmable Logic Device.
- CPLDs are programmable logic devices that are more complex than PALs but less complex than FPGAs.
- CPLDs are a combination of a fully programmable AND/OR array and a bank of macrocells.
- CPLDs are often used as address decoders and custom state machines in digital systems.
- They are ideal for use in portable and handheld digital devices because of their small size and low power consumption.
- CPLDs are based on EPROM or EEPROM technology and can be programmed using VHDL.

Classification and characteristics of memories

CPLD:



Altera-FLASH-logic-CPLDs

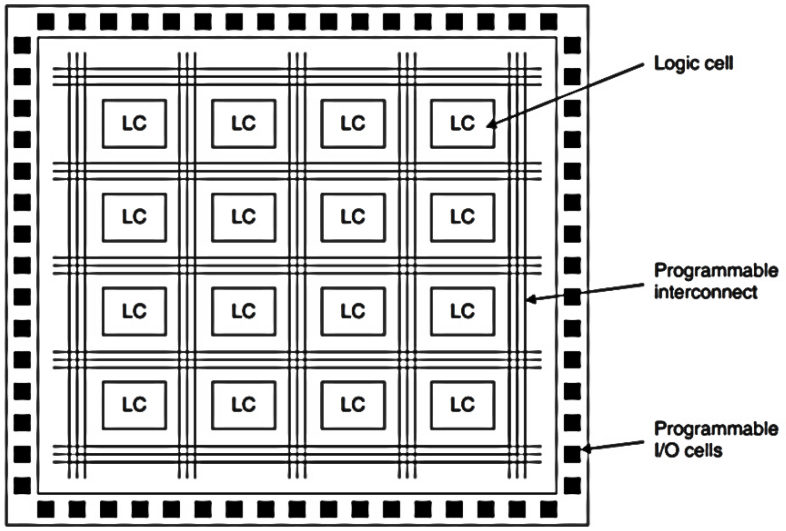
Classification and characteristics of memories

Field Programmable Gate Array (FPGA):

Field Programmable Gate Arrays (FPGAs) are digital ICs that enable the hardware design engineer to program a customized Digital Logic as per his/her requirements.

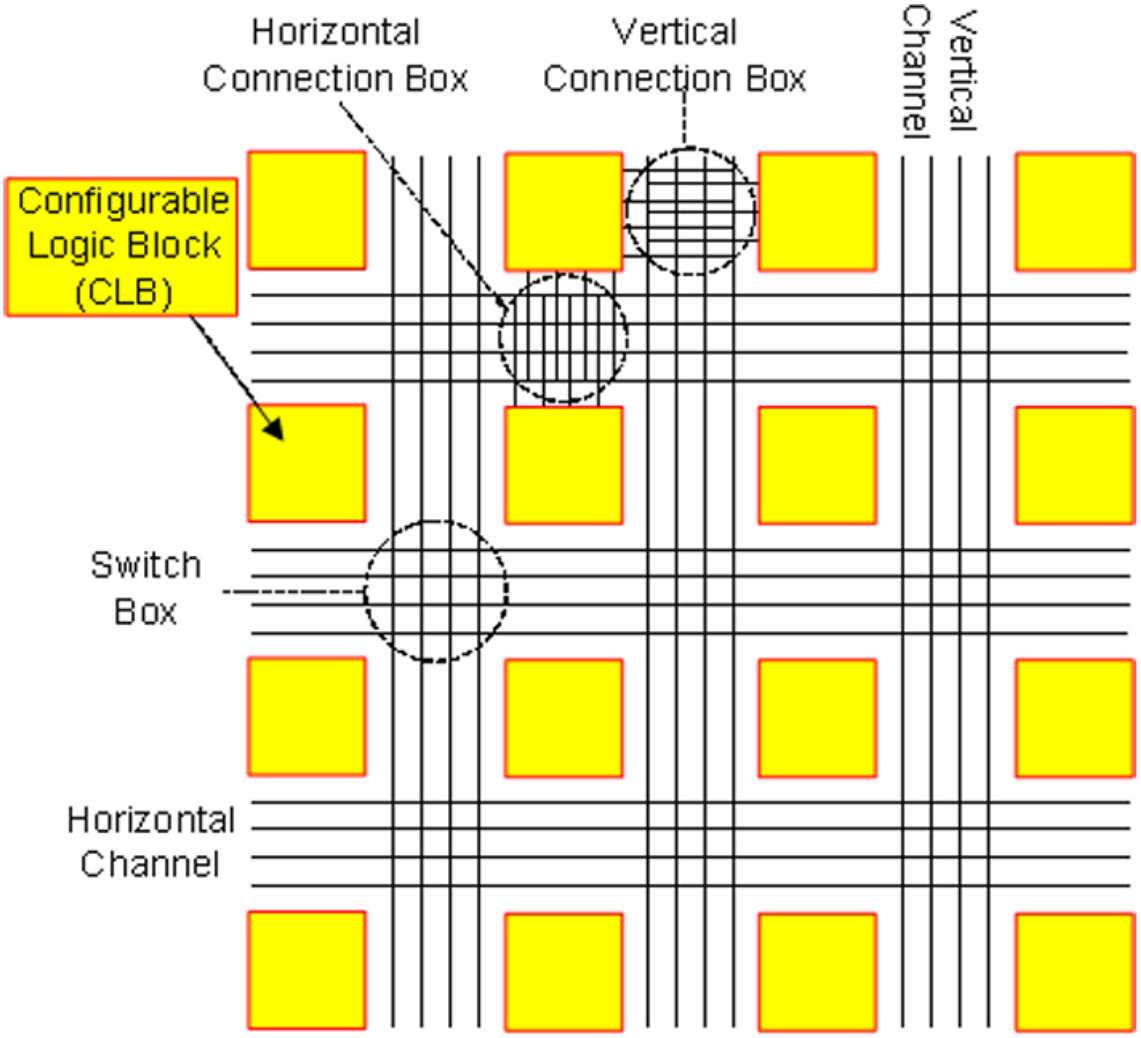
The term “Field Programmable” implies that the Digital Logic of the IC is not fixed during its manufacturing (or fabrication), but rather it is programmed by the end-user (designer).

The architecture of an FPGA is completely different from CPLDs as it consists of programmable Logic Cells, programmable interconnects and programmable IO blocks.



The programmable Logic Cells can be configured to perform any digital function and the programmable interconnects (or switches) provide the connections among different logic cells.

Classification and characteristics of memories



Classification and characteristics of memories

Components of an FPGA:

an FPGA consists of three basic components. They are:

1. Programmable Logic Cells (or Logic Blocks) – responsible for implementing the core logic functions.
2. Programmable Routing – responsible for connecting the Logic Blocks.
3. IO Blocks – which are connected to the Logic Blocks through the routing and help to make external connections.

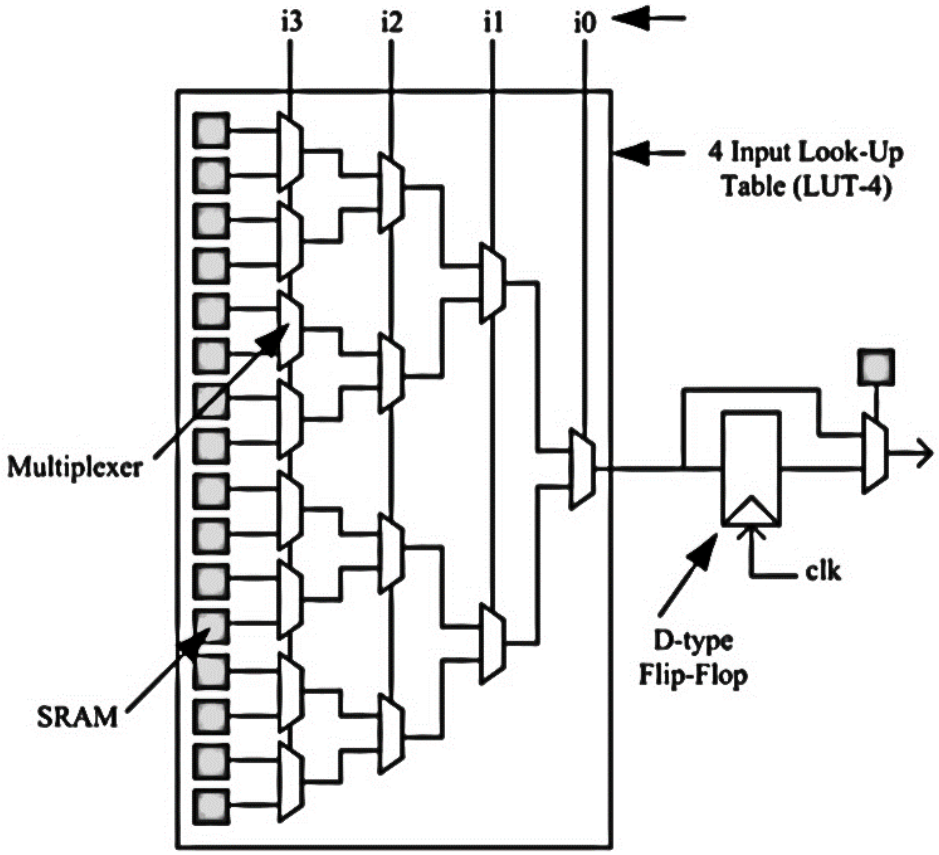
- The Logic Block in FPGAs are called as Configurable Logic Blocks (CLB) or Logic Array Blocks (LAB).
- A CLB/LAB is the basic component of an FPGA, which provides both the logic and storage functionalities.
- The basic logic block can be anything like a transistor, a NAND gate, Multiplexors, Look-up Table (LUT), a PAL like structure, or even a processor.
- Xilinx and Altera use Look-up Table (LUT) based logic blocks to implement the logic as well as the storage functionalities.

Classification and characteristics of memories

Logic block:

A Logic Block can be made up of a single Basic Logic Element or a set of interconnected Basic Logic Elements, where a Basic Logic Element is a combination of a Look-up table (which is in turn made up of SRAM and Multiplexors) and a Flip-flop.

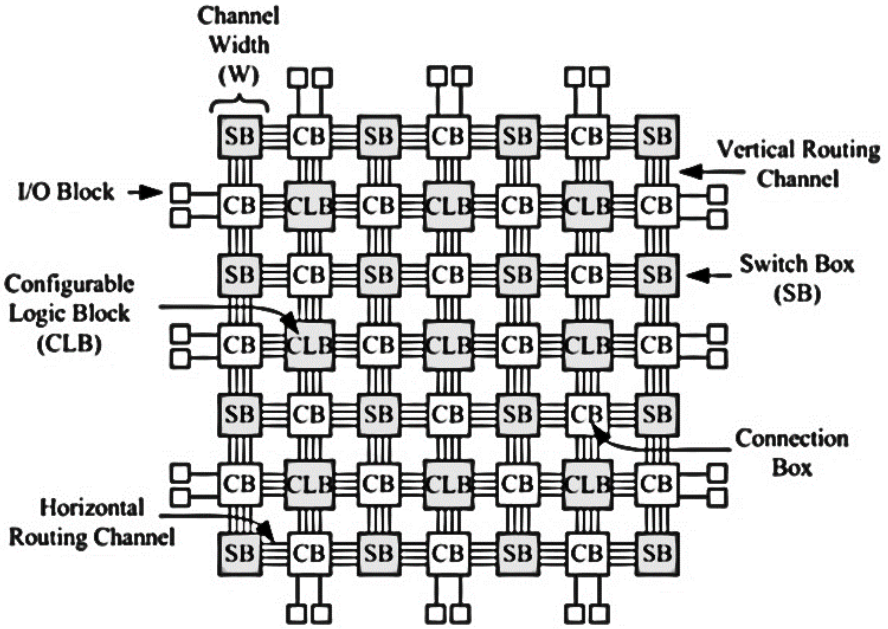
A LUT with 'n' inputs consists of 2^n configuration bits, which are implemented by SRAM Cells. Using these 2^n SRAM Bits, the LUT can be configured to implement any logical function.



Classification and characteristics of memories

Routing:

- If the computational functionality is provided by the Logic Blocks, then the programmable routing network is responsible for interconnection of these logic blocks.
- The Routing Network provides interconnections between one logic block to another, as well as between the logic block and the I/O Block to completely implement a custom circuit.
- Basically, the routing network consists of connecting wires with programmable switches, which can be configured using any of the programming technologies



Island style routing architecture

Classification and characteristics of memories

FPGA Programming technologies:

The following are three of the well-known programming technologies used in FPGAs.

1. SRAM
2. EEPROM / Flash
3. Anti-Fuse

Other technologies include EPROM and Fusible Link but they are used in CPLDs and other PLDs but not in FPGAs.

Classification and characteristics of memories

Features	CPLD	FPGA
Full Forms	CPLD is an abbreviation for Complex Programmable Logic Devices.	FPGA is an abbreviation for Field Programmable Gate Arrays.
Ratio of flip-flops	It has a low flip-flop ratio than FPGA.	It has a high flip-flop ratio than CPLD.
Density	It has a low to medium density.	It has a medium to high density.
Structure resembles	It is equivalent to the PAL.	It is similar to a Gate array.
Logic Blocks	It may only store a few thousand logic blocks.	It may include up to 100,000 small logic blocks.
Power Consumption	It has a larger power usage.	It has lower power consumption.
Based on	It is based on EEPROM.	It is based on RAM.
Cost	It is less expensive than FPGA.	It is more expensive than CPLD.
Applications	It is better suited for simpler apps.	It is appropriate for complicated apps.
Security	It provides more security than FPGA.	It provides less security than CPLD.
Performance	Its performance depends on the routing.	It provides stable performance that is independent of internal routing.
Volatility	Data will not be lost if the power is turned off.	If the power is off, the data may be lost.