Seat No: _____ Enrollment No: _____

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

B.Tech, summer 2022-23 Examination

Semester: 4 **Date: 27/03/2023**
Subject Code: 203105253 **Time: 02:00 pm to 04:30 pm**
Subject Name: Computer Organization & Architecture **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 **Objective Type Questions** - (Fill in the blanks, one word answer, MCQ-not more than Five in case of MCQ) (All are compulsory) (Each of one mark) **(15)**

1. Which of the following is a type of architecture used in the computers nowadays?
   a) Microarchitecture b) Harvard Architecture
   c) Von-Neumann Architecture d) System Design
2. Which of the architecture is power efficient?
   a) RISC b) ISA c) IANA d) CISC
3. What does VLIW stands for?
   a) Very Long Instruction Width b) Very Large Instruction Word
   c) Very Long Instruction Width d) Very Long Instruction Word
4. Which of the following is the full form of CISC?
   a) Complex Instruction Sequential Compilation
   b) Complete Instruction Sequential Compilation
   c) Computer Integrated Sequential Compiler
   d) Complex Instruction Set Computer
5. What does ISO stands for?
   a) International Software Organization b) Industrial Software Organization
   c) International Standards Organization d) Industrial Standards Organization
6. To reduce the memory access time we generally make use of _____
7. The VLIW architecture follows _____ approach to achieve parallelism.
8. In CISC architecture most of the complex instructions are stored in _____
9. _____and _____ are the different type/s of generating control signals.
10. The bit used to signify that the cache location is updated is _____
11. A disk-drive can transfer data directly to and from the RAM.-true/false
12. ROM is secondary memory. True/false
13. Virtual memory is faster than RAM, because it has no physical limitation. .-true/false
14. The 4 stages in the machine-instruction-cycle are: fetch-execute-encode-store. .-true/false
15. Cache memory is usually considerably smaller than RAM. .-true/false

Q.2 Answer the following questions. (Attempt any three) **(15)**

A) Explain the following terms: a)SPA b)SNA c)SZA d)SZE
B) Explain different types of Interrupts
C) Write a note on subroutines.
D) Explain the characteristics of RISC and CISC

Q.3 A) Explain Instruction cycle **(07)**
B) Explain 4 bit incrementer with a necessary diagram **(08)**

OR

B) Explain four types of instruction formats **(08)**

Q.4 A) List and explain different types of shift microoperation. **(07)**

OR

A) Explain all memory reference instruction in detail. **(07)**
B) Describe the significance of parallel processing with example **(08)**

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FACULTY OF ENGINEERING & TECHNOLOGY

B.Tech./Int. Btech Summer 2022 - 23 Examination

Semester: 4/3/8 **Date: 27/03/2023**
Subject Code: 203124209 **Time: 02:00 pm to 04:30 pm**
Subject Name: Computer Organization and Microprocessor Architecture **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
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4. Start new question on new page.

Q.1 **Objective Type Questions** - (Fill in the blanks, one word answer, MCQ-not more than Five in case of MCQ) (All are compulsory) (Each of one mark) **(15)**

1. What is the size of data bus in 8085 microprocessor?
2. How many bits are not used in flag register?
3. What is machine cycle?
4. What is an Assembler?
5. The operation code of ADD is 10000000. Find the Hex code instruction ADD B.
6. Calculate the number of chips required to design 8K-byte memory if the memory chip size is 1024 x 1.
7. Explain OUT instruction.
8. What is partial decoding of I/O devices?
9. Assume the accumulator holds FFH. Illustrate the difference in flag set by adding 01H and by incrementing the accumulator contents.
10. Explain DCX instruction.
11. What is a counter?
12. Explain RRC instruction.
13. Which instruction is used to mask RST 7.5, 6.5, and 5.5 interrupts?
14. What is a micro-operation?
15. Describe the control function with example in register transfer language.

Q.2 **Answer the following questions. (Attempt any three)** **(15)**

A) Explain the flag register in detail.
B) Differentiate between peripheral-mapped I/O and memory-mapped I/O.
C) Draw and explain accumulator bit pattern of RIM Instruction.
D) Sixteen bytes of data are stored in memory locations at 2050H to 205FH. Write instructions to transfer the entire block of data to new memory locations starting at 2070H.

Q.3 A) Draw and explain timing diagram for MVI C, CCH. **(07)**

B) Write an assembly language program to count the number of odd and even numbers from a block data having ten bytes from 2000H to 2009H. **(08)**

OR

B) Write an assembly language program to add the positive numbers from a block of data having ten signed numbers from memory location 4000H to 4009H and display sum if less than FFH , if not then display FFH. **(08)**

Q.4 A) Explain the stack in detail with role of PUSH and POP instructions. **(07)**

OR

A) Describe shift micro operations with hardware implementation. **(07)**

B) Explain different types of memory. **(08)**

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