W10 Mar 18 (D1) Implications of parallelism

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All Sections

These questions are presented under the following assumptions:

- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

N.B.: The source of this question is Patrick R. Schaumont, "**A Practical Introduction to Hardware/Software Codesign** ", Problem 1.3, p. 28.

A single-input, single-output program running on an ARM processor needs to be rewritten such that it will run on three parallel ARM processors. As shown in Fig. 1.12, each ARM has its own, independent data- and instruction memory. For this particular program, it turns out that it can be easily rewritten as a sequence of three functions fA, fB and fC which are also single-input, single output. Each of these three functions can be executed on a separate ARM processor, so that we get an arrangement as shown below. The sub-functions fA, fB, and fC contain 40, 20, and 40% respectively of the instructions of the original program. You can ignore the time needed for communication of variables (out, in, t1, and t2 are integers).

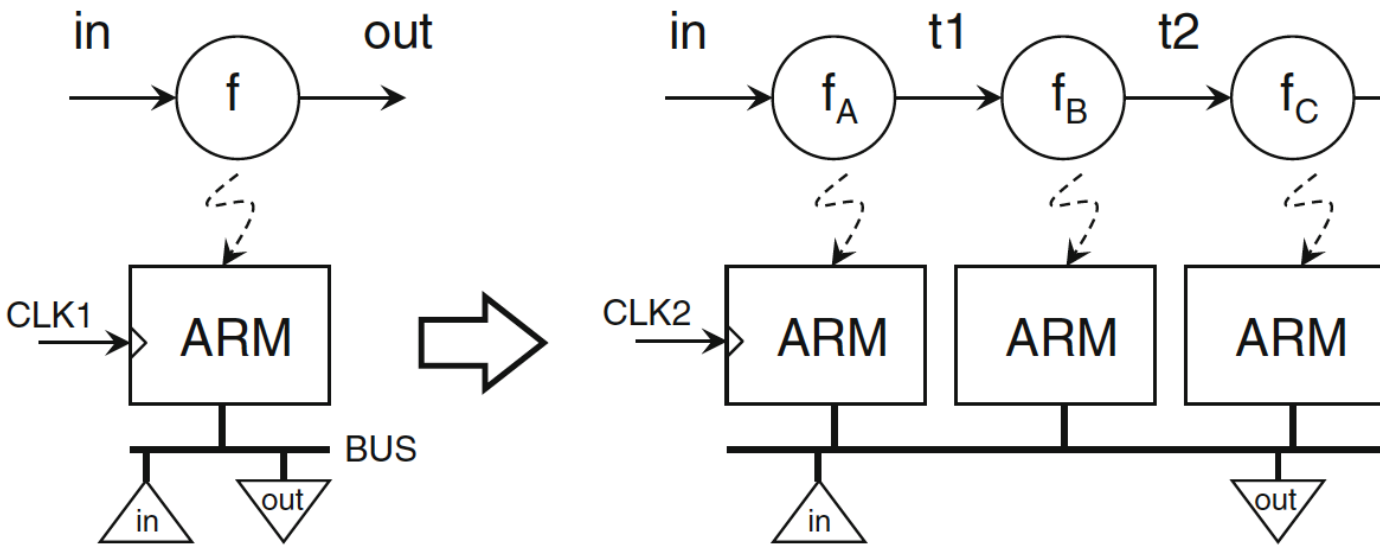

Fig. 1.12 Multiprocessor system for problem 1.3

1. Assume that all ARMs have the same clock frequency (CLK1 = CLK2). Find the maximal speedup that the parallel system offers over the single-ARM system. For example, a speedup of 2 would mean that the parallel system could process two times as much input data as the single-ARM system in the same amount of time.
2. For the parallel system of three ARM described above, we can reduce the power consumption by reducing their clock frequency CLK and their operating voltage V. Assume that both these quantities scale linearly (i.e. Reducing the Voltage V by half implies that the clock frequency must be reduced by half as well). We will scale down the voltage/clock of the parallel system such that the scaled-down parallel system has the same performance as the original, single-ARM sequential system. Find the ratio of the power consumption of the original sequential system to the power consumption of the scaled-down, parallel system (i.e. find the power-savings factor of the parallel system). You only need to consider dynamic power consumption. Recall that Dynamic Power Consumption is proportional to the square of the voltage and proportional to the clock frequency.

Reply

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The function f is split into 3 sequential function fA, fB, fC. The output of fA is fed to fB as input, output of fB is fed to fC as input. It doesn't not seem parallel architecture will speed up for this case, in terms of execution time. Which aspects have to be taken into consideration for comparison of architectures, in this case?

Reply