



ES-SCH4300

SW/HW co-development of embedded systems

Spring semester 2015

### Written examination

Please read the instructions carefully before start answering.

#### Instructions:

1. Write your Candidate number in each exam sheet.
2. The exam is worth a total of 200 points. The points allocated to each part of each question or problem are shown in brackets before the question/problem statement.
3. Answer all questions in the examination sheets.
4. You may answer questions or problems by the same order they appear or not, providing that you clearly identify which question or problem you are answering.
5. Write your answers in clear, legible handwriting, preferably using a black ballpoint or rollerball pen.
6. Almost all questions are open-ended questions designed for you to give a meaningful answer using your own knowledge.

#### Questions:

1. In recent years, programmable logic devices, like FPGAs (Field-Programmable Gate Arrays), have been replacing fixed functional logic gate devices, like ASICs (Application-Specific Integrated Circuits) in consumer electronic products.

(10) Discuss the reasons why the use of ASICs in consumer electronic products is decreasing, while there is an exponential increase in the use of FPGAs.

(10) List and justify the advantages and disadvantages

of using FPGAs over ASICs. *FPGA-ASIC design advantages*  
*external document* *+ disadvantages*

of using FPGAs over

Using a generic model, describe the main components of a typical FPGA internal architecture.

## HBV

Note: you may draw a generic FPGA model to support your description of the different FPGA architecture elements and of their individual functionality.

*Architecture Lecture slide 31+32*

*② Lsdgo external document → chapter 2 pg 7,8; FPGA AUG*



2. One of the main disadvantages of FPGAs is the long and unpredictable propagation times caused by their interconnection architecture.

(10) a. Discuss this limitation, its causes and how it can affect the performance of the systems configured into the FPGA. → *Architecture slide 35 + handwritten answer*

(15) b. List some of the ways manufacturers and designers use to work out this limitation, explaining how each one contributes to mitigate it.

(5) c. Explain how can the user set a desired target for the frequency of operation during the development phase.

*→ Pg 25 + Pg 26 Video quick start*

(10) Identify which changes may be introduced by the designer into the circuit to try to achieve the defined frequency, in case the design tools are unable to reach it.

1-7 1-bn&.uwj.L1 c.a.r%NM

## HBV

3. The frequencies of operation of circuits implemented inside FPGAs are always smaller than the frequencies of operation of modern microprocessor-based computers, in the order of GHz. However, due to the Von Neumann computer architecture certain algorithms run faster when implemented in an FPGA than when running in computer.

*Slide 4 (4, 11, b)*

(10) Discuss the Von Neumann computing paradigm, and its advantages and disadvantages.

- (10)b. Explain why certain algorithms may run faster when implemented in FPGAs than when running in a computer despite the much higher frequency of computers' processors. *↳ BJOw document*



4. To design an embedded system involves a number of different aspects and areas of knowledge. An embedded system needs a hardware platform, which can be fixed, configurable (like FPGAs), or hybrid (like FPGAs with hard core processors). It involves software and may even include an operating system.

(10) Explain, using your own words, what an embedded system is.

*↳ external printed document  
 ↳ 11 and 12 from "hardware Section"*

- (10) Discuss the advantages of using FPGAs to implement embedded systems instead of ASICs.

*↳ external printed document*

- 0) In FPGA-based embedded systems, two types of embedded processors are used – hardcore microprocessors, like the ARM-processor embedded in the Zynq family of FPGAs from Xilinx, and softcore

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microprocessors, like the Microblaze core, distributed as an IP (Intellectual Property) core by Xilinx. Explain the differences between these two types of microprocessors, and the advantages and disadvantages of using one or the other.

synopsys → external "3" documents  
 → 2 book → notes printed

- (20) 6. To choose between implementing a design in hardware or software is straightforward, if you only consider your design effort. Indeed, from a designer's point-of-view, the easiest approach is to write software. However, there are other arguments that must be considered when choosing to implement a design using a pure hardware or software approach, or using a approach.

? → chapter 1 in book ?  
 → the past, present, future p8/16/12  
 → extra lecture printed "hardware/software  
 → p8 20 book  
 co-design 4,5,6,7

a characteristics of System-on-Chip (SoC) architectures is a distributed and ous storage architecture, which combines several different memory hardware/software co-development one. List and explain the driving factors for choosing a co-development approach instead of a traditional hardware or software -based only design approach.

- (20) 7. One of the characteristics of heterogeneous which combines several different memory technologies. Each memory type fulfils a different role in the functionality of the SOC. List and explain the different memory types used in a SOC system and their specific role in the overall functionality of the system.



→ all external documents labeled as pull + pull down  
 + Xilinx user file

8. To be able to connect a keyboard to the USB HID Host of our Nexus-3 board, it is necessary to add a "VI-LUP" constraint to tbL12 (K\_CLK) and J13 (K\_DATA) I/O pins.

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- ) a. Explain what a pull-up is and where and how they are implemented inside the FPGA architecture.
- ) b. Explain, giving examples, when and why is it necessary to add "PULLUP" constraints to I/O pins.
- (10) c. Figure 1 shows a push-button connected to an I/O block of an FPGA. Explain how should we configure the I/O block to be able to correctly read the logic values coming from the push-button, why that configuration is necessary and how we may do that.

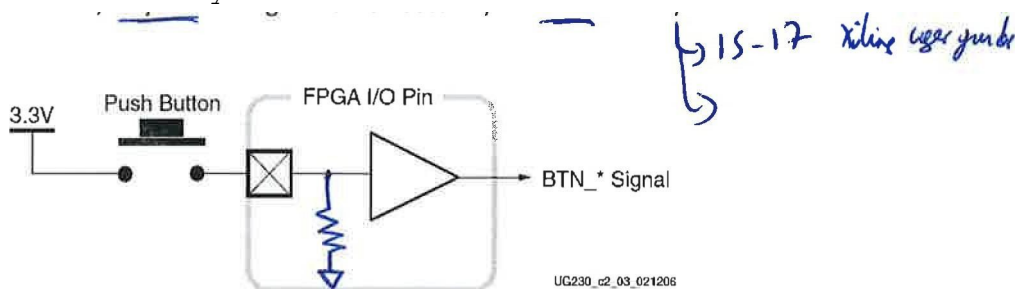


Figure 1: Push-Button Switches

(adapted from: Spartan-3E FPGA Starter Kit Board User Guide, Xilinx)

- (10) 9. One of the mandatory words in hardware/software co-development for embedded

systems using programmable logic devices is "reuse". No one develops complex systems from scratch anymore. Designers reuse previous developed modules and integrate them in new designs. Sometimes, the functionality of a given module is only partially used, leaving unconnected one or more of its input and output ports. Explain how to deal

unconnected input and output ports in

with better illustrate your answer.

VHDL. You may give one or more examples

to

The Instructor:

Manuel Gericota

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q 3 on 68

6. Almost all questions are open-ended questions designed for you to give a meaningful answer using your own knowledge.

Questions:

(10)

Describe what a Programmable Logic Device is. List and justify its advantages over fixed functional logic gate devices, like Application Specific Integrated Circuits (ASICs). → from paper in file → Architecture  
d external paper + programmable logic device 110

justify its  
advantages and  
like

## HBV

Application-Specific

2

- (20) The configurable characteristics of (programmable logic device) are determined by the programming technology used by each device. Currently, five different technologies are used by manufacturers: SRAM (Static Random Access Memory); A\_gjzsf-use-based.-technology; UV-EPROM (Ultra Violet - Erasable Programmable Read Only Memory); EEPROM (Electrically Erasable Programmable Read Only Memory); and Flash technology. Describe in detail the advantages and limitations of each technology and how it influences the programming flexibility of the device.

*Handwritten notes:*

- external paper
- Architect overview
- 1/4
- UV-EPROM
- HBV logo: HØGSKOLEN I BUSKERUD OG VESTFOLD, PROFESJONSHØGSKOLEN
- utboken Side 39 → 40
- ter 2 work is book for one user (42)
- PPO"
- (.10 o
- ③ One of the main disadvantage

One of the main disadvantages of Field Programmable Gate Arrays (FPGAs), when compared to ASICs, is the long and unpredictable propagation times caused by its interconnection architecture.

Explain why the interconnection architecture of the FPGA generates signal propagation delays higher than those generated by the interconnection architecture of ASICs, and how

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those delays affect the performance of the systems configured into it. ➔

0)b. In order to compete with ASICs, FPGA manufacturers introduced a series of new architectural features to work out this limitation, namely different types of specialized blocks and dedicated routing resources. Give examples of how the introduction of these blocks and dedicated resources contributes to mitigate the propagation delay problem.

(5) Explain how the user can set a desired target for the frequency of operation during the development phase, using the ISE Xilinx tools.

Explain which changes may be introduced by the designer into the circuit to try to achieve the desired target frequency, in case the design tools are unable to reach that frequency

→ past paper (93) Feb 2015

One of the advantages of the Von Neumann computer architecture is its flexibility, since it can be used to program almost all existing algorithms. However, this flexibility has its drawbacks.

. Describe in detail the Von Neumann computing paradigm and discuss its **disadvantages**.

(5) Explain how the parallelism enabled by the use of FPGAs to directly implement algorithms in hardware may help overcome those disadvantages, in spite of the slow frequency of operation imposed by the characteristics of their interconnection architecture.



## HBV

→ put Flip Flop in middle; depends 2/4  
 the delay; by 2; you are able to increase  
 frequency; by reducing delay, introducing  
 frequency; long combinational path  
 combinational path using



8. Hardware/software co-design features many advantages when compared to traditional hardware-based or software-based only design approaches.

→ introduction slide 71 → 75 and external lecture PPT

- 5 a. Explain, using your own words, the concept of hardware/software co-design and why, despite being around for more than two decades, the concept is even nowadays so difficult to implement in practice.

↳ definition external

- 0) b. List and explain the driving factors for choosing a co-design approach instead of a traditional hardware or software-based only design approach. -96 → 2015 past paper

- 5) c. The implementation of hardware/software co-design based systems needs a hardware platform, which can be fixed, configurable (like FPGAs), or hybrid (like FPGAs with hard core processors), involves software, and may even include an operating system. Explain the advantages of using FPGAs to implement hardware/software co-design based systems instead of ASICs. I 2015 past paper

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(10)Y. In FPGA-based embedded systems, two types of embedded processors are used – hardcore microprocessors, like the ARM-processor embedded in the Zynq family of FPGAs from Xilinx, and softcore microprocessors, like the Microblaze core, distributed as an IP (Intellectual Property) core by Xilinx. Explain the differences between these two types of microprocessors, and the advantages and disadvantages of using one or the other. + 4-3) 201; *post paper*

(15)7 Custom hardware modules in SOC (System-on-Chip) are usually under control of the central processor. The SOC architecture offers several possible hardware/software interfaces to attach these custom hardware modules. List

those different approaches and describe in detail each one, highlighting their differences. *introduction.*

8. Reuse is a mandatory word when developing new system descriptions using VHDL. The language provides the 'generic' statement to pass information into an entity and component.

(20) a. Using this statement, describe in VHDL a parameterizable up/down counter module.



(5)b. Suppose that in a new project you are developing, you need to use up/down counter modules with different widths – 32-bit and 64-bit. Show how these modules may be instantiated in

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the new project, by just reusing the module developed in

a). *↳ ~~posted it on the~~  
file in computer; ask people to get it*

The Instructor:

Manuel Gericota

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Spring 2015 make Up

Question 1)a) and b)

## FPGA vs. ASIC Design Advantages

| <b>FPGA Design</b>                      |                                                                         |
|-----------------------------------------|-------------------------------------------------------------------------|
| <b>Advantage</b>                        | <b>Benefit</b>                                                          |
| Faster time-to-market                   | No layout, masks or other manufacturing steps are needed                |
| No upfront non-recurring expenses (NRE) | Costs typically associated with an ASIC design                          |
| Simpler design cycle                    | Due to software that handles much of the routing, placement, and timing |
| More predictable project cycle          | Due to elimination of potential re-spins, wafer capacities, etc.        |
| Field reprogramability                  | A new bitstream can be uploaded remotely                                |
| <b>ASIC Design</b>                      |                                                                         |
| <b>Advantage</b>                        | <b>Benefit</b>                                                          |
| Full custom capability                  | For design since device is manufactured to design specs                 |
| Lower unit costs                        | For very high volume designs                                            |
| Smaller form factor                     | Since device is manufactured to design specs                            |

## FPGA vs. ASIC Design Flow

The FPGA design flow eliminates the complex and time-consuming floorplanning, place and route, timing analysis, and mask / re-spin stages of the project since the design logic is already synthesized to be placed onto an already verified, characterized FPGA device. However, when needed, Xilinx provides the advanced floor-planning, hierarchical design, and timing tools to allow users to maximize performance for the most demanding designs.

- based on your product which technology to use. In some cases there is a clear advantage to FPGAs and in other cases ASICs are in advantage.

In this article you find the main differences and comparisons in between the two technologies :

FPGA vs ASIC.

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### Price Comparison FPGA vs ASIC

Let's take an example that shows the total cost of ASIC and FPGA technology including both NRE and production unit price.

ASIC NRE: \$1.5M

ASIC Unit Cost: \$4

FPGA NRE: \$0

FPGA Unit Cost: \$8

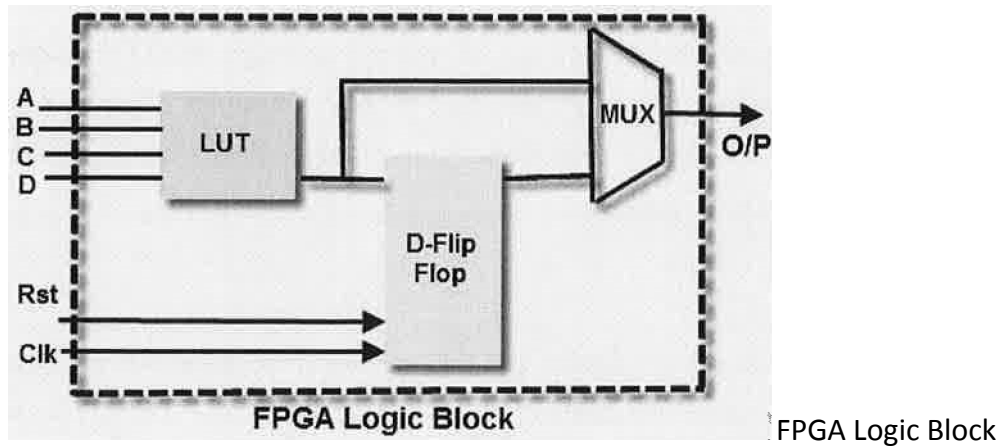
### Conclusion

In conclusion, both ASIC and FPGA are technologies with different benefits, however their difference relies on costs, NRE, performance and flexibility. In general, we can say that for lower volumes' designs, FPGA flexibility allows to save costs and obtain better results; while ASICs chips are more efficient and cost effective on high volume applications.

FPGAs can provide a number of advantages over a fixed function ASIC technology such as standard cells. Normally, ASICs takes months to manufacture and the cost of them will be thousands of dollars to obtain the device. But, FPGAs are fabricated in less than a second, the cost will be from a few dollars to a thousand dollars. The flexible nature of the FPGA comes at a significant cost in area, power consumption and delay. When compared to a standard cell ASIC, an FPGA requires 20 to 35 times more area, and the speed's performance will be 3 to 4 times slower than the ASIC. This article describes about the FPGA basics and FPGA architecture module that includes I/O pad, logic blocks and switch matrix. FPGAs are some of the new trending areas of VLSI. Therefore, these are used in VLSI based projects for electronic engineering students.

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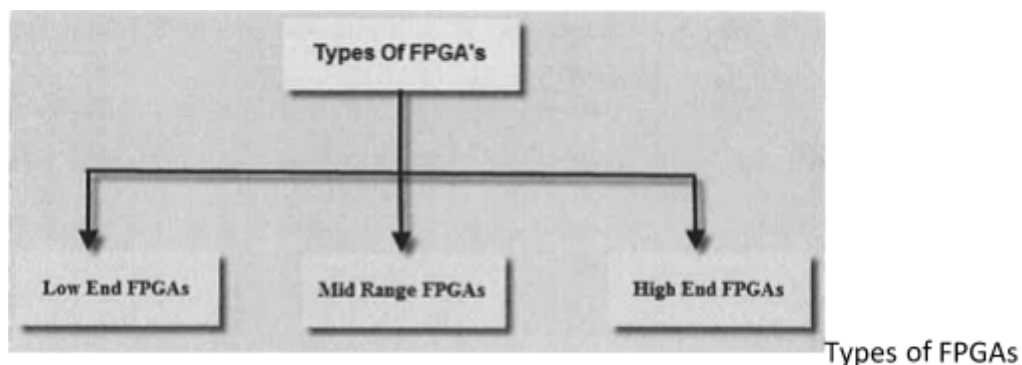
### CLE



Xilinx Virtex-5 is the most popular FPGA, that contains a Look up Table (LUT) which is connected with MUX, and a flip flop as discussed above. Present FPGA consists of about hundreds or thousands of configurable logic blocks. For configuring the FPGA, Modelsim and Xilinx ISE softwares are used to generate a bitstream file and for development.

#### ypes of FPGAs Based on Applications

Field Programmable Gate Arrays are classified into three types based on applications such as Lowend FPGAs, Mid-range FPGAs and high-end FPGAs.



#### Low End FPGAs

These types of FPGAs are designed for low power consumption, low logic density and low complexity per chip. Examples of low end FPGAs are Cyclone family from Altera, Spartan

## HBV

family from Xilinx, fusion family from Microsemi and the Mach XO/ICE40 from Lattice semiconductor.

### Applications of FPGA

Some More Common FPGA Applications are: Aerospace and Defense, Medical Electronics, ASIC Prototyping, Audio, Automotive, Broadcast, Consumer Electronics, Distributed Monetary Systems, Data Center, High Performance Computing, Industrial, Medical, Scientific Instruments, Security systems, Video & Image Processing, Wired Communications, Wireless Communications.

### FPGA vs. ASIC

- Difference between ASICs and FPGAs mainly depends on costs, tool availability, performance and design flexibility. They have their own pros and cons but it is designers responsibility to find the advantages of the each and use either FPGA or ASIC for the product. However, recent developments in the FPGA domain are narrowing down the benefits of the ASICs.

Speed-performance is limited by two main factors: combinational delays in logic blocks, and propagation delays through the interconnect's programmable switches. Unlike maskprogrammed technologies where combinational delay dominates, in FPGAs interconnect accounts for a very significant 40-60 percent of total delay [1]. Two key factors affect delays due to interconnect in an FPGA: 1) the routing architecture, which comprises the wires and switches used to interconnect the logic blocks, and 2) the CAD tools used to implement circuits.

3)a The basic concept behind the von Neumann architecture is the ability to store program instructions in memory along with the data on which those instructions operate. Until von Neumann proposed this possibility, each computing machine was designed and built for a single predetermined purpose. All programming of the machine required the manual rewiring

## HBV

of circuits, a tedious and error-prone process. If mistakes were made, they were difficult to detect and hard to correct. Von Neumann architecture is composed of three distinct components (or sub-systems): a central processing unit (CPU), memory, and input/output (I/O) interfaces. Figure

2.1 represents one of several possible ways of interconnecting these components.

The CPU, which can be considered the heart of the computing system, includes three main components: the control unit (CU), one or more arithmetic logic units (ALUs), and various registers. The control unit determines the order in which instructions should be executed and controls the retrieval of the proper operands. It interprets the instructions of the machine. The execution of each instruction is determined by a sequence of control signals produced by the Neumann architecture: shared memory for instructions and data with one data bus and one address bus between processor and memory. Instructions and data have to be fetched in sequential order (known as the Von Neumann Bottleneck), limiting the operation bandwidth.

Question3) b) CPU's are sequential processing devices. They break an algorithm up into a sequence of operations and execute them one at a time.

FPGA's are (or, can be configured as) parallel processing devices. An entire algorithm might be executed in a single tick of the clock, or, worst case, far fewer clock ticks than it takes a sequential processor. One of the costs to the increased logic complexity is typically a lower limit at which the device can be clocked.

Bearing the above in mind, FPGA's can outperform CPU's doing certain tasks because they can do the same task in less clock ticks, albeit at a lower overall clock rate. The gains that can be achieved are highly dependent on the algorithm, but at least an order of magnitude is not atypical for something like an FFT.

Further, because you can build multiple parallel execution units into an FPGA, if you have a large volume of data that you want to pass through the same algorithm, you can distribute the data across the parallel execution units and obtain further orders of magnitude higher throughput than can be achieved with even a multi-core CPU.



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The price you pay for the advantages is power consumption and \$\$\$'s.

Q4) Embedded Systems is an advanced technology with the combination of software and hardware. Which used in various domains like Telecom, Mobile technology, Industrial, medical, Automation, Automotive systems, Home Automation, Airplanes, Military, Vending machines and Toys etc. Using Embedded Systems, various system can be developed like Smartphone, Pedometers, Infusion pumps, Infotainment system, Electronic gadgets, TV, Fridge, AC etc.

Embedded Systems has various opportunities like Product Designing, Product Development, Software, Hardware, PCB designer, Firmware, RTOS development, Testing so and so.

An embedded system is a computer system with a dedicated function within a larger mechanical or electrical system, often with real-time computing constraints.<sup>[1][2]</sup> It is embedded as part of a complete device often including hardware and mechanical parts. Embedded systems control many devices in common use today.<sup>[6]</sup> Ninety-eight percent of all microprocessors are manufactured as components of embedded systems.<sup>[4]</sup>

Examples of properties of typically embedded computers when compared with general-purpose counterparts are low power consumption, small size, rugged operating ranges, and low per-unit cost. This comes at the price of limited processing resources, which make them significantly • Can achieve much faster processing speeds since they are optimized and not limited by fabric speed

- Fixed and cannot be modified (though it can take advantage of custom logic in FPGA fabric for processing)

Soft Core Processors - 250MHz and less (usually less than 200MHz)

- Can be easily modified and tuned to specific requirements, more features, custom instructions, etc.
- Multiple cores can be used (at the cost of resources)
- Limited by the speed of the fabric.

In recent years, there's been a large move towards hard processor primarily due to the need for faster processing that the soft cores can't provide. When you put a hard core processor with the FPGA fabric, you can typically enable processing of a lot of data, which is needed for communication infrastructure applications (lots of GBs of data going by), for example.

Hard Processor Core

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A hard processor core has dedicated silicon on the FPGA. This allows it to operate with a core frequency and have a DMIPS rating similar to that of a discrete microprocessor. A benefit a hard-core provides is that it exists in an environment where the surrounding peripherals can be customized for the application.

Unfortunately, it does not provide the ability to adjust the core for the application, nor does it allow for the flexibility of adding a processor to an existing design or an additional processor for more processing capabilities. In addition, only specific FPGAs will have the option of having a hard-core; therefore, the choice of vendors and FPGAs are limited.

### Soft Processor Core

A soft-core processor solution is one that is implemented entirely in the logic primitives of an FPGA. Because of this implementation, the processor will not operate at the speeds or have the performance of a hard-core or a discrete solution. In many embedded applications, the high performance achieved by the previous two processing options is not required, and performance can be traded for expanded functionality and flexibility.

Soft-core processors may be appropriate for a simple system, where the only functionalities are the manipulation of GPIO (General Purpose Input/Output). Moreover, they may also fit a complex system, where an operating system is incorporated and interfaces include Ethernet, PCI (Peripheral Component Interconnect), and DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory), and any other custom IP.

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## Questions:

- . We live in an analogue world. However, in our everyday lives we rely more and more in digital systems.

Discuss the main reasons for this shift from an analogue world towards an increasingly digitalized world, listing the advantages of digital vs analogue systems. → Introduction 1-0 4

For many years, the digital world was intimately associated to the idea of computers. In fact, the computer architecture developed in 1945 by John Von Neumann is not only the basis of today's computers, but can also be found at the core of many control systems. → Makeup exam 2015 end

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(5) Identify the main advantage of the Von Neumann's computer architecture that still makes it so valuable today, more than 70 years after its formulation.

(10)b. Explain how the parallelism enabled by the use of FPGAs (Field-Programmable Gate Arrays) may lead to a decline in the supremacy of the Von Newman's architecture, even in spite of the slow frequency of operation of FPGAs, when compared with microprocessors.

not - I you cross;  
-b of introduce De me."  
Jn microprocessor cl.'s n.Jt<sup>-</sup> o

o its when the Lk introduce  
filter;

**HSN** Høgskolen  
i Sørøst-Norge

→ introduction slides pg 33 and external document

Page 1 of 3

find connection between output  
input don't suggest  
• you have segments  
• parasitic capacitance + inductance  
Transistor  
in hope to cross several Transistors

(1) Define the concept of "dark silicon"? Explain how it can affect the performance of a system.

4. The use of Programmable Logic Devices, like FPGAs, experienced a tremendous growth in the last twenty years, conquering even the consumer electronics manufacturers, which traditionally used

ASICs (Application-Specific Integrated Circuits) in their mass production products. ~~2015~~ 2015

(10) Explain why FPGAs are substituting ASICs in consumer electronic products.

(15) b. List and justify the advantages and disadvantages of using FPGAs over ASICs in mass production products.

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- o be able to compete with the speed and efficiency of execution of algorithms implemented in ASICs a set of new, specialised, blocks are being added to FPGAs.
- a. Explain why the frequencies of operation of FPGAs are typically lower than those allowed by ASICs.
- (10) b. Using a generic model, describe the main components of a typical FPGA's internal architecture. Note: you may draw a generic FPGA model to support your description of the different FPGA architectural elements and of their functionality. *2015 past paper*
- (10) c. Explain how any arbitrary combinational logic function  $Y = f(A, B, C, D)$  (where Y is the output and A, B, C and D are the inputs) is implemented by an FPGA. *Architectural slide planation. eg Sand 6*  
 Note: you may use an example of implementation to support your explanation. *post paper*  
 Set g q
- d. List the type of dedicated resources added to the most recent FPGAs and explain how they contribute to increase the efficiency and speed of execution of certain applications, when compared with the more homogeneous, configurable logic block (CLB) -based, arrays of logic characteristic of the first FPGAs. *Architecture pg 70 by book 2.3 configurable logic block*
- (15) e. When implementing our clock or our scoreboard during the semester, we basically had two alternatives for that implementation: a purely hardware-based implementation or a mix of hardware-software implementation based on a soft microprocessor the Microblaze. Discuss the advantages and disadvantages of each one of the alternatives.
- (15) 7. In FPGA-based embedded systems, two types of embedded processors are used – hardcore microprocessors – like the Zynq – and softcore microprocessors – like the Microblaze. Explain the differences between these two types of

## HBV

microprocessors, and the advantages and disadvantages of using one or the other. *→ 2015*

3

## 1 - (SN

(15) When an engineer has to solve a problem using FPGAs, like the design and implementation of the <sup>0</sup> basketball scoreboard in your 3rd lab assignment, a set of design flow steps must be followed to guarantee a successful implementation of the proposed solution. List and explain the importance of each one of those steps, from the analysis of the problem to the

implementation of a solution using an FPGA. *introduction* -o I

(10) 9. Explain, using your own words, the concept of hardware/software co-design and why, despite being around for more than two decades, the concept is even nowadays so difficult to implement in practice.. *makeup* 2015

(15) 10. Hardware/software co-design features many advantages when compared to traditional hardware-based or software-based only design approaches. List and explain the driving factors for choosing a co-design approach instead of a traditional hardware or software-based only design approach

*18  
→ From*

11. The Constraints Editor offers the option to add a pull-up/pull-down to each of the input/output pins of the PGA.

C) p0•twj *sum*

(10)a. Explain what pull-up/pull-down are. *finding documents*

10b. Give a meaningful example of its use.

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Note: you may use a sketch to support your explanation.

The Instructor:  
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### Questions:

- 440) 1. Different problems require different solutions. In the digital electronics field, engineers may choose from different device technologies to implement their designs. technology, gate array technology or field-programmable with different characteristics. Compare the different technologies in terms of silicon area, speed and power.
- Handwritten notes: designs - gate array technology (FPGAs) - each one of them speed and power. Intelect slides pg 27 -> 35

- ← (10) 2. For many years, bulk programmer devices were needed to configure primitive field programmable logic devices. This is



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not the case anymore, due to the new technologies currently used to define the technology functionality of the devices. Describe the differences between the configuration technology used in the primitive devices and the current ones, which enable in-circuit configuration.

→ standard logic  
→ 10 Architecture

In the last 70 years, the Von Neumann computer architecture, developed in 1945 by John Von Neumann, has been the exclusive choice in computer design, being also one of the first options for the development of many control systems.

Identify the main advantage of the Von Neumann's computer architecture that still makes it so valuable today, more than 70 years after its formulation.

advantage

Explain why despite its advantages the microprocessors are no longer able to cope with the performance demands of the most advanced systems. ) -D -S9

introduction slide ① → 1/16

Page 1 of 3 ② → 1/16

(AM explanation by 26 book

✓ (10)  
in paper book  
handwritten  
from internet

c. Explain why FPGAs (Field-Programmable Gate Arrays) are substituting microprocessors in the most performance demanding tasks, even in spite of the slow frequency of operation of

4. FPGAs when compared with microprocessors. Post paper

The maximum frequency of operation of FPGA devices is set by manufacturers. However, this frequency does not mean users may always run their configured systems at the maximum frequency of operation set by the FPGA manufacturer. ...D post I(.Å-.S

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note, ✓

a. Describe in detail the factors that determine the maximum frequency of operation of an ey,v application implemented in an FPGA.

10 b. How can the user set the desired target for the frequency of operation during the development phase?

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← (10)

c. In case the design tools are unable to reach the defined frequency, which changes may be introduced by the designer into the circuit to try to achieve it?

5. Hardware/software co-design features many advantages when compared to traditional hardware-based or software-based only design approaches.

*intente* (15) a. Explain, using your own words, the concept of hardware/software co-design and 'joy', despite

being around for more than two decades, the concept is even nowadays so difficult to implement in practice. -7

*past paper* 2c16

(20) b. List and explain the driving factors for choosing a co-design approach instead of a traditional hardware or software-based only design approach. →

(15) c. The implementation of hardware/software co-design based systems needs a hardware platform, which can be fixed, configurable (like FPGAs), or hybrid (like FPGAs with hard core processors), involves software and may even include an operating system. What are the advantages of using FPGAs to implement hardware/software co-design instead of ASICs? *? past paper 2c16*

(15) 6. In FPGA-based embedded systems, two types of embedded processors are used - hardcore microprocessors and softcore microprocessors. Explain the differences between these two types of microprocessors, and the advantages and disadvantages of using one or the other. → *past paper*

(20) 7. In Systems-on-Chip (SoCs) there are basically three different ways of attaching user's hardware to microprocessors:

- To integrate a custom hardware module as a standard peripheral on a system bus;

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- To attach custom hardware through a local bus system or coprocessor interface provided by the microprocessor;
- To integrate a custom-hardware datapath inside of the microprocessor.

Discuss the advantages and limitations of tch method in rms of communication speed, gype-of communication channel, bandwidth, scalability, and any ot\_er features vou think are important to assess the adequacy of the interface to the requirements of a specific custom-hardware module.

2 of 3

'e?fhe Constraints Editor offers the option to add a pull-up/pull-down to each of

the input/output pins of the FPGA. *From Xilinx Constraint user manual.*

(10M a. Explain what pull-up/pull-down are.

(10) b. Figure 1 shows a push-button connected to an I/O block of an FPGA. Explain how should we configure the I/O block to be able to correctly read the logic values coming from the pushbutton, why that configuration is necessary and how we may do that?

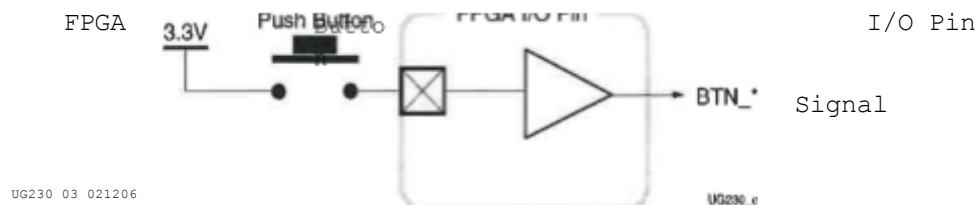


Figure 1: Push-Button Switches

(adapted from: Spartan-3E FPGA Starter Kit Board User Guide, Xilinx)

The Instructor:

ES-SCH4300

**HBV**

Manuel Gericota

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## EXAMINATION INFORMATION PAGE

### Written examination

|                                                                                                                        |                                                                          |                                                                     |
|------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|---------------------------------------------------------------------|
| Subject code:<br>ES-SCH4300                                                                                            | Subject name:<br>Software/Hardware co-development<br>of embedded Systems |                                                                     |
| Examination date:<br>May 9 <sup>th</sup> , 2017                                                                        | Examination<br>time from/to:<br>9h – 12h                                 | Total hours:<br>3 (three) hours                                     |
| Responsible subject<br>teacher:<br>Manuel<br>Gericota                                                                  |                                                                          |                                                                     |
| Campus:<br>Kongsberg                                                                                                   | Faculty:<br>Faculty of Technology and<br>Maritime Sciences               |                                                                     |
| No. of assignments: 5                                                                                                  | No. of<br>attachments:                                                   | No. of pages<br>incl. front<br>page and<br>attachments:<br>4 (four) |
| Permitted aids:<br><br>All aids are allowed, apart from computer, mobile phones or any other<br>communication devices. |                                                                          |                                                                     |

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Information regarding attachments:

Comments:

Please read the instructions carefully before start answering.

Select the type of examination paper

Spreadsheets

Line sheets

CANDIDATES MUST THEMSELVES CHECK THAT ALL ASSIGNMENTS AND ATTACHMENTS ARE IN ORDER.

Høgskolen ES-SCH4300

RSN i Sørøst-Norge

\_\_\_\_\_ SW/HW co-development of embedded systems

Spring semester 2017

Written examination

Please read the instructions carefully before start answering.

Instructions:

1. Write your Candidate number in each exam sheet.
2. The exam is worth a total of 200 points. The points allocated to each part of each question or problem are shown in brackets before the question/problem statement.
3. Answer all questions on the examination sheets.

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4. You may answer questions or problems by the same order they appear or not, providing that you clearly identify which question or problem you are answering.
5. Write your answers in clear, legible handwriting, preferably using a black ballpoint or rollerball pen.
6. Almost all questions are open-ended questions designed for you to give a meaningful answer using your own knowledge.

### Questions:

1. In 1965, Gordon Moore published a paper titled "Cramming more components onto integrated circuits" (Electronics, vol. 38, no. 8, pp. 114-117, April 19, 1965), where he enunciates what became known as the Moore's Law. Over more than 50 years, the semiconductor industry tried to follow what was, without any doubt, an empirical law with no scientific basis other than a mere observation of what was going on back then. But currently, the industry is struggling to keep pace with the Moore's Law.
- (5)a. Identify what was the initial formulation of the Moore's Law.
- (10) b. Explain how the Moore's Law contributed to the advancements in the semiconductor industry.
- c. Explain why, despite those advances and the use of multi-core approaches, the performance of microprocessors is no longer increasing at the same pace as before.
- 0 d. Define the concept of "dark silicon". Explain how it can affect the performance of a multicore microprocessor.

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2. "Intel has agreed to shell out a whopping \$16.7 billion to acquire Altera, a company that makes something Intel lacks: FPGAs (field-programmable gate arrays) from PC World.

5 a. Explain in your own words what is an FPGA and which are the main features that distinguish

FPGAs from ASICs (Application Specific Integrated Circuits).

5 b. Using a generic model, list and describe the main components of a typical FPGA internal architecture.

Note: You may draw a generic FPGA model to support your description of the different FPGA architecture elements and of their individual functionality.

c. Explain how any arbitrary combinational logic function  $Y = f(A, B, C, D)$  (where  $Y$  is the output and  $A$ ,  $B$ ,  $C$  and  $D$  are the inputs) is implemented by an FPGA.

Note: You may use an implementation example to support your explanation.

0)d. Explain how adding programmable logic resources to microprocessors may enhance their performance.

3. Energy efficiency and performance are two important factors to prefer a hardware implementation over a software one.

0 a. Explain why a pure hardware implementation of a given algorithm is more energy efficient and has a better



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relative performance than the software implementation of the same algorithm.

- 0 b. Apart from energy efficiency and performance, there are other arguments that must be considered when choosing to implement a design using a pure hardware or software approach, or using a hardware/software co-design one. List and explain the driving factors for choosing a co-design approach instead of a traditional hardware or software -based only design approach.

4.A Programmable System-on-Chip (PSOC) combines into a single FPGA several components one or more microprocessor cores of the same or different types (CPU, GPU), internal memory blocks, dynamic memory interfaces (DDR3, DDR4), DSP blocks, high-speed interface peripherals (PCIe, USB, Ethernet), analog-to-digital converters - and programmable logic resources where other components, usually known as peripherals, may be implemented by the user. On-chip communication buses enable the transfer of information among all these resources.

- (15) a. Identify the main elements of an on-chip bus and detail the role of those elements in the transfer of information.

- (15) b. Explain what is an address space and why is it necessary to organize the communication between components.

Note: You may use a sketch to support your explanation of what an address space is.

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- (15) c. One of the transfer modes used to transfer data in on-chip buses is the burst mode. Explain how a burst mode transfer differs from a simple read or write transfer.
- (5) d. Identify the main advantage of a burst mode transfer compared to simple read or write transfer.
5. The ability to provide a hardware platform that can be customized on a per-application basis under software control has established Reconfigurable Computing (RC) as a new computing paradigm. The basis of this paradigm is the concept of virtual hardware.
- (15)a. Explain in detail the concept of virtual hardware.
- (10)b. Identify the main goal beyond this new computing paradigm.

The Instructor:  
Manuel Gerjcota