W13 Apr 15 (D1) Array sorter

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All Sections

These questions are presented under the following assumptions:

- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

N.B.: This question is inspired in Patrick R. Schaumont, "**A Practical Introduction to Hardware/Software Codesign** ", Problem 5.2, pp. 151-152.

Consider a high-speed sorter for four 32-bit registers (Fig. 5.12):

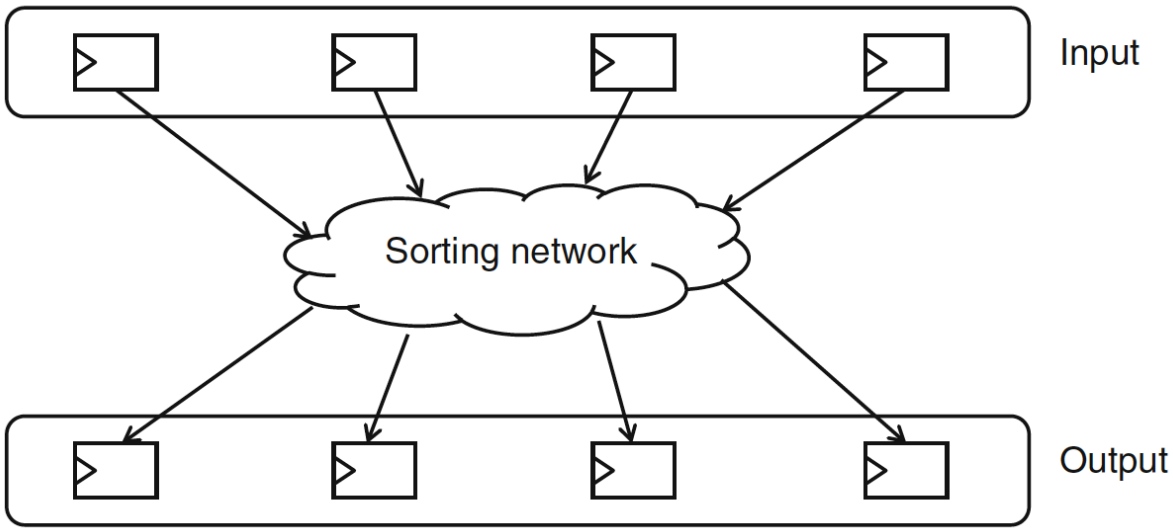

Fig. 5.12 Sorter design for Problem 5.2

1. Present an FSMD architecture that implements this functionality.
2. Can you compare the speed of your hardware architecture to an equivalent software solution?

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