W02 Jan 15 (D1) Simple CPU: JRZ (conditional jump)

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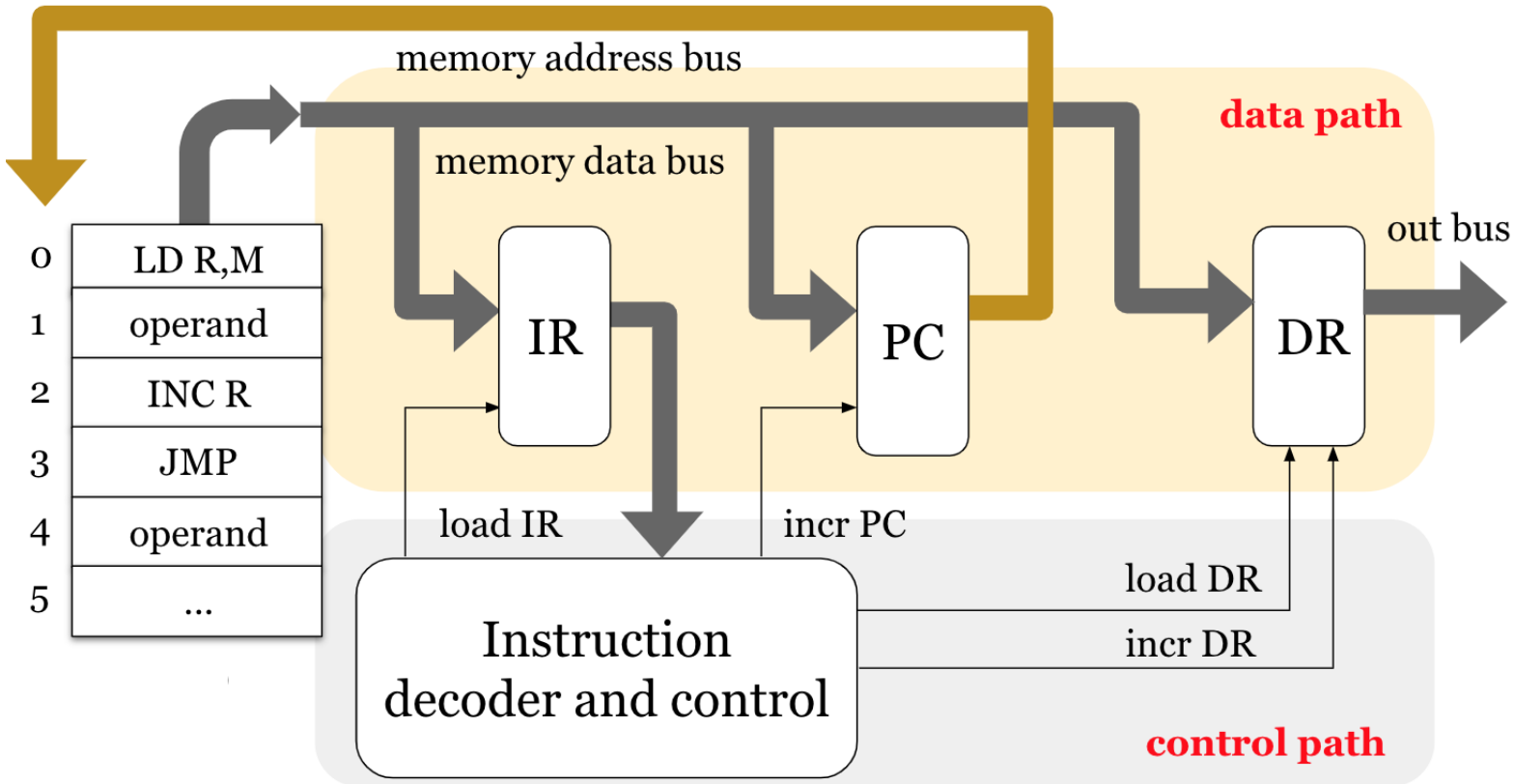
All Sections

These questions are presented under the following assumptions:

- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

The picture shown below represents the minimum set of blocks required to implement an architecture that is able to execute a program stored in memory, including a basic CPU and an external 8-bit memory (N=32) that is used to store instructions and data items.



1. Present an ASMD chart for a JRZ <address> instruction (Jump if R is zero). Assume that <address> is an 8-bit value stored in memory immediately after the JRZ opcode.
2. Add this instruction to your Vivado Basic CPU project and paste below the simulation waveforms that prove its correct operation.

CPUwithROMfiles.zip