W03 Jan 29 (D1) UART receiver ASMD chart: The Stop state

Jose Ferreira

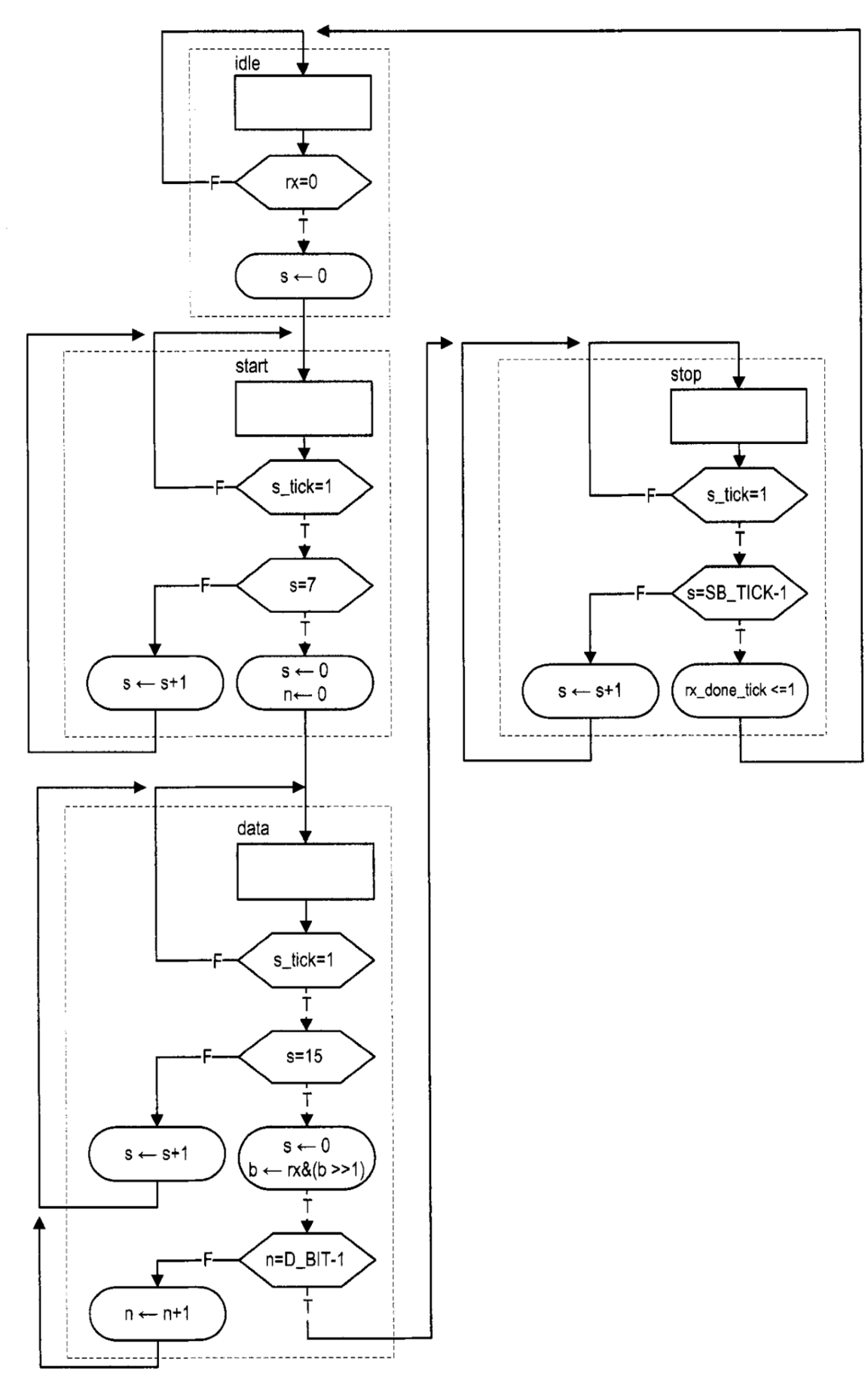
All Sections

These questions are presented under the following assumptions:

- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

Consider the UART receiver ASMD chart presented below.

1. How would the behaviour of this circuit be modified if we deleted state *stop*, and asserted the “rx_done_tick” output immediately before leaving state *data*?
2. Change the corresponding VHDL description (listing 7.1 attached) accordingly, and use an appropriate test bench to check if your answer is correct.



(img source: P. Chu’s **FPGA prototyping by VHDL examples** , Figure 7.3, p. 166)