W01 Jan 08 (D1) Simple CPU: Modify and expand

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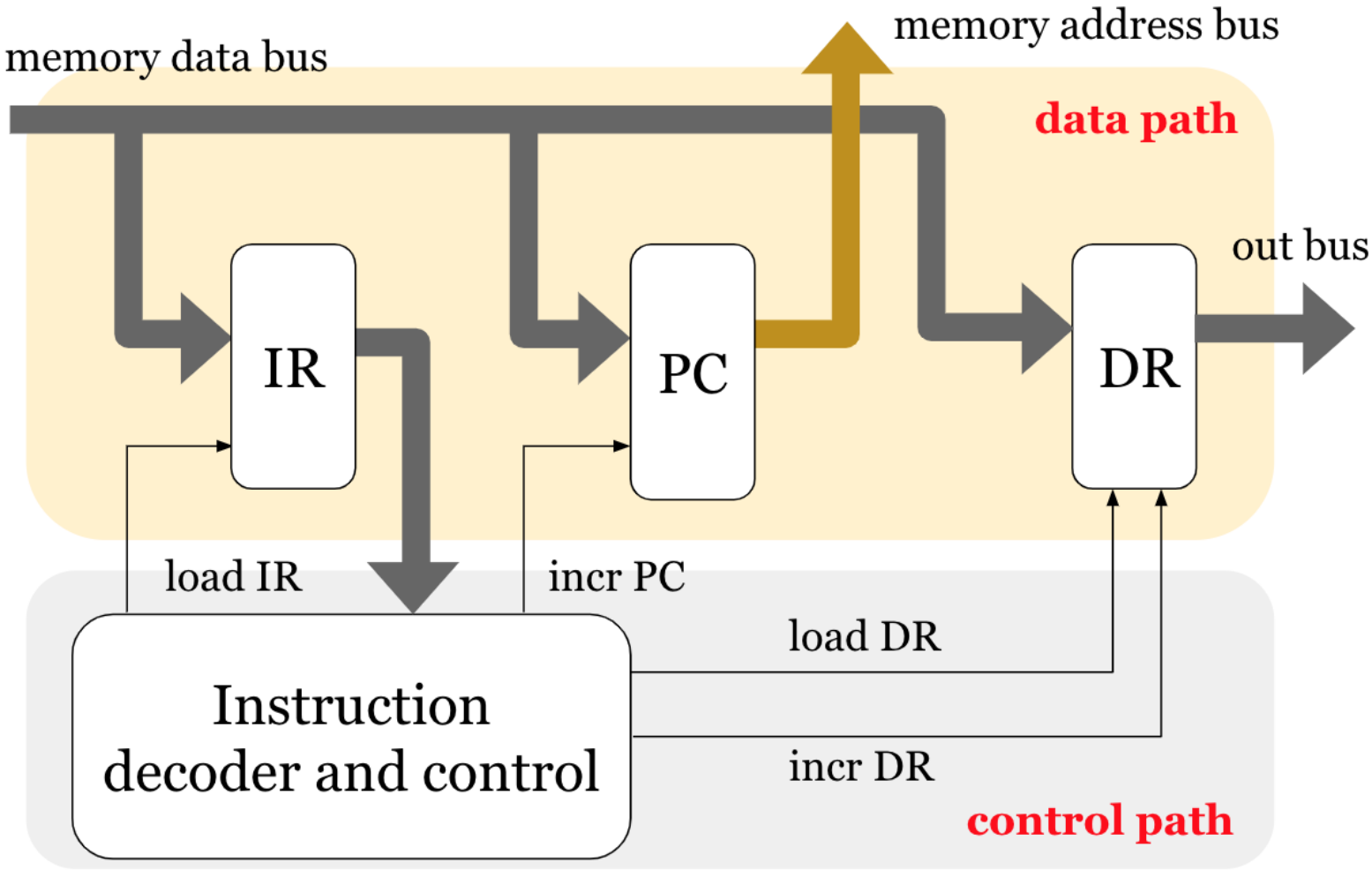
All Sections

These questions are presented under the following assumptions:

- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

The attached files represent a VHDL description and a testbench for the simple CPU architecture represented below, assuming that only two instructions are supported: LD R,M (load R with a data word that is stored immediately after the instruction opcode) and HALT (stop program execution).



1. The attached test bench was created to check the execution of a program comprising only two instructions: LD R,M (where M should contain ”A0” hexadecimal) and HALT. Use Vivado to carry out the simulation, and explain why R loads FFh instead of A0h; make the appropriate changes so that R loads A0h.
2. The attached VHDL description for the CPU shows that the execution of LD R,M takes 3 clock cycles. Would it be possible to execute this instruction in less clock cycles? Change the code appropriately if you answer is yes and prove your solution by simulating with your test bench as created for the previous question.

3. Expand the VHDL description of this simple CPU in order to support two additional instructions: INC R (increment the content of R) and TOG R (toggle the content of R).

SimpleCPU.zip

Victor Johan Hansen

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1. We have 3 states in this FSMD. R can loa…