W02 Jan 15 (D3) Binary multiplication with a FSMD

5

Jose Ferreira

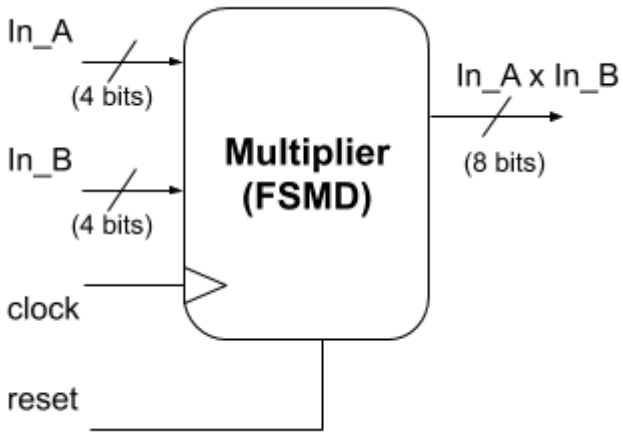
All Sections

These questions are presented under the following assumptions:

- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

Consider a circuit that receives two 4-bit operands, and generates an 8-bit result that represents the product of the two inputs.

1. Represent a block diagram showing an FSMD architecture for this circuit, assuming that the multiplication is carried out by adding In_A with itself, for as many times as indicated by In_B (e.g. 12 x 5 = 12 + 12 + 12 + 12 + 12).
2. Represent an ASMD chart for this FSMD.
3. Create a Xilinx project to implement this FMSD, and demonstrate its correct operation through simulation.
4. Add to your Xilinx project the necessary blocks to demonstrate the operation of your solution in the Basys-3 board, using the 8 switches to define the two operands, and the 7-segment digits to display the result.



5. What changes would be required to your datapath in order to ensure that the multiplication always takes the smallest possible number of clock cycles?

Reply

Leila Mozaffari

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1. 2.

Han Zhou

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Hi, is this FSM data path an acceptable answer ? Another …