W05 Feb 12 (D2) An electronic piano

Jose Ferreira

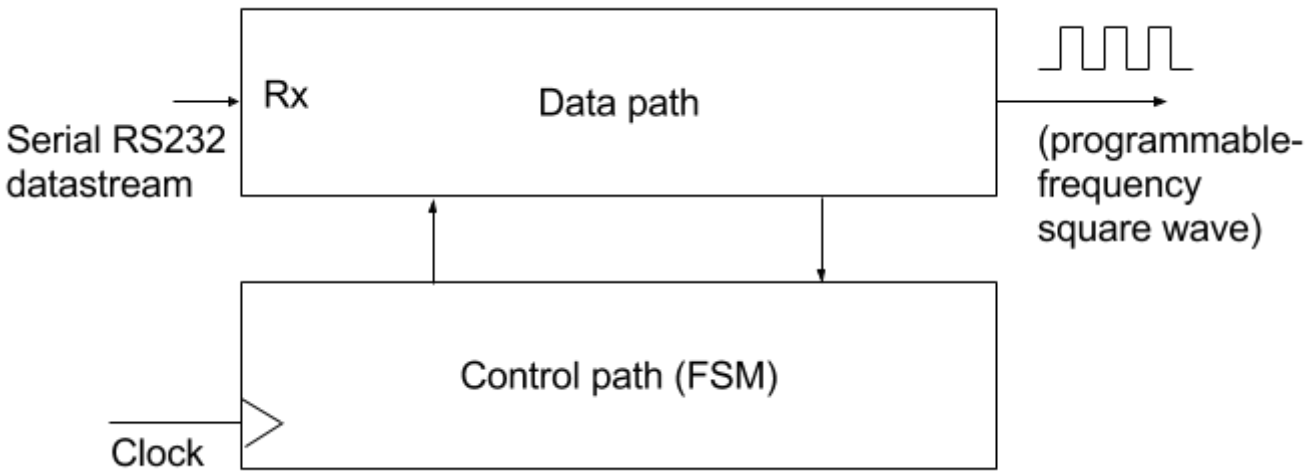
All Sections

These questions are presented under the following assumptions:

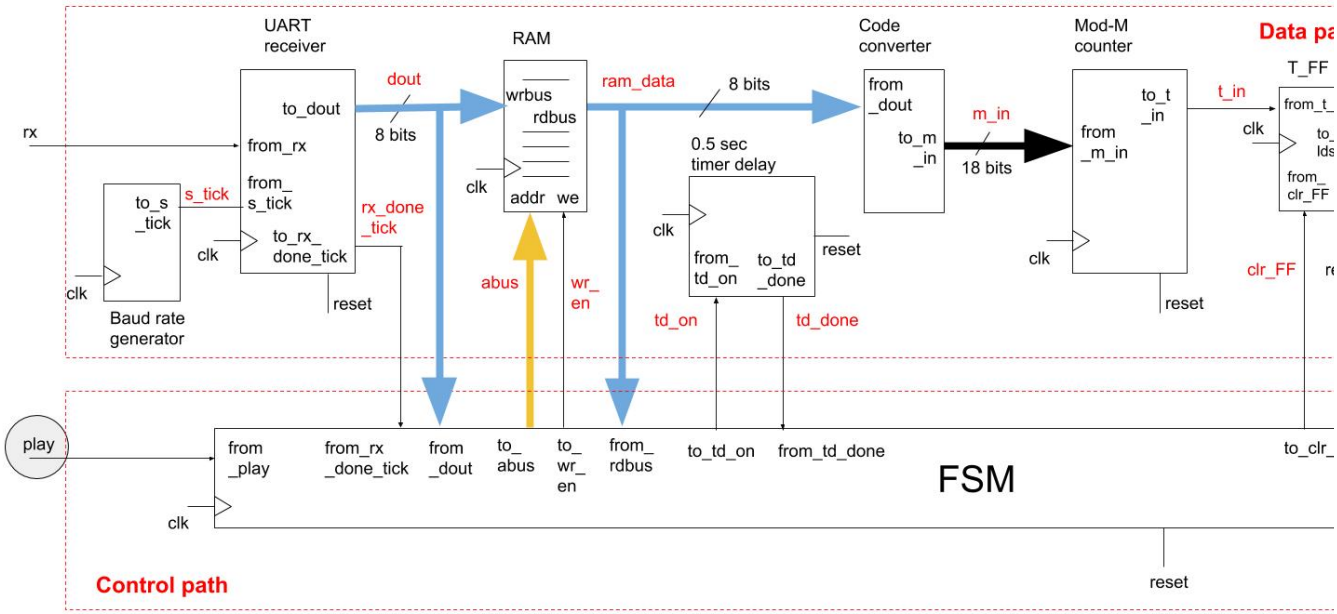
- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

Consider the following functional specification for a simple electronic piano represented by the block diagram illustrated below:

- The range of musical notes should cover octaves 4 (261.626 to 493.883 Hz) and 5 (523.251 to 987.767 Hz), and be represented by a set of corresponding ASCII codes according to any computer keys of your choice
- Each musical note is to be received through an RS232 serial channel and played as soon as it is received
- Each musical note will continue to play until another valid ASCII code is received (representing another musical note from octaves 4 or 5) or until an invalid ASCII code is received (in which case the music will stop)



1. What changes are required -- if any -- to the data path architecture presented below in order to meet the functional requirements presented above?



2. Present an ASMD chart for the corresponding control path.
3. The RAM address is generated by the control path in the diagram shown above (under question 1). Considering that the RAM address generator is most likely a binary counter, is there any reason to include it in the control path instead of the data path?