W02 Jan 15 (D6) Debouncing FSMD

5

Jose Ferreira

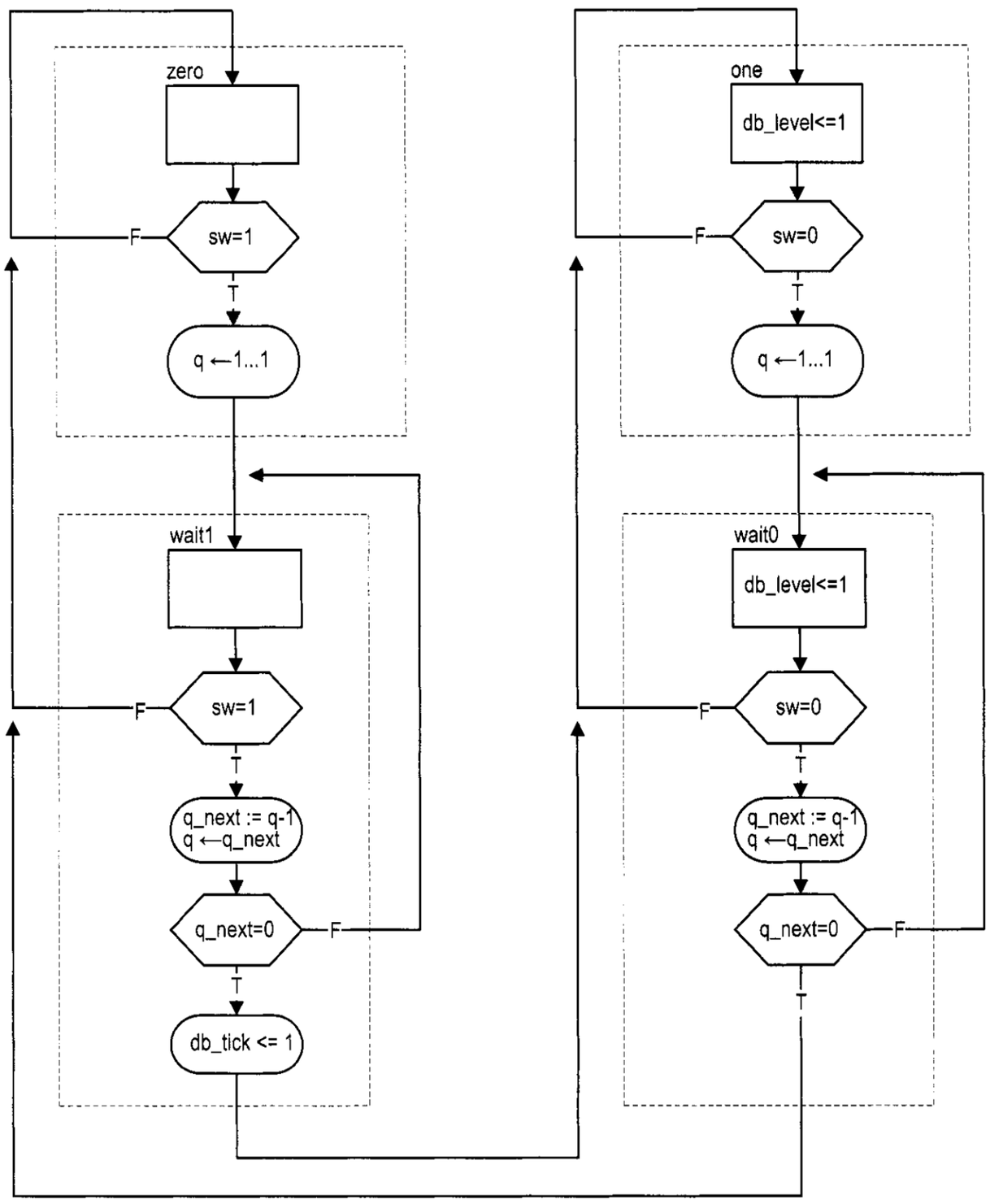
All Sections

These questions are presented under the following assumptions:

- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

Consider the ASMD chart represented below, which specifies the behaviour of a debouncing circuit based on a FSMD architecture, and its explicit and implicit datapath descriptions, as represented in listings 6.1 and 6.2 (attached).

1. What differences would a user notice in the circuit behaviour, if “q_next” was replaced by “q_reg” in the decision boxes of states *wait1* and *wait0*?
2. Modify the ASMD chart in order to ensure that the “db_tick” output pulse rises together with the “db_level” output, instead of immediately before.
3. Modify the ASMD chart in order to generate a “db_tick” pulse also in the case of falling edges of the “db_level” output.
4. Why is it necessary to include the “q_next” signals in the sensitivity list of the “next-state & datapath functional units/routing” process in the implicit VHDL description? (listing 6.2, line 104 in the attached file)



(img source: P. Chu’s **FPGA prototyping by VHDL examples** , Figure 6.6, p. 133)

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for q1, no state change will be happen ? for q2, where is th…