W02 Jan 15 (D4) Odd parity generator as a FSMD: From a datapath to an ASMD chart

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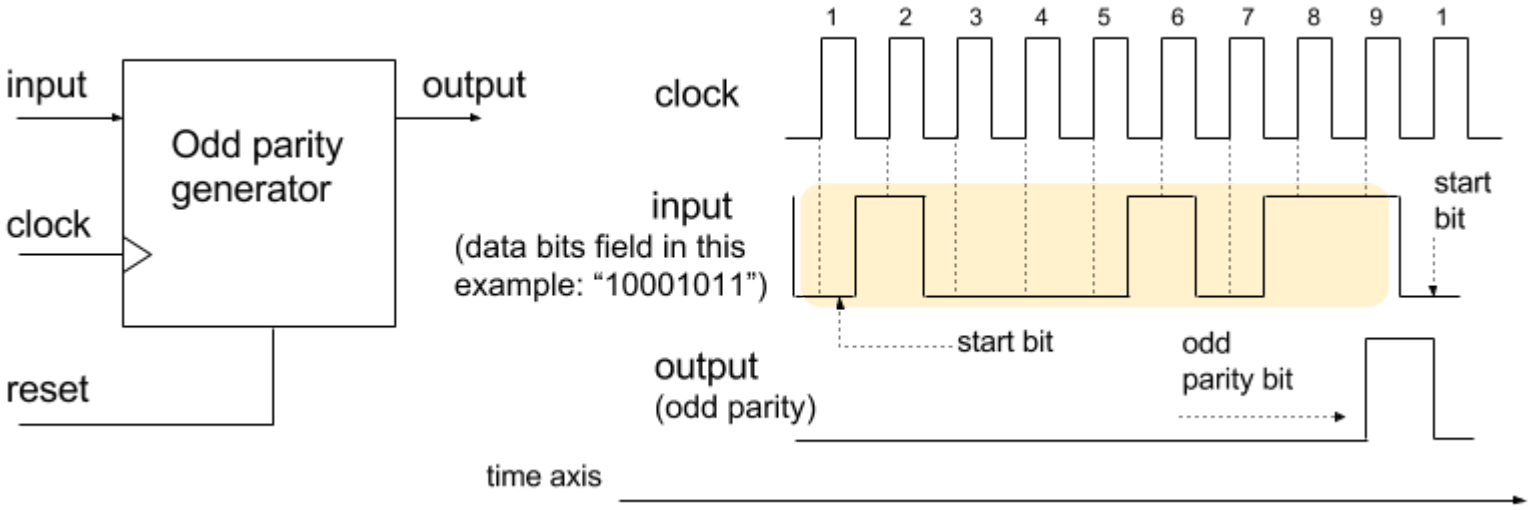
All Sections

These questions are presented under the following assumptions:

- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

Consider an odd parity generator receiving a 9-bit frame that comprises a start bit (‘0’) followed by 8 data bits. This circuit counts the number of ‘1’s in the data bits field, and generates an odd parity output on each 9th clock cycle (see the example below). **N.B.**: The odd parity output will be ‘1’ when the number of ‘1’s in the data bits field is even (so that the total number of ‘1’s is odd), and ‘0’ otherwise.



This circuit may be implementation as a simple FSM, but we want to design it as a FSMD using the datapath illustrated below. Present an ASMD chart for the corresponding control path.