W02 Jan 15 (D5) Odd parity generator as a FSMD: Implementation flaw

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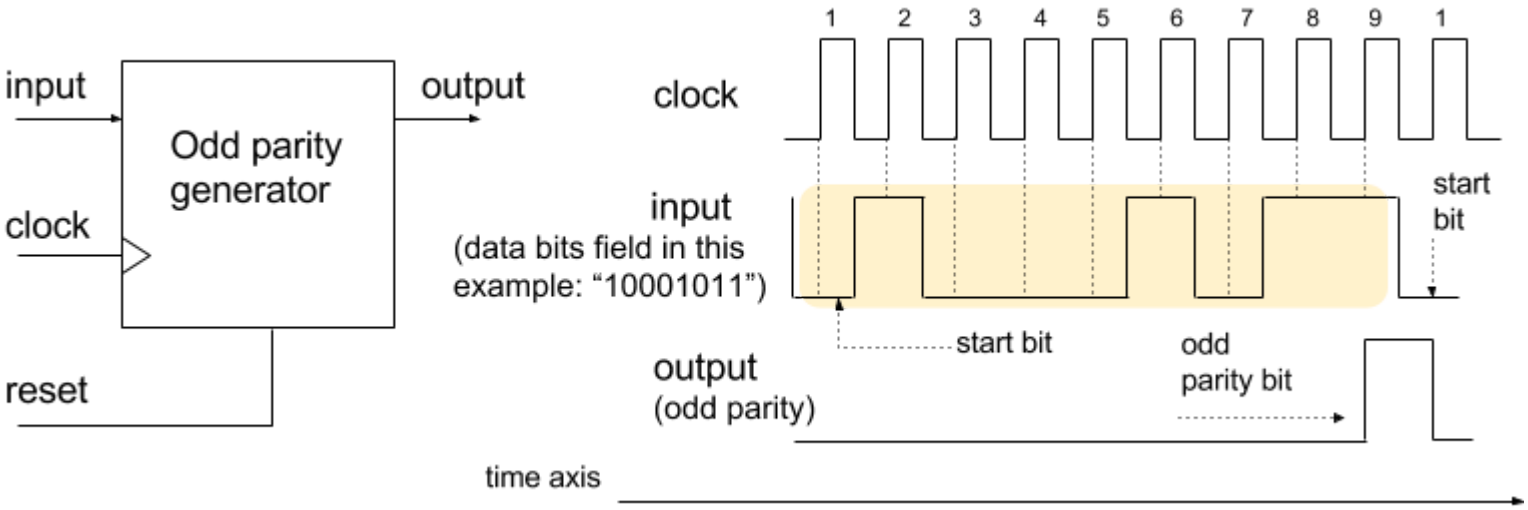
All Sections

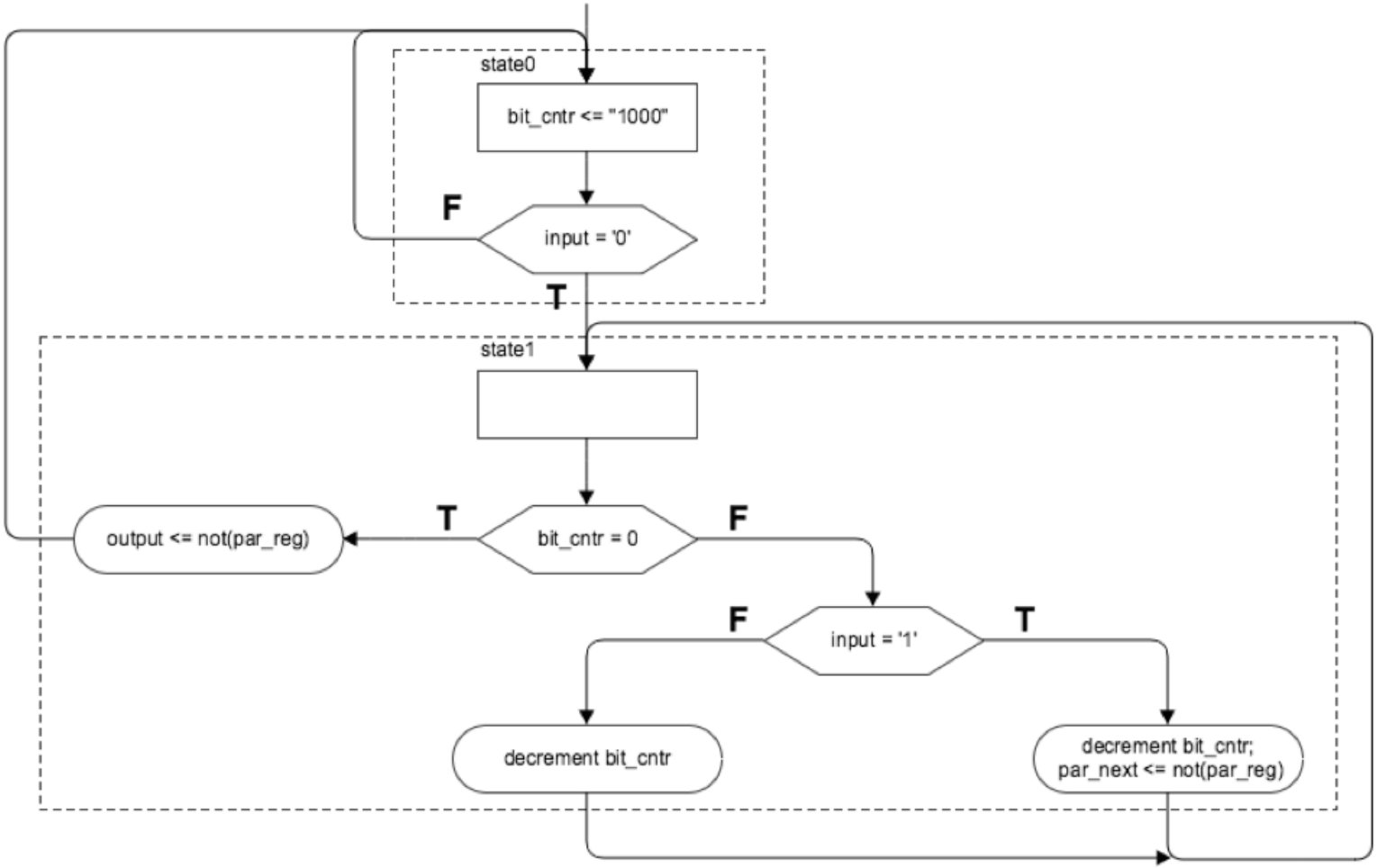
These questions are presented under the following assumptions:

- They may be selected to be part of the final exam
- Responses must be posted by the students (not me)
- I will call your attention to any mistakes or wrong content posted in response

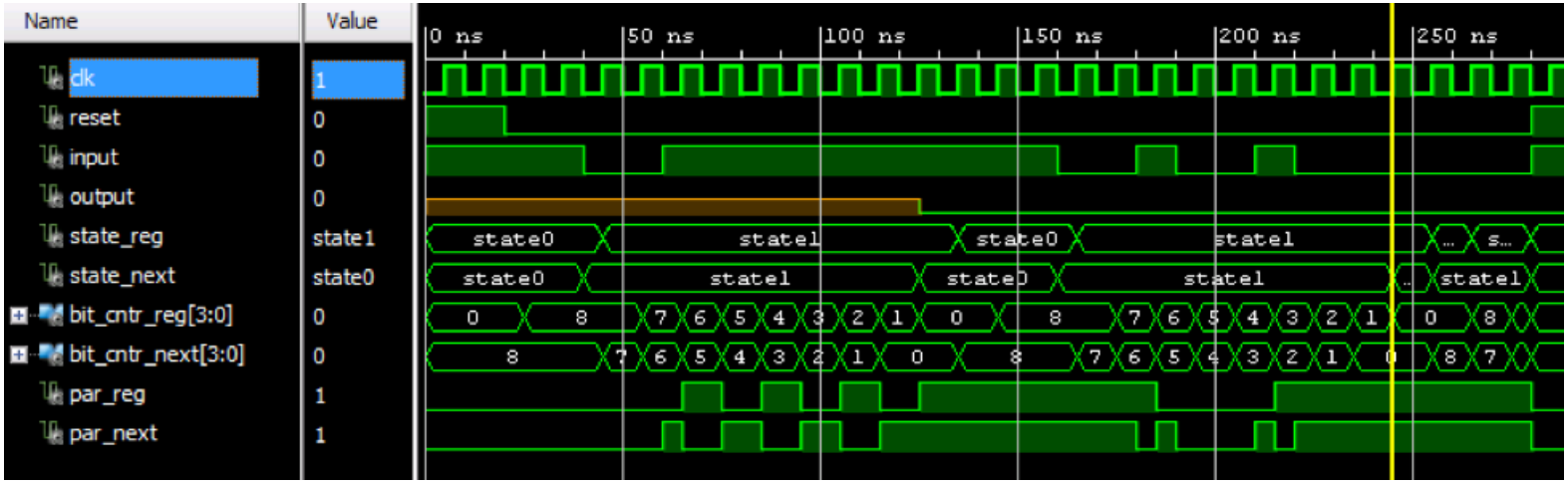
Consider an odd parity generator receiving a 9-bit frame that comprises a start bit (‘0’) followed by 8 data bits. This circuit counts the number of ‘1’s in the data bits field, and generates an odd parity output on each 9th clock cycle (see the example below). **N.B.**: The odd parity output will be ‘1’ when the number of ‘1’s in the data bits field is even (so that the total number of ‘1’s is odd), and ‘0’ otherwise.



This circuit may be implementation as a simple FSM, but we want to design it as a FSMD using the ASMD chart represented below, and the corresponding VHDL description presented in attachment.



A simulation session using the input sequence illustrated below (test bench equally in attachment) shows that this solution does not meet the requirements specified above. Identify the problems and correct the ASMD chart to avoid them.



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Han Zhou

Hi, Jose Where is the attachment you menti…

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