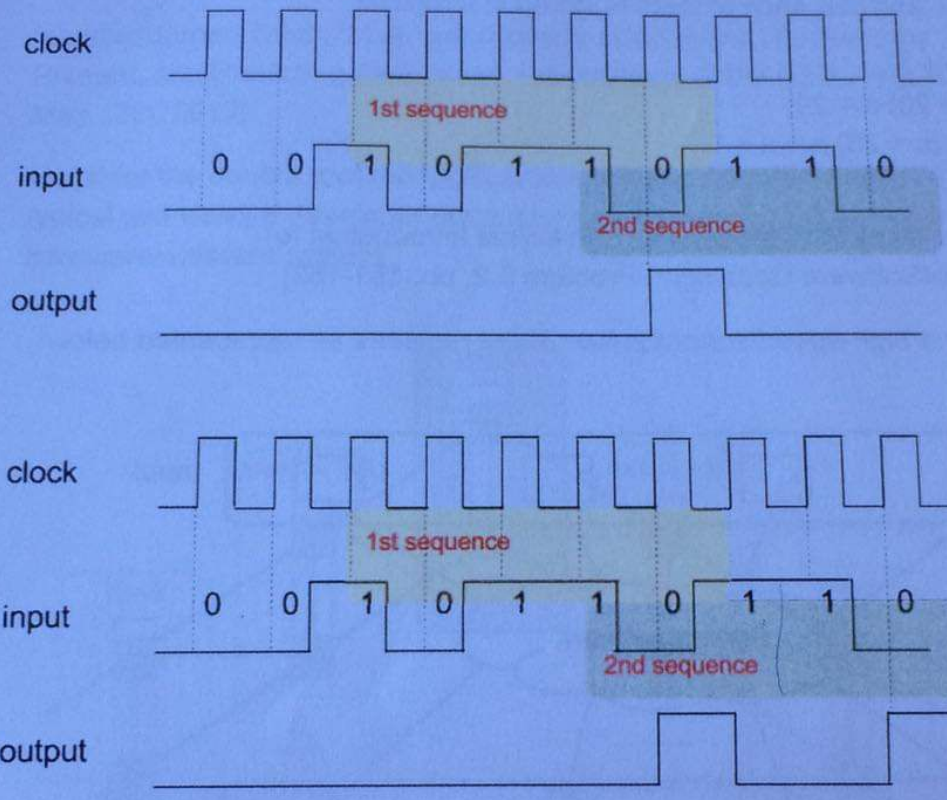
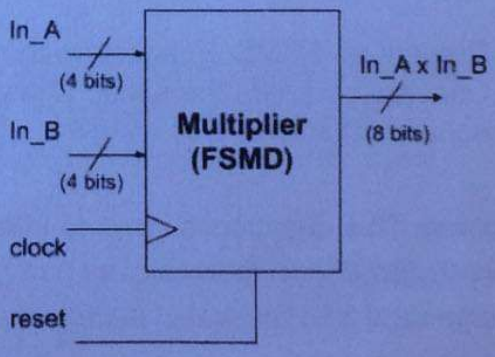
1. Consider a one input / one output FSM that checks if its input bitstream contains the sequence "10110", and generates a pulse in its output when this condition is verified. Present an ASM chart to specify the behaviour of this FSM in each of the two following cases:

1. Assuming that overlapping sequences are not valid.
2. Assuming that overlapping sequences are also valid (see waveforms below to illustrate the two cases).



2. Consider a circuit that receives two 4-bit operands, and generates an 8-bit result that represents the product of the two inputs:



1. Represent a block diagram showing an FSMD architecture for this circuit, assuming that the multiplication is carried out by adding In_A with itself, for as many times as indicated by In_B (e.g. 12 x 5 = 12+12+12+12+12).
2. Represent an ASMD chart for this FSMD.

3. [source: Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Codesign", Problem 1.4, pp. 28-29]

D03e

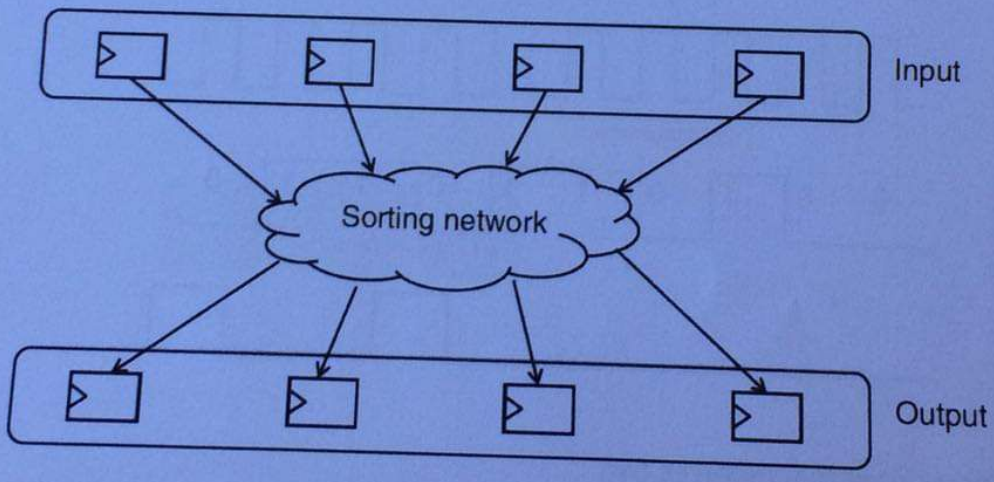
Describe a possible implementation for each of the following C statements in hardware (use a block diagram). You can assume that all variables are integers, and that each of them is stored in a register.

1. a = a + 1;
2. if (a > 20) a = 20;
3. while (a < 20) a = a + 1;

4. [source: Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Codesign", Problem 5.2, pp. 151-152]

D03g

Consider a high-speed sorter for four 32-bit registers as represented below:



1. Present an FSMD architecture that implements this functionality.
2. Can you compare the speed of your hardware architecture to an equivalent software solution?

5. [source: This question is inspired in a discussion proposed by Group 5 (Ole, Eivind, Jan Ali) on this topic, as part of their deliverables for coursework assignment #1. The way it is proposed ahead follows its presentation in

D03j

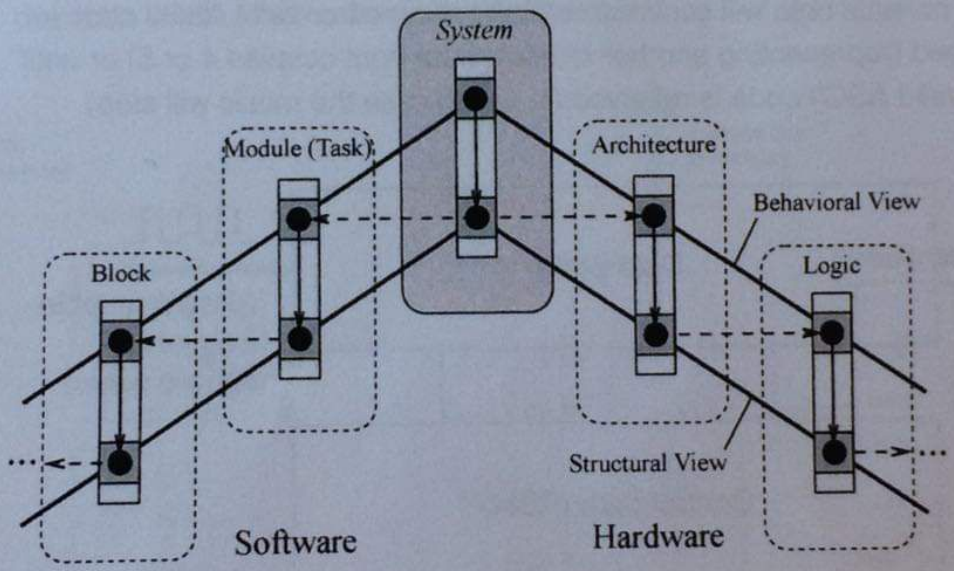
Jürgen Teich, "Hardware/Software Codesign: The Past, the Present, and Predicting the Future", Proceedings of the IEEE, Vol. 100, May 13th, 2012]

> "Apart from the necessity of specification, formal analysis, and cosimulation tools for performance and cost analysis, (...) the major synthesis problem in codesign of electronic systems (...) involves three major so-called mapping tasks."

Name these three tasks, and present a brief description of each one of them.

6. [source: Jürgen Teich, "Hardware/Software Codesign: The Past, the Present, and Predicting the Future", Proceedings of the IEEE, Vol. 100, May 13th, 2012]

Consider the double roof model illustrated below, which describes "the typical two views a developer encounters when designing a complex hardware/software system".



Explain why "a pure top–down design might not be possible or desirable for many companies in many product cases", and briefly explain how a "meet-in-the-middle" design strategy provides a better solution in such cases.

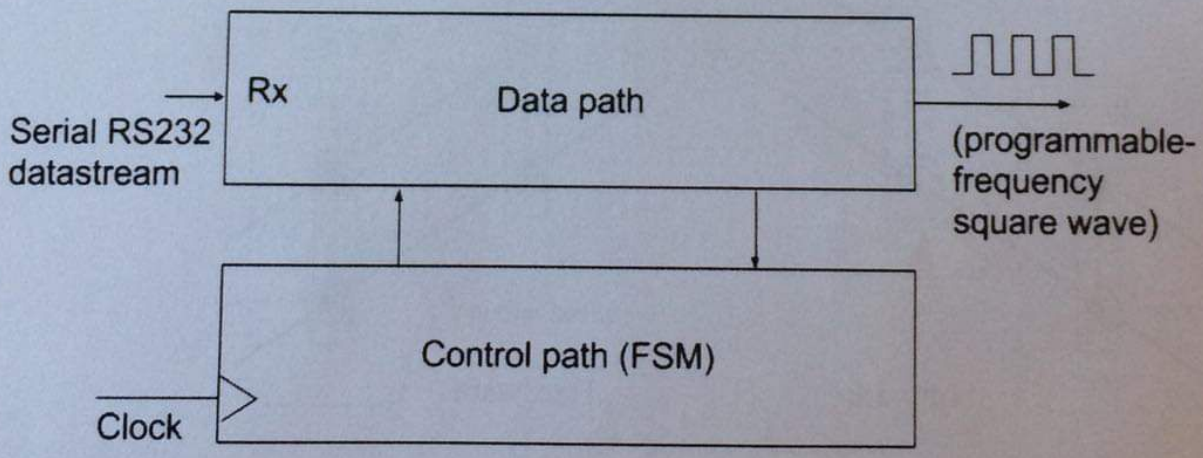
7. [source: This question is inspired in a discussion proposed by Group 2 (Bozhao, Chrisander, Huseyin, Bilgehan) on this topic, as part of their deliverables for coursework assignment #1]

Wikipedia defines hardware acceleration as "the implementation of computing tasks in hardware to decrease latency and increase throughput".

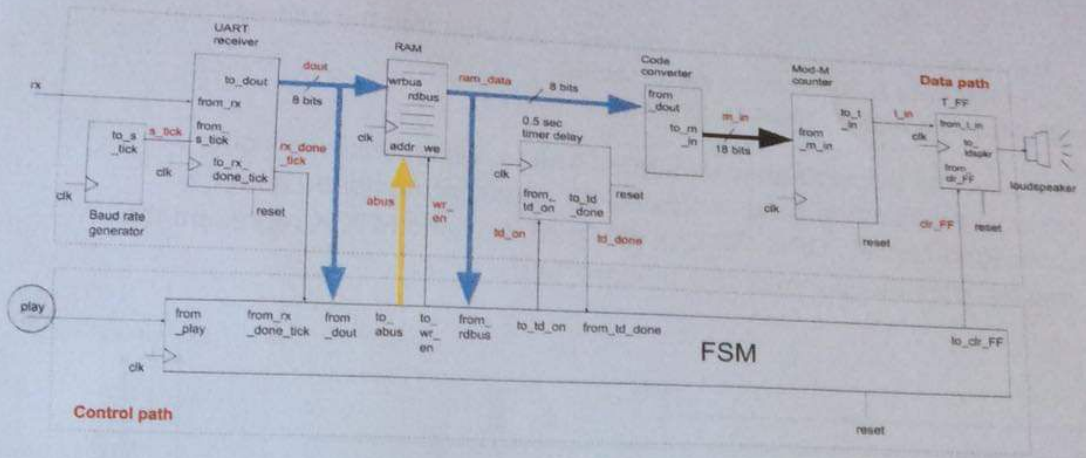
1. Present the meaning of the two design attributes referred above (latency, throughput), and briefly explain why a mixed hardware/software implementation may improve system performance.
2. Can coprocessors be considered as a form of hardware acceleration? What distinguishes this class of circuits from other application-specific hardware architectures that can interact with a general purpose CPU?

8. Consider the following functional specification for a simple electronic piano represented by the block diagram illustrated below:

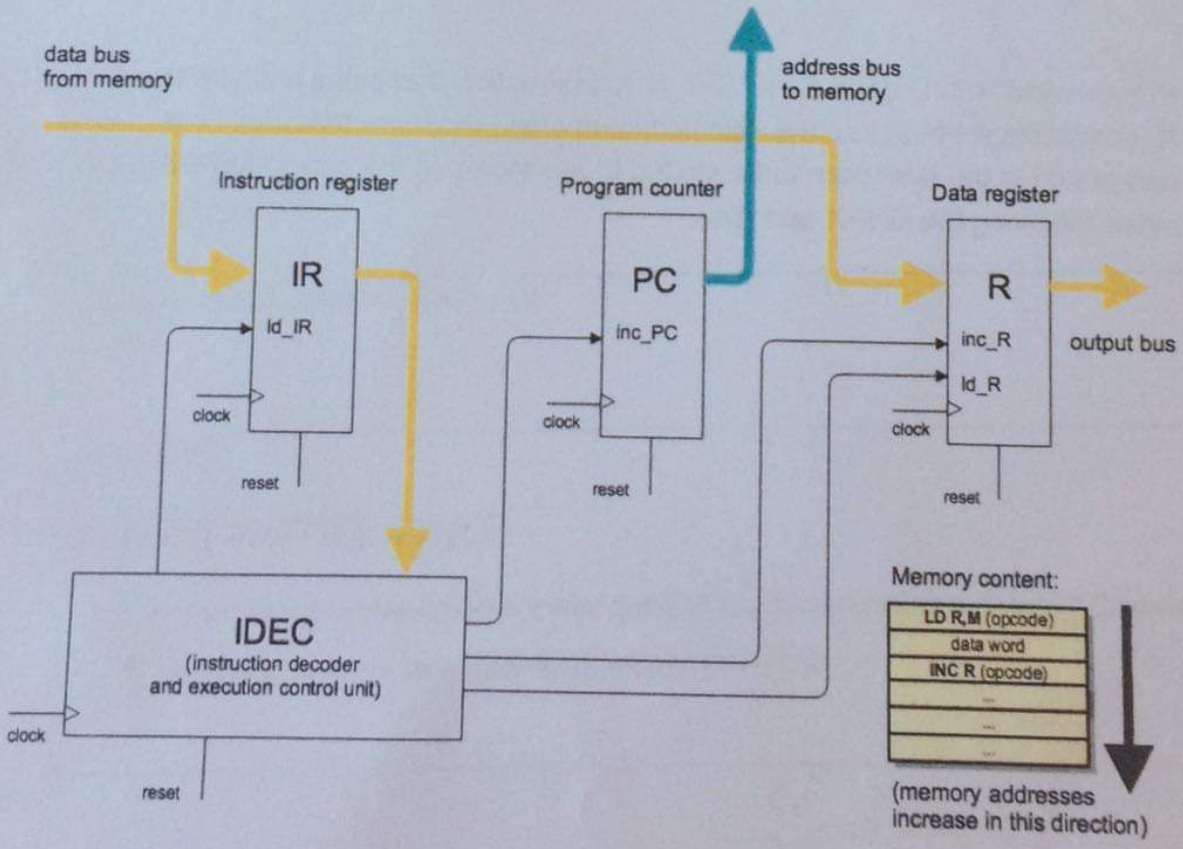
- The range of musical notes should cover octaves 4 (261.626 to 493.883 Hz) and 5 (523.251 to 987.767 Hz), and be represented by a set of corresponding ASCII codes according to any computer keys of your choice
- Each musical note is to be received through an RS232 serial channel and played as soon as it is received
- Each musical note will continue to play until another valid ASCII code is received (representing another musical note from octaves 4 or 5) or until an invalid ASCII code is received (in which case the music will stop)



1. What changes are required – if any – to the data path architecture presented ahead (in the following page) in order to meet the functional requirements presented above?
2. Present an ASMD chart for the corresponding control path.



9. D05q The block diagram shown ahead represents the minimum set of blocks required to implement a CPU (a FSMD architecture that is capable of executing a set of instructions stored in memory): i) an instruction register (IR) to hold the current instruction opcode; ii) a program counter (PC) to drive the address bus; iii) one data register (R); and iv) an instruction decode and execution control unit (IDEC). The data register, beyond storing one data word, is also able to increment it.

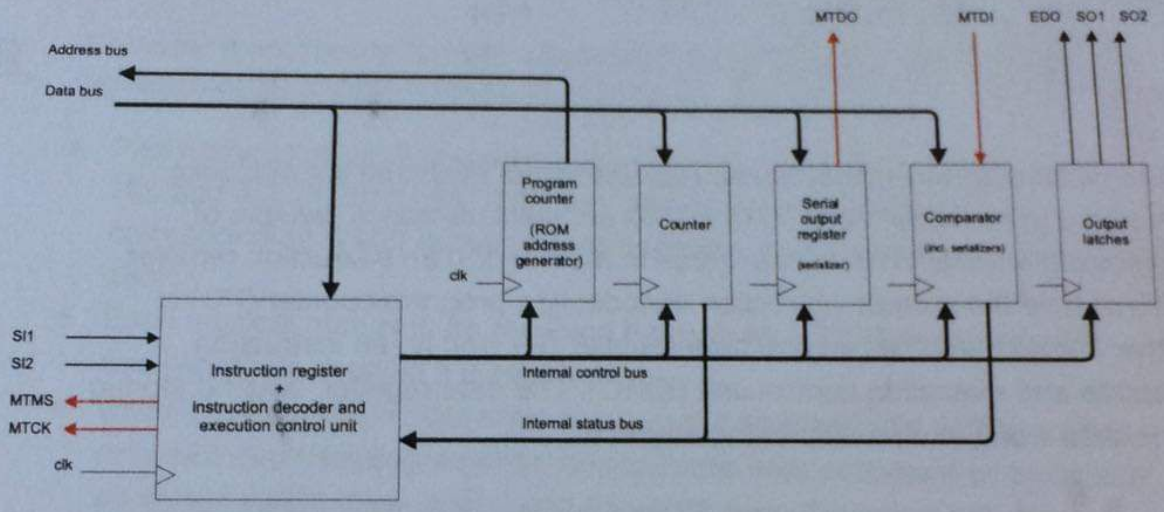


1. What changes are required in the architecture shown above, in order to support a JMP M instruction? (the first byte contains the JMP opcode,

the second byte contains the address – assume that the address bus and the data bus have the same width)

2. Present an ASMD chart for JMP M.

10. Consider the block diagram illustrated ahead, which represents one possible architecture for a dedicated BS controller designed as an application-specific CPU (MTDO, MTDI, MTMS and MTCK represent the "master" pins that connect to the board TAP).



Present and ASMD chart for a "SHF N X" instruction that shifts a bitstream X (comprising N bits) into the selected scan chain. Assume that the N bits comprised in the bitstream to be shifted in are stored in the ceiling_of(N/8) bytes following the SHFN opcode.