CMOS 2 Stage Comparator for Sensor Applications

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Abstract : This literature survey aims to identify a suitable and very simple application for 'Mixed Signal SoC design Marathon using eSim & SKY130'. The survey proposes a novel design for sensor applications. A comparator is planned to be designed and its output is used to drive a sensor. The sensor will indicate correctness of comparator output by driving an LED 'on' or 'off'. The sensor in this design will be a multiplexer which will drive the LED.

Keywords: CMOS, Mixed Signal, Multiplexer

I. Introduction

About Mixed Signal Design: The survey leading to this report yielded that mixed signal design is the most complex of all the VLSI fields. Many different references are studied for identifying mixed signal designs. The author of this paper ended up with the following conclusions.

1. Conference and journal papers: The materials observed work on large digital designs with a part of the design improved by custom analog designs. The works are highly complex and hence not referred.
2. eSim : Previous marathons which were conducted have provided completed circuits. Amongst which most are either digital or analog. Few mixed designs are available but are completed successfully. These will help for practice and learning.
3. Commercial works : Referring to a few companies' works, mixed signal designs are of prime importance nowadays due to the advent of MEMS and SoC.

About the proposed design: Figure 1 shows the proposed implementation of the mixed signal design. A CMOS comparator which is designed in analog will drive a 2:1 Multiplexer which is designed in verilog.

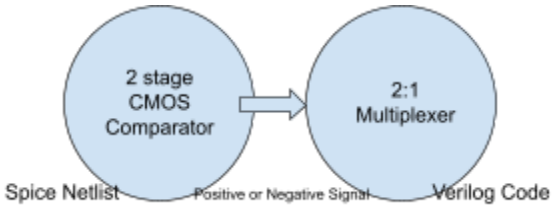

Fig 1: Proposed block diagram

The output of Multiplexer will drive a LED or indicate High or Low based on the eSim functionalities.

2 Stage CMOS comparator: Figure 2 shows a simple CMOS comparator.

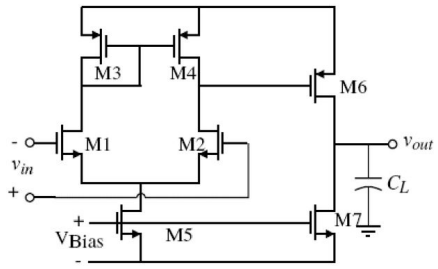

Fig 2: Comparator

2:1 Multiplexer: The multiplexer will be implemented using behavioral modeling.

II. Expected Results

Figure 3 shows the expected output from the CMOS comparator.

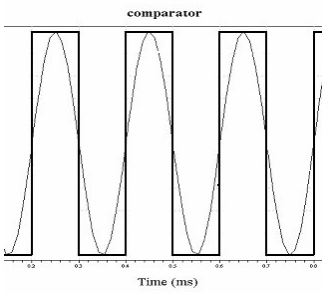

Fig 3: Output of CMOS comparator

The output is expected to work as input to a digital 2:1 multiplexer.

III. Conclusion

The proposed design seems fairly simple and easy. But the author intends to complete the marathon successfully with a good solid understanding of mixed signal design rather than getting stuck in either analog or digital part.

IV. Acknowledgements

Thanks to all the sponsors and coordinating TAs, industries and institutes.

IV. References

1. esim.fossee.in
2. https://www.vlsisystemdesign.com