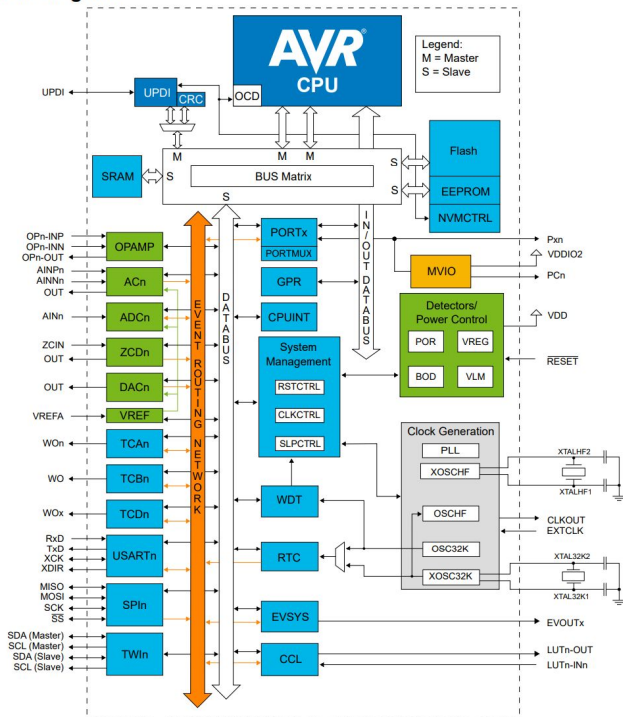


# Block Diagram

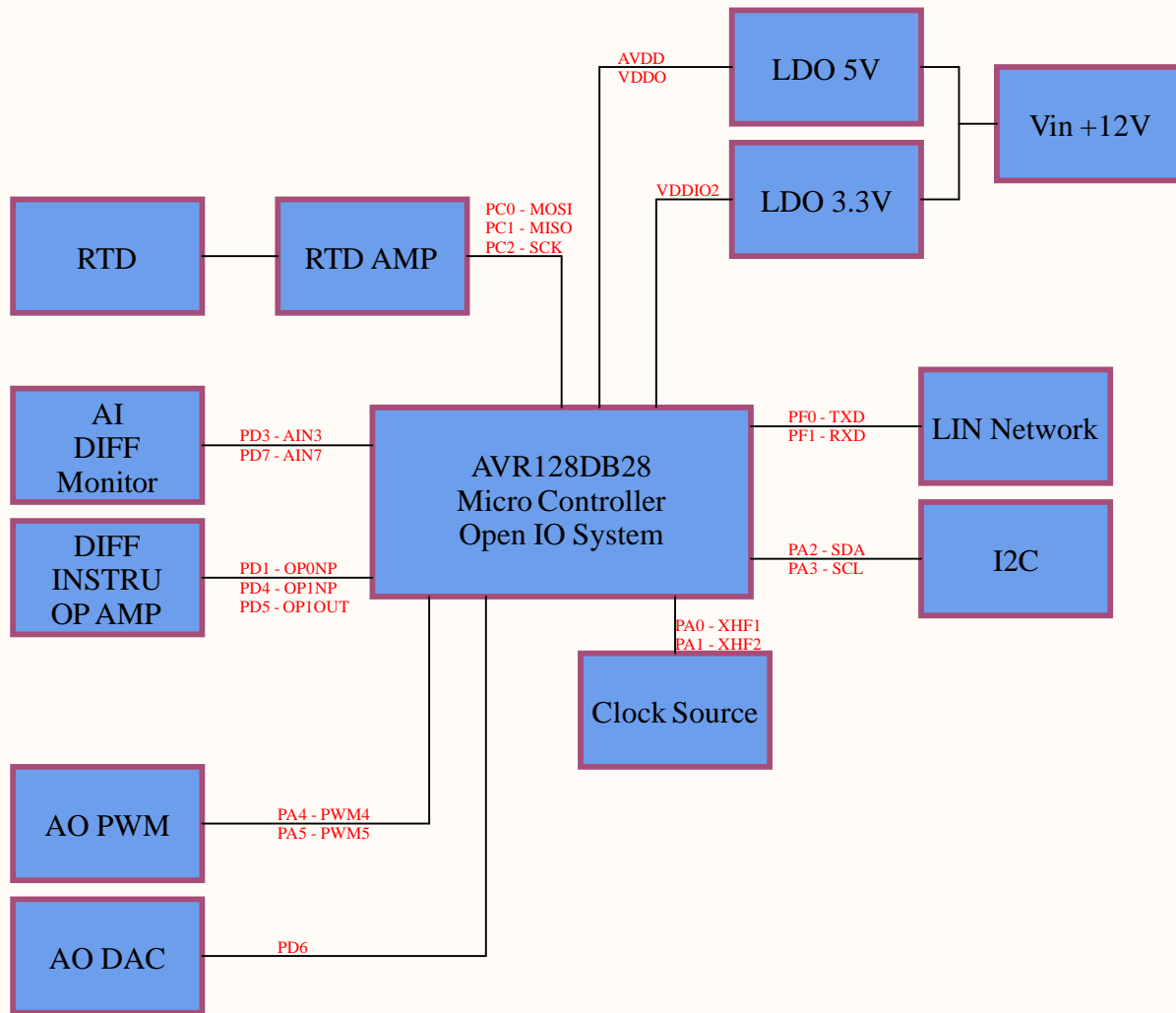


## 28-pin SSOP, SOIC and SPDIP

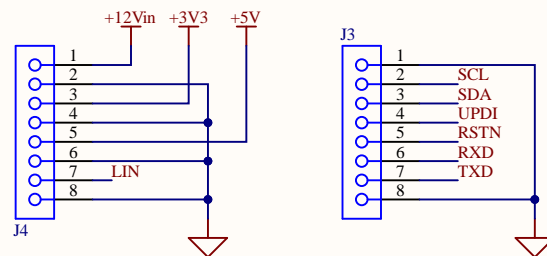
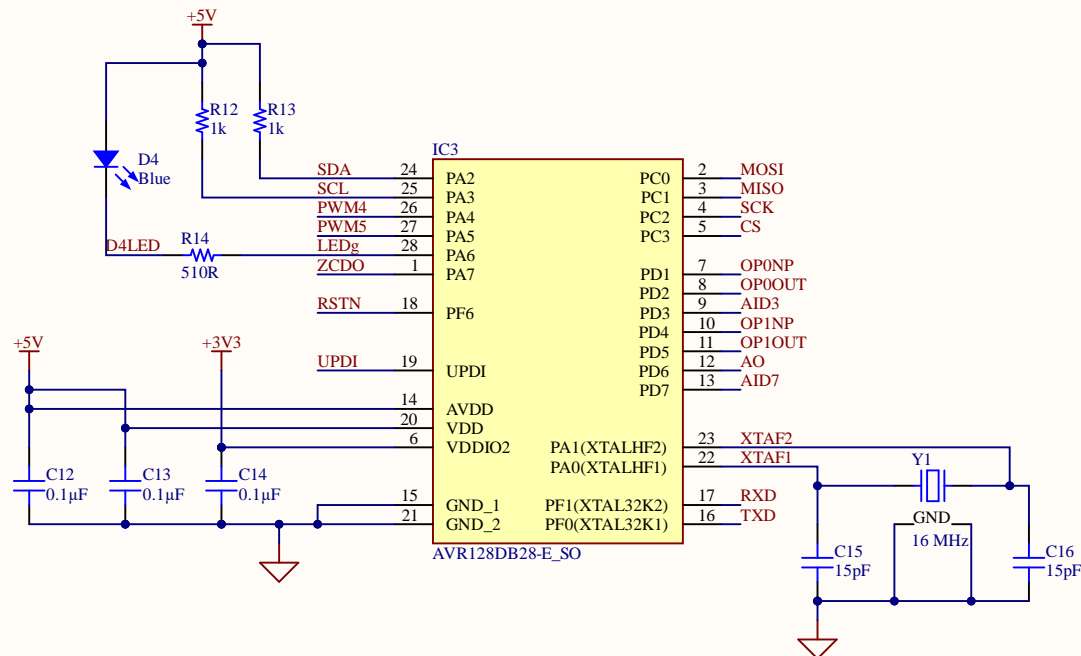
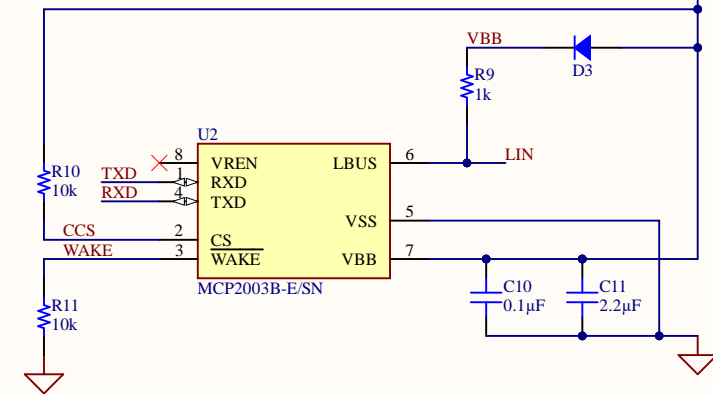
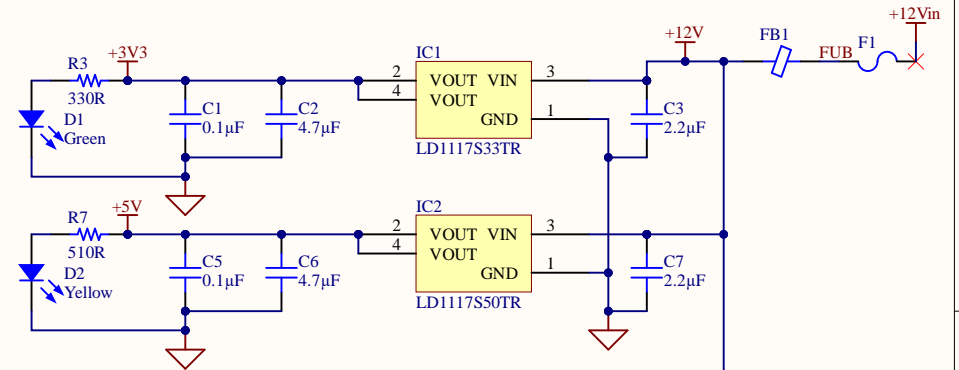
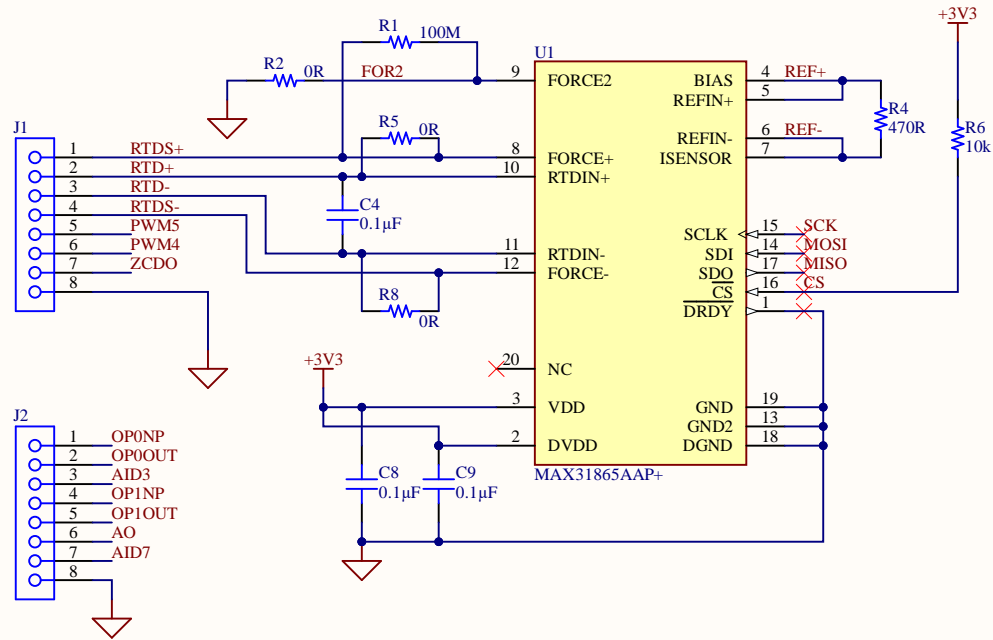
PA7	1	28	PA6
PC0	2	27	PA5
PC1	3	26	PA4
PC2	4	25	PA3
PC3	5	24	PA2
VDDIO2	6	23	PA1 (XTALHF2)
PD1	7	22	PA0 (XTALHF1)
PD2	8	21	GND
PD3	9	20	VDD
PD4	10	19	UPDI
PD5	11	18	PF6
PD6	12	17	PF1 (XTAL32K2)
PD7	13	16	PF0 (XTAL32K1)
AVDD	14	15	GND

Note: For the AVR® DBFamily of devices, AVDD is internally connected to VDD (not separate power domains).

Power	Functionality
Power Supply	Programming/Debug
Ground	Clock/Crystal
Pin on VDD Power Domain	Digital Function Only
Pin on AVDD Power Domain	Analog Function
Pin on VDDIO2 Power Domain	



Title: <b>Block Nano IO Board</b>			
PCB: <b>nanoRTDIOBoard.PrjPcb</b>			
Date: 27/08/2023	Rev: 01	Sheet: 1 Of 2	
Designer: vsbas	Checked: OK	Page A4	



Title: AVR DB IO BOARD			
PCB: nanoRTDIOBoard.PrjPcb			
Date: 27/08/2023	Rev: 01	Sheet: 2 Of 2	
Designer: vsbas	Checked: ok	Page A4	

