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# HIGHLY EFFICIENT LDMOS POWER AMPLIFIER BASED ON CLASS-E TOPOLOGY

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**ABSTRACT:** *This paper describes a highly efficient class-E power amplifier. The design has been carried out at 1 GHz using a LDMOS transistor with 10 W of peak envelope power (PEP). Drain efficiency of 76.1%, power-added efficiency (PAE) of 73.6%, and gain of 14.8 dB are achieved at an output power of 39.1 dBm for a continuous wave (CW) signal.* © 2006 Wiley Periodicals, Inc. Microwave Opt Technol Lett 48: 789–791, 2006; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.21476

**Key words:** *class E; packaging effect; harmonic filtering; PEP; PAE*

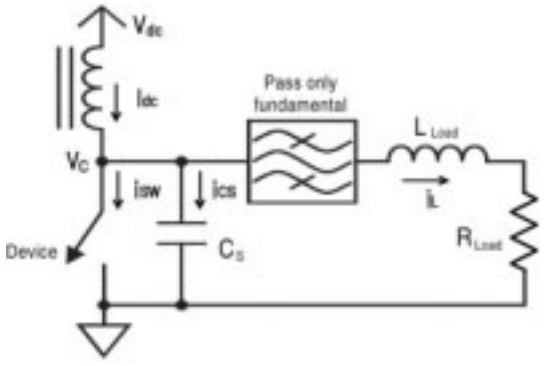



**Figure 1** Configuration of basic class-E amplifier

**TABLE 1 Class-E Design Parameters Using the Simplified Switch**

| $R_{Load}$ | $L_{Load}$ | $C_S$ [pF] | $C_{filter}$ [pF] |
|---|---|---|---|
| 25.60 | 29.49 | 1.14 | 0.51 |
| $V_{DC\_supply}$ [V] | | $P_{out\_want}$ [V] | $L_{filter}$ [nH] |
| 21.07 | | 10.00 | 50.00 |

## 1. INTRODUCTION

The efficiency of a power amplifier is directly connected with the thermal problem. As the efficiency becomes higher, the burden of heat sinking is lightened. And the volume and cost of the amplifier system can be reduced and the reliability of the system improved. High efficiency of an amplifier can be achieved by reducing the power dissipation of active devices and loss of an output network. The power dissipation in an active device can be minimized by eliminating the nonzero overlap of voltage and current waveforms. In a class-E amplifier, the transistor is operated as a switch to eliminate the overlap. The output network loss can be minimized by using a low-loss element such as a transmission line and employing a multisection matching for impedance transformation.

In this work, we have designed a highly efficient power amplifier based on the class-E topology using a commercially available LDMOS transistor. Parasitic elements of the device are compensated for proper class-E operation. For the implementation, the output network is implemented by transmission lines for the minimization of loss and suppression of harmonic power. Due to the structure optimization, we have achieved a state-of-the-art result from the class-E power amplifier.

## 2. DESIGN AND MEASUREMENT RESULTS

In the class-E amplifier shown in Figure 1, the active device is approximated by a switch [1]. If the switch does not have nonzero voltage and current simultaneously, the class-E amplifier does not dissipate any power in the active device. Such a condition can be satisfied by a proper selection of $C_S$, $L_{Load}$, and $R_{Load}$ [2, 3]. Based on the operation concept, we have designed a class-E amplifier. The transistor used in this work is a Motorola MRF282 LDMOS, which is able to deliver an output power of 10 W with 40% efficiency and 11.5-dB gain at 2 GHz for a single tone. The operation voltage of device is 26 V and the minimum breakdown voltage is 65 V.

For the initial test, a simulation using a simplified switch with $R_{on}$ of the transistor, which is 1.37Ω obtained from DC-IV of the device, has been carried out to extract the design param-

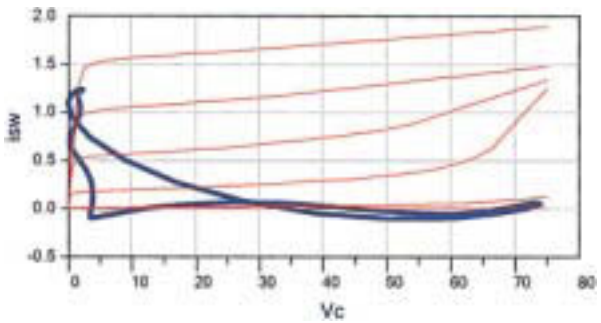



**Figure 2** Simulated load-line of a class-E amplifier using the simplified switch. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

**TABLE 2 Class-E Simulation Results Using the Simplified Switch**

| Drain Efficiency [%] | $P_{out}$ [W] | 2nd Harmonic [dBc] | 3rd Harmonic [dBc] |
|---|---|---|---|
| 92.32 | 8.71 | −27.55 | −42.26 |

eters at 1 GHz. The nonlinear simulation software ADS from Agilent is used. Table 1 shows the design parameters of the simplified amplifier obtained from the simulation. To deliver maximum power to the load, the voltage swing is adjusted to be limited by the breakdown voltage in simulation, as shown in Figure 2. The *LC* resonator is designed to suppress the harmonics. Table 2 shows the simulated results of the class-E amplifier using the switch with efficiency over 92%.

To design a real class-E amplifier from the extracted design parameters, the output capacitor of transistor should be matched to that of the simplified switch model used for the simulation. Output capacitor of MRF282 (j10.8Ω at drain voltage of 21.1 V and gate voltage of 3 V) is a lot higher than that of the switch with a shunt capacitor (j139Ω). Usually, a shunt inductor is used to compensate the output capacitance of the transistor [4]. But the compensation by the shunt inductor is not suitable due to the packaging effect of the commercially available LDMOS transistor. In this work, we employ a series capacitor for compensation of the packaging effect and a shunt inductor for compensation of the output capacitor, as shown in Figure 3. It requires $C_{comp}$ = 27 pF and $L_{comp}$ = 3.67 nH. The *LC* resonator has the ability to suppress the harmonic power, but insufficiently, and hence we constructed an output network with a transmission line along with the resonator. Figure 4 is the output network for harmonic filtering and impedance transformation from a 50Ω load. The harmonic powers can be suppressed using λ/4 transmission-lines at each harmonic frequency from 2nd to 5th [5, 6]. As shown in Table 3, the harmonic impedances are practically open compared to the fundamental impedance. Figure 5 is a schematic of the designed class-E amplifier. Performances of the designed class-E amplifier are drain efficiency of 79.24%, PAE of 76.7%, and gain of 14.86 dB at an output power of 39.86 dB. The circuit is

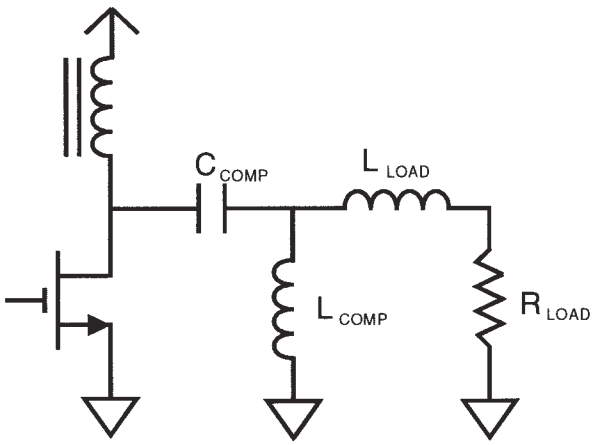



**Figure 3** Proposed schematic to compensate the parasitic elements of the device

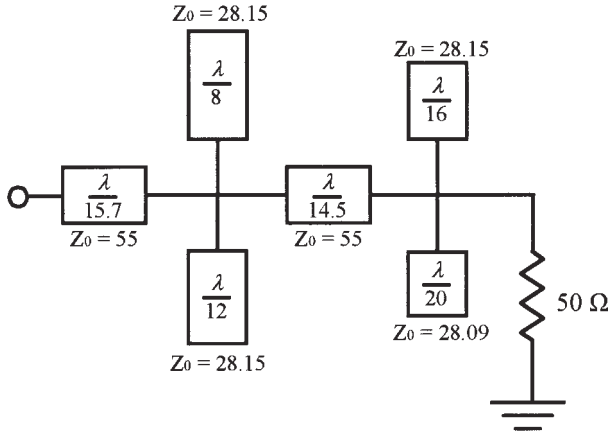



**Figure 4** Output network

implemented using an RF35 substrate; Figure 6 shows a photograph of the implemented class-E amplifier. Figure 7 shows the gain and efficiency of the amplifier at drain voltage of 21.4 V and gate voltage of 3.2 V for the CW signal. In the measurement, the threshold voltage of the device is slightly higher than that given by datasheet. The drain efficiency of 76.1%, PAE of 73.6%, and gain of 14.8 dB are measured at an output power of 39.1 dBm.

## 3. CONCLUSION

Based on a class-E topology, a highly efficient LDMOS power amplifier has been developed. The parasitic elements of device are compensated in order to achieve ideal class-E operation.

An output network was constructed using a transmission line for minimization of the circuit loss and suppression of harmonic power. The implemented amplifier designed for 1 GHz delivered drain efficiency of 76.1%, PAE of 73.6%, and gain of 14.8 dB at

**TABLE 3 Impedance of the Output Network at Each Harmonic**

| Frequency | $Z_{ds\_out}$ |
|---|---|
| 0.00 Hz | 50.00 + *j**0.00 |
| 1.00 GHz | 9.91 + *j**11.67 |
| 2.00 GHz | 0.36 + *j**91.23 |
| 3.00 GHz | 492.87 + *j**2.69E3 |
| 4.00 GHz | 1.63 + *j**46.88 |
| 5.00 GHz | 56.55 + *j**474.21 |

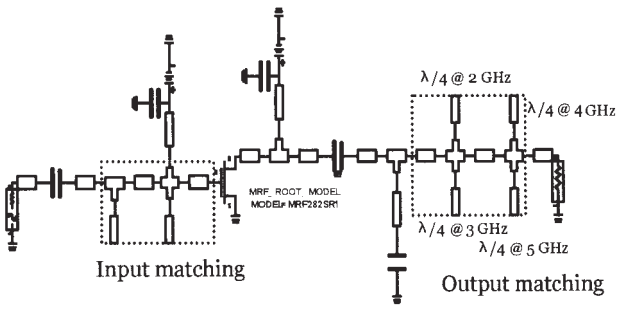
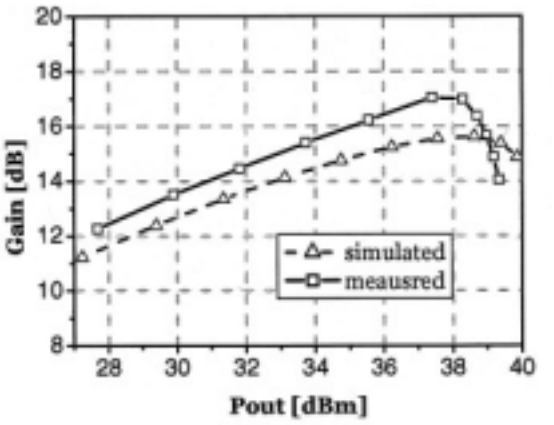


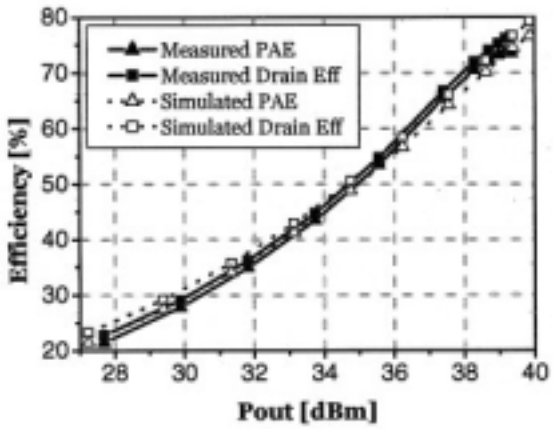

**Figure 5** Circuit schematic

**Figure 6** Photograph of the implemented amplifier using MRF282SR1. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

an output power of 39.1 dBm. This result is the highest efficiency ever reported for a class-E power amplifier at comparable operation conditions.




(a) Gain




(b) Efficiency

**Figure 7** Measured (a) gain and (b) efficiency


## ACKNOWLEDGMENT

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# OPTICAL FIBRE PPM USING A PIN-FET RECEIVER AND CENTRAL DECISION DETECTION


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**ABSTRACT:** *An analysis is presented, for the first time, for an optical fibre PPM system employing central decision detection. Firstly, an ideal matched filter in conjunction with a noise-whitening filter is considered and secondly a raised cosine filter to eliminate intersymbol interference is modelled. It is shown that the latter offers superior performance. The results for a 155.52 Mb/s system predict a sensitivity of −57.6 dBm, an improvement of 6 dB over an equivalent PCM system.* © 2006 Wiley Periodicals, Inc. Microwave Opt Technol Lett 48: 791–794, 2006; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.21477



**Key words:** *pulse position modulation; PIN-FET receiver; optical communications*


## 1. INTRODUCTION

Optical pulse position modulation systems (PPM) [1–4] normally use threshold-crossing techniques to establish the position of a pulse within a given time frame $T_f$ that is subdivided into a number of time-slots $n$ of duration $T_s$. In this coding scheme, $M$ bits of PCM are mapped on to the $n = 2^M$ time slots and, in order to maintain data throughput, this must be done at a rate of $T_f = MT_b$, where $T_b$ is the PCM bit duration.