A Novel Inverse Class E Power Amplifier

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Abstract: - A new inverse class E power amplifier circuit is proposed. Instead of using a bias choke, the bias current is fed through a resonating inductor of the output network. The circuit is particularly suitable for full integration, since removal of the bias choke removes some of the largest parasitic circuit elements of the output network. The new parasitic capacitances are not connected to signal nodes, and have at least one node connected to ground. The DC blocking capacitor is located between the amplifier output and the load, which allows it to be placed outside an integrated circuit. The DC block may be omitted, if it is acceptable to connect DC voltage to the load. The circuit is suitable for envelope modulation, and it is compatible with many known predistorting and efficiency enhancement methods.

Key-Words: - inverse class E power amplifier choke bias DC AC resonator

1 Introduction

In most mobile and portable battery-driven devices where a radio transmitter is used, the power amplifier is the dominating consumer of the battery capacity in the transmitting mode. Since the battery is often the largest and heaviest component of the device, improving the transmitter efficiency helps in designing it smaller and lighter. High transmitter efficiency is also important in fixed installations, since it helps in resolving the transmitter cooling problems.

To improve the available data transfer rate for the given channel bandwidth, many modern wireless systems employ simultaneous envelope and phase modulation. Therefore, it is important that the power amplifier is able to amplify signals with rapidly varying envelope without significant distortion, and is compatible with methods for reducing the distortion due to the non-idealities of the amplifier circuit. In some cellular telephone systems where constant envelope modulation is employed, the base station controls the RF output power of the portable terminal. In these applications, the terminal transmitter power must be controlled with good resolution.

While the classic class A, AB, B, and C amplifiers have many desirable properties, their modest efficiency or other performance limitations when operating under high efficiency conditions are known problems. All commonly known switching power amplifiers provide theoretically 100% efficiency. While this high efficiency is not possible to achieve in practice, in many applications switching amplifier circuits nevertheless provide superior efficiency, compared with the classic amplifier alternatives.

2 Class E Designs

2.1 Conventional Class E designs

The conventional class E switching amplifier [1] has some desirable properties for modern portable applications since it is suitable for envelope modulation and provides high efficiency. However, it has not become popular in wireless systems employing frequencies in the GHz region because of problems with the practical implementation.

One of the related problems is to

ISBN: 978-960-6766-79-4

ISSN 1790-5117

maintain the waveform shapes that are necessary for soft switching, in the presence of non-ideal switching transistor and parasitic circuit elements. While this problem is most often attributed to the non-idealities of the switching transistor, the output network is equally important.

Most class E power amplifier designs employ a bias choke inductor for providing the necessary bias current for the switching transistor. As long as the inductor is ideal, this bias arrangement works very well. However, a large bias inductor has in practice low self-resonance frequency due to the parasitic capacitances of the physical coil, bonding pads, etc. Since the current and voltage waveforms in the signal node of the choke include many harmonic frequency components, the bias choke resonances with its own parasitic elements and with the other components in the circuit may severely filter the internal waveforms of the amplifier, distorting the waveforms that are necessary for zero voltage switching. To mitigate this problem, it is possible to limit the number of harmonics in the waveforms [1], but this will result in partially overlapping current and voltage waveforms, which will degrade the efficiency.

In practice, the bias choke is often replaced with a smaller inductor [2], but in these cases some RF current is coupled through the inductor to the power supply connection node. This may cause unpredictable effects, since anything that is connected to this node may also affect the internal waveforms of the circuit. An inductor with a relatively small inductance may also resonate with the other capacitances of the circuit, close to the operating frequency or one of its harmonics.

2.2 Inverse Class E designs

One of the well-known problems of the conventional class E power amplifier is that the peak voltage across the switching device is quite high, 3.562 times the value of the DC supply voltage, assuming 180° conduction angle. Since the transistors in most modern integrated circuit fabrication processes do not stand much higher peak voltage than the nominal operating voltage, this clearly limits the suitability of the conventional class E circuits for integration with the other electronics.

One way to mitigate this problem is to move from the voltage domain to the current domain. An inverse class E design has been proposed [3] for addressing this and some other problems of conventional class E designs. In this circuit, shown in Fig. 1, the peak voltage across the switch is slightly lower, only 2.862 times the value of the DC supply voltage. The peak voltage across the resonator capacitor C1 is also much lower, but the peak current flowing in the resonator inductor L2 is correspondingly higher. Of course, these effects are consequences of replacing the serial resonator with a parallel resonator network in the output pulse shaping network.

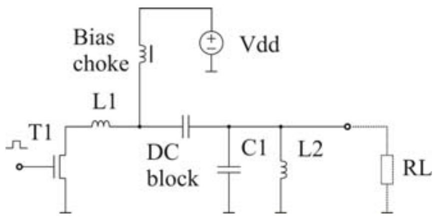

Fig.1 A prior art inverse class E power amplifier.

This circuit suffers from some drawbacks. Since the current and voltage waveforms are very complex, the bias choke should represent high impedance up to several harmonics of the operating frequency. As with the conventional class E circuit, the resonances of the bias choke may spoil the waveforms that are needed for maintaining the conditions for zero current switching. Another concern associated with this circuit in fully integrated implementations is that the parasitic back plate capacitance of the DC blocking capacitor is connected in parallel with C1. If the value of the parasite is comparable with the value of C1, it is difficult to avoid detuning of the resonance circuit. In most integrated circuit fabrication processes, the value of the parasitic back plate capacitance has much larger relative batch-to-batch variation than the value of the capacitor itself, and it does not correlate well with the values of the other capacitors on the same chip. Therefore, it is not possible to eliminate detuning by just absorbing the approximated value of the parasitic capacitance to the value of C1.

In conventional class E designs, it is easy to absorb the transistor's parasitic drain capacitance to one of the output network capacitors. This is not possible in inverse class E designs, since the output network does not have any capacitor in parallel with the switch. This implies that the switching transistor drain capacitance must be very small. Fortunately, the transistors in modern integrated circuits processes are developing to the direction where low drain-source capacitance is combined with low on-state channel resistance. An 870 MHz inverse class E amplifier with 93% power added efficiency has been reported [3], which indicates that the parasitic drain capacitance is not necessarily a major problem.

3 A New Inverse Class E Power Amplifier

The proposed inverse class E amplifier is shown in Fig. 2. This circuit is obtained from the circuit of Fig. 1 by removing the bias choke, moving the DC blocking capacitor to the output, connecting the DC power supply to the lower end of the resonator inductor L2, and bypassing the supply with a large capacitor C2.

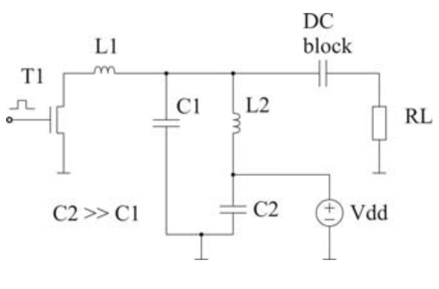

Fig.2 The new inverse class E power amplifier circuit.

Even though the bias arrangements are quite different, the two circuits produce similar AC waveforms. However, the modifications of the output network bring some benefits. Since the DC bias choke was removed, a major source of parasitic resonances in the output network signal path was removed. Since C2 is not connected to any node that is carrying a spectrally rich voltage signal, and since at least one of its plates is connected to ground, the parasitic back plate capacitance of C2 does not disturb the circuit operation. In addition, the value of C2 is not very critical, since the values of C1 and L2 will mostly determine the resonance frequency of the parallel resonator network. As long as C2>>C1, the design equations published in [5] may be used. In the more practical case where C2 is not very much larger than C1, the value of C1 must be increased slightly.

The value of the bypass capacitor C2 should be large, compared with C1. Firstly, C2 should keep the impedance of the path from the lower end of L2 to the bottom plate of C1 low at the operating frequency and its harmonics, in order to close the current path of the parallel resonator C1-L2. Secondly, C2 should short any interfering AC signal trying to enter the parallel resonator through the power supply line, in order to avoid undesired modulation. Obviously, the value of C2 depends on the lowest frequency component of the expected interfering signal entering the circuit through the power supply line.

Yet another advantage of this circuit is that the DC block is not located between the resonance circuit and the switch, but moved to the output. The DC block does not isolate the transistor switch from the output network at low frequencies. Therefore, the small-signal voltage gain of the transistor is kept low at all frequencies outside the pass band of the resonator, which will help in preventing oscillation. Since the parasitic capacitances of the DC block are now next to the load, they may be absorbed to a simple impedance matching network placed between the output and the load.

As with all class E amplifiers, the only reference voltage of the output network is the supply voltage. Therefore, this circuit is compatible with envelope modulation methods employing power supply modulation.

One of the problems of this design is that the resonance inductor L2 has to carry the DC current, in addition to the AC current. In a fully integrated circuit, it is necessary to take into account that the spiral inductor metals are able to handle this current density. This may make the size of L2 considerably larger than is necessary for just obtaining the needed inductance. Another problem is that C2 is assumed to be very large, compared with C1. In practice, C2 may be composed of two capacitors, one of them residing outside the integrated circuit. Alternatively, C2 may be replaced with some other network that provides the low impedances at the desired frequencies.

4 Conclusion

A new inverse class E power amplifier topology is described for the first time. The advantages and disadvantages of the circuit are discussed, and compared with a prior art circuit. The benefits of the new amplifier topology are related to the lack of the bias choke, and the placement of the DC blocking element between the output of the amplifier and the load. Previously published design equations may be used for finding the circuit element values. Employing modern IC technologies, the circuit seems to be very suitable for full integration.

The circuit described in this paper is the subject of a UK patent application, filed in 2nd of June, 2008, by the author.

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