Series-L/parallel-tuned comparison with shunt-C/series-tuned class-E power amplifier

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Abstract: An analysis of the operation of a series-L/parallel-tuned class-E amplifier and its equivalence to the classic shunt-C/series-tuned class-E amplifier are presented. The first reported closed form design equations for the series-L/parallel-tuned topology operating under ideal switching conditions are given. Furthermore, a design procedure is introduced that allows the effect that nonzero switch resistance has on amplifier performance efficiency to be accounted for. The technique developed allows optimal circuit components to be found for a given device series resistance. For a relatively high value of switching device ON series resistance of 4 Ω, drain efficiency of around 66% for the series-L/parallel-tuned topology, and 73% for the shunt-C/series-tuned topology appear to be the theoretical limits. At lower switching device series resistance levels, the efficiency performance of each type are similar, but the series-L/parallel-tuned topology offers some advantages in terms of its potential for MMIC realisation. Theoretical analysis is confirmed by numerical simulation for a 500 mW (27 dBm), 10% bandwidth, 5 V series-L/parallel-tuned, then, shunt-C/series-tuned class E power amplifier, operating at 2.5 GHz, and excellent agreement between theory and simulation results is achieved. The theoretical work presented in the paper should facilitate the design of high-efficiency switched amplifiers at frequencies commensurate with the needs of modern mobile wireless applications in the microwave frequency range, where intrinsically low-output-capacitance MMIC switching devices such as pHEMTs are to be used.

1 Introduction

The class-E power amplifier (PA) is a highly nonlinear amplifier, introduced by Sokal in 1975 [1]. Being a switching power amplifier, it has higher efficiency at high output power levels than a conventional linear power amplifier. Theoretically (using an ideal switch), the efficiency of a class-E amplifier can reach 100%, due to the fact that nonzero values of switch voltage and current do not occur simultaneously, leading to zero power dissipation within the switch.

Most of the class E power amplifier configurations, which have been published to date, can be classified based on the type of load networks used, namely:

(i) shunt-capacitor/series-tuned with an ideal RF choke/DC feed [1–3] (see Fig. 1*a*),

(ii) no-shunt-capacitor/series-tuned with a finite DC feed inductance [4–8] (see Fig. 1*b*),

(iii) shunt-capacitor/series-tuned with a finite DC feed inductance [9–12],

(iv) series-capacitor/parallel-tuned with an ideal RF choke [3].

In this paper, we present an exact analysis of a class E configuration with a series-inductor/parallel-tuned circuit, Fig. 1*c*. In [3] a brief mention of a series-L/parallel-tuned class E amplifier was made, and a complicated topology for it, requiring the use of a transformer, was suggested; no attempt at analysis was given. We have been unable to find any other reference to this type of topology, or to its operating characteristics. While the first and third configurations mentioned here require zero-voltage switching (ZVS) and zero-voltage slope switching, the second and the new proposed configuration require zero-current switching (ZCS) and zero-current slope switching, as will be described later in this paper.

The series-L/parallel-tuned class-E amplifier (provisionally classified as 'voltage-driven' in [13]), Fig. 1*c*, was successfully implemented using a 6×50 μm pHEMT device in [13]. However, a closed equation means to compute the circuit component values for this circuit topology was not presented. In this paper, we rectify that situation and we explore the equivalences between the new proposed series-L/parallel-tuned topology and the most commonly used topology, i.e. shunt-C/series-tuned.

Introducing nonzero ESR (electrical series resistance) of the transistor into the circuit will degrade amplifier efficiency and also alter the ideal component values required for nominal operation for a given ESR. Furthermore, the new optimum values of the circuit elements required for nonzero switch resistance class-E amplifiers cannot be calculated straightforwardly, but must be computed using an iterative procedure such as that reported in [14] for a shunt-C/series-tuned class-E amplifier. In [14] the value of the ON resistance up to 0.5 Ω of the high-frequency three-terminal devices considered is too optimistic even for the advanced technology transistors currently available. In practice, values of around 2–3 Ω are more typical. In this paper, we will consider the effect that relatively high ON resistance, up to 4 Ω, has on both shunt-C/series-tuned and

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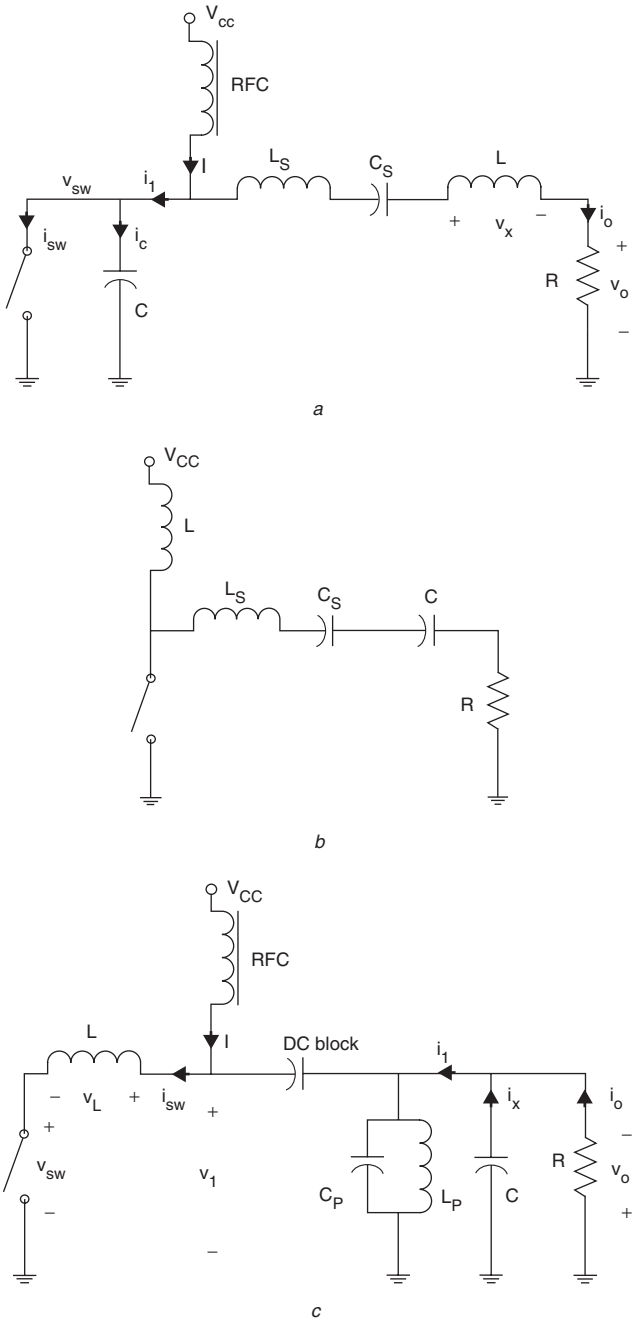

Fig. 1 *Class-E amplifier topologies*
a Shunt-C/series-tuned with an ideal RFC
b No-shunt-C/series-tuned with a finite DC Feed inductance
c Series-L/parallel-tuned

series-L/parallel-tuned amplifier performance. In [13] the authors suggested that the series-L/parallel-tuned topology, when compared to the classic shunt-C/series-tuned class-E PA, should be less sensitive in terms of efficiency to the channel resistance; no attempt at analysis was given to justify or to refute that suggestion.

2 Theory

Figure 1*c* depicts the circuit schematic diagram of the series-L/parallel-tuned class-E amplifier; the transistor is over-driven such that it behaves as a switch. Its switching action stimulates an oscillation in the parallel LC resonator, thus forcing a sinusoidal voltage (v_o) across the load resistance R. On the other hand, the RF choke (RFC) forces DC input signals (i.e. DC input voltage (V_{cc}) and DC input current (I)). The difference between output voltage v_o and DC input voltage V_{cc} must be dropped either across the switch (v_{sw}) or across the series inductor (v_L). When the switch is ON, switch current (i_{sw}) flows, the series inductor L is charged, and the nonzero voltage v_L appears across it. When the switch is OFF, the voltage drops across the switch.

While the excess reactance of the shunt-C/series-tuned topology is inductive, a capacitive reactance is required in the series-L/parallel-tuned topology, Fig. 1*c*, to compensate the phase angle error of the fundamental current flowing through the resistive load. The DC block is used in the circuit to prevent inductance L_p from shorting the bias voltage and also to isolate the DC supply from the output RF signal.

To simplify the analysis of the series-L/parallel-tuned circuit, it is necessary to make certain assumptions:

1. The transistor is modelled as a switch with ideal instant switching action, presenting a short circuit when ON, and an open circuit when OFF.
2. The switch is operated with the 50% duty cycle at the carrier frequency.
3. The switch can sustain the current running through it in the ON state and also must be able to withstand the non-zero voltage that appears across it during the OFF state.
4. The RF choke (RFC) has an infinite inductance and accordingly allows only DC current to flow through it. The DC block has an infinite capacitance and, as the result, only RF current can pass through it.
5. The Q-factor of the parallel LC resonator is high enough so that the output voltage is essentially sinusoidal at the carrier frequency.

Consequently, the output voltage and current are sinusoidal and are defined as

$$v_o(\theta) = V_{cc} \cdot a \cdot \sin(\theta + \varphi) \tag{1}$$

$$i_o(\theta) = V_{cc} \cdot G \cdot a \cdot \sin(\theta + \varphi) \tag{2}$$

where θ is 'angular time' ωt ($\omega = 2\pi f_o$; f_o is the fundamental frequency), φ is the phase angle of the output signal, V_{cc} is a DC input voltage, and G is the load conductance. Parameters a and φ are yet to be determined.

From Fig. 1*c*, $v_1(\theta)$ can be expressed as

$$v_1(\theta) = V_{cc} - v_o(\theta) = V_{cc}(1 - a \cdot \sin(\theta + \varphi)) \tag{3}$$

The switch is closed during the first half-cycle ($0 < \theta < \pi$) and then is opened during the second half cycle ($\pi < \theta < 2\pi$). Integrating $v_1(\theta)$ from 0 to θ results in the switch current given by

$$i_{sw}(\theta) = \frac{1}{\omega \cdot L} \cdot \int_0^{\theta} v_1(\theta)\, \mathrm{d}\theta \tag{4}$$

Nonzero switch current is present when the switch is closed, while a nonzero switch voltage exists when the switch is opened:

$$i_{sw}(\theta) = \begin{cases} \dfrac{V_{cc}}{\omega \cdot L} \cdot (\theta + a \cdot \cos(\theta + \varphi) - a \cdot \cos(\varphi)) & \text{if } 0 < \theta < \pi \\ 0 \quad \text{if} \quad \pi < \theta < 2\pi \end{cases} \tag{5}$$

$$v_{sw}(\theta) = \begin{cases} 0 \quad \text{if } 0 < \theta < \pi \\ V_{cc} \cdot (1 - a \cdot \sin(\theta + \varphi)) \quad \text{if } \pi < \theta < 2\pi \end{cases} \tag{6}$$

The optimum operation of a class-E amplifier is reached when zero-current switching and zero-current slope switching conditions given respectively by (7) and (8) are fulfilled:

$$\left.\frac{\mathrm{d}i_{sw}}{\mathrm{d}\theta}\right|_{\theta=\pi} = 0 \tag{7}$$

$$i_{sw}(\pi) = 0 \tag{8}$$

The parameters a and φ can be obtained upon using (7) and (8):

$$a = \sqrt{\frac{\pi^2}{4}+1} \tag{9}$$

$$\varphi = \tan^{-1}\left(\frac{-2}{\pi}\right) \tag{10}$$

In the time domain the switch current can be expressed in the form of a Fourier series as follows:

$$i_{sw}(t) = I + \sum_{n=1}^{\infty}(a_{in}\cdot\cos(2\cdot\pi\cdot n\cdot f_o\cdot t+\varphi) + b_{in}\cdot\sin(2\cdot\pi\cdot n\cdot f_o\cdot t+\varphi)) \tag{11}$$

At the fundamental frequency (f_o), we can write (11) as

$$i_1(\theta) = a_{i1}\cdot\cos(\theta+\varphi)+b_{i1}\cdot\sin(\theta+\varphi) \tag{12}$$

where a_{i1} and b_{i1} are defined as

$$a_{i1} = \frac{1}{\pi}\cdot\int_0^{\pi} i_{sw}(\theta)\cdot\cos(\theta+\varphi)\mathrm{d}\theta \tag{13}$$

$$b_{i1} = \frac{1}{\pi}\cdot\int_0^{\pi} i_{sw}(\theta)\cdot\sin(\theta+\varphi)\mathrm{d}\theta \tag{14}$$

From which we compute a_{i1} and b_{i1}:

$$a_{i1} = \frac{1}{\pi}\cdot\frac{V_{cc}}{\omega\cdot L}\cdot\left(-2\cdot\cos(\varphi)-\sin(\varphi)\cdot\pi + a\sin(2\varphi)+\frac{1}{2}\cdot a\cdot\pi\right) \tag{15}$$

$$b_{i1} = \frac{1}{\pi}\cdot\frac{V_{cc}}{\omega\cdot L} \times(-2\cdot\sin(\varphi)+\cos(\varphi)\cdot\pi-2\cdot a\cdot\cos^2(\varphi)) \tag{16}$$

On the other hand, from Fig. 1*c*, it is evident that

$$i_x(\theta) = V_{cc}\cdot B\cdot a\cdot\cos(\theta+\varphi) \tag{17}$$

$$i_1(\theta) = i_o(\theta)+i_x(\theta) \tag{18}$$

Then, from (2), (9), (10), (12), (15), (16), (17), and (18), we obtain

$$G\cdot X = \frac{8}{\pi\cdot(\pi^2+4)} \tag{19}$$

$$B\cdot X = \frac{\pi^2-4}{2\cdot(\pi^2+4)} \tag{20}$$

where $X = \omega L$ and $B = \omega C$. Dividing (19) with (20), we obtain

$$B = G\cdot\frac{\pi\cdot(\pi^2-4)}{16} \tag{21}$$

The DC term I in (11) is defined by

$$I = \frac{1}{2\pi}\cdot\int_0^{\pi} i_{sw}(\theta)\mathrm{d}\theta = \frac{1}{2\pi}\cdot\frac{V_{cc}}{\omega\cdot L}\cdot\left(\frac{\pi^2}{2}-2\cdot a\cdot\sin(\varphi)-a\cdot\pi\cdot\cos(\varphi)\right) \tag{22}$$

As $I = V_{cc}G_{dc}$ (G_{dc} is the conductance that the amplifier presents to the power supply), then by substituting (9) and (10), we can simply write G_{dc} as follows:

$$G_{dc} = \frac{1}{\pi\cdot X} \tag{23}$$

However, it is more convenient to express G_{dc} as a function of G, thus, substituting (19) into (23), results in

$$G_{dc} = \frac{\pi^2+4}{8}\cdot G \tag{24}$$

The peak output voltage and current can be expressed as a function of the input DC voltage (V_{cc}) and the input DC current (I), respectively,

$$V_{o_{pk}} = \frac{\sqrt{\pi^2+4}}{2}\cdot V_{cc} \tag{25}$$

$$I_{o_{pk}} = \frac{4}{\sqrt{\pi^2+4}}\cdot I \tag{26}$$

The drain efficiency of an ideal class-E power amplifier is then given by

$$\eta = \frac{P_o}{P_{dc}} = \frac{(V_{o_{pk}}\cdot I_{o_{pk}})/2}{V_{cc}\cdot I} = 1 \tag{27}$$

The peak values of the switch voltage (v_{sw}) and the switch current (i_{sw}) are important parameters in a practical design, i.e. these enable the designer to choose an appropriate active device which can sustain the maximum current running through it, when it is ON, and cope with the nonzero voltage that appears across it, in the OFF state,

$$V_{sw_{pk}} = (1+a)\cdot V_{cc} \tag{28}$$

this situation occurs at

$$\theta_v = \frac{3\pi}{2}-\varphi \tag{29}$$

$$I_{sw_{pk}} = (-2\cdot\varphi\cdot\pi)\cdot I \tag{30}$$

which occurs at

$$\theta_i = -2\cdot\varphi \tag{31}$$

In practice, when designing a power amplifier we require a specific output power (P_o), for a given input DC voltage or current (V_{cc}, I), at a specified operating frequency (f_o). Hence, it would be best to express these equations as a function of these parameters:

$$L = \frac{V_{cc}^2}{P_o\cdot\pi\cdot\omega} \tag{32}$$

$$C = \frac{P_o}{V_{cc}^2\cdot\omega}\cdot\frac{\pi\cdot(\pi^2-4)}{2\cdot(\pi^2+4)} \tag{33}$$

$$G = \frac{P_o}{V_{cc}^2}\cdot\frac{8}{\pi^2+4} \tag{34}$$

The next step is to determine the value of L_p and C_p of the parallel resonator tank. Having computed the load

conductance G and on setting a predetermined value for Q_{LC} as well as the operating frequency f_o, L_p and C_p can be calculated as follows:

$$C_p = Q_{LC} \cdot G/\omega \tag{35}$$

$$L_p = 1/(\omega^2 \cdot C_p) \tag{36}$$

These formulas allow us to determine the circuit elements of an ideal series-L/parallel-tuned class-E power amplifier. Table 1 shows the equivalence between the classical ideal shunt-C/series-tuned topology [2, 3] and the series-L/parallel-tuned topology described here.

Table 1: Circuit component equivalences

Circuit component	*shunt-C/series-tuned	**series-L/parallel-tuned
C	$\frac{P_o}{\pi \cdot \omega \cdot V_{cc}^2}$	$\frac{\pi \cdot (\pi^2 - 4)}{2 \cdot (\pi^2 + 4)} \cdot \frac{P_0}{\omega \cdot V_{cc}^2}$
R	$\frac{8}{\pi^2 + 4} \cdot \frac{V_{cc}^2}{P_o}$	$\frac{\pi^2 + 4}{8} \cdot \frac{V_{cc}^2}{P_o}$
L	$\frac{\pi \cdot (\pi^2 - 4)}{2 \cdot (\pi^2 + 4)} \cdot \frac{V_{cc}^2}{\omega \cdot P_o}$	$\frac{V_{cc}^2}{\pi \cdot \omega \cdot P_o}$
C_s* or C_p**	$\frac{1}{\omega \cdot Q_{LC} \cdot R}$	$\frac{Q_{LC}}{\omega \cdot R}$
L_s* or L_p**	$\frac{1}{\omega^2 \cdot C_s}$	$\frac{1}{\omega^2 \cdot C_p}$

3 Comparison of Ideal shunt-C/series-tuned and series-L/parallel-tuned Class-E Topologies

To verify the theoretical analysis described in Section 2, the design example of a 500 mW, 5 V class E power amplifier, operating at 2.5 GHz and having 10% bandwidth ($Q_{LC} = 10$), is given here. The values for the circuit elements for both topologies in Fig. 1*a* and *c*, computed based on the equations in Table 1, are presented in Table 2. The active device is modelled as a switch which has 0.01 Ω ON resistance (used because the ADS simulation algorithm of the switch component does not allow 0 Ω ON resistance) and 10 kΩ OFF-state impedance. Simulation results are shown in Fig. 2.

Table 2: Component values of design example of 500 mW, 5 V, 2.5 GHz, 10% bandwidth, class-E amplifier

Circuit component	*shunt-C/series-tuned	**series-L/parallel-tuned
C	0.4 pF	0.85 pF
R	28.8 Ω	86.7 Ω
L	2.1 nH	1 nH
C_s* or C_p**	0.22 pF	7.34 pF
L_s* or L_p**	18.4 nH	0.55 nH

The peak values of output voltage ($V_{o_{pk}}$), output current ($I_{o_{pk}}$), switch voltage ($V_{sw_{pk}}$) and switch current ($I_{sw_{pk}}$) are computed using (25), (26), (28), and (30), respectively, and then compared to the simulation results (see Table 3). Included also in Table 3 are the equivalent results for the classic shunt-C/series-tuned topology. Excellent agreement between the theoretical analysis and the simulation results has been obtained. For the particular design example presented in this paper, a large inductor ($L_s + L$), 20.5 nH, and capacitor ($C_p + C$), 8.19 pF, are required, respectively, in the shunt-C/series-tuned and series-L/parallel-tuned topologies (see Table 2). In an MMIC implementation, a large inductor generally consumes more area than a large capacitor, which makes the series-L/parallel-tuned configuration more attractive in terms of implementation simplicity. Moreover, the large parasitic series resistance associated with this inductance will lead to deterioration in the operation of the amplifier. In addition, the parasitic series inductance of the active device transistor can be absorbed by the series L element in the series-L/parallel-tuned topology. This is not possible in the shunt-C/series-tuned topology. From Table 3, it can be observed that the active device used as a switch must be able to sustain more ON-state current in the series-L/parallel-tuned topology and more OFF-state voltage in the shunt-C/series-tuned topology, while the peak dissipation power within the switch is about the same for both topologies.

4 Effect of parasitic ON resistance

Using an ideal switch, a class-E power amplifier can offer 100% efficiency, as discussed in Section 3. However, in practice, nonideal switching action, performed by the active device having nonzero ON resistance, causes efficiency degradation of the amplifier. The channel resistance of the active device, which is the core topic of this Section, decreases efficiency, because when the switch is closed, a nonzero switch voltage (v_{sw}) occurs simultaneously with a nonzero switch current (i_{sw}), leading to power dissipation within the switch. To minimise efficiency degradation it is required that the transistor must have low channel resistance. In [14, 15] the influence of ON resistance on shunt-C/series-tuned amplifier performance was reported. We now give the first closed-form losses analysis of the effect of ON resistance in a series-L/parallel-tuned class-E amplifier.

Consider now Fig. 3, where the parasitic inductance of the transistor (L_{sw}) can be absorbed by the series inductor (L'). The parasitic resistance of the series inductor (r_L') in conjunction with the ON channel resistance of the transistor (R_{ON}) will degrade the amplifier's efficiency. By defining $r = R_{ON} + r_L'$ and $L = L' + L_{sw}$, the influence of r on the class-E amplifier's performance will now be investigated. In the s-domain, the switch current can be expressed as

$$I_{sw}(s) = \frac{V_1(s)}{s \cdot L + r} \tag{37}$$

Applying a Laplace transformation to (3) and substituting the result into (37);

$$I_{sw}(s) = \frac{s^2 \cdot V_{cc} \cdot (1 - a \cdot \sin(\varphi)) - s \cdot V_{cc} \cdot a \cdot \omega \cdot \cos(\varphi) + V_{cc} \cdot \omega^2}{s \cdot (s^2 + \omega^2) \cdot (s \cdot L + r)} \tag{38}$$

On transforming (38) back to the time-domain we obtain

$$i_{sw}(\theta) = \frac{V_{cc}}{r} \cdot \left(1 - \exp\left(\frac{-\theta}{Q}\right)\right) + \frac{V_{cc} \cdot a}{Z} \cdot \sin(\varphi - \beta) \times \exp\left(\frac{-\theta}{Q}\right) - \frac{V_{cc} \cdot a}{Z} \cdot \sin(\theta + \varphi - \beta) \tag{39}$$

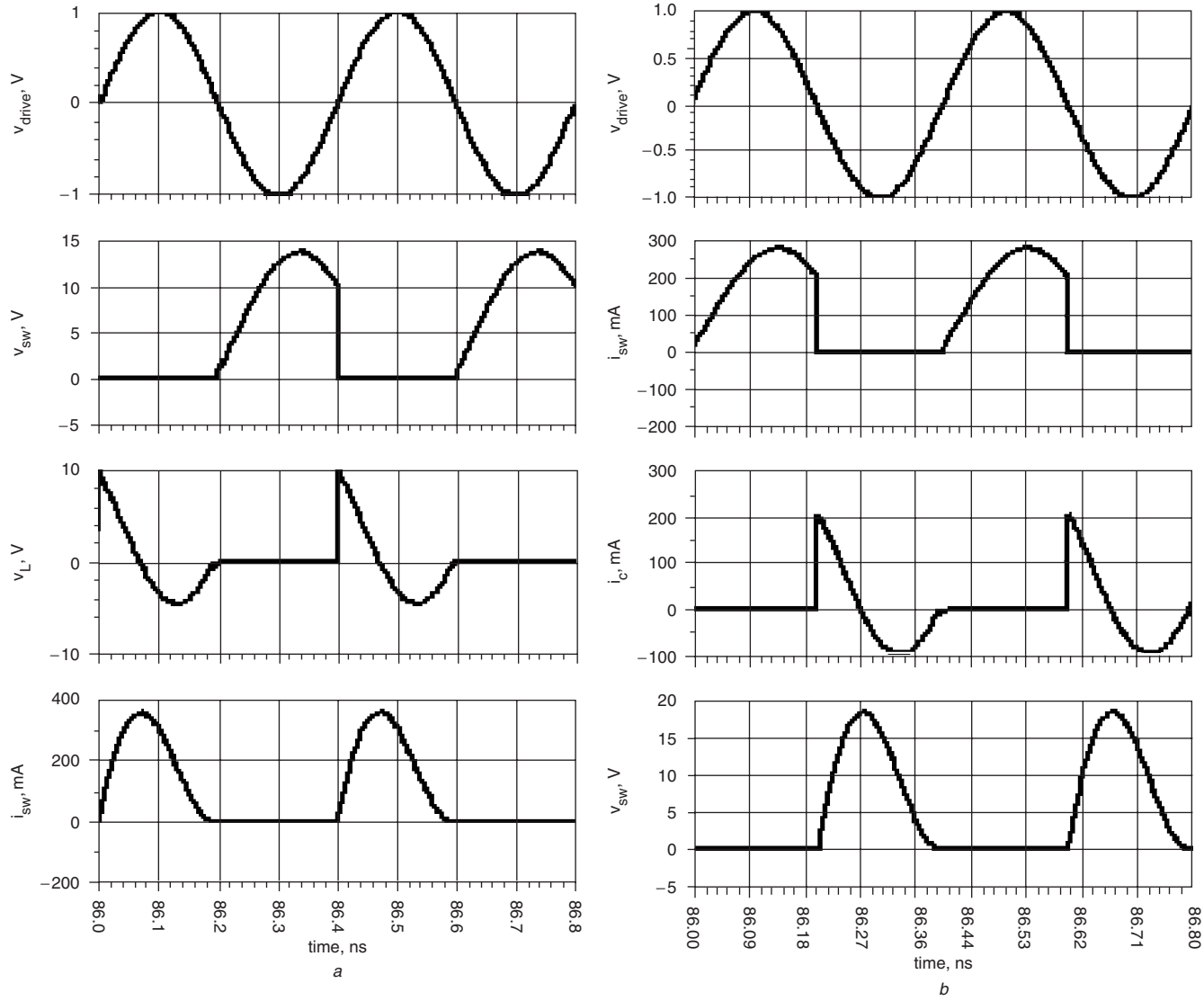

Fig. 2 *Current and voltage waveforms*
a Series-L/parallel-tuned topology
b Shunt-C/series-tuned topology
Note: v_{drive} is a sinusoidal voltage required to drive the switch model used in the ADS simulation in such a way that the switch duty cycle is 50%

Table 3: Comparison of analytical and numerical simulation results

Parameters	Shunt-C/series-tuned		Series-L/parallel-tuned	
	theory	simulation	theory	simulation
$V_{sw_{pk}}$	17.8 V	19.4 V	14.3 V	14.3 V
$I_{sw_{pk}}$	286 mA	288 mA	356 mA	345.4 mA
$V_{o_{pk}}$	5.37 V	5.5 V	9.3 V	8.9 V
$I_{o_{pk}}$	186 mA	192 mA	107 mA	103 mA
I	100 mA	106.3 mA	100 mA	93.6 mA
P_o	500 mW	529 mW	500 mW	461 mW
η	100%	99.5%	100%	98.5%

where

$$Z = \sqrt{X^2 + r^2} \tag{40}$$

$$\beta = \tan^{-1}\left(\frac{X}{r}\right) \tag{41}$$

$$Q = \frac{X}{r} \tag{42}$$

with

$$X = \omega L$$

The nominal operation of a class-E amplifier is reached when conditions (7) and (8) are satisfied. The output phase angle φ and the constant a can be expressed as a function of Q by solving (7) and (8), where the switch current is now described by (39). From (41) and (42), it is obvious that β is also a function of Q:

$$\varphi(Q) = \tan^{-1}(Q) + \tan^{-1}\left[\frac{Q \cdot \left(1 - \exp\left(\frac{-\pi}{Q}\right)\right)}{2 \cdot \exp\left(\frac{-\pi}{Q}\right)}\right] - \pi \tag{43}$$

$$a(Q) = \frac{\exp\left(\frac{-\pi}{Q}\right) - 1}{\exp\left(\frac{-\pi}{Q}\right) + 1} \cdot \frac{\sqrt{Q^2 + 1}}{\sin(\gamma(Q))} \tag{44}$$

$$\beta(Q) = \tan^{-1}(Q) \tag{45}$$

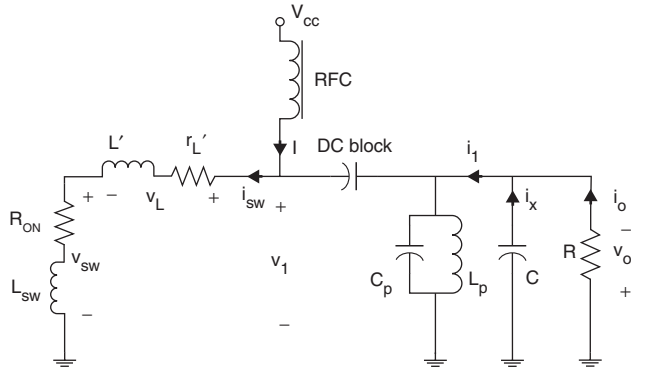

Fig. 3 *ON-state series-L/parallel-tuned topology equivalent circuit for loss analysis*

where

$$\gamma(Q) = \varphi(Q) - \beta(Q) \tag{46}$$

For $r = 0\,\Omega$ (ideal condition), Q is infinite, equations (43) and (44) reduce to (10) and (9), respectively.

At the fundamental frequency f_o, we can rewrite (11) as

$$i_1(\theta) = \mathrm{ICI} \cdot \sin(\theta + \varphi) + \mathrm{ICQ} \cdot \cos(\theta + \varphi) \tag{47}$$

where ICI and ICQ are defined as follows:

$$\mathrm{ICI} = \frac{1}{\pi} \cdot \int_0^{\pi} i_{sw}(\theta) \cdot \sin(\theta + \varphi)\mathrm{d}\theta = \frac{V_{cc}}{\pi \cdot Z} \cdot G(Q) \tag{48}$$

$$\begin{aligned} \mathrm{ICQ} &= \frac{1}{\pi} \cdot \int_0^{\pi} i_{sw}(\theta) \cdot \cos(\theta + \varphi)\mathrm{d}\theta \\ &= \frac{V_{cc}}{\pi \cdot Z} \cdot F(Q) \end{aligned} \tag{49}$$

with

$$\begin{aligned} G(Q) =& 2 \cdot \cos(\varphi(Q)) \cdot \sqrt{Q^2+1} \\ &- \frac{\pi \cdot a(Q)}{2} \cdot \cos(\tan^{-1}(Q)) \\ &+ \left(a(Q) \cdot \sin(\gamma(Q)) - \sqrt{Q^2+1}\right) \cdot \frac{Q^2}{Q^2+1} \\ &\times \left(\exp\left(\frac{-\pi}{Q}\right) + 1\right) \cdot \left(\frac{\sin(\varphi(Q))}{Q} + \cos(\varphi(Q))\right) \end{aligned} \tag{50}$$

and

$$\begin{aligned} F(Q) =& -2 \cdot \sin(\varphi(Q)) \cdot \sqrt{Q^2+1} \\ &+ \frac{\pi \cdot a(Q)}{2} \cdot \sin(\tan^{-1}(Q)) \\ &+ \left(a(Q) \cdot \sin(\gamma(Q)) - \sqrt{Q^2+1}\right) \cdot \frac{Q^2}{Q^2+1} \\ &\times \left(\exp\left(\frac{-\pi}{Q}\right) + 1\right) \cdot \left(\frac{\cos(\varphi(Q))}{Q} - \sin(\varphi(Q))\right) \end{aligned} \tag{51}$$

From Fig. 3 we can also write:

$$i_1(\theta) = v_o(\theta) \cdot Y \tag{52}$$

where Y is the admittance of the RC parallel circuit

$$Y = G + j \cdot \omega \cdot C = G + j \cdot B \tag{53}$$

Substituting (1) and (53) into (52) leads to (54),

$$i_1(\theta) = V_{cc} \cdot a \cdot \sqrt{G^2 + B^2} \cdot \sin(\theta + \varphi + \psi) \tag{54}$$

with

$$\psi = \tan^{-1}\left(\frac{B}{G}\right) \tag{55}$$

Then, from (47) and (54), we obtain

$$\mathrm{ICI} = V_{cc} \cdot a \cdot \sqrt{G^2 + B^2} \cdot \cos(\psi) \tag{56}$$

$$\mathrm{ICQ} = V_{cc} \cdot a \cdot \sqrt{G^2 + B^2} \cdot \sin(\psi) \tag{57}$$

From (48), (49), (56) and (57), we can express the parameter ψ as a function of Q,

$$\psi = \tan^{-1}\left(\frac{F(Q)}{G(Q)}\right) \tag{58}$$

C can then be derived from equations (55) and (58), where $B = \omega C$,

$$C = \frac{G}{\omega} \cdot \frac{F(Q)}{G(Q)} \tag{59}$$

Moreover, from (55) and (56), we obtain

$$\mathrm{ICI} = V_{cc} \cdot a \cdot G \tag{60}$$

The expression for X, as a function of Q and G, can then be obtained from (40), (48), and (60):

$$X = \frac{Q \cdot G(Q)}{\pi \cdot a(Q) \cdot \sqrt{Q^2+1}} \cdot \frac{1}{G} \tag{61}$$

The DC term I in (11) is defined by

$$I = \frac{1}{2\pi} \cdot \int_0^{\pi} i_{sw}(\theta)\mathrm{d}\theta = \frac{V_{cc}}{2 \cdot \pi \cdot X} \cdot P(Q) \tag{62}$$

where

$$\begin{aligned} P(Q) =& \pi \cdot Q - 2 \cdot a(Q) \cdot \frac{Q}{\sqrt{Q^2+1}} \cdot \cos(\gamma(Q)) \\ &+ Q \cdot \left(1 - \exp\left(\frac{-\pi}{Q}\right)\right) \\ &\times \left(a(Q) \cdot \frac{Q}{\sqrt{Q^2+1}} \cdot \sin(\gamma(Q)) - Q\right) \end{aligned} \tag{63}$$

As $I = V_{cc}G_{dc}$, then we can write the equation of G_{dc} as follows:

$$G_{dc} = \frac{P(Q)}{2 \cdot \pi \cdot X} \tag{64}$$

Substituting X from (61) into (64) will lead to the following equation:

$$G_{dc} = \frac{a(Q)}{2} \cdot \frac{P(Q)}{G(Q)} \cdot \frac{\sqrt{Q^2+1}}{Q} \cdot G \tag{65}$$

To be able to determine the drain efficiency of the amplifier, we need to derive expressions for both DC input power (P_{dc}) and RF output power (P_o). The peak of the output voltage is symbolised as $V_{o_{pk}}$ in (67):

$$P_{dc} = V_{cc}^2 \cdot G_{dc} \tag{66}$$

$$P_o = \frac{1}{2} \cdot (V_{o_{pk}})^2 \cdot G = \frac{1}{2} \cdot (V_{cc} \cdot a(Q))^2 \cdot G \tag{67}$$

Equation (67) can be represented in another form, which is very useful for determining the value of the load conductance,

$$G = \frac{2 \cdot P_o}{V_{cc}^2 \cdot a(Q)^2} \tag{68}$$

Efficiency is now simply defined as a ratio of P_o and P_{dc}, described by (67) and (66), respectively. Making use of (65) results in (69) which is a function of Q, Fig. 4:

$$\eta(Q) = a(Q) \cdot \frac{Q}{\sqrt{Q^2+1}} \cdot \frac{G(Q)}{P(Q)} \tag{69}$$

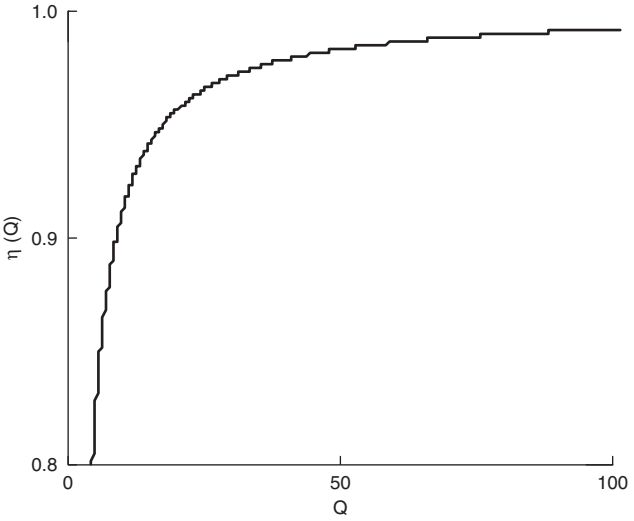

Fig. 4 *Drain efficiency as a function of Q*

It is clear from Fig. 4 that the efficiency will experience degradation as Q is reduced, in other words, the higher the ON-state channel resistance of the active device, the worse the efficiency.

A simpler, but less accurate, method to determine the efficiency of the series-L/parallel-tuned class-E power amplifier will now be discussed. The power dissipated by the ON-state resistance of the transistor can be calculated approximately by assuming that P_{dc}, P_o and all waveforms (except the switch voltage/v_{sw} waveforms during saturation) remain like those of the ideal amplifier.

Then the dissipated power is simply defined as

$$P_d = \frac{1}{2\pi} \cdot \int_0^{\pi} i_{sw}(\theta)^2 \cdot r \, \mathrm{d}\theta \tag{70}$$

$$P_d = \frac{V_{cc}^2 \cdot r}{12 \cdot \pi \cdot X^2} \times \begin{pmatrix} 2 \cdot \pi^3 + 24 \cdot a^2 \cdot \cos(\varphi) \cdot \sin(\varphi) \\ +3 \cdot a^2 \cdot \pi - 24 \cdot a \cos(\varphi) \\ +6 \cdot a^2 \cdot \cos(\varphi)^2 \cdot \pi - 6 \cdot a \cdot \cos(\varphi) \cdot \pi^2 \\ -12 \cdot a \cdot \sin(\varphi) \cdot \pi \end{pmatrix} \tag{71}$$

Substituting (9), (10), (19), and (32) into (71) results in the following:

$$P_d = \frac{\pi^2 \cdot (\pi^2+4)}{384} \cdot (5 \cdot \pi^2 - 36) \cdot P_o \cdot r \cdot G = 4.7583 \cdot P_o \cdot r \cdot G \tag{72}$$

As the drain efficiency is defined as the ratio of P_o and P_{dc}, and the DC input power (P_{dc}) is now the sum of P_o and P_d, we can write

$$\eta = \frac{P_o}{P_o + P_d} = \frac{1}{1 + 4.7583 \cdot r \cdot G} \tag{73}$$

5 Effect of switch resistance on circuit parameters and efficiency

Based on the given input data (P_o, V_{cc}, f_o, Q_{LC} and r), the circuit elements G, C, L, C_p, and L_p can be computed using (68), (59), (61), (35) and (36), respectively. Each of these equations is a strong function of Q, where $Q = \omega L/r$ and

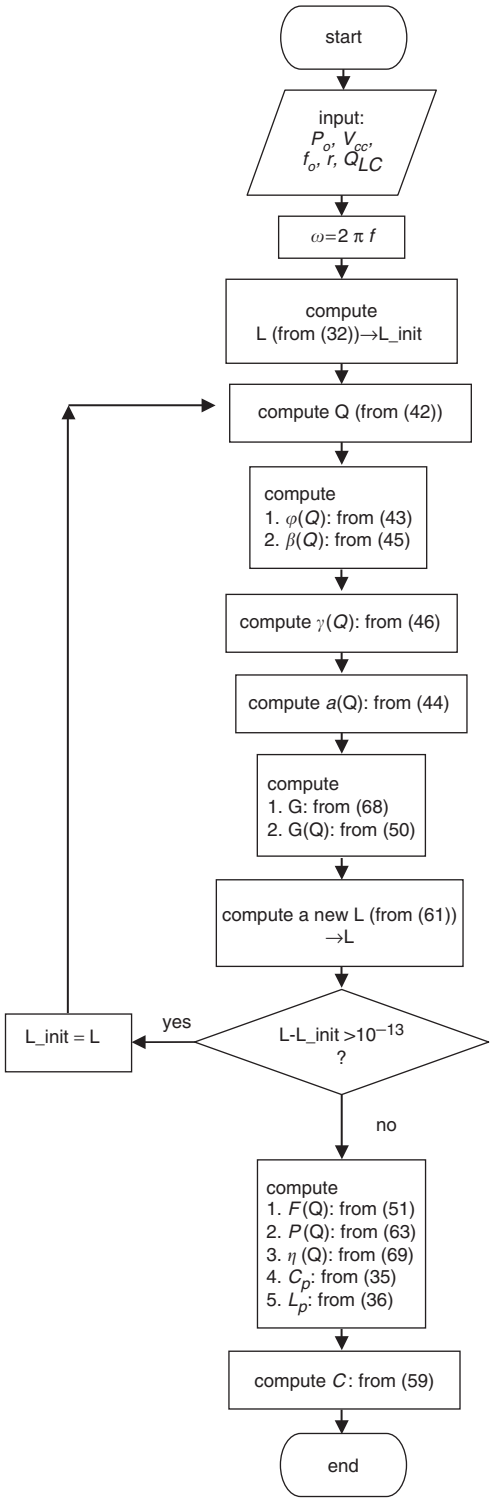

Fig. 5 *Flowchart for derivation of optimal component values*

L is as yet to be determined, therefore it is necessary to perform an iterative procedure (explained by the flowchart in Fig. 5) in order to calculate the circuit parameters.

Consider the effect that switch series resistance has on the previously defined ideal class-E amplifier specifications ($P_o = 500\,\text{mW}$, $V_{cc} = 5\,\text{V}$, $f_o = 2.5\,\text{GHz}$, 10% bandwidth, $Q_{LC} = 10$). For various given values of r, the corresponding component values required for a series-L/parallel-tuned class-E amplifier are presented in Table 4. The parameters n, η_1 and η_2 in Table 4 refer to the number of iterations to reach convergence, the efficiency based on (69), the exact analysis, and the efficiency based on (73), the simplified approach, respectively. Table 4 shows that as r increases the optimum component values of the circuit alter quite significantly when compared to the ideal case ($r = 0\,\Omega$). Moreover, Table 4 also shows that η_2 obtained from simplified approach is valid for small r, but not for higher values of r.

In Table 4, Agilent Advanced Design System (ADS) time domain simulation is used to verify the theoretical analysis, and two sets of simulations were conducted. The first simulation assumes that the values of the circuit elements do not change as r is varied (using component values as described in Table 2, series-L/parallel-tuned). The second simulation uses the component values which result from iterative computation (Table 4, Fig. 5). Excellent agreement between the second simulation results and the exact theoretical analysis (η_1) is achieved. From the second simulation, we can conclude that, as r goes up, efficiency drops, but RF output power (P_o) is not affected significantly. On the other hand, from the first simulation, we can see that, as r goes up, the efficiency degradation is not as significant as that which resulted from the second simulation, but P_o goes down drastically. This is because the DC current I changes as the value of the circuit elements is optimally selected. Thus, for optimal performance char-

Table 4: Optimum component values for series-L/parallel-tuned Class-E amplifiers and comparison of theoretical analysis and simulation

Parameter	$r = 0.01\,\Omega$	$r = 0.1\,\Omega$	$r = 1\,\Omega$	$r = 2\,\Omega$	$r = 3\,\Omega$	$r = 4\,\Omega$
Iterative theoretical analysis						
n	1	1	3	5	7	12
R, Ω	86.64	86.2	81.6	75.9	69.4	60.7
L, nH	1	1	0.94	0.85	0.74	0.6
C, pF	0.85	0.86	0.95	1.1	1.3	1.7
C_p, pF	7.35	7.39	7.8	8.39	9.18	10.5
L_p, nH	0.55	0.55	0.52	0.48	0.44	0.39
η_1, %	99.95	99.45	94.16	87.40	79.04	66.81
η_2, %	99.95	99.45	94.49	88.86	82.94	76.12
ADS simulation (η, P_o, I)						
Using component values from Table 2	98%, 479.1 mW, 97.2 mA	98%, 474.7 mW, 96.8 mA	93%, 433.8 mW, 92.9 mA	88%, 394.6 mW, 88.9 mA	84%, 360.7 mW, 85.4 mA	80%, 331.2 mW, 82.1 mA
Using component values resulting from iterative computation	98%, 479 mW, 97 mA	98%, 479 mW, 97 mA	93%, 478 mW, 103 mA	86%, 478 mW, 110 mA	78%, 477 mW, 122 mA	66%, 476 mW, 144 mA

Table 5: Optimum component values for shunt-C/series-tuned Class-E amplifiers and comparison of theoretical analysis and simulation

Parameter	$r = 0.01\,\Omega$	$r = 0.1\,\Omega$	$r = 1\,\Omega$	$r = 2\,\Omega$	$r = 3\,\Omega$	$r = 4\,\Omega$
Iterative theoretical analysis						
n	1	1	3	4	6	10
R, Ω	28.8	28.55	25.9	22.7	19.2	15.2
C, pF	0.4	0.41	0.44	0.49	0.55	0.66
L, nH	2.11	2.1	1.95	1.77	1.57	1.33
L_s, nH	18.34	18.2	16.5	14.45	12.24	9.65
C_s, pF	0.221	0.223	0.246	0.28	0.33	0.42
η_1, %	99.95	99.52	95.00	89.33	82.60	73.87
η_2, %	99.95	99.52	94.99	89.26	82.43	73.52
ADS simulation (η, P_o, I)						
Using component values from Table 2	98%, 514 mW, 104 mA	97%, 504 mW, 103 mA	92%, 453 mW, 97 mA	89%, 415 mW, 93 mA	85%, 381 mW, 89 mA	82%, 351 mW, 85 mA
Using component values resulting from iterative computation	98%, 514 mW, 104 mA	97%, 508 mW, 104 mA	92%, 498 mW, 107 mA	87%, 498 mW, 113 mA	81%, 500 mW, 123 mA	72%, 503 mW, 138 mA

acterisation, it is essential that the optimal component approach is adopted.

We now consider which topology (shunt-C/series-tuned or series-L/parallel-tuned topology) is less sensitive in terms of efficiency to the ON channel resistance of the active device. For the same design specifications with various given values of r, the corresponding component values required for a shunt-C/series-tuned class-E amplifier are presented in Table 5. The parameters n, η_1 and η_2 in Table 5 now refer to the number of iterations to reach convergence, the efficiency computed using the method described in [14] (exact analysis) and [15] (simplified approach), respectively. Comparison of Tables 4 and 5 leads to the conclusion that the shunt-C/series-tuned topology, with respect to the series-L/parallel-tuned topology, is less sensitive to the ON channel resistance of the active device at higher values of r.

6 Power loss due to the transistor output capacitance (C_{out}) in series-L/parallel-tuned topology

The energy stored in C_{out} just before the transistor is switched on, will be dissipated through the ON channel resistance at turn-on. The corresponding value of the dissipated power due to the discharging mechanism follows:

$$P_{loss} = 0.5 \times C_{out} \times V_{sw\_d}^2 \times f \qquad (74)$$

where V_{sw_d} is the switch voltage level just before the switch is turned on.

To establish how deleterious the value of C_{out} would be in pHEMT technology, we cite a 0.15 μm OMMIC pHEMTs (8×75 μm). This device has a C_{out} of about 0.2 pF at 2.5 GHz. Considering (6), the predicted value of V_{sw_d} when $\theta = \pi$ is $2 \times V_{cc}$ (10 V). Thus, P_{loss} is 25 mW which is 5% of the expected output power (500 mW). This situation is rather different if MOSFET technology is used where, for example, C_{out} is much higher, i.e. 5.7 pF (STMicroelectronics: PD57002) [16] and 1.1 pF (Infineon: BF998) [17], so that power loss due to C_{out} is substantial. Parametric studies by the authors of this paper have shown that values of C_{out} below 0.7 pF can be tolerated without undue loss of efficiency or output harmonic production.

7 Conclusions

A series-L/parallel-tuned class-E amplifier has been analysed in this paper and a set of design equations derived to compute the topology component values and major performance parameters of the circuit. A design procedure was introduced which allows the effect that nonzero switch resistance has on amplifier performance efficiency to be accurately accounted for. The technique developed allows optimal circuit components to be found for the known device series resistance. For a relatively high value of ON series resistance, 4 Ω, drain efficiencies of around 66% for the series-L/parallel-tuned topology and 73% for the classic shunt-C/series-tuned topology appear possible, for values below this both topologies offer about the same efficiency level. However, the series-L/parallel-tuned topology appears to offer advantages in terms of its potential for MMIC realisation because of less stringent inductance requirements than in the shunt-C/series-tuned topology. The theoretical work presented in this paper should facilitate the design of high efficiency switched amplifiers at frequencies commensurate with the needs of modern mobile wireless applications in the microwave frequency range, where low-output capacitance MMIC switching devices such as pHEMTs are to be used.

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