Inverse Class-E Amplifier With Transmission-Line Harmonic Suppression

Thian Mury and Vincent F. Fusco, *Fellow, IEEE*

***Abstract*—This paper reports on the design methodology and experimental characterization of the inverse Class-E power amplifier. A demonstration amplifier with excellent second and third harmonic-suppression levels has been designed, constructed, and measured. The circuit fabricated using a 1.2-mm gate-width GaAs MESFET is shown to be able to deliver 22-dBm output power at 2.3 GHz. The amplifier achieves a peak power-added efficiency of 64% and drain efficiency of 69%, and exhibits 11.6 dB power gain when operated from a 3-V supply voltage. Comparisons of simulated and measured results are given with good agreement between them being obtained. Experimental results are presented for the amplifier's response to Gaussian minimum shift keying modulation, where a peak error vector modulation value of 0.6% is measured.**

***Index Terms*—Class E, GaAs MESFET, Gaussian minimum shift keying (GMSK) modulation, harmonic suppression, high efficiency, RF amplifier, transmission line, zero current switching.**

I. Introduction

IN MOBILE wireless equipment, the RF section dominates power consumption. This is largely a consequence of the handset power amplifier which is a key core component of any RF front-end transmitter. The power amplifier consumes most of the battery power and therefore it is essential to improve its efficiency. An efficient power amplifier will lead to increased battery life time, reduced size of transistor heat sink, and to improved reliability due to reduced thermal dissipation issues.

A Class-E power amplifier can theoretically offer 100% collector or drain efficiency since simultaneous nonzero switching voltage and current are prevented from occurring [1]. Thus, Class-E amplifier's operation shows promise for handset applications, mobile telephony, portable wireless communications, vehicular telemetry, and sensors applications. Moreover being a switching amplifier, it is in principle, possible to directly control output power level through the dc supply voltage without unduly impairing efficiency. Although not pursued here this feature makes the Class-E amplifier useful for envelope elimination and restoration (EER) transmitter-linearization schemes [2].

The classical Class-E power amplifier topology, shown in Fig. 1(a), was introduced by Sokal [1]. Sokal applied zero voltage switching and zero voltage slope switching conditions in order to ensure "soft switching" operation. The recently introduced inverse Class-E topology, shown in Fig. 1(b), [3], utilizes zero current switching and zero current slope switching conditions in order to obtain optimum amplifier operation. In the inverse Class-E amplifier the switching current and voltage waveforms are the duals to those in the classical Class-E topology, Fig. 2. Previously the inverse Class-E and the classic Class-E amplifiers were respectively classified as "series-*L*/parallel-tuned" and "shunt-*C*/series-tuned" in [3] and [9], and "voltage driven" and "current driven" in [5].

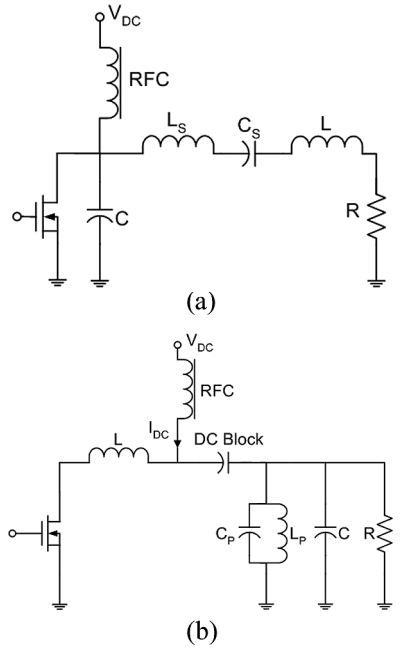

Fig. 1. Basic switching amplifier topologies. (a) Class E. (b) inverse Class E.

The advantages of the inverse Class-E topology when compared to the conventional Class-E topology are that it operates with approximately 20% lower peak switching voltage than the classical Class-E topology. The peak switching voltage for nominal Class-E operation is 3.562 V_{DC}; while for inverse Class-E operation the value is 2.862 V_{DC}. This relaxes the breakdown voltage requirement on the transistor. Secondly, the inverse Class-E amplifier operates with lower inductance values than the classical topology. The lower inductance value requirement means that the inductor's series resistance is reduced and that the inductor has a higher self-resonance frequency. This, in turn, permits the increased possibility of using lumped components for monolithic integrated circuit (IC) realization. Further, as discussed in [4], the inverse Class-E amplifier offers

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The authors are with the Institute of Electronics, Communications, and Information Technology (ECIT), the Queen's University of Belfast, Belfast BT3 9DT, U.K. (e-mail: mury@ecit.qub.ac.uk; v.fusco@ecit.qub.ac.uk).

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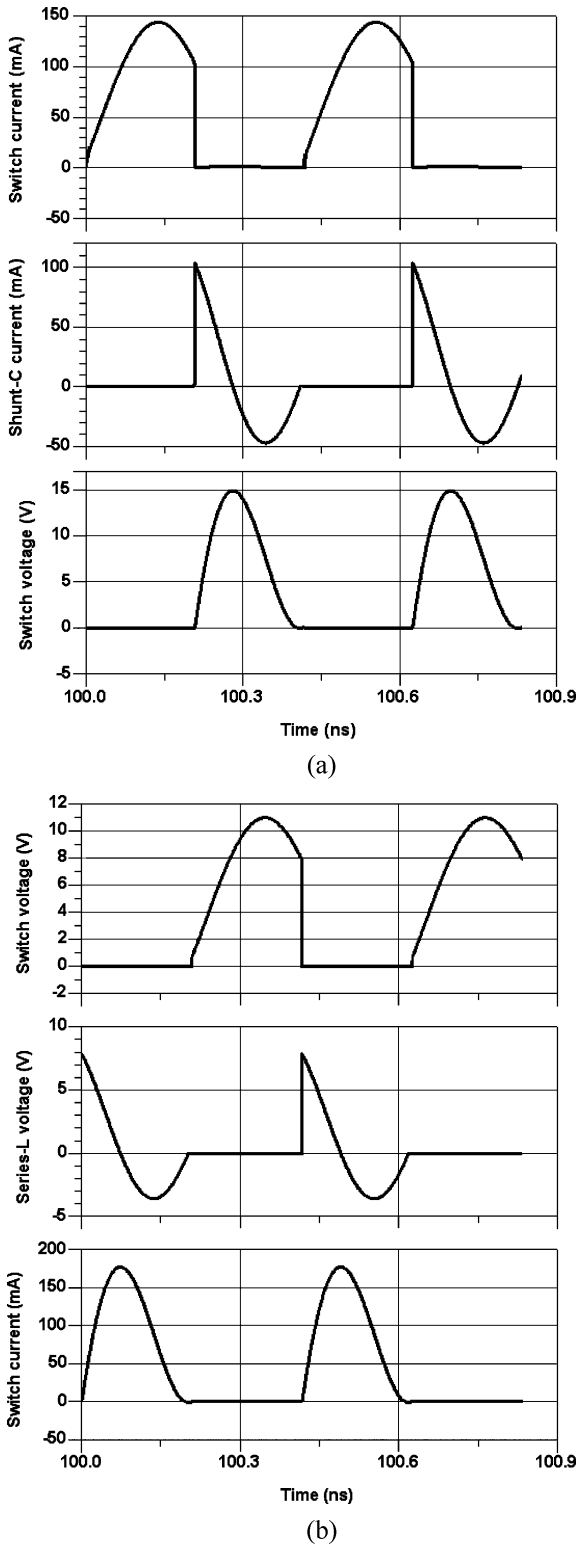

Fig. 2. Voltage and current waveforms of idealized lumped-element load-network 0.2 W 4 V 2.4 GHz. (a) Class E, Fig. 1(a). (b) Inverse Class E, Fig. 1(b).

better scope for optimization for high efficiency at higher output power levels, as well as higher peak output power when compared to optimal classic Class-E designs. Additionally, in [4] it was shown that the inverse Class E is reasonably tolerant to the circuit component value variations as well as switching frequency and duty cycle variations.

To date only one example of an experimentally validated inverse Class-E amplifier has been reported, [5]. This amplifier which operated at 870 MHz was empirically designed. In this paper the systematic synthesis approach developed in [3] for the design of an inverse Class-E amplifier is for the first time experimentally validated.

In this paper, we present the design, fabrication, and measurement of a 22-dBm 3-V inverse Class-E amplifier operated at frequency 2.3 GHz. In order to improve the harmonic suppression performance of the amplifier a distributed-element load network, resulting from an equivalent lumped-element load network transformation is presented. By this means unwanted second and third harmonic signals are terminated by open-circuit shunt stubs. When compared to the classic Class-E topology [6]–[8], transmission-line load-network implementations of the inverse Class-E amplifier deploying both Kuroda identity and Richard transformation result in a physically more compact design [9].

II. Inverse Class-E Circuit Design

The basic circuit of the inverse Class-E amplifier Fig. 1(b) is comprised of a transistor, a series inductance L, and a parallel-tuned load network $L_p - C_p - R$. Here, an additional capacitance C is required in order to compensate for fundamental-frequency phase shift [3]. The dc current $I_{\rm DC}$ passing through the RF choke (RFC) is transformed by transistor ON-OFF switching action into a series of related fundamental-frequency and harmonic currents. The harmonic currents are then filtered out by the parallel-tuned $L_p - C_p$ resonator provided it has a high enough Q-factor, leaving only the fundamental-frequency current. Capacitor C_1 is a dc blocking capacitance which prevents dc current appearing at the output port as well as preventing the dc current from short-circuiting inductor L_p to the ground.

The closed-form design equations given in [3] are used to determine the optimum lumped-component values of the inverse Class-E power amplifier under 50% duty ratio operation for a required output power P_o, at a specified dc supply voltage $V_{\rm DC}$, operating frequency f_o, and loaded Q-factor. These design equations are summarized in (1)–(5) with the loaded Q-factor given in terms of the inductor parameter L_p.

Voltage and current waveforms for an idealized 0.2-W 4-V 2.4-GHz inverse Class-E amplifier, generated using (6)–(10), are shown in Fig. 2(b). The switch voltage, switch current, and the voltage drop across the series inductance L are, respectively, denoted as $v_{\rm SW}(\theta)$, $i_{\rm SW}(\theta)$, and $v_L(\theta)$ where $\theta = \omega t$. It can be seen from Fig. 2(b) that the peak switch voltage value, $v_{\rm SW,pk}$, is about 11.45 V. This agrees with the theoretical prediction i.e., $v_{\rm SW,pk} = 2.862\, V_{\rm DC}$

$$L = \frac{V_{\rm DC}^2}{\pi\omega P_o} \tag{1}$$

$$C = \frac{\pi(\pi^2-4)}{2(\pi^2+4)}\frac{P_o}{\omega V_{\rm DC}^2} \tag{2}$$

$$R = \frac{\pi^2+4}{8}\frac{V_{\rm DC}^2}{P_o} \tag{3}$$

$$L_p = \frac{R}{\omega Q} \tag{4}$$

$$C_p = \frac{1}{\omega^2 L_p} \tag{5}$$

$$v_{\rm SW}(\theta) = \begin{cases} 0 & if\ 0 < \theta < \pi \\ V_{\rm DC}\left[1 - a\sin(\theta + \phi)\right] & if\ \pi < \theta < 2\pi \end{cases} \tag{6}$$

$$v_L(\theta) = \begin{cases} V_{\rm DC}\left[1 - a\sin(\theta + \phi)\right] & if\ 0 < \theta < \pi \\ 0 & if\ \pi < \theta < 2\pi \end{cases} \tag{7}$$

$$i_{\rm SW}(\theta) = \begin{cases} \frac{V_{\rm DC}}{\omega L}\left[\theta + a\cos(\theta + \phi) \right. \\ \quad \left. -a\cos\phi\right] & if\ 0 < \theta < \pi \\ 0 & if\ \pi < \theta < 2\pi \end{cases} \tag{8}$$

where

$$a = \sqrt{\frac{\pi^2}{4} + 1} \tag{9}$$

$$\phi = \tan^{-1}\left(\frac{-2}{\pi}\right). \tag{10}$$

In most cases, the load resistance of a power amplifier has to meet a specific value, 50 Ω is typical. However, it is apparent from (3) that the inverse Class-E synthesis procedure may suggest values other than 50 Ω. Therefore, an impedance transformation may be required for effective 50-Ω system utilization. This can be achieved, for example, by means of a simple L-type matching circuit. Further, if the load network is to be implemented using transmission lines rather than lumped components, direct synthesis using Kuroda identity and Richard transformation as explained in [9] can be applied.

The shunt capacitance C in Fig. 1(b) can be replaced by two open-circuit shunt stubs which are deliberately designed to accommodate the second and third harmonic terminations, and thus dispenses with the need for a parallel-tuned $L_p - C_p$ circuit as in Fig. 1(b). The electrical lengths (θ) of the open-circuit shunt stubs are 45° and 30° at fundamental frequency f_o, which are equivalent to 90° at $2f_o$ and $3f_o$, respectively. As a result these stubs provide the required shorting condition required for second and third harmonic signals. The capacitive behavior of an open-circuit shunt stub is described by (11) and accordingly the characteristic admittance (Y_0) of the open-circuit shunt stubs, assumed lossless, can be computed using

$$Y = j\omega C = jY_0 \tan\theta \tag{11}$$

$$Y_0 = \frac{\omega C}{\tan\theta_1 + \tan\theta_2} \tag{12}$$

where $\theta_1 = 45°$ and $\theta_2 = 30°$, and C is computed from (2).

III. Simulation Results

To confirm the theoretical analysis and synthesis explained in Section II, harmonic balance and momentum simulations have been carried out within the Agilent Advanced Design Systems (ADS) suite. Fig. 3 shows the simulated circuit schematic. Here the transistor used is a 0.3-μm gate-length 1200-μm gate-width MwT-8 GaAs MESFET manufactured by MicroWave Technology, Inc. [10], whose large-signal model is available within the ADS library. Realistic models for optimized lumped component L of 2.2 nH and dc blocking capacitances of 22 pF are obtained from Coilcraft [11] and AVX Corporation [12] respectively. The substrate used was Rogers RO4003C with dielectric constant 3.38 ± 0.05, substrate thickness 508 μm, copper thickness 17 μm, and loss tangent 0.0021 at 2.5 GHz. The dimensions of the optimized open-circuit shunt stubs are as follows: $W = 435$ μm and $L = 9940$ μm for TLsecond; $W = 435$ μm and $L = 6630$ μm for TLthird. Note that the characteristic admittance Y_0 of both stubs, expressed in (12), are here designed to be the same. This means that both stubs have the same width and hence are more convenient for physical realization. However, in general, a designer may choose different Y_0 values for each stub. Here the electrical lengths of TLsecond and TLthird are, respectively, 45° and 30°.

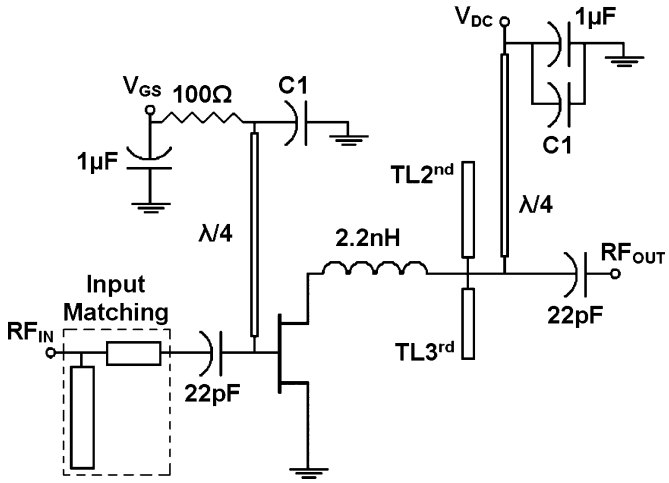

Fig. 3. Complete inverse Class-E circuit schematic as simulated.

The chokes for the gate and drain biasing in Fig. 3 are realized using quarter-wavelength transmission lines which provide an open circuit path for RF signals and a short circuit path for dc. The bypass capacitors $C1$ in Fig. 3 are implemented using radial stubs and self-resonate at f_0 whilst the 1-μF bypass capacitors self-resonate at a low frequency. Simulations using a realistic model for the dc blocking capacitor suggested that the connection of this capacitor as shown in Fig. 3 will lead to a good input match and, hence, to better overall amplifier efficiency.

The harmonic balance simulation results for the amplifier are shown in Figs. 4–7. Fig. 4 depicts the output power, gain, drain and power-added efficiencies (PAEs) versus input power for $V_{GS} = -2.1$ V, $V_{\rm DC} = 4$ V, and $f_o = 2.4$ GHz. It can be seen from Fig. 4 that the peak PAE and η are, respectively, 68.4% and 71.2% at output power 23 dBm, input power 9 dBm, and gain 14 dB. Output power starts to saturate at an input power level of about 7 dBm. Below this level the input and output power relationship is reasonably linear. The gain at low input power levels is about 20 dB, but the efficiency is poor i.e., below 20%.

The simulated switch voltage and current waveforms at the optimum operating point are shown in Fig. 5. From Fig. 5, it can be observed that the peak switch voltage is about 9.5 V. This value is lower than that theoretical analysis predicted i.e., 11.45 V. The simulated switch voltage and current waveforms in Fig. 5 are distorted when compared to the idealized waveforms in Fig. 2(b). This is mainly due to the effects of nonlinear transistor output capacitance C_{DS} and other internal transistor parasitics, non instantaneous transistor switching action,

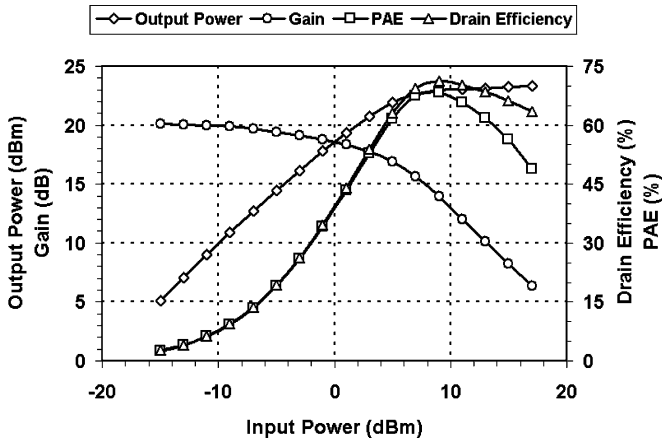

Fig. 4. ADS simulation results ($V_{GS} = -2.1$ V, $V_{\rm DC} = 4$ V, $f_o = 2.4$ GHz): output power, power gain, drain efficiency, and PAE versus input power.

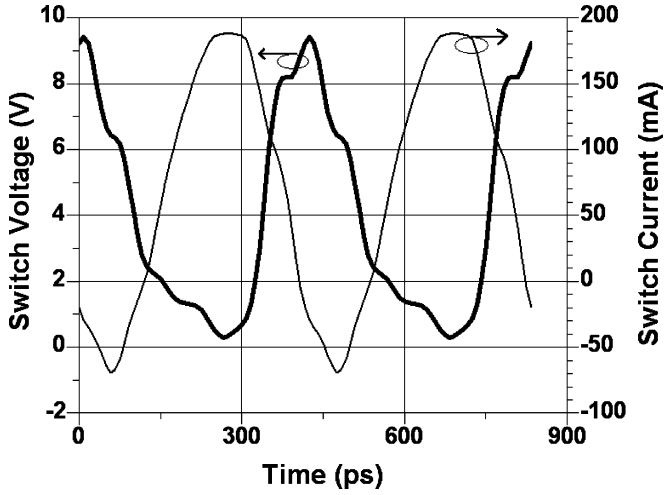

Fig. 5. Simulated switch voltage and current waveforms of the complete inverse Class-E circuit as in Fig. 3.

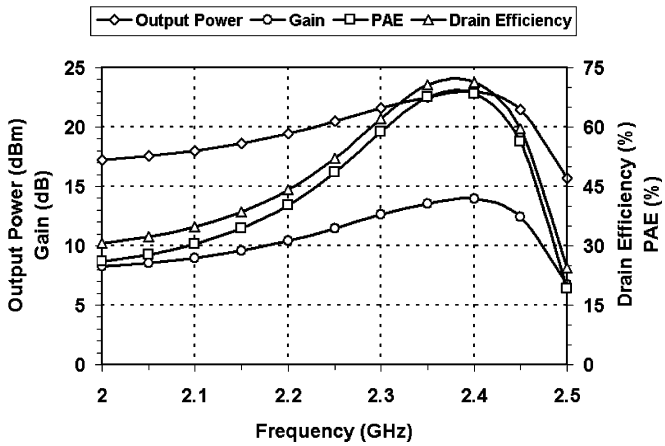

Fig. 6. ADS simulation results ($V_{GS} = -2.1$ V, $V_{\rm DC} = 4$ V, $P_i = 9$ dBm): output power, power gain, drain efficiency, and PAE versus frequency.

and nonzero transistor saturation voltage. The overlapping area of the switch voltage and current waveforms in Fig. 5 implies dissipated power within the switch which will result in amplifier's efficiency degradation.

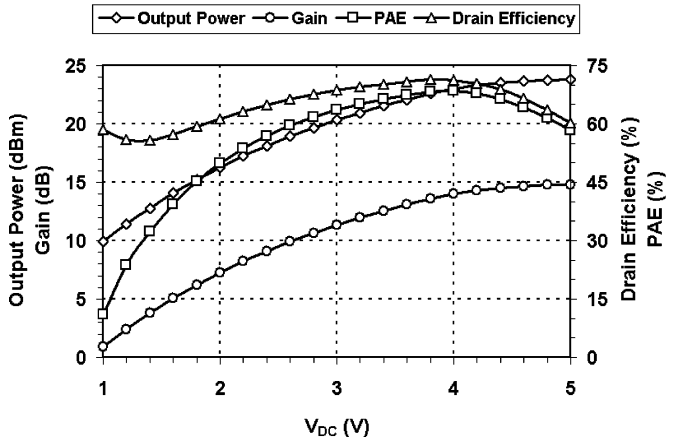

Fig. 7. ADS simulation results ($V_{GS} = -2.1$ V, $P_i = 9$ dBm, $f_o = 2.4$ GHz): output power, power gain, drain efficiency, and PAE versus dc supply voltage.

The output power, gain, drain efficiency, and power added efficiency are plotted versus frequency in Fig. 6 for an input power level of 9 dBm. Here, over a 200-MHz bandwidth i.e., from 2.25- to 2.45-GHz PAE is always better than 48%, $\eta > 52\%$, output power >20.5 dBm, and gain >11.5 dB.

Fig. 7 presents the amplifier performance as its dc supply voltage is varied. Here, $\eta > 55\%$ for $V_{\rm DC}$ ranges from 1 to 5 V and PAE> 50% for $V_{\rm DC}$ ranges from 2 to 5 V are obtained. This implies that the output power can be well-controlled through direct variation of the dc supply voltage without unduly impairing efficiency. In [4] it was demonstrated that the amplitude of the RF output voltage $v_o(\theta)$ is linearly proportional to the $V_{\rm DC}$, and consequently, output power is a quadratic function of $V_{\rm DC}$. The relevant equations in [4] are reproduced as

$$v_o(\theta) = \frac{c}{G}\sin(\theta + \phi) \tag{13}$$

$$c = V_{\rm DC} G \alpha \tag{14}$$

$$\alpha = 1.862 \tag{15}$$

where $\theta = \omega t, \omega = 2\pi f$, f is the operating frequency, G is the load conductance, and ϕ is the output phase. Note that α in (15) is basically a in (9).

From Fig. 7, the typical quadratic behavior of output power as a function of $V_{\rm DC}$ can be confirmed as follows:

$$10^{(23.8\ {\rm dBm} - 9.9\ {\rm dBm})/10} \approx \left(\frac{5\ {\rm V}}{1\ {\rm V}}\right)^2 = 25. \tag{16}$$

The amplifier's input matching circuit is formed by a series line together with a shunt stub, as shown in Fig. 3. From harmonic balance simulations, this matching circuit results in a computed return loss of about 26 dB at 2.4 GHz. Due to stub-to-stub electromagnetic coupling effects, this shifts down to 2.365 GHz as predicted by momentum simulations, and return loss is 31 dB. The second and third harmonic levels obtained from harmonic balance simulations are, respectively, 58 and 73 dBc whereas from momentum simulations they are 45 and 56 dBc, respectively.

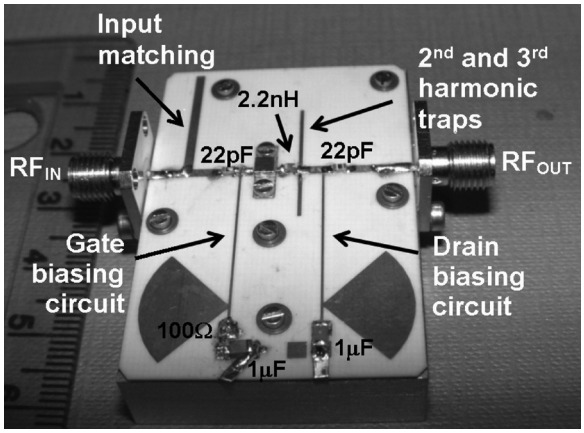

Fig. 8. Photograph of the constructed inverse Class-E amplifier.

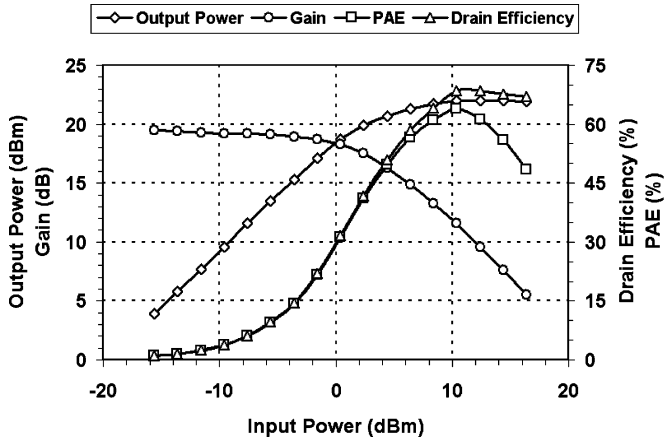

Fig. 10. Measurement results ($V_{GS} = -1.8$ V, $V_{\rm DC} = 3$ V, $f_o = 2.3$ GHz): output power, power gain, drain efficiency, and PAE versus input power.

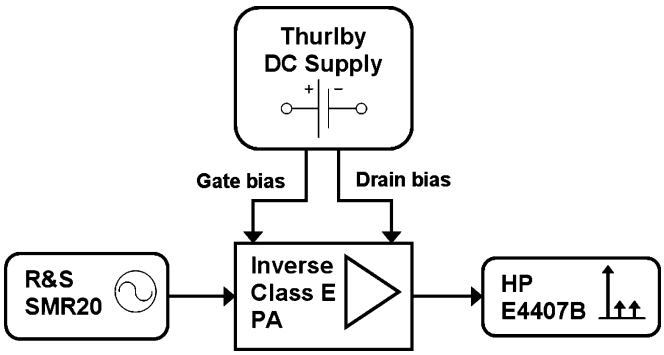

Fig. 9. Power measurement setup.

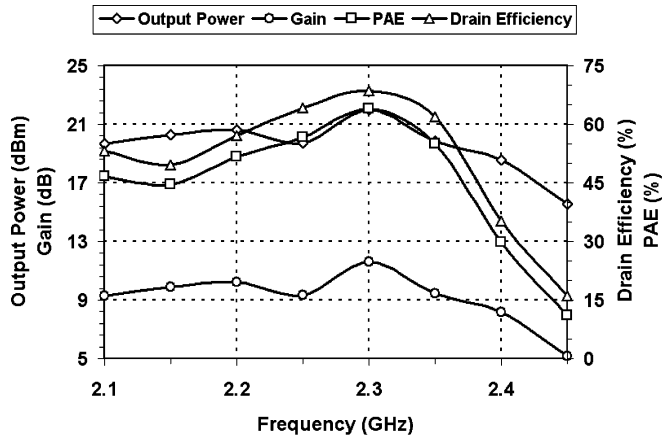

Fig. 11. Measurement results ($V_{GS} = -1.8$ V, $V_{\rm DC} = 3$ V, $P_i = 10.4$ dBm): output power, power gain, drain efficiency, and PAE versus frequency.

IV. Fabrication and Measurement

In order to validate both theoretical analysis and simulation results we fabricated the synthesized inverse Class-E amplifier on Rogers RO4003C 4.7 cm $\times$ 3.2 cm substrate (Fig. 8). The power measurement setup is shown in Fig. 9. Here, the RF input signal was generated using a Rohde and Schwarz SMR20 signal generator and the output signal was fed to an Agilent HP E4407B spectrum analyzer. Both negative gate-biasing voltage and positive drain-biasing voltage are supplied from a Thurlby dc source.

The measured output power, gain, drain efficiency, and PAEs versus input power are illustrated in Fig. 10. In this case, transistor bias is adjusted for best performance to be $V_{GS} = -1.8$ V and $V_{\rm DC} = 3$ V at 2.3 GHz, whereupon a peak PAE $= 64\%$ and $\eta = 69\%$ were obtained at an output power of 22 dBm. The input power applied to the amplifier was 10.4 dBm resulting in 11.6-dB measured gain.

The amplifier performance, for an input power level of 10.4 dBm as a function of operating frequency is presented in Fig. 11. It can be seen that PAE, drain efficiency η, and output power reach their peak values simultaneously at 2.3 GHz. Also from Fig. 11, it is seen that PAE of better than 45% and η of better than 50% are obtained over a 250-MHz bandwidth i.e., from 2.1 to 2.35 GHz. This agrees well with the simulation results given in Fig. 6.

Fig. 12 shows the plot of output power, gain, drain and power added efficiencies versus $V_{\rm DC}$. When the dc supply voltage is swept from 2 to 3.5 V, the PAE remains >59% and $\eta > 62\%$. Again, the typical quadratic behavior of output power as a function of $V_{\rm DC}$ suggested by (17) is observed and thus agrees with theoretical analysis

$$10^{(23.1\ \text{dBm}-18.45\ \text{dBm})/10} \approx \left(\frac{3.5\ \text{V}}{2\ \text{V}}\right)^2 \approx 3. \qquad (17)$$

The comparisons between simulated and measured results are given in Fig. 13. In each case excellent agreement was obtained. Measured second and third harmonic levels are better than -25 dBm. These are about 47 dBc at the optimum output-power operating point, i.e., at $P_o = 22$ dBm.

Table I presents comparisons between this work, inverse Class-E, and the previously published works, conventional Class-E, i.e., [6]–[8] and [13]. In these references, the active devices used are GaAs MESFETs and the operating frequencies are between 950 and 2400 MHz. Empty fields (–) indicate that the authors did not specify the corresponding parameter.

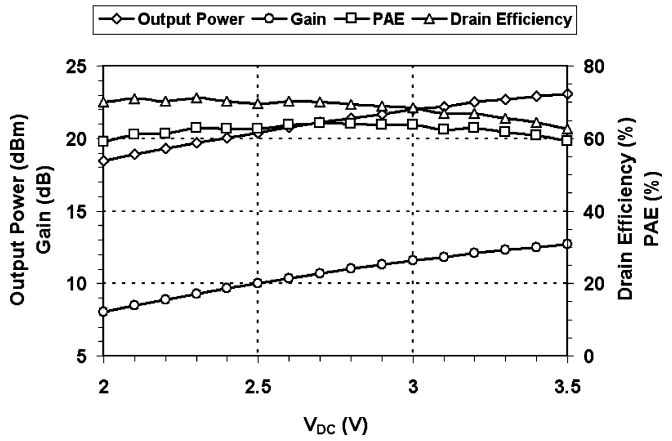

Fig. 12. Measurement results ($V_{GS} = -1.8$ V, $P_i = 10.4$ dBm, $f_o = 2.3$ GHz): output power, power gain, drain efficiency, and PAE versus dc supply voltage.

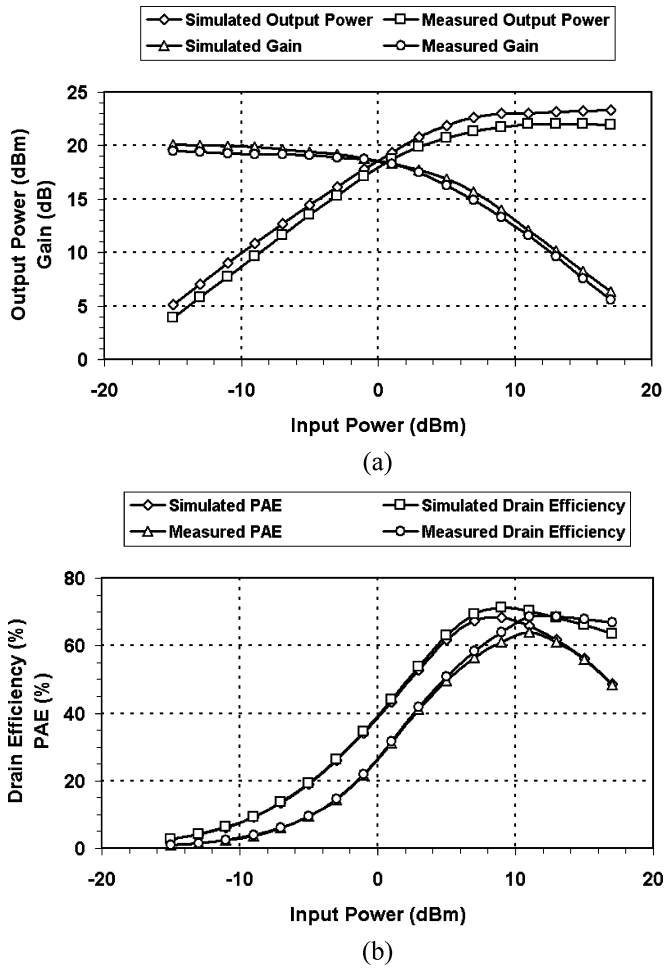

Fig. 13. Comparisons of simulated and measured results. (a) Output power and gain versus input power. (b) Drain efficiency and PAE versus input power.

V. GMSK Modulation

Switching amplifiers such as the inverse Class E are suited for constant envelope modulated signals such as GFSK, GMSK, or FM. Fig. 14(a) shows the output spectrum of the inverse Class-E amplifier measured using a Rohde and Schwarz FSQ 40 signal analyzer when a GMSK modulated signal with a bit period product (BT) 0.3 and a symbol rate (SR) 270.833 kHz was applied using a Rohde and Schwarz SMU 200A vector signal generator. It is observed that no significant spectral re-growth is generated.

The I/Q constellation diagram is illustrated in Fig. 14(b). Here peak error vector modulation (EVM) $= 0.622\%$, peak magnitude error $= 0.339\%$, peak phase error $= -0.35°$, and signal-to-noise ratio $= 51.24$ dB are obtained. This indicates that the amplifier is performing within the GMSK specification.

TABLE I
COMPARISONS WITH THE PREVIOUSLY PUBLISHED WORKS

Ref.	f (GHz)	V_{DC} (V)	P_O (dBm)	PAE/η (%)	G (dB)	2nd/3rd Harmonic (dBc)
[6]	2	6	27	54/62	9.1	-
[7]	0.95	3.5	26.6	-/72	-	-
[8]	2.4	4.3	20	64/70	10.8	-
[13]	1.8	2.4	23	57/-	16	27/61
This work	2.3	3	22	64/69	11.6	47/47

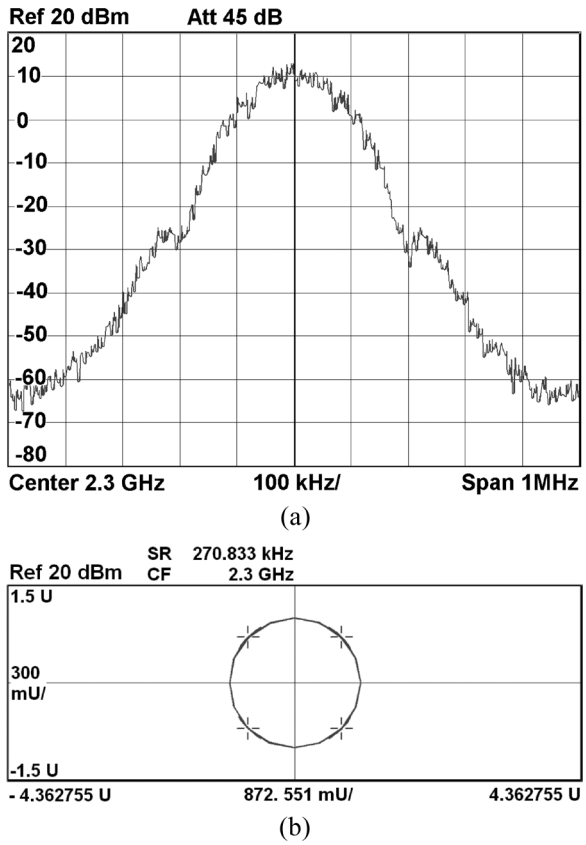

Fig. 14. GMSK modulation: (a) measured output spectrum. (b) I/Q constellation diagram.

VI. Conclusion

This paper presents experimental confirmation of the synthesis procedure for an inverse Class-E amplifier design with excellent second and third harmonic-suppression levels. The theoretical background and design equations required to determine the optimum circuit component values were given together with the techniques needed to transform the lumped load network

into a distributed-element load network with inherent harmonic suppression characteristics. The circuit implemented delivered 22-dBm output power at 2.3 GHz, and achieved peak PAE of 64%, drain efficiency of 69%, and 11.6-dB power gain when operated from a 3-V supply voltage. Quadratic behavior of output power as a function of dc supply voltage as required for effective utilization of the amplifier in EER schemes has, although not exploited here, been confirmed. The amplifiers capability for handling a constant-envelope GMSK modulated signal was validated. Thus, the inverse Class-E amplifier has been shown to have extremely useful properties with good potential for insertion into a wide variety of mobile RF and microwave applications which are dc power sensitive.

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Thian Mury received the B.Sc. degree in electrical and electronic engineering (*summa cum laude*) from Atma Jaya University, Jakarta, Indonesia, and the M.Sc. degree in microelectronics from Delft University of Technology (TUDelft), Delft, The Netherlands, in 2001 and 2004, respectively. Since October 2004, he has been working toward the Ph.D. degree at the Queen's University of Belfast, Belfast, U.K.

His M.Sc. final project was conducted at Philips Semiconductors, Nijmegen, The Netherlands, in 2003–2004. His research interests include RF/Microwave analog circuit design and linearization techniques for high-frequency power amplifiers.

Vincent F. Fusco (S'82–M'82–SM'96–F'04) received the Bachelor's degree in electrical and electronic engineering (First Class Honors), in 1979, and the Ph.D. degree in microwave electronics and D.Sc. degree (awarded for his work on advanced front end architectures with enhanced functionality) from the Queen's University of Belfast, Belfast, U.K., in 1982 and 2001, respectively

He has been with the Queen's University of Belfast, where, since 1995, he has held a personal chair in High Frequency Electronic Engineering. His research interests include nonlinear microwave circuit design, and active and passive antenna techniques. The main focus for this research is in the area of wireless communications. At present he is technical director of the High Frequency Laboratories at ECIT www.ecit.qub.ac.uk, where he is also the Director of the International Centre for Research for System on Chip and Advanced Microwireless Integration, SoCaM. He has published 350 scientific papers in major journals and in referred international conferences, and is the author of two text books. He holds several patents and has contributed invited chapters to books in the field of active antenna design and EM field computation.

Dr. Fusco is a Fellow of the Royal Academy of Engineering and Fellow of the Institute of Electrical Engineers (IEE). In 1986, he was awarded a British Telecommunications Fellowship, and, in 1997, he was awarded the NI Engineering Federation Trophy for outstanding industrially relevant research.