High-Efficiency Broadband Parallel-Circuit Class E RF Power Amplifier With Reactance-Compensation Technique

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***Abstract*—Class E amplifier offers high efficiency approaching 100% for an ideal case. This paper introduces a first practical implementation of a novel broadband class E power amplifier design combining a parallel-circuit load network with a reactance compensation technique. The novel broadband parallel-circuit class E load network using reactance compensation technique has been discussed based on theory and its experimental verification. A proper guidelines method of designing a high-efficiency broadband class E power amplifier with an LDMOS transistor until the final prototype measurement and optimization will be discussed. In the measurement level, the drain efficiency of 74% at an operating power of 8 W and power flatness of 0.7 dB are achieved across a bandwidth of 136–174 MHz. The efficiency result is the highest result for VHF broadband frequency to date with a low supply voltage of 7.2 V. Simulations of the efficiency, output power, drain voltage waveform, and load angle (impedance) were verified by measurements and good agreements were obtained.**

***Index Terms*—Broadband, class E, high efficiency, parallel circuit, power amplifier, reactance compensation.**

I. Introduction

MODERN portable two-way radios are required to operate over a large number of channels for a long period from a small size battery. This means that an effective battery life solution is necessary. Since generally the power amplifier is a main consumer of dc power from a battery in radio transmitters, the straight way of improving battery life is to increase the power amplifier efficiency. As it is well known, a class E load network technique offers high operating efficiency approaching 100% for an ideal case.

The concept of class E with shunt capacitance was introduced by Sokal and Sokal in 1975 [1]. It was followed by a detailed design analysis for an idealized topology given by Raab [2]. Class E with shunt capacitance is a good choice to achieve a high-efficiency solution of an RF power amplifier [3]–[8], [12], [19], [20]. Reference [4] contains a detailed overview of a class E amplifier, including the conceptual target waveforms of switch voltage and current and design equations.

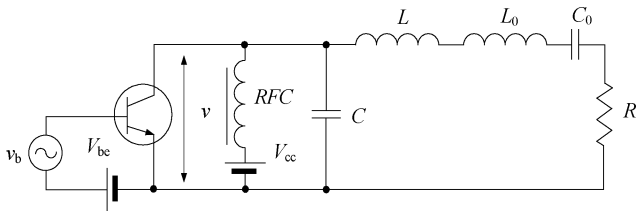

Fig. 1. Basic topology of bipolar class E power amplifier with shunt capacitance circuit.

The class E switching power amplifier concept aims to achieve high efficiency by designing the proper device (collector or drain) voltage and current waveforms so as to minimize losses on the active device since it is a main contributor to the efficiency degradation [9]. For a lossless operation mode, it is necessary to provide the following idealized optimum (nominal) conditions for voltage across the transistor operating as a switch just prior to the start of switch turn on at the moment $t = 0$, when the transistor is voltage saturated:

$$v(\omega t)\big|_{\omega t=2\pi} = 0 \tag{1}$$

$$\left.\frac{dv(\omega t)}{d(\omega t)}\right|_{\omega t=2\pi} = 0 \tag{2}$$

where v is the voltage across the switch.

The characteristics of a class E power amplifier can be determined by finding its steady-state device voltage and current waveforms. The basic circuit of a class E power amplifier with a shunt capacitance is shown in Fig. 1 where the load network consists of a capacitance C shunting the transistor, a series inductance L, a series fundamentally tuned L_0C_0 circuit, and a load resistance R.

In a common case, a shunt capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The collector or drain of the transistor is connected to the supply voltage by an RF choke with high reactance at the fundamental frequency. The active device is considered to be an ideal switch that is driven so as to provide the device switching between its on- and off-state operation conditions. As a result, the device voltage waveform is

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determined by the switch when it is "on" and by the transient response of the load network when the switch is "off."

The basic difference of the class E load network from a conventional complex-conjugate matching circuit in terms of impedances is that an *L*-type load network with shunt capacitor provides inductive impedance at the fundamental frequency seen by the switch and capacitive reactance at the harmonics.

As a result, the efficiency can be significantly increased at the expense of some degradation in power gain.

This paper introduces the first practical implementation of a novel broadband class E power amplifier combining a parallel circuit with a reactance compensation technique. A proper guidelines method of designing a high-efficiency broadband class E amplifier with an LDMOS transistor until the final prototype measurement and optimization will be discussed. This paper will discuss the MOSFET device, but the idea is still applicable for a bipolar device as well. In experiments, we have demonstrated drain efficiency of 74% at an operating power of 8 W for a frequency range of 136–174 MHz (relative bandwidth of 1.279 : 1) with an RD07MVS1 device (which was built with LDMOS technology from Mitsubishi, Kanagawa, Japan). The efficiency result is the highest result for VHF broadband frequency up to date with a low supply voltage of 7.2 V. Simulations of the efficiency, output power, drain voltage waveform, and load angle (impedance) were verified by measurements and good agreements were obtained. The actual lumped components and power amplifier models are developed to understand the correlation between simulation and measurement. An additional performance test such as stability and robustness are carried out in laboratory. The power amplifier is very stable and the transistor was not damaged by operating into 10 : 1 standing wave ratio (SWR) termination at the load.

II. Parallel-Circuit Class E

A. Theory of Parallel-Circuit Class E

In real practice it is impossible to realize the RF choke with infinite impedance at the fundamental and any harmonics. Moreover, using a finite dc-feed inductance has advantages of minimizing size, cost, and complexity of the overall circuit. Several analytical and numerical approaches were proposed to analyze the effect of a finite dc-feed inductance on the class E mode with shunt capacitance [10]–[12]. The class E power amplifier with a parallel circuit is a particular case of a family of the class E load networks with finite dc-feed inductance, which has no any additional reactive element (inductance or capacitance) connected in series to the L_0C_0 filter tuned to the fundamental frequency [8], [13], [14].

In the parallel-circuit class E power amplifier, the transistor also operates as an on-to-off switch and the shapes of the current and voltage waveforms provide a condition where the high currents and high voltages do not overlap simultaneously, which minimizes the power dissipation and maximizes the power amplifier efficiency. For the parallel-circuit class E power amplifiers, the circuit phase angles and values of the circuit elements differ from those of the class E power amplifier with shunt capacitance.

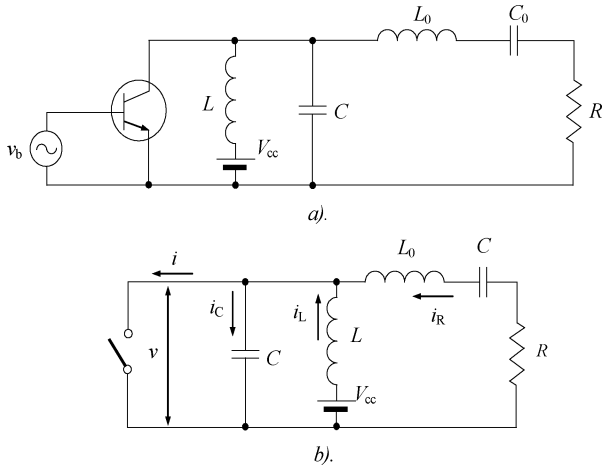

Fig. 2. Equivalent circuits of parallel-circuit class E power amplifiers.

A parallel-circuit class E topology is a very attractive solution having advantages over class E with shunt capacitance such as higher load resistance, low dc-feed inductance, and higher maximum operating frequency. For smaller product implementation, cost and size are the driven factor. Higher load resistance minimizes the impedance transformation ratio and number of matching sections to match with a standard load of 50 Ω. Moreover, especially for VHF and UHF frequencies, the output parasitic capacitance of the device is typically bigger than the required optimum.

The basic circuit of a switched-mode parallel-circuit class E power amplifier is shown in Fig. 2(a).

The load network consists of a parallel inductance L, parallel capacitance C, series L_0C_0-resonant circuit tuned on the fundamental, and load R. In a common case, a parallel capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network.

Let us introduce the same idealized assumptions to analyze the parallel-circuit class E power amplifier with optimum conditions given by (1) and (2) that were applied to analyze the class E power amplifier with a shunt capacitance. For the idealized theoretical analysis, it is advisable to replace the active device by the ideal switch, as shown in Fig. 2(b). Also let the output current flowing through the load be sinusoidal with the initial phase shift φ.

B. Analysis of Parallel-Circuit Class E

When switch is on for $0 \leq \omega t < \pi$, the voltage $v(\omega t) = V_{cc} - v_L(\omega t) = 0$, capacitor current $i_C(\omega t) = \omega C(dv(\omega t)/d(\omega t)) = 0$ and, consequently,

$$\begin{aligned} i(\omega t) &= i_L(\omega t) + i_R(\omega t) \\ &= \frac{V_{cc}}{\omega L}\omega t + I_R[\sin(\omega t + \varphi) - \sin\varphi]. \end{aligned} \tag{3}$$

When the switch is off for $\pi \leq \omega t < 2\pi$, the current $i(\omega t) = 0$, and the current $i_C(\omega t) = i_L(\omega t) + i_R(\omega t)$ flowing through the capacitance C can be rewritten as

$$\begin{aligned} \omega C\frac{dv(\omega t)}{d(\omega t)} = \frac{1}{\omega L}\int_{\pi}^{\omega t}[V_{cc} - v(\omega t)]\,d(\omega t) \\ + i_L(\pi) + I_R\sin(\omega t + \varphi). \end{aligned} \tag{4}$$

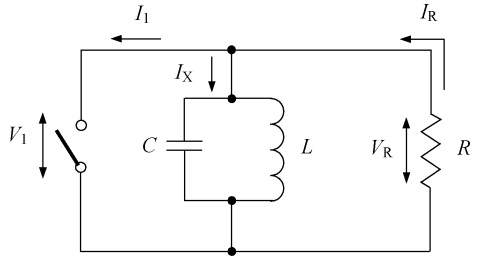

Fig. 3. Load network seen by device output at fundamental.

under the initial off-state condition $v(\pi) = 0$ and $i_L(\pi) = V_{cc}\pi/\omega L - I_R \sin\varphi$.

Equation (3) can be represented in the form of the nonhomogeneous second-order differential equation given by

$$\omega^2 LC\frac{d^2v(\omega t)}{d(\omega t)^2} + v(\omega t) - V_{cc} - \omega L I_R \cos(\omega t + \varphi) = 0 \quad (5)$$

of which a general solution can be obtained in the form of

$$\frac{v(\omega t)}{V_{cc}} = C_1 \cos(q\omega t) + C_2 \sin(q\omega t) + 1 - \frac{q^2 p}{1-q^2}\cos(\omega t + \varphi). \quad (6)$$

where $q = 1/\omega\sqrt{LC}$, $p = \omega L I_R/V_{cc}$, and the coefficients C_1 and C_2 are determined from initial off-state conditions.

To solve (6) with regard to three unknown parameters, it is necessary to use two optimum conditions given by (1) and (2) and to add an additional equation. From Fig. 3, which shows the load network seen by the switch at the fundamental frequency with fundamental current and voltage components, it follows that the fundamental voltage at the switch is applied directly to the load, i.e., its reactive component is equal to zero.

As a result, the additional equation is written as

$$V_X = \frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t + \varphi)\, d(\omega t) = 0. \quad (7)$$

In Fig. 4(a)–(c), the normalized load current and device, voltage, and current waveforms for idealized optimum parallel-circuit class E operation are shown, respectively. From device voltage and current waveforms, it follows that when the transistor is turned on, there is no voltage across the switch and current, i consists of the load sinusoidal and inductive currents flow through the device.

However, when the transistor is turned off, this current now flows through the parallel capacitance C. As a result, there is no nonzero voltage and current simultaneously. When this happens, no power loss occurs and an idealized device efficiency of 100% is achieved.

The fundamental frequency current $i_1(\omega t)$ flowing through the switch consists of two-quadrature components, as shown in Fig. 3, of which amplitudes can be found using Fourier formulas. Consequently, the load angle ϕ between the fundamental frequency voltage $v_1(\omega t)$ and current $i_1(\omega t)$ applied to the switch terminal is equal to

$$\phi = \tan^{-1}\left(\frac{I_X}{I_R}\right) = 34.244^\circ. \quad (8)$$

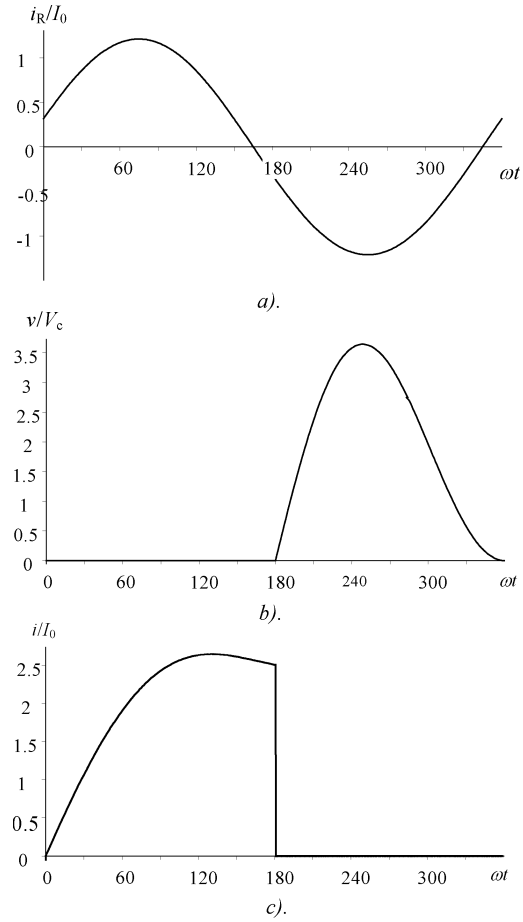

Fig. 4. Normalized: (a) load current and drain, (b) voltage, and (c) current waveforms for idealized optimum parallel-circuit class E.

Alternatively, the load angle ϕ can be represented as a function of load network elements as

$$\tan\phi = \frac{R}{\omega L} - \omega RC. \quad (9)$$

The optimum parallel inductance L and parallel capacitance C can be determined by

$$L = 0.732\frac{R}{\omega} \quad (10)$$

$$C = \frac{0.685}{\omega R}. \quad (11)$$

The optimum load resistance R for the specified values of supply voltage V_{cc} and output power P_{out} can be obtained by

$$R = 1.365\frac{V_{cc}^2}{P_{\text{out}}}. \quad (12)$$

The parameters of the series resonant circuit, depending on an assumed loaded quality factor Q_L, whose value should be as high as possible for a resonant single frequency case, are calculated by

$$C_0 = \frac{1}{\omega R Q_L} \quad (13)$$

$$L_0 = \frac{1}{\omega^2 C_0}. \quad (14)$$

The peak device current $I_{\max}$ and peak device voltage $V_{\max}$ can be determined from (3) and (6) as

$$I_{\max} = 2.647\, I_0 \tag{15}$$

$$V_{\max} = 3.647\, V_{cc}. \tag{16}$$

When realizing the optimum class E operation mode, it is important to know the maximum frequency $f_{\max}$ in which such an efficient operation mode can be achieved. In this case, it is advisable to establish a relationship between maximum operating frequency $f_{\max}$, device output capacitance C_{out}, and dc supply voltage V_{cc}. I_0 is the dc current drawn from the dc supply voltage.

The device output capacitance C_{out} gives the main limitation of the maximum operation frequency, as it is an intrinsic device parameter and cannot be reduced for a given active device. Thus, using (10) and (12), when $C = C_{\text{out}}$ gives the value of maximum operation frequency of

$$f_{\max} = 0.0798 \frac{P_{\text{out}}}{C_{\text{out}} V_{cc}^2} \tag{17}$$

which is 1.4 times greater than that one for the optimum class E power amplifier with shunt capacitance [14].

Consequently, despite the similar topologies shown in Figs. 1 and 2(a), the series LC circuit from the transistor collector to the load resistance R is tuned to the operating frequency in the Fig. 2(a) version corresponding to a parallel-circuit class E, and is tuned to a lower frequency in the Fig. 1 version corresponding to a class E with shunt capacitance, and the parallel resonator of C and L in Fig. 2 resonates at a frequency of 1.412 times the operating frequency, while the same components in Fig. 1 are not used as a resonator and are effectively only the capacitance C because the reactance of the RFC at the operating frequency is much larger than the reactance of C.

III. Reactance Compensation Technique

A. Theory of Reactance Compensation

The conventional design of a high-efficiency switched-mode tuned power amplifier requires a high-Q_L factor to satisfy the necessary harmonic impedance conditions at the output device terminal. However, if a sufficiently small value of the quality factor Q_L can be chosen, a high efficiency broadband operation of the class E power amplifier can be realized. For example, a simple network consisting of a series resonant LC circuit tuned on the fundamental and a parallel inductance provides a constant load phase angle of 50° in a frequency range of approximately 50% [16]. Such a load network based on class E mode with shunt capacitance has contributed to the drain efficiency of a MOSFET power amplifier of approximately 60% over a frequency bandwidth of 140–180 MHz at a supply voltage of 12 V [16].

For the first time, such a reactance compensation technique using a single-resonant circuit has been applied to the varactor tuned Gunn oscillator and parametric amplifier [17]. The reactance compensation circuit technique can also be applied to microwave transistor amplifier design because the input and output transistor impedances generally are simulated by series or shunt RLC circuits. For compensating the reactive part and transforming the active part of the output transistor impedance to the conventional load impedance, quarter- or half-wavelength transmission lines can be successfully used. The reactance compensation matching technique achieves for GaAs MESFET amplifiers a frequency range of 3.7–4.2 GHz with a gain ripple in limits of ±0.1 dB and a return loss of approximately 20 dB [18].

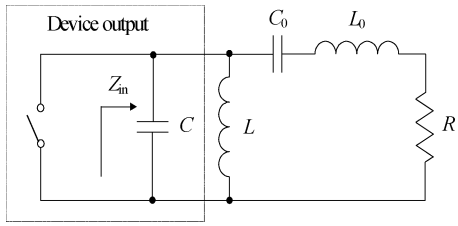

Fig. 5. Single reactance compensation circuit.

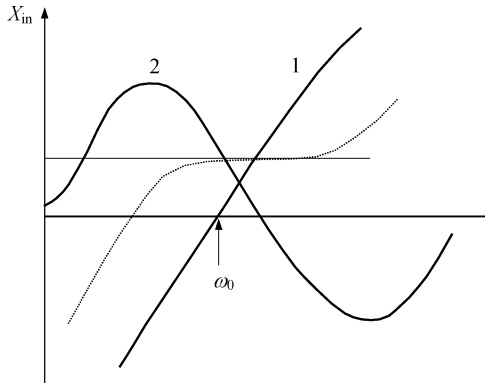

Fig. 6. Reactance compensation principle.

To describe the reactance compensation circuit technique, which is given in [7] for a load network with lumped parameters, consider the simplified equivalent load network with a series resonant L_0C_0 circuit tuned on the fundamental and a shunt LC circuit providing a constant load phase angle relative to the device output terminals, as shown in Fig. 5.

The reactance of the series and shunt resonant circuits vary with frequencies, increasing in the case of a series circuit and reducing in the case of a loaded parallel circuit near the resonant frequency ω_0, as shown in Fig. 6 by curves 1 and 2, respectively, where $X_{\text{in}} = \text{Im}Z_{\text{in}}$. Near the resonant frequency ω_0 of the series circuit with a positive slope of its reactance, the slope of the shunt circuit reactance is negative. This reduces the overall reactance slope of the load network (dotted line). With a proper choice of the circuit elements, a constant load angle over a very large frequency bandwidth is established.

This technique can be easily applied to the switched-mode class E power amplifier with a parallel circuit because its circuit configuration exactly corresponds to the single reactance-compensation circuit, which includes a parallel resonant circuit followed by a series one [7]. The parallel circuit configuration is directly applied for broadband operation conditions, unlike the class E circuit configuration with shunt capacitance and series inductance. In this case, the optimum phase angle ϕ and

load resistance R of the load network can be obtained from (8) and (12), respectively. It needs only to calculate the optimum loaded quality factor of the series L_0C_0 filter to maximize the frequency bandwidth.

B. Analysis of Parallel Circuit With Reactance Compensation

The load network input admittance $Y_{\rm in} = 1/Z_{\rm in}$ can be written by

$$Y_{\rm in} = \left(j\omega C + \frac{1}{j\omega L} + \frac{1}{R + j\omega' L_0}\right) \tag{18}$$

where $\omega' = \omega\left(1 - \omega_0^2/\omega^2\right)$ and $\omega_0 = 1/\sqrt{L_0C_0}$ is the resonant frequency.

The parameters of the series L_0C_0 resonant circuit must be chosen so as to provide a constant phase angle of the load network over a broadband frequency bandwidth. This bandwidth will be maximized if at the resonant frequency ω_0

$$\left.\frac{dB(\omega)}{d\omega}\right|_{\omega=\omega_0} = 0 \tag{19}$$

where $B(\omega) = {\rm Im}Y_{\rm in} = -\left(1 - \omega^2 LC\right)/\omega L$ is the load network susceptance. In this case, to simplify the calculation procedure, a concept of the susceptance reactance compensation is used, as it is similar to the reactance compensation technique. An additional equation can then be written by

$$C + \frac{1}{\omega^2 L} - \frac{2L_0}{R^2} = 0. \tag{20}$$

As the final result, the series capacitance C_0 and inductance L_0 can be calculated from

$$L_0 = 1.026\frac{R}{\omega} \tag{21}$$

$$C_0 = \frac{1}{\omega^2 L_0}. \tag{22}$$

IV. Design of Parallel-Circuit Class E With Reactance Compensation Technique

A. Design Objective

The main objective of our design is to achieve high efficiency of the power amplifier for a wide range of frequencies from 136 to 174 MHz with discrete components. Thermal and battery life of a two-way portable radio can be improved by enhancing the efficiency of the power amplifier. In a transmitter chain line up, a major current drain (approximately 80%) is due to the final power amplifier, and the rest of current is consumed by a driver amplifier. Thus, the objective of this paper is to improve efficiency of a final power amplifier by using a class E switching mode. An efficiency enhancement of the final power amplifier with an output power of 8 W operating in a parallel-circuit class E mode using a single reactance compensation technique across bandwidth from 136 to 174 MHz is our objective. Due to stringent requirements of the product such as size and cost, parallel-circuit class E technique seems to be a very practical solution. This allows the use of a finite dc-feed inductance instead of an RF choke. A single reactance compensation technique provides a constant load angle over a wide frequency band.

TABLE I
Design Goal of the Broadband Class E Parallel-Circuit With Reactance Compensation Technique

Parameter	Goal
Bandwidth	136 MHz - 174 MHz
Power Flatness	< 0.8 dB
Efficiency at 8W	75%
Stability	No oscillation

The design goal is shown in Table I. We are aiming to achieve 75% efficiency at an output power of 8 W across a bandwidth from 136 to 174 MHz. Due to the requirement of the power margin, we set the power flatness less than 0.8 dB for operating across a broad bandwidth. It is a requirement to achieve a stable power operation with 10 : 1 SWR termination at the load. In a real application, the load will be connected with an antenna.

B. Design Methodology

The methodology in the broadband class E power amplifier development was as follows.

1) A realistic specification for a transistor amplifier design was considered.
2) The load network parameters was obtained based on an analytical derivation of a parallel circuit with the reactance compensation approach.
3) *L*-type (or *T* type) low-Q matching circuit was incorporated to match a class E load network with a 50-Ω load.
4) The complex-conjugate input matching circuit design to provide fast switching was considered.
5) The circuit was then simulated to validate its operation, and components were tuned to obtain the optimum switching condition.
6) A prototype board was built and measured.
7) Load impedance (angle) was measured using a vector network analyzer (VNA) and the components were optimized.
8) Final optimization of the output load network monitoring drain voltage was carried out.

The transistor device chosen in this design is Mitsubishi's RD07MVS1 (built with LDMOS technology). The saturation resistance R_{DSON} and output parasitic capacitance C_{OSS} of the device are 0.17 Ω and 60 pF, respectively. Breakdown voltage ${\rm BV_{DS}}$ of the device was rated at 35 V (minimum). The specification datasheet of the RD07MVS1 device is summarized in Table II.

The optimum input impedance $Z_{\rm IN}$ is the impedance that needs to be achieved at 155 MHz. $Z_{\rm IN}$ is verified with a source–pull impedance technique via harmonic balance (HB) simulation. To operate at a class B bias condition, the gate voltage must be set to a $V_{\rm th}$ of 1.8 V. $V_{\rm th}$ is verified with transfer characteristics I_D–$V_{\rm GS}$ simulation.

Referring to the equation derivation of a parallel-circuit class E power amplifier, an optimum value of the resistance R that needs to be seen by the device is given by (12), thus resulting in

$$R = 1.365\frac{7.2^2}{8.5} = 8.3\,\Omega. \tag{23}$$

TABLE II
SUMMARIZED SPECIFICATIONS DATASHEET OF RD07MVS1

Parameter	Value
R_{DSON}	0.17 Ω
C_{OSS}	60 pF @ 7.2 V
V_{th}	1.8 V
Z_{IN}	$1.55 + j5.53$ Ω
BV_{DS}	35 V

To achieve an output power of 8.5 W with a supply voltage of 7.2 V, a value R of 8 Ω (approximately) is required. Thus, at this stage, the load resistance must be set to 8 Ω and the impedance transformation network is incorporated to transform an 8-Ω load resistive impedance to a 50-Ω load at the fundamental frequency. In order to achieve the required transformation and provide satisfactory suppression of harmonics in the load, a three-stage cascaded low-pass-type transformer was proposed. The requirement of harmonic suppression (especially second harmonic) in the two-way radio application is typically more than 73 dBc. However, an additional harmonic filter is recommended for this purpose.

To meet the wide bandwidth requirement, both the parallel LC circuit and series resonant circuit L_0C_0 are tuned on a center bandwidth frequency of 155 MHz. According to (21) and (22), L_0 and C_0 should be equal, respectively, to

$$L_0 = 1.026\frac{8}{330\pi} = 7.9\ \text{nH} \tag{24}$$

$$C_0 = \frac{1}{(330\pi)^2 L_0} = 133\ \text{pF}. \tag{25}$$

Theoretical values for the parallel-circuit class E capacitance C and inductance L should be in accordance to (10) and (11) as

$$C = \frac{0.685}{(2480\pi)} = 83\ \text{pF} \tag{26}$$

$$L = \frac{0.732^{*}8}{(330\pi)} = 5.6\ \text{nH}. \tag{27}$$

A two-stage low-pass filter is used to transform 50 Ω to Z_{IN}. Under a conjugate matching condition, to satisfy input broadband frequency from 136 to 174 MHz, the quality loaded factor Q must be kept low. In this design, a Q of 2 is used. The careful input matching network design is important as well to provide a fast enough driving on–off state.

DC coupling and RF bypass of 330 pF and 1.8 nF, respectively, are implemented in the design. With the aid of simulation, the K factor and pole/zero plots were identified. Stability is guaranteed by applying feedback stabilization circuits of 100 Ω and 0.1 μF. The components are properly grounded and bypassed on board level. A complete circuit schematic of the complete high-efficiency broadband parallel-circuit class E power amplifier combined with the reactance compensation technique is shown in Fig. 7.

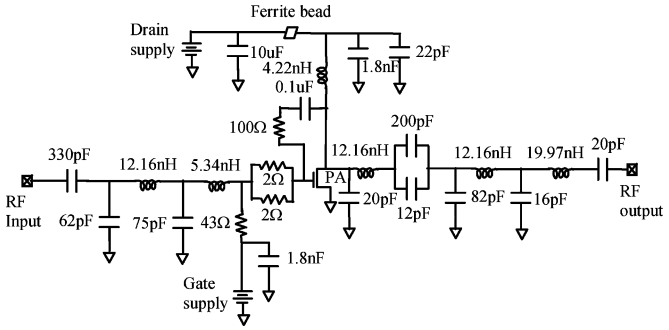

Fig. 7. Complete schematic of 8-W broadband parallel-circuit class E power amplifier with reactance compensation technique (136–174 MHz).

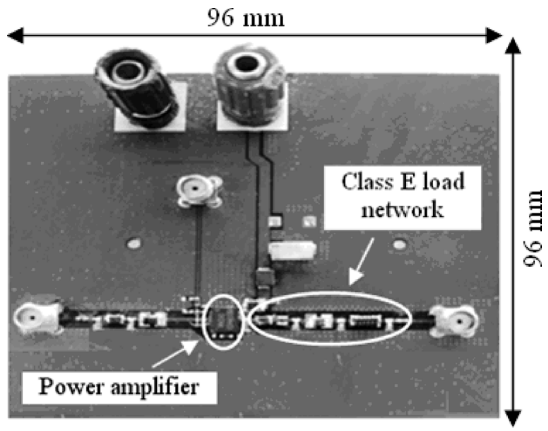

Fig. 8. Prototype board of broadband parallel-circuit class E power amplifier with reactance compensation technique.

V. MEASUREMENT PROTOTYPE

In order to experimentally validate the analytical derivation of a parallel-circuit class E load network combining the reactance compensation technique, a prototype board of a class E power amplifier was designed and fabricated.

A photograph of the prototype board is shown in Fig. 8. In our experiment, a test board using FR-4 material was fabricated. The printed circuit board (PCB) has a dielectric ε_r of 4.5 and a thickness h of 14 mil. The board basically consists of the RF input and output ports, two voltage supply feeds, two-section low-pass input matching, and a output load network with three-stage output matching. The board size is 96 mm × 96 mm. Heat sink is mounted at the bottom of PCB to provide good transferred heat. The capacitors represent a ceramic and tantalum type, and inductors represent an air wound type.

A three-section low-pass output matching circuit transforming the impedance from an 8- to a 50-Ω load is slightly optimized in the board level to provide sufficient harmonic suppression. The input impedance matching circuit consists of the two low-pass matching sections. The drain supply voltage is 7.2 V and quiescent current is set close to deep class B. However, we observed that biasing slightly higher than class B can achieve a good performance between power and efficiency. The RD07MVS1 (LDMOS) power amplifier requires a positive bias voltage. A typical gate voltage from 1.8 to 2 V has been applied to the gate voltage.

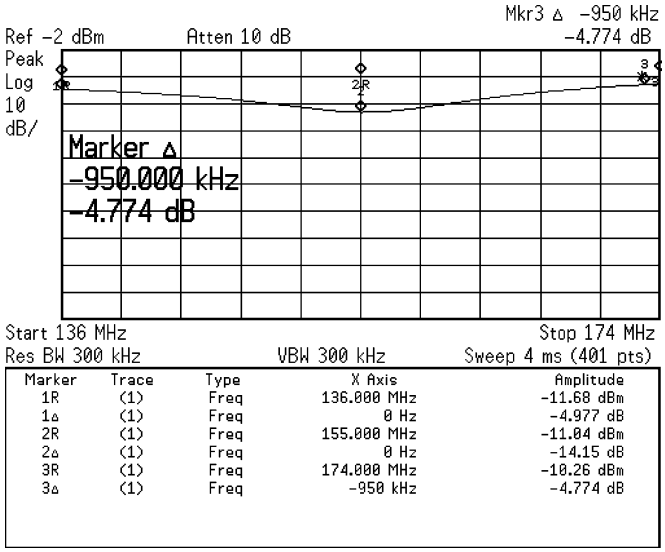

Fig. 9. Measured results of return loss of the input matching network across frequency bandwidth from 136 to 174 MHz.

A two-stage input matching network is used at the power amplifier input. The optimum source impedance of the amplifier device is measured using a source–pull measurement technique and good agreement is obtained with simulation. The measured value of optimum input impedance is close to the specifications given in Table II. The input return loss of the matching network is more than -9 dB from 142 to 167 MHz. However, a return loss of -5 dB is achieved at the bandwidth edges of 136 and 174 MHz. The return loss of the matching network across the entire bandwidth from 136 to 174 MHz, which was captured with Agilent's E-4445 performance spectrum analyzer (PSA), is shown in Fig. 9.

Stable operation without parasitic oscillations is provided with a feedback network and gate loading resistor at the input of the amplifier. The feedback value of 100 Ω (resistor) and 0.1 μF (ceramic capacitor) are predicted in the design level. Gate loading resistors of 2 Ω (in parallel form) are placed at the gate of the amplifier. In addition, a ferrite bead is implemented at the drain line together with 10 μF (tantalum capacitor) and 22 pF (ceramic capacitor) as a precaution of low-frequency parasitic oscillation. A crucial stability test with a termination of 10 : 1 voltage standing-wave ratio (VSWR) was carried out. No oscillation is reported under this condition and the power amplifier operation is very stable. A robustness test is performed in the measurement level with a termination of 10 : 1 VSWR with continuous transmission for 20 min. Maximum peak of drain voltage was measured at approximately 32.5 V, which is still lower than $\mathrm{BV_{DS}}$. No degradation in performance, such as power and efficiency, are reported.

It is important to understand the correlation between simulation and measurement when the load elements are chosen based on actual component models. The equivalent series resistance (ESR) of the lumped components such as a resonant inductor, a resonant capacitor, a decoupling capacitor, an RF bypass capacitor, a matching capacitor, and an inductor were obtained from the RCL library. The lumped components were developed for Agilent's Advanced Design System (ADS) simulation application. All capacitors were from Murata Inc., Kyoto, Japan, except

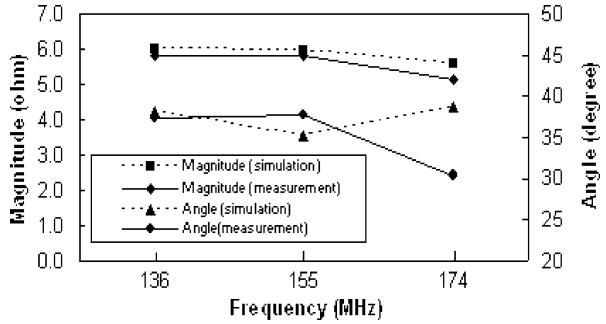

Fig. 10. Simulated and measured results of magnitude and angle of the broadband parallel-circuit class E load network with reactance compensation.

Taiyo Yuden Inc., Schaumburg, IL, for the shunt capacitor, and air wound inductors are from Coilcraft Inc., Tokyo, Japan.

Initially, without any tuning, we could not achieve a good performance of class E switching conditions across the entire bandwidth from 136 to 174 MHz. Therefore, it was then necessary to verify how accurate a value of the load impedance using real elements is. A quick technique to tune the load network is to observe the load impedance (angle) of the load network. This was done by using Hewlett-Packard's network analyzer (HP6778). However, excessive inductance of the SMA connector must be taken into account with a proper port extension method during the impedance measurement. With tedious optimization of the load network, the load angle was tuned to an optimum value of the class E switching conditions. The simulated and measured results of a load angle for broadband frequency bandwidth from 136 to 174 MHz are shown in Fig. 10.

The load angle (impedance) has good accuracy between simulation and measurement. A major variation occurs at 174 MHz where the measured data showed a reduction of 8° compared to simulation. Take note that the actual component model (RCL) for each element is used during the simulation to understand the correlation.

The input RF signal level is important to provide class E switching action. The input RF level could be different with respect to operating frequency. Thus, it is necessary to determine the input RF level to achieve optimum broadband class E performance. The measured results of a parallel-circuit class E power amplifier with a reactance compensation technique at a center bandwidth frequency of 155 MHz are shown in Fig. 11. An input RF signal of 28 dBm is required to provide optimum performance of power and efficiency at an operating frequency of 155 MHz.

The broadband frequency performance of a parallel-circuit class E power amplifier with reactance compensation is shown in Fig. 12.

The maximum drain efficiency of 74.5% with an output power of 8.77 W was achieved at 155 MHz. The overall variations of the drain efficiency were less than 1.3% over the entire frequency range from 136 to 174 MHz. The power flatness is 0.7 dB across the entire range with maximum degradation at a high bandwidth frequency of 174 MHz where it drops down to 7.25 W.

The power gain is 12.2 dB at 155 MHz, dropping at both edges by 0.7 dB at 136 MHz and 1.6 dB at 174 MHz. There

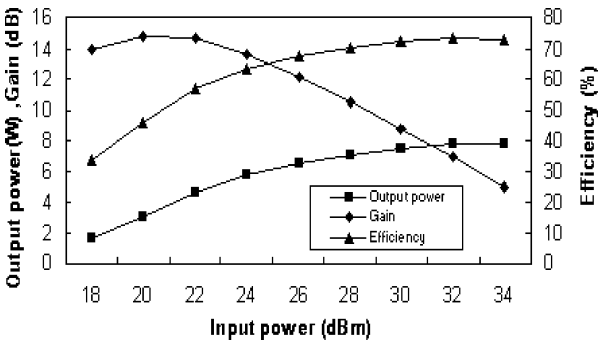

Fig. 11. Measured results of output power, gain, and efficiency versus different input power at an operating frequency of 155 MHz.

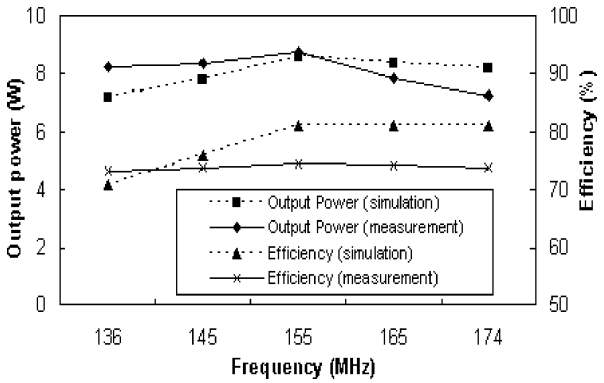

Fig. 12. Simulated and measured results of output power and efficiency of broadband parallel-circuit class E power amplifier with reactance compensation.

TABLE III
SUMMARIZED MEASUREMENT RESULTS OF HIGH-EFFICIENCY PARALLEL-CIRCUIT CLASS E POWER AMPLIFIER WITH REACTANCE COMPENSATION

Parameters	Performance
Operating Bandwidth (MHz)	136 - 174
Output Power (W)	8
Efficiency (%)	74
Power Flatness (dB)	± 0.7
Stability with 10:1 VSWR	Stable
Robustness with 10:1 VSWR	No degradation

is a trend between simulation and measurement of drain efficiency, current drain, and output power. The simulated efficiency degrades by 6% at 136 MHz, but stays almost constant from 155 to 176 MHz. The output power trend for measured data is decreasing as an increment of frequency, but is the other way around for simulation results. However, the output power behavior of measured values is quite close to the simulated value. In the measurement level, the efficiency is increased from 5% to 6% with the increase of the drain supply voltage to 8.5 V. A performance summary of a high-efficiency parallel-circuit class E power amplifier with reactance compensation is shown in Table III.

During a tuning procedure, both input and output load networks were tuned for maximum drain efficiency. The amount

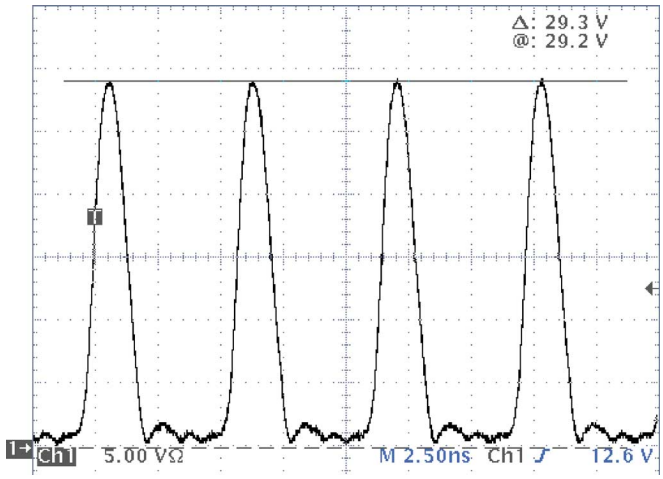

Fig. 13. Measurement results of drain voltage (horizontal: 2.5 ns/div.; vertical: 5 V/div). The peak voltage value of the drain voltage is measured around 29.3 V.

of external capacitance was varied until an optimum condition of the class E switching action was obtained while monitoring drain voltage. The remainder of the shunt capacitance was formed by the intrinsic MOSFET feedback and output capacitance, dc-feed inductor stray capacitance, MOSFET heat sink to ground capacitance, and input capacitance of the scope [9]. To satisfy class E optimum switching conditions across the entire frequency bandwidth from 136 to 174 MHz, the external shunt capacitance of 13 pF (20 pF in simulation) was chosen based on the observation of the drain voltage waveform. Fig. 13 shows the measured drain voltage waveform at a nominal output power of 8 W.

For the measurement, Agilent's 1-GHz oscilloscope (4GSa/s) 54832B digital signal oscilloscope (DSO) is used with a 50-Ω measurement mode. A series resistor of 430 Ω is connected in between the high ohmic voltage probe and drain of the transistor. A dc-coupling capacitor in series with the resistor is important to block the dc current. The drain voltage is attenuated with scale of 20 dB for safety purposes of the oscilloscope without loading the drain voltage. The peak voltage of the drain voltage is measured around 29.3 V at the operating frequency of 155 MHz. The peak voltage is around 29 V across the bandwidth from 136 to 174 MHz. A duty ratio close to 45% is achieved across this bandwidth. The saturation voltage is very low, approximately 2.1 V during the time the switch is turned on. The duty ratio should be selected within the 35%–65% range with a specific duty ratio determined to yield suitable device voltage and current stresses [9]. Maximum peak voltage is observed around 32 V with a load termination of 10 : 1 SWR.

VI. CONCLUSION

The practical verification of a novel idea of a broadband parallel-circuit class E power amplifier with reactance compensation has been presented in this paper. The theoretical analyses were derived and proven by measurements with a prototype board. An efficiency of 74% at an operating power of 8 W across a frequency bandwidth from 136 to 174 MHz with power flatness of 0.7 dB has been demonstrated at the measurement level.

The efficiency result is the highest result for VHF broadband frequency up to date with a lower supply voltage of 7.2 V. There is a good trend between simulation and measurement, especially for load angle (impedance) and output power, drain efficiency, and dc current. This exploration has led to the conclusion that a class E mode parallel-circuit combined with the reactance compensation technique is a very attractive and simple practical solution for improving efficiency of the power amplifier over a wide frequency range.

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