

# Design Equations for Class-E Power Amplifiers

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**Abstract**—In literature, it is widely accepted that the design of Class-E Power Amplifier (PA) with finite dc feed inductance requires a long iterative solution procedure. To avoid such iterative solution methods, analytical design equations should be known. The problem associated with the finite dc feed inductance Class-E PA is usually ascribed to the fact that the circuit element values are transcendental functions of the input parameters which is assumed to prevent the derivation of exact or fully analytical design equations.

Using a proper analytical method, exact design solutions for Class-E PA with any inductor value can however be derived. A mathematically exact analysis of the idealized Class-E PA with finite dc feed inductance has been done and analytical expressions showing the relation between the circuit elements and the input parameters are found. These analytical expressions have been simplified to obtain explicit, relatively simple design equations. In this paper, we present these relatively simple design equations. Using these design equations, Class-E PA with finite dc feed inductance can be designed without iterative design procedures.

The current paper discusses these simplified versions of the exact solution of general Class-E PA with finite dc feed inductance

**Key Words**- Power Amplifier, Class-E.

## I. INTRODUCTION

Since its introduction [1] many aspects of the Class-E power amplifier has been extensively studied [1]- [8]. One such aspect is the Class-E operation with a finite dc-feed inductance. It is well-known that using finite dc feed inductance instead of an RF-choke in a Class-E PA has significant benefits [4], [7], [8], including:

- a reduction in overall size and cost
- a higher load resistance, which typically results in a more efficient output matching network [7]
- a possible reduction in the required supply voltage, which might enable the implementation of the Class-E PA in low-voltage technologies.
- larger switch parallel capacitor  $C$  (Fig. 1) for the same supply voltage, output power and load. This enables higher frequency of operation.

Further benefits of using finite DC feed inductance are seen if the Class-E PA is used in an envelope elimination and restoration (EER) system [3].

An early analysis of Class-E PA with finite dc feed inductance is published by [4] in 1987, followed by e.g. [5] and [6]. The common property of all these papers [7] is that the procedure for obtaining the final circuit design elements is either long, complex and iterative [4], [5] or does not provide

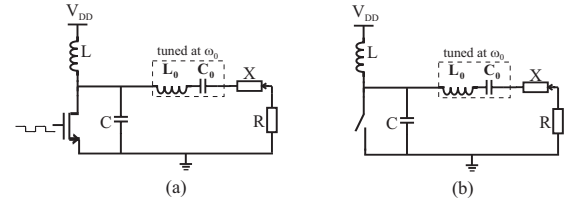


Fig. 1. (a) Single-ended Class-E Power Amplifier with Finite DC-Feed Inductance (b) Idealized model of single-ended Class-E Power Amplifier with Finite DC-Feed Inductance

much insight into the circuit design or is not analytically exact [6].

In this paper, we present design formulas showing the relation between the input parameters and the circuit element values of the finite dc feed inductance Class-E PA. The presented design formulas are based on a mathematical analysis of the ideal Class-E PA with finite dc feed inductance. The complex analytical solution for the design formulas has been simplified and the resulting relatively simple design equations are presented in this paper.

In the analysis, a number of widely accepted assumptions are made, including an ideal switch, a sinusoidal output current on the load resistance and 50% duty cycle. Using fourier series and well-known Class-E conditions [2], [8] a set of non-linear equations is obtained. This set of non-linear equations can be solved which yields analytical expressions that describe the relation between the circuit elements and parameters like supply voltage  $V_{DD}$ , output power  $P_{OUT}$  and operating (angular) frequency  $\omega$ .

Obtaining design equations instead of iterative solution methods for the finite dc feed inductance Class-E PA is also pursued in [7]. In [7], numerically obtained results are interpolated by Lagrange polynomials in order to obtain approximate design equations. However, the design equations given in [7] do not take into account capacitive values for  $X$ . Our analytical solution and simplified design equations clearly show that  $X$  can be capacitive as well as inductive; which can be useful in Class-E PA designs with finite drain inductance. Besides, in contrast to the work in [7], our design approach requires no initial value for the finite drain inductor.

As an application for the use of the generalized Class-E design equations, this paper also shows that the frequency-power product ( $\omega \cdot P_{OUT}$ ) can be optimized which, for low voltage operation, leads to a non-conventional Class-E design

equations with a finite dc feed inductance.

## II. CLASS-E DESIGN EQUATIONS

For easy design of a Class-E PA, the relation between the input parameters ( $V_{DD}$ ,  $P_{OUT}$  and  $\omega$ ) and the circuit element values ( $L$ ,  $C$ ,  $X$  and  $R$ ) should be known. In the remainder of this paper, we use a design set  $\{K_L, K_C, K_P, K_X\}$  that relates input parameters to circuit element values as shown in Table-1.

Table 1: Class-E Design Set

$$\begin{aligned} K_L &= \omega L / R \\ K_C &= \omega C R \\ K_P &= P_{OUT} R / V_{DD}^2 \\ K_X &= X / R \end{aligned}$$

Note that  $L_0$  and  $C_0$  seen in Figure 1 can be determined from the chosen loaded quality factor ( $Q_L = \omega L_0 / R$ ) where  $\omega = 1/\sqrt{L_0 C_0}$ .

A mathematical analysis for the Class-E PA with RF-choke is given in [2], yielding  $K_C = 0.1836$ ,  $K_P = 0.5768$ ,  $K_X = 1.125$  and  $K_L \rightarrow \infty$  for this specific case.

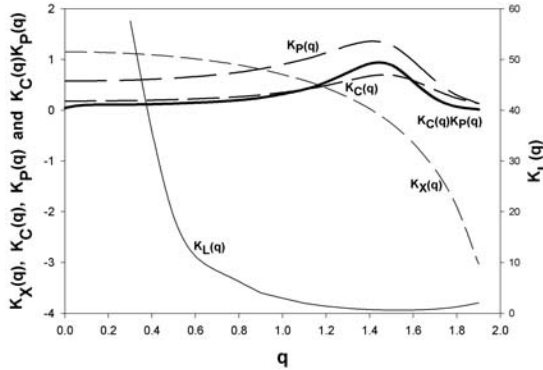


Fig. 2. The Class-E design set  $K_X(q)$ ,  $K_C(q)$ ,  $K_P(q)$ , and  $K_L(q)$  as a function of  $q$ . The  $K_C(q)K_P(q)$  curve is used in §II-B.

A similar mathematical analysis for Class-E PA with finite dc feed inductance shows that each element of the design set  $\{K_L, K_C, K_P, K_X\}$  can be expressed in terms of  $q$  where  $q = 1/(\omega\sqrt{LC})$ . It can be shown that  $q$  can take any real positive value except for a singular point at 1. It follows from this that infinitely many design sets exist for the Class-E PA, corresponding to infinitely many sets of  $\{K_L, K_C, K_P, K_X\}$ . It can easily be shown that properties such as high load resistance, low supply voltage operation, high frequency operation etc. occur in the range  $0 < q < 1.9$ .

In Figure 2, the elements of the design set for finite dc feed inductance Class-E PA is plotted for the range  $0 < q < 1.9$ . It can be seen in Figure 2 that as  $q$  approaches to zero,  $K_L$  asymptotically goes to infinity and consequently the design equations for the finite dc feed inductance Class-E PA approaches to the Class-E PA with an RF-choke.

## A. Simplified Design Equations

The plot in Figure 2 can roughly be subdivided into 4 regions. Of these 4 regions, 2 are not very interesting in the context of this paper:

- for low values of  $q$ , e.g.  $q < 0.6$ , the values of  $K_C$ ,  $K_P$  and  $K_X$  hardly change and  $K_L > 10$ . In this region the design formulas of Class-E with an RF-choke can be used.
- for large  $q$ , e.g.  $q > 1.65$ , both  $K_C$  and  $K_P$  approach to zero. It follows from Table 1 that this corresponds to extreme values of either input parameters or circuit element values.

The curves shown in Figure 2 result from complex exact analytical expressions. In the middle region in Figure 2 the curves can be approximated reasonably well by simple quadratic polynomial fits, given in Table-2 and Table-3 for the ranges  $q \in [0.6, 1]$  and  $q \in [1, 1.65]$  respectively. The error between the fits and the exact analytical solution is  $\approx 2\%$  in the respective  $q$ -ranges.

Table 2: Design set for ( $0.6 < q < 1$ )

$$\begin{aligned} K_L(q) &= 44.93q^2 - 94.32q + 52.46 \\ K_C(q) &= 0.426q^2 - 0.379q + 0.3 \\ K_P(q) &= 0.74q^2 - 0.6q + 0.76 \\ K_X(q) &= -0.73q^2 + 0.411q + 1.03 \end{aligned}$$

Table 3: Design set for ( $1 < q < 1.65$ )

$$\begin{aligned} K_L(q) &= 8.085q^2 - 24.53q + 19.23 \\ K_C(q) &= -6.97q^3 + 25.93q^2 - 31.071q + 12.48 \\ K_P(q) &= -11.90q^3 + 42.753q^2 - 49.63q + 19.70 \\ K_X(q) &= -2.9q^3 + 8.8q^2 - 10.2q + 5.02 \end{aligned}$$

In Class-E PA design, high values of  $K_C$  and  $K_P$  are preferred for high frequency of operation and low supply voltage operation respectively. The presented generalized Class-E design sets represent infinitely many different Class-E realizations. This implies that properties can be traded against each other to get optimum performance for each specific application. As an example the next section discusses optimization for a maximum frequency-power product.

## B. Frequency Power Product

In order to design a finite dc feed inductance Class-E PA, the input parameters ( $\omega$ ,  $V_{DD}$  and  $P_{OUT}$ ) and the value of one of the circuit elements ( $L$ ,  $C$ ,  $R$  and  $X$ ) must be specified. Note that for  $q < 1.412$  the reactance  $X$  is positive and hence then  $X = \omega L_X$ ; for  $q > 1.412$  the reactance  $X$  is capacitive with  $X = -\frac{1}{\omega C_X}$ . By selecting a value for  $q$ , all the remaining three circuit element values are obtained. This  $q$  is therefore a free design parameter that can be used for optimization purposes.

It follows from Table 1 that the frequency-power product for an ideal Class-E PA with finite dc feed inductance can be generically expressed as

$$\omega P_{OUT} = K_P(q) V_{DD}^2 \cdot s \quad (1)$$

where  $s$  is any element in the set  $S$  or the geometric mean of

any elements of the set  $S$ ; this set  $S$  is defined as

$$S = \left\{ \frac{K_L(q)}{L}, \frac{K_C(q)}{R^2 C}, \frac{K_X(q)}{L_X} \right\} \quad q < 1.412$$

$$S = \left\{ \frac{K_L(q)}{L}, \frac{K_C(q)}{R^2 C}, \frac{-1}{K_X(q) R^2 C_X} \right\} \quad q > 1.412$$

The choice for using one of the many resulting expressions for (1) is based on boundary conditions. In modern technologies, the breakdown limits of the active device (the switch) sets the maximum value for  $V_{DD}$ . The capacitance  $C$  is lower-limited by the output capacitance of the active device, which is also technology-related. The value of  $R$  is lower-limited by demands on maximum acceptable losses of the output matching network. The parasitic inductances present in the circuit determines the lowest value of inductors ( $L$ ,  $L_X$ ). The acceptable physical sizes and the quality factor determines the highest value of inductors in practical implementations.

For a Class-E PA designed in low-voltage technologies the  $R$  and  $C$  are usually lower-bound, then (1) can be rewritten into (2) which explicitly includes the limited components.

$$\omega P_{OUT} = K_P(q) V_{DD}^2 \frac{K_C(q)}{R^2 C} \quad (2)$$

It directly follows from (2) that maximum  $f \cdot P_{OUT}$  is obtained at the maximum of  $K_P(q) K_C(q)$ . The  $K_P(q) K_C(q)$  curve is also shown in Figure 2, having its maximum at  $q=1.442$ . The design set for  $q = 1.442$  is given in Table 4.

Table 4: Design set for maximum  $f \cdot P_{OUT}$

$K_L = 0.689$
$K_C = 0.698$
$K_P = 1.355$
$K_X = -0.082$

For a Class-E PA with limited  $V_{DD}$ ,  $R$  and  $C$  the  $f \cdot P_{OUT}$  product is up to 9 times larger if the the design data in Table 4 is used instead of RF-choke Class-E design equations.

### III. MEASUREMENT RESULTS

In this section the design equations for the finite dc-feed inductance Class-E PA and the related advantages in terms of frequency-power product are verified experimentally.

The designed power amplifiers in this section are only low frequency demonstrators of the validity of the design equations rather than targeting a specific application. Observing the drain voltage waveforms on the oscilloscope thus verifying the Class-E operation at relatively low frequencies (4 MHz-17 MHz) is easy. Verification of the design equations at GHz frequency ranges were done with transient and periodic-steady-state (pss) analysis in Spectre circuit simulator with transistor models in 90nm CMOS technology.

The Class-E PAs were constructed by using discrete transistor (MAX 2601), and discrete passive components (ceramic capacitors, metal film resistors and air-core inductors). In the measurements, an Agilent 33250A signal source was used together with 54642A Oscilloscope, 34401A Digital Multimeter and E3631A DC Power Supply. The gate of the transistor is

	$q = 0$	$q = 0.8$	$q = 1.412$	$q = 1.65$
$f$ (MHz)	10.24	10.24	10.24	10.24
$P_{OUT}$ (mW)	72.2	96.6	171.1	103.5
$P_{DC}$ (mW)	87.2	114.8	203.2	134.2
$\eta$	82.8%	84.4%	84.2%	77.1%
$L$ (uH), $C$ (pF)	21, 133	2, 195	0.256, 495	0.259, 359
$R$ ( $\Omega$ ), $X$ ( $\Omega$ )	22, 25.4	22, 22.3	22, 0	22, -19.4
$V_{DD}$ (V)	2	2	2	2
$Q_L$	6	6	6	6

Table 5: Design Details and Measurement Results for Class-E PA for  $q = 0, 0.8, 1.412, 1.65$

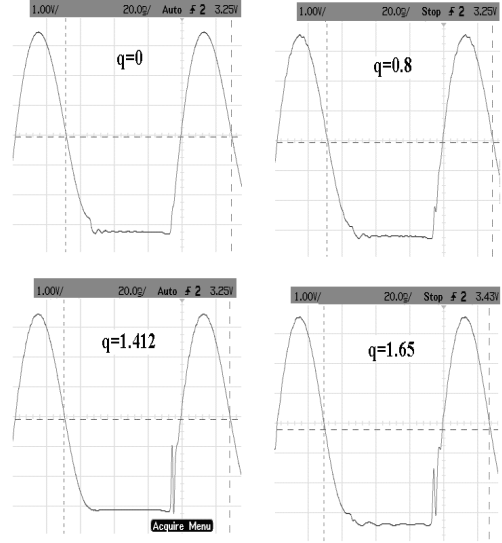


Fig. 3. Drain waveforms of the Class-E PA for  $q = 0, 0.8, 1.412, 1.65$  with the given design specs in Table 5

driven by a square wave signal from the signal source. The rise and fall time is chosen as 10% of the period of the square signal.

#### A. Design Set

Four Class-E PAs ( $q = 0, 0.8, 1.412$  and  $1.65$ ) by using the design set  $K$  has been designed. The design details are given in Table 5. The same  $R$  and  $V_{DD}$  are used in all the four PAs. It can be derived from the design set  $K$  that

$$P_{OUT} = K_P(q) \frac{V_{DD}^2}{R} \quad (3)$$

Therefore, for given  $R$  and  $V_{DD}$  the output power varies with  $K_P(q)$ ; which is verified with the measurement results as seen in Table 5. The highest output power is obtained for  $q = 1.412$  where  $K_P(q)$  reaches it's maximum value as shown in Fig 2.

The observed waveforms seen in Fig 3 are showing the validity of the design equations. Tolerance ( $\approx 5\%$ ) and finite quality factor ( $\approx 20$ ) in the passive circuit elements and non-zero switch (transistor) on resistance ( $\approx 0.7 \Omega$ ) cause small deviation in the Class-E waveforms as observed in Fig 3

	$q = 0$	$q = 1.442$
$f$ (MHz)	4.4	16.8
$P_{OUT}$ (mW)	97.4	202.4
$P_{DC}$ (mW)	117.4	256.0
$\eta$	83%	79.1%
$L$ (uH), $C$ (pF)	21, 300	2, 300
$R$ ( $\Omega$ ), $X$ ( $\Omega$ )	22, 25.3	22, -1.81
$V_{DD}$ (V)	2	2
$Q_L$	5	5
$f \cdot P_{OUT}$	0.43 MHz·W	3.4 MHz·W

Table 6: Design Details and Measurement Results for Class-E PA for  $q = 0, 0.8, 1.412, 1.65$

and lower drain efficiency  $\eta$  (Table 5) than the theoretically expected 100% as seen in Table 5.

### B. Frequency-Power Product

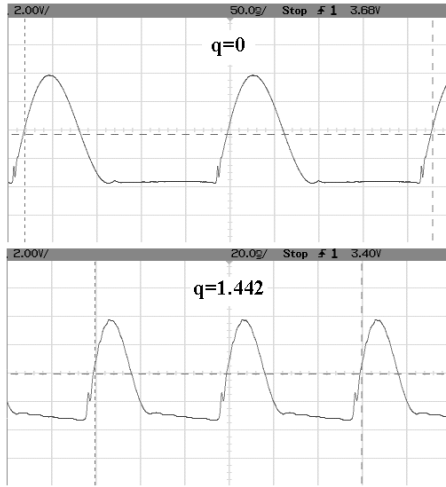


Fig. 4. Drain waveforms of the Class-E PAs for  $q = 0, 1.442$  with the given design specs in Table 6

The presented design set is also very useful to design an optimum Class-E PA under given boundary conditions. Such an example design is demonstrated here. The design parameters  $V_{DD}$ ,  $C$  and  $R$  are bounded and their values are given in Table 6. As it is clear from (2),  $\omega \cdot P_{OUT}$  depends on the value of  $q$  chosen.

Two Class-E PAs were designed for two different values of  $q = 0$  and  $q = 1.442$ . As it is known  $q = 0$  corresponds to RF-Choke Class-E PA and  $q = 1.442$  corresponds to the finite dc-feed inductance Class-E PA whose design set is already introduced in the Table 4. The design specs and the measurement results are given in Table 6.

The discrepancy between the theoretically calculated output power and the measured output power increases for higher frequency of operation. At lower frequency (4.4 MHz) the measured output power 97.4 mW ( $\eta = 83\%$ ) is close to the theoretically expected output power level 104.9 mW ( $\eta = 100\%$ ). At higher frequency (16.8 MHz) the measured output power 202.4 mW ( $\eta = 79.1\%$ ) is less than the theoretically expected output power 246.4 mW ( $\eta = 100\%$ ).

An important reason for the lower output power is the degradation of the driving signal at the gate of the transistor in shape from square wave to sinusoidal at higher frequency. Due to low-pass filtering from the cables and the connections the square waveform signal from the generator approached to a sinusoidal signal at the gate of the transistor; which decreases the output power and the efficiency at high frequency. As it is seen from the given drain waveforms in Fig 4 more deviation from the Class-E waveforms is observed for Class-E $_{q=1.442}$ .

Theoretically, the  $f \cdot P_{OUT}$  of the Class-E $_{q=1.442}$  is expected to be  $\approx 9$  times higher than the  $f \cdot P_{OUT}$  of the Class-E $_{q=0}$ . In the measurements, this  $f \cdot P_{OUT}$  ratio between the Class-E $_{q=1.442}$  and Class-E $_{q=0}$  is observed to be  $\approx 7.9$  that is slightly lower than the theoretical expectation due to the mentioned reduction in the output power of the Class-E $_{q=1.442}$ .

### IV. CONCLUSIONS

An exact mathematical analysis of Class-E PA with finite dc feed inductance was done and; it shows that infinitely many different design equations exist. The actual design equations are complex, and quadratic fits are therefore presented in this work. Using these design equations, the usual need for long iterative solutions is omitted, and it enables easy optimization of the Class-E PA.

As an example for the use of the generalized design equations, it is shown that it enables the optimization of the Class-E PA for maximum frequency-power product at low supply voltages. The overall result being a non-conventional design set and  $\approx 9$  times higher frequency-power product than that of a Class-E PA with RF- choke. The proposed design equations were verified by simulations and measurements.

### ACKNOWLEDGMENT

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### REFERENCES

- [1] G.D.Ewing, "High-Efficiency Radio-Frequency Power Amplifier", PhD thesis, Oregon State University, Corvallis, Oregon, June 1964
- [2] F.Raab, "Idealized operation of the class E tuned power amplifier" *CAS, IEEE Transactions on* Volume 24, Issue 12, Dec 1977, pp. 725-735
- [3] A.Heiskanen, T.Rahkonen, "Comparison of two class E amplifiers for EER transmitter", *IEEE International Symposium on CAS*, 23-26 May 2005, pp. 704-707
- [4] R.Zulinski, J.Steadman, "Class E Power Amplifiers and Frequency Multipliers with finite DC-Feed Inductance", *IEEE Trans. on CAS*, vol. 34, Issue 9, Sep 1987, pp. 1074-1087
- [5] C.-H.Li, Y.-O.Yam, "Maximum frequency and optimum performance of class E power amplifiers", *IEE Proc. Circuits, Devices and Systems*, Vol. 141, Issue 3, June 1994, pp. 174-184
- [6] D.K.Choi, S.I.Long, "Finite DC feed inductor in class E power amplifiers-a simplified approach", *IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, 2-7 June 2002, pp. 1643-1646
- [7] D.Milosevic, J.van der Tang, A.van Roermund, "Explicit design equations for class-E power amplifiers with small DC-feed inductance", *Proceedings of the ECCTD*, Vol. 3, September 2005, pp. 101-104
- [8] A.V.Grebennikov, H.Jaeger, "Class E with parallel circuit - a new challenge for high-efficiency RF and microwave power amplifiers", *IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, 2-7 June 2002, pp. 1627-1630