Analysis of the effect of finite d.c. blocking capacitance and finite d.c. feed inductance on the performance of inverse Class-E amplifiers

T. Mury and V.F. Fusco

Abstract: The first analysis and synthesis equations for the newly introduced inverse Class-E amplifier when operated with a finite d.c. blocking capacitance and a finite d.c.-feed inductance are presented in the paper. Closed-form design equations are derived in order to establish the circuit component values required for optimum synthesis. Excellent agreement between numerical simulation results and theoretical prediction is obtained. It is shown that drain efficiency approaching 100% at a pre-specified output power level can be achieved as zero-current switching and zero-current derivative conditions are simultaneously satisfied. The proposed analysis offers the prospect for realistic MMIC implementation.

1 Introduction

The concept of the Class-E amplifier as introduced by Sokal in 1975 [1] has the potential to be utilised in a broad range of RF and microwave-frequency applications such as portable wireless communications, mobile communications and telemetry/sensors owing to its high RF to d.c. efficiency, which can theoretically approach 100%. The high-efficiency property of this class of switching amplifiers is a consequence of switching voltage and current not occurring simultaneously. Thus power dissipation is minimised and efficiency maximised. Higher efficiency of RF and microwave amplifiers implies longer battery lifetime, at a given output power level. Moreover an increase of drain efficiency for example from 50% to 75% will reduce dissipated heat power by a factor of three for the same output power.

Design equations for an idealised Class-E power amplifier such as that shown in Fig. 1 were derived by Raab and Cripps, [2, 3] respectively; an ideal RF choke (d.c. feed) that has infinite inductance was assumed in their derivations. A more realistic design for a Class-E power amplifier using finite d.c.-feed inductance was proposed in [4–15]. For implementation in MMIC format it is essential that as many realistic effects as possible are taken into account.

The newly-introduced inverse Class-E power amplifier [Note 1] in [16], Fig. 2*a*, employs zero-current switching and zero-current slope switching conditions as introduced in [17]. Note that zero-voltage switching and zero-voltage slope switching conditions are applied in the classic Class-E topology, Fig. 1. The inverse Class-E configuration when compared to the conventional Class-E topology is more attractive for lumped MMIC implementation, [16], since it requires lower inductance values, which in turn implies a smaller area requirement and consequently inductors with lower electrical series resistance (ESR)-a quantity that normally has a major deleterious effect on Class-E amplifier efficiency. In addition the new topology offers lower peak switching voltages, which reduces the possibility of the device failure owing to transistor breakdown mechanisms and therefore further relaxes design requirements. The inverse Class-E topology (represented by the series inductor L in Fig. 2*a*) also affords provision for natural absorption of transistor lead and/or bond wire inductances, which can have a significant effect at high RF and microwave frequencies particularly when high output power level and low d.c. supply voltage are required. Moreover, the parametric study in [16] demonstrated that using a low intrinsic output capacitance (<0.7 pF), $R_{ON} < 2\Omega$ MMIC switching device such as a pHEMT will not significantly degrade the drain efficiency of the inverse Class-E amplifier. Finally, the inverse Class-E topology yields better harmonic suppression than the classic Class-E configuration when operated into a distributed load network, [18].

In all of the above work an ideal RF choke, intended to provide the d.c. path for the supply current and an ideal d.c. block (infinite capacitance) used in order to prevent the d.c. supply voltage from being shorted through the shunt inductance of the LC tank (L_p) in addititon to isolate the d.c. signal from the RF load (see Fig. 2*a*), were assumed. In physical circuits it is necessary to have both a finite d.c.-feed inductance and a finite d.c. blocking capacitance. This paper presents the first theoretical analysis of the inverse Class-E power amplifier with finite d.c. blocking capacitance and finite d.c.-feed inductance.

The discussion in this paper is organised as follow: first we assume that an ideal RF choke is used, then we derive closed-form design equations for optimal circuit component values in the presence of finite d.c. block capacitance. An effective design technique that matches both fundamental and second harmonic impedances of the load network as required for optimum operation is then applied to the circuit in Fig. 2*b* in order to replace the ideal RF choke with

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The authors are with ECIT Institute, Queen's University Belfast, Northern Ireland Science Park, Queen's Road, Queen's Island, Belfast, BT3 9DT, UK

E-mail: v.fusco@ee.qub.ac.uk

Note 1: We name this topology inverse Class-E because the switching current and voltage waveforms are duals to those in the conventional Class-E amplifier topology. The inverse Class-E and the conventional Class-E amplifiers were respectively previously classified as series-L/parallel-tuned and shunt-C/series-tuned in [16, 18] and 'voltage-driven' and 'current-driven' in [20].

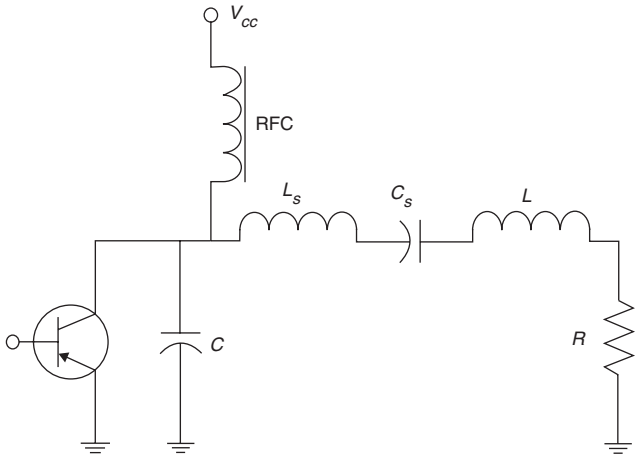

Fig. 1 *Class-E amplifier with ideal RF choke*

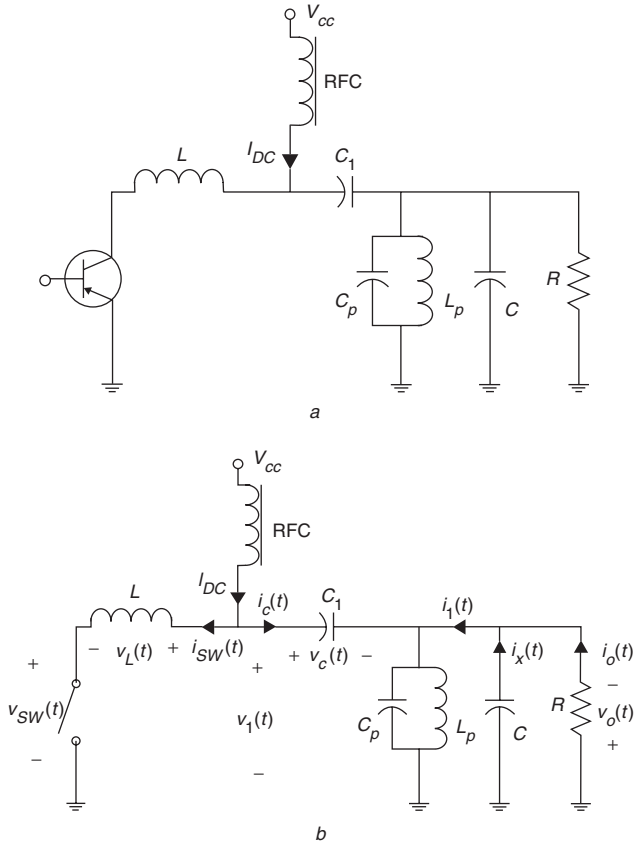

Fig. 2 *Inverse Class-E amplifier with ideal RF choke and finite d.c. blocking capacitance*
a Basic circuit
b Equivalent circuit

a finite d.c. feed inductance. Finally design examples and numerical validations are given.

2 Class-E amplifier with finite d.c.-blocking capacitance

The equivalent circuit of the inverse Class-E amplifier is shown in Fig. 2*b*. The analysis conducted in this Section is based on the following assumptions:

1) Lumped elements contain no parasitics,
2) The transistor has infinite OFF-resistance, zero ON-resistance (R_{ON}), zero output capacitance (C_{OUT}), zero saturation voltage and is modelled as a switch with ideal instantaneous switching action. These requirements have been tested in [16] and the limits on applicability as stated above have been established and shown to be compliant with MMIC pHEMT technology.
3) Initially an ideal RF choke is used to provide the d.c. path for the supply current (I_{DC}).
4) The switch is operated with 50% duty cycle at the carrier frequency.
5) The quality factor of the parallel LC tank (Q_{LC}) is high enough such that the output signal is essentially sinusoidal at the carrier frequency.

2.1 Steady-state analysis of switch voltage and current

As a consequence of high Q_{LC}, the output voltage can be defined as

$$v_o(t) = V_o \sin(\omega t + \varphi) \tag{1}$$

where $\omega = 2\pi f$ is the angular operating frequency, V_o and φ are respectively the amplitude and phase angle of the output signal. V_o and φ are yet to be determined.

The basic equations of currents and voltages in Fig. 2*b* are

$$I_{DC} - i_{SW}(t) = i_C(t) \tag{2}$$

$$v_C(t) = v_1(t) + v_o(t) \tag{3}$$

Equation (3) implies that the difference between the d.c. blocking voltage $v_C(t)$ and output voltage $v_o(t)$ must drop either across the series inductor (L), i.e. when the switch is ON ($v_{SW} = 0$) or across the switch, i.e. when the switch is OFF ($v_L = 0$). The current through and the voltage across the finite d.c. blocking capacitance, C_1, are related by (4)

$$i_C(t) = C_1 \frac{dv_C}{dt} \tag{4}$$

When the switch is closed for $0 \le t \le \pi/\omega$, current $i_{SW}(t)$ flows, the series inductor L is charged and nonzero voltage $v_L(t)$ appears across it. Since the switch voltage is now zero then $v_1(t) = v_L(t)$ and the current $i_{SW}(t)$ is simply expressed by (5)

$$i_{SW}(t) = \frac{1}{L}\int v_1(t)\,dt \tag{5}$$

Substituting (4) and (5) into (2) results in a linear non-homogeneous second-order differential equation

$$LC_1 \frac{d^2 v_c}{dt^2} + v_c(t) - V_o \sin(\omega t + \varphi) = 0 \tag{6}$$

The solution of (6) is given by

$$v_{C\_ON}(t) = A\cos(\omega_o t) + B\sin(\omega_o t) + \frac{V_o}{1-\gamma^2}\sin(\omega t + \varphi) \tag{7}$$

where A and B are constants and ω_o, γ are defined as

$$\omega_o = \frac{1}{\sqrt{LC_1}} \tag{8}$$

$$\gamma = \frac{\omega}{\omega_o} \tag{9}$$

When the switch is opened for $\pi/\omega \le t \le 2\pi/\omega$, $i_{SW}(t)$ is now zero, $v_L(t) = 0$ and therefore voltage $v_1(t)$ drops across the switch, $v_1(t) = v_{SW}(t)$. Substituting $i_{SW}(t) = 0$ and (4)

into (2) gives the following result

$$v_{C\_OFF}(t) = \frac{I_{DC}}{C_1}\left(t - \frac{\pi}{\omega}\right) + K \tag{10}$$

where K is a constant.

The periodic voltage across capacitance C_1 for the whole period is given by (11)

$$v_C(t) = \begin{cases} A\cos(\omega_o t) + B\sin(\omega_o t) + \dfrac{V_o}{1-\gamma^2}\sin(\omega t + \varphi); & 0 \le t \le \dfrac{\pi}{\omega} \\ \dfrac{I_{DC}}{C_1}\left(t - \dfrac{\pi}{\omega}\right) + K; & \dfrac{\pi}{\omega} \le t \le \dfrac{2\pi}{\omega} \end{cases} \tag{11}$$

Next, we need to apply the boundary conditions in (12)–(14), which are based on the electrical continuity property of capacitance C_1 and the initial value of the switch current in order to evaluate the constants A, B and K in (11). By its nature, the waveform $v_C(t)$ must be continuous at the switching transitions, i.e. from ON to OFF and vice versa as described by (12) and (13). At the time instant just before the switch is closed it is assumed that no energy is being stored within the series inductor (L), in other words the current $i_{SW}(t)$ is zero as described by (14).

$$v_{C\_ON}\left(\frac{\pi}{\omega}\right) = v_{C\_OFF}\left(\frac{\pi}{\omega}\right) \tag{12}$$

$$v_{C\_ON}(0) = v_{C\_OFF}\left(\frac{2\pi}{\omega}\right) \tag{13}$$

$$i_{SW}(0) = 0 \tag{14}$$

The solutions for constants A, B and K follow

$$A = \frac{B\sin\left(\dfrac{\pi}{\gamma}\right) - \dfrac{2V_o}{1-\gamma^2}\sin\varphi + \dfrac{I_{DC}\pi}{\omega C_1}}{1 - \cos\left(\dfrac{\pi}{\gamma}\right)} \tag{15}$$

$$B = \frac{I_{DC}}{\omega_o C_1} - \frac{V_o\gamma}{1-\gamma^2}\cos\varphi \tag{16}$$

$$K = A + \frac{V_o}{1-\gamma^2}\sin\varphi - \frac{I_{DC}\pi}{\omega C_1} \tag{17}$$

In order to achieve optimum operation, the inverse Class-E configuration must satisfy zero-current switching (ZCS) and zero-current derivative (ZCD) conditions rather than the zero-voltage switching (ZVS) and zero-voltage derivative (ZVD) conditions that are applied to the Class-E topology. Here the ZCS and ZCD conditions expressed in (18) and (19) respectively are enforced in order to eliminate power losses owing to the ON-to-OFF transition of the transistor thereby yielding optimum efficiencies theoretically approaching 100%.

$$i_{SW}(t)\big|_{t=\frac{\pi}{\omega}} = 0 \tag{18}$$

$$\left.\frac{di_{SW}}{dt}\right|_{t=\frac{\pi}{\omega}} = 0 \tag{19}$$

Solving (18) and (19) results in closed-form expressions of the previously undetermined constants V_o and φ, as follows

$$\varphi = \cot^{-1}\left\{\frac{\pi\omega_o\cos\left(\dfrac{\pi}{\gamma}\right) + \omega\sin\left(\dfrac{\pi}{\gamma}\right)}{\omega\gamma\left[1 - \cos\left(\dfrac{\pi}{\gamma}\right) + \dfrac{\pi}{2\gamma}\sin\left(\dfrac{\pi}{\gamma}\right)\right]} - \frac{2}{\gamma}\cot\left(\frac{\pi}{\gamma}\right) - \frac{\gamma\left[1 - \cos\left(\dfrac{\pi}{\gamma}\right)\right]}{\sin\left(\dfrac{\pi}{\gamma}\right)}\right\} \tag{20}$$

$$V_o = \frac{I_{DC}(1-\gamma^2)\left[1 - \cos\left(\dfrac{\pi}{\gamma}\right) + \dfrac{\pi}{2\gamma}\sin\left(\dfrac{\pi}{\gamma}\right)\right]}{\omega_o C_1 \sin\varphi \sin\left(\dfrac{\pi}{\gamma}\right)} \tag{21}$$

From (20) it is evident that φ is a function of L and C_1 assuming that ω is given, where ω_o and γ are expressed by (8) and (9) respectively. As a validity check we take the limit of φ as C_1 approaches infinity, i.e. an ideal d.c. block, this reduces (20) to (22) which is the same result as (10) in [16].

$$\lim_{C_1 \to \infty} \varphi = \tan^{-1}\left(\frac{-2}{\pi}\right) \tag{22}$$

2.2 Fourier series: d.c. and fundamental-frequency components

The d.c. component in the Fourier series of $v_C(t)$ refers to the input voltage V_{CC}, which is computed as follows

$$V_{CC} = \frac{\omega}{2\pi}\int_0^{\frac{2\pi}{\omega}} v_C(t)dt = \frac{\gamma A}{2\pi}\sin\left(\frac{\pi}{\gamma}\right) + \frac{\gamma B}{2\pi}\left[1 - \cos\left(\frac{\pi}{\gamma}\right)\right] + \frac{V_o}{\pi(1-\gamma^2)}\cos\varphi + \frac{I_{DC}\pi}{4\omega C_1} + \frac{K}{2} \tag{23}$$

From Fig. 2*b*, it is obvious that

$$i_1(t) = v_o(t)Y \tag{24}$$

where $Y = G + jB_C$ is the admittance of the parallel circuit RC. G and B_C are respectively the circuit load conductance and susceptance; $G = 1/R$ and $B_C = \omega C$. Substituting (1) into (24) results in

$$\begin{aligned} i_1(t) &= V_o\sqrt{G^2 + B_C^2}\sin(\omega t + \varphi_1) \\ &= I_1\sin(\omega t + \varphi_1) \end{aligned} \tag{25}$$

with

$$\varphi_1 = \varphi + \Psi \tag{26}$$

and

$$\Psi = \tan^{-1}\left(\frac{B_C}{G}\right) \tag{27}$$

Angle Ψ represents the phase shift between currents $i_o(t)$ and $i_1(t)$ whereas $I_1 = V_o\sqrt{G^2 + B_C^2} = V_o G\sec\Psi$ and φ_1 are the amplitude and phase angle of current $i_1(t)$ respectively. From Fourier series analysis we define I_1 as the in-phase fundamental-frequency component of the switch current $i_{SW}(t)$ and we can compute it using the Fourier integral described by (28). The quadrature fundamental-frequency component of $i_{SW}(t)$ is accordingly zero, (29). The phasor diagram for the fundamental-frequency components of the currents and voltages for optimum

amplifier operation is illustrated in Fig. 3.

$$I_1 = \frac{\omega}{\pi}\int_0^{\frac{2\pi}{\omega}} i_{SW}(t)\sin(\omega t + \varphi_1)dt \tag{28}$$

$$0 = \frac{\omega}{\pi}\int_0^{\frac{2\pi}{\omega}} i_{SW}(t)\cos(\omega t + \varphi_1)dt \tag{29}$$

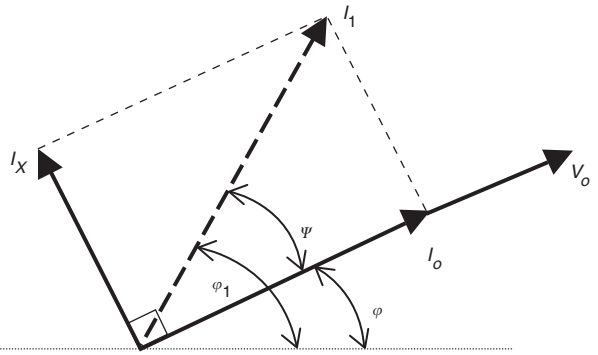

Fig. 3 *Phasor diagram of fundamental-frequency components of the currents and voltages for the optimum operation of the amplifier*

The phase angle φ_1 can be determined from either (28) or (29). Solving (29) is less cumbersome than solving (28) results in a closed-form expression of φ_1, (30).

$$\varphi_1 = \tan^{-1}\left[\frac{\pi N V_o \cos\varphi - 2N(A+M)}{\frac{2I_{DC}}{\pi} + 2\gamma N(P-B) - \pi N V_o \sin\varphi}\right] \tag{30}$$

where

$$N = \frac{\omega C_1}{2\pi(\gamma^2 - 1)} \tag{31}$$

$$P = A\sin\left(\frac{\pi}{\gamma}\right) - B\cos\left(\frac{\pi}{\gamma}\right) \tag{32}$$

$$M = A\cos\left(\frac{\pi}{\gamma}\right) + B\sin\left(\frac{\pi}{\gamma}\right) \tag{33}$$

2.3 Power relationship and circuit element values

In RF amplifier design, the electrical specifications are usually given in terms of output power (P_{OUT}), d.c. input voltage (V_{CC}) and operating frequency (f). Since $\eta = P_{OUT}/P_{DC} = 1$ and P_{DC} is the product of V_{CC} and I_{DC}, then I_{DC} can be calculated as

$$I_{DC} = \frac{P_{OUT}}{V_{CC}} \tag{34}$$

All variables ω_o, γ, A, B, K, φ, V_o and φ_1 respectively as given by (8), (9), (15), (16), (17), (20), (21) and (30) are now a function of L and C_1 only.

Upon enforcing the ideal d.c. block as treated in [16], $v_C(t) = V_{CC}$ and (3) reduces to $v_1(t) = V_{CC} - v_o(t)$. Additional boundary conditions, (35) and (36), must now be imposed in order to ensure that $v_C(t)$ is always positive; t_{min} refers to the time when $v_C(t)$ reaches its minimum value. To evaluate L and C_1, consider now (23), (35) and (36). By solving these three equations numerically, the unknown variables L, C_1 and t_{min} can be computed accordingly.

$$A\cos(\omega_o t_{\min}) + B\sin(\omega_o t_{\min}) + \frac{V_o}{1-\gamma^2}\sin(\omega t_{\min} + \varphi) = 0 \tag{35}$$

$$\frac{dv_{C\_ON}}{dt} = -A\omega_o\sin(\omega_o t_{\min}) + B\omega_o\cos(\omega_o t_{\min}) + \frac{V_o\omega}{1-\gamma^2}\cos(\omega t_{\min} + \varphi) = 0 \tag{36}$$

Once L and C_1 are known, the remaining circuit component values can be determined as follows

$$R = \frac{V_o^2}{2P_{OUT}} \tag{37}$$

$$C = \frac{G}{\omega}\tan(\varphi_1 - \varphi) \tag{38}$$

$$C_p = \frac{Q_{LC}}{\omega R} \tag{39}$$

$$L_p = \frac{1}{\omega^2 C_p} \tag{40}$$

3 Class-E Amplifier with finite d.c.-feed inductance

The analysis in Section 2 whereby the finite d.c. blocking capacitance is accounted for assumes that an ideal RF choke is used in the circuit. However, an effective design technique similar to that presented in [8, 9] permits the inclusion of a finite d.c.-feed inductance in addition to a finite d.c. blocking capacitance is forthcoming upon matching both fundamental and second harmonic load-network impedances, an essential requirement for Class-E operation.

The procedure is that the parallel circuit L_2-C_2 in Fig. 4, where L_2 is the finite d.c.-feed inductance, is made to resonate (i.e. be open circuit) at the second harmonic frequency and therefore (41) must be fulfilled.

$$C_2 = \frac{1}{4\omega^2 L_2} \tag{41}$$

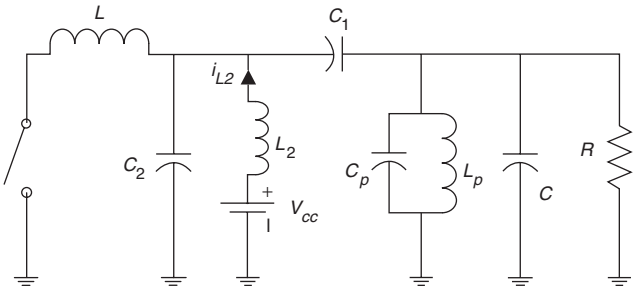

Fig. 4 *Inverse Class-E amplifier with finite d.c.-feed inductance and finite d.c. blocking capacitance*

Figure 5*a* illustrates the equivalent circuit of the fundamental-frequency load network required for optimum operation when a finite d.c. blocking capacitance (C_1) and ideal RF choke are used, as explained in Section 2, Fig. 2*b*. The admittance of such a circuit, Y_1, is expressed by (42) and its value can be evaluated by considering that the component values of R, C and C_1 have been computed based on equations derived in the previous Section, thus

$$Y_1 = \frac{\omega C_1}{1 + \{\omega R(C + C_1)\}^2} \times \left[\omega C_1 R + j\left\{1 + (\omega R)^2 C(C + C_1)\right\}\right] \tag{42}$$

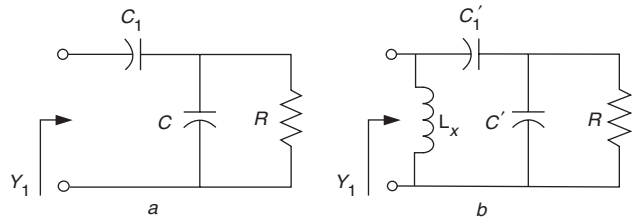

Fig. 5 *Equivalent circuit of fundamental-frequency load network*
a Ideal RFC
b Finite d.c.-feed inductance

Once the ideal RF choke is replaced by a finite d.c.-feed inductance, it can be regarded as a part of the load network. At the fundamental frequency the L_p-C_p tank is open circuited (resonant) while the parallel L_2-C_2 resonator behaves like an inductor, L_X and results in the following equation

$$L_x = \frac{4}{3}L_2 \tag{43}$$

The virtual inductor L_X together with capacitor C'_1 and parallel load circuit R-C' have to meet the required fundamental admittance (i.e. Y_1), see Fig. 5*b*. By assuming that the value of load resistance R remains the same as obtained previously from Section 2 and that L_X or L_2 value is chosen arbitrarily, then new capacitances C' and C'_1 can be evaluated by solving (44) and (45) simultaneously.

$$\frac{(\omega C'_1)^2 R}{1+\{\omega R(C'+C'_1)\}^2} = \mathrm{Re}(Y_1) \tag{44}$$

$$\frac{\omega C'_1}{1+\{\omega R(C'+C'_1)\}^2}\left\{1+(\omega R)^2 C'(C'+C'_1)\right\}-\frac{1}{\omega L_x}=\mathrm{Im}(Y_1) \tag{45}$$

The unwanted higher harmonic signals will be filtered out by the L_p-C_p tank as it provides low impedance to the ground. At the second, third and other higher harmonic frequencies the L_p-C_p parallel resonator behaves like a capacitor as also applies to the L_2-C_2 parallel circuit at third, fourth and other higher harmonics; the equivalent capacitive reactances (in Ω) are given in (46) and (47) respectively for the L_p-C_p and L_2-C_2 parallel tanks.

$$X_{L_pC_p\_n^{th}} = \frac{n}{n^2-1}\omega L_p \quad \text{for } n = 2,3,4,\ldots \tag{46}$$

$$X_{L_2C_2\_m^{th}} = \frac{4m}{m^2-4}\omega L_2 \quad \text{for } m = 3,4,5,\ldots \tag{47}$$

We may now summarise the discussion above as follows: the circuit component values L, C_1, R, C, C_p and L_p are first computed using the derived-equations in Section 2 and then the corresponding admittance Y_1 can be evaluated using (42). Next we may choose any appropriate value for L_2; C_2 and L_X can afterwards be calculated using (41) and (43) respectively. Finally the solution of (44) and (45) results in revised capacitance values for C and C_1, i.e. C' and C'_1.

4 Design examples and numerical validation

Consider now the effect that the synthesis strategy developed above has on the theoretical performance of an inverse Class-E amplifier topology in Figs. 2*b* and 4 with the requirement for use in the ISM unlicensed frequency band [19]. Namely output power $P_{OUT}=0.5\,\mathrm{W}$ ($\sim$27 dBm), input d.c. voltage $V_{CC}=5\,\mathrm{V}$ and operating frequency $f=2.5\,\mathrm{GHz}$. First the supply current $I_{DC}=0.1\,\mathrm{A}$ is computed using (34), the solving (23), (35) and (36) where ω_o, γ, A, B, K, φ, and V_o are respectively described by (8), (9), (15)–(17) and (20), (21) yields the values of L and C_1 as $L=1.34\,\mathrm{nH}$ and $C_1=2.25\,\mathrm{pF}$. The values of $R=46.3\,\Omega$, $C=0.7\,\mathrm{pF}$, $C_p=6.9\,\mathrm{pF}$ and $L_p=0.6\,\mathrm{nH}$ are then evaluated using (37)–(40) subject to a choice of quality factor for the L_p-C_p tank, in this case $Q_{LC}=5$, a value typical of that encountered in a commercial MMIC process.

The circuit depicted in Fig. 2*b* was simulated using the Harmonic Balance analysis programme provided within Agilent's Advanced Design System (HB-ADS). The transistor was modelled with $R_{OFF}=1\,\mathrm{M\Omega}$ and $R_{ON}=0.001\,\mathrm{m\Omega}$, since $R_{ON}=0.\,\Omega$ leads to numerical problems. The simulation results in $P_{OUT}=477\,\mathrm{mW}$, $I_{DC}=96\,\mathrm{mA}$ and $\eta=99.4\%$, which are in good agreement with the given specifications; the output power is 4.6% lower than the specification because the Q_{LC} considered here is small, i.e. 5. Performance could be improved by choosing a higher Q_{LC} value in order to give better harmonic suppression, however higher Q_{LC} requires a higher capacitance value (C_p), which is generally less suitable for MMIC implementation. The simulated values of peak switch current (I_{SW}) and voltage (V_{SW}) are respectively 361 mA and 13.43 V, compared to 356 mA and 14.3 V as given in [16]. Care must be taken in the selection of an appropriate transistor in so far as it must be capable of sustaining both peak switching current and voltage; otherwise transistor breakdown mechanisms will lead to amplifier failure.

The simulated time-domain waveforms of currents and voltages for the circuit are given in Fig. 6 ($R_{OFF}=100\,\mathrm{k\Omega}$, $R_{ON}=0.01\,\Omega$). The $i_{SW}(t)$ waveform in Fig. 6 shows that the ZCS and ZCD conditions are well-satisfied and therefore power losses owing to the ON-to-OFF transition of the switch have been eliminated and efficiency approaching 100% can be obtained. In Fig. 6, the voltage $v_C(t)$ is sinusoidal during the ON state and a linear function during the OFF state as predicted by (11), its values are definite positive (≥ 0) as conditioned by (35).

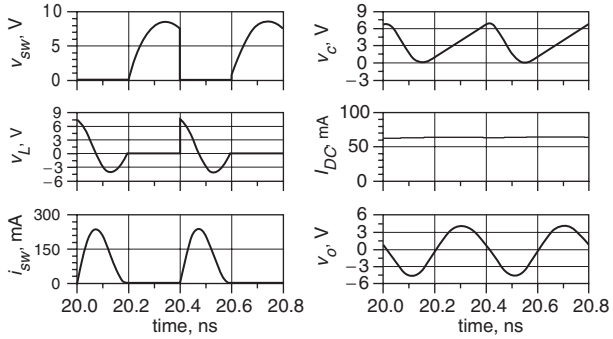

Fig. 6 *Time-domain transient waveforms of 500 mW-5 V-2.5 GHz inverse Class-E amplifier (ideal RFC)*

Now consider the technique explained in Section 3 deployed in order to replace the ideal RF choke with a finite d.c.-feed inductance, see Fig. 4. First we arbitrarily (within probable MMIC process limits) choose $L_2=3.75\,\mathrm{nH}$; the values of C_2, C' and C'_1 are then be evaluated using (41)–(45), this gives $C_2=0.27\,\mathrm{pF}$, $C'=2.17\,\mathrm{pF}$ and $C'_1=5.16\,\mathrm{pF}$, if we choose a lower inductance value say $L_2=2.1\,\mathrm{nH}$, we obtain $C_2=0.48\,\mathrm{pF}$, $C'=3.15\,\mathrm{pF}$ and $C'_1=7.29\,\mathrm{pF}$. As can be seen by reducing the value of L_2, capacitance C_2, C' and C'_1 increase. In practice the trade off between inductance and capacitance values has to be carefully considered from the perspective of size/area usage, yield and impact of components parasitic effects on MMIC

amplifier implementation. The HB-ADS simulations give the following results: $P_{OUT}=506\,\text{mW}$, $I_{DC}=101\,\text{mA}$, $\eta=99.7\%$, $V_{SW}=14.98\,\text{V}$ and $I_{SW}=356.6\,\text{mA}$ for $L_2=3.75\,\text{nH}$; $P_{OUT}=512\,\text{mW}$, $I_{DC}=102.6\,\text{mA}$, $\eta=99.8\%$, $V_{SW}=15.35\,\text{V}$ and $I_{SW}=356\,\text{mA}$ for $L_2=2.1\,\text{nH}$. The corresponding time-domain waveforms are depicted in Fig. 7 (for $L_2=3.75\,\text{nH}$) and Fig. 8 (for $L_2=2.1\,\text{nH}$), note now both d.c. and fundamental currents (i_{L2}) flow through the finite d.c.-feed inductance L_2. Observe that the output power is 1% and 2.4% higher than the specified value (500 mW) for the cases of $L_2=3.75\,\text{nH}$ and $L_2=2.1\,\text{nH}$ respectively and that drain efficiency is better than previous simulation results where an ideal RF choke was assumed. This is because the load network at higher harmonics (2nd, 3rd, etc.) provides a lower impedance to ground as the values of C' and C_1' are now bigger than C and C_1 ($C=0.7\,\text{pF}\rightarrow C'=2.17\,\text{pF}$ and $C_1=2.25\,\text{pF}\rightarrow C_1'=5.16\,\text{pF}$ for example in the case of $L_2=3.75\,\text{nH}$) and thus the unwanted harmonic signals are more thoroughly suppressed.

An inverse Class-E amplifier was successfully implemented using an OMMIC ED02AH $6\,\mu\text{m}\times 50\,\mu\text{m}$ pHEMT device in [20]. Its output power was measured to be $P_{OUT}=63\,\text{mW}$ for a supply voltage $V_{CC}=2\,\text{V}$ at an operating frequency of $f=870\,\text{MHz}$ (low-band GSM-Tx frequency). However, in [20] the synthesis equations required to compute the circuit component values for this topology were not presented. Based on the analysis and techniques presented in this paper, we now evaluate the optimal circuit element values for the same amplifier specifications mentioned above, see Table 1. In [20] Q_{LC} was small (<1) whereas in our case $Q_{LC}=5$ is used. Moreover from Table 1 it can be seen that using the analysis developed in this paper that the large inductance value of L_p and a large capacitance value of C_1 (approximating an ideal d.c. block) that were used in [20] can be substantially reduced. The value of d.c.-feed inductance is chosen to be the same as in [20], i.e. 37 nH, nevertheless values lower than 37 nH could have been adopted. The numerical simulation results of this exercise are given in Table 1, and waveforms of current and voltage are plotted in Fig. 9 (assuming an ideal RF choke) and in Fig. 10 (using a finite d.c.-feed inductance).

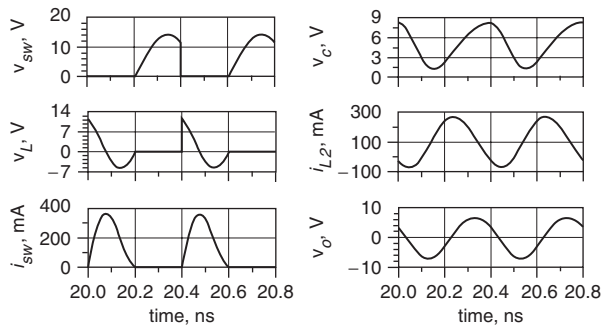

Fig. 7 *Time-domain transient waveforms of 500 mW-5 V-2.5 GHz inverse Class-E amplifier (finite d.c.-feed inductance: $L_2=3.75\,\text{nH}$)*

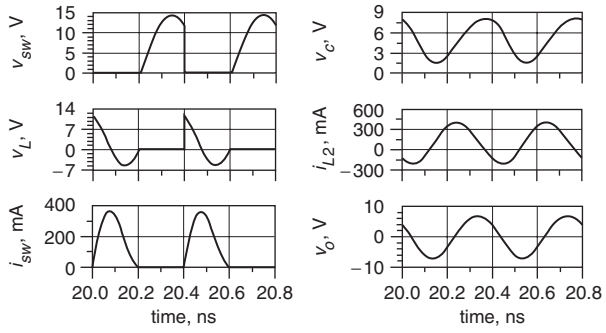

Fig. 8 *Time-domain transient waveforms of 500 mW-5 V-2.5 GHz inverse Class-E amplifier (finite d.c.-feed inductance: $L_2=2.1\,\text{nH}$)*

Table 1: Optimal circuit component values and simulation results of 63 mW-2 V-870 MHz inverse Class-E amplifier

Component and result	This paper		[20]
	Ideal RF choke	Finite d.c.-feed	
R (Ω)	58.7	58.7	50
L (nH)	4.9	4.9	6.5
C (pF)	1.57	2.97	N/A
C_p (pF)	15.6	15.6	1
L_p (nH)	2.15	2.15	37
C_1 (pF)	5.1	7.7	47
L_2 (nH)	N/A	37	37
C_2 (pF)	N/A	0.23	N/A
P_{OUT} (mW)	60.1	62.3	63
η (%)	99.4	99.6	96

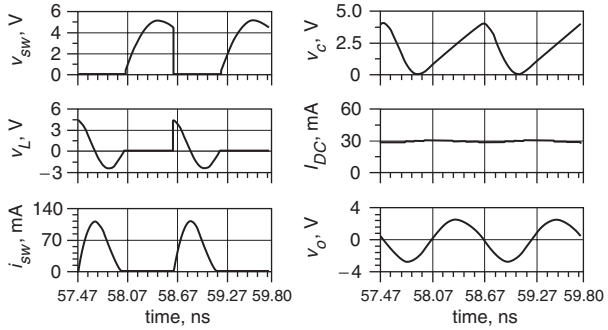

Fig. 9 *Time-domain transient waveforms of 63 mW-2 V-870 MHz inverse Class-E amplifier (ideal RFC)*

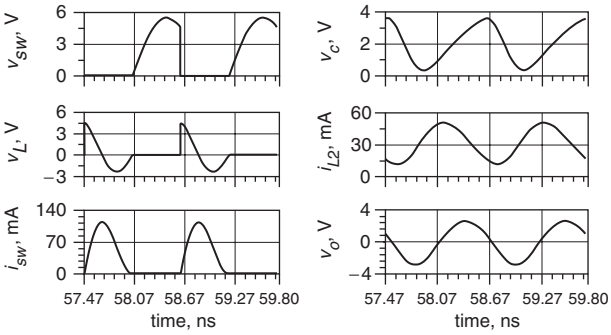

Fig. 10 *Time-domain transient waveforms of 63 mW-2 V-870 MHz inverse Class-E amplifier (finite d.c.-feed inductance: $L_2=37\,\text{nH}$)*

5 Conclusions

In this paper, we present the first analysis and synthesis equations for the newly introduced inverse Class-E amplifier operated with finite d.c. blocking capacitance and finite d.c.-feed inductance. It is demonstrated that by using the design techniques proposed in this paper, drain efficiency

approaching 100% and a specified output power level can be achieved even in the presence of a low quality factor tank (Q_{LC}). It has been shown that deploying a low value finite d.c.-feed inductance will increase the peak switch voltage but will provide lower impedance to ground at the second and other higher harmonics thus offering improved harmonic suppression at the load. We envisage that this type of amplifier could be more readily implemented in MMIC form than other previously reported topologies and that this could open the way for even higher frequency applications of Class-E amplifiers as microwave and millimetre-wave transistor switch technology improves. Thus a broad variety of applications such as in portable wireless communications and telemetry/sensors where small size and high RF-to-d.c. efficiency are of importance could be more readily constructed.

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