Lab 11 – Exploring the Operation of a 2-Read,1-Write Memory for use in a Basic Processor

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Summary/Abstract

This lab was an instantiation of many past labs such as the seven seg decoder displays to display the bits, the finite state machine, the ALU to calculate the binary numbers into hexadecimal, and the synchronous logic to have them all running at once. The binary numbers are selected with specific switches assigned and once you select switch 7, the write enable selects on and the address point selected will then store the value chosen after pressing the button. After placing my TUID into memory and then selected each address bit the lab was easily understood as a 1-write, 2-read memory. These bits were displayed simultaneously whenever the address was selected. After creating the Verilog, we simulated to receive a matching loop index of 48 which is how many test vectors are in the test bench.

Introduction

In this lab we instantiated an 8-word deep by 4-bit wide memory. This memory was 2-read,1-write. It has three separate address busses to access the same internal memory cells so one for writing and two for reading. This means that one can read two different words or memory locations simultaneously. We also controlled the read and write operations as well as displaying the memory contents by selecting various combinations of switches and push buttons.

Procedure

The procedure to this lab consisted of instantiating the memory, instantiating the display driver, creating the AND gate and a multiplexer. Using the specifications, we instantiated, we selected switches that would be represented as hexadecimals in the display. We also selected bits that would be written and read along with a button to write to that memory location.

Results

Design Code

```
// lab11 : version 11/13/2018
//
module memory_display (output logic [6:0] cathode, output logic [3:0] anode,
    output logic m_sec, output logic [3:0] rp_data, output logic [3:0] rq_data,
    input logic rst, input logic clk, input logic m_write,
    input logic w_ena, input logic [3:0] w_data, input logic [7:0] sw);

logic w_wr;
logic [3:0] digit0, digit1, digit2, digit3;

rf_8x4_2r1w u_rf(.rq_data(rq_data), .rp_data(rp_data), .w_data(w_data), .w_addr(sw[2:0]),
.rq_addr(sw[6:4]), .rp_addr(sw[2:0]), .w_wr(w_wr), .clk(clk));

display_driver u_dd(.digit0({1'b0, sw[2:0]}), .digit1(digit1), .digit2({1'b0,sw[6:4]}), .digit3(rq_data),
.cathode(cathode), .anode(anode), .anode_sel(), .m_sec(m_sec), .display_on(1'b1), .clk(clk), .rst(rst));

assign w_wr = w_ena & m_write;
always_comb begin

case(sw[7])

1'b1:begin
digit1 = w_data;
end

1'b0:begin
digit1 = rp_data;
end
endcase
end
endmodule
```

Simulation Results

```
Match--loop index i:          24
Match--loop index i:          25
Match--loop index i:          26
Match--loop index i:          27
Match--loop index i:          28
Match--loop index i:          29
Match--loop index i:          30
Match--loop index i:          31
Match--loop index i:          32
Match--loop index i:          33
Match--loop index i:          34
Match--loop index i:          35
Match--loop index i:          36
Match--loop index i:          37
Match--loop index i:          38
Match--loop index i:          39
Match--loop index i:          40
Match--loop index i:          41
Match--loop index i:          42
Match--loop index i:          43
Match--loop index i:          44
Match--loop index i:          45
Match--loop index i:          46
Match--loop index i:          47
Simulation complete - no mismatches!!!
$finish called at time : 48000005 ns : File "/home/tuh42003/2613_2018f/lab11/tb_memory_display.sv" Line 143
run: Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:05 . Memory (MB): peak = 1359.281 ; gain = 0.000 ; free physical = 9969 ; free virt
ual = 13688
## set systemTime [clock seconds]
## puts "----Simulation date/time: [clock format $systemTime -format %D] [clock format $systemTime -format %H:%M:%S]"
----Simulation date/time: 11/13/2018 13:27:27
## exit
```

Hardware Implementation

My design was demonstrated to Catherine on the afternoon of 11/12 during the lab period.

Conclusion

This lab was the most interesting of all the labs. Memory is an important concept to understand the future course of processors. This explains much about past labs and why they were created as they were necessary for memory.

Appendix

This section is optional. Any extra code or information can be put here, depending on the lab requirements. In the main part of the report, you would refer to: *additional information or details in the appendix*.