CS311: Computer Architecture Laboratory
Assignment 6 - L1 Cache Simulation

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The configurations of the caches are as follows:

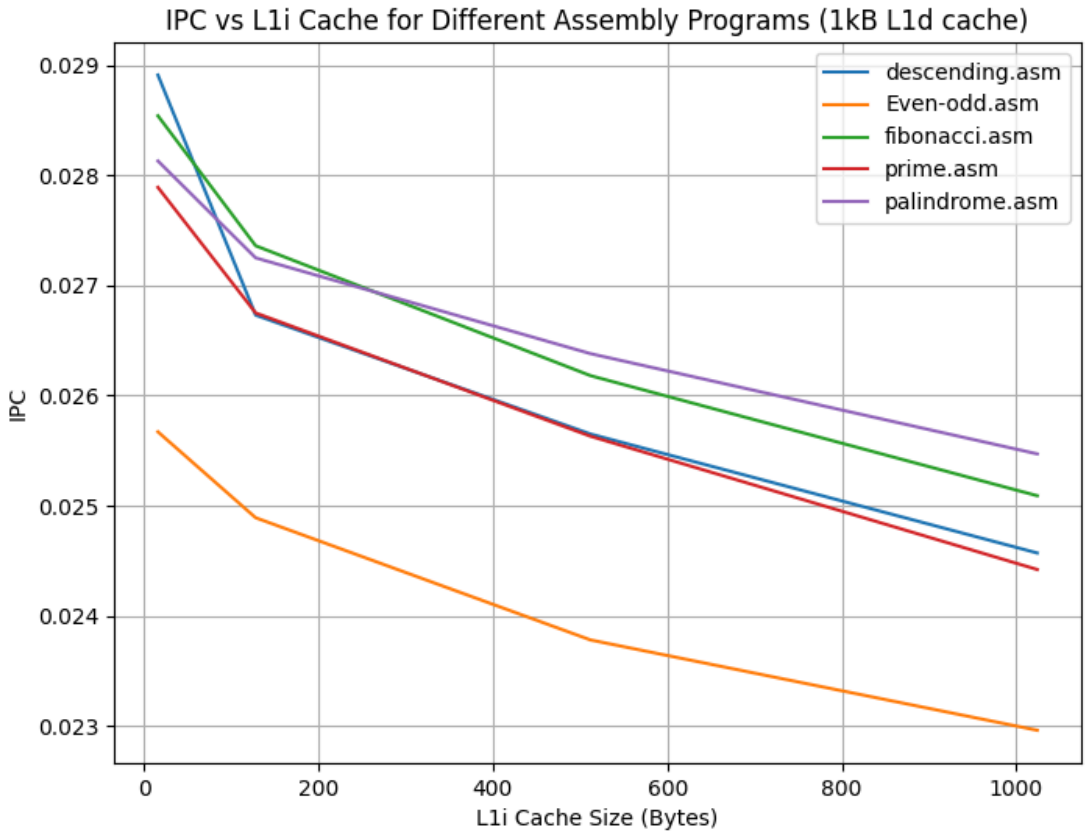
Cache size	16B	128B	512B	1kB
Latency	1 cycle	2 cycles	3 cycles	4 cycles

- Line Size - 4B
- Associativity - Fully Associative
- Write Policy - Write Through

Analysis and Tabulation:

1. Varying Instruction Cache
   First we fix the size of the L1d-cache at 1kB and vary the size of the L1i-cache from 16B to 1kB.

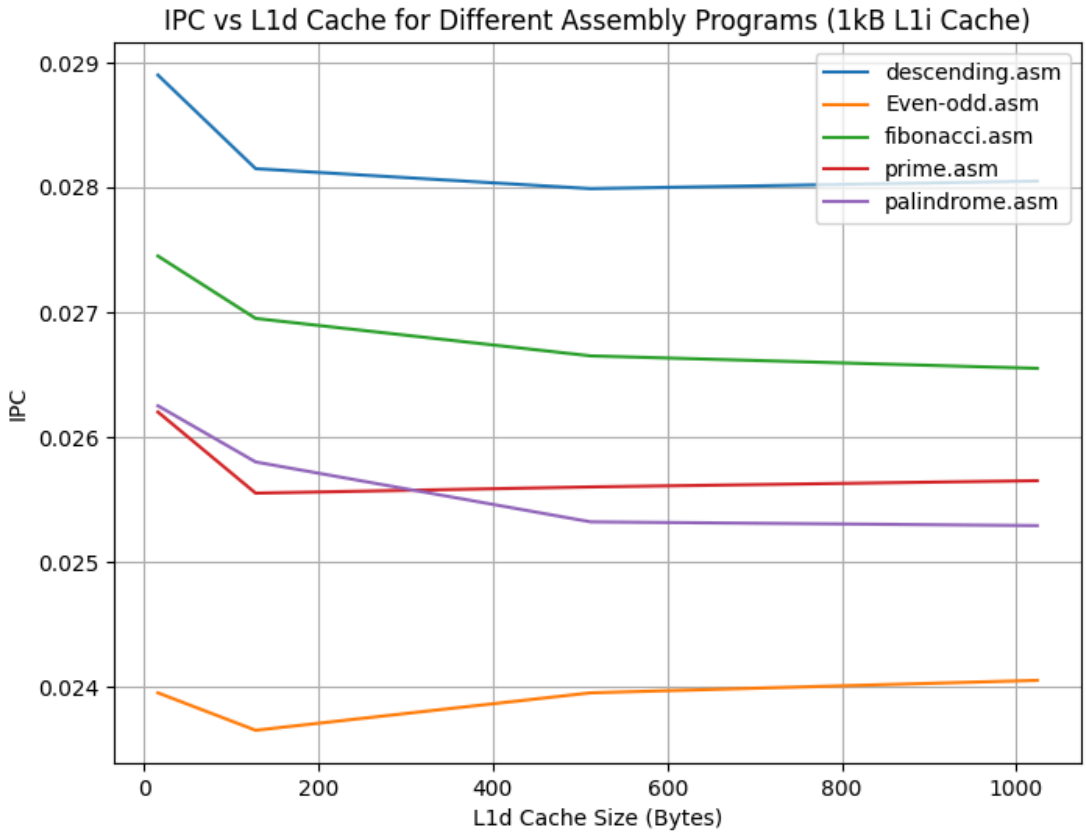
Assembly Program	IPC without Cache	IPC L1i = 16B	IPC L1i = 128B	IPC L1i = 512B	IPC L1i = 1024B (1kB)
descending.asm	0.02497	0.02891	0.02673	0.02565	,0.02457
Even-odd.asm	0.02435	0.02567	0.02489	0.02378,	0.02296
fibonacci.asm	0.02478	0.02854,	0.02736	0.02618	0.02509
prime.asm	0.02456	0.02789	0.02675	0.02563	0.02442
palindrome.asm	0.02462	0.02813	0.02725	0.02638	0.02547



2. Varying Data Cache

   Now we fix the size of the L1i-cache at 1 kB and vary the size of the L1d-cache from 16B to 1kB

Assembly Program	IPC without Cache	IPC L1d = 16B	IPC L1d = 128B	IPC L1d = 512B	IPC L1d = 1024B (1kB)
descending.asm	0.02497	0.02890	0.02815	0.02799	0.02805
Even-odd.asm	0.02435	0.02395	0.02365	0.02395,	0.02405
fibonacci.asm	0.02478	0.02745	0.02695	0.02665	0.02655
prime.asm	0.02456	0.02620	0.02555	0.02560	0.02565
palindrome.asm	0.02462	0.02625	0.02580	0.02532	0.02529


IPC vs L1d Cache for Different Assembly Programs (1kB L1i Cache)
descending.asm
Even-odd.asm
fibonacci.asm
prime.asm
palindrome.asm
IPC
0.029
0.028
0.027
0.026
0.025
0.024
0
200
400
600
800
1000
L1d Cache Size (Bytes)