



1. Description

1.1. Project

Project Name	capstone_1
Board Name	NUCLEO-F334R8
Generated with:	STM32CubeMX 6.9.1
Date	10/03/2023

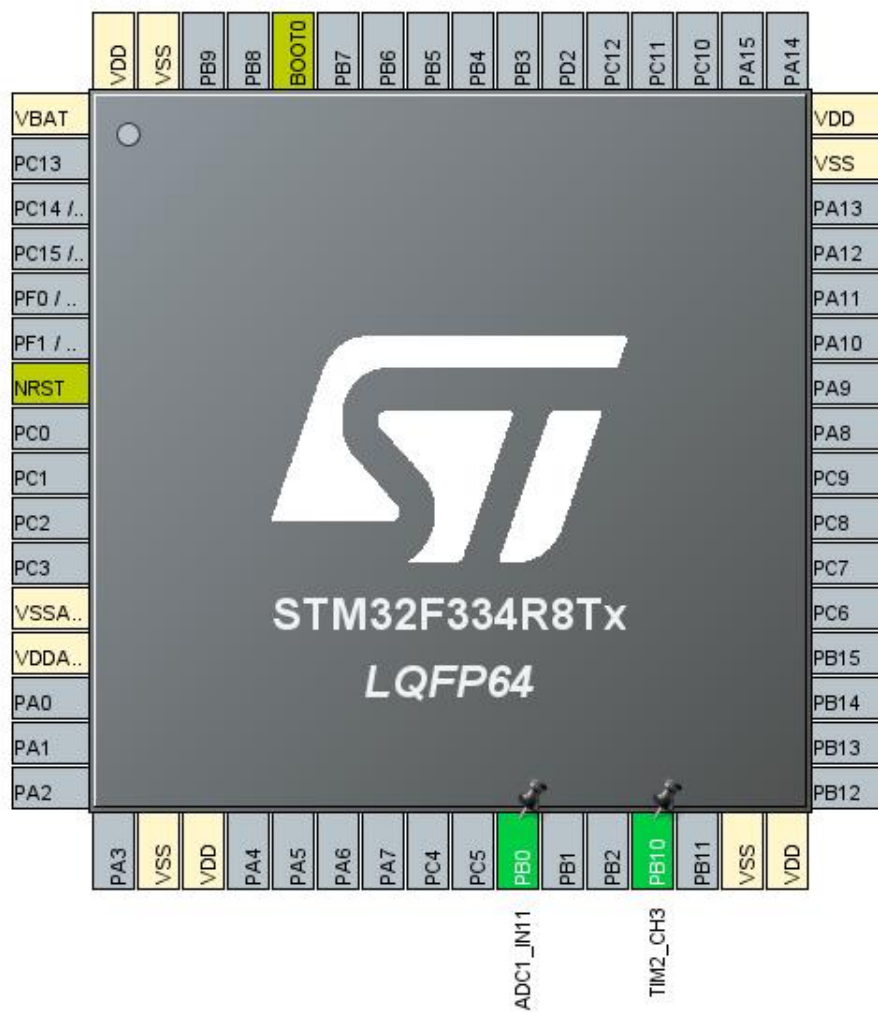
1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F334
MCU name	STM32F334R8Tx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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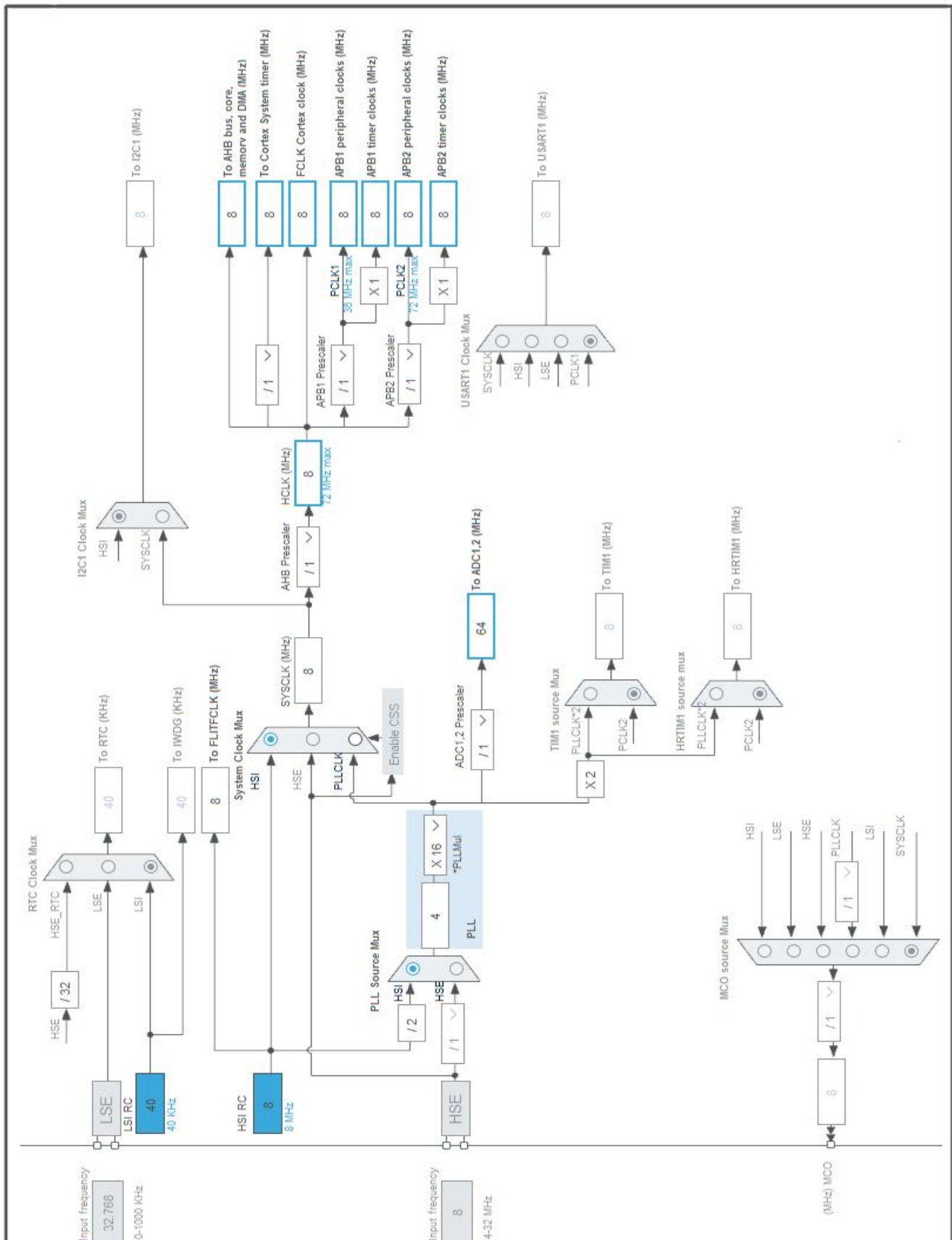
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
18	VSS	Power		
19	VDD	Power		
26	PB0	I/O	ADC1_IN11	
29	PB10	I/O	TIM2_CH3	
31	VSS	Power		
32	VDD	Power		
47	VSS	Power		
48	VDD	Power		
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	capstone_1
Project Folder	C:\Users\luig25453\STM32CubeIDE\Device_drivers\capstone_1
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.4
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_TIM2_Init	TIM2

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F3
Line	STM32F334
MCU	STM32F334R8Tx
Datasheet	DS9994_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	3.6

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

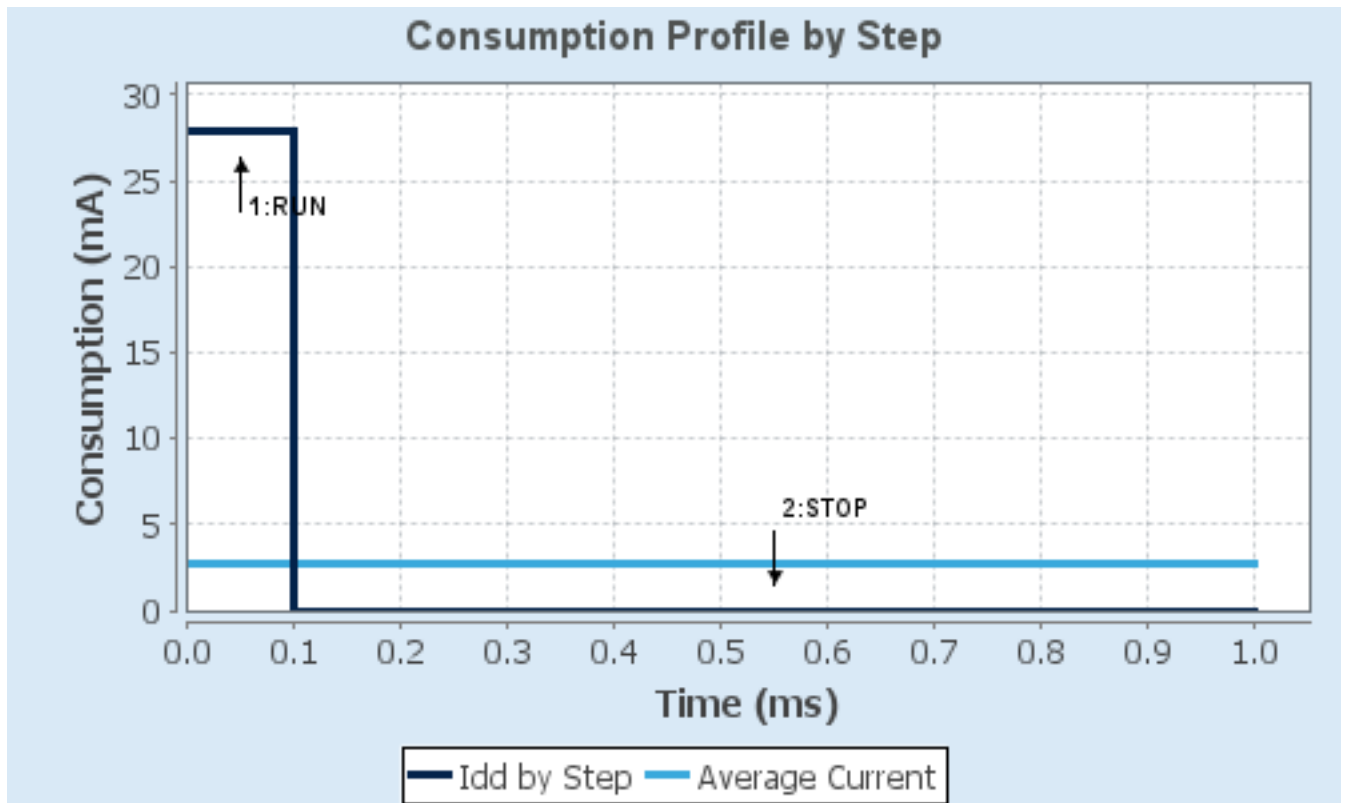
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	RAM	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSEBYP PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27.84 mA	9.55 μ A
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.49	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.79 mA
Battery Life	1 month, 20 days, 5 hours	Average DMIPS	90.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. ADC1

IN11: IN11 Single-ended

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler ADC Asynchronous clock mode

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data overwritten

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

SequencerNbRanks 1

Rank 1

Channel Channel 11

Sampling Time 1.5 Cycles

Offset Number No offset

Offset 0

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

2.2. RCC

2.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

2.3. TIM2

Clock Source : Internal Clock

Channel3: PWM Generation CH3

2.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	8 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable
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PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PB0	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	

3.2. DMA configuration

nothing configured in DMA service

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM2 global interrupt	unused		
Floating point unit interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

Middleware

System Core

Analog

Timers

Connectivity

Computing

DMA

ADC1 

TIM2 

GPIO 

I2C 

RCC 

5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f3_bsdl.zip
System View Description	https://www.st.com/resource/en/svd/stm32f3-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
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Flyers	https://www.st.com/resource/en/flyer/fldpstpf11120.pdf
Product Certifications	https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
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