



INTEL® XEON® SCALABLE PROCESSOR: THE FOUNDATION OF DATA CENTRE INNOVATION

Intel Software Developer Conference – London, 2017

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Agenda

- Intel® Xeon® Scalable Processor Overview, Platform Features
- Skylake-SP CPU Architecture
- Performance Summary

Content Acknowledgement

- Akhilesh Kumar, Skylake-SP CPU Architect
- Malay Trivedi, Lewisburg PCH Architect

Intel® Xeon® Processor Roadmap



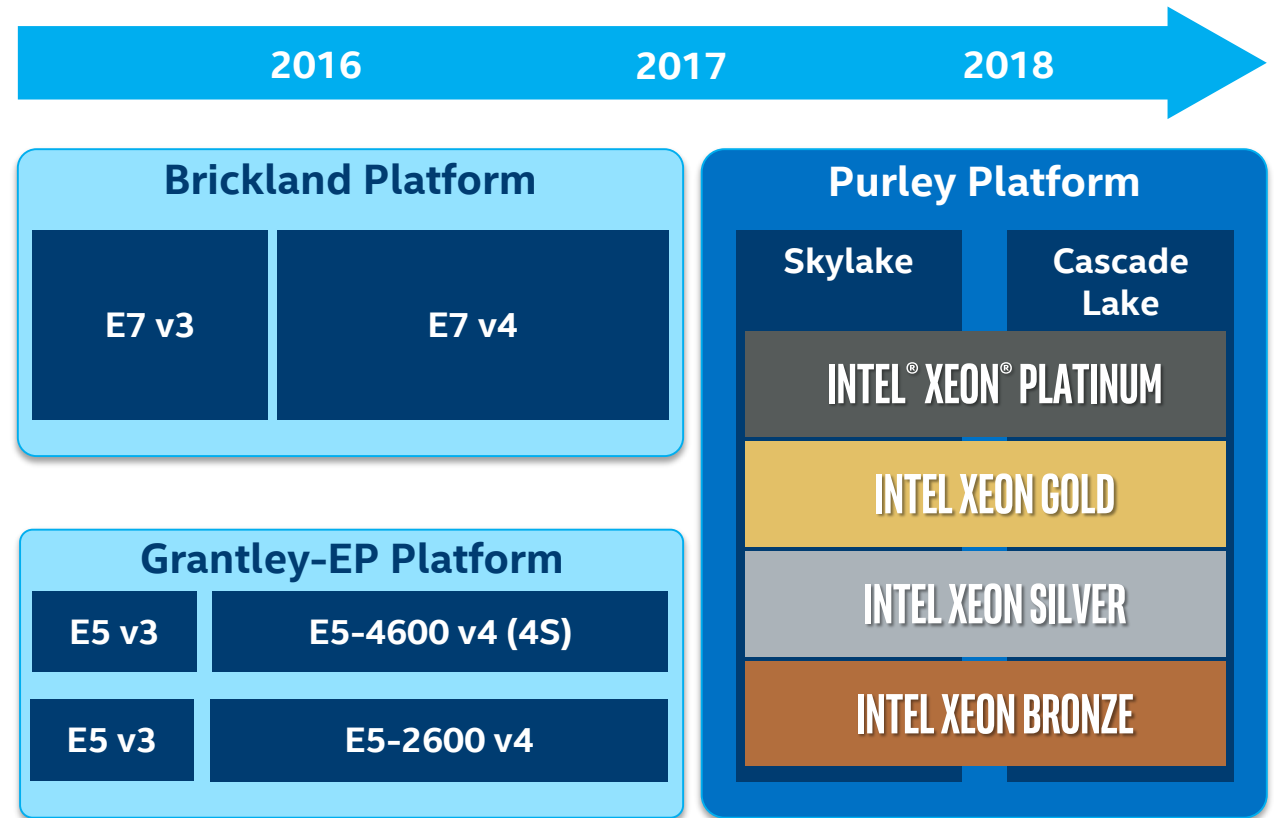
Intel® Xeon® Processor E7

Targeted at **mission critical** applications that value a **scale-up** system with leadership **memory capacity** and **advanced RAS**



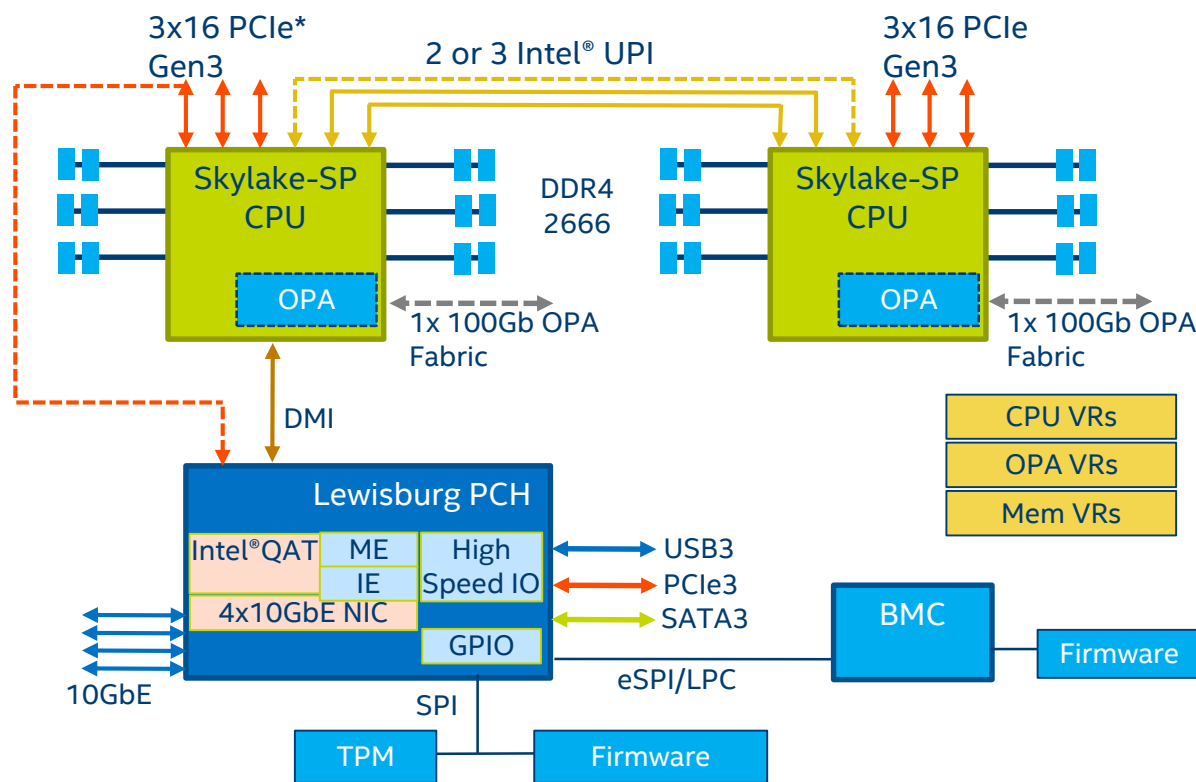
Intel® Xeon® Processor E5

Targeted at a wide variety of applications that value a **balanced system** with leadership performance/watt/\$



CONVERGED PLATFORM WITH INNOVATIVE SKYLAKE-SP MICROARCHITECTURE

Intel® Xeon® Scalable Processor Feature Overview

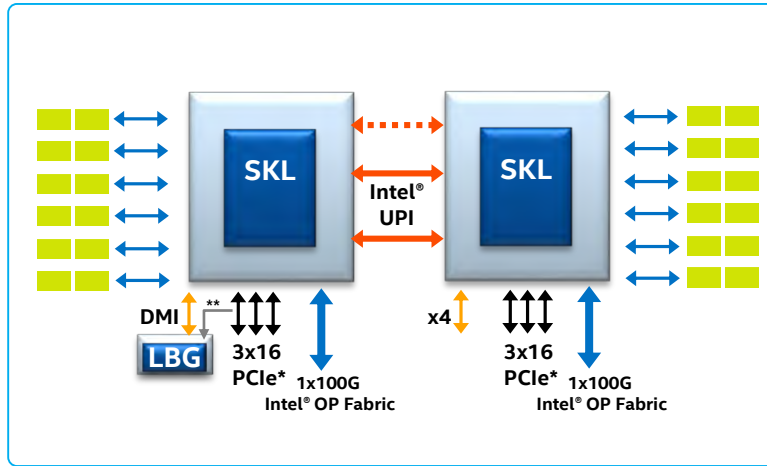


BMC: Baseboard Management Controller	PCH: Intel® Platform Controller Hub	IE: Innovation Engine
Intel® OPA: Intel® Omni-Path Architecture	Intel QAT: Intel® QuickAssist Technology	ME: Manageability Engine
NIC: Network Interface Controller	VMD: Volume Management Device	NTB: Non-Transparent Bridge

Feature	Details
Socket	Socket P
Scalability	2S, 4S, 8S, and >8S (with node controller support)
CPU TDP	70W – 205W
Chipset	Intel® C620 Series (code name Lewisburg)
Networking	Intel® Omni-Path Fabric (integrated or discrete) 4x10GbE (integrated w/ chipset) 100G/40G/25G discrete options
Compression and Crypto Acceleration	Intel® QuickAssist Technology to support 100Gb/s comp/decomp/crypto 100K RSA2K public key
Storage	Integrated QuickData Technology, VMD, and NTB Intel® Optane™ SSD, Intel® 3D-NAND NVMe & SATA SSD
Security	CPU enhancements (MBE, PPK, MPX) Manageability Engine Intel® Platform Trust Technology Intel® Key Protection Technology
Manageability	Innovation Engine (IE) Intel® Node Manager Intel® Datacenter Manager

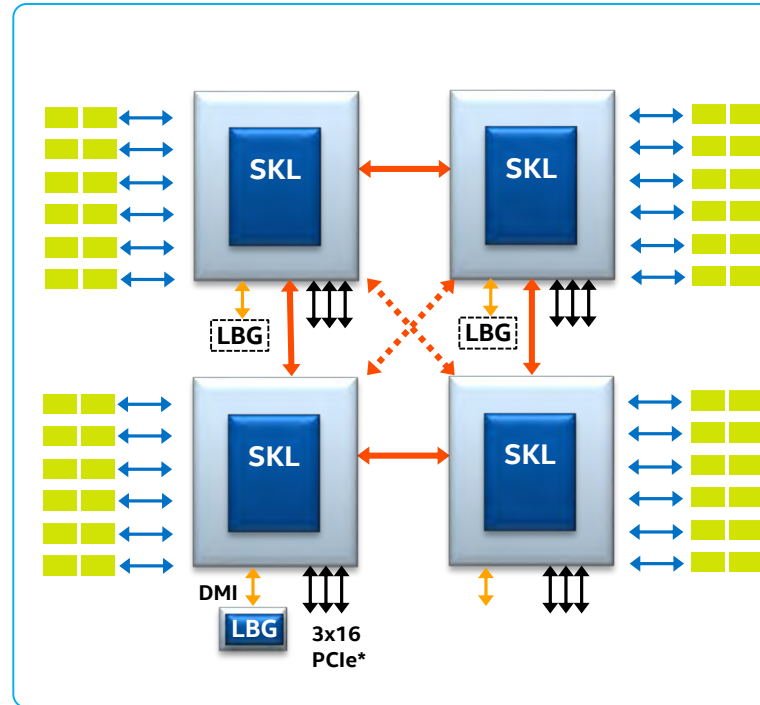
Platform Topologies

2S Configurations



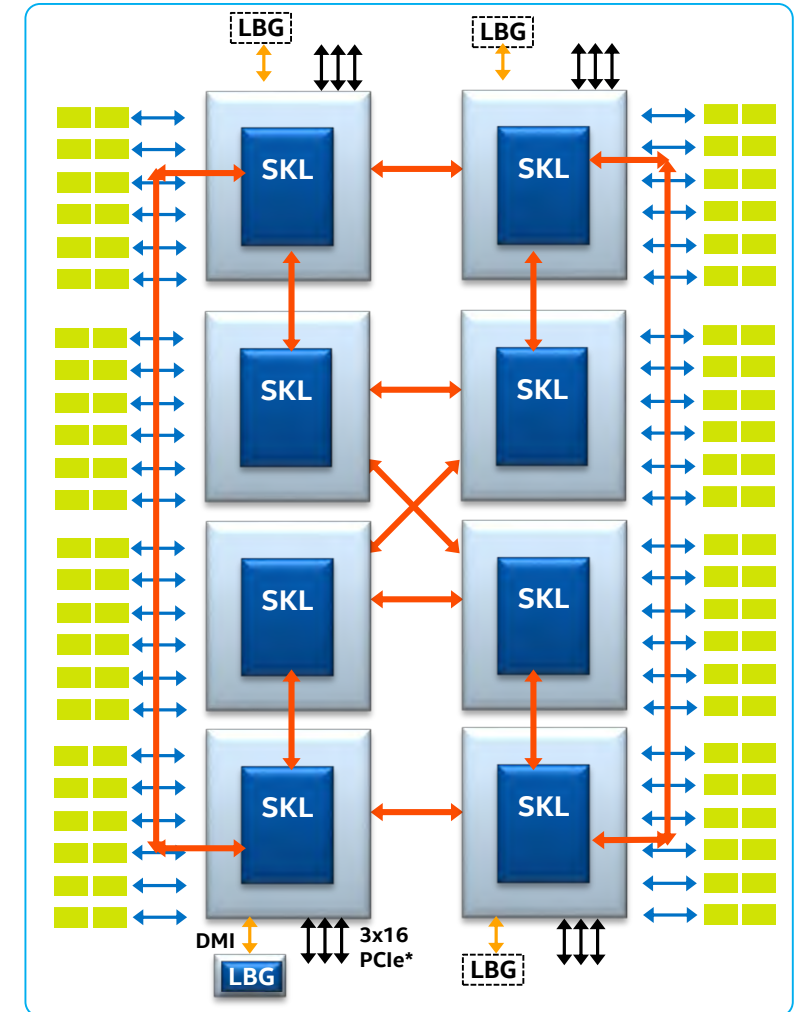
(2S-2UPI & 2S-3UPI shown)

4S Configurations



(4S-2UPI & 4S-3UPI shown)

8S Configuration



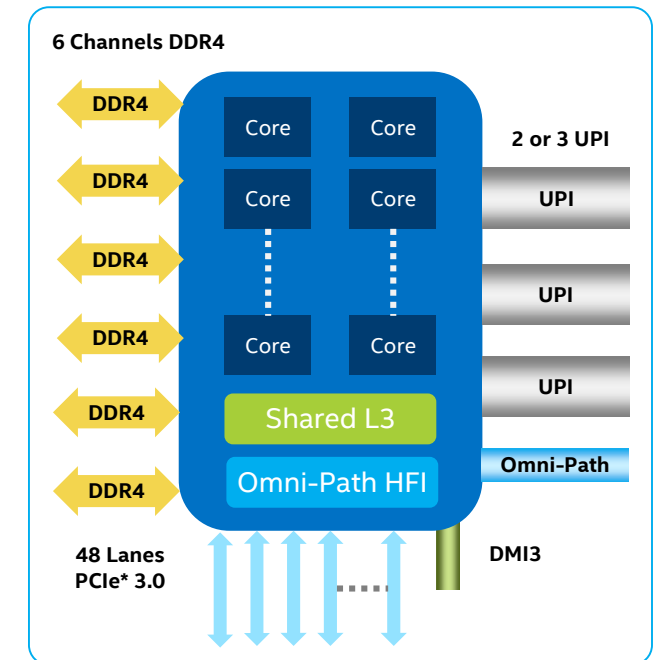
INTEL® XEON® SCALABLE PROCESSOR SUPPORTS CONFIGURATIONS RANGING FROM 2S-2UPI TO 8S

Intel® Xeon® Scalable Processor

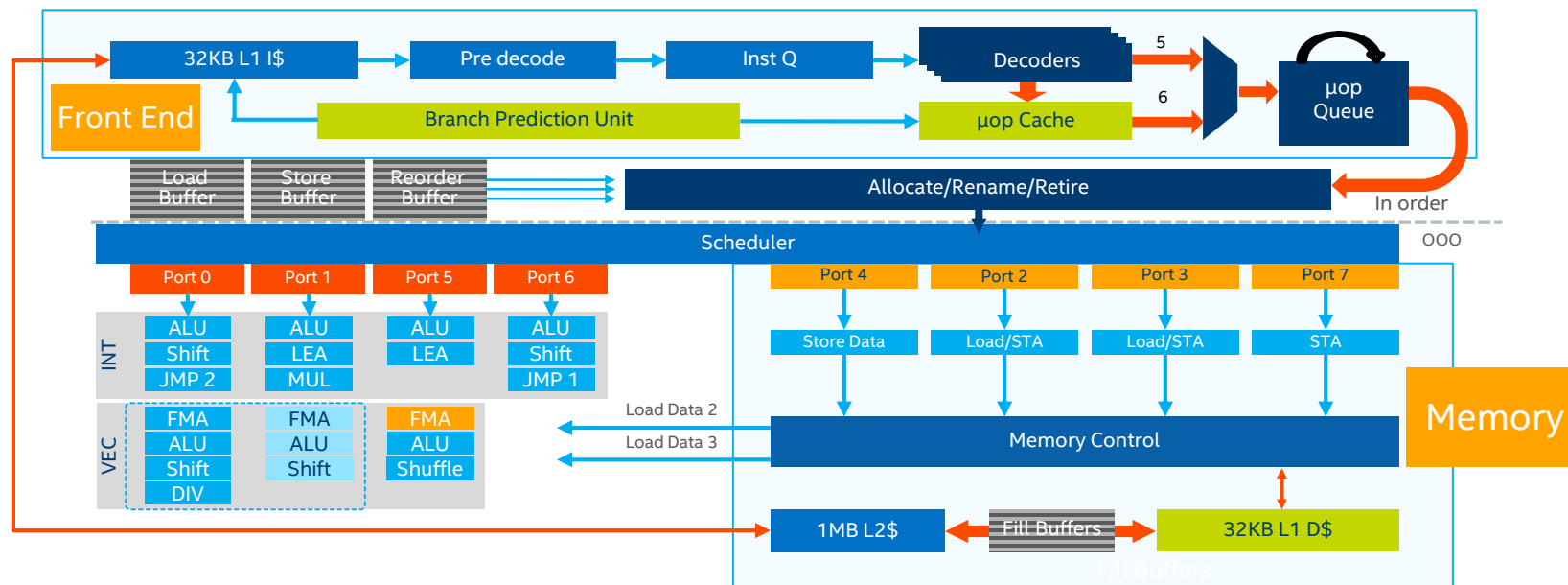
Re-architected from the Ground Up

- Skylake core microarchitecture, with data center specific enhancements
- Intel® AVX-512 with 32 DP flops per core
- Data center optimized cache hierarchy – 1MB L2 per core, non-inclusive L3
- New mesh interconnect architecture
- Enhanced memory subsystem
- Modular IO with integrated devices
- New Intel® Ultra Path Interconnect (Intel® UPI)
- Intel® Speed Shift Technology
- Security & Virtualization enhancements (MBE, PPK, MPX)
- Optional Integrated Intel® Omni-Path Fabric (Intel® OPA)

Features	Intel® Xeon® Processor E5-2600 v4	Intel® Xeon® Scalable Processor
Cores Per Socket	Up to 22	Up to 28
Threads Per Socket	Up to 44 threads	Up to 56 threads
Last-level Cache (LLC)	Up to 55 MB	Up to 38.5 MB (non-inclusive)
QPI/UPI Speed (GT/s)	2x QPI channels @ 9.6 GT/s	Up to 3x UPI @ 10.4 GT/s
PCIe* Lanes/ Controllers/Speed(GT/s)	40 / 10 / PCIe* 3.0 (2.5, 5, 8 GT/s)	48 / 12 / PCIe 3.0 (2.5, 5, 8 GT/s)
Memory Population	4 channels of up to 3 RDIMMs, LRDIMMs, or 3DS LRDIMMs	6 channels of up to 2 RDIMMs, LRDIMMs, or 3DS LRDIMMs
Max Memory Speed	Up to 2400	Up to 2666
TDP (W)	55W-145W	70W-205W



Core Microarchitecture Enhancements



	Broadwell uArch	Skylake uArch
Out-of-order Window	192	224
In-flight Loads + Stores	72 + 42	72 + 56
Scheduler Entries	60	97
Registers – Integer + FP	168 + 168	180 + 168
Allocation Queue	56	64/thread
L1D BW (B/Cyc) – Load + Store	64 + 32	128 + 64
L2 Unified TLB	4K+2M: 1024	4K+2M: 1536 1G: 16

- Larger and improved branch predictor, higher throughput decoder, larger window to extract ILP
- Improved scheduler and execution engine, improved throughput and latency of divide/sqrt
- More load/store bandwidth, deeper load/store buffers, improved prefetcher
- **Data center specific enhancements: Intel® AVX-512 with 2 FMAs per core, larger 1MB MLC**

ABOUT 10% PERFORMANCE IMPROVEMENT PER CORE ON INTEGER APPLICATIONS AT SAME FREQUENCY

Intel® Advanced Vector Extensions 512 (Intel® AVX-512)

- 512-bit wide vectors
- 32 operand registers
- 8 64b mask registers
- Embedded broadcast
- Embedded rounding

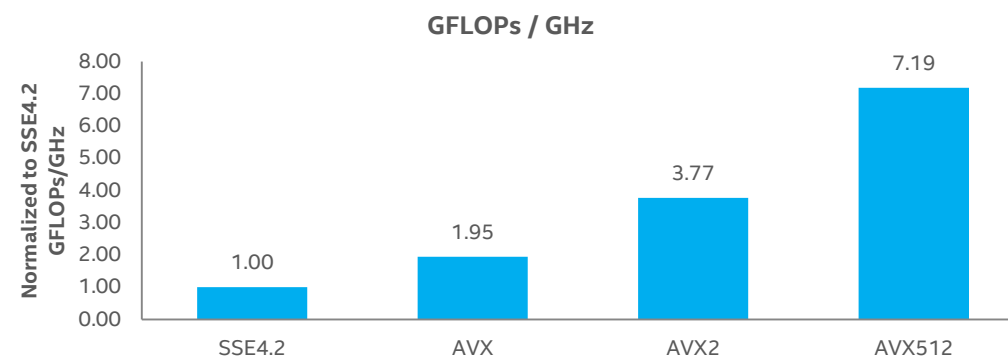
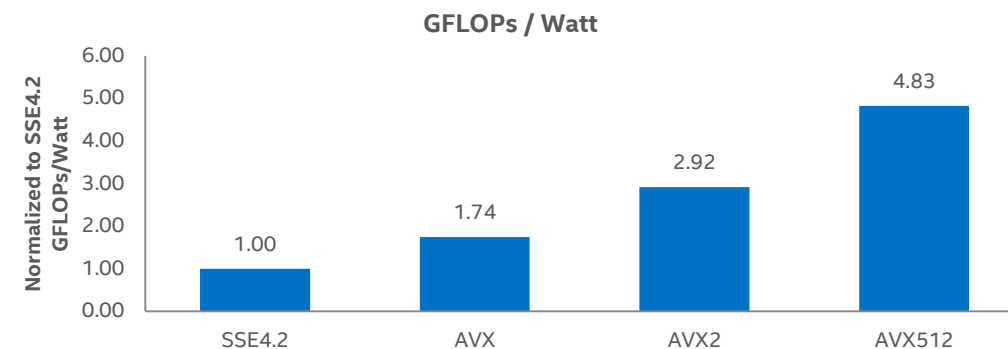
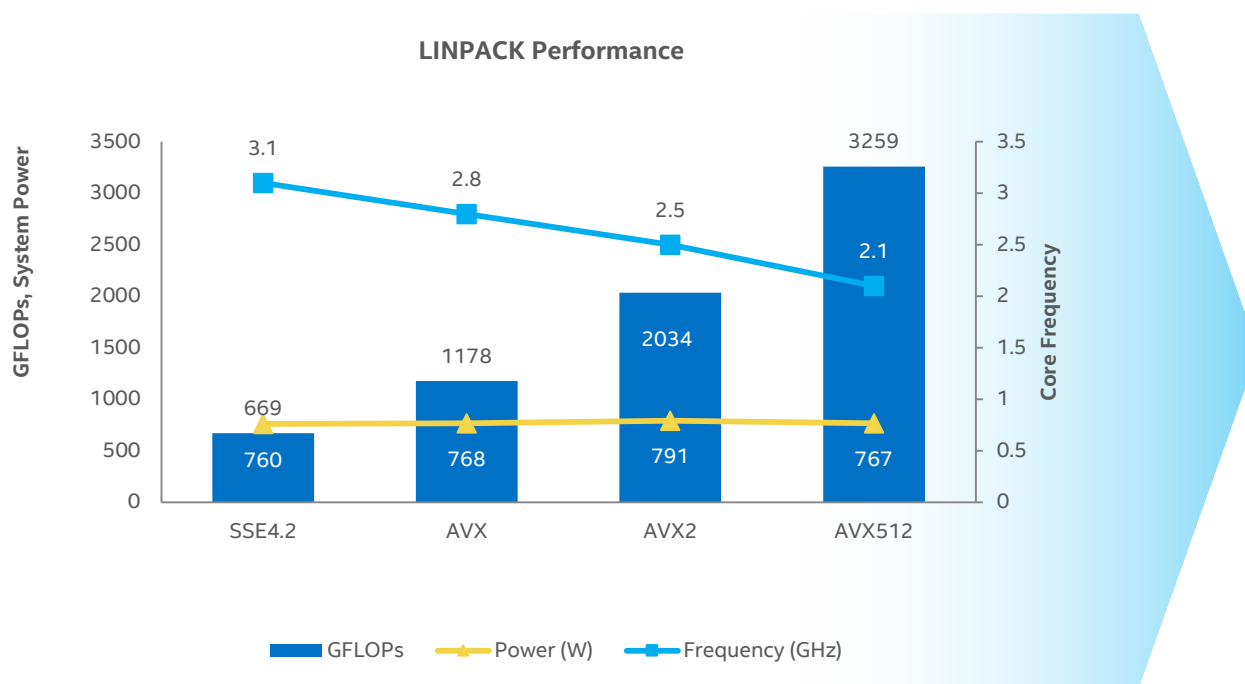
Microarchitecture	Instruction Set	SP FLOPs / cycle	DP FLOPs / cycle
Skylake	Intel® AVX-512 & FMA	64	32
Haswell / Broadwell	Intel AVX2 & FMA	32	16
Sandybridge	Intel AVX (256b)	16	8
Nehalem	SSE (128b)	8	4

Intel AVX-512 Instruction Types

AVX-512-F	AVX-512 Foundation Instructions
AVX-512-VL	Vector Length Orthogonality : ability to operate on sub-512 vector sizes
AVX-512-BW	512-bit Byte/Word support
AVX-512-DQ	Additional D/Q/SP/DP instructions (converts, transcendental support, etc.)
AVX-512-CD	Conflict Detect : used in vectorizing loops with potential address conflicts

POWERFUL INSTRUCTION SET FOR DATA-PARALLEL COMPUTATION

Performance and Efficiency with Intel® AVX-512

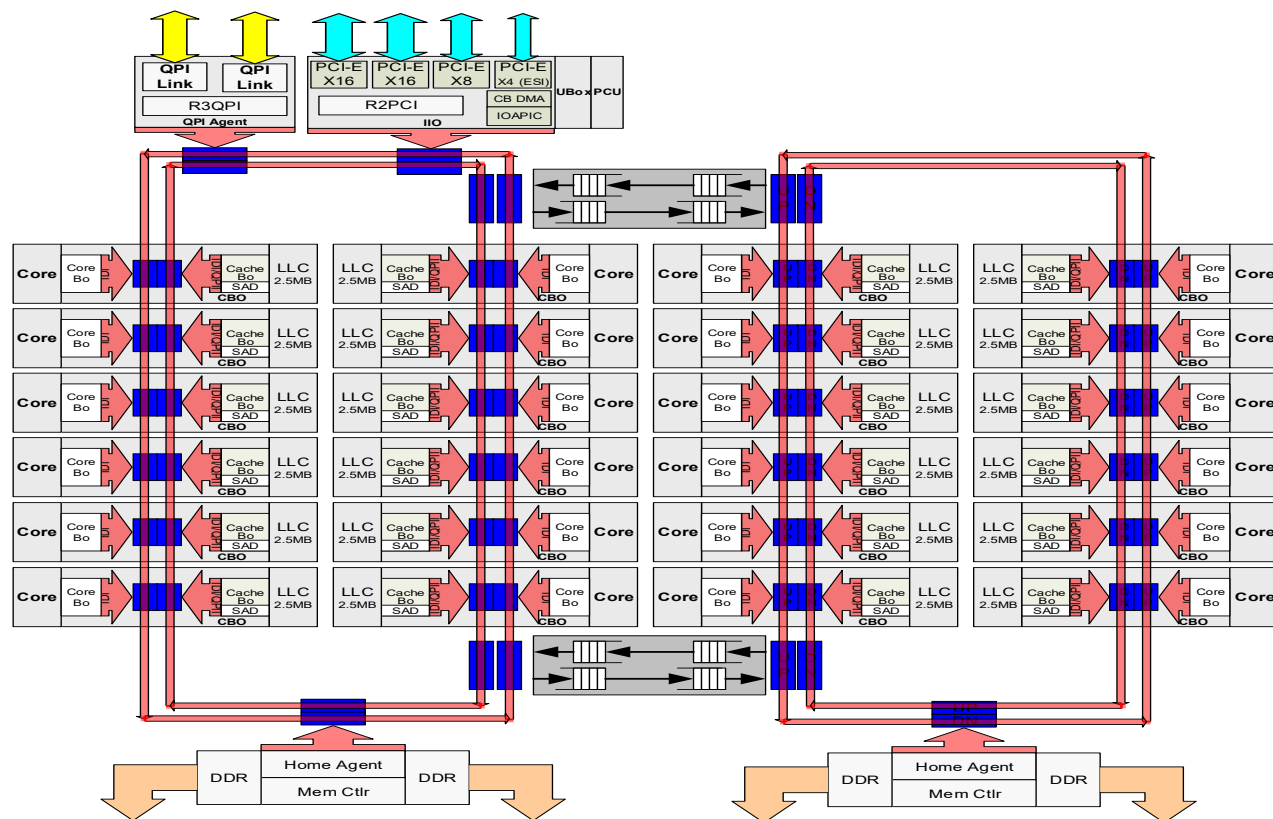


INTEL® AVX-512 DELIVERS SIGNIFICANT PERFORMANCE AND EFFICIENCY GAINS

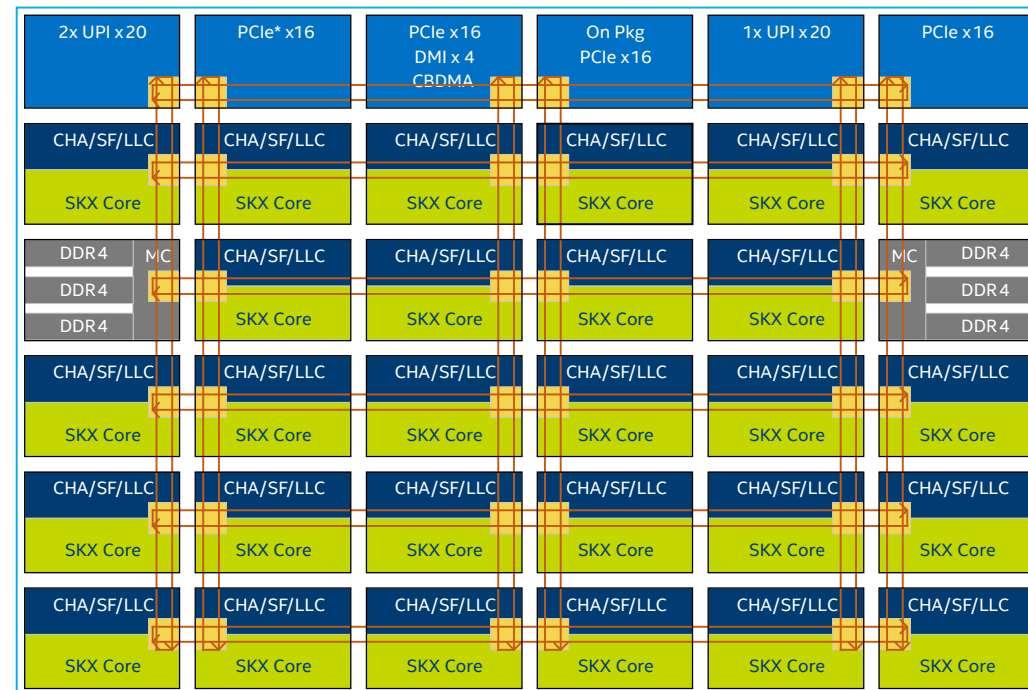
Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, UPI=10.4, SNC1, 6x32GB DDR4-2666 per CPU, 1 DPC. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

New Mesh Interconnect Architecture

Broadwell EX 24-core die



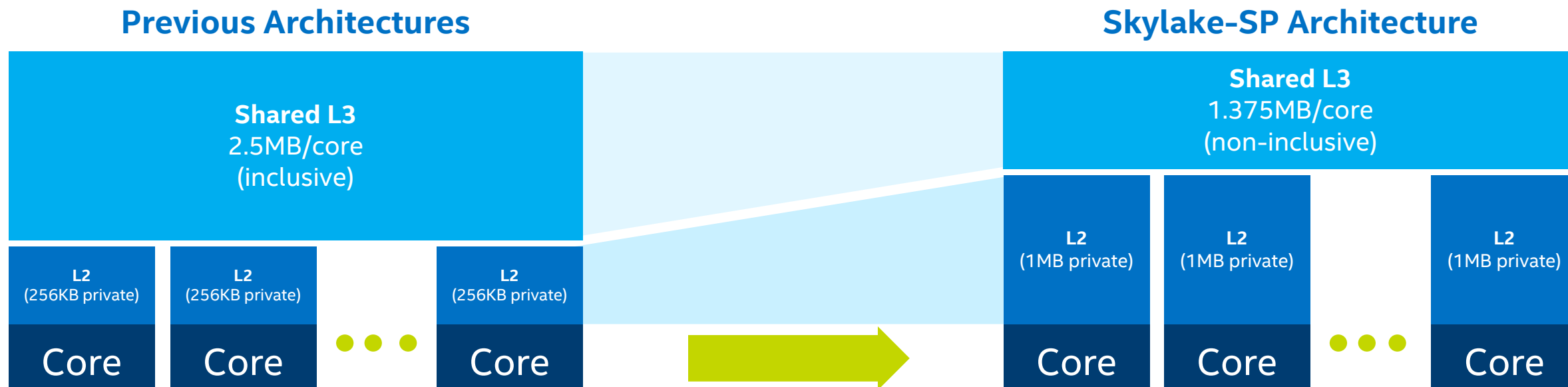
Skylake-SP 28-core die



CHA – Caching and Home Agent ; SF – Snoop Filter; LLC – Last Level Cache;
SKX Core – Skylake Server Core; UPI – Intel® UltraPath Interconnect

MESH IMPROVES SCALABILITY WITH HIGHER BANDWIDTH AND REDUCED LATENCIES

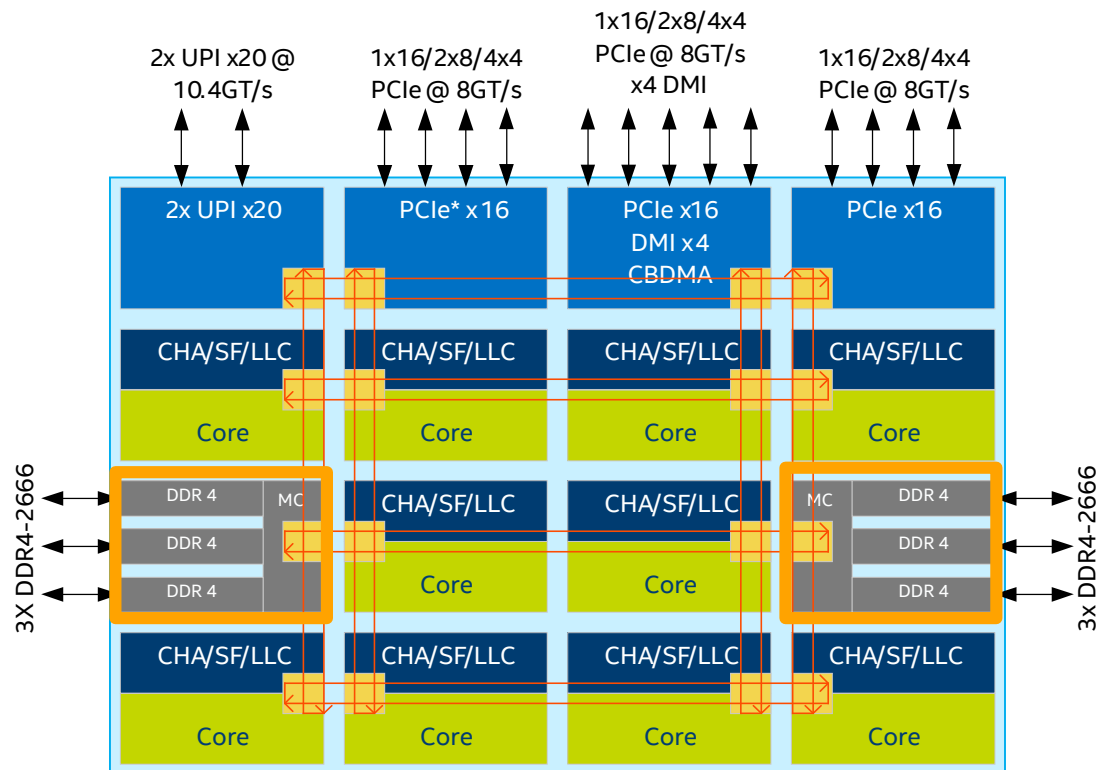
Re-Architected L2 & L3 Cache Hierarchy



- On-chip cache balance shifted from shared-distributed (prior architectures) to private-local (Skylake architecture):
 - Shared-distributed → shared-distributed L3 is primary cache
 - Private-local → private L2 becomes primary cache with shared L3 used as overflow cache
- Shared L3 changed from inclusive to non-inclusive:
 - Inclusive (prior architectures) → L3 has copies of all lines in L2
 - Non-inclusive (Skylake architecture) → lines in L2 **may not** exist in L3

SKYLAKE-SP CACHE HIERARCHY ARCHITECTED SPECIFICALLY FOR DATA CENTER USE CASE

Memory Subsystem



2 Memory Controllers, 3 channels each → total of 6 memory channels

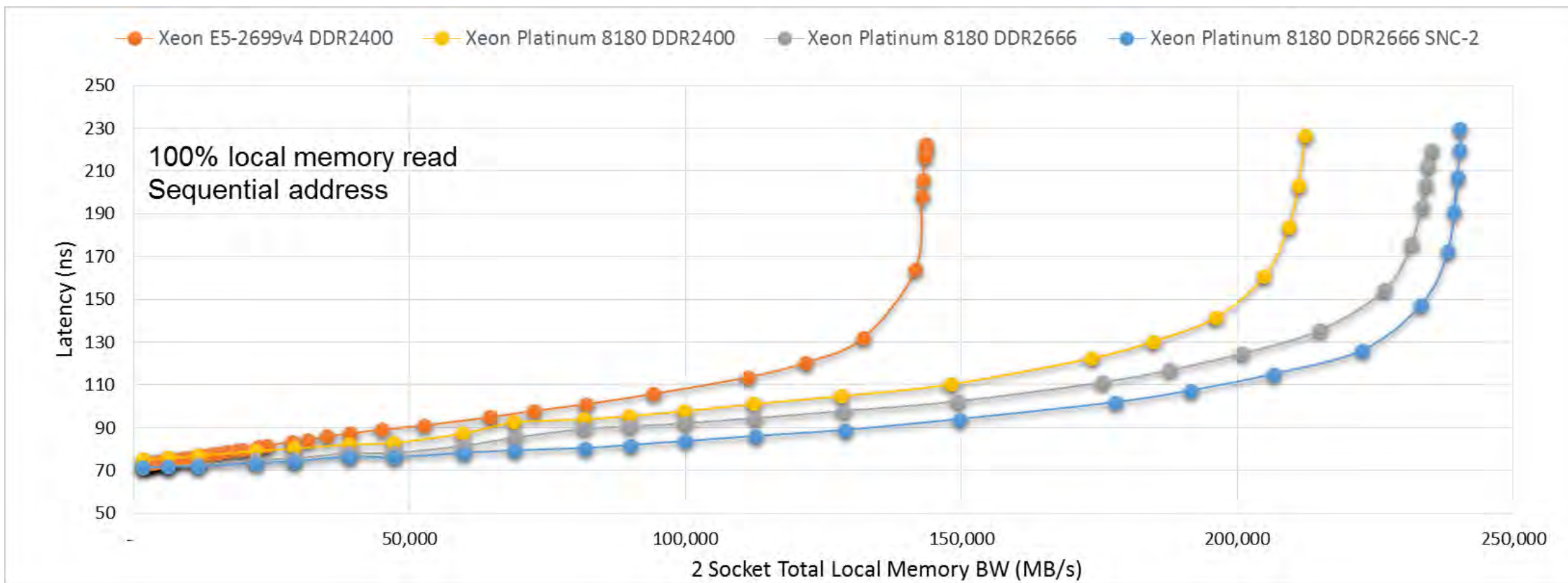
- DDR4 up to 2666, 2 DIMMs per channel
- Support for RDIMM, LRDIMM, and 3DS-LRDIMM
- 1.5TB Max Memory Capacity per Socket (2 DPC with 128GB DIMMs)
- >60% increase in Memory BW per Socket compared to Intel® Xeon® processor E5 v4

Supports XPT prefetch to reduce LLC miss latency
Introduces a new memory device failure detection and recovery scheme with Adaptive Double Device Data Correction (ADDDC)

SIGNIFICANT MEMORY BANDWIDTH AND CAPACITY IMPROVEMENTS

Memory Performance

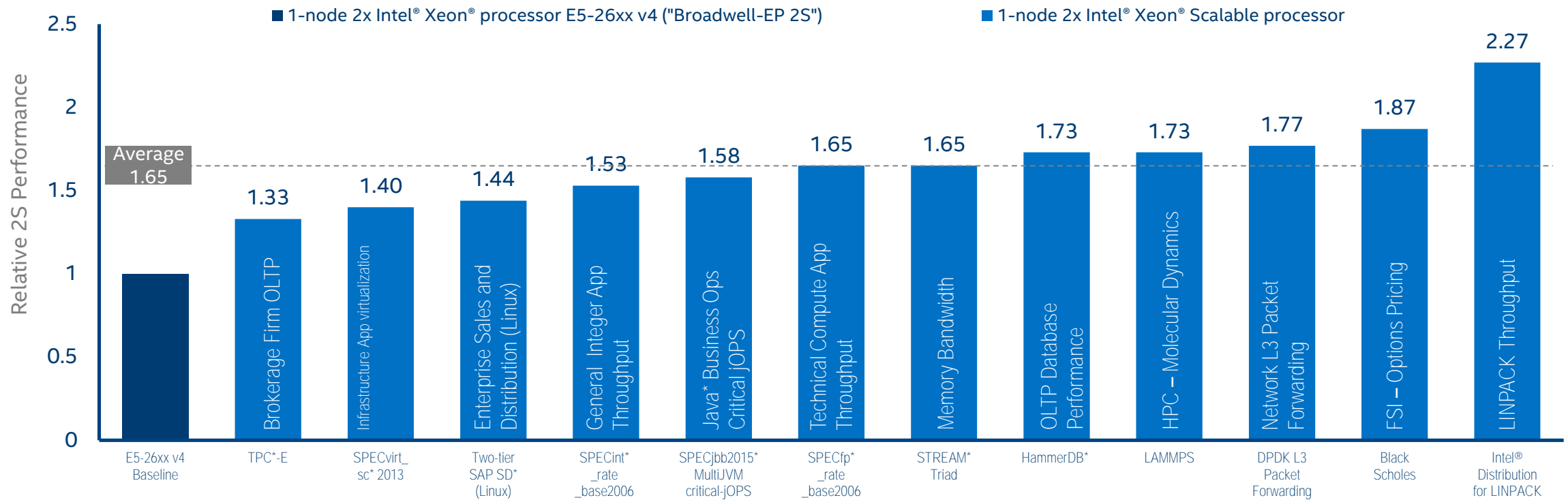
Bandwidth-Latency Profile



Source as of June 2017: Intel internal measurements on platform with Xeon Platinum 8180, Turbo enabled, UPI=10.4, SNC1/SNC2, 6x32GB DDR4-2400/2666 per CPU, 1 DPC, and platform with E5-2699 v4, Turbo enabled, 4x32GB DDR4-2400, RHEL 7.0. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to

1.65x Average¹ Generational Gains on 2-Socket Servers with Intel® Xeon® Scalable Processor

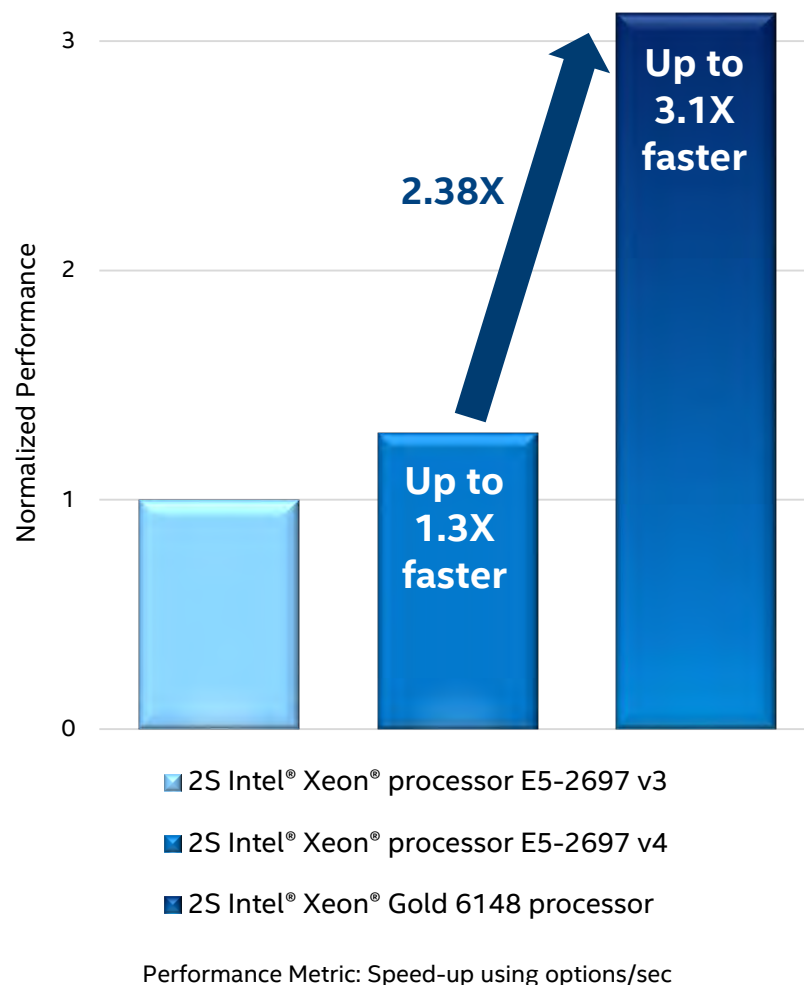
Higher is better



¹ Geomean based on Normalized Generational Performance (estimates based on Intel internal testing and published results of TPC-E, SPECvirt_sc*2013, SAP SD 2-Tier, SPEC*int_rate_base2006, SPEC*fp_rate_base2006, SPECjbb2015* MultiJVM, STREAM* triad, HammerDB, LAMMPS, DPDK L3 Packet Forwarding, Black-Scholes, Intel Distribution for LINPACK).

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to [Intel Performance Site](#). Intel does not control or audit the design or implementation of third party benchmark data or Web sites referenced in this document. Intel encourages all of its customers to visit the referenced Web sites or others where similar performance benchmark data are reported and confirm whether the referenced benchmark data are accurate and reflect performance of systems available for purchase. Configurations: see slides 23, 24. *Other names and brands may be claimed as the property of others.

Monte Carlo European Option increased performance with the 2S Intel® Xeon® Gold 6148 processor¹



¹ See configurations on slide 76.

MONTE CARLO EUROPEAN OPTIONS

Application:

Monte Carlo is a numerical method that uses statistical sampling techniques to approximate solutions to quantitative problems. In finance, Monte Carlo algorithms are used to evaluate complex instruments, portfolios, and investments. This is compute bound, double precision workload.

Potential Customer Benefits:

- Higher performance allow either doing the same work faster leading to improved TCO or simulation of more paths leading to higher confidence in results.

Performance Factors:

- Using Intel® AVX-512 SIMD vectorization improved performance by 1.85X over Intel® AVX2.
- Higher core counts of Intel Xeon® Gold 6148 processor contributes to higher performance.
- Better memory hierarchy adds to the performance
- Code modernization strategy: Parallelizing outer loop over options and vectorize inner loop of paths.

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AT A GLANCE

Hardware:

2S Intel® Xeon® Gold 6148 Processor

Platform Features:

Intel® Advanced Vector Extensions 512 (Intel® AVX-512)

More cores

Improved memory hierarchy

Software Tools/Libraries:

Intel® Parallel Studio XE 2017 Composer Edition (C++)

INTEL® XEON® SCALABLE PROCESSOR

The Secure, Agile, Next-Generation Platform for Multi-Cloud Infrastructures



PERVASIVE PERFORMANCE FOR ACTIONABLE INSIGHTS

Skylake-SP cores

Intel® AVX-512

Feeds: UPI, 6x DDR4, 3x16 PCIe,
Intel® SSDs

Integration: Intel® Ethernet /
Omni-Path / Intel® QuickAssist /
FPGA



SECURITY WITHOUT COMPROMISE

Intel® AVX-512

PPK, MPX, MBE

Intel® QAT w/ Secure Key
Management

Intel® Boot Guard

Intel® Trusted Infrastructure



AGILE SERVICE DELIVERY

Intel® Volume Management Device
Technology

Intel® RAS

Open Stack Software Optimizations

CODE THAT PERFORMS AND OUTPERFORMS

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Software

BENCHMARK CONFIGURATION SUMMARY

Configurations: Average Generational Gains on 2S Servers

1. 1.65x Average Performance: Geomean based on Normalized Generational Performance (estimates based on Intel internal testing and published results of TPC-E, SPECvirt_sc*2013, SAP SD 2-Tier, SPEC*int_rate_base2006, SPEC*fp_rate_base2006, SPECjbb2015* MultiJVM, STREAM* triad, HammerDB, LAMMPS, DPDK L3 Packet Forwarding, Black-Scholes, Intel Distribution for LINPACK).
 - a) Up to 1.33x on TPC*-E: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Lenovo Group Limited with 512 GB Total Memory on Windows Server* 2012 Standard using SQL Server 2016 Enterprise Edition. Data Source:http://www.tpc.org/tpce/results/tpce_result_detail.asp?id=116032402, Benchmark: TPC Benchmark* E (TPC-E), Score: 4938.14 vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 processor on Lenovo Group Limited with 1536 GB Total Memory on Windows Server* 2016 Standard using SQL Server 2017 Enterprise Edition. Data Source: http://www.tpc.org/tpce/results/tpce_result_detail.asp?id=117062701, Benchmark: TPC Benchmark* E (TPC-E), Score: 6598.36. Higher is better
 - b) Up to 1.40x on SPECvirt_sc* 2013: Claim based on best-published 2-socket SPECvirt_sc* 2013 result submitted to/published at http://www.spec.org/virt_sc2013/results/res2016q3/virt_sc2013-20160823-00060-perf.html as of 11 July 2017, Score: 2360 @ 137 VMs vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor with 768 GB (24 x 32 GB, 2R x4 PC4-2666 DDR4 2666MHz RDIMM) Total Memory on SUSE Linux Enterprise Server 12 SP2. Data Source: <http://www.spec.org>, Benchmark: SPECvirt_sc* 2013, Score: 3323 @ 189 VMs Higher is better
 - c) Up to 1.44x on 2-Tier SAP* SD : Claim based on best-published two-socket SAP SD 2-Tier on Linux* result published at <http://global.sap.com/solutions/benchmark/sd2tier.epx> as of 11 July 2017. New configuration: 2-tier, 2 x Intel® Xeon® Platinum 8180 Processor (56 cores/112 threads) on DellEMC PowerEdge* R740xd with 768 GB total memory on Red Hat Enterprise Linux* 7.3 using SAP Enhancement Package 5 for SAP ERP 6.0, SAP NetWeaver 7.22 pl21, and Sybase ASE 16.0. Source: Certification #: 2017017: www.sap.com/benchmark, SAP* SD 2-Tier enhancement package 5 for SAP ERP 6.0 score: 32,085 benchmark users.
 - d) Up to 1.53x on SPECint*_rate_base2006 : Claim based on best-published two-socket SPECint*_rate_base2006 result submitted to/published at <http://www.spec.org/cpu2006/results/> as of 11 July 2017. New configuration: 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Huawei 2288H V5 with 384 GB total memory on SUSE Linux Enterprise Server 12 SP2 (x86_64) Kernel 4.4.21-69-default, using C/C++: Version 17.0.1.132 of Intel C/C++ Compiler for Linux. Source: submitted to www.spec.org, SPECint*_rate_base2006 Score: 2800. Results are pending SPEC approval; they are considered estimates until SPEC approves
 - e) Up to 1.58x on SPECjbb*2015 MultiJVM critical-jOPS: Claim based on best-published two-socket SPECjbb*2015 MultiJVM critical-jOPS results published at <http://www.spec.org/jbb2015/results/jbb2015multijvm.html> as of 11 July 2017. New configuration: 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Cisco* Systems UCS C240 M5 with 1536 GB total memory on Red Hat Enterprise Linux* 7.3 (Maipo) using Java* HotSpot 64-bit Server VM, version 1.8.0_131. Source: submitted to <http://www.spec.org>, SPECjbb2015* - MultiJVM scores: 141,360 max-jOPS and 118,551 critical-jOPS
 - f) Up to 1.65x on SPECfp*_rate_base2006 :Claim based on best-published two-socket SPECfp*_rate_base2006 result submitted to/published at <http://www.spec.org/cpu2006/results/> as of 11 July 2017. New configuration: 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Huawei 2288H V5 with 384 GB total memory on SUSE Linux Enterprise Server 12 SP2 (x86_64) Kernel 4.4.21-69-default, using C/C++ and Fortran: Version 17.0.0.098 of Intel C/C++ and Intel Fortran Compiler for Linux. Source: submitted to www.spec.org, SPECfp*_rate_base2006 Score: 1850.
 - g) Up to 1.65x on STREAM - triad: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Grantley-EP (Wellsburg) with 256 GB Total Memory on Red Hat Enterprise Linux* 6.5 kernel 2.6.32-431 using Stream NTW avx2 measurements. Data Source: Request Number: 1709, Benchmark: STREAM - Triad, Score: 127.7 Higher is better vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Neon City with 384 GB Total Memory on Red Hat Enterprise Linux* 7.2-kernel 3.10.0-327 using STREAM AVX 512 Binaries. Data Source: Request Number: 2500, Benchmark: STREAM - Triad, Score: 199 Higher is better

Configurations: Average Generational Gains on 2S Servers

- h) Up to 1.73x on HammerDB: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Grantley-EP (Wellsburg) with 384 GB Total Memory on Red Hat Enterprise Linux* 7.1 kernel 3.10.0-229 using Oracle 12.1.0.2.0 (including database and grid) with 800 warehouses, HammerDB 2.18. Data Source: Request Number: 1645, Benchmark: HammerDB, Score: 4.13568e+006 Higher is better vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Purley-EP (Lewisburg) with 768 GB Total Memory on Oracle Linux* 7.2 using Oracle 12.1.0.2.0, HammerDB 2.18. Data Source: Request Number: 2510, Benchmark: HammerDB, Score: 7.18049e+006 Higher is better
- i) Up to 1.73x on LAMMPS: LAMMPS is a classical molecular dynamics code, and an acronym for Large-scale Atomic/Molecular Massively Parallel Simulator. It is used to simulate the movement of atoms to develop better therapeutics, improve alternative energy devices, develop new materials, and more. E5-2697 v4: 2S Intel® Xeon® processor E5-2697 v4, 2.3GHz, 36 cores, Intel® Turbo Boost Technology and Intel® Hyperthreading Technology on, BIOS 86B0271.R00, 8x16GB 2400MHz DDR4, Red Hat Enterprise Linux* 7.2 kernel 3.10.0-327. Gold 6148: 2S Intel® Xeon® Gold 6148 processor, 2.4GHz, 40 cores, Intel® Turbo Boost Technology and Intel® Hyperthreading Technology on, BIOS 86B.01.00.0412.R00, 12x16GB 2666MHz DDR4, Red Hat Enterprise Linux* 7.2 kernel 3.10.0-327.
- j) Up to 1.77x on DPDK L3 Packet Forwarding: E5-2658 v4: 5 x Intel® XL710-QDA2, DPDK 16.04. Benchmark: DPDK l3fwd sample application Score: 158 Gbits/s packet forwarding at 256B packet using cores. Gold 6152: Estimates based on Intel internal testing on Intel Xeon 6152 2.1 GHz, 2x Intel®, FM10420(RRC) Gen Dual Port 100GbE Ethernet controller (100Gbit/card) 2x Intel® XXV710 PCI Express Gen Dual Port 25GbE Ethernet controller (2x25G/card), DPDK 17.02. Score: 281 Gbits/s packet forwarding at 256B packet using cores, IO and memory on a single socket
- k) Up to 1.87x on Black-Scholes: which is a popular mathematical model used in finance for European option valuation. This is a double precision version. E5-2697 v4: 2S Intel® Xeon® processor CPU E5-2697 v4 , 2.3GHz, 36 cores, turbo and HT on, BIOS 86B0271.R00, 128GB total memory, 8 x16GB 2400 MHz DDR4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux* 7.2 kernel 3.10.0-327. Gold 6148: Intel® Xeon® Gold processor 6148@ 2.4GHz, H0QS, 40 cores 150W. QMS1, turbo and HT on, BIOS SE5C620.86B.01.00.0412.020920172159, 192GB total memory, 12 x 16 GB 2666 MHz DDR4 RDIMM, 1 x 800GB INTEL SSD SC2BA80, Red Hat Enterprise Linux* 7.2 kernel 3.10.0-327
- l) Up to 2.27x on LINPACK*: 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Grantley-EP (Wellsburg) with 64 GB Total Memory on Red Hat Enterprise Linux* 7.0 kernel 3.10.0-123 using MP_LINPACK 11.3.1 (Composer XE 2016 U1). Data Source: Request Number: 1636, Benchmark: Intel® Distribution of LINPACK, Score: 1446.4 Higher is better vs. 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Wolf Pass SKX with 384 GB Total Memory on Red Hat Enterprise Linux* 7.3 using mp_linpack_2017.1.013. Data Source: Request Number: 3753, Benchmark: Intel® Distribution of LINPACK, Score: 3295.57 Higher is better

Monte Carlo Benchmark Configuration Summary

Monte Carlo – Testing conducted on Monte Carlo software comparing 2S Intel® Xeon® Gold 6148 processor to 2S Intel® Xeon® Processor E5-2697 v3 and to 2S Intel® Xeon® Processor E5-2697 v4. OS: Red Hat Enterprise Linux* 7.2 kernel 3.10.0-327. Testing by Intel March 2017. BASELINE: 2S Intel® Xeon® processor E5-2697 v3, 2.6GHz, 28 cores, turbo and HT on, BIOS 86B.0036.R05, 64GB total memory, 8x8GB 2133 MHz DDR4, Fedora release 20 kernel 3.15.10-200. NEXT GEN: 2S Intel® Xeon® processor E5-2697 v4 , 2.3GHz, 36 cores, turbo and HT on, BIOS 86B0271.R00, 128GB total memory, 8 x16GB 2400 MHz DDR4 RDIMM, 1 x 1TB SATA, Red Hat Enterprise Linux* 7.2 kernel 3.10.0-327. NEW: 2S Intel® Xeon® Gold 6148 processor @ 2.4GHz, H0QS, 40 cores 150W. QMS1, turbo and HT on, BIOS SE5C620.86B.01.00.0412.020920172159, 192GB total memory, 12 x 16 GB 2666 MHz DDR4 RDIMM, 1 x 800GB Intel® SSD SC2BA80, Red Hat Enterprise Linux* 7.2 kernel 3.10.0-327.