Vladimir Kostyukov

Compiler Engineer

☎ *+7(923)1319766*
✉ *vladimir.v.kostyukov@gmail.com*
http://vkostyukov.ru

Summary

Software Engineer with 3 years of experience developing compilers and VMs. Creative and passionate programmer with in-depth knowledges of managed runtimes and compilers. Excellent Java and C/C++ programming skills allied with experience in performance analysis and benchmarking.

Skills

Programming Languages
Fluent in *Java* and *Scala*
Efficient in *C/C++*
Knowledges in *JavaScript*, *Python*, *Perl*

Scopes
Programming Languages Design and Implementation, Performance Analysis, Object Oriented Programming, Functional Programming, Purely Functional Data Structures, Design and Analysis of Algorithms

Experience

2011/04 – ... **Software Engineer**, Intel Corporation, Novosibirsk, Russia.

I am a member of the **Managed Runtimes** team. My first project there was development (from scratch) a proof of concept PKCS#11 Java Crypto Provider (5k LOC), which based on Intel IPP libraries. The developed prototype showed 6X speedup relative to the default Java implementation.
I am currently involved into development of the x86 Trace-JIT compiler (targeted to Intel® Atom™ Architecture) for Dalvik VM. More precisely, I am responsible for development of both back-end (including code generation and instruction scheduling) and middle-end (including data-flow analysis and optimizations on CFG) components of the compiler.
Tools: *Linux Shell, Git, Gerrit, Bugzilla, GCC, Intel VTune, Intel TBB, Intel IPP*
Keywords: *Performance Analysis, Compilers and Interpreters, JIT Compilation, Low-Level and High-Level Optimizations, Data-Flow Analysis, CFG Construction and Analysis, Instruction Scheduling, Registerization, Benchmarking, Debugging*

2010/10 – 2011/04 **Software Intern**, Intel Corporation, Novosibirsk, Russia.

As a member of **Compilers and Languages** group I was responsible for performance tracking and analysis of Intel Compiler for MIC platform (a GPUGP chip with up to 128 cores). I gained an Intel SSG Award for being a pioneer of Intel MIC compiler performance tracking (developed a Perl-based harness and ported initial four workloads from NVidia CUDA SDK).
Tools: *Intel Compiler Collections, Perl, Intel VTune, Linux Shell*
Keywords: *Performance Analysis, GPU Offload, Benchmarking, Multithreading and Concurrency, Synchronization, Parallel Algorithms, Lock-Free Algorithms*

2010/07 – 2010/08 **Summer School Intern**, Intel Corporation, Novosibirsk, Russia.
I was working in **Java Xeon** team on the analysis of bottlenecks in the SPECjvm2008.serial test at Intel's modern architectures. The suggested solution (based on reducing number of stack frames) showed up to 50% speedup on WSM-EX platform (in a multithreaded mode).
Tools: *Linux Shell, JDK, GCC, Intel VTune, Vim, SPECjvm2008, Eclipse*
Keywords: *Java Performance Analysis, Benchmarking, Concurrency, JMM, JVM Internals, Serialization*

2007/10 – 2010/07 **Technician**, Altai State Technical University, Barnaul, Russia.
While working in IT department, I was responsible for maintaining network environment of university campus. I also was leading a technical support team of ACM ICPC NEERC.
Tools: *Linux Shell, Clonezilla*
Keywords: *Scripting, OS Cloning, Network Administration*

Projects

la4j **Linear Algebra for Java**, http://la4j.org.
The la4j is a lightweight and 100% Java library that provides Linear Algebra primitives and algorithms. It is highly popular sparse/dense matrix library, which combines both fluent API and good performance.
Tools: *Java SE, Eclipse, Maven, jUnit, Git, Travis-CI*
Keywords: *Linear Algebra, Math, API Design, TDD, Design Patterns, Open Source*

Quipu **Quipu Programming Language**, http://esolangs.org/wiki/Quipu.
The Quipu is an Esoteric programming language inspired by «talking knots» – recording devices historically used by Incas. It is a «believed Turing-complete» language, which means author believes that the language is Turing-complete, but no formal proof was provided.
Tools: *Scala*
Keywords: *Source Code Parsing, Interpretation*

Education

2006 – 2011 **Master of Science** in CS, Altai State Technical University, Barnaul.
Master's thesis: *"Distributed monitoring and dispatching system of the processes in heterogenous environment"*.
Grade: 95/100

Certificates

2010 **IPPP-2-12**, Intel Parallel Programming Professional.
2010 **HPC School 2010**, Participant Certificate.
2010 **Intel Summer School 2010**, Participant Certificate.
2010 **Intel Winter School**, Participant Certificate.