XTend7100

COM Express® and PMC/XMC Carrier for Development and Testing

XTend7100 User's Manual

Revision A

X-ES
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...Always Fast

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XTend7100 User’s Manual

Revision History

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Safety Information

ESD Warning

Before handling any product described in this manual, please remember that electrostatic discharge (ESD) can easily damage electrical components and potentially result in product failure. The installer must be properly grounded at all times, else static charge will accumulate and may cause ESD damage.

Please adhere to the following guidelines to ensure the safety of your product:

- **Handle the product only when absolutely necessary.**
- **When handling the product, wear a grounding wrist strap at all times.**
- **Hold the product only by its edges. Do not touch any electrical components on the printed circuit board (PCB).**
- **Place the product only on a grounded ESD-dissipative mat. Simply placing the product on a static-shielding bag offers little to no ESD protection.**
- **Never place the product on metal or other conductive surfaces.**
- **If possible, store the product in an ESD-safe bag or clamshell when it is not in use.**

Manual Conventions

The following typographical and syntactical conventions are used throughout this manual:

`0x0`	This notation denotes a hexadecimal number.
`0b0`	This notation denotes a binary number.
#	When used as a postfix, this notation denotes an Active Low Signal (e.g., RESET#). It is also used to indicate the negative half of a signal pair (e.g., RX/RX# or TX/TX#).
-	This notation denotes an unused (unconnected) pin.

Overview

The XTend7100 is a COM Express and PMC/XMC carrier card designed to provide a low-cost and compact platform for development. The XTend7100, in conjunction with a standard off-the-shelf ATX power supply, provides a complete desktop or benchtop COM Express and PMC/XMC platform for development, evaluation, and testing.

The XTend7100 features an integrated fan below the PMC site to provide ample airflow for the most power-hungry PrPMCs. The XTend7100 also provides on-board +5 V, +3.3 V, and -12 V power supplies, sourcing only +12 V from the ATX power supply. This arrangement avoids the voltage drop and ampacity problems commonly associated with powering high power cards using ATX supplies.

The XTend7100 allows access to a small subset of the COM Express I/O via fixed connectors. The remaining I/O is accessible by utilizing compatible COM Express I/O Module (CIM) cards. The CIM site allows the XTend7100 to accommodate many different COM Express cards and provide access to any additional I/O not available via the XTend7100 integrated I/O connectors.

1.1 Features

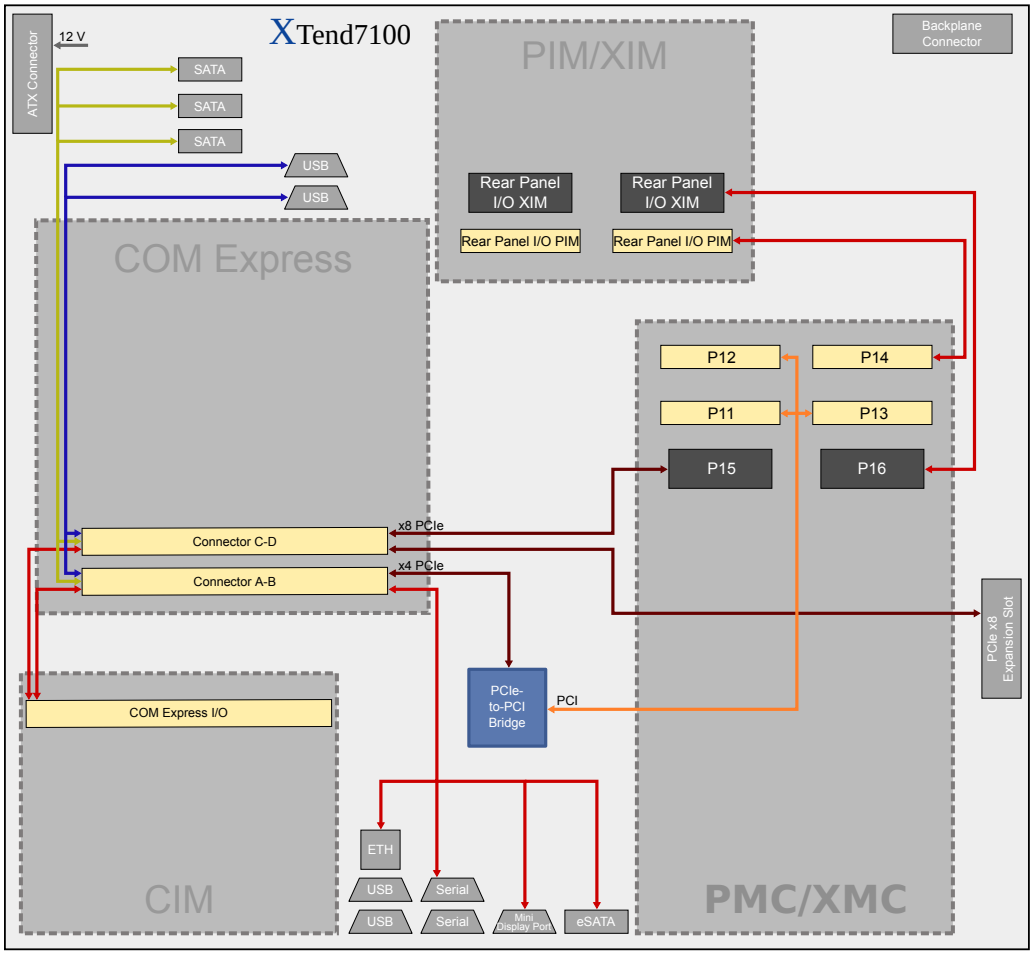
The following is a brief summary of the XTend7100's features:

- Single COM Express site with AB and CD connectors
- Supports Type 6 COM Express modules
- Single PMC/XMC site
- Single COM Express I/O Module (CIM) site
- Single PIM/XIM site for PMC/XMC card
- x8 PCIe edge connector
- ATX power supply connector
- Onboard +5 V, +3.3 V, and -12 V power supplies
- Micro ATX mounting holes for mounting in a standard PC chassis

1.2 Block Diagram

Figure 1.1 provides a high-level overview of the XTend7100.

Figure 1.1: General Block Diagram



1.3 Configurations

Table 1.1 describes the XTend7100 factory configuration options.

Table 1.1: Available Configurations

Part Number	Description
90071245-1	Benchtop configuration for Type 6 boards
90071245-2	Chassis configuration for Type 6 boards

1.4 Additional Information

Please refer to the documents listed within this section for additional information about the XTend7100 and its components that extends beyond the scope of this manual.

1.4.1 Standards

The technical information in this manual describes the unique features of the XTend7100. It is assumed that the reader has familiarity with the standard interfaces and devices incorporated into the XTend7100 that are not described in this manual.

Table 1.2 lists industry standards that apply to the XTend7100. Please see these documents for more information.

Table 1.2: Applicable Standards

Standard	Document	Author	Revision
IEEE P1386/Draft 2.4a	*Common Mezzanine Card Family: CMC*	IEEE	Ratified March 21, 2001
PCI Express	*PCI Express Base Specification*	PCI-SIG	Revision 3.0
PICMG COM.0	*COM Express® Module Base Specification*	PICMG	Rev. 2.1; May 14, 2012
-	*COM Express™ Carrier Design Guide*	PICMG	Rev. 1.0; March 13, 2009
VITA 20-2001	*Conduction Cooled PMC*	VITA	Ratified February 2005
VITA 36	*PMC I/O Module Specification*	VITA	Revision 0.1
VITA 42.0-2008	*XMC*	VITA	Ratified December 2008
VITA 42.3-2006	*XMC PCI Express Protocol Layer Standard*	VITA	Ratified June 2006
JTAG	*IEEE Standard 1149.1-1990*	IEEE	February 15, 1990

Quick Start

This chapter describes how to quickly get started using the XTend7100. It also provides information about troubleshooting, technical support, and service procedures.

ESD Caution

Before continuing, remember that you can potentially damage the XTend7100 and other electronic equipment by improperly handling it and failing to follow the appropriate precautionary measures.

If you have not done so already, please review the guidelines described in the Safety Information section at the beginning of this manual.

2.1 Requirements

The following are the minimum requirements for using the XTend7100 as described in this chapter:

- XTend7100 carrier card
- ATX power supply
- COM Express module
- Console, Ethernet, or other cabling for COM Express module

2.2 Supplying Power

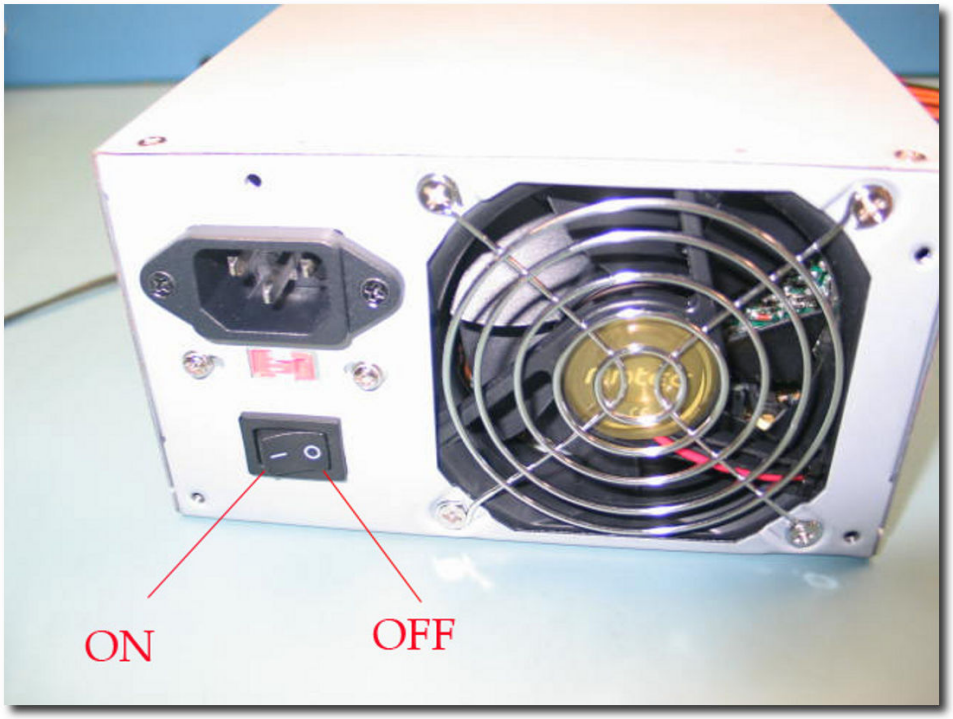
Verify that your ATX power supply is sufficient for the XTend7100 and any other modules you plan to connect to it. Most PC-compatible, 300 W or greater, ATX supplies can supply adequate power for the XTend7100.

2.3 Installing the XTend7100

To install the XTend7100, follow these steps:

1. Make sure ATX power supply's rear main switch on the back of the unit (usually located next to the unit's AC power input cable) is switched to the "off" position (usually denoted by an "O" character on the switch).

Figure 2.1: ATX Power Switch



2. Plug the ATX supply's AC power cable into the appropriate wall outlet and also into the back of the ATX supply.

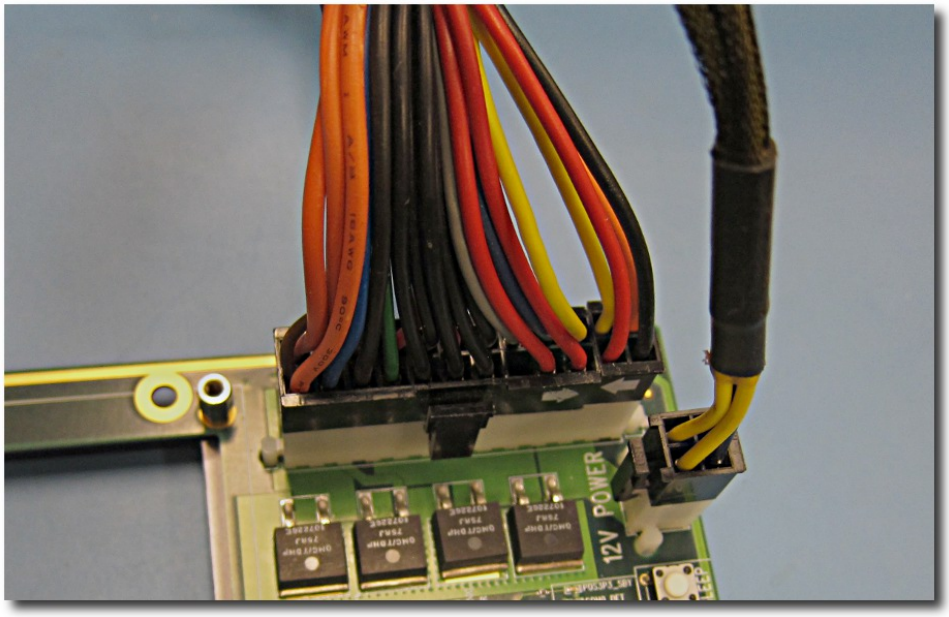
Figure 2.2: Plug AC Power Into Wall

Figure 2.3: Plug AC Power into Back of ATX Supply

3. Connect the ATX power supply's main 20- or 24-pin harness to the XTend7100's P960 connector, as shown in Figure 2.4. Ensure that the harness connector is securely snapped into this connector.

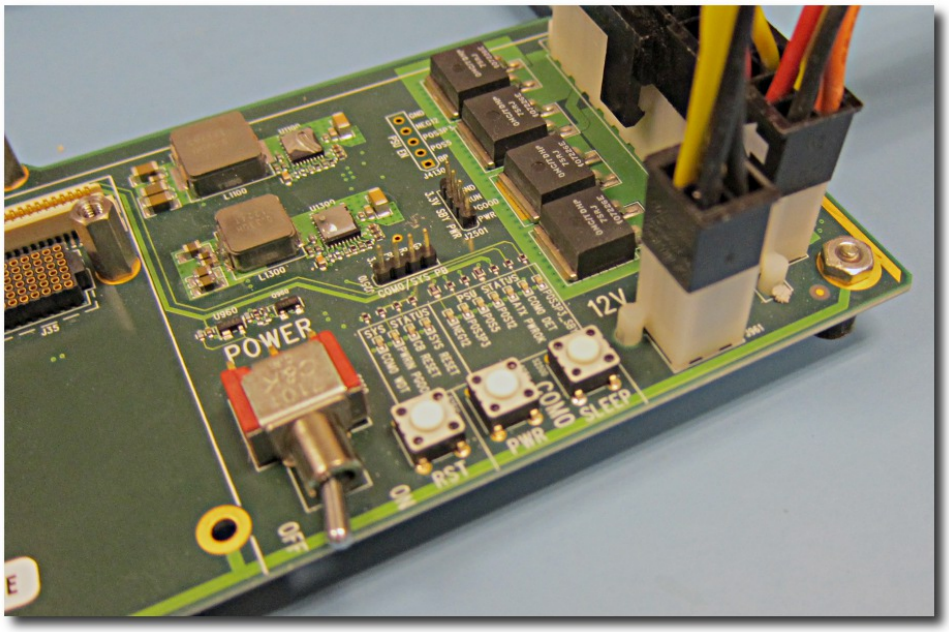
   If your ATX supply has a 4-pin 12 V power connector (yellow and black wires), plug this connector into the 12 V POWER connector (P961) of the XTend7100.

Figure 2.4: XTend7100 ATX Connections



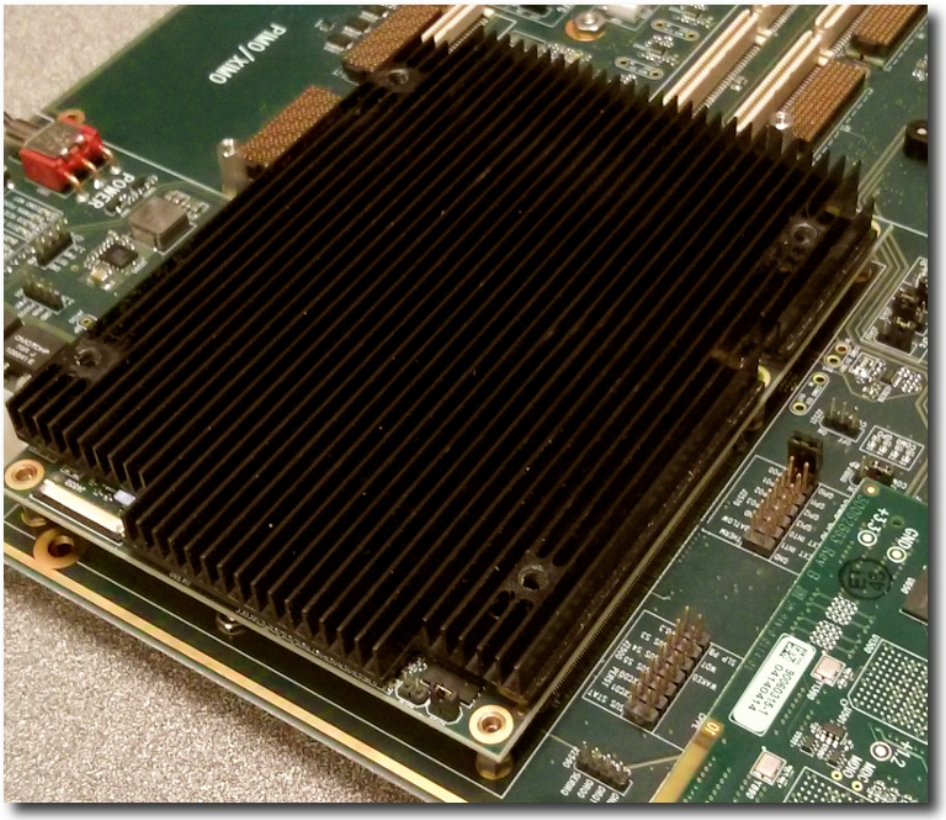
4. Make sure the XTend7100's POWER switch is in the "OFF" position, as shown in Figure 2.5.

Figure 2.5: XTend7100 Power Switch in OFF Position



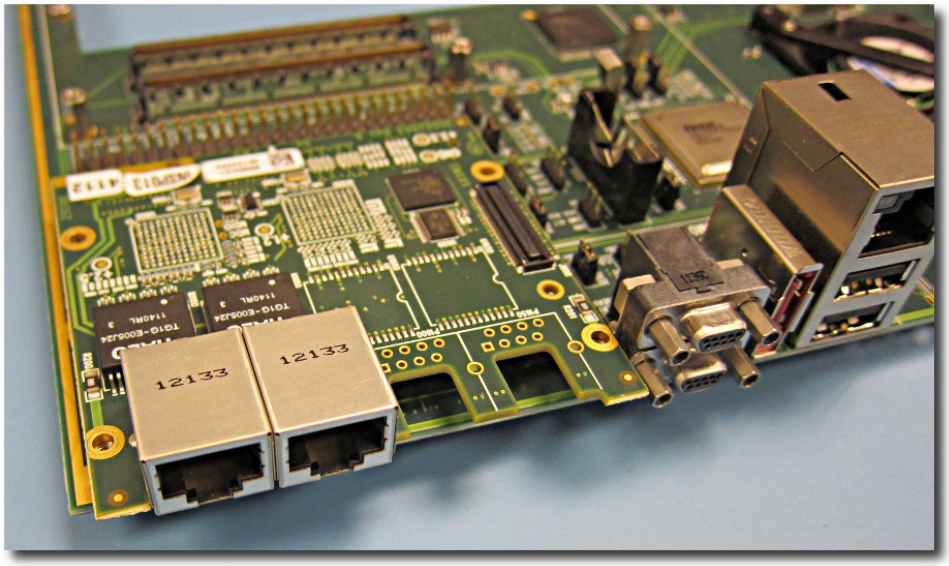
5. Install a COM Express module onto the COM0 site of the XTend7100, as shown in Figure 2.6.

Figure 2.6: COM0 Installed



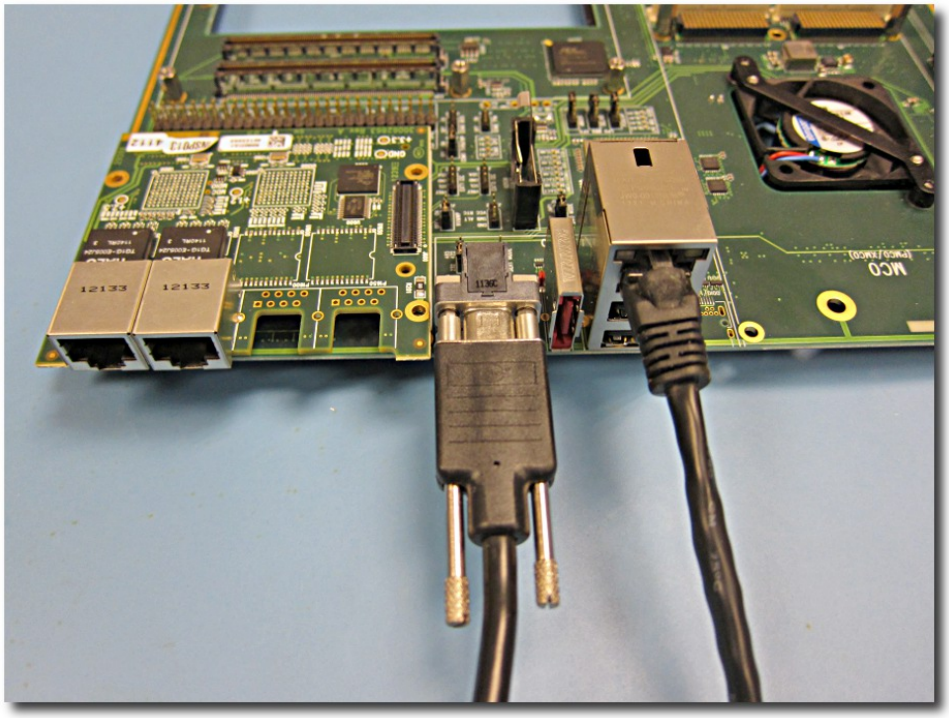
If applicable, install a CIM into the CIM0 site. This will provide additional I/O from the COM Express module.

Figure 2.7: CIM0 Installed



6. Connect the primary serial and Ethernet cables, as shown in Figure 2.8. Most X-ES modules use a 115200 baud rate with 8-N-1 and no flow control. Consult your COM Express card's user manual for specific host serial console settings. Connect any additional I/O to the CIM.

Figure 2.8: Connect I/O



7. Move the ATX power supply's switch from the OFF position to the ON position. Move the XTend7100's POWER switch from the OFF position to the ON position. You should see the green POS12, POS5, POS3P3, and NEG12 LEDs illuminate, indicating that the XTend7100 is powered up. The four 40 mm fans also should begin to spin immediately.

Figure 2.9: ATX Power Switch in ON Position

8. The COM Express module now should be powered up with console data output on the associated serial ports. If you do not see any serial output on your host machine, double check that you have the correct baud rate on your host machine, that the module securely seated in the COM0 site, and that the XTend7100 is getting power from the ATX supply. (See power LEDs in Section 3.7.)

2.3.1 Operational Notes

- *ALWAYS* power down the XTend7100 (via S960 or the ATX supply's main power switch) when installing or uninstalling any card.
- *Do not force any connector other than the +12 V yellow/black wired motherboard power connector into P961. Damage can occur to the XTend7100 or ATX supply if this is done.*
- Most ATX supplies have a restriction that prevents one from switching the main power switch on/off rapidly. When this is done, the ATX supply will go into fault mode and will not turn on for approximately 30 seconds. To prevent this, switch the main ATX power switch on/off at approximate 3 second intervals. (S960 does not have this restriction and is the recommended method to power cycle the card.)

2.4 Connecting the Serial Console

The simplest way to communicate with COM Express module on the XTend7100 is through a serial console connection. This can be done by connecting to an available COM port on a personal computer (PC) workstation. If you have not yet installed the COM Express module, please refer to Section 2.3 before continuing with this section.

Caution

Before making any connections, always check to make sure that all equipment is powered-down. Also, be sure to follow the appropriate handling procedures for ESD-sensitive devices.

To connect the serial console port, follow these steps:

1. Identify where to access the COM Express module's serial console port. Typically, this will be the fixed serial port connector (P2210).
2. Determine the appropriate cable configuration according to your connector. This depends on the serial console port connector itself, most often a micro-DB-9 connector. The X-ES part number for a Micro-DB-9 to DB-9 serial cable is 90000075.
3. Connect to the workstation's console port. Typically, this is either a male DB-9 connector or a standard female USB connector.

The remainder of this section describes various connection scenarios. If you have questions about the availability of specific configurations or need further assistance, please contact X-ES (see Section 2.6).

2.4.1 Connecting the PC Workstation Console

After determining the appropriate cable configuration and attaching it to the XTend7100's serial console port, connect the female DB-9 end of the cable to the console port on the PC workstation. Typically, this is either a male DB-9 or standard USB connector (see Figure 2.10).

Figure 2.10: Examples of DB-9 and USB Serial Port Connectors on PC Workstation

Connecting via a standard USB connector on the PC workstation also requires a male DB-9 to USB adapter cable (see Figure 2.11).

In this case, connect the cable from the XTend7100's serial port to adapter cable. Then connect the adapter cable to the PC workstation's USB port.

Note

In order to use the PC workstation's USB port, an appropriate USB-to-serial converter device driver must be installed on the PC workstation.

Figure 2.11: DB-9 to USB Adapter Cable

Figure 2.12 shows a PC workstation with a null modem cable attached. Also shown in this photo is a typical development system with a micro-DB-9 connector and adapter cable attached to the null modem cable. In this example, the micro-DB-9 serial connector is on a mezzanine card. However, it could also be on a rear transition module or other development system I/O panel.

Figure 2.12: PC Workstation with Null Modem Cabling Example

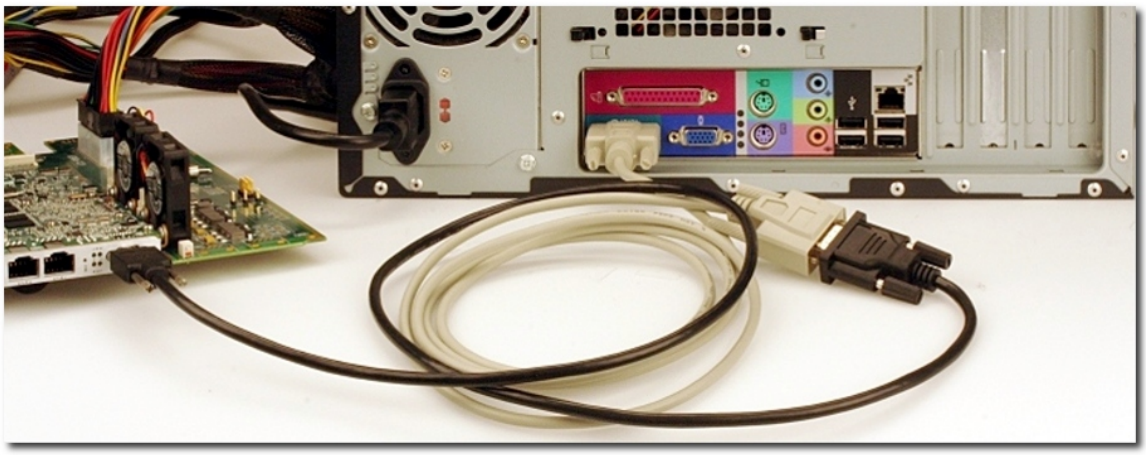


Figure 2.13 shows a PC workstation with a USB adapter cable and null modem cable attached. Also shown in this photo is a typical development system with a micro-DB-9 connector and adapter cable attached to the null modem cable. As in the other examples, the module's serial port could also be on a rear transition module or other development system I/O panel.

Figure 2.13: PC Workstation with USB Cabling Example

2.5 Basic Troubleshooting

In the event that the XTend7100 does not seem to be working properly, follow these troubleshooting steps:

1. Be sure the XTend7100 is fully connected to ATX power supply.
2. Be sure the system is not overheating.
3. Check that all required power cables are connected.
4. Check that any serial cables or network cables in use are securely connected.
5. Check the XTend7100 for proper DC voltages. Labelled test points for each of the card voltages are located on the back side of the module under the PMC site.

2.6 Technical Support

The X-ES SupportNet web site at https://support.xes-inc.com allows registered users to access product information, documentation updates, software downloads, and technical support. X-ES customers can request login access by following the New User Sign-Up link.

Contact X-ES using any of the following methods:

- SupportNet: https://support.xes-inc.com
- E-mail: <support@xes-inc.com>
- Phone: 608-833-1155

Before contacting X-ES support, please be prepared to supply the following information, where applicable:

- XTend7100 serial number

Tip

To determine the serial number of your XTend7100, look for the white or light-green sticker attached to the PCB. The serial number will be the eight-digit number directly below the part number (90071245).

- Chassis manufacturer and model number
- Manufacturer and model number of any other boards in the system, as applicable

- Any custom modifications to the XTend7100
- Serial console screen output of the error, if applicable

2.7 Service Information

If you need to return the XTend7100 to X-ES for service, please e-mail <support@xes-inc.com> or call 608-833-1155 and ask for a Return Merchandise Authorization (RMA) number. Be prepared to supply the XTend7100 serial number, the reason for return, and your original purchase order number.

When returning hardware that is out of warranty, billing information is required as well. Contact X-ES for any warranty-related questions.

When returning the XTend7100, be sure to enclose it in an anti-static bag or clamshell, such as the original shipping material. Send the XTend7100, pre-paid, to:

Extreme Engineering Solutions, Inc.
3225 Deming Way, Suite 120
Middleton, WI 53562
USA

Printed Circuit Board

This chapter provides detailed information about the XTend7100 printed circuit board (PCB). This information includes physical characteristics, power and environmental requirements, component maps, jumper definitions, and LED descriptions.

3.1 Physical Specifications

Table 3.1 describes the physical specifications of the XTend7100.

Table 3.1: Dimensions and Weight

Attribute	Value
Form Factor	Custom
Length	270 mm
Width	233.35 mm
Weight	Contact X-ES

3.2 Power Requirements

Table 3.2 gives the maximum current that can be drawn from the PMC site. In practice, this is limited by cooling capability, rather than by the DC-DC converters on the XTend7100.

Table 3.2: PrPMC Site Maximum Current Ratings

Voltage	Current
+3.3 V	10 A
+5.0 V	10 A
+12.0 V	Sourced from ATX supply
-12.0 V	2 A

Table 3.3 gives the maximum power that should be drawn from the ATX power supply. Note that +3.3 V, +5 V, and -12 V are loaded only by TO-220 package-type resistors to satisfy the minimum current requirements of the ATX specification.

Table 3.3: Maximum Current Requirements (from ATX Supply)

Voltage	Current
+3.3 V	44 mA (15-ohm resistor to GND)
+5.0 V	66 mA (10-ohm; resistor to GND)
+12.0 V	Max. current varies, depending on installed boards
-12.0 V	0.16 A (75-ohm resistor to GND)

3.3 Environmental Requirements

The XTend7100's conformance to a particular level is determined by rigorous analysis and testing. All qualification testing may not be completed at the time of this writing. Specific product configurations may be required to meet high-temperature operational requirements for certain levels. The low temperature limits for certain products may be below the operating temperature limits defined by the manufacturers of components used within the product assembly. In conjunction with performing qualification testing at these lower levels, X-ES also screens every product that falls into this category to verify operation at these lower temperatures.

Please contact X-ES for the most current information regarding this product.

Caution

Do not use the XTend7100 in an environment other than its intended one without contacting X-ES first.

Level 1 ruggedization, described in Table 3.4, is for standard commercial applications.

Table 3.4: Standard Air-Cooled - Level 1

Category	Specification
Operating Temp.	0 to +55°C ambient, 300 LFM, per MIL-STD-810F Method 501.4 Procedure II and Method 502.4 Procedure II
Storage Temp.	-40 to +85°C ambient*
Operating Vibration	0.002 g^2/Hz, 1 hour per axis from 5 to 2000 Hz
Operating Shock	20 g, 11 ms sawtooth, per MIL-STD-810F Method 516.5 Procedure I
Humidity	0 to 95% non-condensing, per MIL-STD-810F Method 507.4

*If the manufacturer's advertised storage temperature limit for any component used within this product does not meet these levels, these tests will be performed during qualification.

3.4 Component Maps

Figure 3.1: Front Component Map (Revision A)

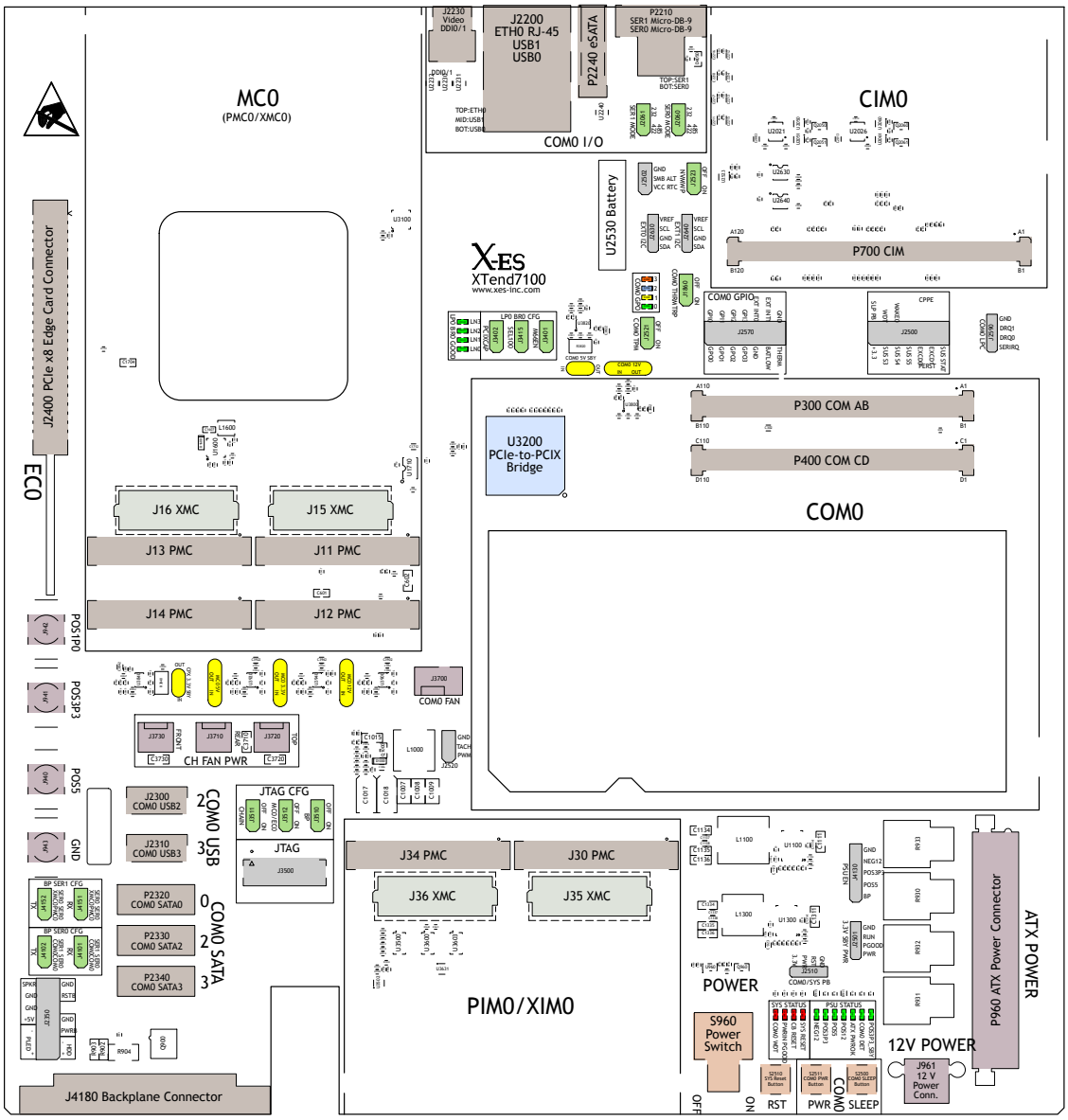
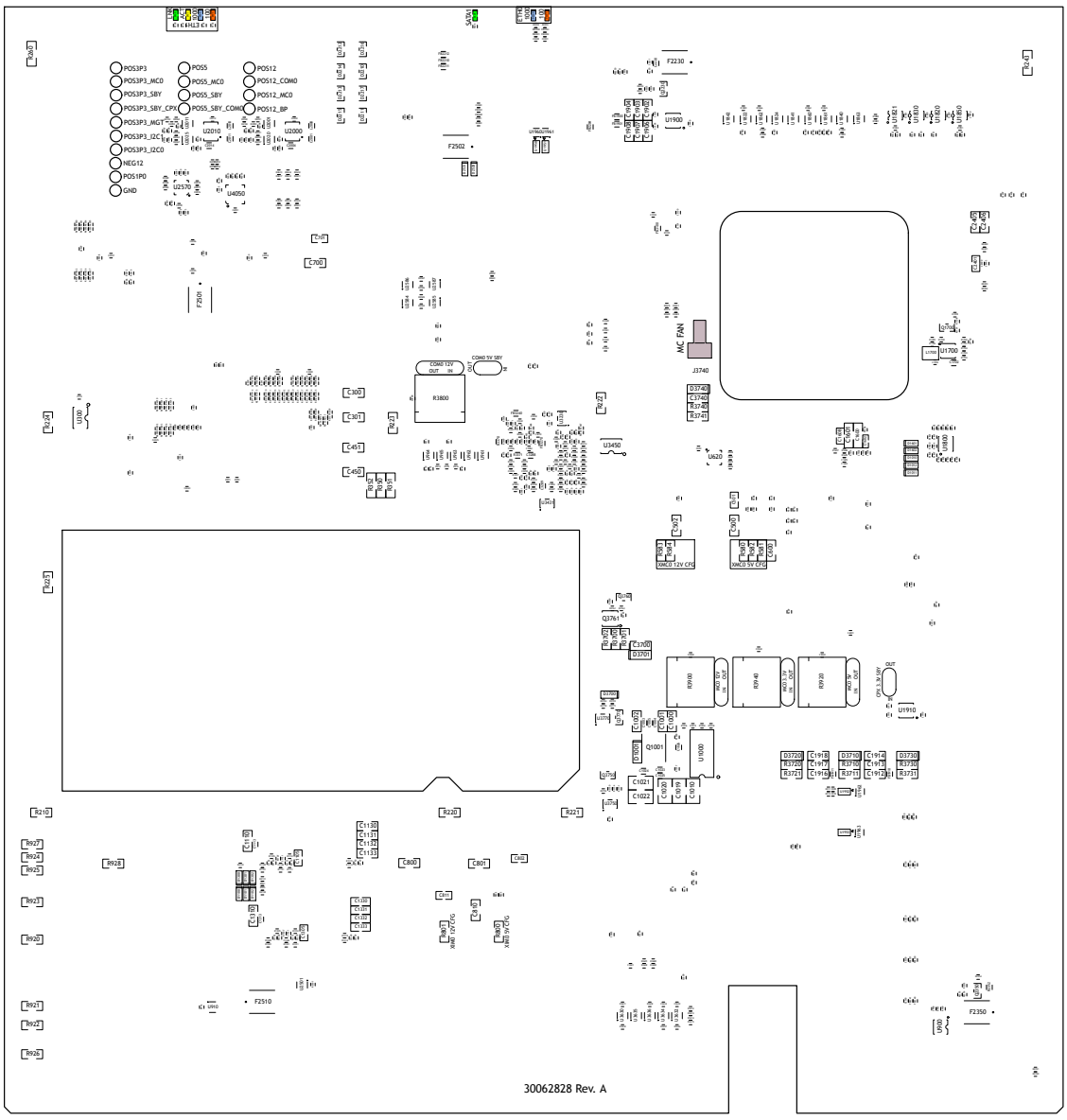


Figure 3.2: Back Component Map (Revision A)



3.5 Jumpers

Table 3.5 describes the jumpers used on the XTend7100.

Table 3.5: Jumper Functions

Jumper	Description
J1860	**COM0 Thermal Trip (COM0 THRMTRP).** Enables/disables thermal trip signal from COM Express card. See Table 4.16.
J2060/J2061	**Serial Mode (SER0 MODE / SER1 MODE).** Configures serial ports 0 and 1 for RS-232 or RS-422 mode. See Table 4.12.
J2521	**COM0 TPM Select (COM0 TPM).** Enables/disables TPM. See Table 4.17.
J2523	**Non-volatile Memory Write-Protection (NVMWP).** Enables/disables non-volatile memory write protection. See Table 4.15.
J3401	**PCI Rate (M66EN).** Determines the PCI bus rate. See Section 5.3.
J3402	**PCI Mode (PCIXCAP).** Determines the PCI bus mode. See Section 5.3.
J3415	**PCI-X 100 MHz Enable (SEL100).** Determines whether 100 MHz PCI-X bus rate is enabled. See Section 5.3.
J3510	**JTAG On/Off (BP).** Factory use only.
J3511	**JTAG Chain On/Off (CHAIN).** Turns JTAG chain on/off. See Table 9.2.
J3512	**JTAG Hosted Card On/Off (MC0/EC0).** Turns JTAG on/off for hosted mezzanine or edge card. See Table 9.2.
J4101/J4102	**Backplane SER0 Configuration (BP SER0 CFG).** Factory use only.
J4151/J4152	**Backplane SER1 Configuration (BP SER0 CFG).** Factory use only.

3.6 Headers

Table 3.6 summarizes the headers used on the XTend7100.

Table 3.6: Header Functions

Header	Description
J2350	**ATX Front Panel Connector.** Connects the various buttons/LEDs found in the front of a standard ATX chassis to the XTend7100.
J2500	**COM0 Standby Header (COM0 SBY).** See Section 4.6.1.
J2501	**3.3 V Standby Power Header (3.3V SBY PWR).** Provides access to +3.3 V Standby control signals.
J2502	**RTC Power / SMBus Alert.** Provides access to RTC power and SMBus alert functionality. See Section 4.6.4.
J2510	**COM0 Power and System Reset Buttons Header (COM0/SYS PB).** Provides access to RESET# and PWRBTN# signals from header.
J2520	**Fan Control Header.** Provides an access point to monitor the fan PWM and RPM, if supported on the COM Express module.
J2570	**COM0 GPIO Header (COM0 GPIO).** See Section 4.6.3.
J2590	**LPC Header (COM0 LPC).** See Section 4.6.2.
J2630/J2640	**External I²C Headers (EXT0/EXT1 I²C).** See Section 4.2.6.
J3500	**JTAG Header.** See Chapter 9.
J3710	**Rear Chassis Fan Power Header (REAR).** Connector for rear chassis fan power.
J3720	**Side/Top Chassis Fan Power Header (TOP).** Connector for side/top chassis fan power.
J3730	**Front Chassis Fan Power Header (FRONT).** Connector for front chassis fan power.
J3740	**Mezzanine Card Fan Power Header (MC FAN).** Connector for mezzanine card fan power.
J4130	**PSU Enable Header (PSU EN).** Provides access to enable signals for +5 V, +3.3 V , -12 V supplies.

3.7 LEDs

Table 3.7 describes the LEDs used on the XTend7100.

Table 3.7: LED Definitions

LED	Color	Description
D1840	Red	**PWRIN PGOOD System Status.** When illuminated, indicates that the input power from the ATX connector is out of tolerance.
D1841	Red	**SYS RESET System Status.** When illuminated, indicates that SYS_RESET# input to the COM Express module is asserted.
D1842	Red	**CB RESET System Status.** When illuminated, indicates that the CB_RESET# signal is asserted. This signal is a reset input to every subsystem on the carrier, except the COM Express module.
D2200	Blue	**ETH0 Gigabit Ethernet Link.** Indicates Ethernet port 0 is linked at 1000 Mb/s.
D2201	Orange	**ETH0 Ethernet 100 Mb Link.** Indicates Ethernet port 0 is linked at 100 Mb/s.
D2502	Red	**COM0 WDT System Status.** When illuminated, indicates that the WDT output from the COM Express module is asserted.
D2584	Green	**COM0 GPO 0.** Illuminated when GP00 is driven high.
D2585	Yellow	**COM0 GPO 1.** Illuminated when GP01 is driven high.
D2586	Blue	**COM0 GPO 2.** Illuminated when GP02 is driven high.
D2587	Orange	**COM0 GPO 3.** Illuminated when GP03 is driven high.
D304	Green	**SATA1 Status.** Used by the COM Express module to indicate SATA activity.
D3340	Green	**PCI Bridge Lane 3 Good.** When lit, indicates PCIe bridge lane 3 is good.

Table 3.7: LED Definitions *(continued)*

LED	Color	Description
D3341	Green	**PCI Bridge Lane 2 Good.** When lit, indicates PCIe bridge lane 2 is good.
D3342	Green	**PCI Bridge Lane 1 Good.** When lit, indicates PCIe bridge lane 1 is good.
D3343	Green	**PCI Bridge Lane 0 Good.** When lit, indicates PCIe bridge lane 0 is good.
D700	Green	**ETH1 Ethernet Link.** Indicates Ethernet port 1 is linked.
D701	Yellow	**ETH1 Ethernet Activity.** Indicates Ethernet port 1 activity.
D702	Blue	**ETH1 Ethernet Gigabit Link.** Indicates Ethernet port 1 is linked at 1000 Mb/s.
D703	Orange	**ETH1 Ethernet 100 Mb Link.** Indicates Ethernet port 1 is linked at 100 Mb/s.
D910	Green	**ATX PWROK Power Supply Status.** When illuminated, indicates that ATX_PWR is OK.
D911	Green	**POS12 Power Supply Status.** When illuminated, indicates that the POS12 voltage is up.
D912	Green	**POS5 Power Supply Status.** When illuminated, indicates that the POS5 voltage is up.
D913	Green	**POS3P3 Power Supply Status.** When illuminated, indicates that the POS3P3 voltage is up.
D914	Green	**POS3P3_SBY Power Supply Status.** When illuminated, indicates that the POS3P3_SBY standby voltage is up.
D915	Green	**NEG12 Power Supply Status.** When illuminated, indicates that the NEG12 voltage is up.
D960	Green	**COM0 DET Power Supply Status.** When illuminated, indicates a supported COM Express card is installed.

3.8 Switches and Buttons

This section describes the various on-board switches for the XTend7100. Refer to the component map in Section 3.4 for the locations of these switches.

3.8.1 Power Switch

A SPDT power switch (S960) is provided. This switch, in conjunction with a MAX6816 de-bouncer, grounds or disconnects from ground pin 14 of the ATX connector (P960). This effectively turns the ATX supply on and off in a "soft" fashion (rather than using the power switch on the back of the supply). When S960 is flipped in the position towards the ATX power, connector, the PS_ON# signal is grounded, and the ATX supply turns on. When flipped in the position away from the ATX connector, PS_ON# is disconnected from ground, and the ATX supply turns off.

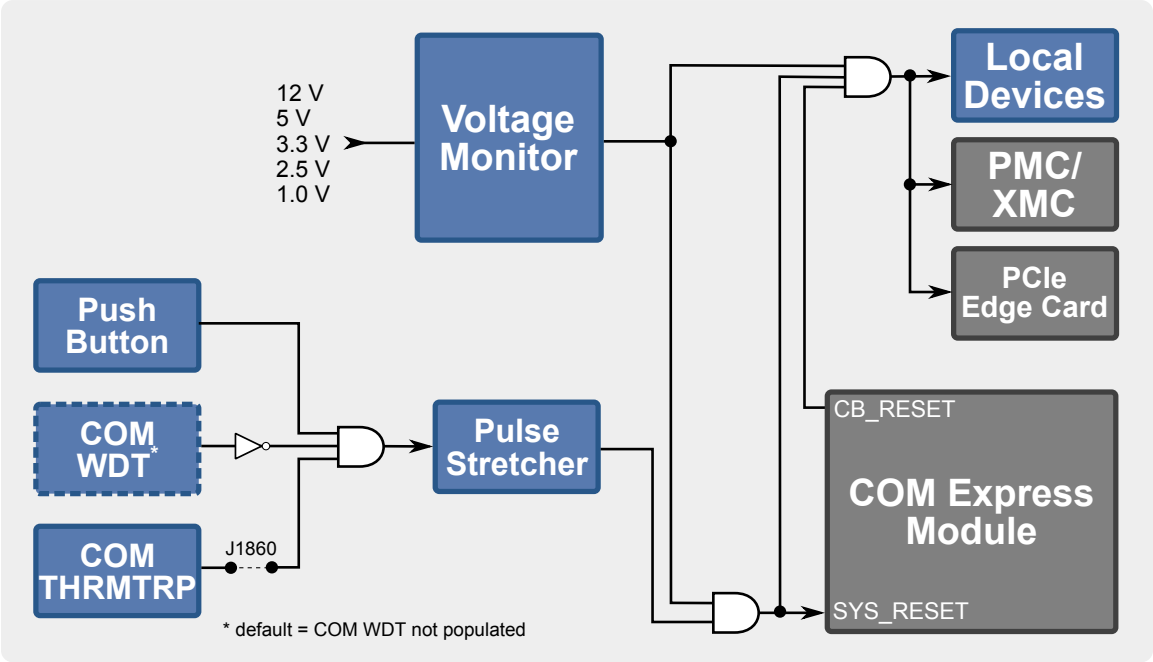
Note

This switch is applicable for use only in XTend7100 desktop configurations. It has no effect in chassis configurations.

3.8.2 Reset Button

A momentary button switch (S2510) is provided near the main power switch. When pressed, it issues a reset to the entire backplane.

Figure 3.3: Reset Block Diagram



3.8.3 Sleep and Power Buttons

The XTend7100 has two additional buttons near the power switch that affect the COM Express interface, as described in Table 3.8.

Note

On Rev. A XTend7100 chassis configurations, the power button (S2511) does not assert the PWRBTN# pin on the COM Express connector. The PWRBTN# trace is disconnected from the COM Express module to serve as a chassis power button input. PWRBTN# is wired into the chassis front panel power switch to control power on/off.

Table 3.8: COM0 Power and Sleep Buttons

Name	Ref. Des.	Description
COM0 SLEEP	S2500	When pressed, causes the SLEEP# pin on the COM Express connector to be asserted.
COM0 PWR	S2511	When pressed, causes the PWRBTN# pin on the COM Express connector to be asserted.

3.9 ATX Power Connectors

A 24-pin ATX Power Connector (P960) is provided to allow the XTend7100 to receive power. A PC-compatible ATX power supply is all that is required. All configurations feature load resistors on the +12 V, -12 V, +5 V, and +3.3 V lines in order to satisfy minimum loading requirements per the ATX Specification.

An optional 4-pin +12 VDC Power Connector (P961) is also provided. This is intended for use with newer ATX supplies, which feature the +12 V motherboard power harness (yellow and black wires). This connector is only provided as an option to provide more amperage, above the single +12 V wire that P960 provides.

Caution

To avoid damage to the XTend7100 only plug the ATX supply's four-pin, yellow and black-wired connector into P961.

Table 3.9: Connector Pinout, ATX Power, P960

Pin	Signal	Pin	Signal
1	+3.3V_ATX	2	+3.3V_ATX
3	GND	4	+5V_ATX
5	GND	6	+5V_ATX
7	GND	8	-
9	+5V_SB	10	+12V
11	+12V_ATX	12	+3.3V_ATXV
13	+3.3V_ATX	14	-12V_ATX
15	GND	16	PS_ON#
17	GND	18	GND
19	GND	20	-

Table 3.9: Connector Pinout, ATX Power, P960 *(continued)*

Pin	Signal	Pin	Signal
21	+5V_ATX	22	+5V_ATX
23	+5V_ATX	24	GND

Table 3.10: Connector Pinout, ATX Power (+12 V), P961

Pin	Signal	Pin	Signal
1	GND	2	GND
3	+12V	4	+12V

3.10 Local Power Supplies

The XTend7100 implements three DC-DC converter power supplies. These are 12 V to 5 V, 12 V to 3.3 V, and 12 V to -12 V buck converters. The purpose of these converters is to lift the cross-loading limitations which many ATX power supplies exhibit when powering high-current loads.

ATX power supplies, due to cost constraints, typically have only a single transformer inside with a single control input to control the level of the 12 V, 5 V, and 3.3 V rails, concurrently. When the ATX supply sees a large load on one rail, it must dynamically adjust the single transformer's pulse width to regulate the voltage of that rail. Since there is only one transformer, adjusting the transformer pulse width to bring one voltage into specification will often throw the other voltages off. This can cause unpredictable behavior when powering devices such as PrPMCs, which typically use lots of +5 V and/or +3.3 V and little to no +12 V and also exhibit current transients (for example, when starting a second CPU on a dual processor PrPMC). The XTend7100 eliminates this limitation by only sourcing +12 V from the ATX supply (of which ATX supplies typically provide ample power through) and providing only the minimum loads on +5 V, +3.3 V, and -12 V from the ATX connector so the cross loading is fairly static in nature.

Another problem with ATX supplies is voltage drop on the 3.3 V rail. Due to the low voltage and high current that is commonly present on this rail when powering PrPMCs, the I^2R drop from the ATX supply to the PrPMC can often be significant, especially when routed through multiple current limiters or Hot Swap circuitry, which is commonly found on cPCI and/or VME carriers. Since the 3.3 V rail has a fairly tight tolerance, any accumulated drop across backplanes and Hot Swap FETs can result in a PrPMC whose power-on reset monitor chip activates during current transients, resetting the board unexpectedly. The XTend7100 avoids this problem by providing a direct power plane and independent regulators for the PrPMC +5 V, +3.3 V, and -12 V rails.

3.11 Backplane Connector

A 32-pin backplane connector (Molex P/N 85001-0012) is provided for interfacing with an XTend5000 backplane in a manufacturing test environment. Note that this connector is only populated on some configurations of XTend7100 and typically is not used for desktop operation. Please contact X-ES support for more information on XTend5000 and J4180.

Table 3.11: Connector Pinout, Backplane, J4180

Pin	Signal	Pin	Signal
1	+12V_BP	2	GND
3	+12V_BP	4	GND
5	+12V_BP	6	GND
7	+12V_BP	8	GND
9	+12V_BP	10	GND
11	+12V_BP	12	GND
15	BP_SER0_TX_A	16	BP_SER0_RX_A
17	BP_SER1_TX_A	18	BP_SER1_RX_A
19	BP_PWREN	22	-12V_SHDN_BP#
23	JTAG_BP_TCK	24	RST_BP#
25	JTAG_BP_TMS	26	BP_SHDN0#
27	JTAG_BP_TRST#	28	BP_SHDN1#
29	JTAG_BP_TDI	30	+5V_RUN_BP
31	JTAG_BP_TDO	32	+3.3VA_RUN_BP

COM Express Interface

This chapter describes details associated with the XTend7100's COM Express® interface. The XTend7100 can host a type 6 COM Express module (see Section 1.3). The XTend7100 provides access to nearly every COM Express signal, either through fixed I/O, the COM Express I/O module, or via 0.1 in. headers.

4.1 PCI Express

The XTend7100 can support different PCIe topologies from the COM Express module. Eight PCIe lanes run from the x8 PCIe expansion slot. Also, eight lanes go to the P15 connector, and four lanes go to the PCIe-to-PCI bridge.

4.2 I²C

The XTend7100 supports two I²C interfaces, I²C0 and I²C1. All devices use standard 7-bit I²C addressing; their addresses, as defined here, do not include the 8th R/W bit used in an actual I²C cycle. Table 4.1 and Table 4.2 describe the device assignments.

Table 4.1: I²C0 Device Assignment

Address	Device
20	PCA9670 COM GPI Loopback
24	PCA9670 Mezzanine Site GPIO
40-45	INA219B Current/Voltage Monitoring Devices
50	XMC PCIe J15 Connector SEEPROM
57	M24512 SEEPROM (512 kilobit)
-	CIM Site. Refer to CIM user's manual to determine if any I²C devices are present.
-	External Header. See Section 4.2.6 for more information.
-	PCI Express Edge Card Slot. See Chapter 7 for more information.

Table 4.2: I²C1 Device Assignment

Address	Device
20	PCA9670 COM GPI Loopback
24	PCA9670 Mezzanine Site GPIO
40-45	INA219B Current/Voltage Monitoring Devices
57	M24512 SEEPROM (512 kilobit)
-	CIM Site. Refer to CIM user's manual to determine if any I²C devices are present.
-	External Header. See Section 4.2.6 for more information.
-	PCI Express Edge Card Slot. See Chapter 7 for more information.

4.2.1 PCA9670 COM GPI Loopback (0x20)

The XTend7100 supports PCA9670 COM GPI Loopback at I²C address 0x20. This is intended primarily for factory use. Table 4.3 shows the device's external pin connections.

Table 4.3: I²C GPIO Pins, PCA9670 Mezzanine Site

Pin	Assignment
7	**COM0_BATLOW#.** Connected to the COM0_BATLOW# net.
6	**COM0_THRM#.** Connected to the COM0_THRM# net.
5	**COM0_EXT_INT1#.** Connected to the COM0_EXT_INT1# net.
4	**COM0_EXT_INT0#.** Connected to the COM0_EXT_INT0# net.
3	**COM0_GPI_3#.** Connected to the COM0_GPI_3# net.
2	**COM0_GPI_2#.** Connected to the COM0_GPI_2# net.
1	**COM0_GPI_1#.** Connected to the COM0_GPI_1# net.
0	**COM0_GPI_0#.** Connected to the COM0_GPI_0# net.

4.2.2 PCA9670 Mezzanine Site GPIO (0x25)

The PCA9670 GPIO device at I²C address 0x25 provides access to the Mezzanine Site GPIO. Table 4.4 shows the device's external pin connections.

Table 4.4: I²C GPIO Pins, PCA9670 Mezzanine Site

Pin	Assignment
7	**PMC Enumeration Ready.** Reads the state of the PMC EREADY (J22.58) pin.
6	**PMC Monarch.** Reads the state of the PMC MONARCH# (J22.64) pin.
5	**PMC Present.** Reads the state of the PMC PRESENT# (J21.7) pin.
4	**XMC Present.** Reads the state of the XMC MPRESENT# (J25.F12) pin.
3	**XMC Built-in Self Test.** Reads the state of the XMC MBIST# (J25.C11) pin.
2	**XMC Wake.** Reads the state of the XMC WAKE# (J25.D19) pin.
1	**No Connection.**
0	**XMC Root.** Reads the state of the XMC ROOT0# (J25.E19) pin.

4.2.3 INA219B Monitor Devices (0x40-0x45)

These devices allow the XTend7100 to determine power consumption for the PMC/XMC and COM Express sites. See Chapter 8 for details.

4.2.4 XMC Mezzanine Site (0x50)

The XTend7100 assigns Geographical Address 0x50 to the module hosted in the XMC site. Please see the module's datasheet for more information.

4.2.5 M24512 SEEPROM (0x57)

The STMicro M24512 I²C serial EEPROM provides 64 KB of non-volatile storage.

4.2.6 I²C Headers

Two internal headers, J2630 and J2640 (see Section 3.4), provide access for external I²C devices. A PCA9517 I²C-level translator separates the onboard I²C interface and the headers, which are wired up to the A side of the PCA9517 and can be connected to I²C buses with voltages from 0.9 V to 5.5 V. Please refer to the *PCA9517 Datasheet* for more information.

Note

The XTend7100 does not provide any power or pull-up resistors for the external I²C interface.

Table 4.5: Connector Pinout, I²C Headers, J2630/J2640 (EXT0/EXT1 I²C)

Pin	Signal	Description
1	HDR*n*_I2C_SDA	External I²C Serial Data
2	GND	Ground
3	HDR*n*_I2C_SCL	External I²C Serial Clock
4	HDR*n*_I2C_VREF	Provides a voltage reference equal to the operating I²C bus voltage

4.3 External I/O Connectors

The XTend7100 has I/O available on the periphery of the board between the PMC/XMC site and the CIM site. The connectors in this area consist of one Mini DisplayPort (mDP), one RJ-45, two USB 2.0 ports, one eSATA port, and two RS-232/422 serial ports. The second serial port can be converted to a Controller Area Network (CAN) bus for modules that support it.

4.3.1 Mini DisplayPort Connector

The XTend7100's rear panel video port connector is a Mini DisplayPort connector. Figure 4.1 shows the pin locations in the connector, and Table 4.6 lists the pinout. Please contact X-ES for details regarding Mini DisplayPort-to-DisplayPort, -DVI, or -HDMI cables.

Figure 4.1: Mini DisplayPort Connector

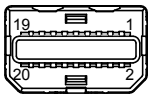


Table 4.6: Connector Pinout, Rear Panel Video DDI0/DDI1

Pin	Signal	Pin	Signal
1	GND	2	DDI0_HPD
3	DDI0_0	4	DDI0_AUX_SEL
5	DDI0_0#	6	1 MΩ pull-down
7	GND	8	GND
9	DDI0_1	10	DDI0_3
11	DDI0_1#	12	DDI0_3#
13	GND	14	GND
15	DDI0_2	16	DDI0_CTRLCLK_AUX
17	DDI0_2#	18	DDI0_CTRLDATA_AUX#
19	GND	20	DDI0_PWR (fused 3.3 V)

4.3.2 Ethernet Connector

The XTend7100's rear Ethernet port is accessible via an RJ-45 connector. Figure 4.2 shows the pin locations in the connector, and Table 4.7 lists the pinout. The status of the COM Express LINK1000# and LINK100# signals are given by LEDs D2200 (blue) and D2201 (orange), respectively.

Figure 4.2: RJ-45 Connector

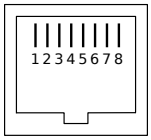


Table 4.7: Connector Pinout, Rear Panel ETH0

Pin	Signal	Pin	Signal
1	BI_DA (bi-directional pair A+)	2	BI_DA# (bi-directional pair A-)
3	BI_DB (bi-directional pair B+)	4	BI_DC (bi-directional pair C+)
5	BI_DC# (bi-directional pair C-)	6	BI_DB# (bi-directional pair B-)
7	BI_DD (bi-directional pair D+)	8	BI_DD# (bi-directional pair D-)

4.3.3 USB Connectors

The XTend7100's rear panel USB 2.0 ports are accessible via two, stacked, standard, Type A, USB connectors. Figure 4.3 shows the pin locations in the connector, and Table 4.8 lists the pinout. Note that USB1 is located at the top of the stack, and USB0 is on the bottom.

Figure 4.3: USB Connectors

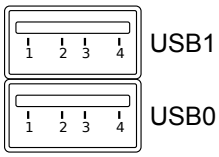


Table 4.8: Connector Pinout, Rear Panel USB0/USB1

Pin	Signal
1	V_{CC} (current-limited +5 V USB power)
2	DATA#
3	DATA
4	GND

4.3.4 eSATA Connector

The XTend7200 includes an eSATA jack on the rear I/O area. Figure 4.4 shows the pin locations in the connector, and Table 4.9 lists the pinout.

Figure 4.4: eSATA Connector

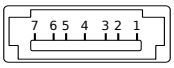


Table 4.9: Connector Pinout, Rear Panel SATA1

Pin	Signal
1	GND
2	B+ (Receive +)
3	B- (Receive -)
4	GND
5	A- (Transmit -)
6	A+ (Transmit +)
7	GND

4.3.5 Serial Connectors

The XTend7100 provides dual serial ports on the rear I/O panel via stacked micro-DB-9 connectors. Figure 4.5 shows the pin locations in the connector. Table 4.10 and Table 4.11 list the pinouts. Note that SER1 has a configuration option to support CANbus.

Figure 4.5: Micro-DB-9 Connectors

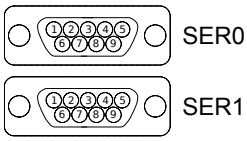


Table 4.10: Connector Pinout, Rear Panel SER0

Pin	Signal	Pin	Signal
1	-	2	Received Data 0
3	Transmitted Data 0	4	Received Data 1
5	GND	6	Transmitted Data 1

Table 4.10: Connector Pinout, Rear Panel SER0 *(continued)*

Pin	Signal	Pin	Signal
7	-	8	-
9	GND		

Table 4.11: Connector Pinout, Rear Panel SER1

Pin	Signal	Pin	Signal
1	-	2	Received Data 0 / CAN_L
3	Transmitted Data 0 / CAN_GND	4	Received Data 1 / -
5	GND / -	6	Transmitted Data 1 / -
7	- / CAN_H	8	-
9	GND / -		

Configuring the serial ports for either RS-422 or RS-232 operation is accomplished via two jumpers, as described in Table 4.12.

Table 4.12: Serial Mode Jumpers, J2060/J2061 (SER0/SER1 MODE)

Setting	Description
Jumper on pins 1 and 2	Selects RS-422 mode.
Jumper on pins 2 and 3	Selects RS-232 mode.

4.4 Internal I/O Connectors

The XTend7100 has I/O available on the interior of the board near the PIM site. The connectors in this area consist of two vertical USB 2.0 connectors and three vertical SATA connectors. Refer to Section 3.4 for the location of these connectors.

4.4.1 USB Connectors

The XTend7100's on-board, internal, USB 2.0 ports are accessible via two, standard, Type A, USB connectors. Figure 4.6 shows the pin locations in the connector, and Table 4.13 lists the pinout.

Figure 4.6: USB Connectors

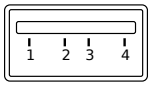


Table 4.13: Connector Pinout, Internal USB2/USB3

Pin	Signal
1	V_{CC} (current-limited +5 V USB power)
2	DATA#
3	DATA
4	GND

4.4.2 SATA Connectors

The XTend7100 includes three internal SATA connectors. Figure 4.7 shows the pin locations in the connector, and Table 4.14 lists the pinout.

Figure 4.7: SATA Connector

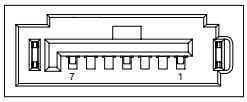


Table 4.14: Connector Pinout, Internal SATA0/SATA2/SATA3

Pin	Signal
1	GND
2	A+ (Transmit +)

Table 4.14: Connector Pinout, Internal SATA0/SATA2/SATA3 *(continued)*

Pin	Signal
3	A- (Transmit -)
4	GND
5	B- (Receive -)
6	B+ (Receive +)
7	GND

4.5 Other Jumpers

This section describes miscellaneous configuration jumpers located to the left of the CIM site (see Section 3.4).

Table 4.15: Memory Write-Protect Configuration Jumper, J2523 (NVMWP)

Setting	Description
Jumper on pins 1 and 2	Write-protect all non-volatile memory on the XTend7100. Also, indicate to the COM Express module and PMC/XMC sites to write-protect their memory.
Jumper on pins 2 and 3	Enable write access to all non-volatile memory on the XTend7100.

Table 4.16: Thermal Trip On/Off Jumper, J1860 (COM0 THRMTRP)

Setting	Description
Jumper on pins 1 and 2	COM0_THRMTRIP# signal output from the COM Express card causes a board-level reset while it is asserted.
Jumper on pins 2 and 3	COM0_THRMTRIP# does not cause a board-level reset when asserted.

Table 4.17: TPM On/Off Jumper, J2521 (COM0 TPM)

Setting	Description
Jumper on pins 1 and 2	Enable the COM Express Modules TPM.
Jumper on pins 2 and 3	Disable the COM Express Modules TPM.

4.6 Other Headers

Due to the large number of signals on the COM Express connector, some I/O and miscellaneous signals are routed to 0.1 in. headers on the printed circuit board. Most are located in the area between the COM Express module and the CIM site. (See component map in Section 3.4.)

4.6.1 Standby Block

The Standby block allows for access to the standby/sleep-related signals provided by the COM Express module. Please refer to your COM Express module's documentation for details regarding its support for these signals. Table 4.18 lists the header pinout.

Table 4.18: Connector Pinout, Standby Pin Block, J2500 (COM0 SBY)

Pin	Signal	Pin	Signal
1	+3.3V_SBY_F	2	COM0_SLEEP_PB# *
3	COM0_SUS_S3#	4	COM0_WDT
5	COM0_SUS_S4#	6	COM0_WAKE0#
7	COM0_SUS_S5#	8	COM0_WAKE1#
9	COM0_EXCD0_PERST#	10	COM0_EXCD0_CPPE#
11	COM0_EXCD1_PERST#	12	COM0_EXCD1_CPPE#
13	COM0_SUS_STAT#	14	GND

*De-bounced and stretched by 20 ms before being fed to COM0_SLEEP#.

4.6.2 LPC Block

The LPC block provides access to the LPC interrupt and DMA request signals on the COM Express AB connector. Refer to your COM Express module's documentation for details regarding its support for these signals. Table 4.19 lists the header pinout.

Table 4.19: Connector Pinout, LPC Pin Block, J2590 (COM0 LPC)

Pin	Signal
1	COM0_LPC_SERIRQ
2	COM0_LPC_DRQ0#
3	COM0_LPC_DRQ1#
4	GND

4.6.3 GPIO Block

The GPIO block allows for access to general-purpose input (GPI), general-purpose output (GPO), and several other signals provided by the COM Express module. Please refer to your COM Express module's documentation for details regarding its support for these signals. Table 4.20 lists the header pinout. The GPO signals also are connected to LEDs D2584-D2587 (see Section 3.7).

Table 4.20: Connector Pinout, GPIO Pin Block, J2570 (COM0 GPIO)

Pin	Signal	Pin	Signal
1	COM0_GPO0	2	COM0_GPI0
3	COM0_GPO1	4	COM0_GPI1
5	COM0_GPO2	6	COM0_GPI2
7	COM0_GPO3	8	COM0_GPI3
9	GND	10	COM0_EXT_INT0#
11	COM0_BATLOW#	12	COM0_EXT_INT1#
13	COM0_THRM#	14	GND

4.6.4 RTC Power / SMB Alert Header

The RTC Power / SMB Alert header allows for access to the VCC_RTC voltage and the ability to trigger an SMB alert. Table 4.21 lists the header pinout.

Note

Since VCC_RTC is sourced from the lithium battery, take care not to draw too much current from this pin.

Table 4.21: Connector Pinout, Power / SMB Alert Header, J2502

Pin	Signal
1	COM0_VCC_RTC_F
2	COM0_SMB_ALERT#
3	GND

4.7 COM Express Signals

See Table 4.22 for a list of signals present on the COM Express connectors.

Table 4.22: COM Express Signal Descriptions

Signal	Description
-	**No Connection.**
+12V_COM0	**12-Volt Power Rail.** Supplied from COM Express backplane.
+5V_SBY_COM0	**5-Volt Standby Power Rail.** Supplied from COM Express backplane.
CIM0_I2C*n*_SCL	**I²C Clock.** Serial clock for bus *n*. See Section 4.2 for connected devices.
CIM0_I2C*n*_SDA	**I²C Data.** Serial data for bus *n*. See Section 4.2 for connected devices.
COM0_AC/HDA	**AC97/High Definition Audio.**
COM0_BATLOW#	**Low Battery.** Indicates that the external battery is low.
COM0_CB_RESET#	**COM Express Carrier Reset.** Output from COM Express card. Causes carrier card reset.
COM0_DDI*n*	**Digital Display Interface Signals.** Refer to your COM Express module documentation for more information.
COM0_ETH*n*_ACT#	**Ethernet Activity.** Indicates Ethernet port *n* activity.
COM0_ETH*n*_CTREF	**Ethernet Center Tap.** Center-tap voltage for Ethernet port *n*.
COM0_ETH*n*_DA /COM0_ETH*n*_DA#	**Ethernet DA (10/100/1000BASE-T).** Port *n* bi-directional transmit and receive signals for 1000BASE-T operation. Transmit (output) for 10/100BASE-T operation.
COM0_ETH*n*_DB /COM0_ETH*n*_DB#	**Ethernet DB (10/100/1000BASE-T).** Port *n* bi-directional transmit and receive signals for 1000BASE-T operation. Receive (input) for 10/100BASE-T operation.
COM0_ETH*n*_DC /COM0_ETH*n*_DC#	**Ethernet DC (10/100/1000BASE-T).** Port *n* bi-directional transmit and receive signals for 1000BASE-T operation. Not used for 10/100BASE-T operation.

Table 4.22: COM Express Signal Descriptions *(continued)*

Signal	Description
COM0_ETH*n*_DD /COM0_ETH*n*_DD#	**Ethernet DD (10/100/1000BASE-T).** Port *n* bi-directional transmit and receive signals for 1000BASE-T operation. Not used for 10/100BASE-T operation.
COM0_ETH*n*_LINK#	**Ethernet Link.** Indicates Ethernet port *n* is linked.
COM0_ETH*n*_LINK100#	**Ethernet Link.** Indicates Ethernet port *n* is linked at 100 Mb/s.
COM0_ETH*n*_LINK1000#	**Ethernet Link.** Indicates Ethernet port *n* is linked at 1000 Mb/s.
COM0_EXCD*n*_	**Express Card.** Refer to your COM Express module documentation for more information.
COM0_EXT_INT*n*#	**External Interrupt.** External interrupt signal to COM Express module.
COM0_FAN_PWMOUT	**Control FAN0 Speed.** Not active in standard configurations. Contact X-ES for details.
COM0_FAN_TACHIN	**FAN0 Tachometer.** Not active in standard configurations. Contact X-ES for details.
COM0_GPI_*n*/COM0_GPO_*n*	**General Purpose Input / Output.** General purpose inputs/outputs to/from COM Express module.
COM0_LPC_CLK /COM0_LPC_FRAME# /COM0_LPC_SERIRQ /COM0_LPC_DRQ[1:0]# /COM0_LPC_AD[3:0]	**LPC.** Low Pin Count bus signals.
COM0_NVM_WP	**Non-Volatile Write Protect.** See Table 4.15.
COM0_PWRBTN#	**Power Button.** Brings module out of S5.
COM0_SATA*n*_RX /COM0_SATA*n*_RX#	**SATA Receive.** Receive signal for SATA port *n*.
COM0_SATA*n*_TX /COM0_SATA*n*_TX#	**SATA Transmit.** Transmit signal for SATA port *n*.
COM0_SATA_LED#	**SATA Activity.** Illuminates LED (D304) when SATA1 port is active.
COM0_SLEEP#	**Sleep Button.** Used to transition the module to and from sleep states.
COM0_SMB_ALERT#	**SMBus Alert.**
COM0_SPKR	**Speaker Output.**

Table 4.22: COM Express Signal Descriptions *(continued)*

Signal	Description
COM0_SUS_S*n*#	**Suspend State Indicator.** Indicates system is in suspense state *n*.
COM0_SUS_STAT*n*#	**Suspend Status.** Indicates imminent suspend operation.
COM0_SYS_RESET#	**COM Express Module Reset.** Input to COM Express card. Module will reset when low.
COM0_THRM#	**Over Temperature Situation.** Input to module to indicate an over temperature situation.
COM0_THRMTRIP#	**Thermal Trip.** Low indicates that the processor is over temperature. See Table 4.16.
COM0_TYPE*n*#	**Module Type Indicator.** Used to detect what type of COM Express module is installed.
COM0_USB*n*_D /COM0_USB*n*_D#	**USB Data.** Port *n* USB data.
COM0_USB*n*_*p*_OC#	**USB Over Current.** USB over-current status for ports *n* and *p*.
COM0_USB_SSRX[0:3] /COM0_USB_SSRX[0:3]#	**USB Super-Speed Receive.** Receive signal for USB 3.0 port *n*.
COM0_USB_SSTX[0:3] /COM0_USB_SSTX[0:3]#	**USB Super-Speed Transmit.** Transmit signal for USB 3.0 port *n*.
COM0_VCC_RTC	**RTC Power.** Real-time clock supply voltage for COM Express module.
COM0_VGA_HSYNC /COM0_VGA_VSYNC	**VGA Synchronization Signals.** Horizontal and vertical synchronization signals.
COM0_VGA_I2C_DAT /COM0_VGA_I2C_CK	**VGA I²C Interface.** I²C bus, used to auto-sense display settings.
COM0_VGA_RED /COM0_VGA_GREEN /COM0_VGA__BLUE	**VGA Pixel Data.** Red/green/blue pixel data.
COM0_WAKE*n*#	**Wake-Up Signals.** PCI Express and general purpose wake-up signal.
COM0_WDT	**Watchdog.** Indicates that a watchdog time-out event has occurred.
COM0_[A:D]*n*	**Miscellaneous.** Pin implementation varies based on configuration. Contact X-ES for details.
GND	**Digital Ground.**

Table 4.22: COM Express Signal Descriptions *(continued)*

Signal	Description
PE_COM0TOBR0_[0:3] /PE_BR0TOCOM0_[0:3]	**PCI Express Bridge Interface.** PCI Express lanes to/from the PCIe bridge.
PE_COM0TOCIM0_[0:7] /PE_CIM0TOCOM0_[0:7]	**PCI Express CIM Interface.** PCI Express lanes to/from the CIM expansion slot.
PE_COM0TOEC0_[0:7] /PE_EC0TOCOM0_[0:7]	**PCI Express Edge Card Interface.** PCI Express lanes routed to/from the edge card connector.
PE_COM0TOXMC0_[0:7] /PE_XMC0TOCOM0_[0:7]	**PCI Express XMC Interface.** PCI Express lanes to/from the XMC J15 connector.
PE_COM0_CLK_REF /PE_COM0_CLK_REF#	**PCIe Reference Clock.** Provided by the COM Express card and buffered to the other PCIe devices on the XTend7100 (PCIe-to-PCI bridge, PCIe switch, XMC site, and edge card site).
PWR_OK	**Power OK.** XTend7100 asserts PWR_OK when +12 V, +5 V, and +3.3 V supplies have been stable for about 90 ms.

4.8 COM Express Connectors

The XTend7100 utilizes two 220-pin socket connectors, P300 (AB) and P400 (CD), to implement the COM Express interface. Please refer to Section 3.4 for the location of these connectors on the XTend7100 printed circuit board. See the *PICMG COM Express Specification* for detailed signal descriptions.

Table 4.23: Connector Pinout, P300 (COM0 AB)

Pin	Signal	Pin	Signal
A1	GND	B1	GND
A2	COM0_ETH0_TRD3	B2	COM0_ETH0_ACT#
A3	COM0_ETH0_TRD3#	B3	COM0_LPC_FRAME#
A4	COM0_ETH0_LINK100#	B4	COM0_LPC_AD0
A5	COM0_ETH0_LINK1000#	B5	COM0_LPC_AD1
A6	COM0_ETH0_TRD2#	B6	COM0_LPC_AD2
A7	COM0_ETH0_TRD2	B7	COM0_LPC_AD3
A8	COM0_ETH0_LINK#	B8	COM0_LPC_DRQ0#
A9	COM0_ETH0_TRD1#	B9	COM0_LPC_DRQ1#

Table 4.23: Connector Pinout, P300 (COM0 AB) *(continued)*

Pin	Signal	Pin	Signal
A10	COM0_ETH0_TRD1	B10	COM0_LPC_CLK
A11	GND	B11	GND
A12	COM0_ETH0_TRD0#	B12	COM0_PWRBTN#
A13	COM0_ETH0_TRD0	B13	COM0_SMB_CK
A14	COM0_ETH0_CTREF	B14	COM0_SMB_DAT
A15	COM0_SUS_S3#	B15	COM0_SMB_ALERT#
A16	COM0_SATA0_TX	B16	COM0_SATA1_TX
A17	COM0_SATA0_TX#	B17	COM0_SATA1_TX#
A18	COM0_SUS_S4#	B18	COM0_SUS_STAT#
A19	COM0_SATA0_RX	B19	COM0_SATA1_RX
A20	COM0_SATA0_RX#	B20	COM0_SATA1_RX#
A21	GND	B21	GND
A22	COM0_SATA2_TX	B22	COM0_SATA3_TX
A23	COM0_SATA2_TX#	B23	COM0_SATA3_TX#
A24	COM0_SUS_S5#	B24	PWR_OK
A25	COM0_SATA2_RX	B25	COM0_SATA3_RX
A26	COM0_SATA2_RX#	B26	COM0_SATA3_RX#
A27	COM0_BATLOW#	B27	COM0_WDT
A28	COM0_SATA_LED#	B28	COM0_AC/HDA_SDIN2
A29	COM0_AC/HDA_SYNC	B29	COM0_AC/HDA_SDIN1
A30	COM0_AC/HDA_RST#	B30	COM0_AC/HDA_SDIN0
A31	GND	B31	GND
A32	COM0_AC/HDA_BITCLK	B32	COM0_SPKR
A33	COM0_AC/HDA_SDOUT	B33	COM0_I2C_CK
A34	COM0_PRG_SPI_EN#	B34	COM0_I2C_DAT
A35	COM0_THRMTRIP#	B35	COM0_THRM#
A36	COM0_USB6_D#	B36	COM0_USB7_D#
A37	COM0_USB6_D	B37	COM0_USB7_D
A38	COM0_USB_6_7_OC#	B38	COM0_USB_4_5_OC#

Table 4.23: Connector Pinout, P300 (COM0 AB) *(continued)*

Pin	Signal	Pin	Signal
A39	COM0_USB4_D#	B39	COM0_USB5_D#
A40	COM0_USB4_D	B40	COM0_USB5_D
A41	GND	B41	GND
A42	COM0_USB2_D#	B42	COM0_USB3_D#
A43	COM0_USB2_D	B43	COM0_USB3_D
A44	COM0_USB_2_3_OC#	B44	COM0_USB_0_1_OC#
A45	COM0_USB0_D#	B45	COM0_USB1_D#
A46	COM0_USB0_D	B46	COM0_USB1_D
A47	COM0_VCC_RTC	B47	COM0_EXCD1_PERST#
A48	COM0_EXCD0_PERST#	B48	COM0_EXCD1_CPPE#
A49	COM0_EXCD0_CPPE#	B49	COM0_SYS_RESET#
A50	COM0_LPC_SERIRQ	B50	COM0_CB_RESET#
A51	GND	B51	GND
A52	PE_COM0TOCIM0_1	B52	PE_CIM0TOCOM0_1
A53	PE_COM0TOCIM0_1#	B53	PE_CIM0TOCOM0_1#
A54	COM0_GPI_0	B54	COM0_GPO_1
A55	PE_COM0TOCIM0_0	B55	PE_CIM0TOCOM0_0
A56	PE_COM0TOCIM0_0#	B56	PE_CIM0TOCOM0_0#
A57	GND	B57	COM0_GPO_2
A58	PE_COM0TOBR0_3	B58	PE_BR0TOCOM0_3
A59	PE_COM0TOBR0_3#	B59	PE_BR0TOCOM0_3#
A60	GND	B60	GND
A61	PE_COM0TOBR0_2	B61	PE_BR0TOCOM0_2
A62	PE_COM0TOBR0_2#	B62	PE_BR0TOCOM0_2#
A63	COM0_GPI_1	B63	COM0_GPO_3
A64	PE_COM0TOBR0_1	B64	PE_BR0TOCOM0_1
A65	PE_COM0TOBR0_1#	B65	PE_BR0TOCOM0_1#
A66	GND	B66	COM0_WAKE0#
A67	COM0_GPI_2	B67	COM0_WAKE1#

Table 4.23: Connector Pinout, P300 (COM0 AB) *(continued)*

Pin	Signal	Pin	Signal
A68	PE_COM0TOBR0_0	B68	PE_BR0TOCOM0_0
A69	PE_COM0TOBR0_0#	B69	PE_BR0TOCOM0_0#
A70	GND	B70	GND
A71	COM0_SATA5_TX	B71	COM0_SATA4_TX
A72	COM0_SATA5_TX#	B72	COM0_SATA4_TX#
A73	COM0_A73	B73	COM0_B73
A74	COM0_A74	B74	COM0_B74
A75	COM0_SATA5_RX	B75	COM0_SATA4_RX
A76	COM0_SATA5_RX#	B76	COM0_SATA4_RX#
A77	COM0_ETH1_LINK100#	B77	COM0_ETH1_TRD3#
A78	COM0_ETH1_TRD1#	B78	COM0_ETH1_TRD3
A79	COM0_ETH1_TRD1	B79	COM0_ETH1_LINK#
A80	GND	B80	GND
A81	COM0_ETH1_TRD0#	B81	COM0_ETH1_TRD2#
A82	COM0_ETH1_TRD0	B82	COM0_ETH1_TRD2
A83	COM0_ETH1_LINK1000#	B83	COM0_ETH1_CTREF
A84	COM0_ETH1_ACT#	B84	+5V_SBY_COM0
A85	COM0_GPI_3	B85	+5V_SBY_COM0
A86	COM0_EXT_INT1#	B86	+5V_SBY_COM0
A87	COM0_EXT_INT0#	B87	+5V_SBY_COM0
A88	PE_COM0_CLK_REF	B88	COM0_PRG_SPI_CS1#
A89	PE_COM0_CLK_REF#	B89	COM0_VGA_RED
A90	GND	B90	GND
A91	COM0_PRG_SPI_PWR	B91	COM0_VGA_GREEN
A92	COM0_PRG_SPI_MISO	B92	COM0_VGA_BLUE
A93	COM0_GPO_0	B93	COM0_VGA_HSYNC
A94	COM0_PRG_SPI_CLK	B94	COM0_VGA_VSYNC
A95	COM0_PRG_SPI_MOSI	B95	COM0_VGA_I2C_CK
A96	COM0_TPM_PP	B96	COM0_VGA_I2C_DAT

Table 4.23: Connector Pinout, P300 (COM0 AB) *(continued)*

Pin	Signal	Pin	Signal
A97	COM0_TYPE10#	B97	COM0_PRG_SPI_CS0#
A98	COM0_SER0_TX	B98	COM0_B98
A99	COM0_SER0_RX	B99	COM0_B99
A100	GND	B100	GND
A101	COM0_SER1_TX	B101	COM0_FAN_PWMOUT
A102	COM0_SER1_RX	B102	COM0_FAN_TACHIN
A103	COM0_NVM_WP	B103	COM0_SLEEP#
A104	+12V_COM0	B104	+12V_COM0
A105	+12V_COM0	B105	+12V_COM0
A106	+12V_COM0	B106	+12V_COM0
A107	+12V_COM0	B107	+12V_COM0
A108	+12V_COM0	B108	+12V_COM0
A109	+12V_COM0	B109	+12V_COM0
A110	GND	B110	GND

Table 4.24: Connector Pinout, P400 (COM0 CD)

Pin	Signal	Pin	Signal
C1	GND	D1	GND
C2	GND	D2	GND
C3	COM0_USB_SSRX0#	D3	COM0_USB_SSTX0#
C4	COM0_USB_SSRX0	D4	COM0_USB_SSTX0
C5	GND	D5	GND
C6	COM0_USB_SSRX1#	D6	COM0_USB_SSTX1#
C7	COM0_USB_SSRX1	D7	COM0_USB_SSTX1
C8	GND	D8	GND
C9	COM0_USB_SSRX2#	D9	COM0_USB_SSTX2#
C10	COM0_USB_SSRX2	D10	COM0_USB_SSTX2
C11	GND	D11	GND
C12	COM0_USB_SSRX3#	D12	COM0_USB_SSTX3#

Table 4.24: Connector Pinout, P400 (COM0 CD) *(continued)*

Pin	Signal	Pin	Signal
C13	COM0_USB_SSRX3	D13	COM0_USB_SSTX3
C14	GND	D14	GND
C15	COM0_DDI1_6	D15	COM0_DDI1_CTRLCLK_AUX
C16	COM0_DDI1_6#	D16	COM0_DDI1_CTRLDATA_AUX#
C17	COM0_C17	D17	COM0_D17
C18	COM0_C18	D18	COM0_D18
C19	PE_CIM0TOCOM0_2	D19	PE_COM0TOCIM0_2
C20	PE_CIM0TOCOM0_2#	D20	PE_COM0TOCIM0_2#
C21	GND	D21	GND
C22	PE_CIM0TOCOM0_3	D22	PE_COM0TOCIM0_3
C23	PE_CIM0TOCOM0_3#	D23	PE_COM0TOCIM0_3#
C24	COM0_DDI1_HPD	D24	COM0_D24
C25	COM0_DDI1_4	D25	COM0_D25
C26	COM0_DDI1_4#	D26	COM0_DDI1_0
C27	COM0_C27	D27	COM0_DDI1_0#
C28	COM0_C28	D28	COM0_D28
C29	COM0_DDI1_5	D29	COM0_DDI1_1
C30	COM0_DDI1_5#	D30	COM0_DDI1_1#
C31	GND	D31	GND
C32	COM0_DDI2_CTRLCLK_AUX	D32	COM0_DDI1_2
C33	COM0_DDI2_CTRLDATA_AUX#	D33	COM0_DDI1_2#
C34	COM0_DDI2_DDC_AUX_SEL	D34	COM0_DDI1_DDC_AUX_SEL
C35	COM0_C35	D35	COM0_D35
C36	COM0_DDI3_CTRLCLK_AUX	D36	COM0_DDI1_3
C37	COM0_DDI3_CTRLDATA_AUX#	D37	COM0_DDI1_3#
C38	COM0_DDI3_DDC_AUX_SEL	D38	COM0_D38
C39	COM0_DDI3_0	D39	COM0_DDI2_0
C40	COM0_DDI3_0#	D40	COM0_DDI2_0#
C41	GND	D41	GND

Table 4.24: Connector Pinout, P400 (COM0 CD) *(continued)*

Pin	Signal	Pin	Signal
C42	COM0_DDI3_1	D42	COM0_DDI2_1
C43	COM0_DDI3_1#	D43	COM0_DDI2_1#
C44	COM0_DDI3_HPD	D44	COM0_DDI2_HPD
C45	COM0_C45	D45	COM0_D45
C46	COM0_DDI3_2	D46	COM0_DDI2_2
C47	COM0_DDI3_2#	D47	COM0_DDI2_2#
C48	COM0_C48	D48	COM0_D48
C49	COM0_DDI3_3	D49	COM0_DDI2_3
C50	COM0_DDI3_3#	D50	COM0_DDI2_3#
C51	GND	D51	GND
C52	PE_XMC0TOCOM0_0	D52	PE_COM0TOXMC0_0
C53	PE_XMC0TOCOM0_0#	D53	PE_COM0TOXMC0_0#
C54	COM0_TYPE0#	D54	COM0_PEG_LANE_RV#
C55	PE_XMC0TOCOM0_1	D55	PE_COM0TOXMC0_1
C56	PE_XMC0TOCOM0_1#	D56	PE_COM0TOXMC0_1#
C57	COM0_TYPE1#	D57	COM0_TYPE2#
C58	PE_XMC0TOCOM0_2	D58	PE_COM0TOXMC0_2
C59	PE_XMC0TOCOM0_2#	D59	PE_COM0TOXMC0_2#
C60	GND	D60	GND
C61	PE_XMC0TOCOM0_3	D61	PE_COM0TOXMC0_3
C62	PE_XMC0TOCOM0_3#	D62	PE_COM0TOXMC0_3#
C63	COM0_C63	D63	COM0_D63
C64	COM0_C64	D64	COM0_D64
C65	PE_XMC0TOCOM0_4	D65	PE_COM0TOXMC0_4
C66	PE_XMC0TOCOM0_4#	D66	PE_COM0TOXMC0_4#
C67	COM0_C67	D67	GND
C68	PE_XMC0TOCOM0_5	D68	PE_COM0TOXMC0_5
C69	PE_XMC0TOCOM0_5#	D69	PE_COM0TOXMC0_5#
C70	GND	D70	GND

Table 4.24: Connector Pinout, P400 (COM0 CD) *(continued)*

Pin	Signal	Pin	Signal
C71	PE_XMC0TOCOM0_6	D71	PE_COM0TOXMC0_6
C72	PE_XMC0TOCOM0_6#	D72	PE_COM0TOXMC0_6#
C73	GND	D73	GND
C74	PE_XMC0TOCOM0_7	D74	PE_COM0TOXMC0_7
C75	PE_XMC0TOCOM0_7#	D75	PE_COM0TOXMC0_7#
C76	GND	D76	GND
C77	COM0_C77	D77	COM0_D77
C78	PE_EC0TOCOM0_0	D78	PE_COM0TOEC0_0
C79	PE_EC0TOCOM0_0#	D79	PE_COM0TOEC0_0#
C80	GND	D80	GND
C81	PE_EC0TOCOM0_1	D81	PE_COM0TOEC0_1
C82	PE_EC0TOCOM0_1#	D82	PE_COM0TOEC0_1#
C83	COM0_C83	D83	COM0_D83
C84	GND	D84	GND
C85	PE_EC0TOCOM0_2	D85	PE_COM0TOEC0_2
C86	PE_EC0TOCOM0_2#	D86	PE_COM0TOEC0_2#
C87	GND	D87	GND
C88	PE_EC0TOCOM0_3	D88	PE_COM0TOEC0_3
C89	PE_EC0TOCOM0_3#	D89	PE_COM0TOEC0_3#
C90	GND	D90	GND
C91	PE_EC0TOCOM0_4	D91	PE_COM0TOEC0_4
C92	PE_EC0TOCOM0_4#	D92	PE_COM0TOEC0_4#
C93	GND	D93	GND
C94	PE_EC0TOCOM0_5	D94	PE_COM0TOEC0_5
C95	PE_EC0TOCOM0_5#	D95	PE_COM0TOEC0_5#
C96	GND	D96	GND
C97	COM0_C97	D97	COM0_D97
C98	PE_EC0TOCOM0_6	D98	PE_COM0TOEC0_6
C99	PE_EC0TOCOM0_6#	D99	PE_COM0TOEC0_6#

Table 4.24: Connector Pinout, P400 (COM0 CD) *(continued)*

Pin	Signal	Pin	Signal
C100	GND	D100	GND
C101	PE_EC0TOCOM0_7	D101	PE_COM0TOEC0_7
C102	PE_EC0TOCOM0_7#	D102	PE_COM0TOEC0_7#
C103	GND	D103	GND
C104	+12V_COM0	D104	+12V_COM0
C105	+12V_COM0	D105	+12V_COM0
C106	+12V_COM0	D106	+12V_COM0
C107	+12V_COM0	D107	+12V_COM0
C108	+12V_COM0	D108	+12V_COM0
C109	+12V_COM0	D109	+12V_COM0
C110	GND	D110	GND

4.9 CIM Support

Table 4.25: Connector Pinout, P700 (CIM0)

Pin	Signal	Pin	Signal
A1	GND	B1	GND
A2	COM0_ETH1_TRD3#	B2	-
A3	COM0_ETH1_TRD3	B3	-
A4	COM0_ETH1_TRD2#	B4	-
A5	COM0_ETH1_TRD2	B5	-
A6	COM0_ETH1_TRD1#	B6	-
A7	COM0_ETH1_TRD1	B7	-
A8	COM0_ETH1_TRD0#	B8	-
A9	COM0_ETH1_TRD0	B9	-
A10	COM0_ETH1_CTREF	B10	-
A11	GND	B11	GND
A12	COM0_USB_SSRX0#	B12	COM0_USB_SSTX0#
A13	COM0_USB_SSRX0	B13	COM0_USB_SSTX0

Table 4.25: Connector Pinout, P700 (CIM0) *(continued)*

Pin	Signal	Pin	Signal
A14	GND	B14	GND
A15	COM0_USB_SSRX1#	B15	COM0_USB_SSTX1#
A16	COM0_USB_SSRX1	B16	COM0_USB_SSTX1
A17	GND	B17	GND
A18	COM0_USB_SSRX2#	B18	COM0_USB_SSTX2#
A19	COM0_USB_SSRX2	B19	COM0_USB_SSTX2
A20	GND	B20	GND
A21	COM0_USB_SSRX3#	B21	COM0_USB_SSTX3#
A22	COM0_USB_SSRX3	B22	COM0_USB_SSTX3
A23	GND	B23	GND
A24	COM0_USB6_D#	B24	COM0_USB7_D#
A25	COM0_USB6_D	B25	COM0_USB7_D
A26	COM0_USB_6_7_OC#	B26	COM0_USB_2_3_OC#
A27	COM0_USB2_D#	B27	COM0_USB3_D#
A28	COM0_USB2_D	B28	COM0_USB3_D
A29	GND	B29	GND
A30	COM0_AC/HDA_SYNC	B30	COM0_AC/HDA_SDIN2
A31	COM0_AC/HDA_RST#	B31	COM0_AC/HDA_SDIN1
A32	COM0_AC/HDA_BITCLK	B32	COM0_AC/HDA_SDIN0
A33	COM0_AC/HDA_SDOUT	B33	COM0_SPKR
A34	COM0_I2C_CK	B34	COM0_SMB_CK
A35	COM0_I2C_DAT	B35	COM0_SMB_DAT
A36	+3.3V_AUX_CIM0	B36	COM0_SMB_ALERT#
A37	COM0_LPC_SERIRQ	B37	COM0_C48
A38	COM0_D38	B38	COM0_D45
A39	COM0_D48	B39	COM0_C45
A40	GND	B40	GND
A41	COM0_DDI2_CTRLCLK_AUX	B41	COM0_DDI3_CTRLCLK_AUX
A42	COM0_DDI2_CTRLDATA_AUX#	B42	COM0_DDI3_CTRLDATA_AUX#

Table 4.25: Connector Pinout, P700 (CIM0) *(continued)*

Pin	Signal	Pin	Signal
A43	GND	B43	GND
A44	COM0_DDI2_0	B44	COM0_DDI3_0
A45	COM0_DDI2_0#	B45	COM0_DDI3_0#
A46	GND	B46	GND
A47	COM0_DDI2_1	B47	COM0_DDI3_1
A48	COM0_DDI2_1#	B48	COM0_DDI3_1#
A49	COM0_DDI2_HPD	B49	COM0_DDI3_HPD
A50	COM0_DDI2_2	B50	COM0_DDI3_2
A51	COM0_DDI2_2#	B51	COM0_DDI3_2#
A52	COM0_DDI2_DDC_AUX_SEL	B52	COM0_DDI3_DDC_AUX_SEL
A53	COM0_DDI2_3	B53	COM0_DDI3_3
A54	COM0_DDI2_3#	B54	COM0_DDI3_3#
A55	GND	B55	GND
A56	COM0_SATA5_TX	B56	COM0_SATA4_TX
A57	COM0_SATA5_TX#	B57	COM0_SATA4_TX#
A58	GND	B58	GND
A59	COM0_SATA5_RX	B59	COM0_SATA4_RX
A60	COM0_SATA5_RX#	B60	COM0_SATA4_RX#
A61	COM0_A73	B61	COM0_B73
A62	COM0_A74	B62	COM0_B74
A63	-	B63	COM0_C67
A64	COM0_C17	B64	COM0_C77
A65	COM0_C18	B65	COM0_D17
A66	GND	B66	GND
A67	COM0_DDI1_6	B67	COM0_D35
A68	COM0_DDI1_6#	B68	COM0_D77
A69	COM0_C35	B69	COM0_D18
A70	COM0_D28	B70	CB_RESET#
A71	GND	B71	GND

Table 4.25: Connector Pinout, P700 (CIM0) *(continued)*

Pin	Signal	Pin	Signal
A72	CIM0_REFCLK	B72	SYS_RESET_CIM0#
A73	CIM0_REFCLK#	B73	COM0_NVM_WP
A74	GND	B74	GND
A75	PE_CIM0TOCOM0_0	B75	PE_COM0TOCIM0_0
A76	PE_CIM0TOCOM0_0#	B76	PE_COM0TOCIM0_0#
A77	GND	B77	GND
A78	PE_CIM0TOCOM0_1	B78	PE_COM0TOCIM0_1
A79	PE_CIM0TOCOM0_1#	B79	PE_COM0TOCIM0_1#
A80	GND	B80	GND
A81	PE_CIM0TOCOM0_2	B81	PE_COM0TOCIM0_2
A82	PE_CIM0TOCOM0_2#	B82	PE_COM0TOCIM0_2#
A83	GND	B83	GND
A84	PE_CIM0TOCOM0_3	B84	PE_COM0TOCIM0_3
A85	PE_CIM0TOCOM0_3#	B85	PE_COM0TOCIM0_3#
A86	GND	B86	GND
A87	COM0_C27	B87	COM0_D24
A88	COM0_C28	B88	COM0_D25
A89	GND	B89	GND
A90	COM0_C63	B90	COM0_D63
A91	COM0_C64	B91	COM0_D64
A92	GND	B92	GND
A93	-	B93	-
A94	-	B94	-
A95	GND	B95	GND
A96	-	B96	COM0_B98
A97	-	B97	COM0_B99
A98	GND	B98	GND
A99	COM0_DDI1_4	B99	COM0_DDI1_5
A100	COM0_DDI1_4#	B100	COM0_DDI1_5#

Table 4.25: Connector Pinout, P700 (CIM0) *(continued)*

Pin	Signal	Pin	Signal
A101	GND	B101	GND
A102	COM0_LPC_FRAME#	B102	COM0_LPC_AD0
A103	COM0_LPC_DRQ0#	B103	COM0_LPC_AD1
A104	GND	B104	GND
A105	COM0_C83	B105	COM0_D83
A106	COM0_C97	B106	COM0_D97
A107	GND	B107	GND
A108	COM0_LPC_DRQ1#	B108	COM0_LPC_AD2
A109	COM0_LPC_CLK	B109	COM0_LPC_AD3
A110	GND	B110	GND
A111	COM0_VGA_RED	B111	COM0_VGA_HSYNC
A112	COM0_VGA_GREEN	B112	COM0_VGA_VSYNC
A113	COM0_VGA_BLUE	B113	COM0_VGA_I2C_CK
A114	GND	B114	COM0_VGA_I2C_DAT
A115	+3.3V	B115	GND
A116	+3.3V	B116	+3.3V
A117	GND	B117	GND
A118	+12V	B118	+12V
A119	+12V	B119	+12V
A120	GND	B120	GND

PMC Interface

The XTend7100 provides a single PMC site, designated as PMC0. This is an implementation of the electrical PCI bus on the Common Mezzanine Card (CMC) standard (IEEE 1386.1) with the addition of the Processor PMC (PrPMC) extension specified in VITA 32.

5.1 PMC V(I/O)

Due to legacy concerns with older PCI silicon, the IEEE 1386.1 specification provides dedicated bus signaling voltage pins, designated V(I/O). These pins are either connected to +3.3 V or +5 V on the PMC carrier card.

> **Important**
>
> **The XTend7100 factory configuration only supports +3.3 V V(I/O).**

5.2 PrPMC Monarch Support

The PMC standard was originally intended for peripheral I/O cards without CPUs. In this configuration, a CPU on the PMC carrier card would enumerate the "non-intelligent" PMC modules and perform PCI interrupt handling, utilizing the PMCs as peripheral devices. There eventually became a desire to place CPUs on the PMC modules themselves. This led to the notion of a PrPMC, or Processor PMC. With the advent of PrPMCs, there also came a desire to allow the PrPMC itself to handle bus enumeration and interrupt handling. In this configuration, the CPU could essentially be moved from the carrier card to the PrPMC. A PrPMC which performs PCI Enumeration and Interrupt handling on the bus it is attached to is known as a Monarch PMC. A PrPMC which acts as a peripheral device is known as a non-Monarch PMC.

By default, the XTend7100 supports one non-Monarch PMC site. PrPMCs will automatically detect whether they are Monarch or not by sampling the state of the MONARCH# pin (J12.64). For information on configuring the PMC site as a Monarch, please contact X-ES.

5.3 PCI Arbitration, Clocking, and Reset

The XTend7100's PEX8114 PCIe-to-PCI bridge device handles arbitration, clocking, and reset propagation to the PMC site. The PCI bus mode (PCI or PCI-X) and clock frequency is determined by three jumpers, located on the front side of the XTend7100 printed circuit board (see Section 3.4). These jumpers allow for various modes of operation, ranging from 33 MHz PCI to 133 MHz PCI-X. Table 5.1 describes the jumper settings.

Table 5.1: PCI Mode Jumper Settings

Mode	Rate	Jumper Settings		
		J4301 (M66EN)	J4302 (PCIXCAP)	J4315 (SEL100)
PCI	33 MHz	Pins 1 and 2 connected	Pins 1 and 2 connected	Pins 1 and 2 connected
PCI	66 MHz	Pins 2 and 3 connected	Pins 1 and 2 connected	Pins 1 and 2 connected
PCI-X	66 MHz *	Pins 2 and 3 connected	Pins 2 and 3 connected	Pins 1 and 2 connected
PCI-X	100 MHz	Pins 2 and 3 connected	Removed (no conn.)	Pins 2 and 3 connected
PCI-X	133 MHz	Pins 2 and 3 connected	Removed (no conn.)	Pins 1 and 2 connected

*This is the default (recommended) setting. When a PMC is installed that does not support PCI-X or can only operate at 33 MHz, the PEX8114 will auto-negotiate the link to the fastest capable PCI rate.

5.4 IDSEL Assignments

PMC0's IDSEL and IDSELB are connected to PCI AD17 and AD21, respectively. These assignments determine the PCI device number on the PCI bus, as seen from OS software.

5.5 Interrupt Twisting

The PMC site shares four interrupt nets on XTend7100. These are denoted as INTA#, INTB#, INTC#, and INTD#. On the XTend7100, all four interrupt lines connect to the PEX8114 bridge. Per the PCI Specification, the interrupts on the motherboard (XTend7100) are not simply connected to their corresponding pin on J11 of the PMC connectors; rather, they are distributed depending on the slot number. OS Software must take this "twisting" into account when assigning interrupt vectors on PrPMCs. Table 5.2 shows the connectivity.

Table 5.2: XTend7100 Interrupt Mapping

PMC0 Interrupt	PEX8114 Interrupt
INTA#	INTB#
INTB#	INTC#

Table 5.2: XTend7100 Interrupt Mapping *(continued)*

PMC0 Interrupt	PEX8114 Interrupt
INTC#	INTD#
INTD#	INTA#

5.6 PMC Signals

See Table 5.3 for a list of signals present on the PMC connectors.

Table 5.3: PMC Signal Descriptions

Signal	Description
-	**No Connection.**
+3.3V	**3.3-Volt Power Rail.** Supplied from PMC backplane.
+5V	**5-Volt Power Rail.** Supplied from PMC backplane.
+12V	**12-Volt Power Rail.** Supplied from PMC backplane.
-12V	**–12-Volt Power Rail.** Supplied from the XTend7100's on-card power supply.
GND	**Digital Ground.**
AD[31:0]	**PCI Address/Data Bus.** The PCI address/data bus consists of 32 signals used as inputs and outputs for address/data handling.
AD[63:32]	**PCI Address/Data Bus.** Upper 32 bits of the PCI address/data bus used as inputs and outputs for address/data handling.
C/BE[3:0]#	**Command/Byte Enables.** During the address phase, these signals define bus commands and signify which byte lanes are carrying meaningful data.
C/BE[7:4]#	**Command/Byte Enables.** Command- and byte-enable signals for the upper 32 bits of the address/data bus.
CLK*n*	**Clock.** This is an input signal, which provides timing for all PCI transactions.
INT[D:A]#	**Interrupts.** These are PCI interrupt lines.
DEVSEL#	**Device Select.** Indicates that a device on the bus has decoded the current address and has been selected as the target of the access.
FRAME#	**Frame.** Indicates the initiation and final data phase of a bus transaction.

Table 5.3: PMC Signal Descriptions *(continued)*

Signal	Description
IDSEL/IDSELB	**Initialization Device Select.** This is an input signal, acting as a chip-select during configuration read and write transactions.
IRDY#	**Initiator Ready.** Indicates that this PCI controller, acting as a PCI master, can complete the current data phase of a PCI transaction.
LOCK#	**Lock.** Indicates that an atomic operation to a bridge may require multiple transactions to complete.
PAR	**Parity.** Indicates odd parity across AD[31:0] and C/BE[3:0] when asserted during address and data phases.
PERR#	**Parity Error.** This signal is asserted when a parity error is detected on the bus.
PRESENT#	**Present.** Indicates to the host, when grounded, that the PMC module is installed.
REQ#/REQB#	**Request.** Indicates that an agent is requesting control of the PCI bus to perform a transaction.
GNT#/GNTB#	**Grant.** Indicates that an agent has been granted control of the PCI bus.
REQ64#/ACK64#	**Request/Acknowledge 64-Bit Transaction.** Indicates a request or acknowledge to perform a 64-bit transaction.
RST#	**Reset.** When asserted, resets the module.
SERR#	**System Error.** The system error signal indicates that an address parity error, a target-abort, or some other system error has occurred.
STOP#	**Stop.** The stop signal requests that the initiator stop the current transaction.
TRDY#	**Target Ready.** Indicates the target is ready to accept a transaction.
PCIXCAP#	**PCI-X Capability.** Indicates if modules are capable of PCI-X operation and, if so, at what frequency. Conventional cards connect this pin to ground. PCI-X 66 MHz cards connect this pin to ground through a 10K-ohm resistor. PCI-X 133 MHz cards leave this connection open.
M66EN	**66 MHz Enable.** When logic high, indicates a 66 MHz bus.

Table 5.3: PMC Signal Descriptions *(continued)*

Signal	Description
MONARCH#	**PCI Monarch.** When connected to GND, this signal indicates that the XTend7100 is to provide local PCI bus enumeration and interrupt handling. When open, it indicates that the XTend7100 acts as a PCI peripheral and does not provide local PCI bus enumeration and interrupt handling.
EREADY	**Ready for Enumeration.** This signal is an output for non-Monarch modules and an input for Monarch modules. EREADY indicates that all modules on the PCI are ready to be enumerated. EREADY is connected to the GPIO driver.
PUP/PDN	**Bus Mode Signals.** Indicates to the XTend7100 that the installed mezzanine shall be identified as PMC.
TRST#/TCK/TMS /TDI/TDO	**JTAG.** PMC interface JTAG signals.

5.7 PMC Connectors

Table 5.4: Connector Pinout, J11 (PMC0)

Pin	Signal	Pin	Signal
1	TCK	2	-12V
3	GND	4	INTB#
5	INTC#	6	INTD#
7	PRESENT#	8	+5V
9	INTA#	10	-
11	GND	12	-
13	CLK	14	GND
15	GND	16	GNT1#
17	REQ1#	18	+5V
19	+3.3V	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21

Table 5.4: Connector Pinout, J11 (PMC0) *(continued)*

Pin	Signal	Pin	Signal
29	AD19	30	+5V
31	+3.3V	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	PCIXCAP#	40	LOCK#
41	-	42	-
43	PAR	44	GND
45	+3.3V	46	AD15
47	AD12	48	AD11
49	AD9	50	+5V
51	GND	52	C/BE0#
53	AD6	54	AD5
55	AD4	56	GND
57	+3.3V	58	AD3
59	AD2	60	AD1
61	AD0	62	+5V
63	GND	64	REQ64#

Table 5.5: Connector Pinout, J12 (PMC0)

Pin	Signal	Pin	Signal
1	+12V	2	TRST#
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	-
9	-	10	-
11	PUP1	12	+3.3V
13	RST#	14	PDN1_1
15	+3.3V	16	PDN1_2

Table 5.5: Connector Pinout, J12 (PMC0) *(continued)*

Pin	Signal	Pin	Signal
17	-	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3V
25	AD17	26	AD23
27	+3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	AD21
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	M66EN	48	AD10
49	AD8	50	+3.3V
51	AD7	52	REQ5#
53	+3.3V	54	GNT5#
56	GND	58	EREADY
59	GND	60	RESETOUT#
61	ACK64#	62	+3.3V
63	GND	64	MONARCH#

Table 5.6: Connector Pinout, J13 (PMC0)

Pin	Signal	Pin	Signal
1	-	2	GND
3	GND	4	C/BE7#
5	C/BE6#	6	C/BE5#

Table 5.6: Connector Pinout, J13 (PMC0) *(continued)*

Pin	Signal	Pin	Signal
7	C/BE4#	8	GND
9	+3.3V	10	PAR64
11	AD63	12	AD62
13	AD61	14	GND
15	GND	16	AD60
17	AD59	18	AD58
19	AD57	20	GND
21	+3.3V	22	AD56
23	AD55	24	AD54
25	AD53	26	GND
27	GND	28	AD52
29	AD51	30	AD50
31	AD49	32	GND
33	GND	34	AD48
35	AD47	36	AD46
37	AD45	38	GND
39	+3.3V	40	AD44
41	AD43	42	AD42
43	AD41	44	GND
45	GND	46	AD40
47	AD39	48	AD38
49	AD37	50	GND
51	GND	52	AD36
53	AD35	54	AD34
55	AD33	56	GND
57	+3.3V	58	AD32
59	-	60	-
61	-	62	GND
63	GND	64	-

5.8 PIM Support

The PMC standard provides a dedicated connector for user-definable I/O. This is denoted as J14 (PMC0) on the carrier card. As indicated in the following pin assignment tables, the J14 connector at the PMC site is directly connected to similar pins on the J34 connector of the PCI I/O Module (PIM) site. This is designated as PIM0, which corresponds to PMC0's J14 I/O.

The PIM site allows for a plug-on mezzanine card that can be installed to provide I/O connectors for the PMC site. Examples of such mezzanines are X-ES's XIt2020 and XIt2040 PIMs. Consult the appropriate PMC module User's Manual for details regarding an appropriate PIM.

The PIM site also has another connector, J30, to provide power if active devices are required on the PIM. Table 5.8 describes the pinout for this connector.

Table 5.7: Connector Pinout, J14/J34 (PMC0/PIM0)

Pin	Signal	Pin	Signal
1	J14_P1	2	J14_P2
3	J14_P3	4	J14_P4
5	J14_P5	6	J14_P6
7	J14_P7	8	J14_P8
9	J14_P9	10	J14_P10
11	J14_P11	12	J14_P12
13	J14_P13	14	J14_P14
15	J14_P15	16	J14_P16
17	J14_P17	18	J14_P18
19	J14_P19	20	J14_P20
21	J14_P21	22	J14_P22
23	J14_P23	24	J14_P24
25	J14_P25	26	J14_P26
27	J14_P27	28	J14_P28
29	J14_P29	30	J14_P30
31	J14_P31	32	J14_P32
33	J14_P33	34	J14_P34
35	J14_P35	36	J14_P36
37	J14_P37	38	J14_P38
39	J14_P39	40	J14_P40

Table 5.7: Connector Pinout, J14/J34 (PMC0/PIM0) *(continued)*

Pin	Signal	Pin	Signal
41	J14_P41	42	J14_P42
43	J14_P43	44	J14_P44
45	J14_P45	46	J14_P46
47	J14_P47	48	J14_P48
49	J14_P49	50	J14_P50
51	J14_P51	52	J14_P52
53	J14_P53	54	J14_P54
55	J14_P55	56	J14_P56
57	J14_P57	58	J14_P58
59	J14_P59	60	J14_P60
61	J14_P61	62	J14_P62
63	J14_P63	64	J14_P64

Table 5.8: Connector Pinout, J30 (PIM0)

Pin	Signal	Pin	Signal
1	-	2	+12V
3	-	4	-
5	+5V	6	-
7	-	8	-
9	-	10	+3.3V
11	-	12	-
13	GND	14	-
15	-	16	-
17	-	18	GND
19	-	20	-
21	+5V	22	-
23	-	24	-
25	-	26	+3.3V
27	-	28	-

Table 5.8: Connector Pinout, J30 (PIM0) *(continued)*

Pin	Signal	Pin	Signal
29	GND	30	-
31	-	32	-
33	-	34	GND
35	-	36	-
37	+5V	38	-
39	-	40	-
41	-	42	+3.3V
43	-	44	-
45	GND	46	-
47	-	48	-
49	-	50	GND
51	-	52	-
53	+5V	54	-
55	-	56	-
57	-	58	+3.3V
59	-	60	-
61	-12V	62	-
63	-	64	-

XMC Interface

The XTend7100 provides one XMC site per the VITA 42 standard. This site is designated as XMC0. VITA 42 is an extension of the CMC (IEEE 1386, Common Mezzanine Card) specification and adds two new connectors, J15 and J16, for high-speed differential I/O capability to/from the carrier card.

The basic interface is implemented as a direct connect between transmit/receive pairs on XMC0 and transmit/receive pairs on the COM Express CD connector. The interconnect supports x8, x4, x2, and x1 links, as well as 20 pairs and 38 single-ended I/O signals through J16 back to the XIM site. A 100 MHz differential reference clock (denoted by REFCLK+ and REFCLK-) with appropriate termination is provided to the XMC site for bus standards such as PCI Express.

6.1 XMC VPWR Voltage

VITA 42 specifies variable power pins (VPWR) for XMCs. These power pins can either be connected to +5 V or +12 V on the carrier card. The XTend7100 allows for either of these voltages to be connected to the XMC connector. By default, the VPWR pins are connected to 5 V on XTend7100. Please contact X-ES for details regarding the 12 V configuration.

6.2 XMC0 Root Capability

For point-to-point PCI Express connectivity, one point must be a root complex, and one must be an endpoint. By default, XMC0 is configured as an endpoint. Please contact X-ES for details regarding the configuration of the XMC site as a root complex.

6.3 XMC Signals

Table 6.1 describes the signals present on the XMC connectors.

Table 6.1: XMC Signal Descriptions

Signal	Description
-	**No Connection.**
VPWR	**Power.** Main power supply rail. VPWR may be supplied with +12 V or +5 V. The default +5 V power supplied from the XTend7100.
+3.3V	**3.3-Volt Power Rail.** Supplied from XMC backplane.
+12V	**12-Volt Power Rail.** Supplied from XMC backplane.
-12V	**−12-Volt Power Rail.** Supplied from the XTend7100's on-card power supply.
+3.3V_AUX	**3.3-Volt Auxiliary Power Rail.** Supplied from XMC backplane.
GND	**Digital Ground.**
PE_COM0TOXMC0_[0:*x*] /PE_COM0TOXMC0_[0:*x*]#	**PCI Express Transmit.** PCI Express transmit data from the XTend7100 carrier to the mezzanine card for lanes 0 through *x*.
PE_XMC0TOCOM0_[0:*x*] /PE_XMC0TOCOM0_[0:*x*]#	**PCI Express Receive.** PCI Express receive data from the mezzanine card to the XTend7100 carrier for lanes 0 through *x*.
REFCLK/REFCLK#	**PCI Express Reference Clock.** 100 MHz reference clock driven from the XTend7100 to the XMC module (HCSL signaling level).
ROOT#	**PCI Express Root.** Driven low by the XTend7100 to indicate the XMC should operate in root complex mode, or high to indicate endpoint mode.
WAKE#	**PCI Express Wake.** Open drain signal driven by the XMC to the XTend7100. It signals the XTend7100 to reactivate the PCI Express link's main power rails and reference clocks.
MVMRO	**XMC Non-Volatile Memory Read Only.** Driven to the XMC to prevent any non-volatile storage on the XMC from being written when asserted high.

Table 6.1: XMC Signal Descriptions *(continued)*

Signal	Description
MPRESENT#	**XMC Module Present.** This signal allows the XTend7100 to determine whether an XMC is present. The XMC module ties this signal to ground.
MRSTI#	**XMC Reset In.** Driven low by the XTend7100 to reset the XMC module.
MRSTO#	**XMC Reset Out.** Driven by the XMC to provide a reset input to the XTend7100.
MSCL	**I²C Serial Clock.** Driven by the XTend7100 as a clock reference for the I²C interface. This is the same I²C bus that all local devices are connected to.
MSDA	**I²C Serial Data.** Bi-directional signal used as a data line for the I²C interface between the XTend7100 and the hosted XMC. This is the same I²C bus that all local devices are connected to.
TRST#/TCK/TMS/TDI/TDO	**JTAG.** XMC interface JTAG signals.

6.4 XMC Connectors

Table 6.2: Connector Pinout, J15 (XMC0)

Pin	A	B	C	D	E	F
1	PE_XMC0TOCOM0_0	PE_XMC0TOCOM0_0#	+3.3V	PE_XMC0TOCOM0_1	PE_XMC0TOCOM0_1#	VPWR
2	GND	GND	TRST#	GND	GND	RST#
3	PE_XMC0TOCOM0_2	PE_XMC0TOCOM0_2#	+3.3V	PE_XMC0TOCOM0_3	PE_XMC0TOCOM0_3#	VPWR
4	GND	GND	TCK	GND	GND	RSTO#
5	PE_XMC0TOCOM0_4	PE_XMC0TOCOM0_4#	+3.3V_MC0	PE_XMC0TOCOM0_5	PE_XMC0TOCOM0_5#	VPWR
6	GND	GND	TMS	GND	GND	+12V_MC0
7	PE_XMC0TOCOM0_6	PE_XMC0TOCOM0_6#	+3.3V_MC0	PE_XMC0TOCOM0_7	PE_XMC0TOCOM0_7#	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	-	-	-	-	-	VPWR
10	GND	GND	TDO	GND	GND	GND
11	PE_COM0TOXMC0_0	PE_COM0TOXMC0_0#	BIST#	PE_COM0TOXMC0_1	PE_COM0TOXMC0_1#	VPWR
12	GND	GND	GND	GND	GND	PRESENT#
13	PE_COM0TOXMC0_2	PE_COM0TOXMC0_2#	+3.3V_AUX_XMC0	PE_COM0TOXMC0_3	PE_COM0TOXMC0_3#	VPWR
14	GND	GND	GND	GND	GND	I2C_SDA

Table 6.2: Connector Pinout, J15 (XMC0) *(continued)*

Pin	A	B	C	D	E	F
15	PE_COM0TOXMC0_4	PE_COM0TOXMC0_4#	-	PE_COM0TOXMC0_5	PE_COM0TOXMC0_5#	VPWR
16	GND	GND	MVMR0	GND	GND	I2C_SCL
17	PE_COM0TOXMC0_6	PE_COM0TOXMC0_6#	-	PE_COM0TOXMC0_7	PE_COM0TOXMC0_7#	-
18	GND	GND	-	GND	GND	-
19	REFCLK	REFCLK#	-	WAKE#	ROOT0#	-

6.5 XIM Support

The XTend7100 provides access to signals from the XMC connectors at the XIM site.

Table 6.3: Connector Pinout, J16/J36 (XMC0/XIM0)

Pin	A	B	C	D	E	F
1	J16_A1	J16_B1	J16_C1	J16_D1	J16_E1	J16_F1
2	GND	GND	J16_C2	GND	GND	J16_F2
3	J16_A3	J16_B3	J16_C3	J16_D3	J16_E3	J16_F3
4	GND	GND	J16_C4	GND	GND	J16_F4
5	J16_A5	J16_B5	J16_C5	J16_D5	J16_E5	J16_F5
6	GND	GND	J16_C6	GND	GND	J16_F6
7	J16_A7	J16_B7	J16_C7	J16_D7	J16_E7	J16_F7
8	GND	GND	J16_C8	GND	GND	J16_F8
9	J16_A9	J16_B9	J16_C9	J16_D9	J16_E9	J16_F9
10	GND	GND	J16_C10	GND	GND	J16_F10
11	J16_A11	J16_B11	J16_C11	J16_D11	J16_E11	J16_F11
12	GND	GND	J16_C12	GND	GND	J16_F12
13	J16_A13	J16_B13	J16_C13	J16_D13	J16_E13	J16_F13
14	GND	GND	J16_C14	GND	GND	J16_F14
15	J16_A15	J16_B15	J16_C15	J16_D15	J16_E15	J16_F15
16	GND	GND	J16_C16	GND	GND	J16_F16
17	J16_A17	J16_B17	J16_C17	J16_D17	J16_E17	J16_F17
18	GND	GND	J16_C18	GND	GND	J16_F18
19	J16_A19	J16_B19	J16_C19	J16_D19	J16_E19	J16_F19

Table 6.4: Connector Pinout, J35 (XIM0)

Pin	A	B	C	D	E	F
1	-	-	+3.3V	-	-	XIM0_VPWR
2	GND	GND	-	GND	GND	-
3	-	-	+3.3V	-	-	XIM0_VPWR
4	GND	GND	-	GND	GND	-
5	-	-	+3.3V	-	-	XIM0_VPWR
6	GND	GND	-	GND	GND	+12V
7	-	-	+3.3V	-	-	XIM0_VPWR
8	GND	GND	-	GND	GND	-12V
9	-	-	-	-	-	XIM0_VPWR
10	GND	GND	-	GND	GND	-
11	-	-	-	-	-	XIM0_VPWR
12	GND	GND	-	GND	GND	-
13	-	-	+3.3V_AUX_XIM0	-	-	XIM0_VPWR
14	GND	GND	-	GND	GND	-
15	-	-	-	-	-	XIM0_VPWR
16	GND	GND	-	GND	GND	-
17	-	-	-	-	-	-
18	GND	GND	-	GND	GND	-
19	-	-	-	-	-	-

Edge Card Interface

The XTend7100 provides a x8 PCI Express (PCIe) edge card slot that can host various I/O or development cards. It features an open-ended design that can accommodate PCIe edge cards of almost any size.

7.1 Edge Card Signals

See Table 7.1 for a list of signals present on the PCIe edge card connector.

Table 7.1: Edge Card Signal Descriptions

Signal	Description
-	**No Connection.**
+3.3V	**3.3-Volt Power Rail.**
+3.3V_AUX	**3.3-Volt Auxiliary Power Rail.**
+5V	**5-Volt Power Rail.**
+12V	**12-Volt Power Rail.**
GND	**Digital Ground.**
REFCLK/REFCLK#	**PCI Express Reference Clock.** 100 MHZ reference clock driven from the COM Express REFCLK output. This is a buffered version of the one generated by the COM Express card.
PE_EC0TOCOM0_[0:7] /PE_EC0TOCOM0_[0:7]#	**PCI Express Transmit.** PCI Express transmit data from the XTend7100 carrier to the edge card for lanes 0 through 7.
PE_COM0TOEC0_[0:7] /PE_COM0TOEC0_[0:7]#	**PCI Express Receive.** PCI Express receive data from the edge card to XTend7100 carrier for lanes 0 through 7.
PERST#	**Reset.** When asserted low, indicates to the PCIe edge card that a PCI Express reset has occurred.

Table 7.1: Edge Card Signal Descriptions *(continued)*

Signal	Description
I2C_SDA	**I²C Data.** Common data line for the XTend7100's local I²C bus.
I2C_SCL	**I²C Clock.** Common clock for the XTend7100's local I²C bus.
PRESENT#	**PCIe Edge Card Present.** Used by the JTAG circuitry to determine if a PCIe edge card is installed.
TRST#/TCK/TMS /TDI/TDO	**JTAG.** XMC interface JTAG signals.

7.2 Edge Card Connector

Table 7.2: Connector Pinout, J2400 (EC0)

Pin	Signal	Pin	Signal
A1	EC0_PRSNT1#	B1	+12V
A2	+12V	B2	+12V
A3	+12V	B3	+12V
A4	GND	B4	GND
A5	TCK	B5	I2C_SCL
A6	TDI	B6	I2C_SDA
A7	TDO	B7	GND
A8	TMS	B8	+3.3V
A9	+3.3V	B9	TRST#
A10	+3.3V	B10	+3.3V_AUX
A11	PERST#	B11	-
A12	GND	B12	-
A13	REFCLK	B13	GND
A14	REFCLK#	B14	PE_COM0TOEC0_0
A15	GND	B15	PE_COM0TOEC0_0#
A16	PE_EC0TOCOM0_0	B16	GND
A17	PE_EC0TOCOM0_0#	B17	PRESENT#
A18	GND	B18	GND

Table 7.2: Connector Pinout, J2400 (EC0) *(continued)*

Pin	Signal	Pin	Signal
A19	-	B19	PE_COM0TOEC0_1
A20	GND	B20	PE_COM0TOEC0_1#
A21	PE_EC0TOCOM0_1	B21	GND
A22	PE_EC0TOCOM0_1#	B22	GND
A23	GND	B23	PE_COM0TOEC0_2
A24	GND	B24	PE_COM0TOEC0_2#
A25	PE_EC0TOCOM0_2	B25	GND
A26	PE_EC0TOCOM0_2#	B26	GND
A27	GND	B27	PE_COM0TOEC0_3
A28	GND	B28	PE_COM0TOEC0_3#
A29	PE_EC0TOCOM0_3	B29	GND
A30	PE_EC0TOCOM0_3#	B30	-
A31	GND	B31	PRESENT#
A32	-	B32	GND
A33	-	B33	PE_COM0TOEC0_4
A34	GND	B34	PE_COM0TOEC0_4#
A35	PE_EC0TOCOM0_4	B35	GND
A36	PE_EC0TOCOM0_4#	B36	GND
A37	GND	B37	PE_COM0TOEC0_5
A38	GND	B38	PE_COM0TOEC0_5#
A39	PE_EC0TOCOM0_5	B39	GND
A40	PE_EC0TOCOM0_5#	B40	GND
A41	GND	B41	PE_COM0TOEC0_6
A42	GND	B42	PE_COM0TOEC0_6#
A43	PE_EC0TOCOM0_6	B43	GND
A44	PE_EC0TOCOM0_6#	B44	GND
A45	GND	B45	PE_COM0TOEC0_7
A46	GND	B46	PE_COM0TOEC0_7#
A47	PE_EC0TOCOM0_7	B47	GND

Table 7.2: Connector Pinout, J2400 (EC0) *(continued)*

Pin	Signal	Pin	Signal
A48	PE_EC0TOCOM0_7#	B48	PRESENT#
A49	GND	B49	GND

Power Measurement

The XTend7100 can determine power consumption for the PMC/XMC and COM Express sites. This is accomplished through the use of six separate INA219B devices, which measure the input voltages for these sites. The INA219B is a high-side current and voltage monitor that can provide real-time power measurements for the processor card via the I²C bus.

Note

X-ES has written a Linux bash script that configures and polls the INA219B devices. Please contact X-ES for details.

Alternatively, the XTend7100 provides test points (see component map in Section 3.4, yellow highlights) that all allow for measuring the voltage drop across a shunt resistor to determine power consumption. Since these test points are not at the kelvin connections to the sense resistors, readings may not be entirely accurate.

Table 8.1: Power Measurement Devices

I²C Bus	Address	Description	Shunt Resistance
1	0x40	12 V COM Express input current	10 mΩ
1	0x41	5 V COM Express standby input current	50 mΩ
1	0x42	3.3 V standby current (from all payload sites)	50 mΩ
1	0x43	12 V PMC/XMC input current	10 mΩ
1	0x44	5 V PMC/XMC input current	10 mΩ
1	0x45	3.3 V PMC/XMC input current	10 mΩ

JTAG

The XTend7100 provides a JTAG interface that allows for debug access to the PCIe-to-PCI bridge, PCIe switch, PMC/XMC sites, and PCIe edge card site.

Note

Since the COM Express specification does not include JTAG, the XTend7100's COM Express site cannot be accessed through its JTAG interface. Please consult your COM Express module's user documentation for details regarding available test interfaces.

Table 9.1 shows the JTAG header pins, which follow the ASSET InterTech boundary scan pod pinout. See the component map in Section 3.4 for the location of J3500.

Table 9.1: Connector Pinout, JTAG Header, J3500

Pin	Signal	Pin	Signal
1	TMS	2	TRST#
3	TDI	4	GND
5	10 kΩ pull-up to 3.3 V	6	pin removed
7	TDO	8	GND
9	-	10	GND
11	TCK	12	GND
13	-	14	-

The XTend7100 has three jumpers (see Section 3.4) that determine the configuration for the JTAG interface, as shown in Table 9.2.

Table 9.2: JTAG Configuration Jumpers

Ref. Des.	Label	Jumper Positions	Description
J3510	BP	n/a	Factory use only
J3511	CHAIN	ON = pins 1 and 2 connected; OFF = pins 2 and 3 connected	Include/exclude internal JTAG chain
J3512	MC0/EC0	ON = pins 1 and 2 connected; OFF = pins 2 and 3 connected	Include/exclude PMC/XMC and edge card sites in chain

Figure 9.1: JTAG Chain with J3511 and J3512 Set OFF

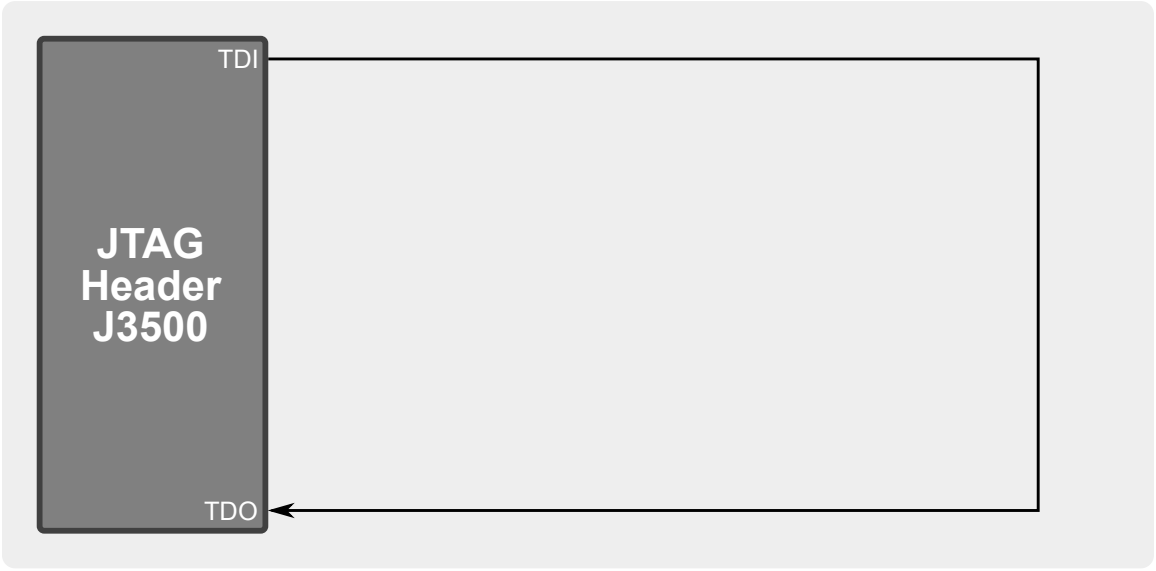


Figure 9.2: JTAG Chain with J3511 Set ON and J3512 Set OFF

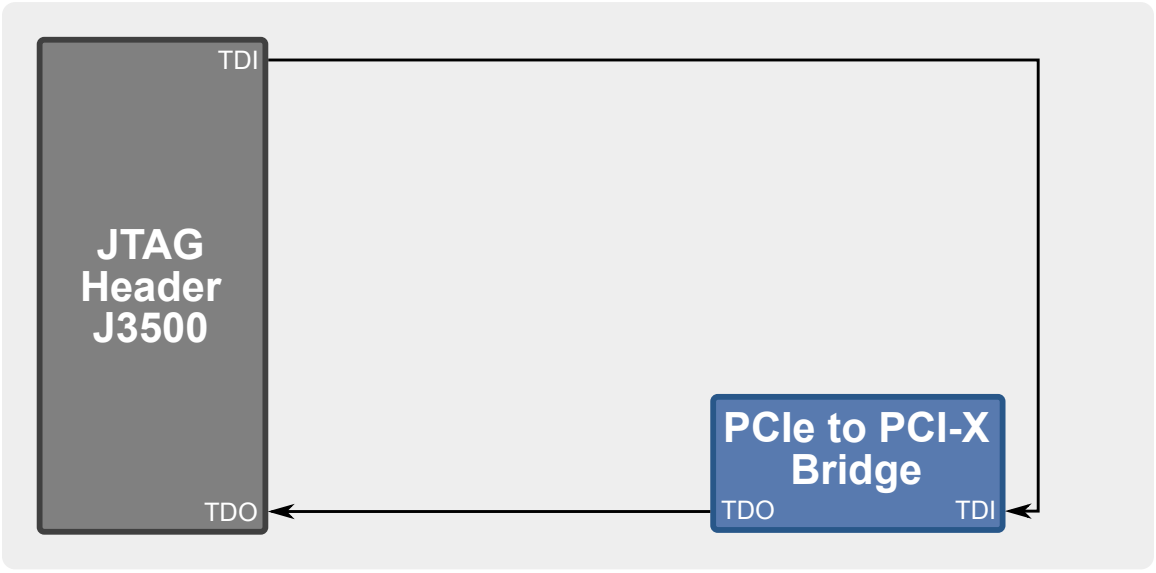


Figure 9.3: JTAG Chain with J3511 Set OFF and J3512 Set ON

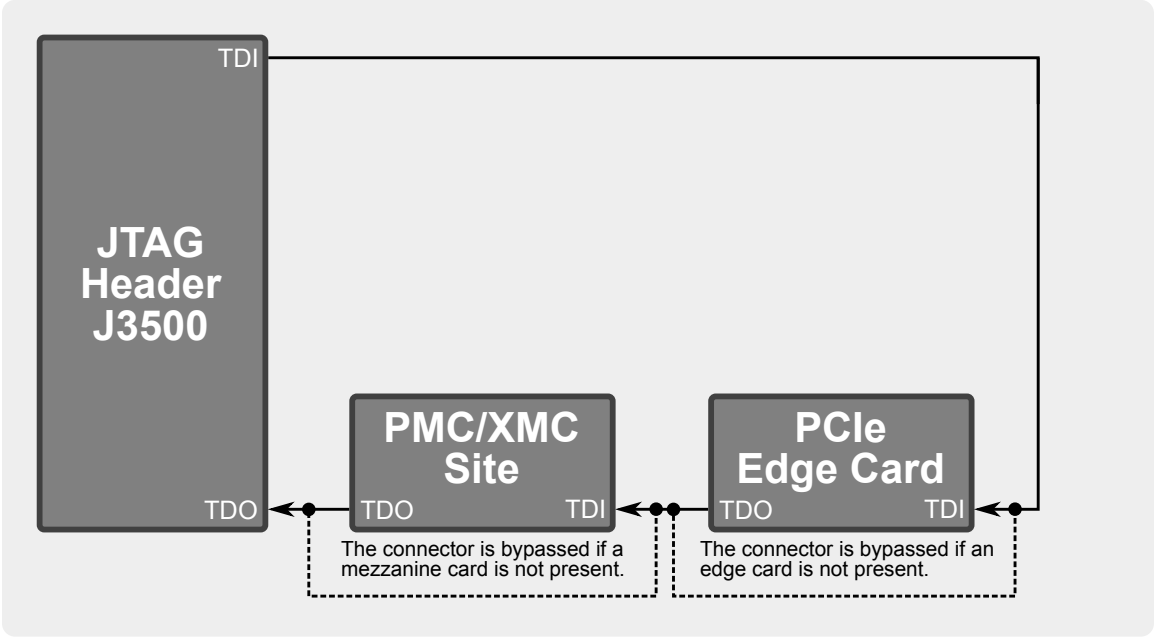
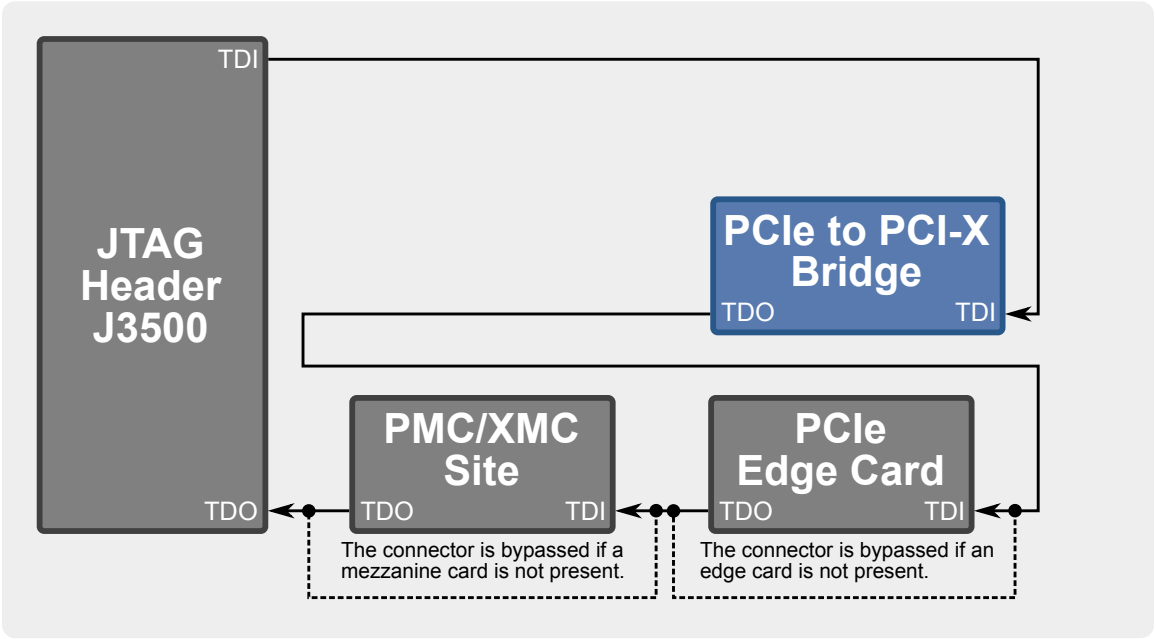


Figure 9.4: JTAG Chain with J3511 and J3512 Set ON



XTend7100 User's Manual

Rev. A

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