XPort5005

XMC Form Factor PCI Express Mini Card Carrier

XPort5005 User's Manual

Revision A

X-ES
Extreme Engineering Solutions

...Always Fast

Extreme Engineering Solutions
3225 Deming Way, Suite 120 • Middleton, WI 53562
Phone: 608.833.1155 • Fax: 608.827.6171
sales@xes-inc.com • http://www.xes-inc.com

XPort5005 User's Manual

Revision History

Revision	Date	Remark
A	August 2, 2013	Initial creation

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Safety Information

ESD Warning

Before handling any product described in this manual, please remember that electrostatic discharge (ESD) can easily damage electrical components and potentially result in product failure. The installer must be properly grounded at all times, else static charge will accumulate and may cause ESD damage.

Please adhere to the following guidelines to ensure the safety of your product:

- **Handle the product only when absolutely necessary.**
- **When handling the product, wear a grounding wrist strap at all times.**
- **Hold the product only by its edges. Do not touch any electrical components on the printed circuit board (PCB).**
- **Place the product only on a grounded ESD-dissipative mat. Simply placing the product on a static-shielding bag offers little to no ESD protection.**
- **Never place the product on metal or other conductive surfaces.**
- **If possible, store the product in an ESD-safe bag or clamshell when it is not in use.**

Manual Conventions

The following typographical and syntactical conventions are used throughout this manual:

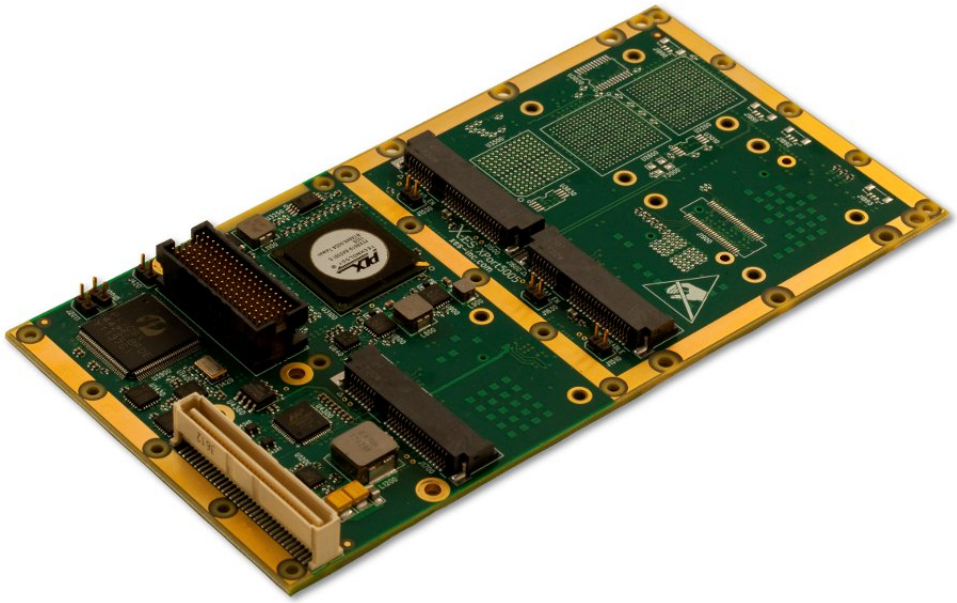
`0x0`	This notation denotes a hexadecimal number.
`0b0`	This notation denotes a binary number.
#	When used as a postfix, this notation denotes an Active Low Signal (e.g., RESET#). It is also used to indicate the negative half of a signal pair (e.g., RX/RX# or TX/TX#).
-	This notation denotes an unused (unconnected) pin.

Overview

The XPort5005 is an XMC module that can be quickly configured to support a platform's specific I/O or storage needs. The XPort5005 allows system integrators to reduce the total cost, complexity, and time to market for supporting the varying I/O and storage requirements of different platforms by enabling rapid support for MIL-STD-1553, CAN bus, ARINC 429, GPS, IEEE 1394 (FireWire), Solid-State Drives (SSD), AES-256 encryption, GPIO, WLAN (Wi-Fi), WiMax, Cellular (4G/LTE and 3G), RS-232/422/485, Bluetooth, and more.

The XPort5005 offers a flexible solution for meeting current and future platform requirements. The XPort5005 can support up to two full height (F2/H1) Mini PCI Express or mSATA modules and one half-height (H1) Mini PCI Express module. The XPort5005 supports operational temperatures from -40C to +85C for conduction cooled applications and -40C to +70C for forced air cooled applications. The rugged XPort5005 design also provides for robust mounting of its Mini PCI Express modules, supporting the XPort5005's use within platforms with the most demanding of environmental requirements, including vehicle transportation, rail transportation, military, and aerospace applications.

Figure 1.1: XPort5005 Photo (90071400-1 Configuration)



1.1 Features

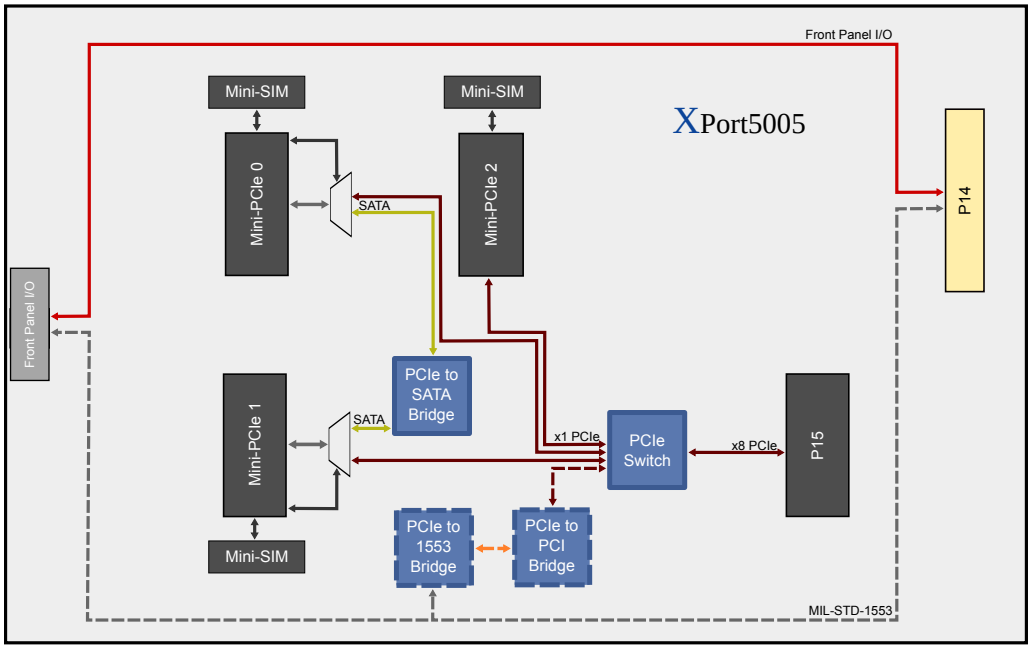
The following is a brief summary of the XPort5005's features:

- Up to two dual redundant channels of MIL-STD-1553
- Supports up to three Mini PCI Express cards
- Up to four CAN bus 2.0 interfaces
- Conduction- or air-cooled
- Supports two Full-Height Mini-PCIe modules or two mSATA modules
- Supports a single Half-Height Mini-PCIe module
- XMC PCIe interface
- Includes three mini-SIM card sockets
- Mini-PCIe CEM 2.0-compliant
- Each Mini-PCIe site supports PCIe
- Integration services with third-party modules available
- Conformal coating available

1.2 Block Diagram

Figure 1.2 provides a high-level overview of the XPort5005.

Figure 1.2: General Block Diagram



1.3 Available Accessories

Table 1.1 provides a list of X-ES accessories available for the XPort5005.

Table 1.1: Available Accessories

Part Number	Description
90071720-1	**XTend213.** Front panel I/O breakout card for the XPort5005

1.4 Available Software

Table 1.2 describes the various software solutions that X-ES offers for the XPort5005. Other operating systems may be supported by request; contact X-ES for more information.

Table 1.2: Available Software

Part Number	Description
90071400-101	**VxWorks Driver and BSP.** Support for Wind River VxWorks
90071400-103	**Linux BSP.** Support for Linux
90071400-107	**INTEGRITY BSP.** Support for Green Hills INTEGRITY
90071400-109	**QNX BSP.** Support for QNX Neutrino

1.5 Additional Information

Please refer to the documents listed within this section for additional information about the XPort5005 and its components that extends beyond the scope of this manual.

1.5.1 Standards

The technical information in this manual describes the unique features of the XPort5005. It is assumed that the reader has familiarity with the standard interfaces and devices incorporated into the XPort5005 that are not described in this manual.

Table 1.3 lists industry standards that apply to the XPort5005. Please see these documents for more information.

Table 1.3: Applicable Standards

Standard	Document	Author	Revision
PCI Express	*PCI Express Base Specification*	PCI-SIG	Revision 1.1
PCI Express Mini Card	*PCI Express Mini Card Electromechanical Specification*	PCI-SIG	Revision 2.0
VITA 20-2001	*Conduction Cooled PMC*	VITA	Ratified February 2005
VITA 42.0-2008	*XMC*	VITA	Ratified December 2008
VITA 42.3-2006	*XMC PCI Express Protocol Layer Standard*	VITA	Ratified June 2006

1.5.2 Other X-ES Documents

Table 1.4 lists additional documents that are available from X-ES. Contact X-ES to obtain any of these documents.

Table 1.4: Additional X-ES Documents

Document	Author
XPort5005 VxWorks Manual	X-ES
XPort5005 Linux Manual	X-ES

1.6 Basic Troubleshooting

In the event that the XPort5005 does not seem to be working properly, follow these troubleshooting steps:

1. Check that the XPort5005 is fully seated in the host card.
2. Check that all required power cables are connected.
3. Check that the power supply is supplying power at the correct voltages. If possible, use an oscilloscope to look for excessive power supply ripple or noise.
4. Check that any serial, I/O, or network cables in use are securely connected.
5. Check the status of the green SW0_PORT_GOOD 0 LED (see Section 2.4 for location). When lit or blinking, it indicates the XPort5005's on-board PCIe switch is linked to the host.
6. If the XPort5005 does not boot, check the status of the red Reset LED on the XPort5005. When lit, it indicates the XPort5005 is in reset.

1.7 Technical Support

The X-ES SupportNet web site at https://support.xes-inc.com allows registered users to access product information, documentation updates, software downloads, and technical support. X-ES customers can request login access by following the New User Sign-Up link.

If you have followed the entire troubleshooting procedure in Section 1.6 and are still experiencing problems getting the XPort5005 to work properly, contact X-ES using any of the following methods:

- SupportNet: https://support.xes-inc.com
- E-mail: <support@xes-inc.com>
- Phone: 608-833-1155

Before contacting X-ES support, please be prepared to supply the following information, where applicable:

- XPort5005 serial number

> **Tip**
>
> **To determine the serial number of your XPort5005, look for the white or light-green sticker attached to the PCB. The serial number will be the eight-digit number directly below the part number (90071400).**

- Backplane manufacturer and model number
- Manufacturer and model number of any other boards in the system, as applicable
- Any custom modifications to the XPort5005
- State of the red Reset LED (see Section 2.4), if the XPort5005 is not booting
- Serial console screen output of the error, if applicable

1.8 Service Information

If you need to return the XPort5005 to X-ES for service, please e-mail <support@xes-inc.com> or call 608-833-1155 and ask for a Return Merchandise Authorization (RMA) number. Be prepared to supply the XPort5005 serial number, the reason for return, and your original purchase order number.

When returning hardware that is out of warranty, billing information is required as well. Contact X-ES for any warranty-related questions.

When returning the XPort5005, be sure to enclose it in an anti-static bag or clamshell, such as the original shipping material. Send the XPort5005, pre-paid, to:

Extreme Engineering Solutions, Inc.
3225 Deming Way, Suite 120
Middleton, WI 53562
USA

Printed Circuit Board

This chapter provides detailed information about the XPort5005 printed circuit board (PCB). This information includes physical characteristics, power and environmental requirements, component maps, jumper definitions, and LED descriptions.

2.1 Physical Specifications

Table 2.1 describes the physical specifications of the XPort5005.

Table 2.1: Dimensions and Weight

Attribute	Value
Form Factor	XMC
Length	149 mm
Width	74 mm
Stacking Height	10 mm *
Weight (air-cooled) †	70 g
Weight (conduction-cooled) †	71 g

*With build options for 12 mm and 15 mm stacking heights

† Typical value without modules. Actual weight may vary according to specific product revision and configuration. Please contact X-ES for details.

2.2 Power Requirements

The XPort5005 requires +3.3-volt and VPWR XMC voltage rails to operate. VPWR may be +5 V or +12 V.

2.2.1 Power Sequencing

Module testing was performed under the following power sequencing requirements. Contact X-ES if your power requirements differ.

At all times: The VPWR DC level should be equal to or greater than the +3.3-volt DC level. The VPWR and +3.3-volt DC levels should not achieve a negative potential (below 0-volt DC potential).

During power-on: The maximum time between the VPWR and +3.3-volt DC outputs reaching minimum operating levels should be 20 ms. The VPWR and +3.3-volt DC levels should rise monotonically. These rise times should be greater than 1 ms and no greater than 30 ms, measured from when the voltages begin to be energized (above 0-volt DC potential) to when they reach their minimum operating levels.

During power-off: The maximum time between the VPWR and +3.3-volt DC levels falling below minimum operating levels should be 20 ms. The VPWR and +3.3-volt DC levels should fall monotonically. These fall times should be no greater than 30 ms, measured from when the voltages fall below their minimum operating levels to when they are completely de-energized (reach 0-volt DC potential).

2.2.2 Power Rail Requirements

The data in Table 2.2 was measured while operating under these testing conditions: (Please contact X-ES for details.).

Table 2.2: Power Requirements

Configuration	Power Requirements			
	3.3 V Rail	5.0 V Rail	VPWR Rail	Max. Power*
XMC, 5-volt	Contact X-ES			
XMC, 12-volt				

*Estimated power with all rails at nominal voltages ±5%.

The mezzanine card standard also specifies +12-volt and -12-volt power pins (separate from VPWR) that are located on the connector. These pins are not used by the XPort5005.

2.3 Environmental Requirements

The XPort5005 may be built to support use in either an air-cooled or conduction-cooled environment. Note that this section describes *all* the X-ES ruggedization levels. Please contact X-ES for specific information regarding the XPort5005.

The XPort5005's conformance to a particular level is determined by rigorous analysis and testing. All qualification testing may not be completed at the time of this writing. Specific product configurations may be required to meet high-temperature operational requirements for certain levels. The low temperature limits for certain products may be below the operating temperature limits defined by the manufacturers of components used within the product assembly. In conjunction with performing qualification testing at these lower levels, X-ES also screens every product that falls into this category to verify operation at these lower temperatures.

Please contact X-ES for the most current information regarding this product.

Caution

Do not use the XPort5005 in an environment other than its intended one without contacting X-ES first. For example, do not use a conduction-cooled board in an air-cooled chassis. Operating the XPort5005 in a chassis other than the intended one may cause the board to overheat and fail.

Level 1 ruggedization, described in Table 2.3, is for standard commercial applications.

Table 2.3: Standard Air-Cooled - Level 1

Category	Specification
Operating Temp.	0 to +55°C ambient, 300 LFM, per MIL-STD-810F Method 501.4 Procedure II and Method 502.4 Procedure II
Storage Temp.	-40 to +85°C ambient*
Operating Vibration	0.002 g²/Hz, 1 hour per axis from 5 to 2000 Hz
Operating Shock	20 g, 11 ms sawtooth, per MIL-STD-810F Method 516.5 Procedure I
Humidity	0 to 95% non-condensing, per MIL-STD-810F Method 507.4

*If the manufacturer's advertised storage temperature limit for any component used within this product does not meet these levels, these tests will be performed during qualification.

Level 3 ruggedization, described in Table 2.4, is for applications requiring an extended thermal range, as well as increased shock and vibration tolerances.

Note

Level 3 ruggedization requires special consideration at the system level. Contact X-ES to discuss specific environmental requirements for rugged air-cooled products.

Table 2.4: Rugged Air-Cooled - Level 3

Category	Specification
Operating Temp.	-40 to +70°C ambient, 600 LFM, per MIL-STD-810F Method 501.4 Procedure II and Method 502.4 Procedure II
Storage Temp.	-55 to +105°C ambient per MIL-STD-810F Method 501.4 Procedure I and Method 502.4 Procedure I*
Operating Vibration	0.04 g²/Hz (maximum), 1 hour per axis from 5 to 2000 Hz†
Operating Shock	30 g, 11 ms sawtooth, per MIL-STD-810F Method 516.5 Procedure I
Humidity	0 to 95% non-condensing, per MIL-STD-810F Method 507.4

*If the manufacturer's advertised storage temperature limit for any component used within this product does not meet these levels, these tests will be performed during qualification.

†5-100 Hz, PSD increasing at 3 dB/octave; 100-1000 Hz, PSD 0.04 g²/Hz; 1000-2000 Hz, PSD decreasing at 6 dB/octave

Level 5 ruggedization, described in Table 2.5, is for applications requiring an extended thermal range beyond that of the previous levels.

Table 2.5: Conduction-Cooled - Level 5

Category	Specification
Operating Temp.	-40 to +85°C board rail surface temperature, per MIL-STD-810F Method 501.4 Procedure II and Method 502.4 Procedure II
Storage Temp.	-55 to +105°C ambient per MIL-STD-810F Method 501.4 Procedure I and Method 502.4 Procedure I*
Operating Vibration	0.1 g²/Hz (maximum), 1 hour per axis from 5 to 2000 Hz†
Operating Shock	40 g, 11 ms sawtooth, per MIL-STD-810F Method 516.5 Procedure I
Humidity	0 to 95% non-condensing, per MIL-STD-810F Method 507.4

*If the manufacturer's advertised storage temperature limit for any component used within this product does not meet these levels, these tests will be performed during qualification.

†5-100 Hz, PSD increasing at 3 dB/octave; 100-1000 Hz, PSD 0.1 g²/Hz; 1000-2000 Hz, PSD decreasing at 6 dB/octave

2.4 Component Maps

Figure 2.1: Front Component Map (Revision A)

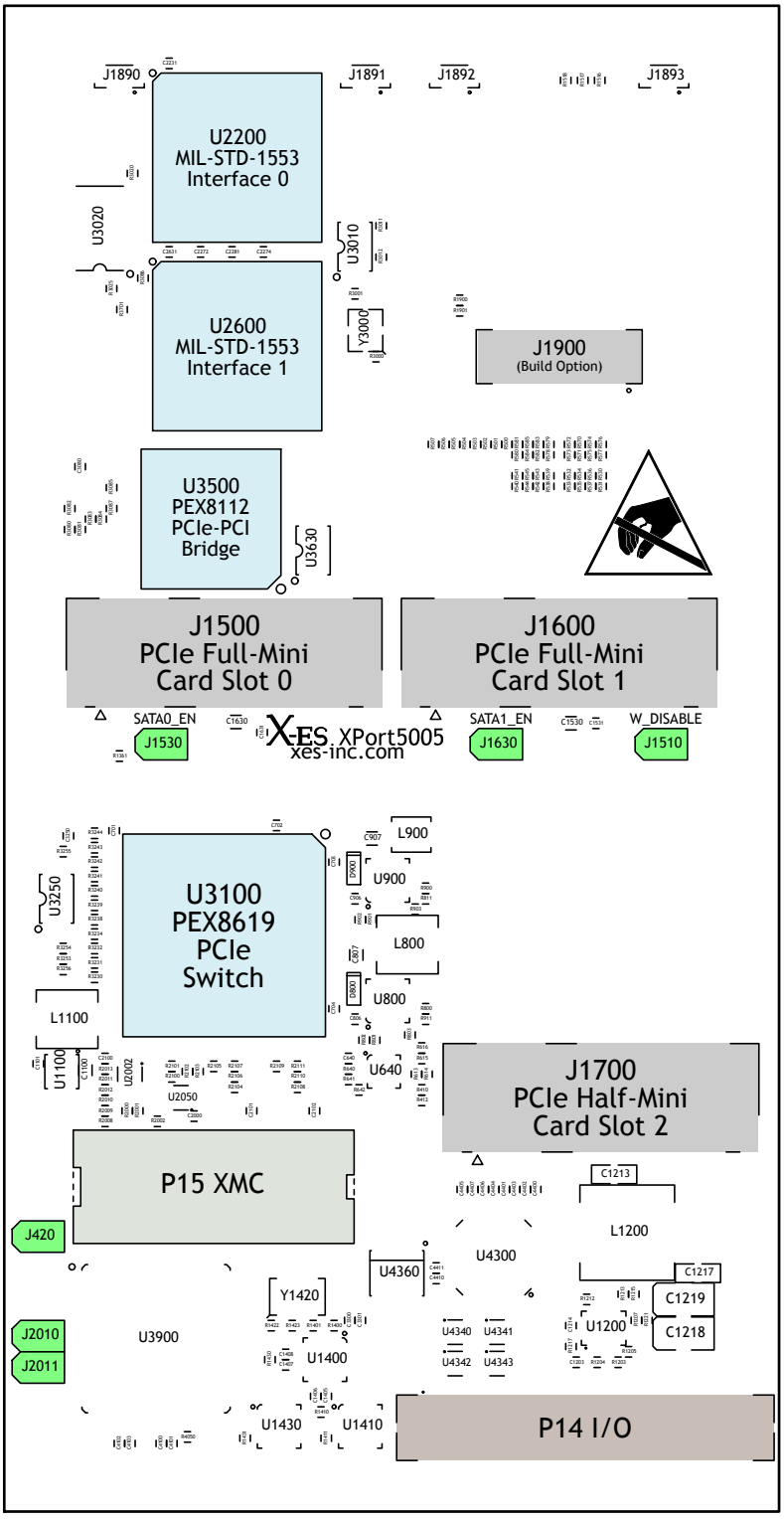
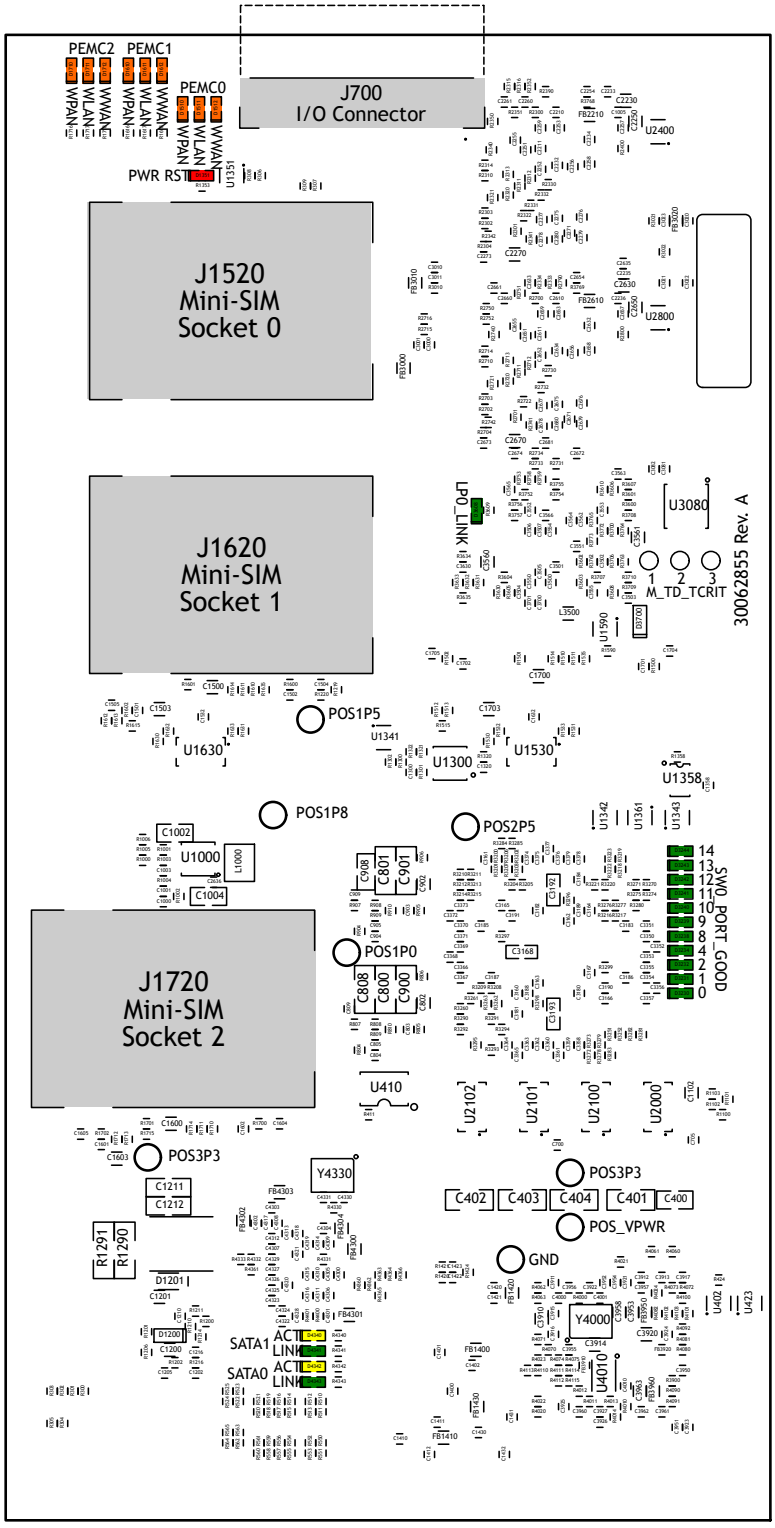


Figure 2.2: Back Component Map (Revision A)



2.5 Jumpers

Table 2.6 describes the jumpers used on the XPort5005.

Table 2.6: Jumper Functions

Jumper	Description
J420	**Non-Volatile Memory Write Enable.** Removing this jumper allows the host to control non-volatile memory write access on the XPort5005. Installing this jumper will enable write access to all non-volatile memory on the card.
J2010	**XMC Backplane JTAG Enable.** By default, the XMC Connector JTAG signals (TRST#, TMS, TCK, TDI, TDO) are not connected to the JTAG chain of the XPort5005, and TDI is connected to TDO on the XMC connector side. When this jumper is installed, the XMC connector JTAG signals are connected to the XPort5005 JTAG chain. Note that J2010 should never be installed when the JTAG COP connector is in use. J2010 is intended for factory use only.
J2011	**JTAG Chain Enable.** By default, the XPort5005's JTAG chain is empty. When this jumper is installed, all the on-board devices are buffered.
J1510	**PCIe Mini Wireless Disable.** When installed, this jumper asserts the hardware wireless disable signal on all the of XPort5005's PCIe Mini Card slots.
J1530	**SATA0 Enable.** When installed, this jumper routes SATA to Mini Card slot 0 in place of PCIe. (Install when using mSATA module in card slot 0.)
J1630	**SATA1 Enable.** When installed, this jumper routes SATA to Mini Card slot 1 in place of PCIe. (Install when using mSATA module in card slot 1.)

2.6 LEDs

Table 2.7 describes the LEDs used on the XPort5005.

Table 2.7: LED Definitions

LED	Color	Description
D1351	Red	**Reset.** When lit, indicates the XPort5005 and populated card slots are held in reset.
D2150	Orange	**PEMC0 WPAN.** Wireless status LED. Functionality is determined by Mini Card hosted in slot 0.
D2151	Orange	**PEMC0 WLAN.** Wireless status LED. Functionality is determined by Mini Card hosted in slot 0.
D2152	Orange	**PEMC0 WWAN.** Wireless status LED. Functionality is determined by Mini Card hosted in slot 0.
D2160	Orange	**PEMC1 WPAN.** Wireless status LED. Functionality is determined by Mini Card hosted in slot 1.
D2161	Orange	**PEMC1 WLAN.** Wireless status LED. Functionality is determined by Mini Card hosted in slot 1.
D2162	Orange	**PEMC1 WWAN.** Wireless status LED. Functionality is determined by Mini Card hosted in slot 1.
D2170	Orange	**PEMC2 WPAN.** Wireless status LED. Functionality is determined by Mini Card hosted in slot 2.
D2171	Orange	**PEMC2 WLAN.** Wireless status LED. Functionality is determined by Mini Card hosted in slot 2.
D2172	Orange	**PEMC2 WWAN.** Wireless status LED. Functionality is determined by Mini Card hosted in slot 2.
D3230-D3234	Green	**SW0_PORT_GOOD.** 0-4 indicate the connection width between the XPort5005 and host (x1, x2, x4, x8) (solid = 5 Gbps; blinking = 2.5 Gbps)
D3238-D3244	Green	**SW0_PORT_GOOD.** 8 = x1 link to the USB 2.0 bridge; 9 = unused; 10 = x1 link to card 0; 11 = x1 link to card 1; 12 = x1 link to card 2; 13 = x1 link to SATA bridge; 14 = x1 link to PCI bridge (solid = 5 Gbps; blinking = 2.5 Gbps)

Table 2.7: LED Definitions *(continued)*

LED	Color	Description
D3608	Green	**LP0_LINK.** When lit, indicates a valid link between the PCIe-PCI bridge and the PCIe switch
D4340	Yellow	**SATA1 ACT.** Indicates data transfer activity on SATA port 1
D4341	Green	**SATA1 LINK.** Indicates a valid connection to SATA port 1
D4342	Yellow	**SATA0 ACT.** Indicates data transfer activity on SATA port 0
D4343	Green	**SATA0 LINK.** Indicates a valid connection to SATA port 0

Mezzanine Interface

This chapter describes details associated with the XPort5005's Mezzanine Card Interface.

3.1 PMC

The XPort5005 can only be configured as an XMC. However, the XPort5005 provides an option to include P14 for additional I/O capabilities.

3.1.1 PMC I/O Signals

Table 3.1 describes the signals present on the PMC connectors.

Table 3.1: PCI I/O Signal Descriptions

Signal	Description
-	**No Connection.**
CANBUS_[0:1][A:B]	**CANbus Links.** CANbus (controller area network) link A or B from slot 0 or 1.
1553_[0:1][A:B] /1553_[0:1][A:B]#	**1553 Links.** IEEE 1533 primary (A) or secondary (B) link pairs for slot 0 or 1.
1553_0_DIRIG	**1553 Digital IRIG.** Optional IEEE 1533 digital IRIG input for both modules
M[0:1]_DIS_BC_R	**1553 Disable BC.** Optional disable BC for module 0 or 1
M[0:1]_EXT_TRIG_R	**1553 External Trigger.** Optional external trigger for primary and secondary links
1553_0_TXEN[1:2]#	**1553 TX Inhibit.** Optional transmission inhibit for primary and secondary links

3.1.2 PMC Connector

P14 is the only PMC connector present on the XPort5005.

3.1.2.1 P14

Table 3.2: P14 Pinout

Pin	Signal	Pin	Signal
1	-	2	-
3	-	4	-
5	GND	6	GND
7	-	8	-
9	-	10	-
11	GND	12	GND
13	-	14	-
15	-	16	-
17	GND	18	GND
19	-	20	-
21	-	22	-
23	GND	24	GND
25	-	26	-
27	-	28	-
29	1553_1_A#	30	1553_1_B#
31	1553_1_A	32	1553_1_B
33	-	34	-
35	-	36	-
37	-	38	-
39	-	40	-
41	1553_0_A#	42	1553_0_B#
43	1553_0_A	44	1553_0_B
45	CANBUS_0A	46	CANBUS_1A
47	CANBUS_0A#	48	CANBUS_1A#

Table 3.2: P14 Pinout *(continued)*

Pin	Signal	Pin	Signal
49	CANBUS_0B	50	CANBUS_1B
51	CANBUS_0B#	52	CANBUS_1B#
53	-	54	-
55	-	56	-
57	[M1_DIS_BC_R]*	58	-
59	[1553_0_DIRIG]*	60	[M1_EXT_TRIG_R]*
61	[1553_0_TXEN1#]*	62	[1553_0_TXEN2#]*
63	[M0_DIS_BC_R]*	64	[M0_EXT_TRIG_R]*

*build option, disabled by default

3.2 XMC

The XPort5005 is an XMC module that conforms to the VITA 42 / VITA 42.3 specification and supports a x8 PCI Express interface. It can operate at PCI Express Gen2 speeds.

3.2.1 PCI Express Configuration Space

Table 3.3 shows the expected PCI configuration space headers that will appear to an external card's CPU when the XPort5005 is operating as an endpoint. A PCI Express endpoint (EP) uses a Type 0 configuration header.

Table 3.3: PCI Express Endpoint Port Type 0 Configuration Header

External Bus	Device Name *	Vendor ID	Device ID
XMC	PEX8112	0x10B5	0x8112
XMC	PEX8619	0x10B5	0x8619
XMC	88SE9182	0x1B4B	0x9182
XMC	BU-67301	0x4DDC	0x1A00

*Device list may vary, depending on the specific configuration. Contact X-ES for details.

3.2.2 PCI Express Switch

The XPort5005 utilizes a PLX PEX8619 16-lane PCI Express Gen2 switch with non-transparent bridging and integrated DMA controller. Non-transparent bridging allows for multiple hosts, and the DMA controller allows for offloading memory-intensive transfers to the switch.

Table 3.4: PEX8619 PCI Express Port Assignment

PCI Express Port	Device Assignment
Port 0, Lanes 7-0	XMC
Port **x**, Lane 8	n/c
Port **x**, Lane 9	n/c
Port **x**, Lane 10	PCIe Mini Site 0
Port **x**, Lane 11	PCIe Mini Site 1
Port **x**, Lane 12	PCIe Mini Site 2
Port **x**, Lane 13	88SE9125
Port **x**, Lane 14	PEX8112

3.2.3 XMC Signals

The XPort5005 is a VITA 42, PrXMC-compliant XMC. It supports all required functions for operating as Root Complex or Endpoint.

Table 3.5 describes the signals present on the XMC connectors.

Table 3.5: XMC Signal Descriptions

Signal	Description
-	**No Connection.**
VPWR	**Main Power Rail.** VPWR may be +12 V or +5 V.
+3.3V	**3.3-Volt Power Rail.**
GND	**Digital Ground.**
PE*n*_TX[0:*x*] /PE*n*_TX[0:*x*]#	**PCI Express Transmit.** PCI Express slot *n* transmit data from the XPort5005 mezzanine card to the carrier for lanes 0 through *x*.
PE*n*_RX[0:*x*] /PE*n*_RX[0:*x*]#	**PCI Express Receive.** PCI Express slot *n* receive data from the carrier to the XPort5005 mezzanine card for lanes 0 through *x*.

Table 3.5: XMC Signal Descriptions *(continued)*

Signal	Description
REFCLK/REFCLK#	**PCI Express Reference Clock.** 100 MHz reference clock driven from carrier into the module. By default, the PCI Express REFCLK is generated completely on-board the XPort5005. As such, these pins are not used. Optionally, the XPort5005 can be factory-configured to source REFCLK from these pins.
GA[2:0]	**IPMI I²C Channel Select.** Received by the XMC to determine its IPMI I²C address.
MSCL	**IPMI I²C Serial Clock.** Received by the XMC as a clock reference for the IPMI I²C interface. This is only connected to a SEEPROM that stores FRU information, and does not connect to the XPort5005's local I²C bus.
MSDA	**IPMI I²C Serial Data.** Bi-directional signal used as a data line for the IPMI I²C interface. This is only connected to a SEEPROM that stores FRU information, and does not connect to the XPort5005's local I²C bus.
NVMRO	**Non-Volatile Memory Read Only.** Received by the XMC to prevent any non-volatile storage on the XMC from being written when asserted high.
MRSTI#	**Reset In.** Received by the XMC to indicate system reset when asserted low.
MRSTO#	**Reset Out.** Driven by the XMC to provide a reset input to the carrier. The XMC does not assert this signal in response to MRSTI# and therefore, may be connected to MRSTI#.
TRST#/TCK/TMS /TDI/TDO	**JTAG.** XMC interface JTAG signals.
GPIO*n*	**GPIO.** Port *n* general purpose input/output.

3.2.4 XMC Connector

3.2.4.1 P15

Table 3.6: P15 Pinout

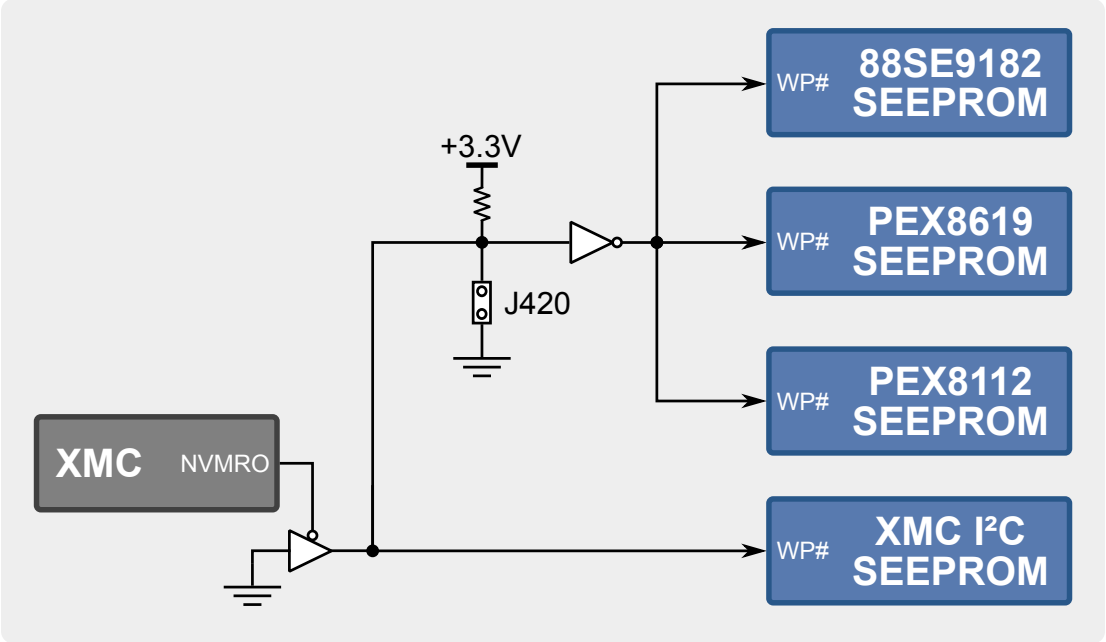
Pin	A	B	C	D	E	F
1	PE0_TX0	PE0_TX0#	+3.3V	PE0_TX1	PE0_TX1#	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PE0_TX2	PE0_TX2#	+3.3V	PE0_TX3	PE0_TX3#	VPWR
4	GND	GND	TCK	GND	GND	-
5	PE0_TX4	PE0_TX4#	+3.3V	PE0_TX5	PE0_TX5#	VPWR
6	GND	GND	TMS	GND	GND	-
7	PE0_TX6	PE0_TX6#	+3.3V	PE0_TX7	PE0_TX7#	VPWR
8	GND	GND	TDI	GND	GND	-
9	-	-	-	-	-	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PE0_RX0	PE0_RX0#	-	PE0_RX1	PE0_RX1#	VPWR
12	GND	GND	GA1	GND	GND	GND
13	PE0_RX2	PE0_RX2#	-	PE0_RX3	PE0_RX3#	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PE0_RX4	PE0_RX4#	-	PE0_RX5	PE0_RX5#	VPWR
16	GND	GND	NVMRO	GND	GND	MSCL
17	PE0_RX6	PE0_RX6#	-	PE0_RX7	PE0_RX7#	-
18	GND	GND	-	GND	GND	-
19	REFCLK0	REFCLK0#	-	-	-	-

3.3 Non-Volatile Memory Write Protection

The XPort5005 supports write protecting all non-volatile memory from an on-card jumper and from the XMC interface. This allows the XPort5005 to be configured to be write protected in a secure environment. Allowing this to be driven from the XMC backplane to the XPort5005 allows for the entire system to be protected by the system host.

Figure 3.1 shows a detailed diagram of the non-volatile write protection logic. When the XPort5005 is installed on an XMC carrier, the NVMWP functionality is determined by the XMC host, with J420 allowing a local override of the write protect when that jumper is installed. See Section 2.5 for more information on J420.

Figure 3.1: Non-Volatile Memory Write Protection



PCIe Mini Card Interface

This chapter describes details associated with the XPort5005's PCI Express Mini Card interface, which is detailed in the *PCI Express Mini Card Electromechanical Specification, Rev. 2.0*. The XPort5005 employs high-speed multiplexors that allow for the use of mSATA drives in its two Full-Mini Card slots.

4.1 PCIe Mini Card Connectors

The XPort5005 has three PCIe Mini Card connector slots on the front side of the printed circuit board. Two of these connectors provide support for either Full- or Half-Mini Cards or mSATA drives, and the third supports a Half-Mini Card.

4.1.1 Full-Mini Slot 0 (J1500)

Table 4.1: J1500 Pinout

Pin	Signal	Pin	Signal
1	-	2	+3.3V
3	PEMC0_COEX1	4	GND
5	PEMC0_COEX2	6	PEMC0_COEX3
7	-	8	PEMC0_UIM_PWR
9	GND	10	PEMC0_UIM_DATA
11	PEMC0_REFCLK#	12	PEMC0_UIM_CLK
13	PEMC0_REFCLK	14	PEMC0_UIM_RST
15	GND	16	PEMC0_UIM_SPU
17	USB_PEMC0_UIM_D#	18	PEMC0_PRESENT_R#
19	USB_PEMC0_UIM_D	20	PEMC0_W_DISABLE1#
21	GND	22	PEMC_RST#

Table 4.1: J1500 Pinout *(continued)*

Pin	Signal	Pin	Signal
23	PE_PEMC0TOMUX0_0#	24	+3.3V
25	PE_PEMC0TOMUX0_0	26	GND
27	GND	28	PEMC0_ANTCTRL0
29	GND	30	PEMC_SCL
31	PE_MUX0TOPEMC0_0#	32	PEMC_SDA
33	PE_MUX0TOPEMC0_0	34	GND
35	GND	36	USB_PEMC0_D#
37	GND	38	USB_PEMC0_D
39	+3.3V	40	GND
41	+3.3V	42	PEMC0_WWAN_LED#
43	GND	44	PEMC0_WLAN_LED#
45	PEMC0_ANTCTL2	46	PEMC0_WPAN_LED#
47	PEMC0_ANTCTL3	48	PEMC0_ANTCTRL1
49	-	50	GND
51	PEMC0_W_DISABLE2#	52	+3.3V

4.1.2 Full-Mini Slot 1 (J1600)

Table 4.2: J1600 Pinout

Pin	Signal	Pin	Signal
1	-	2	+3.3V_PEMC
3	PEMC1_COEX1	4	GND
5	PEMC1_COEX2	6	PEMC1_COEX3
7	-	8	PEMC1_UIM_PWR
9	GND	10	PEMC1_UIM_DATA
11	PEMC1_REFCLK#	12	PEMC1_UIM_CLK
13	PEMC1_REFCLK	14	PEMC1_UIM_RST
15	GND	16	PEMC1_UIM_SPU
17	USB_PEMC1_UIM_D#	18	PEMC1_PRESENT_R#

Table 4.2: J1600 Pinout *(continued)*

Pin	Signal	Pin	Signal
19	USB_PEMC1_UIM_D	20	PEMC1_W_DISABLE1#
21	GND	22	PEMC_RST#
23	PE_PEMC1TOMUX1_0#	24	+3.3V_PEMC
25	PE_PEMC1TOMUX1_0	26	GND
27	GND	28	PEMC1_ANTCTRL0
29	GND	30	PEMC_SCL
31	PE_MUX1TOPEMC1_0#	32	PEMC_SDA
33	PE_MUX1TOPEMC1_0	34	GND
35	GND	36	USB_PEMC1_D#
37	GND	38	USB_PEMC1_D
39	+3.3V_PEMC	40	GND
41	+3.3V_PEMC	42	PEMC1_WWAN_LED#
43	GND	44	PEMC1_WLAN_LED#
45	PEMC1_ANTCTL2	46	PEMC1_WPAN_LED#
47	PEMC1_ANTCTL3	48	PEMC1_ANTCTRL1
49	-	50	GND
51	PEMC1_W_DISABLE2#	52	+3.3V_PEMC

4.1.3 Half-Mini Slot 2 (J1700)

Table 4.3: J1700 Pinout

Pin	Signal	Pin	Signal
1	-	2	+3.3V_PEMC
3	PEMC2_COEX1	4	GND
5	PEMC2_COEX2	6	PEMC2_COEX3
7	-	8	PEMC2_UIM_PWR
9	GND	10	PEMC2_UIM_DATA
11	PEMC2_REFCLK#	12	PEMC2_UIM_CLK
13	PEMC2_REFCLK	14	PEMC2_UIM_RST

Table 4.3: J1700 Pinout *(continued)*

Pin	Signal	Pin	Signal
15	GND	16	PEMC2_UIM_SPU
17	USB_PEMC2_UIM_D#	18	GND
19	USB_PEMC2_UIM_D	20	PEMC2_W_DISABLE1#
21	GND	22	PEMC_RST#
23	PE_PEMC2TOSW0_0#	24	+3.3V_PEMC
25	PE_PEMC2TOSW0_0	26	GND
27	GND	28	PEMC2_ANTCTRL0
29	GND	30	PEMC_SCL
31	PE_SW0TOPEMC2_0#	32	PEMC_SDA
33	PE_SW0TOPEMC2_0	34	GND
35	GND	36	USB_PEMC2_D#
37	GND	38	USB_PEMC2_D
39	+3.3V_PEMC	40	GND
41	+3.3V_PEMC	42	PEMC2_WWAN_LED#
43	GND	44	PEMC2_WLAN_LED#
45	PEMC2_ANTCTL2	46	PEMC2_WPAN_LED#
47	PEMC2_ANTCTL3	48	PEMC2_ANTCTRL1
49	-	50	GND
51	PEMC2_W_DISABLE2#	52	+3.3V_PEMC

4.2 Mini-SIM Sockets

The XPort5005 can host up to three mini-SIM cards on the back side of the printed circuit board.

4.2.1 SIM Socket 0 (J1520)

Table 4.4: J1520 Pinout

Pin	Signal
P1	PEMC0_UIM_PWR
P2	PEMC0_UIM_RST
P3	PEMC0_UIM_CLK
P4	USB_PEMC0_UIM_D
P5	GND
P6	PEMC0_UIM_SPU
P7	PEMC0_UIM_DATA
P8	USB_PEMC0_UIM_D#
P10	GND
P11	GND

4.2.2 SIM Socket 1 (J1620)

Table 4.5: J1620 Pinout

Pin	Signal
P1	PEMC1_UIM_PWR
P2	PEMC1_UIM_RST
P3	PEMC1_UIM_CLK
P4	USB_PEMC1_UIM_D
P5	GND
P6	PEMC1_UIM_SPU
P7	PEMC1_UIM_DATA
P8	USB_PEMC1_UIM_D#
P10	GND
P11	GND

4.2.3 SIM Socket 2 (J1720)

Table 4.6: J1720 Pinout

Pin	Signal
P1	PEMC2_UIM_PWR
P2	PEMC2_UIM_RST
P3	PEMC2_UIM_CLK
P4	USB_PEMC2_UIM_D
P5	GND
P6	PEMC2_UIM_SPU
P7	PEMC2_UIM_DATA
P8	USB_PEMC2_UIM_D#
P10	GND
P11	GND

Accessory Connectors

This chapter describes internal connectors on the XPort5005 that provide an interface for accessories from X-ES.

5.1 Overview

Table 5.1 gives a brief description of the XPort5005's accessory connectors.

Table 5.1: Accessory Connector Descriptions

Name	Reference Designator	Description
Front Panel I/O Connector	J700	Allows for access to I/O from hosted modules and onboard 1553 interface.

5.2 Accessory Connector Pinouts

Table 5.2: Front Panel I/O Connector Pinout (J700)

Pin	Signal
1	1553_0_A
2	1553_0_A#
3	GND
4	1553_0_B
5	1553_0_B#
6	GND
7	1553_1_A
8	1553_1_A#
9	GND

Table 5.2: Front Panel I/O Connector Pinout (J700) *(continued)*

Pin	Signal
10	1553_1_B
11	1553_1_B#
12	GND
13	1553_0_TXEN1#
14	M0_DIS_BC
15	M0_EXT_TRIG
16	1553_0_DIRIG
17	1553_0_TXEN2#
18	M1_DIS_BC
19	M1_EXT_TRIG
20	GND
21	GND
22	GND

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Extreme Engineering Solutions, Inc.
3225 Deming Way, Suite 120 • Middleton, WI 53562
Phone: 608.833.1155 • Fax: 608.827.6171
sales@xes-inc.com • http://www.xes-inc.com