Electrical and Computer Engineering

ECE 453

Lab 1:

Power Supply Schematic Capture

1. Lab Work

In this Lab 1, you will create the schematics for the power supply for your project. Several of the components that you will use have been specified for you. You will be required to read the device datasheets for those components to determine how to correctly interconnect these devices.

2. Requirements

- All components must have supplier links that include manufacturer and supplier part numbers.
- All resistors/capacitors must have a minimum size of 0805.
- All components must have a schematic symbol and PCB footprint
- Your power mezzanine board must use wall wart to supply power
    - Wall wart is required to be 12V
    - You need to have an associated barrel jack to connect the wall wart to your board. Use the following part for the wall wart barrel jack.
- The power mezzanine card MUST generate a 5.0V rail from the 12V input.
    - The 12V to 5.0V regulator must be a **TPS5420DR** switching regulator.
    - Create component schematic symbols/footprints for any components required by the regulator (resistors, capacitors, diodes, etc).
- The power mezzanine card MUST generate a 3.3V rail from the 5V rail.
    - The 5.0V to 3.3V regulator must be a **TLV73333PDBVR** linear regulator.
    - Create component schematic symbols/footprints for any components required by the regulator (resistors, capacitors, diodes, etc).
- The power mezzanine card MUST monitor the 5.0V and 3.3V rails.
    - The 3.3V power rail MUST be monitored using a TPS3705-33D.
    - The 5.0V power rail MUST be monitored using the PFI input of the TPS3705-33D.
    - Detect if the 5.0V rail drops below 4.55V
    - The 3.3V and 5.0V power rails must have a “power good” LED to indicate that regulators are functioning correctly.
- Do not modify the connections to the schematic symbols already provided in the project. These connections have been completed for you so that the Power Mezzanine card you are developing can properly interface with the Digital Interface board being assembled by one of your teammates..
- Do not modify the location of the pre-populated connectors on the printed circuit board.

3. Post Lab: What to Turn in

File Name	Description
Lab1_PWR.zip	Altium Project ZIP file. This should include Altium documents and libraries. All components should have completed supplier links, schematic symbols, and PCB footprints. Be sure to run the ECE453_PWR.OutJob to generate a PDF of the **schematics** and an Excel file for the **BOM**. Delete the History folder before creating the ZIP file.

4. Design Review Check List

	Schematic Requirements	Completed
1	All Nets have net names	
2	All parts have a unique reference designators	
3	All parts have supplier links that include the manufacturer and part num.	
4	Reference Designators are clearly visible and do not overlap.	
5	All integrated circuits have a 1uF bypass capacitor on EACH supply pin. Not necessary for single MOSFETs.	
6	All unused pins should be marked with No ERC Connectors	
7	Design Compiles without errors. You can ignore errors related to mechanical parts.	
8	Informational Comments	
9	Test Points added for critical signals	
10	Test Points for all power signals, including GND	