Electrical and Computer Engineering

ECE453

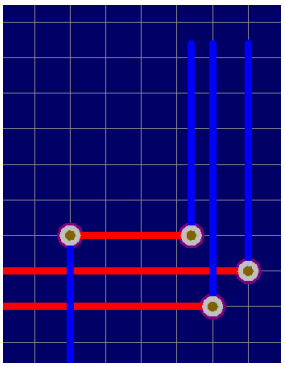
Lab 2

PCB Routing

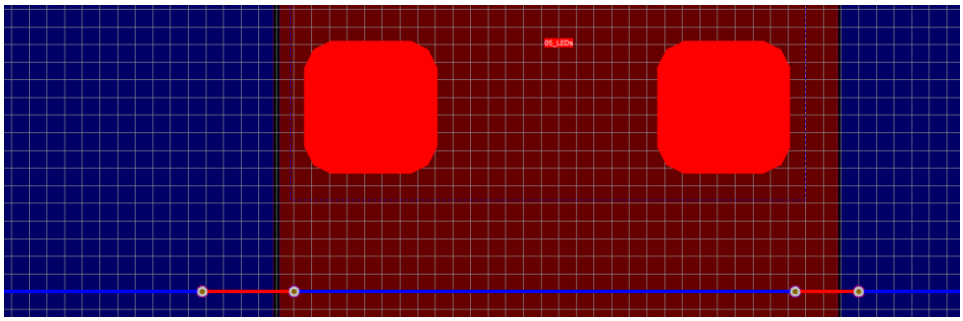
1. Lab 2 Overview

In Lab 2, you will complete the PCB placement and routing of your power mezzanine card.

- Use an orthogonal approach to routing signals. All vertical tracks should be on the bottom layer. All Horizontal tracks should be on the top layer. This is going to help avoid situations where a signal cannot be routed.



- If you have an exceptionally long track that create necks in your polygons, you can add a short length of track on the opposite layer. This is called stitching a signal. Stitching ensures that your polygons have good electrical connectivity and provide an adequate current return path.



- Use Polygons to connect power and ground.
- All Test Points should have a visible Text Label indicating which signal the test point is connected to.
- Use the PCB checklist found on the course website to ensure that your PCB can be manufactured correctly.

2. Ordering Your PCB

Have an instructor review your printed circuit board layout. Once you have implemented any corrections indicated by your instructor, you will need to place an order with a contract manufacturer such as PCB Way or Advanced Circuits. This order needs to take place so that your printed circuit boards arrive within 7 days of turning in this assignment.

3. What to Turn in

Folder Name	Description
Lab2_PCB.zip	Altium Project ZIP file that includes completed .SchDoc, .PcbDoc, .SchLib, and .PcbLib files required for the power mezzanine board. A PDF receipt from your chosen contract manufacturer. Delete the History folder before creating the ZIP file.

4. Design Review Check List

	PCB Requirements	Completed
1	Bypass Capacitors within 200 mils to the pin they service.	
2	Power signals like 3v3 should be carried by very thick traces (25-200mils) or preferably by dedicated polygon pours/planes.	
3	No conductive material within 50 mils of the board edge.	
4	Multiple LEDs and Diodes placed in the same area should have the same orientation.	
5	There should be a 10 mil trace on a mechanical layer that defines the board outline	
6	Minimum hole size set to 15 mils	
7	Minimum annular ring of 6 mils on all vias and through hold parts.	
8	All nets are Routed	
9	Reference designators for each part clearly indicate which part they are associated with	
10	All test points have a text string in a silk screen layer indicating what net they are connected to.	
11	Design passes Design Rule Check with 0 errors and 0 warnings	