Rectification of Finite Field Arithmetic Circuits using Computer Algebra Techniques

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This article presents a complete and scalable symbolic computer algebra approach for rectification of faulty finite field arithmetic circuits at multiple nets. Contemporary approaches that utilize SAT solving, and Craig interpolation is infeasible in rectifying arithmetic circuits. Our approach represents the circuit as a system of polynomials and rectifies it against a polynomial specification by applying Gröbner basis (GB) based algorithms. Given a set of m candidate nets as rectification targets, first, we utilize algebra-based techniques to derive the necessary and sufficient conditions for the existence of a rectification function at the targets. Then, upon confirmation, we compute the patch functions collectively for the targets with variable support in primary inputs. For patch function computation, we present two approaches: a greedy approach which resolves the rectification functions for the targets, and an approach which explores a subset of don't care conditions for the targets. In this regard, we show how the algebraic computing model allows to explore the space of admissible rectification patches, collectively, for the m targets. Our approach is implemented as a custom software and utilizes existing open-source symbolic algebra libraries for computations. As part of our custom software, we show how our rectification formulation can be efficiently represented and manipulated using the Boolean data-structure of Zero-suppressed Binary Decision Diagrams (ZDDs). We substantiate the approach with experimental results demonstrated over large operand width benchmarks up to 571 bits, including those that conform to the NIST-standard for ellyptic curve cryptography.

CCS Concepts: • **Hardware** → Electronic design automation.

Additional Key Words and Phrases: Logic Synthesis, Rectification, Arithmetic Circuits

1 INTRODUCTION

Debugging and rectification of digital logic circuits aims to correct a given defective circuit implementation to match its intended specification. As opposed to a complete redesign of the circuit, it is desirable to synthesize rectification sub-functions with minimal topological changes to the existing design – a problem often termed as *partial synthesis*. The process constitutes identifying candidate nets in the circuit as potential targets for rectification, followed by a check to ascertain the rectifiability of the circuit at these targets. If the check confirms that the targets admit correction, corresponding rectification functions are computed and synthesized to patch the circuit at these targets.

It is akin to performing synthesis for Engineering Change Order (ECO), wherein a highly optimized implementation is minimally modified to match the updated specification in a cost-effective way. This is achieved by reusing prior design efforts and avoiding rerunning the entire synthesis flow while adhering to the resource constraints and the physical design limitations.

The rectification problem has witnessed much research over the years – some of the earliest being [20, 30, 32]. Owing to a manifold improvement in the efficiency of SAT solvers, there has been a renewed interest in the problem over the last decade from the logic synthesis, testing, and verification communities [6, 12, 13, 33]. These techniques generally employ SAT, Quantified Boolean Formula (QBF) solving, and Craig Interpolation (CI) based techniques for rectification. While

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successful for control-dominated applications, these techniques are computationally infeasible for the rectification of arithmetic circuits. Symbolic Computer Algebra (SCA) techniques are found to be more suitable for formal analysis and verification of arithmetic circuits. However, utilization of the various facets and capabilities of the SCA techniques for post-verification debugging and rectification has only recently begun to be addressed [9, 15, 16, 23, 27–29].

1.1 Motivation

This article addresses the problem of *multi-target rectification of faulty finite field arithmetic circuits*. Such circuits find applications in cryptography, error-control codes, RFID tags, testing of VLSI circuits, among others. Specifically, Elliptic Curve Cryptography (ECC) is one of the most important usage models where the public-key cryptography is designed on the algebraic structure of elliptic curves over finite fields. Due to its shorter key length and efficiency [22], ECC is fast becoming the encryption standard with applications in cryptocurrency transaction signing and securing web traffic. The main building blocks of ECC hardware implementations are fast, custom-built finite field arithmetic circuits, thus raising the potential for errors in the implementation, which have to be eventually rectified. It was shown [2] that incorrect cryptography hardware can lead to full leakage of the security key and even counterfeiting [34]. To secure data privacy and avoid vulnerabilities in crypto-systems, their rectification is imperative.

1.2 Problem Statement and Objective

We are given the following:

- As the specification, a multivariate polynomial f with coefficients in a finite field of 2^n elements (denoted $\mathbb{F}_{2^n}$), for a given $n \in \mathbb{Z}_{>0}$.
- An irreducible polynomial $P_n(x)$ of degree n with coefficients in $\{0, 1\}$ used to construct $\mathbb{F}_{2^n}$.
- A faulty circuit implementation C, with no assumptions on the number or the type of bugs present in C.
- A set $W = \{w_1, \dots, w_m\}$ of m candidate targets from C, pre-specified or selected using contemporary signal selection heuristics [6, 18, 19].

The objective of our approach is to:

- Ascertain that C admits rectification at these m targets.
- Compute a set of individual rectification functions $U = \{u_1, \dots, u_m\}$ for the corresponding targets.
- Derive *don't care conditions* corresponding to the m rectification functions.
- Synthesize the rectification polynomials into logic sub-circuit patches.

1.3 Approach and Contribution

We model the rectification problem using concepts from algebraic geometry and use symbolic computer algebra algorithms to determine rectifiability and to compute rectification functions. The specification f and implementation C are modeled in terms of polynomial ideals. The rectifiability check is formulated on these ideals using the Strong Nullstellensatz over finite fields. Subsequently, the rectification functions are computed using the Gröbner bases [1] of these ideals. In this regard, our approach goes beyond the Nullstellensatz-based results produced from the m-target rectifiability check presented in [28], and *computes m* individual rectification functions, altogether. We show how, in our algebraic model the don't cares correspond to *varieties of polynomial ideals*, and how they can be computed with Gröbner bases. The rectification functions are computed as polynomials whose common zeros correspond to the minterms of the functions. Overall, our contributions are as follows:

- Formulate a check to determine the rectifiability of C at the m targets.
  - This check implies the existence of a polynomial function over $\mathbb{F}_{2^n}$ with mapping $u_i : \mathbb{F}_2^{|X_{PI}|} \longrightarrow \mathbb{F}_2$ at individual targets w_i. Here, $1 \leq i \leq m$, $\mathbb{F}_2 = \{0, 1\}$, and X_{PI} denotes the set of primary input variables of C.
  - Substituting the polynomial function at the corresponding targets, $w_i = u_i[X_{PI}]$, rectifies the circuit.
- While there may exist multiple rectification functions for each of the m targets, we compute one such individual function for each of the targets. We present two approaches for patch function computation:
  - First, a heuristic which greedily resolves the rectification functions for the targets.
  - A second heuristic which explores a subset of *don't care conditions* for the targets.
    * We present efficient techniques to explore the space of various admissible rectification functions, in turn, computing subsets of don't care conditions which helps in simplifying the rectification patches.
    * Synthesis of the corresponding polynomial patch functions along with don't cares, demonstrates the efficacy of our approach in terms of improved area and delay characteristics of the patches.
- We further propose a synthesis procedure that can translate such polynomial functions to Boolean rectification functions. Subsequently, these functions are translated to Boolean logic by converting the algebraic multiplication and addition operations to the Boolean AND and XOR operations, respectively.
- We present theoretical concepts and algorithms, and their implementations, to provide a scalable and efficient solution for the rectification of finite field arithmetic circuits.
  - In this regard, we show how to efficiently represent and manipulate our multi-target rectification formulation on circuits using the Boolean data-structure of Zero-suppressed Binary Decision Diagrams (ZDDs).
  - We utilize ZDDs to perform the core GB-based reduction computation.
- We substantiate the efficacy of our techniques by rectifying large operand-width finite field arithmetic circuits, where conventional SAT-solver based rectification approaches are infeasible.
  - We reason about the presence or absence of solutions and other properties of a system of polynomials without explicitly solving them. In contrast, the contemporary approaches explicitly solve for a solution at each step and hence are infeasible towards rectification of arithmetic circuits.

The article is organized as follows: The following section covers preliminary background. Section 4 reviews the polynomial modeling concepts. Rectification check formulation is described in Section 5, followed by the rectification function and don't care computations in Section 7. Section 9 discusses the implementation details, and experimental results are described in Section 10, and Section 11 concludes the article.

2 REVIEW OF PRIOR WORK

Contemporary approaches formulate rectification using QBF solving [13], using CI or iterative SAT solving [33, 35]. The rectification techniques in [10, 18, 33, 36] iteratively and incrementally compute multiple single-fix functions that partially patch the circuit in each iteration. They ensure that, in each iteration, erroneous minterms are resolved and no new errors are introduced, eventually converging the circuit to the given specification. Recent techniques incorporate resource awareness in patch generation by re-expressing the obtained Skolem functions in terms of internal signals [6], employ improved heuristics for target selection [18], or resolve a combination of such objectives, such as the symbolic sampling approach of [19]. In [19] the authors propose a robust ECO approach to derive patches with minimal impact on the heavily optimized existing implementation against a structurally dissimilar ECO-evolved specification. They enumerate rectification points functionally by simulation and match the circuitry of patches implicitly to maximize the reuse of existing logic in the implementation. To achieve scalability, the method proposes modeling and analyzing its computations in symbolic sampling domain. However, circuits that implement polynomial computations over large bit-vector operands are hard to rectify using models based on Boolean function, SAT/SMT-solvers, etc. Our experiments show that the contemporary SAT solvers fail to rectify finite field circuits beyond 16-bit operands.

2.1 Symbolic Computer Algebra

In the context of arithmetic circuits, symbolic computer algebra techniques for integer arithmetic [8, 9, 23] and finite field circuits [15, 16, 27] have been considered for rectification. The rectification approaches presented in [8, 9] rely heavily on the structure of the arithmetic circuit. Further, if the circuit contains redundancies, their approach fails [26] to resolve the rectification question. Further, the approach of [23] is limited by the fault model, which addresses only a gate misplacement fault. The authors in [15, 16] present a Weak Nullstellensatz based rectification formulation to determine the existence of rectification functions and solve them using GB-based techniques. Subsequently, the rectification function is computed by the application of Craig Interpolation in polynomial algebra over finite fields. The authors show how the lattice of all algebraic interpolants correspond to don’t care conditions for the rectification function, and synthesize rectification functions from algebraic interpolants. As an alternative to CI, in [27] we presented an approach where rectification was formulated using ideal membership and extended GB theory. However, all these algebraic approaches address only *single-fix rectification* – where irrespective of the type or number of bugs in the circuit, rectification is attempted at a single net. This is too restrictive, and depending on the nature of the bugs, the circuit may not admit single-fix rectification at all. In such cases, the correction has to be attempted at multiple targets.

Recently, we proposed a word-level SCA based approach [28] to *decide multi-target rectifiability* in finite field circuits. Given a set of m-targets within a n-bit operand width circuit, the approach presents a Strong Nullstellensatz based decision procedure to determine the existence of rectification functions at these targets. The efficiency of the approach is derived by interpreting the m-targets as a m-bit-vector. The problem was modeled at a word-level to enable the use of higher level abstraction in rectification and synthesis. However, enabling such word-level reasoning might induce computation issues across elements from the n-bit-vector space (circuit) and the m-bit-vector space (rectification patch). To resolve this incompatibility, we presented theory and mathematical derivations that facilitate algebraic computations over a unified domain modeled over $k = LCM(n, m)$. However, for finite field circuits, with practical applications in cryptography, the operand width n as dictated by the National Institute of Standards and Technology (NIST) is generally a prime number. For example, NIST-ECC recommends n to be 163 or larger (n= 163, 233, 283, 409, 571, etc.). Thus, for any given target size m, $k = LCM(n, m) = n * m$ becomes extremely large. This results in algebraic computations involving substantially large primitive elements and constants. The large size coupled with the complicated arithmetic nature of these circuits increases the complexity of the rectification problem. Moreover, the proposed approach [28] can only ascertain whether *there exists* a set of functions that can patch the circuit at the targets. As it is only a decision procedure, the approach cannot *compute* rectification functions. Thus the problem of multi-fix rectification of data-path circuits remains unsolved, and theoretical and algorithmic solutions to compute and synthesize rectification patches for arithmetic circuits are still desired.

3 PRELIMINARIES

This section reviews some basic concepts from symbolic computer algebra and associated algorithms utilized in this article.

Finite fields: Let $\mathbb{B}$ denote the Boolean domain, and $\neg, \wedge, \vee, \oplus$ the NOT, AND, OR and XOR operators, respectively. Let $\mathbb{F}_2 = \{0, 1\}$ be the field of 2 elements, and let $\mathbb{F}_q = \mathbb{F}_{2^n}$ denote the *finite field* of $q = 2^n$ elements, for a given $n \in \mathbb{Z}_{>0}$. We denote $\overline{\mathbb{F}}_q$ as the *algebraic closure* of $\mathbb{F}_q$. The algebraic closure of the finite field $\mathbb{F}_{2^n}$ is the union of all fields $\mathbb{F}_{2^k}$ such that $n|k$ (n divides k). $\mathbb{F}_{2^n}$ is the n-dimensional extension of $\mathbb{F}_2$, and it is constructed as $\mathbb{F}_{2^n} = \mathbb{F}_2[x] \pmod{P_n(x)}$. Here $P_n(x) \in \mathbb{F}_2[x]$ is a given degree-n polynomial, *irreducible* in $\mathbb{F}_2$, with a root γ, i.e. $P_n(\gamma) = 0$, which is a generator of $\mathbb{F}_{2^n}$. Then γ is called a primitive element (PE) of $\mathbb{F}_{2^n}$ and it generates the entire field: $\mathbb{F}_{2^n} = \{0, 1 = \gamma^{2^n-1}, \gamma, \gamma^2, \dots, \gamma^{2^n-2}\}$. Note: $\forall \gamma \in \mathbb{F}_{2^n}, \gamma^{2^n-1} = 1$. An element $A \in \mathbb{F}_{2^n}$ can be written as $A = a_0 + a_1 \cdot \gamma + \dots + a_{n-1} \cdot \gamma^{n-1}$, where $a_0, \dots, a_{n-1} \in \mathbb{F}_2$. In $\mathbb{F}_{2^n}$, the addition $(''+'')$ and multiplication $(''\cdot'')$ operations are performed in the base field $\mathbb{F}_2$ and reduced modulo the corresponding primitive polynomial $P_n(x)$. For $n, k \in \mathbb{Z}_{>0}$, if $n|k$, then $\mathbb{F}_{2^n} \subset \mathbb{F}_{2^k}$. Thus, $\mathbb{F}_2 \subset \mathbb{F}_{2^n}, \forall n > 1$. All fields of the type $\mathbb{F}_{2^n}$ have characteristic 2, and therefore $-1 = +1$ in $\mathbb{F}_{2^n}$.

Polynomial representation: Let $R = \mathbb{F}_q[x_1, \dots, x_d]$ be the polynomial ring in variables $x_1, \dots, x_d$ with coefficients in $\mathbb{F}_q$. A polynomial $f \in R$ is written as a finite sum of terms $f = c_1M_1 + c_2M_2 + \dots + c_rM_r$, where $c_1, \dots, c_r$ are coefficients from $\mathbb{F}_q$ and $M_1, \dots, M_r$ are monomials, i.e. power products of the type $x_1^{e_1} \cdot x_2^{e_2} \cdots x_d^{e_d}$, $e_j \in \mathbb{Z}_{\geq 0}$. To systematically manipulate the polynomials, a monomial order $>$ (or a term order) is imposed on R such that the monomials of all polynomials are ordered according to $>$. Subject to $>$, we have that $M_1 > M_2 > \dots > M_r$. Then, $lc(f) = c_1$, $lm(f) = M_1$, and $lt(f) = c_1M_1$ denote the *leading coefficient, leading monomial*, and *leading term* of f, respectively. Also, for $f \in R$, $tail(f) = f - lt(f)$. This work employs *lexicographic* (lex) term orders.

Polynomial Reduction via division: Let $f,\ g$ be polynomials. If $lm(f)$ is divisible by $lm(g)$, then we say that f *is reducible to* r modulo g, denoted $f \xrightarrow{g} r$, where $r = f - \frac{lt(f)}{lt(g)} \cdot g$. This operation forms the core of polynomial division algorithms and it has the effect of canceling the leading term of f to obtain r. Similarly, f can be *reduced* w.r.t a set of polynomials $F = \{f_1, \dots, f_s\}$. Then $f \xrightarrow{F}_+ r$ denotes the *reduction* of f modulo the set of polynomials F resulting in a remainder r, obtained by iteratively canceling terms in f by $lt(f_j), f_j \in F$, via polynomial division. The remainder r is said to be *reduced* such that no term in r is divisible by the leading term of any $f_j \in F$.

Algorithm 1 [1] presents the procedure which performs polynomial *reduction* by iteratively canceling one monomial at a time. The algorithm initializes h with the polynomial f and cancels its leading term by some polynomial f_j. If the leading term $lt(h)$ cannot be canceled by any $lt(f_j)$, then it is added to the final remainder r. We repeat this process until all the terms in h are analyzed. Along with the remainder r, the algorithm also returns the set of quotients $\{u_1, \dots, u_s\}$ of division of f by $\{f_1, \dots, f_s\}$, respectively, such that $f = u_1 \cdot f_1 + \dots + u_s \cdot f_s + r$.

Section 4 in the sequel describes how to represent a circuit C as a set of polynomials $F = \{f_1, \dots, f_s\}$ contained in R. We analyze the solutions to the polynomial equations $f_1 = \dots = f_s = 0$ and the multivariate polynomial specification $f = 0$ to formulate verification and rectification. For this purpose, we consider the *ideal* generated by the polynomials and their *variety.*

Algorithm 1 Multivariate Reduction of f by $F = \{f_1, \ldots, f_s\}$

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1: procedure multi_variate_division($f, \{f_1, \ldots, f_s\}, f_j \neq 0$)
2:     $u_j \leftarrow 0;\ r \leftarrow 0,\ h \leftarrow f$
3:     while $h \neq 0$ do
4:         if $\exists j$ s.t. $lm(f_j) \mid lm(h)$ then
5:             choose $j$ least s.t. $lm(f_j) \mid lm(h)$
6:             $u_j = u_j + \frac{lt(h)}{lt(f_j)}$
7:             $h = h - \frac{lt(h)}{lt(f_j)} f_j$
8:         else
9:             $r = r + lt(h)$
10:            $h = h - lt(h)$
11:    return $(\{u_1, \ldots, u_s\}, r)$
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Ideals and varieties: A given set of polynomials $F = \{f_1, \ldots, f_s\}$ from R, generates the *ideal* $J = \langle F \rangle \subseteq R$, defined as $J = \langle f_1, \ldots, f_s \rangle = \{h_1 \cdot f_1 + \cdots + h_s \cdot f_s \ : \ h_1, \ldots, h_s \in R\}$. Polynomials $f_1, \ldots, f_s$ form the *generators* or the *basis* of ideal J.

Let $\boldsymbol{a} = (a_1, \ldots, a_d) \in \mathbb{F}_q^d$ be a point in the affine space, and f a polynomial in R. If $f(\boldsymbol{a}) = 0$, we say that f *vanishes* on $\boldsymbol{a}$, or $\boldsymbol{a}$ is a *zero* of the polynomial f. In this work, we have to analyze the *set of all common zeros* of the polynomials of $F = \{f_1, \ldots, f_s\}$ that lie within the field $\mathbb{F}_q$ – i.e. the set of all point $\boldsymbol{a} \in \mathbb{F}_q^d$ such that $f_1(\boldsymbol{a}) = \cdots = f_s(\boldsymbol{a}) = 0$. This zero set is called the *variety*, which depends not just on the given set of polynomials in F, but rather on the ideal generated by polynomials. We denote it by $V(J)$, where: $V(J) = V_{\mathbb{F}_q}(J) = V_{\mathbb{F}_q}(\langle f_1, \ldots, f_s \rangle) = \{\boldsymbol{a} \in \mathbb{F}_q^d : \forall f \in J, f(\boldsymbol{a}) = 0\}$.

Boolean functions comprise a finite set of points. Hence, we can reason about them as varieties. If a point is an element of a variety, then that point can be considered either an on-, off-, or DC-set minterm of a corresponding Boolean function. Algebraic geometry analyzes the variety of ideals without explicitly computing them, which is infeasible in practice. Thus, to compute the union, intersection, and set difference of functions, operations are performed on the represented ideals by analyzing their corresponding varieties. Table 1 describes the correspondence between operations on Boolean functions, its variety interpretation, and the computation on ideals. We interpret the points within on-, off-, and DC-sets as varieties and utilize the correspondences from Table 1 for rectification formulations.

Table 1. Correspondences between algebraic operations and Boolean operations. Here, J_1 and J_2 correspond to the ideal generated by $\langle f \rangle$ and $\langle g \rangle$, respectively.

Boolean Function	*Variety interpretation*	*Ideal operation*
$f \vee g$	$V(J_1) \cup V(J_2)$	$J_1 * J_2$
$f \wedge g$	$V(J_1) \cap V(J_2)$	$J_1 + J_2$
$f - g$	$V(J_1) \setminus V(J_2)$	$J_1 : J_2$

Given two ideals $J_1 = \langle f_1, \ldots, f_s \rangle, J_2 = \langle h_1, \ldots, h_r \rangle$, the *sum of ideals* is denoted as $J_1 + J_2 = \langle f_1, \ldots, f_s, h_1, \ldots, h_r \rangle$, their *product* is given as $J_1 * J_2 = \langle f_i \cdot h_j : 1 \leq i \leq s, 1 \leq j \leq r \rangle$, and a *colon ideal* operation is defined as $J_1 : J_2 = \{f \in R \ : \ f \cdot g \in J_1, \forall g \in J_2\}$. Ideals and varieties are dual concepts: $V(J_1 + J_2) = V(J_1) \cap V(J_2)$, whereas $V(J_1 * J_2) = V(J_1) \cup V(J_2)$. A colon ideal operation corresponds the set difference of two varieties, $V(J_1 : J_2) = V(J_1) \setminus V(J_2)$. Modern computer algebra tools [4, 7] implement these ideal operations, which we utilize.

Gröbner Bases: An ideal may have many different sets of generators such that their varieties are the same. A *Gröbner basis* (GB) is one such generating set with special properties that allows to solve many polynomial decision and quantification problems.

Definition 3.1. *[Gröbner Basis] [1]: For a monomial ordering $>$, a set of non-zero polynomials $G = \{g_1, g_2, \dots, g_t\}$ contained in an ideal J, is called a Gröbner Basis (GB) of $J \iff \forall f \in J$, $f \xrightarrow{g_1,g_2,\dots,g_t}_+ 0$.*

The GB G for an ideal J can be computed using Buchberger's algorithm [5]. The algorithm, shown in Alg. 2, takes the set of polynomials $F = \{f_1, \dots, f_s\}$ as input and computes their GB $G = \{g_1, g_2, \dots, g_t\}$, such that $J = \langle F \rangle = \langle G \rangle$. Moreover, the polynomials of F and G have the same solution-set, i.e. $V(J) = V(\langle F \rangle) = V(\langle G \rangle)$.

In the algorithm,

$$Spoly(f_i, f_j) = \frac{L}{lt(f_i)} \cdot f_i - \frac{L}{lt(f_j)} \cdot f_j \tag{1}$$

where $L = LCM(lm(f_i), lm(f_j))$, and LCM denotes the least common multiple.

Algorithm 2 Buchberger's Algorithm

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Require: $F = \{f_1, \dots, f_s\}$
Ensure: $G = \{g_1, \dots, g_t\}$
1: $G := F$;
2: while $G' \neq G$ do
3:     $G' := G$
4:     for each pair $\{f_i, f_j\}, i \neq j$ in $G'$ do
5:         $Spoly(f_i, f_j) \xrightarrow{G'}_+ h$
6:         if $h \neq 0$ then
7:             $G := G \cup \{h\}$
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Ideal Membership Test: The above definition inherently provides a decision procedure to test for membership of a polynomial in an ideal: f is a member of an ideal J *if and only if* $f \xrightarrow{GB(J)}_+ 0$. When $f \notin J$, then division by $GB(J)$ results in a non-zero remainder r that is unique/canonical.

A Gröbner basis can be further reduced. A reduced Gröbner basis of J ($redGB(J)$) is a canonical representation of the ideal J.

Definition 3.2. *[Reduced Gröbner Basis]: A redGB for a polynomial ideal J is a GB $G = \{g_1, \dots, g_t\}$ such that:*

- *$lc(g_i) = 1, \forall g_i \in G$*
- *$\forall g_i \in G$, no monomial of g_i lies in $\langle lt(G - \{g_i\}) \rangle$*

Strong Nullstellensatz, Radical ideals, and Varieties: For any element $\varphi \in \mathbb{F}_q$, $\varphi^q = \varphi$ holds. Therefore, the polynomial $x^q - x$ vanishes everywhere in $\mathbb{F}_q$, and we call it a *vanishing polynomial.* We denote by $F_0 = \{x_1^q - x_1, \dots, x_d^q - x_d\}$ the set of all vanishing polynomials in R, and $J_0 = \langle F_0 \rangle$ denotes the ideal of all vanishing polynomials in R. Then, $V_{\mathbb{F}_q}(J_0) = V_{\overline{\mathbb{F}}_q}(J_0) = \mathbb{F}_q^d$. Moreover, given any ideal J, $V_{\mathbb{F}_q}(J) = V_{\overline{\mathbb{F}}_q}(J) \cap \mathbb{F}_q^d = V_{\overline{\mathbb{F}}_q}(J) \cap V_{\overline{\mathbb{F}}_q}(J_0) = V_{\overline{\mathbb{F}}_q}(J + J_0) = V_{\mathbb{F}_q}(J + J_0)$.

Definition 3.3. *[Ideal of vanishing polynomials]: Given an ideal $J \subset R$ and $V(J) \subseteq \mathbb{F}_q^d$, the ideal of polynomials that vanish on $V(J)$ is $I(V(J)) = \{f \in R : \forall \boldsymbol{a} \in V(J), f(\boldsymbol{a}) = 0\}$.*

If f vanishes on $V(J)$, then $f \in I(V(J))$.

Definition 3.4. *[Radical ideal]: For any ideal $J \subset R$, the radical of J is defined as $\sqrt{J} = \{f \in R : \exists m \in \mathbb{N}\ s.t. f^m \in J\}$.*

When $J = \sqrt{J}$, then J is called a *radical ideal*. Over algebraically closed fields, the *Strong Nullstellensatz* establishes the correspondence between radical ideals and varieties.

Definition 3.5. *[Maximal ideal]: An ideal $J \subset R$ is said to be maximal if $J \neq R$ and any ideal J' containing J is such that either $J' = J$ or $J' = R$.*

Lemma 3.1. *(From [11]) For an arbitrary ideal $J \subset \mathbb{F}_q[x_1, \ldots, x_d]$, and $J_0 = \langle x_1^q - x_1, \ldots, x_d^q - x_d \rangle$, the ideal $J + J_0$ is radical; i.e. $\sqrt{J + J_0} = J + J_0$.*

The Strong Nullstellensatz, which has a special form over finite fields, characterizes the ideal $I(V(J))$.

Theorem 3.1. *[The Strong Nullstellensatz over finite fields (Theorem 3.2 in [11])]: For any ideal $J \subset \mathbb{F}_q[x_1, \ldots, x_d]$, $I(V(J)) = J + J_0$.*

Reverse Topological Term Order: The computational complexity of the GB algorithm is exponential in the number of variables d. For efficient GB computations on polynomials derived from a circuit, [21] proposed the use of a specialized term order that exploits the topology of the circuit and renders the set of polynomials $F = \{f_1, \ldots, f_s\}$ for the gates of the circuit, a Gröbner basis itself. This term order '>' is called the *Reverse Topological Term Order (RTTO).*

Definition 3.6. *[Reverse Topological Term Order] [21]: Let C be an arbitrary combinational circuit. Let $\{x_1, \ldots, x_d\}$ denote the set of all variables (signals) in C. Starting from the primary outputs, perform a reverse topological traversal of the circuit and order the variables such that $x_k > x_j$ if x_k appears earlier in the reverse topological order. Impose a lex term order $>$ to represent each gate as a polynomial f_j, s.t. $f_j = x_k + tail(f_j)$. As each gate output is a distinct net, the leading terms of all polynomials in F become relatively prime. Then, the set of polynomials $F = \{f_1, \ldots, f_s\}$ corresponding to the gates of the circuit is a Gröbner basis when RTTO is used for ordering.*

Consequently, remainders generated by polynomial division using RTTO $>$ comprise only primary input variables. Our rectification approach also uses RTTO $>$ for polynomial representation and manipulation.

4 MODELING CIRCUITS WITH POLYNOMIAL IDEALS

A multivariate polynomial f over $\mathbb{F}_{2^n}$ is given as a specification, where n is the operand word-length (data-path size). A combinational circuit C is given as its implementation. The function implemented by C is modeled with a system of polynomials over $R = \mathbb{F}_{2^n}[Z, A, X]$, where X corresponds to all the bit-level variables (nets) in the circuit. Let $X_{PO} \subset X$, and $X_{PI} \subset X$ denote the set of all bit-level primary output variables, and primary input variables from C, respectively. Each internal gate is represented by a gate variable, and let $X_g \subset X$ denote the set of all such variables. Then, $X = X_{PO} \cup X_g \cup X_{PI}$. Further, $Z = \{z_0, \ldots, z_{n-1}\}$ and $A = \{a_0, \ldots, a_{n-1}\}$ represent the output and input operand words of the circuit, respectively, where $z_i \in X_{PO}$ and $a_i \in X_{PI}$.

The field $\mathbb{F}_{2^n}$ is constructed as $\mathbb{F}_{2^n} = \mathbb{F}_2[x] \pmod{P_n(x)}$, where $P_n(x)$ is the given primitive polynomial of degree n with γ as a root, i.e. $P_n(\gamma) = 0$. As C comprises Boolean logic gates, the gates are represented by polynomials $\pmod 2$, i.e. over $\mathbb{F}_2 (\subset \mathbb{F}_{2^n})$, using the mapping $\mathbb{B} \mapsto \mathbb{F}_2$:

$$\begin{aligned} z = \neg a &\implies z + a + 1; \\ z = a \wedge b &\implies z + a \cdot b; \\ z = a \vee b &\implies z + a + b + a \cdot b; \\ z = a \oplus b &\implies z + a + b; \end{aligned} \tag{2}$$

A circuit with n-bit operands is modeled as a polynomial function in $\mathbb{F}_{2^n}$. Algebraically, the correspondences between the bit-level and word-level variables of the circuit are represented as:

$$\begin{aligned} Z = z_0 + \gamma \cdot z_1 + \cdots + \gamma^{n-1} \cdot z_{n-1} &\implies Z + z_0 + \gamma \cdot z_1 + \cdots + \gamma^{n-1} \cdot z_{n-1}; \\ A = a_0 + \gamma \cdot a_1 + \cdots + \gamma^{n-1} \cdot a_{n-1} &\implies A + a_0 + \gamma \cdot a_1 + \cdots + \gamma^{n-1} \cdot a_{n-1}; \end{aligned} \tag{3}$$

Since $\mathbb{F}_2 \subset \mathbb{F}_{2^n}$, the polynomials in Eqn. (2) can also be interpreted as polynomials over $\mathbb{F}_{2^n}$. The advantage of working over $\mathbb{F}_{2^n}$ is that we can represent and manipulate both the bit-level and n-bit word-level polynomials in one unified domain, $\mathbb{F}_{2^n}$. We denote the set of polynomials $F = \{f_1, \ldots, f_s\} \subset R$ to represent these gate-level and bit-vector relations within circuit C. Let $J = \langle F \rangle$ be the ideal generated by this set. Let $F_0 = \{x_i^2 - x_i, Y^{2^n} - Y \ : \ x_i \in X,\ Y \in \{Z, A\}\}$ be the set of all vanishing polynomials, and $J_0 = \langle F_0 \rangle$ the corresponding ideal. Inclusion of ideal J_0 in the computations ensures that the nets in the circuit can only assume values in $\mathbb{F}_2$, and the variables Y only assume values in $\mathbb{F}_{2^n}$. Then, ideal $J + J_0 = \langle F + F_0 \rangle$ models the functionality of implementation C.

One can verify the correctness of the circuit C by checking if the given specification f is implied by the ideal representing C. In other words, $f \equiv C \iff f \xrightarrow{GB(J+J_0)}_+ 0$ [21]. It is shown in [21] that the Gröbner basis computation in the above procedure results in the same set even if vanishing polynomials for only the primary input variables, X_{PI}, are included in J_0. This stems from the fact that, over circuits, the evaluation of any non-primary input variables is a consequence of the assignment to primary input variables X_{PI}. Let $J_0^{X_{PI}} = \langle F_0^{X_{PI}} \rangle = \{x_i^2 - x_i \ : \ x_i \in X_{PI}\}$. Then, it is sufficient to perform $f \xrightarrow{GB(J+J_0^{X_{PI}})}_+ 0$? to check for the above ideal membership. For simplicity, it is assumed from hereon that $J_0 = \langle F_0 \rangle$ represents $J_0^{X_{PI}}$, unless specified otherwise.

Moreover, as described in Def. 3.6, imposition of RTTO $>$ renders the set of polynomials $F + F_0$ in itself a Gröbner basis. As a result, the expensive GB computation is avoided altogether, and the verification check reduces to that of polynomial division $f \xrightarrow{F+F_0}_+ r$, and checking whether $r = 0$.

In the manuscript, we use the circuit of Fig. 1, as a running example to demonstrate our algebraic approach for rectification.

Example 4.1. *The circuit C in Fig. 1 is a faulty implementation of a 3-bit (n=3) Mastrovito multiplier. The field $\mathbb{F}_{2^3}$ is constructed using $P_3(x) = x^3 + x + 1$ with γ as a root, i.e. $P_3(\gamma) = 0$. The specification polynomial is $f : Z + A \cdot B$, where Z is the output word, and A, B the input words. Impose RTTO $>$ on the polynomials, i.e. a lex term order on all polynomials with the variables of C ordered reverse topologically from primary outputs to primary inputs:*

$\{Z\} > \{A > B\} > \{z_0 > z_1 > z_2\} > \{d_0 > f_0 > e_2 > e_3\} > \{e_0 > e_1 > rr_0 > d_6 > d_7 > d_8\} > \{d_1 > d_2 > d_3 > r_0 > d_5 > rr_1\} > \{r_1 > rr_3 > rr_2\} > \{r_2 > r_3 > rr_4\} > \{r_4 > d_4\} > \{a_0 > a_1 > a_2 > b_0 > b_1 > b_2\}$.

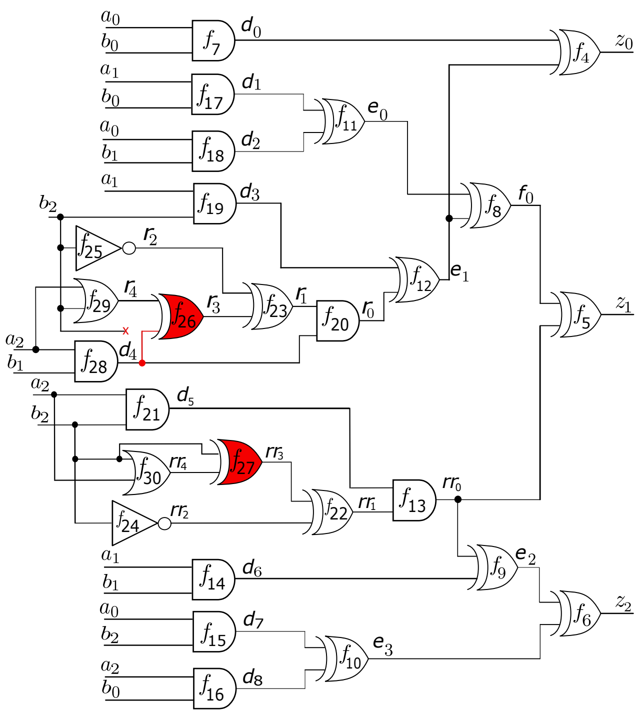

Fig. 1. A faulty implementation of the circuit C: a 3-bit finite field multiplier (n=3) with bugs introduced at net r_3 (AND gate replaced with an XOR gate and one of the inputs mis-connected to d_4 instead of b_2) and net rr_3 (AND gate replaced with an XOR gate).

Under RTTO $>$, the following polynomials represent C:

$$\begin{aligned}
f_1 &: Z + z_0 + \gamma \cdot z_1 + \gamma^2 \cdot z_2; & f_{16} &: d_8 + a_2 \cdot b_0;\\
f_2 &: A + a_0 + \gamma \cdot a_1 + \gamma^2 \cdot a_2; & f_{17} &: d_1 + a_1 \cdot b_0;\\
f_3 &: B + b_0 + \gamma \cdot b_1 + \gamma^2 \cdot b_2; & f_{18} &: d_2 + a_0 \cdot b_1;\\
f_4 &: z_0 + d_0 + e_1; & f_{19} &: d_3 + a_1 \cdot b_2;\\
f_5 &: z_1 + f_0 + rr_0; & f_{20} &: r_0 + r_1 \cdot d_4;\\
f_6 &: z_2 + e_2 + e_3; & f_{21} &: d_5 + a_2 \cdot b_2;\\
f_7 &: d_0 + a_0 \cdot b_0; & f_{22} &: rr_1 + rr_3 + rr_2;\\
f_8 &: f_0 + e_0 + e_1; & f_{23} &: r_1 + r_2 + r_3;\\
f_9 &: e_2 + rr_0 + d_6; & f_{24} &: rr_2 + b_2 + 1;\\
f_{10} &: e_3 + d_7 + d_8; & f_{25} &: r_2 + b_2 + 1;\\
f_{11} &: e_0 + d_1 + d_2; & f_{26} &: r_3 + r_4 + d_4;\\
f_{12} &: e_1 + d_3 + r_0; & f_{27} &: rr_3 + rr_4 + b_2;\\
f_{13} &: rr_0 + d_5 \cdot rr_1; & f_{28} &: d_4 + a_2 \cdot b_1;\\
f_{14} &: d_6 + a_1 \cdot b_1; & f_{29} &: r_4 + a_2 + b_2 + a_2 \cdot b_2;\\
f_{15} &: d_7 + a_0 \cdot b_2; & f_{30} &: rr_4 + a_2 + b_2 + a_2 \cdot b_2;
\end{aligned}$$

where the polynomials f_{26}, f_{27} correspond to the introduced bugs. Then $J = \langle F \rangle = \{f_1, f_2, \ldots, f_{30}\}$, $J_0 = \langle F_0 \rangle = \{a_0^2 - a_0, a_1^2 - a_1, a_2^2 - a_2, b_0^2 - b_0, b_1^2 - b_1, b_2^2 - b_2\}$. So, ideal $J + J_0 = \langle F + F_0 \rangle$ encapsulates the function implemented by C.

Computing $f : Z + A \cdot B \xrightarrow{F+F_0}_+ r$ results in $r = \gamma^2 \cdot (a_1a_2b_1b_2 + a_1a_2b_2 + a_2b_1b_2) + \gamma^1(a_1a_2b_1b_2 + a_1a_2b_2) + \gamma^0 \cdot (a_2b_1b_2)$. Since $r \neq 0$, the circuit is buggy.

5 RECTIFICATION CHECK

If verification results in a non-zero remainder r, then the circuit is deemed faulty and rectification needs to be performed to fix the circuit. We use the aforementioned polynomial ideal setup to *state and prove* whether or not the circuit can indeed be rectified at a given set of m targets. This check implies the *existence of a polynomial function* with mapping $u_i : \mathbb{F}_2^{|X_{PI}|} \rightarrow \mathbb{F}_2$, at individual targets w_i. Subsequently, we formulate the computation of rectification functions $U = \{u_1, \ldots, u_m\}$ by utilizing the outcome of this decision procedure. The computed polynomial functions when substituted at the corresponding targets, $w_i = u_i[X_{PI}]$, rectifies the circuit.

Let $W = \{w_1, \ldots, w_m\} \subset \{X_g, X_{PO}\}$ denote a given set of m candidate targets. Let $W_c = \{(0, 0, \ldots, 0), \ldots, (1, 1, \ldots, 1)\}$ represent the set of all $\{0, 1\}$-assignments to targets W. Here, $|W| = m$ and $|W_c| = 2^m$, with each $W_c[l]$, $1 \leq l \leq 2^m$, representing one set of assignments to targets W ($|W_c(l)| = m$). In other words, the tail of gate polynomials representing the targets are replaced by the corresponding $\{0, 1\}$-values from $W_c[l]$.

Theorem 5.1. **[Multi-fix Rectification Theorem]** *A specification polynomial f, a faulty circuit implementation C represented using the ideal $J + J_0 = \langle F + F_0 \rangle \subset R = \mathbb{F}_{2^n}[Z, A, X]$, and a set of targets W are given. RTTO $>$ is imposed on R. The following ideals are constructed:*

- $J_l = \langle F_l \rangle = \langle f_1, \ldots, f_{w_1} : w_1 + W_c[l][1], \ldots, f_{w_m} : w_m + W_c[l][m], \ldots, f_s \rangle$, *for* $1 \leq l \leq 2^m$.

Reduce f by $F_l + F_0$ to obtain remainders rem_l: $f \xrightarrow{F_l+F_0}_+ rem_l$, for $1 \leq l \leq 2^m$. Then, the faulty circuit C is rectifiable at the target set W ***if and only if***

$$\bigcup_{l=1}^{2^m} V(\langle rem_l \rangle) = \mathbb{F}_2^{|X_{PI}|} \tag{4}$$

Proof 5.1. *As rectification at target-set W makes C match f, f should be implied by the ideal J or f should vanish on $V(J)$. Moreover, each rem_l comprises only X_{PI} variables in its support. This is because RTTO $>$ ensures that each non-primary input variable (each gate output and word-level variable) appears as the leading term of some polynomial in F. Thus each non-primary input variable is canceled in the reduction $f \xrightarrow{F_l+F_0}_+ rem_l$. Furthermore, as X_{PI} take values in $\mathbb{F}_2$, $x^2 = x, \forall x \in X_{PI}$. Hence, $V(rem_l) \subseteq \mathbb{F}_2^{|X_{PI}|}$. Thus, the rectification theorem can be equivalently stated as: "f vanishes on $V(J) \iff \bigcup_{l=1}^{2^m} V(\langle rem_l \rangle) = \mathbb{F}_2^{|X_{PI}|}$".*

(i) **To prove "$\Rightarrow$"**: *Let $x_{PI} \in \mathbb{F}_2^{|X_{PI}|}$ be an assignment to the primary input variables of C. Every assignment x_{PI} results in a corresponding assignment x_{int} to rest of the variables in C. For each such point $(x_{PI}, x_{int}) \in \mathbb{F}_{2^n}$, the set of m targets W evaluate to one set of possible $\{0, 1\}$ assignment from W_c. When the m-targets in W evaluate to $W_c[1] = (0, 0, \ldots, 0)$, $J_1 = \langle F_1 \rangle$ vanishes on the point (x_{PI}, x_{int}). Likewise, $J_2 = \langle F_2 \rangle$ vanishes on (x_{PI}, x_{int}) when the targets evaluate to $W_c[2] = (0, 0, \ldots, 1)$, and so on. Since $f \xrightarrow{F_l \cup F_0}_+ rem_l, 1 \leq l \leq 2^m$, and f vanishes on the point (x_{PI}, x_{int}) to begin with, we obtain that for every primary input assignment x_{PI}, one of the rem_l vanishes. This implies that $\bigcup_{l=1}^{2^m} V(\langle rem_l \rangle) = \mathbb{F}_2^{|X_{PI}|}$.*

(ii) **To prove "$\Leftarrow$"**: *Say there exists an assignment to the primary inputs $x_{PI} \in \mathbb{F}_2^{|X_{PI}|}$ such that rem_1 vanishes on x_{PI}, i.e. $rem_1(x_{PI}) = 0$. For the given point x_{PI}, the rest of the variables of C get a corresponding assignment x_{int}. As $f \xrightarrow{F_1 \cup F_0}_+ rem_1$, we have that f is a member of the ideal $J_1 + J_0 + \langle rem_1 \rangle$. Therefore, when $rem_1(x_{PI}) = 0$, the ideal J_1 also vanishes on $(x_{PI}, x_{int}) \in \mathbb{F}_{2^n}$ because the point (x_{PI}, x_{int}) is a valid evaluation of the circuit. Further, J_0 by definition vanishes everywhere in R. This implies that $f(x_{PI}, x_{int}) = 0$. The argument similarly holds for each rem_l vanishing on some x_{PI}. This proves that for all primary inputs, if any $rem_l : 1 \le l \le 2^m$ vanishes, then f vanishes too; and that completes the proof.*

As described before, due to RTTO >, each rem_l comprises only X_{PI} variables in its support. Moreover, we have that $J_0 = \langle F_0 \rangle = \{x_i^2 - x_i : x_i \in X_{PI}\}$. As the union of varieties corresponds to the variety of the product of the ideals (Table 1), the expression for $\bigcup_{l=1}^{2^m} V(\langle rem_l \rangle)$ can be rewritten as:

$$\begin{aligned}\bigcup_{l=1}^{2^m} V(\langle rem_l \rangle) =& V(\langle rem_1 \rangle) \cup V(\langle rem_2 \rangle) \cup \cdots \cup V(\langle rem_{2^m} \rangle)\\ =& V(\langle rem_1 * rem_2 * \cdots * rem_{2^m} \rangle)\\ =& V_{\overline{\mathbb{F}}_q}(\langle rem_1 * rem_2 * \cdots * rem_{2^m} \rangle + J_0)\\ =& V_{\mathbb{F}_q}(\langle rem_1 * rem_2 * \cdots * rem_{2^m} \rangle + J_0)\end{aligned}$$

Therefore, to check for rectification at the set of targets W, the test "Is $\bigcup_{l=1}^{2^m} V(rem_l) = \mathbb{F}_2^{|X_{PI}|}$" can be performed by checking if $\prod_{l=1}^{2^m} rem_l \xrightarrow{J_0}_+ 0$.

Example 5.1. *Continuing Ex. 4.1, we demonstrate the rectification check for $W = \{w_1, w_2\} = \{r_3, rr_3\}$.*

Constructing the J_l ideals:

- $J_1 = \langle F_1 \rangle$, *where* $F_1[f_{26} : r_3 + 0], F_1[f_{27} : rr_3 + 0], (r_3 = 0, rr_3 = 0)$
- $J_2 = \langle F_2 \rangle$, *where* $F_2[f_{26} : r_3 + 0], F_2[f_{27} : rr_3 + 1], (r_3 = 0, rr_3 = 1)$
- $J_3 = \langle F_3 \rangle$, *where* $F_3[f_{26} : r_3 + 1], F_3[f_{27} : rr_3 + 0], (r_3 = 1, rr_3 = 0)$
- $J_4 = \langle F_4 \rangle$, *where* $F_4[f_{26} : r_3 + 1], F_4[f_{27} : rr_3 + 1], (r_3 = 1, rr_3 = 1)$

Reducing the Spec $f : Z + A \cdot B$ modulo these ideals, we get:

- $rem_1 = f \xrightarrow{F_1+F_0}_+ (\gamma + 1)a_2b_1b_2 + (\gamma^2 + \gamma)a_2b_2$
- $rem_2 = f \xrightarrow{F_2+F_0}_+ (\gamma + 1)a_2b_1b_2$
- $rem_3 = f \xrightarrow{F_3+F_0}_+ (\gamma + 1)a_2b_1b_2 + a_2b_1 + (\gamma^2 + \gamma)a_2b_2$
- $rem_4 = f \xrightarrow{F_4+F_0}_+ (\gamma + 1)a_2b_1b_2 + a_2b_1$

When we compute $\prod_{l=1}^{2^m} rem_l \xrightarrow{J_0}_+$, we obtain remainder 0, thus confirming that the target set $W = \{r_3, rr_3\}$ indeed admits correction.

6 CHARACTERIZING RECTIFICATION FUNCTIONS

We now show how to utilize the above rectifiability check setup to characterize the rectification functions. Intuitively, Theorem. 5.1 can be elaborated as follows. In each ideal J_l, the polynomials representing the targets from W are replaced by the corresponding values from $W_c[l]$. Subsequently, the specification polynomial f is reduced by each ideal $J_l + J_0$ to produce corresponding remainder

rem_l. The variety of rem_l, for any l, corresponds to the set of all assignments to primary inputs X_{PI} (minterms) where the specification f agrees with the implementation C. Thus, the condition of Theorem. 5.1 implies that every minterm in the input space is contained in the union of varieties of each rem_l. Therefore, for every minterm from the input space, there exists an assignment $W_c[l]$ to target set $W = \{w_1, \dots, w_m\}$ where f and C match. Consequently, there exists a set of individual rectification functions $U = \{u_1, \dots, u_m\}$ with individual function mapping $u_i : \mathbb{F}_2^{|X_{PI}|} \longrightarrow \mathbb{F}_2$ for each targets w_i that can be computed to rectify every error minterm.

To illustrate the characteristics of the hitherto unknown rectification functions U, consider the special case of rectification formulation at a single target ($m = 1$). It follows that:

$$W = \{w_1\},\ U = \{u_1\},\ and\ W_c = \{(0), (1)\}$$

$$f \xrightarrow{F_1+F_0}_+ rem_1,\ where,\ F_1[f_{w_1} : w_1 + 0]\ or\ w_1 = 0$$

$$f \xrightarrow{F_2+F_0}_+ rem_2,\ where,\ F_2[f_{w_1} : w_1 + 1]\ or\ w_1 = 1$$

Suppose that the application of Theorem. 5.1 at net w_1 ascertains that $rem_1 * rem_2 \xrightarrow{J_0}_+ 0$, implying that C admits rectification at w_1. Consider the following observations:

- $V(rem_1)$ consists of all the points (minterms) where w_1 is assigned 0 and the circuit evaluation matches the specification evaluation.
- $V(rem_2)$ consists of all the points (minterms) where w_1 is assigned 1 and the circuit evaluation matches the specification evaluation.
- $V(rem_1) \cap V(rem_2)$ consists of all the points (minterms) where w_1 is assigned 0 (rem_1) or 1 (rem_2) and the circuit evaluation matches the specification evaluation.

From the proof of Theorem. 5.1, we know that the entire input space is contained in the union of points (minterms) from $V(rem_1)$ and $V(rem_2)$. The proof implies that there *exists a polynomial function* $u_1 \in \mathbb{F}_2[X_{PI}]$ with mapping $u_1 : \mathbb{F}_2^{|X_{PI}|} \longrightarrow \mathbb{F}_2$ at target w_1, that rectifies the circuit C. As $w_1 = u_1$ rectifies the circuit at net w_1, consider the following statements:

(1) Polynomial function u_1 should vanish on $V(rem_1)$, in other words should evaluate to 0 at least on $V(rem_1)$.
(2) Polynomial function u_1 should not vanish on $V(rem_2)$, in other words should evaluate to non-zero values at least on $V(rem_2)$.
    - However, since u_1 can only evaluate in $\mathbb{F}_2$, we can rephrase this statement as: u_1 should evaluate to 1 on $V(rem_2)$.
(3) Polynomial function u_1 evaluates to 0 or 1 for points in $V(rem_1) \cap V(rem_2)$.

We know that the remainders rem_1 and rem_2 contain only X_{PI} variables in its support and collectively encapsulates points (minterms) where specification agrees with the implementation. Clearly, we can consider the remainders rem_1 and rem_2 for characterizing and evaluating the function u_1.

In logic synthesis terms, the sets $V(rem_1)$, $V(rem_2)$, and $V(rem_1) \cap V(rem_2)$ are the OFF-set, ON-set, and DC-set, respectively, for the rectification function. In the sequel (Sec. 8) we show how to utilize the remainder polynomials rem_l to synthesize a patch sub-circuit.

7 RECTIFICATION FUNCTION EVALUATION FOR MULTIPLE TARGETS

Thm. 5.1 determines whether there exists a set of polynomial functions $U = \{u_1, \dots, u_m\}$ such that substituting every patch function u_i as the *tail* at its respective target w_i, for $i = 1, \dots, m$, makes C functionally equivalent to specification.

For a given set of targets W, due to the presence of don't cares (DC), there may exist more than one set U of rectification functions that rectify the circuit. Exploring all the DC conditions for m targets might be computationally infeasible; we present two different approaches to overcome this. First, we present an approach to evaluate an on- and off-set for each rectification function by greedily resolving all the DC conditions. Following this, we present an approach to heuristically explore and evaluate a subset of the DC conditions, along with on- and off-sets for each rectification function.

7.1 Rectification Function Evaluation using Greedy Approach

To illustrate the greedy approach, consider the case with $m = 2$ ($W = \{w_1, w_2\}$), where $W_c = \{(0,0), (0,1), (1,0), (1,1)\}$, and we must compute rectification functions u_1 and u_2 corresponding to targets w_1 and w_2, respectively. For brevity, let $V_{W_c[l]} = V(\langle rem_l \rangle)$, for $1 \leq l \leq 2^m$; in this case, $V_{W_c[1]} = V_{(0,0)} = V(\langle rem_1 \rangle)$, $V_{W_c[2]} = V_{(0,1)} = V(\langle rem_2 \rangle)$, and so on.

Recall that $V_{(0,0)}$ comprises the set of points where the specification matches the implementation under the assignments $w_1 = w_2 = 0$ to the targets. This implies that at these points, the rectification functions u_1 and u_2 should evaluate to 0. Table 2 shows the required evaluations of u_1 and u_2 for the points in each variety, following the same reasoning, assuming each $V_{W_c[l]}$ is pairwise disjoint. The on (off)-set of the rectification function for a target corresponds to the union of the varieties where the function evaluates to 1 (0). In this case, the on- and off-sets of u_1 consist of the set of points in $V_{(1,0)} \cup V_{(1,1)}$ and $V_{(0,0)} \cup V_{(0,1)}$, respectively. Similarly, the on- and off-set of u_2 comprise points in $V_{(0,1)} \cup V_{(1,1)}$ and $V_{(0,0)} \cup V_{(1,0)}$. The functions u_1 and u_2 could be synthesized using these sets.

Table 2. Required rectification function evaluations

Variety	u_1	u_2
$V_{(0,0)}$	0	0
$V_{(0,1)}$	0	1
$V_{(1,0)}$	1	0
$V_{(1,1)}$	1	1

However, the above argument is only correct when each $V_{W_c[l]}$ is pairwise disjoint, which may not be true in practice. For example, for a point contained in $V_{(0,0)} \cap V_{(0,1)}$, (u_1, u_2) may evaluate either to $(0,0)$, or to $(0,1)$ in order for the implementation to evaluate to the same value as the specification; this point would be in both the on- and off-set of u_2 in the method previously described. A decision procedure is necessary to determine the evaluation of (u_1, u_2) at these intersections unambiguously. *We present a greedy approach that resolves such ambiguities by imposing an order on the sets.*

An example of our greedy approach to evaluate (u_1, u_2) for an order $V_{(0,0)} > V_{(0,1)} > V_{(1,0)} > V_{(1,1)}$ is as follows: First, we place all the points from $V_{(0,0)}$ into the off-sets of (u_1, u_2). Next, we place all the points from $V_{(0,1)} \setminus V_{(0,0)}$ into the off-set of u_1 and the on-set of u_2. We perform the set difference to avoid placing the points in $V_{(0,0)} \cap V_{(0,1)}$ into both the on-set and off-set of u_2. Next, we place all the points from $V_{(1,0)} \setminus (V_{(0,0)} \cup V_{(0,1)})$ into the on-set of u_1, and the off-set of u_2. Finally, we place the remaining points from $V_{(1,1)} \setminus (V_{(0,0)} \cup V_{(0,1)} \cup V_{(1,0)})$ into the on-set of (u_1, u_2). The resulting on- and off-sets for u_1 and u_2 are shown below.

$$\begin{aligned}
V(u_{1_{on}}) &= (V_{(1,1)} \setminus (V_{(0,0)} \cup V_{(0,1)} \cup V_{(1,0)})) \cup (V_{(1,0)} \setminus (V_{(0,0)} \cup V_{(0,1)}))\\
V(u_{1_{off}}) &= (V_{(0,0)}) \cup (V_{(0,1)} \setminus V_{(0,0)})\\
V(u_{2_{on}}) &= (V_{(0,1)} \setminus V_{(0,0)}) \cup (V_{(1,1)} \setminus (V_{(0,0)} \cup V_{(0,1)} \cup V_{(1,0)}))\\
V(u_{2_{off}}) &= (V_{(0,0)}) \cup (V_{(1,0)} \setminus (V_{(0,0)} \cup V_{(0,1)}))
\end{aligned}$$

This approach with the given order greedily places points into the off-sets of the rectification functions (u_1, u_2) where possible and only place points into the on-sets of the rectification functions when necessary. Subject to the given order, the on-sets of the rectification functions are thus minimized. For the experiments in this paper, we always use the order $V_{W_c[i]} > V_{W_c[j]}$ for $i < j$, as in the above example, though any order would yield valid rectification functions.

Generalizing our greedy approach for m targets, we first construct the following composite sets (varieties):

$$S_l = \begin{cases} V_{W_c[1]}, & \text{if } l = 1 \\ V_{W_c[l]} \setminus (\bigcup_{j=1}^{l-1} V_{W_c[j]}), & 2 \leq l \leq 2^m \end{cases} \tag{5}$$

The resulting on-set and off-set functions for each target i, where $1 \leq i \leq m$ are:

$$\begin{aligned}
V(u_{i_{on}}) &= \bigcup S_l, \ \forall l \mid W_c[l][i] = 1\\
V(u_{i_{off}}) &= \bigcup S_l, \ \forall l \mid W_c[l][i] = 0
\end{aligned} \tag{6}$$

7.2 Notion of Don't Cares at Multiple Targets

Although the greedy approach yields a correct rectification function, it does not compute any Don't Care (DC) conditions but instead heuristically assigns points to the off-set when possible at the intersections of varieties. DC conditions can be exploited to synthesize efficient patch functions. In this section, we explore the sets of points where DC conditions appear and propose an approach to systematically compute a subset of these DC points for each target.

Let $U_d \subseteq U$ denote a subset of the target rectification functions. We are interested in the DC conditions which arise for these functions at points where they may evaluate to any value, for some fixed evaluation of the remaining functions in the set $\{U \setminus U_d\}$. For example, consider a point in $V_{(0,0)} \cap V_{(0,1)}$ for a circuit with two targets. As discussed previously, u_1 must evaluate to 0 at this point, but $U_d = \{u_2\}$ may evaluate either to 0 or to 1, so this is a *DC* point for u_2.

Not every intersection of varieties yields *DC* points which follow the conditions described above. Consider a point in $V_{(0,0)} \cap V_{(1,1)}$. Here, (u_1, u_2) must evaluate either to $(0, 0)$ or to $(1, 1)$. If this point were assigned to the *DC* set of u_2, for example, the specification and implementation would only evaluate the same if u_1 evaluated to the same value as u_2. Thus, u_1 would become a function of u_2 at this point. This point cannot be placed into the on-set, off-set, or DC-set of u_1 before u_2 is evaluated. To avoid inter-dependencies between the rectification functions, we do not classify points in such intersections as *DC* points. We rely on our greedy heuristic to evaluate these points. In contrast, in the previous case, $u_1 = 0$ and $u_2 = DC$ for a point in $V_{(0,0)} \cap V_{(0,1)}$.

Finally, consider a point in $V_{(0,0)} \cap V_{(0,1)} \cap V_{(1,0)}$. This point cannot be a DC point for both targets simultaneously since the evaluation $(1, 1)$ here will result in an incorrect rectification function. However, because $V_{(0,0)} \cap V_{(0,1)} \cap V_{(1,0)} \subset V_{(0,0)} \cap V_{(0,1)}$, we could treat this point as a *DC* point for u_2 and evaluate u_1 to 0. Alternatively, because $V_{(0,0)} \cap V_{(0,1)} \cap V_{(1,0)} \subset V_{(0,0)} \cap V_{(1,0)}$, we could treat this point as a *DC* point for u_1 and evaluate u_2 to 0. Thus, we have a choice to place this point in the *DC*-set of either target, but not both.

Finding every intersection containing *DC* points for every target can be very expensive for circuits with more than a few targets. We, therefore, propose an approach to compute a subset of the *DC* points by considering only the set of pairwise intersections of varieties that contain *DC* points for exactly one target, denoted as DC_{pair}.

Let $d(W_c[j], W_c[k])$ denote the Hamming distance between the two sets of assignments to the targets $W_c[j]$ and $W_c[k]$. We compute the set of varieties which contain *DC* points for one target, denoted DC_{pair}, from the equation below, where $1 \leq j, k \leq 2^m$.

$$DC_{pair} = \{V_{W_c[j]} \cap V_{W_c[k]} \mid d(W_c[j], W_c[k]) = 1\} \tag{7}$$

Since the Hamming distance $d = 1$ between the assignments $W_c[j]$ and $W_c[k]$ for each intersection of varieties in DC_{pair}, exactly one rectification function may evaluate either to 0 or to 1. The remaining rectification functions require fixed evaluations of 1 or 0. Therefore, each intersection of varieties in DC_{pair} yields *DC* points for exactly one rectification function in U, and either on- or off-set points for the remaining rectification functions in U. We use DC_{pair} to compute the *DC* points for each rectification function, as described below.

7.3 Rectification Function Evaluation utilizing Don't Care Conditions

Once the set DC_{pair} has been found, a few steps remain to compute the on-, off-, and don't-care sets for each target. First, we follow an approach identical to the greedy approach to evaluate points outside of DC_{pair}. We construct new composite sets S_l^d for $1 \leq l \leq 2^m$, which are identical to the composite sets (varieties) created for the previous approach, except that all the points from DC_{pair} set are removed.

$$S_l^d = \begin{cases} V_{W_c[1]} \setminus DC_{pair}, & \text{if } l = 1 \\ V_{W_c[l]} \setminus ((\bigcup_{j=1}^{l-1} V_{W_c[j]}) \cup DC_{pair}), & 2 \leq l \leq 2^m \end{cases} \tag{8}$$

Points in these composite sets are assigned to the on- and off-set for each rectification function in the same way as Eqn. (6), substituting S_l with S_l^d. Next, we place the points in DC_{pair} in the on-, off-, or *DC* sets for each rectification function by imposing an order on the intersections and resolving them as explained in the following example.

Given a circuit with two targets, $DC_{pair} = \{V_{(0,0)} \cap V_{(0,1)}, V_{(0,0)} \cap V_{(1,0)}, V_{(0,1)} \cap V_{(1,1)}, V_{(1,0)} \cap V_{(1,1)}\}$. We impose the order $V_{(0,0)} > V_{(0,1)} > V_{(1,0)} > V_{(1,1)}$. We place the points in $V_{(0,0)} \cap V_{(0,1)}$ into the off-set of u_1 and the *DC* set of u_2. We then place the points in $V_{(0,0)} \cap V_{(1,0)} \setminus V_{(0,0)} \cap V_{(0,1)}$ into the *DC* set of u_1 and the off-set of u_2. We place points in $V_{(0,1)} \cap V_{(1,1)} \setminus ((V_{(0,0)} \cap V_{(0,1)}) \cup (V_{(0,0)} \cap V_{(1,0)}))$ into the *DC* set of u_1 and the on-set of u_2. Finally, we place points in $V_{(1,0)} \cap V_{(1,1)} \setminus ((V_{(0,0)} \cap V_{(0,1)}) \cup (V_{(0,0)} \cap V_{(1,0)}) \cup (V_{(0,1)} \cap V_{(1,1)}))$ into the on-set of u_1 and the *DC* set of u_2. Following this approach, we calculate on- off- and *DC* sets for each rectification function.

8 SYNTHESIZING RECTIFICATION FUNCTIONS

The above techniques show how to construct a rectification function by reasoning about the varieties of remainders rem_l, $1 \leq l \leq 2^m$. However, algebraically, we compute these functions using their corresponding ideals. In this section, we show how the ideals corresponding to the remainders computed in Theorem 5.1 can be utilized for rectification function computation.

Consider the remainders rem_l ($\langle rem_l \rangle \subseteq \mathbb{F}_{2^n}[X_{PI}]$) computed in Theorem 5.1. Since we use a polynomial model over $\mathbb{F}_{2^n}$, the remainders rem_l computed using our algebraic rectification techniques may evaluate to non-Boolean values (non-synthesizable). In other words, each rem_l is a polynomial function with mapping of the form $f : \mathbb{F}_2^{|X_{PI}|} \mapsto \mathbb{F}_{2^n}$. However, we are interested in operating on synthesizable functions in order to derive a patch sub-circuit. To achieve this, we present techniques to transform a polynomial function of the form rem_l to another polynomial p_{G_l} such that $V(\langle rem_l \rangle) = V(\langle p_{G_l} \rangle)$, and p_{G_l} is a function with mapping of the form $f : \mathbb{F}_2^{|X_{PI}|} \mapsto \mathbb{F}_2$.

Consider an ideal $J \subseteq R = \mathbb{F}_q[x_1, \dots, x_d]$ and let $J_0 = \{x_i^q - x_i : 1 \leq i \leq d\}$. Given that ideals of the form $J + J_0$ contain a finite variety, and that they are radical, results from algebraic geometry show:

Fact 8.1. *The ideal $J + J_0$ can be expressed as the intersection of maximal ideals. For radicals, the intersection is the same as their product: $J + J_0 = \bigcap_{i=1}^k M_i = \prod_{i=1}^k M_i$, where M_i are maximal in R. Furthermore, each maximal ideal M_i is of the form $M = (x_1 - \epsilon_1, \dots, x_d - \epsilon_d)$, where $\epsilon_j \in \mathbb{F}_2, \forall 1 \leq j \leq d$.*

Proposition 8.1. *The ideal $\prod_{i=1}^k M_i$ can be expressed as generators $(f_1, \dots, f_s, J_0)$ such that $f_1, \dots, f_s$ have coefficients only in $\mathbb{F}_2$.*

The above observations imply that any arbitrary polynomial $f \in R$, when combined with J_0, can be expressed as $\langle f \rangle + J_0 = \langle g_1, \dots, g_t, J_0 \rangle$, where $g_1, \dots, g_t$ have coefficients in $\mathbb{F}_2$. It is a property of such ideals $(\langle f \rangle + J_0)$ that the generators of their reduced Gröbner bases (Def. 3.2) have coefficients only in $\mathbb{F}_2$.

Proposition 8.2. *Given a set of generators $G = \{g_1, \dots, g_t\}$ with coefficients only in $\mathbb{F}_2$, a polynomial p can always be constructed as $p = ((1 + g_1)(1 + g_2) \dots (1 + g_t) + 1)$, such that $V(\langle p \rangle) = V(\langle g_1, \dots, g_t \rangle + J_0)$ and p evaluates to values in $\mathbb{F}_2$.*

It is easy to assert that $V(\langle p \rangle) = V(G)$. Consider a point $\boldsymbol{a} \in V(G)$. As all of $g_1, \dots, g_t$ vanish (= 0) at $\boldsymbol{a}$,

$$\begin{aligned} p(\boldsymbol{a}) &= (1 + g_1(\boldsymbol{a}))(1 + g_2(\boldsymbol{a})) \cdots (1 + g_t(\boldsymbol{a})) + 1 \\ &= (1 + 0)(1 + 0) \cdots (1 + 0) + 1 = 0 \end{aligned}$$

Conversely, for a point $\boldsymbol{a'} \notin V(G)$, at least one of $g_1, \dots, g_t$ will evaluate to 1. Without loss of generality, if g_1 evaluates to 1 at $\boldsymbol{a'}$, then $p = (1 + 1)(1 + 0) \cdots (1 + 0) + 1 = 1 \neq 0$. In addition to $V(\langle p \rangle) = V(G)$, p either evaluates to 0 or 1.

Even though the remainders rem_l have coefficients in $\mathbb{F}_{2^n}$ (higher field), their varieties are in $\mathbb{F}_2^{|X_{PI}|}$ ($V(\langle rem_l \rangle) \subseteq \mathbb{F}_2^{|X_{PI}|}$) as they correspond to bit-level assignments to X_{PI}. We have that $I(V(\langle rem_l \rangle)) = \langle rem_l \rangle + J_0$ (Theorem 3.1). Let $G_l = redGB(\langle rem_l \rangle + J_0)$ denote the generators of the reduced Gröbner basis computation for a given rem_l. This, in turn implies that for any point in $\mathbb{F}_2^{|X_{PI}|}$, each generator of G_l will either evaluate to 0 or 1.

We utilize the above facts and reduced GB computation to construct a synthesizable Boolean function p_{G_l} from a polynomial function rem_l. Consequently, the rectification function operations are restricted to algebraic computations in $\mathbb{F}_2[X_{PI}] \equiv \mathbb{B}$.

To compute the patch u_i, we perform the following steps:

- Compute reduced Gröbner bases G_l of $\langle rem_l, J_0 \rangle$ for each rem_l.
- Construct a singleton polynomial p_{G_l} such that $V(p_{G_l}) = V(\langle rem_l, J_0 \rangle)$.
- Impose an order on the sets for DC_{pair} and composite set computations.
- Compute DC_{pair} using Eqn. (7), and then obtain the composite sets in Eqn. (8) which are then assigned to DC-, on- and off-sets of the rectification functions (Sec. 7.2).

- In order to perform the variety union, intersection, and difference operations, we use ideal product, sum, and colon operations, respectively, on the singleton polynomial p_{G_l} representation of the ideal.
- The above procedure delivers $u_{i_{DC}}$ and $u_{i_{on}}$ as singleton polynomials in $\mathbb{F}_2[X_{PI}]$. Translate $u_{i_{DC}}$ and $u_{i_{on}}$ into Boolean functions by interpreting the product, sum, and '+1' as Boolean AND, XOR, and INV gates, respectively. Optimize the on-set $u_{i_{on}}$ w.r.t. to the DC-set $u_{i_{DC}}$.

EXAMPLE 8.1. *Continuing with Ex. 5.1:*

- $rem_3 = (\gamma + 1)a_2b_1b_2 + a_2b_1 + (\gamma^2 + \gamma)a_2b_2$
- $G_3 = redGB(\langle rem_3, J_0\rangle) = \{a_2b_1, a_2b_2\}$
- $p_{G_3} = (1 + a_2b_1) * (1 + a_2b_2) + 1 = a_2b_1b_2 + a_2b_1 + a_2b_2$
  - *Here,* $V(p_{G_3}) = V(\langle rem_3, J_0\rangle)$
- *Similarly:*
  - $p_{G_1} = a_2b_2$
  - $p_{G_2} = a_2b_1b_2$
  - $p_{G_4} = a_2b_1b_2 + a_2b_1$

The rectification polynomials for the targets (r_3, rr_3) computed using the greedy approach (Sec. 7.1)

$$u_{1_{on}} = a_2b_1b_2; \qquad u_{1_{off}} = a_2b_1b_2 + 1; \qquad r_3 = u_{1_{patch}} = (a_2 \wedge b_1 \wedge b_2);$$
$$u_{2_{on}} = a_2b_2; \qquad u_{2_{off}} = a_2b_2 + 1; \qquad rr_3 = u_{2_{patch}} = (a_2 \wedge b_2).$$

The rectification polynomials for the targets (r_3, rr_3) computed using the on-set and don't care simplification (Sec. 7.3)

$$u_{1_{dc}} = a_2b_1b_2 + a_2b_2; \qquad u_{1_{on}} = a_2b_1b_2; \qquad r_3 = u_{1_{patch}} = a_2 \wedge b_2;$$
$$u_{2_{dc}} = a_2b_2 + 1; \qquad u_{2_{on}} = a_2b_2; \qquad rr_3 = u_{2_{patch}} = 1.$$

9 EFFICIENCY IMPROVEMENT USING ZDDS

The techniques described in rectification check and function computation predominantly involve Gröbner basis computations and polynomial reductions. By virtue of RTTO >, the complexity of remainder (rem_l) generation in the rectification check was moved from one of computing GB to that of GB-reduction by way of multivariate polynomial division. However, the function computation operation also involves computing a reduced GB, which can be especially prohibitive when applied to circuits with large size operands. Hence, there is a need for efficient representation to overcome the infeasibility of these operations using conventional computer algebra tools.

As the GB algorithms are employed to compute rectification function patches via remainders generated from the circuit, we analyze the circuit and its topology to derive specific information, which we use to guide the computation of patches efficiently. Moreover, we further show how our ZDD based algorithms can effectively utilize this information to compute rectification patches. By combining our theories and algorithms, we can explore the space of all possible rectification functions through their ON-set, OFF-set, and DC-set of corresponding Boolean functions.

In this regards, we take inspiration from [17] and utilize PolyBori's [4] reduction procedure with ZDDs [24, 25] as the underlying data structure to improve our proposed approach. PolyBori proposed the use of ZDDs to compute Gröbner bases for Boolean polynomials. PolyBori is a generic Boolean GB computational engine that caters to many permissible term orders. Its division algorithm is also generally based on the conventional concept of canceling one monomial in every step of reduction. In contrast, our algorithms are tailored for GB-reduction under the RTTO > . The efficiency of our approach stems from the observation that the RTTO > imposes a special structure on the ZDDs, which allows for multiple monomials to be canceled in one division-step, along with

Table 3. Time is in seconds; I = Benchmark Index, n = Datapath Size, m = target word size, AM = Maximum resident memory utilization in Mega Bytes (Average across benchmarks), #G = Number of gates $\times 10^3$, , #BO = Number of faulty outputs, PBS = Required time for PolyBori setup (ring declaration/poly collection/spec collection), RC = Required time for verification, multi-fix setup and rectifiability check, GFC = Required time for function computation using the greedy approach, DFC = Required time for function computation with don't cares

				Mastrovito						Montgomery						Point Addition					
I	*n*	*m*	AM	#G	#BO	PBS	RC	GFC	DFC	#G	#BO	PBS	RC	GFC	DFC	#G	#BO	PBS	RC	GFC	DFC
1	**16**	5	100	0.8	6	0.05	0.01	1.7	4.7	0.9	16	0.05	0.44	190	277*	0.9	7	0.07	0.02	6.6	20
2	**32**	5	120	2.8	8	0.14	0.02	2	8	2.8	32	0.16	0.1	114	180*	2.9	13	0.2	0.06	36	85*
3	**64**	3	160	11.2	5	0.61	3.59	5	15	9.6	47	0.53	0.14	7	14	10.6	64	0.8	0.18	10	35
4	**96**	2	240	24.5	5	1.45	0.12	0.4	0.7	21	96	1.35	3.14	87	111*	24.8	96	2.53	0.5	7.7	90
5	**128**	2	370	43.2	5	3.23	0.24	0.8	1.2	35.8	128	2.92	2.06	28	393*	43.2	128	6.42	4.38	49	62*
6	**163**	5	550	69.8	6	6.21	0.4	4.4	7.7	57.5	128	5.38	1.53	131	220*	71.6	22	15.9	1.53	3.2	8
7	**233**	2	750	119	3	12.7	0.66	0.3	1.7	112	233	12.6	2.69	6	40	122	233	19.7	1.44	6.4	32
8	**409**	2	2400	384	2	190	2.22	0.3	9	340	409	136	6.15	2.7	5.2	368	409	224	5.3	7.7	8*
9	**571**	2	5000	827	5	2143	5.96	0.3	26	663	427	1386	49	1.6	30	813	5	2492	13.2	1.2	20

simplifying the search for divisors. The efficiency is derived by treating the polynomials as unate cube sets and checking isomorphism between the implementation and specification graphs.

10 EXPERIMENTAL RESULTS

The benchmark suit includes two modular multipliers (Mastrovito and Montgomery), and a circuit that performs Point Addition over NIST standard Elliptic curves. These benchmarks are taken from [21] and synthesized using the *abc* tool with a gate library comprising two input gates. Table 3 presents the results of our approach when performing MFR against their respective polynomial specifications. We introduce bugs by means of gate and wiring modifications in the synthesized netlists such that multiple output bits are affected in the design (column #BO). We introduce multiple such modifications at various topological levels: some closer to PIs, some in the middle of the circuit, and some near POs. In our experiments, the number of targets is chosen from $m = \{2, 3, 5\}$. Our approach isn't limited by this set m and can perform MFR for any given number of targets.

Our approach is implemented as a custom software in Python programming language. We use PolyBori's [4] ZDD based API to implement the division, $f \xrightarrow{F_l' \cup F_0'}_+ rem_l$, $1 \leq l \leq 2^m$. Subsequently, the remainders generated from these divisions are utilized in the decision procedure, as well as the function computations. Further, we use *sis* [31] and *abc* [3] to perform logic optimization and synthesis. Specifically, in *sis* we run a script to perform *kernel extraction* and *full simplify* to optimize the rectification functions computed in Sec.7.2. We use *abc* to perform *structural hashing, balancing, refactoring, rewriting, etc.*. Finally, we *map* the computed functions using a library of AND-XOR-INV gates and extract the synthesis results for *area* and *delay*. The experiments are performed on a 3.5GHz Intel(R) Core$^{\text{TM}}$ i7-4770K Quad-Core CPU with 32 GB RAM.

Table 3 presents the characteristics of the benchmark suit and the execution time for the computations using our approach. Column PBS denotes the time taken to build the respective ZDD models (commensurates with the operand word-length n). Execution time for rectification check (RC) and function computation (GFC and DFC) depend on various factors such as: i) the number of bugs; ii) the number of targets; iii) location of the bugs; iv) location of the targets; v) the number of affected outputs; and vi) size of the patch function being computed in terms of number of gates. Collectively, these factors decide the size of the remainder rem_l, and the number of remainders l. We omit the comparison with the contemporary approaches as they fail (timeout = 3 hrs) to rectify circuits beyond 16-bits, which is the smallest benchmark from our results table.

Table 4 presents the synthesis results post *abc* mapping for GFC and DFC approaches in terms of area (number of gates) and the longest topological delay. The asterisk (*) in the DFC columns denotes the cases where *full simplify* (*sis*) fails to utilize the pairwise intersection don't care network for the on-set function simplification. In these cases, *sis* aborts simplification as the BDD size exceeds 480,000 nodes. For these entries, the patch functions are synthesized using *abc* which ignores the don't care network. The time taken for GFC is less than the time taken for DFC computations. However, synthesis results computed using DFC where *sis* completed simplification successfully are of better quality than the one computed using GFC for most of the cases.

Table 4. Synthesis results for mapped patch network; I = Benchmark Index, GFC = Greedy function computation, DFC-on = Function computation with don't care optimization of on-set, DFC-off = Function computation with don't care optimization of complement of off-set, A = Area in terms of number of gates , D = Longest delay

	Mastrovito						Montgomery						Point Addition					
	GFC		DFC-on		DFC-off		GFC		DFC-on		DFC-off		GFC		DFC-on		DFC-off	
I	A	D	A	D	A	D	A	D	A	D	A	D	A	D	A	D	A	D
1	19	3	17	3			27788	50	27941*	62*			761	40	265	12		
2	34	5	35	4			19340	65	19384*	57*			8882	69	9063*	60*		
3	1675	29	1577	46			1511	30	560	18			3040	32	3733	41		
4	86	11	21	5			55085	50	55568*	52*			6642	89	6193	70		
5	283	21	103	12			25819	44	26744*	35*			27544	36	27289*	35*		
6	222	17	99	7			27035	68	27409*	61*			66	8	39	7		
7	9	4	9	4			8094	25	4948	28			4345	30	5169	34		
8	16	4	11	4			844	13	4	2			2707	24	2611*	23*		
9	21	7	18	6			299	19	287	19			622	22	210	16		

11 CONCLUSION

This paper presents an automated symbolic computer algebra approach to perform MFR of faulty finite field arithmetic circuits at a given set of targets. Our approach reasons about the rectification functions by means of algebraic varieties in finite fields, and computes these functions using Gröbner bases of ideals corresponding to the circuit. We present two MFR approaches, a heuristic which greedily tries to resolve the rectification functions for the targets, and a variety intersection heuristic that explores a subset of don't cares condition for the target functions. Our approach is able to compute rectification functions for circuits with large (NIST-standard) operand widths n.

As part of future work, we are working on function computation in terms of internal nets. Further, we are also investigating the extension of this approach to integer arithmetic circuits.

REFERENCES

[1] W. W. Adams and P. Loustaunau. 1994. *An Introduction to Gröbner Bases.* American Mathematical Society.

[2] E. Biham, Y. Carmeli, and A. Shamir. 2008. Bug Attacks. In *Proceedings on Advances in Cryptology*. 221–240.

[3] Robert Brayton and Alan Mishchenko. 2010. ABC: An Academic Industrial-strength Verification Tool. In *Computer Aided Verification (CAV)*. Springer, 24–40.

[4] M. Brickenstein and A. Dreyer. 2009. PolyBoRi: A framework for Gröbner-basis computations with Boolean polynomials. *Journal of Symbolic Computation* 44 (2009), 1326–1345.

[5] B. Buchberger. 1965. *Ein Algorithmus zum Auffinden der Basiselemente des Restklassenringes nach einem nulldimensionalen Polynomideal.* Ph.D. Dissertation. University of Innsbruck.

[6] Ai Quoc Dao, Nian-Ze Lee, Li-Cheng Chen, Mark Po-Hung Lin, Jie-Hong R. Jiang, Alan Mishchenko, and Robert Brayton. 2018. Efficient Computation of ECO Patch Functions. In *Design Automation Conference (DAC)*. ACM, 51:1–51:6.

[7] Wolfram Decker, Gert-Martin Greuel, Gerhard Pfister, and Hans Schönemann. 2016. Singular 4-1-0 — A computer algebra system for polynomial computations. http://www.singular.uni-kl.de.

[8] F. Farahmandi and P. Mishra. 2016. Automated Test Generation for Debugging Arithmetic Circuits. In *Design, Automation Test in Europe Conference Exhibition (DATE)*.

[9] F. Farahmandi and P. Mishra. 2017. Automated Debugging of Arithmetic Circuits Using Incremental Gröbner Basis Reduction. In *International Conference on Computer Design (ICCD)*. 193–200.

[10] M. Fujita. 2015. Toward Unification of Synthesis and Verification in Topologically Constrained Logic Design. *Proc. IEEE* (2015).

[11] S. Gao, A. Platzer, and E. Clarke. 2011. Quantifier Elimination over Finite Fields with Gröbner Bases. In *Intl. Conf. Algebraic Informatics*.

[12] A. M. Gharehbaghi and M. Fujita. 2017. A new approach for selecting inputs of logic functions during debug. In *International Symposium on Quality Electronic Design (ISQED)*. 166–173.

[13] K. Gitina, S. Reimer, M. Sauer, R. Wimmer, C. Scholl, and B. Becker. 2013. Equivalence Checking of Partial Designs Using Dependency Quantified Boolean Formulae. In *IEEE International Conference on Computer Design (ICCD)*. 396–403.

[14] U. Gupta. 2020. *Rectification of Finite Field Arithmetic Circuits with Craig Interpolation using Algebraic Geometry.* Ph.D. Dissertation. University of Utah.

[15] U. Gupta, I. Ilioaea, V. Rao, A. Srinath, P. Kalla, and F. Enescu. 2018. On the Rectifiability of Arithmetic Circuits using Craig Interpolants in Finite Fields. In *International Conference on Very Large Scale Integration (VLSI-Soc)*. 49–54.

[16] U. Gupta, P. Kalla, I. Ilioaea, and F. Enescu. 2019. Exploring Algebraic Interpolants for Rectification of Finite Field Arithmetic Circuits with Groebner Bases. In *24th IEEE European Test Symposium (ETS)*. 1–6.

[17] Utkarsh Gupta, Priyank Kalla, and Vikas Rao. 2019. Boolean Gröbner Basis Reductions on Finite Field Datapath Circuits Using the Unate Cube Set Algebra. *IEEE Trans. CAD (TCAD)* (2019).

[18] Y. Kimura, A. M. Gharehbaghi, and M. Fujita. 2019. Signal Selection Methods for Efficient Multi-Target Correction. In *IEEE International Symposium on Circuits and Systems (ISCAS)*. 1–5.

[19] V. N. Kravets, N. Lee, and J. R. Jiang. 2019. Comprehensive Search for ECO Rectification Using Symbolic Sampling. In *Design Automation Conference (DAC)*. 1–6.

[20] C. C. Lin, K. C. Chen, S. C. Chang, and M. Marek-Sadowska. 1995. Logic Synthesis for Engineering Change. In *Proc. Design Automation Conf. (DAC)*. 647–652.

[21] J. Lv, P. Kalla, and F. Enescu. 2013. Efficient Gröbner Basis Reductions for Formal Verification of Galois Field Arithmetic Circuits. In *IEEE Trans. on CAD (TCAD)*. 1409–1420.

[22] K. Magons. 2016. Applications and Benefits of Elliptic Curve Cryptography. In *International Conference on Current Trends in Theory and Practice of Computer Science (SOFSEM)*.

[23] Alireza Mahzoon, Daniel Große, and Rolf Drechsler. 2018. Combining Symbolic Computer Algebra and Boolean Satisfiability for Automatic Debugging and Fixing of Complex Multipliers. In *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. 351–356.

[24] Shin-ichi Minato. 1993. Zero-suppressed BDDs for Set Manipulation in Combinatorial Problems. In *Design Automation Conference (DAC)*. 272–277.

[25] Shin-ichi Minato. 1994. Calculation of Unate Cube Set Algebra Using Zero-suppressed BDDs. In *Design Automation Conference (DAC)*. 420–424.

[26] Vikas Rao. 2018. http://eng.utah.edu/~utkarshg/cex.pdf,.

[27] V. Rao, U. Gupta, A. Srinath, I. Ilioaea, P. Kalla, and F. Enescu. 2018. Post-Verification Debugging and Rectification of Finite Field Arithmetic Circuits using Computer Algebra Techniques. In *Formal Methods in Computer-Aided Design*

(FMCAD). 1–9.

[28] V. Rao, I. Ilioaea, H. Ondricek, P. Kalla, and F. Enescu. 2021. Word-Level Multi-Fix Rectifiability of Finite Field Arithmetic Circuits. In *International Symposium on Quality Electronic Design (ISQED)*. To Appear.

[29] V. Rao, H. Ondricek, P. Kalla, and F. Enescu. 2021. Computing Rectification Functions for Finite Field Arithmetic Circuits using Computer Algebra Techniques. In *ACM Great Lakes Symposium on VLSI (GLSVLSI)*. To Appear.

[30] C. Scholl and B. Becker. 2001. Checking Equivalence for Partial Implementations. In *Design Automation Conference (DAC)*.

[31] E. Sentovich *et al.* 1992. *SIS: A System for Sequential Circuit Synthesis.* Technical Report UCB/ERL M92/41. ERL, Dept. of EECS, Univ. of California, Berkeley.

[32] A. Smith, A. Veneris, M. F. Ali, and A. Viglas. 2005. Fault Diagnosis and Logic Debugging using Boolean Satisfiability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2005).

[33] K. F. Tang, P. K. Huang, C. N. Chou, and C. Y. Huang. 2012. Multi-patch Generation for Multi-error Logic Rectification by Interpolation with Cofactor Reduction. In *Design, Automation Test in Europe Conference Exhibition (DATE)*. 1567–1572.

[34] P. Tuyls and L. Batina. 2006. RFID-Tags for Anti-counterfeiting. In *Topics in Cryptology – CT-RSA 2006*. 115–131.

[35] B. H. Wu, C. J. Yang, C. Y. Huang, and J. H. R. Jiang. 2010. A Robust Functional ECO Engine by SAT Proof Minimization and Interpolation Techniques. In *International Conference on Computer-Aided Design (ICCAD)*. 729–734.

[36] H. T. Zhang and J. H. R. Jiang. 2018. Cost-Aware Patch Generation for Multi-Target Function Rectification of Engineering Change Orders. In *Design Automation Conference (DAC)*. 1–6.