Research Progress

Vikas Rao

Awards and Recognitions

- Publication [7]: Best Paper Award Nominee
- Publication [10]: Best Paper with Student as First Author Award
- 2017 Design Automation Conference A. Richard Newton Young Student Fellowship
- 2020 Design Automation Conference Ph.D. Forum Presentation

Experience

- Research and Development Intern, Synopsys, Fall 2019

  - Responsibility involved research and evaluation of the state-of-the-art techniques to address Datapath verification problems and to subsequently apply these learnings towards enhancing the Hector Data Path Solver (HDPS) engine.
  - Worked on development and integration of a prototype polynomial solver to verify integer multipliers.

Publications

- **Book Chapter**

  [1] U. Gupta, I. Ilioaea, V. Rao, A. Srinath, P. Kalla, and F. Enescu, “Rectification of Arithmetic Circuits with Craig Interpolants in Finite Fields,” in *VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms. Springer International Publishing*, Jun 2019, vol. 561, pp. 79–106.

- **Journals**

  [2] U. Gupta, P. Kalla, and V. Rao, “Boolean Gröbner Basis Reductions on Finite Field Datapath Circuits Using the Unate Cube Set Algebra,” in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Mar 2019, vol. 38, no. 3, pp.576–588.

  [3] V. Rao, H. Ondricek, P. Kalla, “Word-level Multi-fix Rectification of Finite Field Arithmetic Circuits”, Due Submission to *ACM Transactions on Design Automation of Electronic Systems,* 2021.

- **Refereed Conference Proceedings**

  [4] V. Rao, H. Ondricek, P. Kalla, F. Enescu, “Rectification of Arithmetic Circuits using Computer Algebra Techniques”, Due submission to *ACM Transactions on Design Automation of Electronic Systems (ACM-TODAES)*, 2021.

  [5] V. Rao, H. Ondricek, P. Kalla, F. Enescu, “Rectification of Integer Arithmetic Circuits using Computer Algebra Techniques”, Due submission to *International Conference on Computer Design (ICCD)*, 2021.

  [6] V. Rao, H. Ondricek, P. Kalla, F. Enescu, “Algebra Techniques for rectification of finite field circuits”, Due notification – *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2021.

  [7] V. Rao, H. Ondricek, P. Kalla, F. Enescu, “Word-level Multi-Fix Rectification of Finite Field Arithmetic Circuits using Computer Algebra Techniques”, Due notification - *International Workshop on Logic and Synthesis (IWLS)*, 2021.

  [8] V. Rao, I. Ilioaea, H. Ondricek, P. Kalla, F. Enescu, “Word-level Multi-fix Rectifiability of Finite Field Arithmetic Circuits”, *International Symposium on Quality Electronic Design (ISQED)*, 2021.

  [9] V. Rao, U. Gupta, I. Ilioaea, A. Srinath, P. Kalla, and F. Enescu, “Post-Verification Debugging and Rectification of Finite Field Arithmetic Circuits using Computer Algebra Techniques,” in *Formal Methods in Computer Aided Design (FMCAD)*, Oct 2018, pp. 1–9.

  [10] U. Gupta, I. Ilioaea, V. Rao, A. Srinath, P. Kalla, and F. Enescu, “On the Rectifiability of Arithmetic Circuits using Craig Interpolants in Finite Fields,” in *IFIP/IEEE International Conference on Very Large-Scale Integration (VLSI-SOC)*, Oct 2018, pp. 49–54.

  [11] V. Rao, Utkarsh Gupta, I. Ilioaea, P. Kalla, F. Enescu, “Resolving Unknown Components in Arithmetic Circuits Using Computer Algebra Methods”, *International Workshop on Logic and Synthesis (IWLS)*, Jun 2018.

  [12] U. Gupta, I. Ilioaea, P. Kalla, F. Enescu, V. Rao, and A. Srinath, “Craig Interpolants in Finite Fields using Algebraic Geometry: Theory and Applications,” in *Intl. Workshop on Logic and Synthesis (IWLS)*, Jun 2018, pp. 70–77.

  [13] U. Gupta, P. Kalla, and V. Rao, “Boolean Gröbner Basis Reductions on Datapath Circuits Using the Unate Cube Set Algebra,” in *26th International Workshop on Logic & Synthesis (IWLS)*, Jun 2017, pp. 124–131.