Research Progress

Utkarsh Gupta

Awards

- Publication [1]: Best Paper award nominee.
- Publication [2]: Best Paper with Student as First Author award.
- 2017 IWLS Travel Grant.
- 2015 DAC A. Richard Newton Young Student Fellowship.

Experience

- Formal Verification Intern, Apple, Summer 2019.
  - Planned, developed, and executed FV on RTL design which is part of error handling in Apple microprocessor cache.
  - FV environment provided high confidence on correctness of relevant logic and resulted in interesting corner case bugs discoveries in the early stage of design cycle.
- Formal Verification Intern, Intel, Summer 2018.
  - Gained hands-on experience verifying System Verilog RTL designs using state of the art FV tools and methodology.
  - Developed a formal verification plan and used it for verifying floating point arithmetic components of Intel AI Processors.
  - Formally verified industrial grade FIFO to be used in Intel's next generation High Performance Computing Chips.

Publications

[1] U. Gupta, I. Ilioaea, V. Rao, A. Srinath, P. Kalla, and F. Enescu, "On the Rectifiability of Arithmetic Circuits using Craig Interpolants in Finite Fields," in *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC)*, Oct 2018, pp. 49–54.

[2] U. Gupta, P. Kalla, and V. Rao, "Boolean Gröbner Basis Reductions on Datapath Circuits Using the Unate Cube Set Algebra," in *26th International Workshop on Logic & Synthesis*, June 2017, pp. 124–131.

[3] U. Gupta, I. Ilioaea, V. Rao, A. Srinath, P. Kalla, and F. Enescu, "Rectification of Arithmetic Circuits with Craig Interpolants in Finite Fields," in *VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms*. Springer International Publishing, Jun 2019, vol. 561, pp. 79–106.

[4] U. Gupta, P. Kalla, I. Ilioaea, and F. Enescu, "Exploring Algebraic Interpolants for Rectification of Finite Field Arithmetic Circuits with Groebner Bases," in *24th IEEE European Test Symposium (ETS)*, May 2019, pp. 1–6.

[5] U. Gupta, I. Ilioaea, P. Kalla, F. Enescu, V. Rao, and A. Srinath, "Craig Interpolants in Finite Fields using Algebraic Geometry: Theory and Applications," in *Intl. Workshop on Logic and Synthesis (IWLS)*, June 2018, pp. 70–77.

[6] U. Gupta, P. Kalla, and V. Rao, "Boolean Gröbner Basis Reductions on Finite Field Datapath Circuits Using the Unate Cube Set Algebra," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 38, no. 3, pp. 576–588, Mar 2019.

[7] V. Rao, U. Gupta, I. Ilioaea, A. Srinath, P. Kalla, and F. Enescu, "Post-Verification Debugging and Rectification of Finite Field Arithmetic Circuits using Computer Algebra Techniques," in *2018 Formal Methods in Computer Aided Design (FMCAD)*, Oct 2018, pp. 1–9.