ECE/CS 6770 – Homework Assignment 3

1. Following are first order equations for leakage:

   - $P_{off} = W_{tot} V_{dd} I_{off}$
   - $I_{off} = I_0^{(-\frac{qV_t}{mkT})}$

   Describe how these parameters dictate process based leakage control, and which of these parameters a designer can effect to produce lower leakage designs.

2. Following equations that represent delay down a wire based on the operating regime that it is in:

   - RC
   - $\frac{L}{R}$
   - $\sqrt{LC}$

   Describe these regimes. Which regime do we commonly design in on a digital integrated circuit?

   For short, intermediate, and long wire lengths, which of these regimes would give the lowest latency?

3. How do speed paths and races affect yield and performance of a design? What is the difference between a race and speed path?

4. What is clock skew? What is clock jitter?

5. Identify a number of clock deskew strategies and how they would be implemented on a large design such as a microprocessor.

6. Active power is represented as $P = CV^2 f$. What are some design approaches to reduce power?

7. How is clock gating implemented? what are some advantages and drawbacks that is poses?

8. What is MCF? How does it affect the waveform of a victim wire?

9. What is the algorithm used for static timing analysis? What is the algorithm used for dynamic timing analysis?

10. What are the OCV, AOCV, and POCV algorithms used in static timing analysis? Why would we use them?

11. How can leakage be reduced by design approaches?

12. Does the body effect dictate leakage? How?

13. What is hot carrier injection? How does it change design performance? What is the time scale for these changes?

14. How does DIBL effect the power of a design?

15. What are the time constants for reaching a low leakage state with

16. How would one determine a set of vectors that would put a circuit into a low leakage state?

17. T or F: Is a NAND gate higher leakage than an inverter of the same drive strength?

18. How does one implement "dark silicon"? What are the considerations?

19. How can one modify V_t and V_{dd} to optimize performance or power? How would one modify voltage and threshold to get a higher performance chip? How would one modify them to get lower power at the same performance?

20. How does transistor threshold affect timing and leakage? How would one design with multiple thresholds, or controllable thresholds to optimize both performance and leakage?

21. Can one create transistors with multiple thresholds? If it cold be done, how would a gate be optimized in such a case to improve power and reduce leakage?

22. Are all metal layers in an advanced process designed with the same metal? Are they designed with the same width, height, and spacing rules? Why or why not?

23. What are the design considerations for the return path of a transmission line?

24. Describe inductance and mutual inductance.

25. Why is skin effect a bigger issue when operating in the transmission line regime?

26. What happens when a signal operating in the transmission line regime moves from a segment that has higher impedance to a segment that has lower impedance?

27. What are design techniques to reduce coupling? How do the do so? Which methods are easier to implement? Which produce the best result (most speedup at lowest design cost)?

28. Which is the most accurate model for wire delay: L, π, or T? How many segments of a π and L model accurately models a wire with about 5% accuracy?

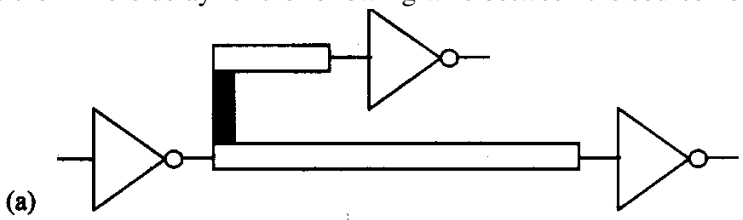
29. Calculate the delay of a 10,000 μm M3 wire that has 0.2 fF per μ and 0.04 Ω per square.

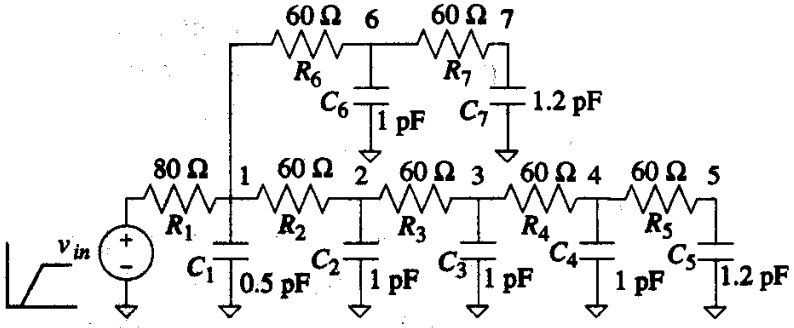
30. What is the delay for a 5,000 μm wire on the same chip?

31. Calculate the delay if spacing between adjacent wires doubles for the 10 mm long wire.

32. Calculate the delay if the wire width doubles for the 10 mm long wire.

33. Calculate the Elmore delay for the following wire between the source node and node 7.





34. Can wire delay be greater than transistor delay in a design? How?