ECE/CS 6770 – Homework Assignment 1

1. What is the fundamental transistor area scaling value used based on Moore's law?
2. What are the primary advantages of Moore's law?
3. What is the equation for I_{DSat}?
4. Using the equation from the previous question, which parameter best reduces power in a design? What is the performance cost of that parameter?
5. What are the three parameters from the above equation that are generally under a designer's control?
6. What is the fundamental problem with the gate insulator which has caused us to move to different materials?
7. What is the purpose of strained silicon? How does it affect design performance?
8. What is the ideal transistor structure?
9. Why did the channel length being being reduced at a faster rate than the technology "node" starting with about the 250nm process node?
10. Name three important changes in materials or processing that have enabled us to continue constant field scaling since the 250nm node.
11. Define constant field scaling in terms of the three fundamental assumptions that it enforces. How do each of these scale?
12. Name several ways that actual scaling has varied from "ideal" constant field scaling theory.
13. Define DIBL. Why do we care about it
14. What does the acronym CMOS stand for? Has it been an accurate description of the process that we have been using lately? Why or why not?
15. What is one material being used for gate insulator in modern process technologies?
16. What is the gate materials being used in modern process technologies?
17. Why is there a limit to the thickness of the gate insulator?
18. Why has voltage scaling historically been significantly less than constant field scaling dictates?
19. What are several disadvantages to the way voltage scaling has been applied?
20. What is the relationship between performance, V_{dd}, and V_{th}?
21. How does current scale as voltage drops above threshold?

22. How does current scale as voltage drops below threshold?

23. How can one increase performance by adjusting transistor threshold?

24. Why have channel doping profiles changed as transistors are scaled?

25. What is the body effect?

26. Does the body effect become worse or better with scaling? Why?

27. Does body effect limit the number of transistors that can be placed in series stacks? If so, why?

28. What are hot carriers, and how do I get some?

29. What is the equation for dynamic power in a chip?

30. What is the equation for leakage power?

31. If I have a design that operates at 500MHz in a 240nm process node, consumes 5W of power, and has an area of 537k mm^2, what should this design look like in a 32nm node?

32. If the DEC Alpha 21164 processor was shrunk using the theory of constant field scaling, what would it's clock frequency, area, and power be at a 32nm node? (50W @ 300MHz, 500nm process, 300mm^2)

33. Do the analysis above for the Sun UltraSparc III. (70W @ 600MHz, 250nm, 360mm^2).

34. If you were to purchase a 32nm scaled DEC Alpha 21164 or Sun UltraSparc III, which would you buy and why?

35. The nominal voltage for a 180nm process is 1.8V. I have a 180 nm design that operates at 250MHz with 40W using 0.9V power supply and each operation takes 1000ns to complete. What is the energy per operation e?

36. Calculate $e\tau^2$ for the above design, where τ is considered the time to complete one operation.

37. I have a 65nm design that operates at 1.2GHz at 1V at 50mW. It completes an operation in one microsecond. What is the energy to perform this operation?

38. If I scale the voltage in the above design to 500mV, what should be the resulting power, time, and energy to complete the operation?

39. What is the $e\tau$ and $e\tau^2$ values for the above design operating at 1V and 500mV respectively? (τ is the time to complete the operation.)

40. Two different low power designs for the same problem are reported. One used voltage scaling in the results, and the other did not. How would you best calculate which is the lowest power design?