ECE/CS 6770 – Lab Assignment 9

Due 4 May 2017 via Canvas

1 Introduction

During the course of this class you have studied many of the second order effects that cause our integrated circuits to operate outside of the "digital" or "clocked" domains where devices operate as predictive discrete voltages and delays. We have also performed some lab experiments to build efficient designs, perform robust and scripted design flows to improve productivity, and research and understand some transistor effects. In this lab you will perform a short research experiment to study an effect of your choosing.

2 Research Study

For this last lab, you will choose an effect that you can design or simulate that relates in some form to a topic we discussed in class.

Following is a short list of examples of what you might want to perform. They introduce how you might set up your experiment.

1. Find the definition of the metal stack for a process. Determine from the spice files or other documentation the resistance and capacitance of the metal layers. Determine the effect of length on the delay of the different wires. Run a set of simulations and graph the delay of the wires ranging from short wires to long wires. The results should look something like the graph shown in the lectures.

2. Study the effect of swizzling on the delay of a bus. Determine appropriate drivers and loads for the system. Model the coupling effects on a bus of four wires. Create a switching pattern where one signal rises, one falls, and two remain stable. Model the capacitance as a single capacitor between adjacent wires. Configure the signals changing that result in the largest coupling delay on the wires. Now emulate swizzling by splitting each capacitance into smaller components that couple to other wires to model wire swizzling. Run a spice simulation and show the difference in coupling and delay down the wires. Determine the reduction in delay based on swizzling.

3. Study the effect of delay when driving different loads. Evaluate the delay through an inverter chain as the loads increase from a fan-out of one to a fan-out of 8. Compare this to the delay that is predicted with the logical effort equations. Does the delay scale linearly as predicted by logical effort?

4. Emulate the effect of process variation on a pair of inverters. Use one inverter as the reference model as was done in the MIS lab, and provide an appropriate load. Compare the effect of variation on delay of the inverter against the reference model. Modify the threshold of the second devices by copying the models of the pmos and nmos transistors (naming them pmos2 and nmos2 or something similar) and modifying the threshold

voltage of the transistors in the copied models. Report on the variation, and describe and justify the amount of threshold variation that you used for the comparison.

Following are some more mini projects ideas with less detail. The setup and test methods are not described in as much detail as above. Make sure you have correctly configured your mini research project to achieve the desired results, and that the result is not biased by other effects.

1. Leakage based on series transistor stacks and input voltage values.

2. Transistor structure difference. For example, can legging be used to reduce the variation in delay between the two inputs in a NAND gate?

3. Determine the "kick-back" capacitance onto a dynamic node. For example, create a domino inverter that drives a NAND gate with fanout of 5 or 6. Drive the output of the domino gate and then put the gate in a tristate mode. Switch the other input of the NAND gate, and see what effect it has on the dynamic gate output. Study the difference in kick-back coupling depending on which input the dynamic gate is tied.

4. Study the difference in delay as temperature is changed. This can be done by modifying the temperature models in a spice file.

5. Study how the delay of a static gate changes as voltage is reduced. Reduce the voltage down into the subthreshold region. Report on the change in delay at that inflection point.

6. Study the effect of rise and fall times in the switching energy of a circuit. This will be simulated based on fanout load and drive strength. Have one transistor drive another where the second transistor has a nominal (FO4) fanout, to a *very* large fanout – say FO27. To compare the effects, change the size of first transistor rather than the second.

7. Build a four deep clocked FIFO and an asynchronous FIFO. Compare the two designs in terms of energy and latency.

8. Redo lab 1 again by designing a dynamic gate implementation of the function given in that lab. Compare the results of the dynamic gate with that of your original design.

9. Measure the effect on a flip-flop if the setup time is not obeyed. Walk a switching data signal across the clock signal and measure the difference in output delay. You will need to use spice for this evaluation as Verilog simulators will not model this effect.

10. Measure the difference between the delay and power of NAND gates and NOR gates. Measure the difference as this varies from 2 to 4 inputs.

11. Evaluate the change in performance as you change the back body bias of the transistors in an inverter.

12. Measure the power and delay difference between gates where the pmos and nmos transistors have the same drive strength versus a different skew ratio. Look in the spice model file, and find the transistor gain. If the gain ratio is 3:1, then make a four-deep inverter chain with pmos transistors 3× the size of the nmos transistors. Compare this for power and delay of a low skewed inverter chain where the pmos transistors are sized 2× the size of the nmos transistors.

13. Pick some other effect that you would like to investigate.

3 Project Details and Requirements

Make sure you pick a project that is well defined and that can be performed with a similar effort that was required for the previous labs. Don't pick something that will take too much time, or that is too simple and trivial.

Most of the tests will involve running spice, although that is not a requirement of the mini project. Feel free to pick something at the system or architecture level so long as it can be easily measured. If you do use spice, remember that the `.measure` command will help you collect results.

You will be graded on the engineering quality and setup of your project, and the quality of the results and reports. One good method for this is to pretend that you are in a work environment. Pretend that you will be using what you are investigating in a design, and that the quality of the team project depends on these results, and that you need to report your results to the rest of your team! The report should describe the results in sufficient detail to other team members on your project that they can proceed with their work based on your results. Make sure the reports are clear and concise, and directly report the results. This will usually be with plots or tables.

Many of these project will require you to compare what you are studying against a reference design. If this is the case, make it easy to show by graphing the results *in the same plot*, putting the results in a table, etc.

Depending on the project, you may be more productive if you script your study and allow the script to step through the data to run simulations and collect results.

4 Deliverables

Pick one of the examples to study above, or talk to the instructor if you have a different idea for a study. Turn in your data and report via canvas.

Include in a README file the following. Also tar up with the README other files used in your study including graph or waveforms that are needed to show your results results as png or image files. Include any necessary files for your project such as the circuit, spice control files, model files if you modified them, Verilog files, scripts, etc.

- Describe the project you selected and what you expected to observe.
- Describe your project setup. What did you need to do to perform your test? Describe how you measured the results and if you performed scripting.
- Describe your results.
- Describe the importance of your effect on design. Note if this an effect that could be exploited to improve a design for power or performance.