Homework Assignment 6

CS/ECE 6810: Computer Architecture

April 11, 2018

Main Memory

Due Date: 4/18/2018

(90 points)

Important Notes:

- Solutions turned in must be your own. Please, mention references (if any) at the end of each question. Please refrain from cheating.
- All solutions must be accompanied by the equations used/logic/intermediate steps and assumptions. Writing only the final answer will receive **zero** credit.
- All units must be mentioned wherever required.
- Late submissions (**after 11:59 pm on 04/18/2018**) will not be accepted
- All submissions must be in PDF only. Scanned copies of handwritten solutions will not be accepted as a valid submission.

1. Memory Scheduling Mechanisms (20 points)

For the following memory access pattern, estimate when each memory access completes for two different scheduling mechanisms: **open-page policy** and **close-page policy**. You are allowed to reorder requests already waiting in the memory controller. The access pattern only specifies the row being touched. All accesses are to the **same** bank. Assume that bus latencies are zero. Assume that the bank is already pre-charged at time 0. Assume that pre-charge takes 20 ns, loading a row buffer takes 20 ns, and cache line transfer to output pins also takes 20 ns.

Row being accessed	Arrival time at memory controller	Open-page	Close-page
X	10 ns		
X	70 ns		
Y	90 ns		
X	100 ns		
Y	180 ns		

2. Memory System Design (20 points)

Modern systems have processors with four memory channels. Assume that a memory channel has 64 bits for data and 24 bits for address and command. Assume that a memory channel is connected to eight x8 memory chips. Consider a new memory system that shrinks the data bus of the memory channel to 32 bits. Assume that such a channel would be connected to four x8 memory chips. Mention **two pros** and **two cons** of the new memory system (Be very concise).

3. Virtually Indexed Physically Tagged Cache (20 points)

Assume that the OS uses a minimum page size of 4 KB. Assume that your L1 cache must be 8-way set-associative. If you're trying to correctly implement a virtually indexed physically tagged cache (with no additional support from the OS), what is the largest L1 cache that you can design?

4. DRAM Control (10 points)

Express the latency of a memory load as a function of tRAS, tRP, tRCD, tCL in the following situations:

i. The correct row is already placed in the row buffer
ii. Another row is already placed in the row buffer.

5. DRAM Control Tasks – Request Scheduling (20 points)

Find the total number of commands sent by an in-order command scheduler for the given sequence of memory addresses for reads, using the following address mapping scheme:

Address = row(12):bank(3):rank(1):channel(0):column(16)
Assume that all banks are initially precharged.

Addresses: 00040108
01040101
00161804
01040104