OUT-OF-ORDER LOADS/STORES

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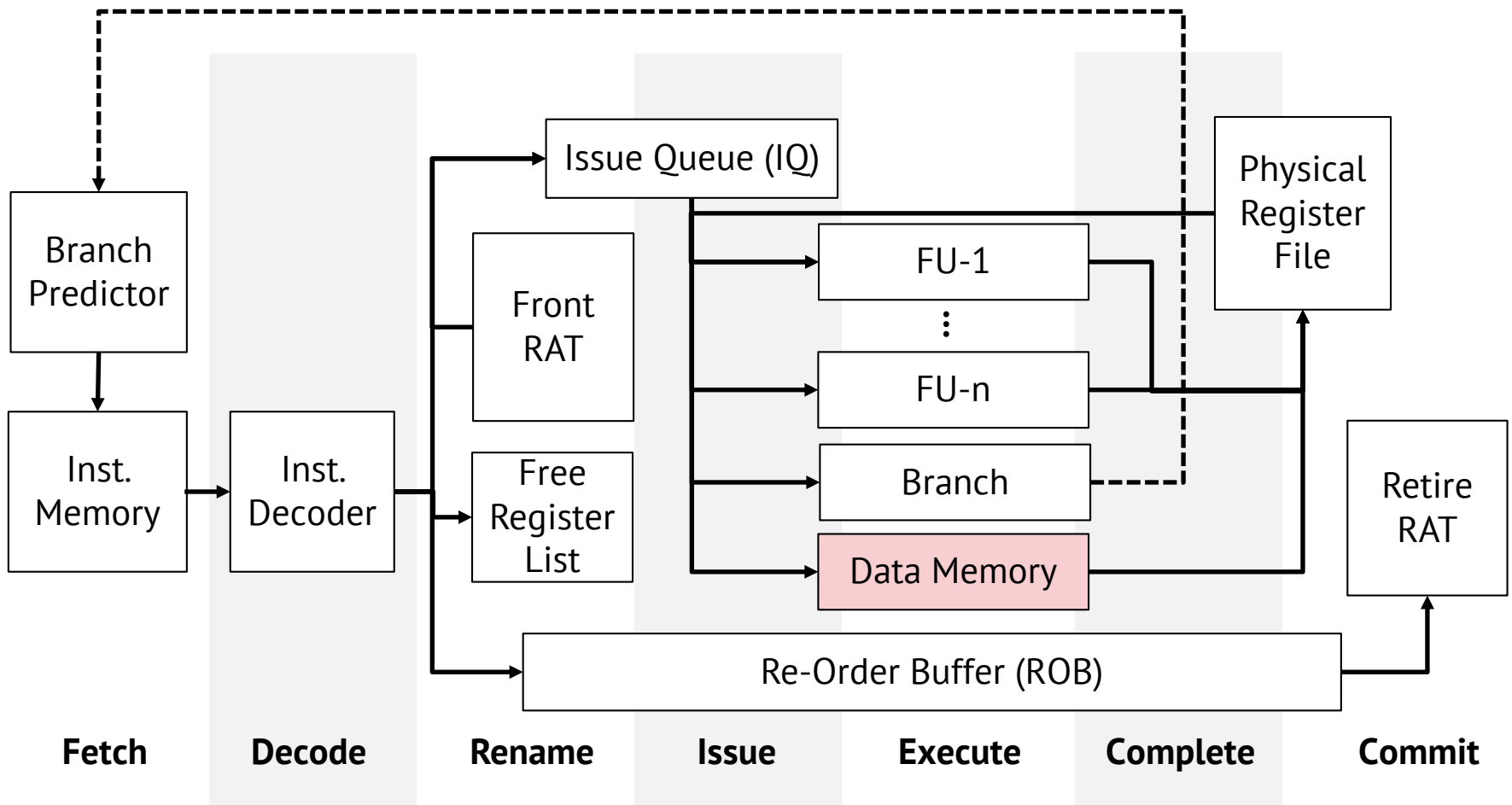
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Loads and Stores

□ What if IQ also had load and store instructions?

Memory Data Dependence

☐ Can we continue executing loads/stores out-of-order?

  ◻ Effective address is required for dependence check

Instructions in the issue queue

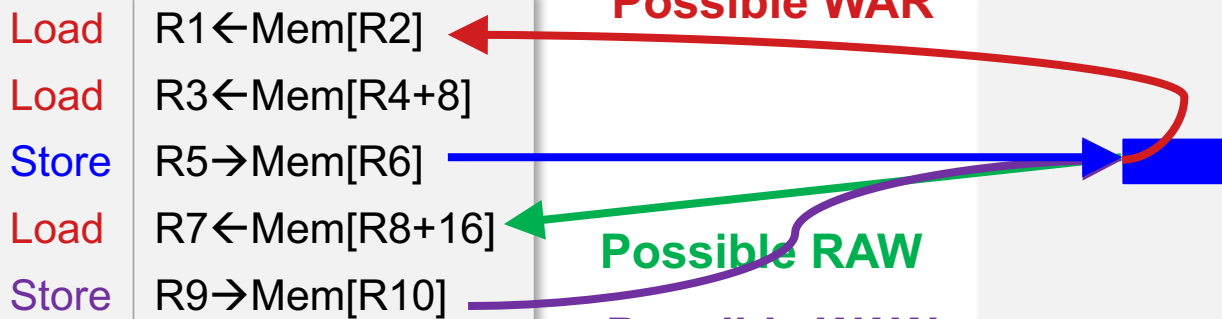|	
Load	R1←Mem[R2]
Load	R3←Mem[R4+8]
Store	R5→Mem[R6]
Load	R7←Mem[R8+16]
Store	R9→Mem[R10]

Possible WAR

Possible RAW

Possible WAW

Memory

Does renaming help?

Load-Store Queue

- Dedicated queue only for load/store instructions
  - Check availability of operands every cycle
- Two steps for load/store instructions
  - Compute the effective address when register is available
  - Send the request to memory if there is no memory hazards
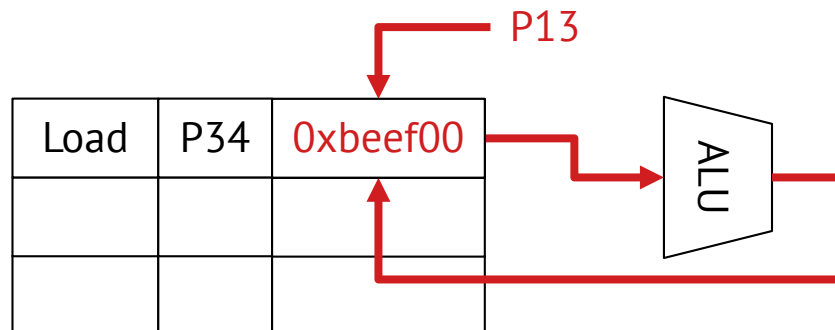
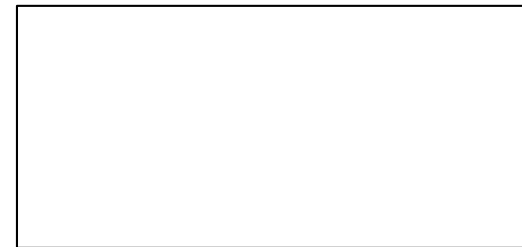|		
Load	P34	0xbeef00

P13

ALU

Memory Dependence Check

☐ Checking for RAW, WAR, and WAW hazards

Load	P34	0x12345
Load	P61	
Store	P26	
Load	P11	
Load	P29	0x12345
Store	P30	0x11111
Load	P15	0x22222
Load	P10	0x11111

1. Which load instructions can be issued?

Due to RAW hazards, only those loads that are not following any unknown stores can be issued.
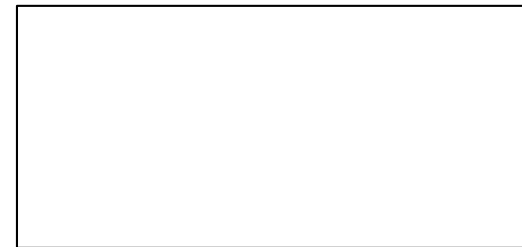
Can we bypass memory?

Memory

Memory Dependence Check

☐ Checking for RAW, WAR, and WAW hazards

Load	P34	0x12345
Load	P61	
Store	P26	
Load	P11	
Load	P29	0x12345
Store	P30	0x11111
Load	P15	0x22222
Load	P10	0x11111

2. Which store instructions can be issued?

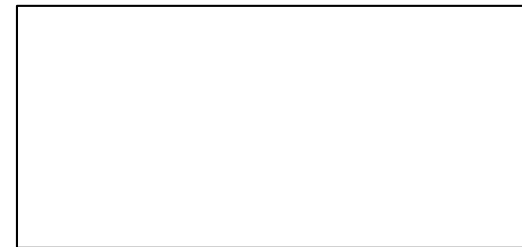**Due to WAW and WAR hazards, only when there is no younger instructions. (why?)**

Memory

Memory Dependence Check

☐ Checking for RAW, WAR, and WAW hazards

Load	P34	0x12345
Load	P61	
Store	P26	0x22222
Load	P11	
Load	P29	0x12345
Store	P30	0x11111
Load	P15	0x22222
Load	P10	0x11111

Which instructions can be issued?

Memory

Memory Dependence Prediction

☐ Can we predict memory dependence?

Load	P34	0x12345
Load	P61	
Store	P26	
Load	P11	
Load	P29	0x12345
Store	P30	0x11111
Load	P15	0x22222
Load	P10	0x11111

Issue/execute load instructions even if they are following unresolved stores

What if the prediction was not correct?

Out-of-order Pipeline with LSQ

☐ LSQ is an extension to IQ