

Matching Multiplications in Bit-Vector formulas

Rahul Jain

TIFR, Mumbai

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Co-authors: Supratik Chakraborty¹ Ashutosh Gupta²

¹IIT Bombay

²TIFR, Mumbai

Outline

- 1 Introduction
- 2 Algorithm
- 3 Experiments

- SMT solvers are important in verification

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- Map system properties to formula satisfiability

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Our work deals with Bit-Vectors

Theory of fixed size bit-vectors(\mathcal{T}_{BV})

Definition: vector of Boolean values with a given length ℓ :

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- Computing systems manipulate finite sequences of 0's and 1's
- Widely used in hardware and software verification

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- SAT is NP complete

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We consider,

- **Bit-vector formulas with multiplication** inspired from hardware verification
- A class of such formulas involving word-level reasoning over multiplication

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**Our work - Enable maximal word-level reasoning
for the class of problems**

Decomposed multiplication

In hardware verification, there are decomposed multiplications

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For example:

$$\begin{array}{r} \begin{array}{cc} 2 & 3 \\ 1 & 3 \end{array} * \\ \hline \begin{array}{cc} 2 * 3 & 3 * 3 \\ 2 * 1 & 3 * 1 \end{array} + \\ \hline \end{array}$$

Hardware implementation: $(2 * 1) * 10^2 + (2 * 3 + 3 * 1) * 10^1 + (3 * 3) * 10^0$

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The above decomposed multiplication is an instance of:

Long multiplication

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- Let us apply long multiplication on $v_1 \bullet v_2$ and $v_3 \bullet v_4$.

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- Let us apply long multiplication on $v_1 \bullet v_2$ and $v_3 \bullet v_4$.
- We obtain the following **partial products**.

	v_1	v_2	
	v_3	v_4	*
<hr/>			
	$v_1 * v_4$	$v_2 * v_4$	
$v_1 * v_3$	$v_2 * v_3$	+	
<hr/>			

E.g. Long multiplication: SMT formula

```
1 (set-logic QF_BV)
2 (declare-fun v1 () (_ BitVec 2))
3 (declare-fun v2 () (_ BitVec 2))
4 (declare-fun v3 () (_ BitVec 2))
5 (declare-fun v4 () (_ BitVec 2))
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7 (define-fun e1 () (_ BitVec 4) (concat #b00 v1))
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12 (assert
13   (not (=
14     (bvmul (concat (concat #b0000 v1) v2)
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20   ))
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22 (check-sat)
23 (exit)
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New formula is of the form: $\neg(A = B) \wedge (A = B)$

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- We developed a backtracking based algorithm to capture all
- Matching is equivalent to well known hard problem *integer factorization* with restricted input space

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Algorithm overview

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Given formula F , for every term t with root as *bvadd*:

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- Checks whether t conforms to the structure of a SMT formula encoding long multiplication
- If yes, extracts the **partial products**, with proper offsets in Λ
- `MATCHLONG(t)` calls `GETMULTOPERANDS(Λ)`

Structure of a SMT formula encoding long multiplication

```
1  (bvadd (concat (bvmul e1 e3) #b0000)  
2          (concat #b00 (bvmul e1 e4) #b00)  
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- Top level operation: *bvadd*

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Structure of a SMT formula encoding long multiplication

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- Top level operation: *bvadd*
- Each *bvadd* argument is a *concat* operation
- Each *concat* argument is either a **partial product** or a string of **zeroes**

Algorithm: MATCHLONG(t)

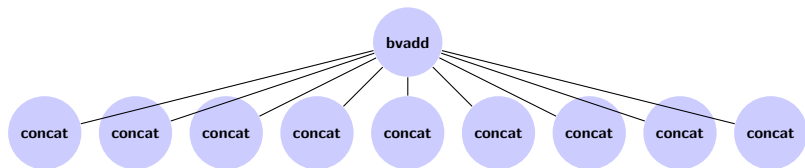
On input t of the form:

```
1  (bvadd (concat (bvmul e1 e4) #b00000000)
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3      (concat #b00 (bvmul e2 e4) #b000000)
4      (concat #b0000 (bvmul e1 e6) #b0000)
5      (concat #b0000 (bvmul e2 e5) #b0000)
6      (concat #b0000 (bvmul e3 e4) #b0000)
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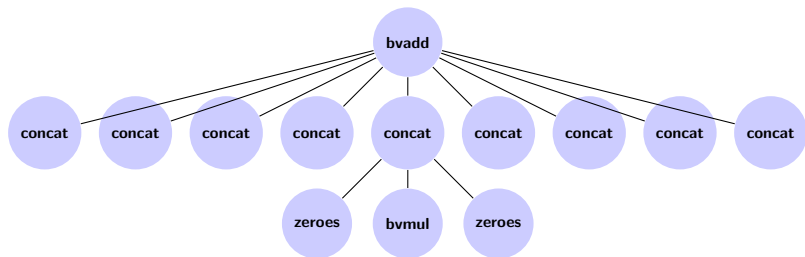
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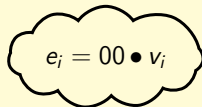
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$$e_i = 00 \bullet v_i$$

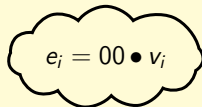
• Output: Λ

Offset	8	6	4	2	0
			$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
		$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
	$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
	Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

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	Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- A call to GETMULTOPERANDS(Λ) is made.

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- Checks if Λ can be matched to an instance of long multiplication
- If yes, extract the **operands** and add **assertion** stating **equality** decomposed and word-level multiplication

GETMULTOPERANDS(Λ)

Input: Λ - the **partial products**, with proper offsets

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
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Λ_4	Λ_3	Λ_2	Λ_1	Λ_0


Output: x and y : the two multiplication operands

Example run

Current Λ index:

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x:
- Current y:




Known partial
products removed

Example run

Current Λ index: 4

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
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$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
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- Current x: v_1
- Current y: v_4




Known partial
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Example run

Current Λ index: 3

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1
- Current y: v_4




Known partial
products removed

Example run

Current Λ index: 3

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: $v_1 v_2$
- Current y: $v_4 v_5$




Known partial products removed

Example run

Current Λ index: 2

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: $v_1 v_2$
- Current y: $v_4 v_5$



Known partial products removed

Example run

Current Λ index: 2

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
$v_1 v_4$	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: $v_1 v_2$
- Current y: $v_4 v_5$


Known partial
products removed

Example run

Current Λ index: 2

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
$v_1 v_4$	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
	$v_1 v_5$	$v_1 v_6$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: $v_1 v_2 v_3$
- Current y: $v_4 v_5 v_6$




Known partial products removed

Example run

Current Λ index: 1

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: $v_1 v_2 v_3$
- Current y: $v_4 v_5 v_6$



Known partial products removed

Example run

Current Λ index: 1

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: $v_1 v_2 v_3$
- Current y: $v_4 v_5 v_6$


Known partial
products removed

Example run

Current Λ index: 0

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: $v_1 v_2 v_3$
- Current y: $v_4 v_5 v_6$



Known partial
products removed

Example run

Current Λ index: 0

		$v_3 v_4$	$v_2 v_6$	$v_3 v_6$
	$v_2 v_4$	$v_2 v_5$	$v_3 v_8$	
$v_1 v_4$	$v_1 v_5$	$v_1 v_6$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: $v_1 v_2 v_3$
- Current y: $v_4 v_5 v_6$

Known partial
products removed

Need for backtracking

- The algorithm may not work always

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- The algorithm may not work always
- Our modification: backtracking based algorithm

Need for backtracking

- The algorithm may not work always
- Our modification: backtracking based algorithm
- We look at one such example

Example run: Backtracking

Current Λ index:

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x :
- Current y :
- Backtrack allowed:

Example run: Backtracking

Current Λ index: 4

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x:
- Current y:
- Backtrack allowed:

Example run: Backtracking

Current Λ index: 4

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1
- Current y: v_3
- Backtrack allowed: *false*

Example run: Backtracking

Current Λ index: 3

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1
- Current y: v_3
- Backtrack allowed: *false*

Example run: Backtracking

Current Λ index: 3

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 0
- Current y: v_3 v_3
- Backtrack allowed: *false true*

Example run: Backtracking

Current Λ index: 2

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_1 v_3$ $v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 0
- Current y: v_3 v_3
- Backtrack allowed: *false true*

Example run: Backtracking

Current Λ index: 2

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_1 v_3$ $v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 0
- Current y: v_3 v_3
- Backtrack allowed: *false true*

Example run: Backtracking

Current Λ index: 2

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_1 v_3$ $v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 0 v_2
- Current y: v_3 v_3 v_3
- Backtrack allowed: *false true false*

Example run: Backtracking

Current Λ index: 1

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 0 v_2
- Current y: v_3 v_3 v_3
- Backtrack allowed: *false true false*

Example run: Backtracking

Current Λ index: 1

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 0 v_2
- Current y: v_3 v_3 v_3
- Backtrack allowed: *false true false*

Conflict! Backtrack to last index with backtrack set to true!

Example run: Backtracking

Current Λ index: 3

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1
- Current y: v_3
- Backtrack allowed: *false*

Example run: Backtracking

Current Λ index: 3

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 v_1
- Current y: v_3 0
- Backtrack allowed: *false* *false*

Example run: Backtracking

Current Λ index: 2

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_1 v_3$ $v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 v_1
- Current y: v_3 0
- Backtrack allowed: *false* *false*

Example run: Backtracking

Current Λ index: 2

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_1 v_3$ $v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 v_1
- Current y: v_3 0
- Backtrack allowed: *false* *false*

Example run: Backtracking

Current Λ index: 2

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_1 v_3$ $v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 v_1 v_2
- Current y: v_3 0 v_3
- Backtrack allowed: *false false false*

Example run: Backtracking

Current Λ index: 1

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 v_1 v_2
- Current y: v_3 0 v_3
- Backtrack allowed: *false false false*

Example run: Backtracking

Current Λ index: 1

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 v_1 v_2
- Current y: v_3 0 v_3
- Backtrack allowed: *false false false false*

Example run: Backtracking

Current Λ index: 0

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 v_1 v_2
- Current y: v_3 0 v_3
- Backtrack allowed: *false false false false*

Example run: Backtracking

Current Λ index: 0

		$v_1 v_3$	$v_1 v_3$	$v_2 v_3$
$v_1 v_3$	$v_1 v_3$	$v_2 v_3$		
Λ_4	Λ_3	Λ_2	Λ_1	Λ_0

- Current x: v_1 v_1 v_2
- Current y: v_3 0 v_3
- Backtrack allowed: *false false false false false*

Outline

1 Introduction

2 Algorithm

3 Experiments

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Implementation

- Implemented in bit-vector rewrite module of Z3 SMT solver
- Various preliminary checks for early exit during identification
- New formula generated after adding assertions
- Can be solved using any solver
- We compare our tool with Z3, BOOLECTOR, CVC4

Benchmarks

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- Our experiments include 20 benchmarks
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- Benchmarks generated by varying:
 - Total bit length of the input bit-vectors
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 - Assigning specific blocks as equal or setting them to zero
- SYSTEMVERILOG to SMT formula:
 - Benchmarks written in SYSTEMVERILOG
 - Fed to STEWORD, a hardware verification tool
 - STEWORD: Converts SYSTEMVERILOG design to SMT formula

Results

Table: Multiplication experiments. Times are in seconds. Bold denotes minimum time.

Benchmark	SMTSOLVER			OURSOLVER			PORTFOLIO
	Z3	BOOLECTOR	CVC4	Z3	BOOLECTOR	CVC4	
base	184.3	42.2	16.54	0.53	43.5	0.01	0.01
ex1	2.99	0.7	0.36	0.33	0.8	0.01	0.01
ex1_sc	t/o	t/o	t/o	1.75	t/o	0.01	0.01
ex2	0.78	0.2	0.08	0.44	0.3	0.01	0.01
ex2_sc	t/o	1718	2826	3.15	1519	0.01	0.01
ex3	1.38	0.3	0.08	0.46	0.7	0.01	0.01
ex3_sc	t/o	1068	t/o	3.45	313.2	0.01	0.01
ex4	0.46	0.2	0.03	0.82	0.2	0.01	0.01
ex4_sc	287.3	62.8	42.36	303.6	12.8	0.01	0.01
sv_assy	t/o	t/o	t/o	0.07	t/o	0.01	0.01
mot_base	t/o	t/o	t/o	13.03	1005	0.01	0.01
mot_ex1	t/o	t/o	t/o	1581	13.8	0.01	0.01
mot_ex2	t/o	t/o	t/o	2231	13.7	0.01	0.01
wal_4bit	0.09	0.05	0.02	0.09	0.1	0.04	0.02
wal_6bit	2.86	0.6	0.85	0.28	0.8	14.36	0.28
wal_8bit	209.8	54.6	225.1	0.59	30.0	3471	0.59
wal_10bit	t/o	1523	t/o	1.03	98.6	t/o	1.03
wal_12bit	t/o	t/o	t/o	1.55	182.3	t/o	1.55
wal_14bit	t/o	t/o	t/o	2.27	228.5	t/o	2.27
wal_16bit	t/o	t/o	t/o	2.95	481.7	t/o	2.95

Summary

Equivalence of word-level and decomposed multiplication:

- Leading SMT solvers failed to identify word-level reasoning
- Bit-blasting lead to time blow up
- Proposed a new pre-processing heuristic
- Implemented as part of Z3 bit-vector rewriting module
- Added assertions to the input formula
- Reduction in solving time
- Implemented similar pattern matching algorithm for Wallace tree multiplier

Thank you!