VIKAS KUMAR RAO
Applying for PhD Degree in Electrical & Computer Engineering

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CAREER OBJECTIVE

Seeking a challenging position where my knowledge and technical skills across ASIC/ FPGA prototyping, GPU IP expertise, Emulation/system validation, Pre-Silicon Verification, Post-Silicon Validation, and HDL programming/scripting language strengths will be fully utilized in achieving company's stated goals.

ACADEMICS

Master's in VLSI-CAD, June '10 — **8.71**
Manipal University, MCIS

B.E in Electronics and communication, May '08 — **69.20%**
Visveswaraya Technological University, JSSATE

PROFILE SUMMARY

- **July 2014 - Till Date** working as **Graphics Hardware Engineer** at **Intel Corporation, Bangalore, India.**
- **Aug 2010 - June 2014** worked as **Graphics System Validation Engineer** at **Intel Corporation, Bangalore, India.**
- **July 2009 - July 2010** worked as **Student Intern** at **Intel Corporation, Bangalore, India.**

Combined 6 years 4 months of overall industry experience in areas of Emulation / ASIC Prototyping / GPU IP content development / Pre-Silicon Verification, FPGA modeling and Post silicon System Validation:

- Low cost *FPGA prototyping* expertise of multiple *graphics sub IP modules* derived from industry standard *DX/OpenGL* compliant graphics pipeline on DINI based *virtex5/virtex6/virtex7* series of FPGA Cards.
- ASIC prototyping with *Mentor Veloce emulation platform* on *4 generations* of *Intel's GPU* microarchitectures spread across 32nm, 22nm, 14nm and 10nm processes.
- EDA tool expertise on *Xilinx ISE, Vivado, VCS, DC, CoreGen, Synplify_pro* and *Synplify_premier*
- Hands on test writing skills for *constrained random stimulus generation* based on *ruby for GPU sub IP's*.
- Experience with *System Verilog* based *Test Bench* development, *dpi checkers/monitors*.
- Worked on *coverage* driven *functional verification* and experience with system Verilog *assertions* for debug.
- Hands on Post-Silicon debug capabilities and system level modelling concepts for 4 generations of 32/*22/14/10nm* architectures including debug exposure to *PSMI scan* interface.
- Knowledge on FPGA debug methodology tools - *chip scope and Identify*
- Experience with developing transaction based, C Co-Sim/ HDL Co-Sim simulation acceleration models.
- *Transactor* and *BFM* design expertise based on industry standard *SCEMI 1.0/2.0 specification* using *Verilog/system-Verilog* HDL's and c programming.

TECHNICAL SKILLS

EDA simulation Tools	**:**	VCS, Modelsim
EDA synthesis Tools	**:**	Xilinx ISE, VIVADO, Synplify Pro, Synplify Premier, and CoreGen
HDL	**:**	Verilog, VHDL, System Verilog
Programming Languages	**:**	C, basics of C++
Scripting languages	**:**	Ruby, PERL, Shell
Emulation platforms	**:**	Mentor Veloce
FPGA platforms	**:**	custom V5 card, DINI DNV6_F2PCIe (LX 330T), DNV7F2A (XC7V2000T)
Debug tools	**:**	chip scope, Identify, Logic Analysers, Velwavegen
Post Silicon Validation	**:**	JTAG based In-target-probe (ITP), PSMI interface
Operating systems	**:**	UNIX, Windows

PUBLICATIONS AND TRAININGS

- "Unified Validation Environment Across CLT Simulation & Emulation", **Intel VPG Tech Summit - 2014**, co-presenter
- "Scalable high-throughput FPGA Transactor", submitted to **Intel DTTC conference – 2014**, author.
- "Software Framework for FPGA Based Validation of Gen Graphics", selected and attended at **Intel DTTC conference, Oregon – 2013**, co-author.
- "FPGA based Solutions for ASIC development", **Intel India Innovation Day - 2012**, poster presentation.
- FPGA Based prototyping methodology workshop, **Synopsys EDA India Ltd - 2012**, Bengaluru.
- ISE Design flow and essentials of FPGA Design, **Sandeepani school of VLSI Design – 2012**, training.

BRIEF PROJECT DETAILS

Project : 14nm Skylake/Broxton

Skylake is the code name for Intel's to be developed "tock" based 14nm processor architecture for client/tablets.

Tools and Platform **:** JTAG based In-target-probe and PSMI based scan captures on Skylake silicon.

Roles and responsibilities **:**

- Responsible for hands on end to end debug of HW failures on Skylake post-silicon - Duties included test plan preparation, multiple test plan reviews with design and architectural teams, test template and test list development, execution monitoring and debug of failures.
- Role demanded anchoring multiple task forces integrating design/architecture/pre-silicon and debug teams across geo's on single platform to resolve the HW failures.
- Was identified to lead a PSMI based scan dump methodology cross-site effort to enhance and influence the debug framework for usage across teams and subsequent projects.

Achievements and Impact **:**

- Found 2 critical corner case functional bugs which were timing dependent and failing only on silicon, this also resulted in retaining the complex DCN which was pushed for de-featuring if not for these unresolved bugs.
- The bugs uncovered new methodology parameters which were included as part of standard process for all the upcoming projects.
- Was recognised as the expertise and single point of contact for PSMI based scan dump captures among entire team and was used for root causing other critical functional bugs.

Tools and Platform **:** ISE/VIVADO/Synplify-premier/VCS on v6/v7 platform

Roles and responsibilities **:**

- For the first time a low cost FPGA platform was designed and utilized to functionally validate the texture sampler sub-IP. The timeline of the FPGA platform validation was much ahead of the full validation emulation cycle process which was yet to begin on full graphics pipe.
- Was assigned as a client for the whole FPGA setup and was responsible for handling the validation of functionally complex texture sampler cluster derived from Microsoft's DX11 graphics spec.
- Lot of pre-work had to be done to understand the cluster functionality and interface changes to adapt it to FPGA environment.
- 50+ design changes involved for the project were to be understood and wrote effective test cases to cover the same.
- Regressed all the test cases on FPGA platform with multiple seeds and debugged all the real/false/environment and golden reference failures.
- Reproduced the relevant failures at lower level sub units of sampler cluster with RTL level source code debugging on Synopsys DVE/VCS GUI environment to root cause the issues.

Achievements and Impact **:**

- Found 20 functional RTL bugs and 40 golden reference bugs delivering a functionally clean texture sampler sub-IP for silicon tape-in.
- The project removed the dependency of texture sampler validation on other sub-IP's present in the graphics design and acted as a validation platform for design to run complex test cases which would take humungous time to run in pre-Silicon simulation platforms otherwise.
- The project was recognized as a reliable framework and is being used as a validation platform for texture sampler sub-IP for future projects at Intel.

Tools and Platform **:** Synopsys DVE and Intel proprietary tools on mentor Veloce platform.

Roles and responsibilities **:**

- Responsible for system level emulation validation of texture sampler cluster - Duties include test plan preparation, multiple test plan reviews with design and architectural teams, test template and test list development, execution monitoring and debug of failures.
- Worked on enabling execution in emulation and post-silicon in parallel to FPGA texture sampler validation environment to find the graphics pipe level bugs with developed test content.
- Worked on exploring emulation coverage methodology to make sure the code/functional coverage were appropriate and resulted in projection of high confidence for the cluster.
- Comprehended 50+ design changes involved for the project were effectively understood and translated to test cases for functional validation of the features.

Achievements and Impact **:**

- Found 3 RTL bugs and multiple environment issues to provide a functionally healthy graphics pipe level RTL from texture sampler side for tape-in.
- Wrote multiple test cases, debugging and exploring different methodologies/tools bringing in efficiency to the overall validation architecture.
- The coverage effort was a first time initiative and pushed other team members to pursue, adopt the methodology for other units adding cover point analysis hence reducing the test gaps and increasing the confidence.

Project : 10nm Cannonlake

Cannonlake is the code name for Intel's to be developed "tick" based 10nm processor architecture which is the successor of Skylake for client/tablets.

Tools and Platform **:** ISE/VIVADO/Synplify premier/VCS/chip scope/identify on v7 platform

Roles and responsibilities **:**

- Responsible for test plan, development, review and deployment of code written on Ruby/C++ based random
- Responsible for porting and modelling the RTL from texture sampler graphics IP to be suitable for FPGA validation environment.
- Was a client in Skylake for the same IP, Handling the model deployment for Cannonlake now.
- Any duplicate/BFM/FPGA related issues found in the process of execution/deployment needs to be debugged and cleaned. Non-reproducible in-circuit failures will be debugged with the help of identify/Chip scope

Achievements and Impact **:**

- Have been delivering the models effectively, facilitating regression of complex test cases for the new project.
- The model deployment is well ahead of the graphics full pipe emulation validation timeline thus giving scope for early bug finding and also freeing up high cost emulator bandwidth for other cluster/full graphics pipe validation.
- Test content and code reviews resulted in high quality functional emulation models to be dispatched for a healthier and bug free silicon Tape-In.

Project : 22nm Valleyview

Valleyview is Intel's 22nm Atom based SoC.

Tools and Platform **:** Logic analysers, ITP and Intel proprietary tools on Valleyview Silicon

Roles and responsibilities **:**

- Got into Valleyview debug on request during critical period and anchored 2 task forces to get around two major issues.
- Responsibilities during this tenure included setting up the driver environment, taking dumps and removing false failures out of the picture

Achievements and Impact **:**

- The Valleyview Post Silicon clean-up/execution/debug on the task forces resulted in one-tape-in gate removal and one post-Si RTL bug

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Project : 22nm Haswell/14nm Broadwell/14nm Cherryview SoC

Haswell, Broadwell and Cherryview are Intel's latest microarchitectures/SoC.

Tools and Platform **:** ISE/VIVADO/Synplify premier/VCS/chip scope/identify on v5/v6 platform

Roles and responsibilities **:**

- Worked on development of low cost FPGA based platform for validation of Execution Unit which forms the heart of all computations in the processor architecture.
- Roles included development of BFM's, interface understanding, tool hacks and integration of overall environment for Haswell architecture.
- Role also demanded interaction with FAE's to fix synthesis and FPGA related issues.
- Ported the complete framework into FPGA simulation environment which involved integration of all BFM's and multiple regressions and debugs to rule out all the false failures.
- The design of the interface changed considerably from project to project. This resulted in the need for a modular Transactor and BFM design to add in the scalability factor.

Achievements and Impact **:**

- Design completion from scratch to get the overall environment up and running resulted in 24 RTL bugs in the first project.
- Portability and scalability of the framework resulted in leveraging of complete project as a validation standard for all future projects at Intel as well as a future design vehicle framework.

Project : 22nm Ivy Bridge

Ivy Bridge is the code name for Intel's 22nm architecture which had the Tri-gate transistor ("3-D") technology being used in the process for the first time.

Tools and Platform **:** Synopsys DVE and Intel proprietary tools on mentor Veloce/ Ivy Bridge silicon.

Roles and responsibilities **:**

- was responsible for system level emulation validation and also post Silicon debug of pixel backend sub-IP derived from industry standard DX/OpenGL compliant graphics pipeline,
- Responsibilities included writing test cases, debugging and exploring different methodologies/tools bringing in efficiency to the overall validation architecture of the cluster.
- Worked across Geo's to collect performance trackers for characterizing the workloads against defined metrics.
- Was responsible for setting up driver environment and reproducing issues from emulation/simulation/Silicon environments.

Achievements and Impact **:**

- Was responsible for deploying a healthy pixel backend cluster towards Tape-in.
- Was involved in closure of more than 20 RTL bugs and several environment issues.
- Performance characterization feedback resulted in effective design analysis and RTL tweaking.
- Driver environment setup resulted in a critical bug reproduction which was a potential Tape-in block.

Project : 32nm Sandy Bridge

Sandy Bridge is the code name for Intel's first Integrated GMCH (integrated graphics and memory controller) processor onto a single die inside the processor package. In contrast, Sandy Bridge's predecessor, Clarkdale, had two separate dies (one for GMCH, one for processor) within the processor package. This tighter integration reduces memory latency even more.

Tools and Platform **:** DVE/VCS GUI in Linux environment

Roles and responsibilities **:**

- handling test cases and managing huge database of execution reports
- Ruby based test case writing
- Improving the efficiency by writing Perl/Shell scripts to automate the processes mentioned above.
- Reproduce the failures at lower level sub units and RTL level source code debugging on Synopsys DVE/VCS GUI environment and Working with Emulation engineers and ULT owners to debug the same.
- DPI- based tracker/checker writing and post-processing of results.

Achievements and Impact **:**

- Was responsible in delivering functionally clean graphics clusters regressed at virtual platforms for next level emulation build and consequently resulting in healthy real world silicon.
- Brought in efficiency by automating the regression report extraction/processing.

RECOGNITIONS AND AWARDS

- Multiple recognitions and awards for novel validation methodology development and paper presentations.
- Recognised for exceptional organizing and planning skills.
- Credited with efficient resource mapping, training and ramp up of junior engineers, and new hires.
- Dynamic team player who is consistently motivated toward success and completion of projects with an ability to work independently.
- Good communication skills with experience working across multiple geo's.

ACADEMIC PROJECTS AND THESIS

MS (internship project at Intel) – **pipe level validation of 3D graphics engine** –

Presented thesis on efficient validation of 3D graphics engine. My role in the project was to verify test scenarios on Intel's first integrated graphics model in pre-silicon environment. Enhanced the regression mechanisms by automating the flow and also co-developed DPI based interface to analyse the regression outputs. Entire effort involved coding on Ruby, Perl, C++, and system Verilog.

MS (2nd semester) **- Configuration of AMBA Advanced Peripheral Bus (APB) -**

Designed the low power AMBA-APB bus as a slave peripheral for transmission and reception of data, Configuring the signals on the interface from high bandwidth, high speed AMBA-AHB/ASB into APB bridge and then driving them onto one of the multiple APB slaves present for low bandwidth applications. The right slave being selected on the basis of several interface signals (pselect, penable, paddr and preset) with three different modes (idle, setup and enable) also taken into account, code written in Verilog and simulated using VCS and Modelsim.

MS (vacation project- at *AXIOM*) **- Asynchronous Serial Bit Stream Reception/Transmission -** project included designing individual modules (Receiver, Transmitter, FIFO) for receiving and transmitting programmable number of bits (multiples of 4, up to 32) at programmable data rates under three different modes with interfacing, acknowledgement and other reference signals being taken from the specification provided by the vendor, code written in Verilog and simulated in Modelsim.

MS (1st semester) **- AES 128 bit encryption and decryption -**

encrypting and securing a 128 bit data by using a 128 bit cipher key where the procedure includes stages such as S-box substitution, shift rows, mix-columns and add round keys which operate on a 4x4 base matrix called state wherein the keys for each round are generated using a separate key expansion block and then decryption of the same is done by using the inverse procedure to retrieve the data, code written in Verilog and simulated in Modelsim.

BE **- Wireless DVD signal transmitter and receiver -**

Wireless transmission of audio and video signals from DVD player to TV using i2c serial transmission protocol with start and stop time frames being input by the user dynamically with help of four multifunctional keypad switches and accounted by a real time clock (DS-1307) which are interfaced to 8051 microcontroller. A relay is also interfaced to the microcontroller in-order to control the auto on/off of DVD player. The time frame values and procedures are displayed on a 16*2 LCD display, code written in C.

PERSONAL DETAILS AND EXTRACURRICULARS

Date of Birth	**:**	25-03-1987
Languages	**:**	English, Kannada, Tulu, Telugu, Tamil, and Hindi
Interests	**:**	Singing, candid wedding/fashion photography, Biking, Trekking, Movies
Community Service	**:**	social initiative drives as part of Intel Involved Match Grant Program

REFERENCE

- Available on request