Interconnect Design and Modeling

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Interconnect

- Increasing emphasis on interconnect
  - delay
  - power
  - inductance
- Modeling no longer lumped RC

Interconnect

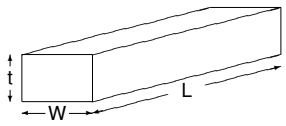
- Wires have three important characteristics:
  1. Resistance: relates current i to voltage V (carrier flow)
  2. Capacitance: relates charge Q to voltage V (electric energy)
  3. Inductance: relates current i to flux H (magnetic energy)

Wire Resistance

- Simple model because current confined to material
- Since R is small, distance is primary metric
- Long wires have regular shape that simplifies modeling

$$R = R_{sq}\frac{L}{W}$$

$$R_{sq} = \frac{1}{\sigma t}$$



Wire Resistance

- Wire thickness fixed by fabrication process
- Therefore design characterized by R_{sq}

Metal	Resistance
Aluminum	$R_{sq} = 2.9\frac{\mu\Omega\cdot\text{cm}}{t}$
Copper	$R_{sq} = 1.8\frac{\mu\Omega\cdot\text{cm}}{t}$

. . . but for copper, thickness t is less than whole wire thickness due to barrier layer

Wire Resistance

For 350nm process technology:

Metal	Resistance
metal 4	0.02
metal 1–3	0.04
poly	~ 2
unsilicided poly	~ 40
ndiff	~ 2
unsilicided ndiff	~ 40
pdiff	~ 2
unsilicided pdiff	~ 120
contact	$\sim 2\Omega$

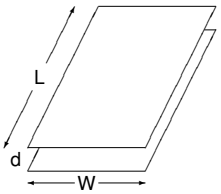
Wire Capacitances

Two simple models

1. Parallel plate
2. Cylindrical

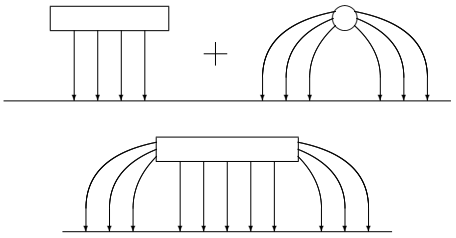
Good approximation obtained by combination of the two

parallel plate model:
$C = \frac{\varepsilon}{d} LW$
$\varepsilon = 0.035 \frac{fF}{\mu}$
Since $\frac{\varepsilon}{d}$ is fixed by technology,
$C = C_i W L$



Wire Capacitance

Combine parallel plate and cylindrical model for full wire model:



$$C_{fringe} = \varepsilon L \left\{ \frac{\pi}{\ln\left(1+\frac{2d}{t}\left(1+\sqrt{1+\frac{t}{d}}\right)\right)} - \frac{t}{4d} \right\}$$

for each fringe, d = spacing to plate

Wire Capacitance

- Common fringe cap ranges: $0.3 \leq \frac{t}{d} \leq 1$
- $C_{fringe} = 0.04 \frac{fF}{\mu} - 0.05 \frac{fF}{\mu}$
- Total Cap = parallel plate + both fringe caps
- $C = C_i W L + 2 C_{fringe}$
- With low-κ materials, horizontal and vertical caps can have different relative dielectrics, so:
  $C_{wire} = \varepsilon_0 L \left(2\kappa\varepsilon_{horiz} \frac{thick}{spacing} + 2\varepsilon_{vert} \frac{width}{ILD_{thick}} \right) + \text{fringe}(\varepsilon_{horiz}, \varepsilon_{vert})$

Transmission Lines

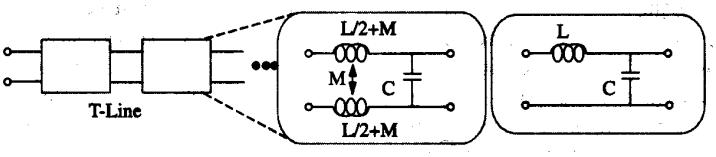
- Transmitters launch electromagnetic waves down wires
- Wave only observes effects of current wire segment
  - effect of load and other segments don't initially affect signal
- Geometry at current location determine ratio of voltage and current
- **impedance** Z is the voltage and current ratio
  - has same dimensions as resistance: $\frac{V}{I}$

Transmission Lines

- Ideal transmission line modeled as distributed LC circuit
  - inductance and capacitance model stored magnetic (L) and electric (C) energy of the wave.
- Impedance is set by $Z = \sqrt{\frac{L}{C}}$
- Propagation velocity is $v = \frac{1}{\sqrt{LC}}$

Image Currents

- Inherently two terminal device
  1. signal path
  2. return path
- Signal path and return current are equal and opposite
- The LC model only models differential signal between port pairs
  - return current is where most difficulties arise



Transmission Line Return Current

- Coaxial cable provides excellent return current
- PCBs can be designed as transmission lines
  - reference planes (V_{dd} or Gnd) under signal plane
  - this forms *microstrip* lines
- Lack of explicit signal return results in current on other signals
  - This coupling results in crosstalk and mutual inductance
- Worst transmission line design is in IC Packages
  - no ground plane
  - return currents far from signal path

Transmission Line Noise

- Inductive noise creates crosstalk on adjacent signal wires
- Coupling is through frequency dependent reactance:
  - ωL
  - $\frac{1}{\omega C}$
- Hence noise depends on the bandwidth of the signals
  - high frequencies (fast edge rates) create greater coupling
  - limit signal bandwidth (edge rate dependence) to reduce noise
  - significant issue in clock design!

Inductance

- Voltage between two points a and b
- Points in presence of an electric field $V = \int_a^b E \cdot \partial l$
- Two separate paths exist between a & b, a *drive* and *return* path

If electric field is time invariant, the integral is irrelevant $\oint E \cdot \partial l = 0$
This is Kirchoff's Voltage Law - which doesn't hold here

- Use maxwell's equation $\nabla x E = -\frac{\mu \partial H}{\partial t}$
- Creates time varying magnetic field with nonzero curl in electric field in each loop
  - therefore, $\oint E \cdot \partial l = V_L \neq 0$
- Can be produced with time-varying current density J in Maxwell's equation term $\nabla x H = \frac{\varepsilon \partial E}{\partial t} + J$

Inductance

- Voltage between a and b *cannot be defined* unless the paths of drive and return current are known.
- Even if paths are known, Kirchoff's Voltage Law cannot necessarily be applied since voltage is non zero
- We therefore define a fictitious element called an **inductor**
  - V_L of inductor is proportional to time variation of injected current $V_L \propto \frac{\partial I}{\partial t} = L\frac{\partial I}{\partial t}$
  - L now the proportionality of the *inductance* of current loops

Inductance Loops

- Small loops minimize area through which magnetic flux flows
  - and therefore minimize voltage drop
- Aggressors induce current in victims in opposite direction
- If victim has large resistance, (as in all CMOS gates)
  - displaced charge can't immediately flow
  - charge depletion is created at far end of victim wire (voltage dip)
  - charge accumulation at near end (voltage rise)
  - this resists further charge depletion (poor inductance path)
  - only a small amount of inductance supported in each wire
  - inductance then pushed out to farther wires

Inductance Loops

- Accurate models minimally require many return paths
- Inductance modeling influenced by
  - noise (coupling, power supply, etc.)
  - switching activity along signal wires
  - wire density

Inductance Loops

- Inductance and resistance are related to return paths
- Return paths shared by many signals
- Intersecting current loops result in **mutual inductance**
- Mutual inductance may be of similar magnitude to self inductance

Interconnect Scaling

The transistor delay scales approximately linear to scaling factor s

What happens to wire delay?

Interconnect Scaling

The transistor delay scales approximately linear to scaling factor s

What happens to wire delay?

- Many claim that wire delay scales up...
  - ...but depends on how the wires are scaled!
- You need to understand the assumptions

For example, in technology scaled by s:

- wire length scales by:
  - s, remains constant, scales up with die...
- wire thickness scales by:
  - s, remains constant, scales up by $\sqrt{\frac{1}{s}}$...

Interconnect Scaling

- Gate delay scales as s
- Best wire delay scaling doesn't come close:
  - scaling all dimensions:
    - RC remains constant
  - leaving thickness t fixed
    - wire delay still scales worst than s
    - dependencies exist on width and spacing
    - leave constant width or spacing gives scaling of s
      - but only if wire length scales!
      - increasing or constant length increases delay

Interconnect Scaling

- Aspect ratio $(\frac{H}{W})$ *was* increasing
  - yield, dishing, variation in sheet resistance
  - dielectric versus spacing issues
  - tradeoff between $R\downarrow$ and $C\uparrow$
- Recently it has been fairly constant at ~ 2

Interconnect Scaling

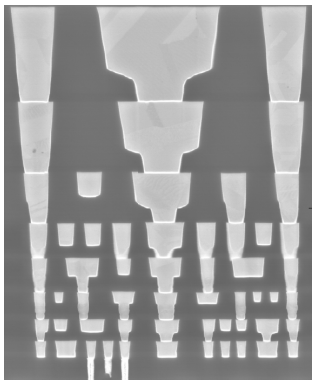
- Horizontal cap scaling slower than vertical cap
  - wire height vs spacing vs dielectric
  - must account for switching activity in adjacent wires!
- **Barrier cladding** doesn't proportionally scale even keeping constant scaled width and height
  - aluminum (Al)
    - highly resistive cladding of titanium or titanium nitride
    - over-layers improve lithographic patterning and via yields
  - copper (Cu)
    - additionally required to prevent Cu seepage into dielectric
    - side-wall barrier thickens
    - gives potentially worse resistance scaling than Al
    - sheet resistance now becomes function of width...

Interconnect Scaling (nm except for ILD κ)

180nm node	width	spacing	thickness	ILD height	ILD κ
local	280	280	450	650	3.5
intermediate	350	350	650	650	3.5
global	800	800	1250	650	3.5
130nm node	**width**	**spacing**	**thickness**	**ILD height**	**ILD κ**
local	200	200	450	450	3.2
intermediate	280	280	450	450	3.2
global	600	600	1200	450	3.2
90nm node	**width**	**spacing**	**thickness**	**ILD height**	**ILD κ**
local	150	150	300	300	2.8
intermediate	200	200	450	300	2.8
global	500	500	1200	300	2.8
65nm node	**width**	**spacing**	**thickness**	**ILD height**	**ILD κ**
local	100	100	200	200	2.2
intermediate	140	140	350	200	2.2
global	450	450	1200	200	2.2

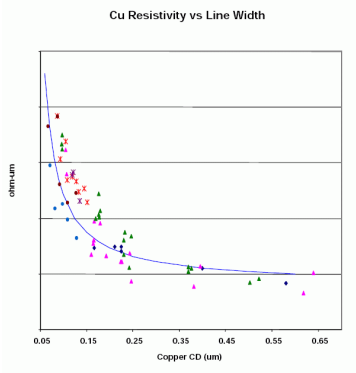
Wire Aspect Ratios

SEM photo of Intel's 65nm wire spacings:



Copper Wire Sizing

Global wires picked after resistance flattens out in coper wires



Wire Inductance Scaling

Fortunately, scaling has kept wire inductance in check

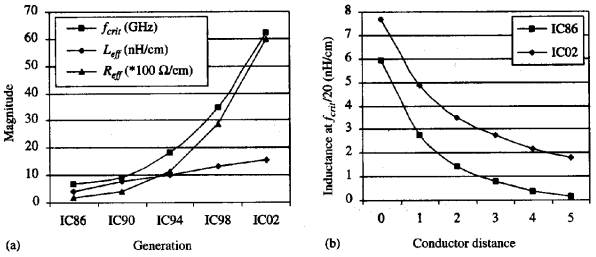
- Low impedance enables signals to be used as inductive return paths
  - $Z = R + j\omega L$
    ωL is the inductance at a given frequency.
- Fast edge rates increase current and magnetic energy
  - impedance resists edge rates
  - f_{crit} measures impact of inductance relative to edge rate
  - f_{crit} exists where $\omega L = R$
  - occurs when $f = \frac{1}{\pi T_{edge-rate}}$

Wire Inductance Scaling

- Two main factors in on-chip self-inductance
  1. if driver rise time much faster than propagation velocity down wire
     - relation of ωL and $T_{edge-rate}$
  2. whether attenuation constant ($\frac{Z_0}{2R_{wire}}$) is greater than one

Wire Inductance Scaling

- Fortunately, increasing resistance inhibits self-inductance in most signal wires
- When plotted against f_{crit} scaling of inductance is not severe



Wire Inductance Scaling

- Mutual inductance relevant over increasing distance as we scale
- **Skin effect**
  - current flows in the periphery of conductor rather than in uniform fashion.
  - effect directly proportional to edge rates (slopes)
  - decreases inductance and increases resistance
  - most relevant for wide interconnect (clocks, global wires, power supplies)
- At high frequencies (180GHz+), distribution of return currents less dispersive
  - reduces inductance of current loops

Inductive Ringing

Ringing or reflections occur with impedance mismatches in a transmission line

- Long wires have different segments with different impedance
  - on-chip pad driver, package pin to PCB, trace on PCB, coaxial or twisted pair between boards, trace on receiving PCB, package wire to receiver chip, receiver load.
- Each segment must satisfy:
  1. conservation of energy (wires not active devices)
     - energy flowing into connection must equal energy flowing out
  2. continuity of voltage
     - voltages at two sides of connection must be equal

Inductive Ringing

- If connected impedances Z are equal, solution is trivial as signal continues with same voltage
- If second segment has lower impedance, voltage in this segment must be lower
  - must reduce voltage and increase current in second segment
  - *achieved by negative wave sent back to the transmitter*
  - superimposing forward and backward waves in first segment matches current and voltage of forward wave in second segment!
- Conversely, if second segment has higher impedance, reflected wave is positive

Inductive Ringing

- Ringing occurs when load impedance Z_L doesn't match the characteristic impedance of the transmission line Z_0
- Z_L and Z_0 don't match on our chips:
  - load impedance: $Z_L = \frac{-j}{\omega C_L}$
  - transmission impedance: $Z_0 \approx \sqrt{\frac{R}{2\omega C}}(1-j)$ for lossy conductor with $f \ll f_{crit}$ or $R \gg \omega L$
  - relative sign and magnitude of reflected voltage: $V_{reflect} = \Gamma V_{in} = \frac{Z_L - Z_0}{Z_L + Z_0} V_{in}$ where Γ is the reflection coefficient

Inductive Ringing

- Some ringing will exist on on-chip interconnect although it is usually minor
- Biggest issue is *under-estimation* of noise by not modeling inductive ringing!

Inductive Ringing

- Reflections are feedback to previous stages
- Indicates current-to-voltage ratio is incorrect, and needs adjusting
- No information about impedance available at reflection generating connection
  - several round trips may occur between reflection generating connections
- After settling, voltage and current ratio is uniform
- The $\frac{V}{I}$ ratio determined by final load impedance

If wire delay is small compared to rise time of the signal, settling happens so quickly that driver effectively sees load directly, and reflections can be ignored.

Transmission Line Connections

- Driver or receiver stage connections are same as wire segments
  - mismatch will result in ringing
- Can design systems with mismatched driver and receiver impedances
  - low impedance driver to guarantee voltage swing
  - receiver *must* match wire impedance to avoid reflections
  - (example: oscilloscope cable and probe)

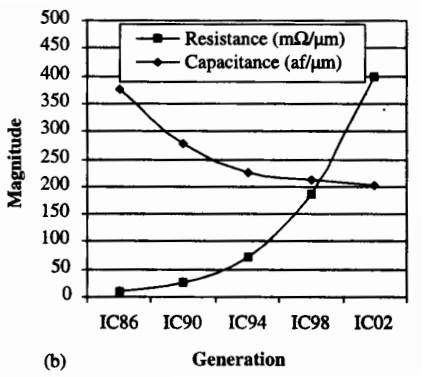
Transmission Line Connections

- Matched impedance drivers:
  - driver impedance matches transmission line, $\Rightarrow$ removes reflections
  - if receiver left unterminated (high impedance)
    - wave of half the desired signal launched in wire $\frac{Z_0}{Z_{drv}+Z_0}$
    - voltage doubles with reflection at open end of transmission line
    - thus presenting full swing at output
    - reflected wave absorbed at driver

Design Techniques to Reduce Induction

- Increasing spacing between conductors for C coupling detrimental to inductance (increases return paths)
- Introduce supply rails that are used to conduct return current
  - also useful for C shielding
  - due to distance of inductive effect, signal-to-rail ratios above 2:1 still useful (though not for C)
- Orthogonal rail planes above/below signal planes
  - all signals adjacent to low resistance return
  - modification to supply grid design
  - no help for capacitive coupling
- Skew switching times of bus signals, or dual-rail design
- Staggered repeater locations

R and C Scaling



Scaling Solutions

- Shift to copper interconnect
- Using low-κ dielectric insulators
  - "strengthens" electric field lines between conductors compared to a vacuum.
  - increases surface charge, and hence capacitance
  - have moved from $\kappa = 4.0$ to $\kappa = 2.2$

Other Scaling Considerations

1. Wire effect on performance
2. Process variation
3. Architectural issues
   - $IR, \frac{dI}{dt}, I^2R$ power losses
4. Modeling and performance verification
5. Power dissipation

Simple Wire Delay Models

Simple wire delay models have three major effects

1. Resistive constant: RC
   - carrier flow and energy
2. Transmission impedance: $\frac{L}{R}$
   - interconnect length independent
   - models increase in inductive generated current
   - normally bound by saturation current of transistors
3. Time of flight: $\sqrt{LC}$
   - phase velocity in dielectric medium

Simple Wire Delay Model

Time constant in ps for wide bus

Time Constant	1cm	1mm	100μm
RC	2900.0	29.0	0.3
L/R	4.6	4.6	4.6
$\sqrt{LC}$	115.0	11.5	1.2

Models a wide bus above a ground plane and beneath orthogonally routed signals for a 180nm process.

- Transmission line delay is constant
- Long wires dominated by RC
- Medium wires dominated by RC and time of flight $\sqrt{LC}$
- Short wires dominated by transmission edge rate effects (think signal slopes)

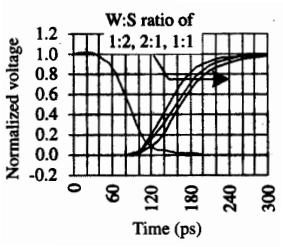
Reducing Crosstalk in Designs

1. Place a ground plane closer to wire
   - increases the ground capacitance
   - reduces coupling by shielding some of the field lines
   - . . . but increases total capacitance on the wire
2. Increase spacing between the wires
   - decreases the coupling
3. Add shield wires between signals
   - converts coupling cap to Gnd cap
   - increases area
4. Change the dielectric constant between the wires (low κ dielectrics)

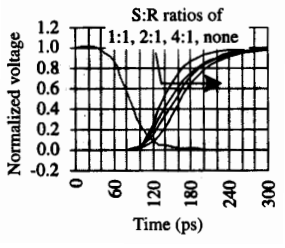
Crosstalk and Power Solutions

1. Wire separation and wire width tradeoffs
2. Shielding
3. Signal swizzling
4. Temporally skew signals (disjoint switching windows)
5. Stagger inverter locations (cancel out transitions)
6. Interleave signal directions
7. Signal protocols
   - dual-rail signaling

Wire Width and Spacing Tradeoff



Delay as wire widths and spacing are changed



Worst case delay improvements with shielding and swizzling (4:1 case)

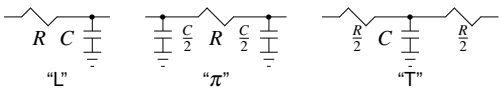
Wire Delay

Wires are a distributed RC circuit

- Wire has R per mm and C per mm

Model by breaking wires into segments

- 3 options, two okay, one very bad:



Which is best and which is worst?

Wire Delay

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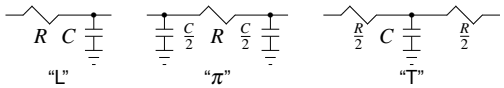


"L" "π" "T"

Which is best and which is worst?
L model is very bad!
64 L sections and 4 π sections give $\sim$ 5% accuracy for RC line
π model is best

Wire Delay

A physical wire is a distributed RC circuit

- The delay of a π or T section can be modeled as:
  - $t_d = \frac{1}{2}R_T C_T$
  - this holds for increased wire segments
- Simple delay for L model is:
  - $t_d = RC$
  - adding segments reduces delay:
  - $\frac{n+1}{n}\frac{1}{2}R_T C_T$
- T and π models much better than L!

So simple wire delay can be calculated as $t_d = \frac{1}{2}RC$

Wire Delay

Assume an M3 wire 10mm long and 1.5μ wide driving a 0.1pF load

- What is the intrinsic wire delay?
- What size driver should you use?

Intrinsic delay:

- Wire cap depends on configuration (metal layer, spacing...)
  use 0.2fF per μ, so 0.2fF $\times 10,000 =$ 2pF
- Wire resistance $= 0.04\Omega \times \frac{10,000}{1.5} = 266\Omega$
- $\frac{1}{2}RC =$ 266ps

Wire Delay

Driver Size:

- FO4 implies input cap should be $\sim \frac{2.1pF}{4}$ =0.5pF
- (This overestimates optimal, but is a reasonable approximation)

If wire is 20mm long, intrinsic delay scales by $4\times$

- Delay is now 1.1ns!!

Wire Delay and Wire Width

Can reduce wire delay by making wires wider

- Resistance decreases with increased width
- Capacitance grows more slowly
  - fringe capacitance doesn't change

Using example with our M3 wire

- Increase width from 1.5 to 3μ
  - resistance is now $0.5\times$
  - capacitance increases by 1.3 to 1.4$\times$ (depends on spacing...)
- New delay is now 0.65$\times$

Wire Delay and Wire Width

Jointly increasing width and spacing

- Increasing spacing of wires from 1 to 3μ
  - decreases capacitance by 20–30%
- New delay is now 0.55$\times$

Moving to M4 will make this even better due to increased aspect ratio

Long Wire Drive Approaches

1. Repeater insertion and critical distance
2. Low swing signaling
   - active regeneration
3. Current-mode communication, current direction sensing signals
4. Wave pipelining

Wire Modeling: Elmore Delay

Elmore model first used in 1980's to model delay of transistor level circuits:

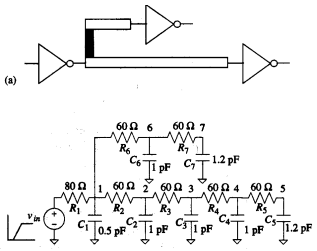
1. Model transistor as resistor driven by voltage source
2. Model wire as a series of RC segments
3. Delay is calculated as:

$$T_{dn} = \sum_{i \in P(n)} R_i C_{di}$$

   - n is the node for which we are calculating the delay
   - $P(n)$ is the path from the root of the tree to node n
   - C_{di} is the sum of capacitors downstream from resistor R_i

This model supports hierarchical interconnect and load structures.

Wire Modeling: Elmore Delay



The Elmore delay from the root to node 5 is calculated as follows:

$$\begin{aligned} T_{d5} &= R_1(C_1+C_2+C_3+C_4+C_5+C_6+C_7) \\ &+R_2(C_2+C_3+C_4+C_5)+R_3(C_3+C_4+C_5) \\ &+R_4(C_4+C_5)+R_5C_5 \end{aligned}$$

Properties of Elmore Delay

The Elmore model has some significant advantages:

1. Overestimation of delay
2. Closed-form equation
3. Structural format easy for designers to understand and calculate
4. Linear-time complexity to solve for interconnect
   - can complete timing rollups of huge systems in minutes

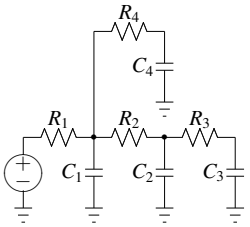
Properties of Elmore Delay

5. Hierarchical representation
   - Off-path loads simple model of total capacitance
   - Hierarchical delay calculation
     - calculate delay to branching point
     - add this to downstream delay of each branch
6. More accurate than simple π model

The main disadvantage:

1. only a first-order delay model - still not very accurate!

Elmore Example



For $R_1 = 20\Omega, R_2 = 25\Omega, R_3 = 25\Omega, R_4 = 30\Omega$, and $C_1 = 0.3$pF, $C_2 = 0.5$pF, $C_3 = 0.8$pF, $C_4 = 0.8$pF

$$T_{d3} = R_1(C_1+C_2+C_3+C_4)+R_2(C_2+C_3)+R_3C_3$$

$$T_{d3} = 20(0.3+0.5+0.8+0.8)+25(0.5+0.8)+25\times 0.8$$

$$T_{d3} = 100.5\text{ps}$$

Accurate Wire Delay Models

Picoseconds matter in high performance design.

- Hence more accurate wire delay models are needed

Asymptotic Waveform Analysis (AWE) is common means of improving wire models

- Based on work from the early 1990's
- Known as a "moment-matching" technique
- Applied to developing **model order reduction**

Moment Matching

- AWE approximates dominant poles
- The poles can be used to generate
  - time domain responses (time constants)
  - frequency domain responses
- Dominant poles are generated in AWE by *moment matching*
- Moments:
  - defined in classical probability mechanics and theory express frequency domain coefficients
  - can easily be calculated for linear circuits in general
  - can be mapped to a set of dominant poles and zeros

Calculating Moments

The transfer function $V_{in} = \delta(t)$ of a circuit can be expressed as:

$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1+a_1 s+a_2 s^2+\cdots+a_i s^i}{1+b_1 s+b_2 s^2+\cdots+b_j s^j}$
where $j > i$

This can be approximated in the complex frequency domain as a series in powers of s:

$H(s) = m_0 + m_1 s + m_2 s^2 + m_3 s^3 + \cdots$

The m coefficients are the moments we will calculate.

Calculating Moments

Setting these two equations equal to each other and multiplying by the denominator produces the form:

$(1 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4)(m_0 + m_1 s + m_2 s^2 + \cdots) =$
$1 + a_1 s + a_2 s^2 + a_3 s^3$

for a fourth order circuit. By collecting the first four power of s terms we derive:

$a_1 = m_0 b_1 + m_1$
$a_2 = m_0 b_2 + m_1 b_1 + m_2$
$a_3 = m_0 b_3 + m_1 b_2 + m_2 b_1 + m_3$

Calculating Moments

For an RC circuit the DC gain is 1, so $a_0 = 1$ and $a_0 = m_0$. The next four s terms express the coefficients of the pole polynomials in terms of m_j:

$0 = m_0 b_4 + m_1 b_3 + m_2 b_2 + m_3 b_1 + m_4$
$0 = m_1 b_4 + m_2 b_3 + m_3 b_2 + m_4 b_1 + m_5$
$0 = m_2 b_4 + m_3 b_3 + m_4 b_2 + m_5 b_1 + m_6$
$0 = m_3 b_4 + m_4 b_3 + m_5 b_2 + m_6 b_1 + m_7$

Solving Poles and Zeros

These equations are used to solve the following matrix:

$$\begin{bmatrix} m_0 & m_1 & m_2 & m_3 \\ m_1 & m_2 & m_3 & m_4 \\ m_2 & m_3 & m_4 & m_5 \\ m_3 & m_4 & m_5 & m_6 \end{bmatrix} \begin{bmatrix} b_4 \\ b_3 \\ b_2 \\ b_1 \end{bmatrix} = - \begin{bmatrix} m_4 \\ m_5 \\ m_6 \\ m_7 \end{bmatrix}$$

The first 8 m_j's are used to calculate the poles (b's) and zeros (a's) for a fourth order circuit.

Calculating Moments

The above method only works well if the moments (m's) are easy to calculate.

- Each moment m is different for every node
- Set the cap current and voltage for RC node in the network
- Solve for each moment i independently
- Solving for m_0, we set $s = 0$ giving the dc solution
  - this is equivalent to the Elmore delay!
- Solving for m_1 gives the standard deviation σ

One can match moments in AWE by expanding our original equation into partial fractions (the pole residue form)

Model Reduction

Accurately modeling interconnect requires at least a π model

- The π circuit contains three variables for each stage:
  - C_l, R, and C_r

If we need four π sections for a $\sim$ 5% accuracy, this results in many simulations

Model Reduction

- Cells are typically characterized uses the following information:
  1. input signal transition time
  2. load capacitance
- These normally are skewed across five points each, for 25 simulations
- We therefore want to model our interconnect load as a single **effective capacitance** C_{eff}
- This needs to relate our 50% switching delay, and our 20-80% (or 10-90%) transition times.

Model Reduction

- Waveforms have three basic sections:
  1. a quadratic waveform up to the 20% transition point
  2. a ramp-like waveform from 20% to 50-60%
  3. an exponential decay to the rail
- We want to approximate the delay to the 50% switching point with C_{eff}
- No single C_{eff} can model the exponential tail

C_{eff} Calculation

Select two k-factor equations:

$$t_d = k(t_{in}, C_L)$$
$$t_{r/f} = k'(t_{in}, C_L)$$

Select time points t_{20} and t_{50} that are related to the delay and transition times of the driver by

$$t_{50} = t_d + \frac{t_{in}}{2}$$
$$t_{20} = t_d + \frac{t_{in}}{2} - \frac{t_{r/f}}{2}$$

C_{eff} Calculation

We can model these regions as:

$$V_{out}(t) = \begin{cases} V_t - ct^2, & 0 \le t \le t_{20} \\ a + b(t - t_x), & t_{20} \le t \le t_{50} \end{cases}$$

where a, b, and c determine the constants in k

Setting a π model equal to a pure capacitor gives the following solution:

$$\frac{1}{t_{50}} \int_0^{t_{50}} I_\pi(t)dt = \frac{1}{t_{50}} \int_0^{t_{50}} I_{C_{eff}}(t)dt$$

Algebraic manipulation yields the approximate C_{eff} calculation:

$$C_{eff} = C_l + C_r \left[1 - \frac{RC_r}{t_{50} - \frac{t_{20}}{2}} + \frac{(RC_r)^2}{t_{20}\left(t_{50} - \frac{t_{20}}{2}\right)} e^{-\frac{t_{50} - t_{20}}{RC_r}} \left(1 - e^{-\frac{t_{20}}{RC_1}} \right) \right]$$

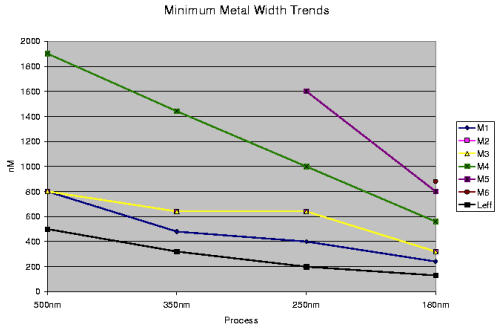
C_{eff} Calculation

Iterative solution:

- Start with initial guess of $C_{eff} = C_{tot}$
- Simulate the $k()$ and $k'()$ equations for t_d and $t_{r/f}$
- Calculate t_{50} and t_{20} from above equations
- Substitute into C_{eff} approximation from previous slide
  - this gives a C_{eff} estimate
- If this and previous C_{eff} estimate are within tolerance, quit else iterate

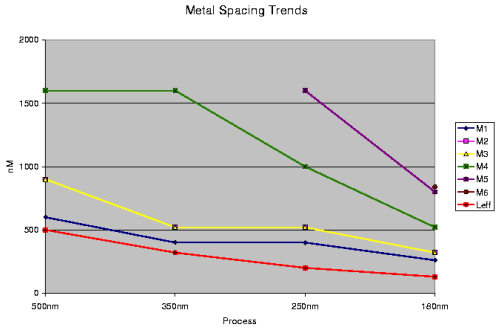
Minimum Metal Width Scaling

Minimum metal width, Intel Processes



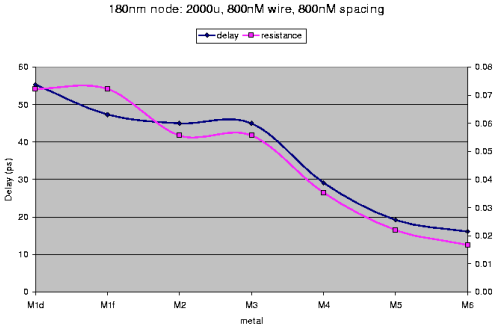
Minimum Metal Spacing Scaling

Minimum metal spacing, Intel Processes



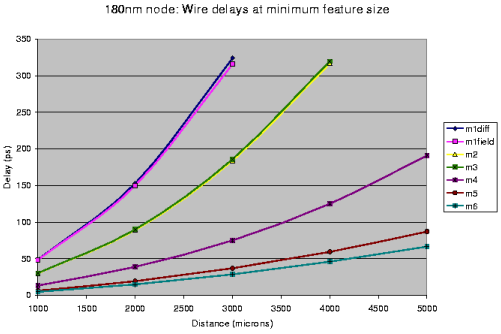
Wire Resistance Ladder

Wire resistance for different metal layers



Wire Delay Ladder

Wire delays for minimum size wires



Electromigration Physics

Electromigration caused when electrons accelerated through electric field collide with ions in the metal lattice

- An issue when current density reaches “critical velocity” $J = \sigma E$
- Collisions result in physical relocation of ions in lattice
- Depletion (holes) form in some places, and accumulation (hill) in another
- Depletion can exacerbate current density, resulting in open circuit
- Accumulation can result in short circuit to other metal lines

modeling includes RMS currents, and bi- or uni-directionality of current

Review

1. Three primary model characteristics of wires (RLC)
2. Simple resistance model for wires
3. Relative resistance of copper and aluminum
4. The two simple capacitance models for a wire
5. Magnitude of fringe capacitance relative to plate cap
6. Impedance of a wire
7. What is an inductor L
8. Inductor model terminals, and their behavior
9. Design of a PC Board microstrip

Review

1. Inductive crosstalk
2. Effect of inductive loop size in inductive cross talk
3. Self-inductance vs mutual inductance
4. Scaling of parameters in interconnect scaling that are not part of transistor scaling (length, thickness, . . .)
5. RC scaling in interconnect
6. Effect of aspect ratio in interconnect, and how it is scaling
7. Cladding, and barrier cladding

Review

1. Inter-layer dielectric scaling and values
2. How edge rates relate to inductance
3. Scaling of on-chip self-inductance (rise time, propagation velocity, attenuation constant)
4. Skin effect
5. Mechanism that causes inductive ringing
6. Design techniques to reduce induction
7. Wire delay models - resistive, impedance, time of flight

Review

1. How wire delay models scale and their effect on wire length
2. Design techniques to reduce capacitive coupling
3. Process methods of reducing crosstalk (κ)
4. Wire delay models: L, π, T
5. Calculation of wire delay using simple π model
6. Design techniques to reduce long wire delay
7. Elmore wire delay
8. Benefits and drawbacks of Elmore delay

Review

1. Calculate Elmore delay of a circuit network
2. Basic understanding of AWE, moment matching, how moments are generated and solved.
3. Other representations of moments m_0 and m_1
4. Two parameter models for circuit and wire delays
5. Why π model is not efficient for cell-based design modeling
6. Model order reduction and effective capacitance C_{eff} model
7. How electromigration physically displaces metal molecules