Homework Assignment 4

CS/ECE 6810: Computer Architecture

March 14, 2018

Memory Hierarchy: Cache

Due Date: 3/27/2018

(100 points)

Important Notes:

- Solutions turned in must be your own. Please, mention references (if any) at the end of each question. Please refrain from cheating.
- All solutions must be accompanied by the equations used/logic/intermediate steps. Writing only the final answer will receive **zero** credit.
- All units must be mentioned wherever required.
- Late submissions (**after 11:59 pm on 03/27/2018**) will not be accepted
- All submissions must be in PDF only. Scanned copies of handwritten solutions will not be accepted as a valid submission.

1. Cache Hierarchy (20 points): Consider a processor with the following memory organization: L1 Cache, L2 Cache, L3 Cache and main memory. Each cache stores both tags and data. The data and tag arrays are going to be accessed with the same index value. Assume that the processor does **serial** tag/data look-up (first tag lookup and then data access) for L2 and L3 caches and **parallel** tag/data look-up for L1 cache. The table given below provides the time take to access the tag and data arrays in cycles.

Cache Level	Tag Access	Data Access	Hit rate
L1 (32KB)	1	-	50%
L2 (1 MB)	3	18	55%
L3 (8MB)	25	85	75%
Main Memory (8GB)	-	440	-

Find the number of cycles required to complete 2000 load instructions accessing this hierarchy.

2. **Performance Metric (20 points):** Consider a processor with a cache that has a hit time of 5 cycles. If a miss occurs, then the penalty would be 150 cycles. Calculate AMAT if the miss rate of this cache is 20%.

3. **Cache Addressing (30 points):** Consider a processor using 2 cache levels. Level-1 cache is a 32KB direct mapped cache with 16B blocks used for both instructions and data. Level-2 is a 1MB, 4-way set associative cache with 64B cache lines. Assume that the processor can address up to 8GB of main memory.
   (a) Find the number of bits for tag, index, and offset for level-1 and level-2 caches.
   (b) Compute the size of the data and tag arrays in KB for each level.

4. **Cache Replacement Policies (30 points):** Consider a 2-way set associative cache with two sets. When running two different programs on this machine, the following access patterns are observed.
   - Program 1: C,A,B,D,B,F,C,E,A,D,B,F,A,B,C,E,B,A,F,D.
   - Program 2: D,F,C,B,A,A,F,C,D,D,A,B,A,B,C,E,B,A,B,D.

   Assuming that blocks A, B, and C are mapped to set 1 and blocks D, E, and F are mapped to set 2, compute the miss rates for each program (running solely) when Ideal, LRU, and MRU replacement policies are applied.