

1-

Access order – L1 → L2 → L3 → main memory.

Since data access happens only after the tag hit occurs in case of serial tags, we need to consider the data penalty only for hits. But for a miss, the data penalty can be ignored.

For a single load instruction, the memory access time for the given structure is -
 $.5*1 + .5*(.55*(1+3+18) + .45*(.75*(1+3+25+85) + .25*(1+3+25+440))) = 52.16875$

For 2000 load instructions the total number of cycles = $2000*52.16875 = 104337.5$ cycles

2-

$$AMAT = t_h + r_m * t_p$$

$$AMAT = 5 + 0.2*150 = 35$$

3-

$$\text{address bits (memory)} = 8\text{gb} = 2^{33} \text{ B} = 33$$

For L1 cache:

$$\text{byte offset} = 16\text{B} = 2^4 \text{ B} = 4$$

$$\text{index bits} = 32*2^{10}/2^4 = 2^{11} \text{ B} = 11$$

$$\text{tag bits} = 33-4-11 = 18$$

$$\text{tag array} = (18*2^{11})/2^{13} = 18/4 \text{ KB} = 4.5 \text{ KB}$$

$$\text{data array} = 32 \text{ KB}$$

For L2 Cache:

$$\text{byte offset} = 64\text{B} = 2^6 \text{ B} = 6$$

$$\text{index bits} = 2^{20}/4*2^6 = 2^{12} \text{ B} = 12$$

$$\text{tag bits} = 33-6-12 = 15$$

$$\text{tag array} = (15*4*2^{12})/2^{13} = 30 \text{ KB}$$

$$\text{data array} = 1\text{MB}$$

4-
a- first pattern

sequence	IDEAL					LRU					MRU						
	hit(0)/miss(1)	set1		set2		hit(0)/miss(1)	set1		set2		hit(0)/miss(1)	set1		set2			
C	1	C				1	C				1	C					
A	1	C	A			1	C	A			1	C	A				
B	1	C	B			1	B	A			1	C	B				
D	1	C	B	D		1	B	A	D		1	C	B	D			
B	0	C	B	D		0	B	A	D		0	C	B	D			
F	1	C	B	D	F	1	B	A	D	F	1	C	B	D	F		
C	0	C	B	D	F	1	B	C	D	F	0	C	B	D	F		
E	1	C	B	D	E	1	B	C	E	F	1	C	B	D	E		
A	1	A	B	D	E	1	A	C	E	F	1	A	B	D	E		
D	0	A	B	D	E	1	A	C	E	D	0	A	B	D	E		
B	0	A	B	D	E	1	A	B	E	D	0	A	B	D	E		
F	1	A	B	F	E	1	A	B	F	D	1	A	B	F	E		
A	0	A	B	F	E	0	A	B	F	D	0	A	B	F	E		
B	0	A	B	F	E	0	A	B	F	D	0	A	B	F	E		
C	1	C	B	F	E	1	C	B	F	D	1	A	C	F	E		
E	0	C	B	F	E	1	C	B	F	E	0	A	C	F	E		
B	0	C	B	F	E	0	C	B	F	E	1	A	B	F	E		
A	1	A	B	F	E	1	A	B	F	E	0	A	B	F	E		
F	0	A	B	F	E	0	A	B	F	E	0	A	B	F	E		
D	1	A	B	D	E	1	A	B	F	D	1	A	B	D	E		
11/20 = .55 55.00%						15/20=7.5 75.00%						11/20 = .55 55.00%					

b- second pattern

sequence	IDEAL					LRU					MRU						
	hit(0)/miss(1)	set1		set2		hit(0)/miss(1)	set1		set2		hit(0)/miss(1)	set1		set2			
D	1			D		1			D		1			D			
F	1			D	F	1			D	F	1			D	F		
C	1	C		D	F	1	C		D	F	1	C		D	F		
B	1	C	B	D	F	1	C	B	D	F	1	C	B	D	F		
A	1	C	A	D	F	1	A	B	D	F	1	C	A	D	F		
A	0	C	A	D	F	0	A	B	D	F	0	C	A	D	F		
F	0	C	A	D	F	0	A	B	D	F	0	C	A	D	F		
C	0	C	A	D	F	1	A	C	D	F	0	C	A	D	F		
D	0	C	A	D	F	0	A	C	D	F	0	C	A	D	F		
D	0	C	A	D	F	0	A	C	D	F	0	C	A	D	F		
A	0	C	A	D	F	0	A	C	D	F	0	C	A	D	F		
B	1	B	A	D	F	1	A	B	D	F	1	C	B	D	F		
A	0	B	A	D	F	0	A	B	D	F	1	C	A	D	F		
B	0	B	A	D	F	0	A	B	D	F	1	C	B	D	F		
C	1	B	C	D	F	1	C	B	D	F	0	C	B	D	F		
E	1	B	C	D	E	1	C	B	D	E	1	C	B	E	F		
B	0	B	C	D	E	0	C	B	D	E	0	C	B	E	F		
A	1	B	A	D	E	1	A	B	D	E	1	C	A	E	F		
B	0	B	A	D	E	0	A	B	D	E	1	C	B	E	F		
D	0	B	A	D	E	0	A	B	D	E	1	C	B	D	F		
9/20=.45 45.00%						10/20=0.5 50.00%						12/20=0.6 60.00%					