To be completed the week of **8/31/2015**. Lab reports should be turned in by **one week following your section by 5:00 PM** electronically from the course website. Please attach any hand calculations to the report.Names:_____

Single-Stage Amplifiers

In this lab, single-stage voltage amplifiers, will be introduced and designed. For the lab we will use two transistors, namely the 2N3904 NPN bipolar transistor and its PNP counterpart, the 2N3906.

In this experiment, the following circuits will be designed and constructed and their performance validated both experimentally and in simulation.

1. Single Stage PNP Amplifier
2. Current Mirror Biased NPN Amplifier

Prelab

All circuits for each experiment should be designed and simulated using your favorite SPICE tool before the lab. Results from the experiment should be compared to your simulation results and hand calculations.

Experiment 1: PNP Common-Emitter Amplifier

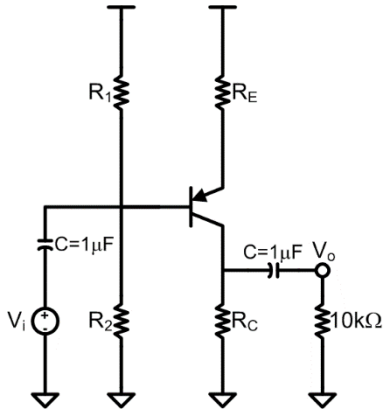

Figure 1. PNP Common-emitter amplifier

The common-emitter amplifier shown above uses negative feedback to create a stable bias point, regardless of variations in β and V_{BE}, assuming the following conditions are met:

$$V_{BB} \gg V_{BE}$$

$$R_E \gg \frac{R_B}{\beta + 1}$$

where V_{BB} is the voltage on the base and R_B is the parallel combination of R_1 and R_2. For further reading, please look at pages 188-214 of Razavi (or the attached handout).

1. For the circuit shown in Figure 1, using a supply voltage of 12V and the large capacitors are 1μF, calculate values of R_1, R_2, R_C and R_E that will result in the transistor operating in the FAR with a collector current, I_C, of 5 mA. Choose R_C such that the voltage drop across it is 4 V and R_E such that its voltage drop is 2 V. Enter your values in the table below, using one column for the calculated value and one for the closest 5% tolerance resistor you can find to the calculation.

	Calculation	Standard 5% Resistor
R_1		
R_2		
R_E		
R_C		

2. Simulate your circuit to find the DC bias point of the amplifier. During the lab you should build the circuit and compare to your simulation results to your measured results:

	Simulation	Measurement
I_C		
I_B		
V_B		
V_E		
V_C		

3. Based on the DC bias point, calculate the small-signal parameters and estimating the voltage gain as follows, calculate a value for the voltage gain:

$$A_v \approx -\frac{g_m R_C}{1 + g_m R_E}$$

4. Simulate the circuit using AC analysis and verify the calculated gain and pole frequencies. Using a signal generator and oscilloscope, verify these results in measurement.
5. Increase the input amplitude to 1-V to see what happens to the output waveform

	Calculation	Simulation	Measurement
Av			
FL			
FH			

Experiment 2: Current Mirror Biased Common-Emitter (CE) Amplifier

For this experiment, we use the current mirror of the first lab to bias the NPN transistor, Q_1 to act as a CE amplifier. We will use a similar configuration when we start investigating differential pairs that will become the basis for operational amplifiers.

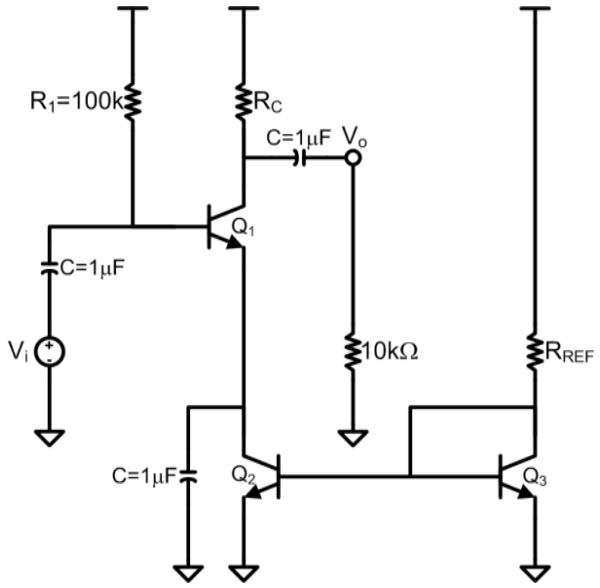

Figure 2. Wilson Current Mirror

1. For the circuit shown in Figure 1, using a supply voltage of 12V, calculate values of R_{REF}, that will result in the transistor, Q_1, operating in the FAR with a collector current, I_C, of 5 mA. Using convention from the text, choose R_C based on recommendations for voltage drops from the text. Enter your values in the table below, using one column for the calculated value and one for the closest 5% tolerance resistor you can find to the calculation.

	Calculation	Standard 5% Resistor
R_{REF}		
R_C		

2. Simulate your circuit to find the DC bias point of Q_1. During the lab you should build the circuit and compare to your simulation results to your measured results:

	Simulation	Measurement
I_C		
I_B		
V_B		
V_E		
V_C		

3. Based on the DC bias point, calculate the small-signal parameters of Q_1 and calculate the voltage gain; You will need to use inspection analysis for this!
4. Simulate the circuit using AC analysis and verify the calculated gain and the pole frequencies (FL and FH). Using a signal generator (Amplitude = 100mV, varying the frequency) and oscilloscope, verify these results in measurement.
5. Increase the input amplitude to 1-V to see what happens to the output waveform.
6. Note: In the measurement the device can heat up resulting in "thermal runaway". You can use negative feedback to fix this (e.g., RE).

	Calculation	Simulation	Measurement
Av			
FL			
FH			

Conclusions and follow up

1. What is the purpose of the capacitor from collector to ground for transistor Q_2? Try removing it and examine the circuits performance. Does gain increase, decrease, stay the same? What about the DC operating point?

2. Generally summarize what causes the differences between hand calculations / simulations and measured values.

3. What happened to the signal as you increased the input amplitude? Why?