CS/EE 6810: Computer Architecture

- Background: CS 3810 or equivalent, based on Hennessy and Patterson's Computer Organization and Design

- Text for CS/EE 6810: Hennessy and Patterson's Computer Architecture, A Quantitative Approach, 5th Edition

- Topics
  - Measuring performance/cost/power
  - Instruction level parallelism, dynamic and static
  - Memory hierarchy
  - Multiprocessors
  - Storage systems and networks

Lectures

- Class format:
  - Most lectures on YouTube ***BEFORE*** class
  - Use class time for lecturing, discussions, clarifications, problem-solving, assignments

Organizational Issues

- Office hours, MEB 3414, by appointment
- TAs: Padmashree TS, Zinnia Mukherjee, see class webpage for office hrs
- Canvas for hw submissions, announcements, grades
- Special accommodations, add/drop policies (see class webpage)
- Class web-page, slides, notes, and videos at http://www.cs.utah.edu/~rajeev/cs6810

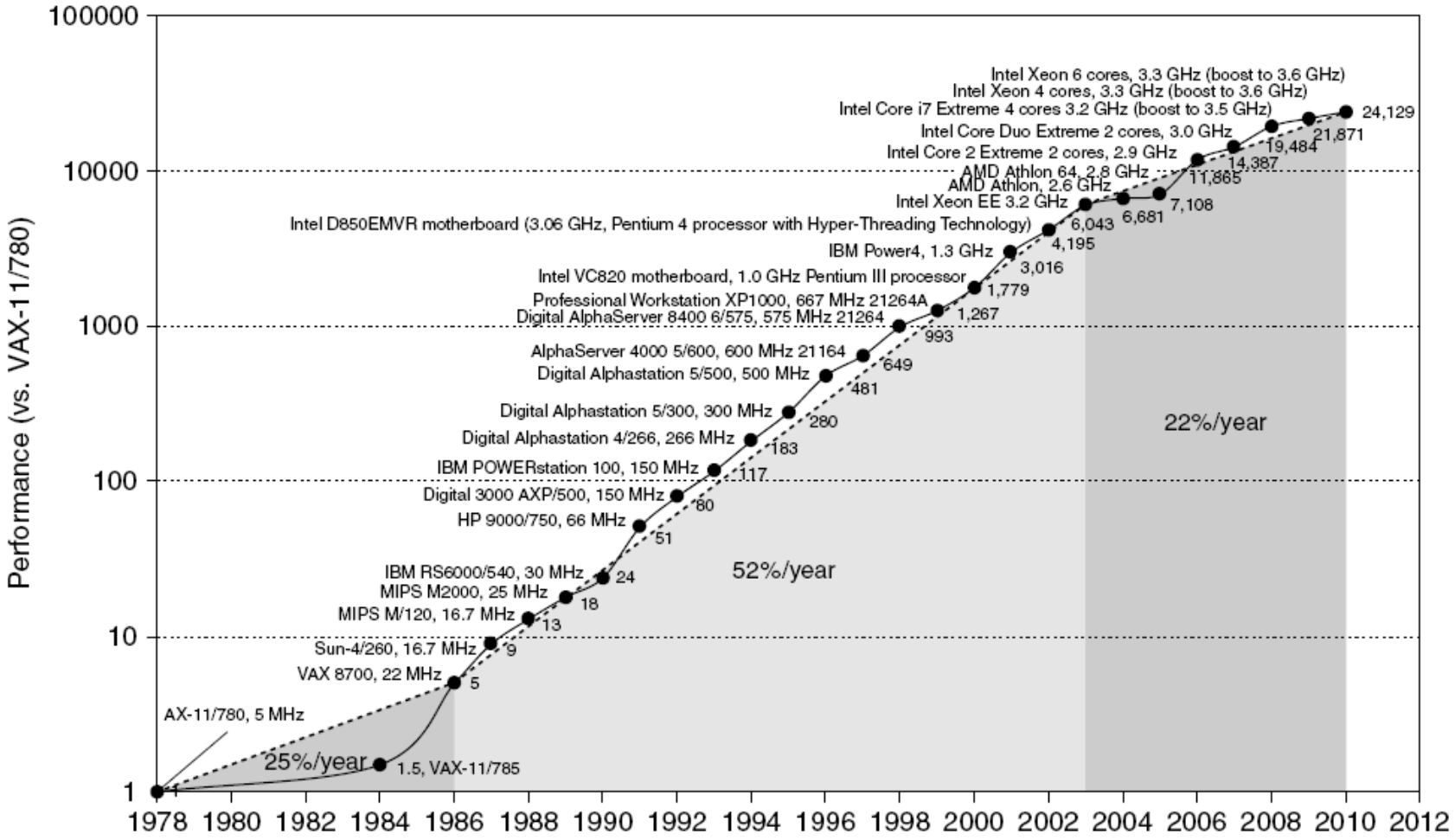
Grading

- Midterm (25%), Final exam (25%), Homeworks (50%)
- We will drop your lowest homework score
- No tolerance for cheating

Lecture 1: Computing Trends, Metrics

- Topics: (Sections 1.1 - 1.5, 1.8 - 1.10)
  - Technology trends
  - Metrics (performance, energy, reliability)

Historical Microprocessor Performance

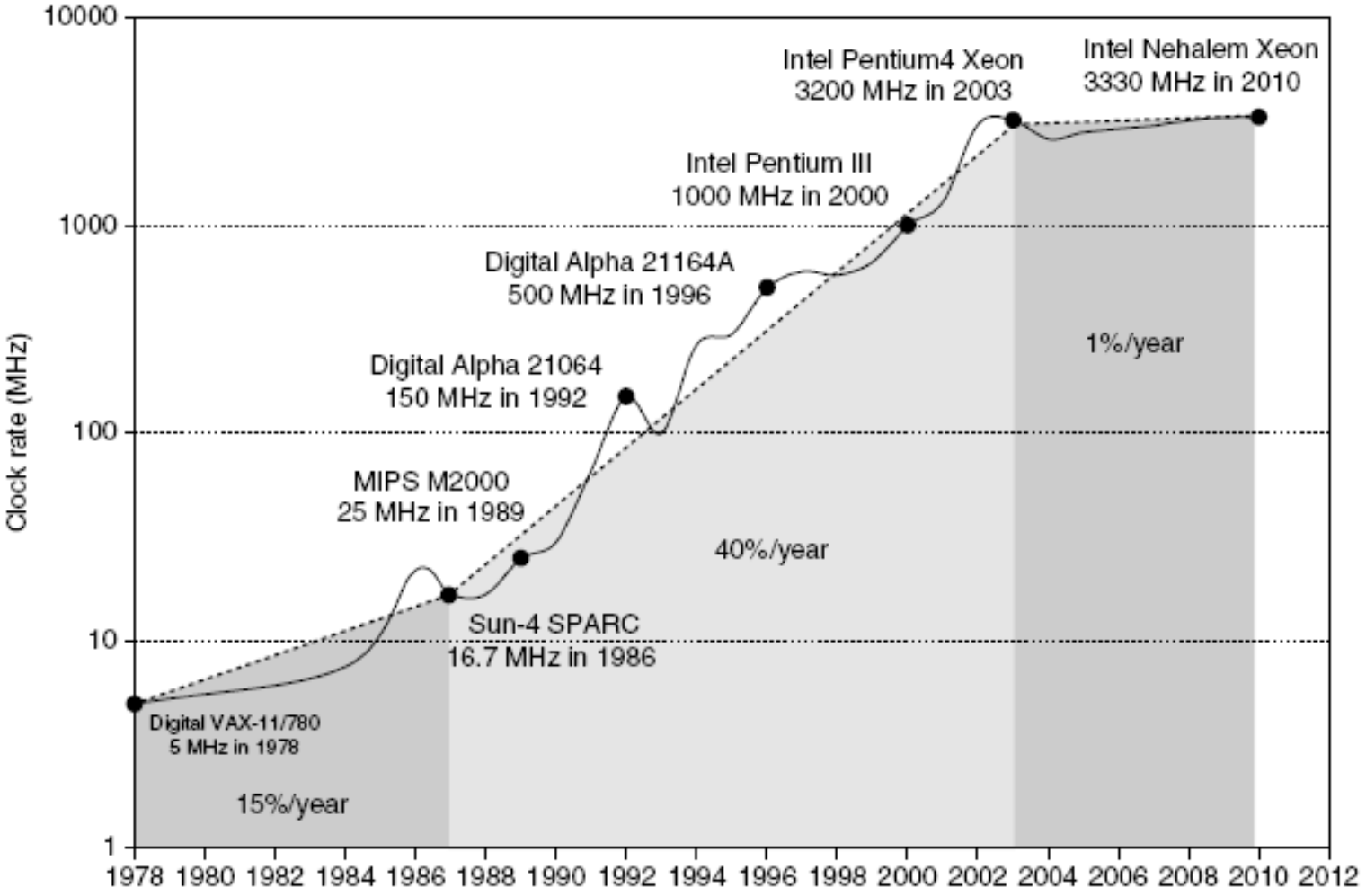


Source: H&P textbook

Points to Note

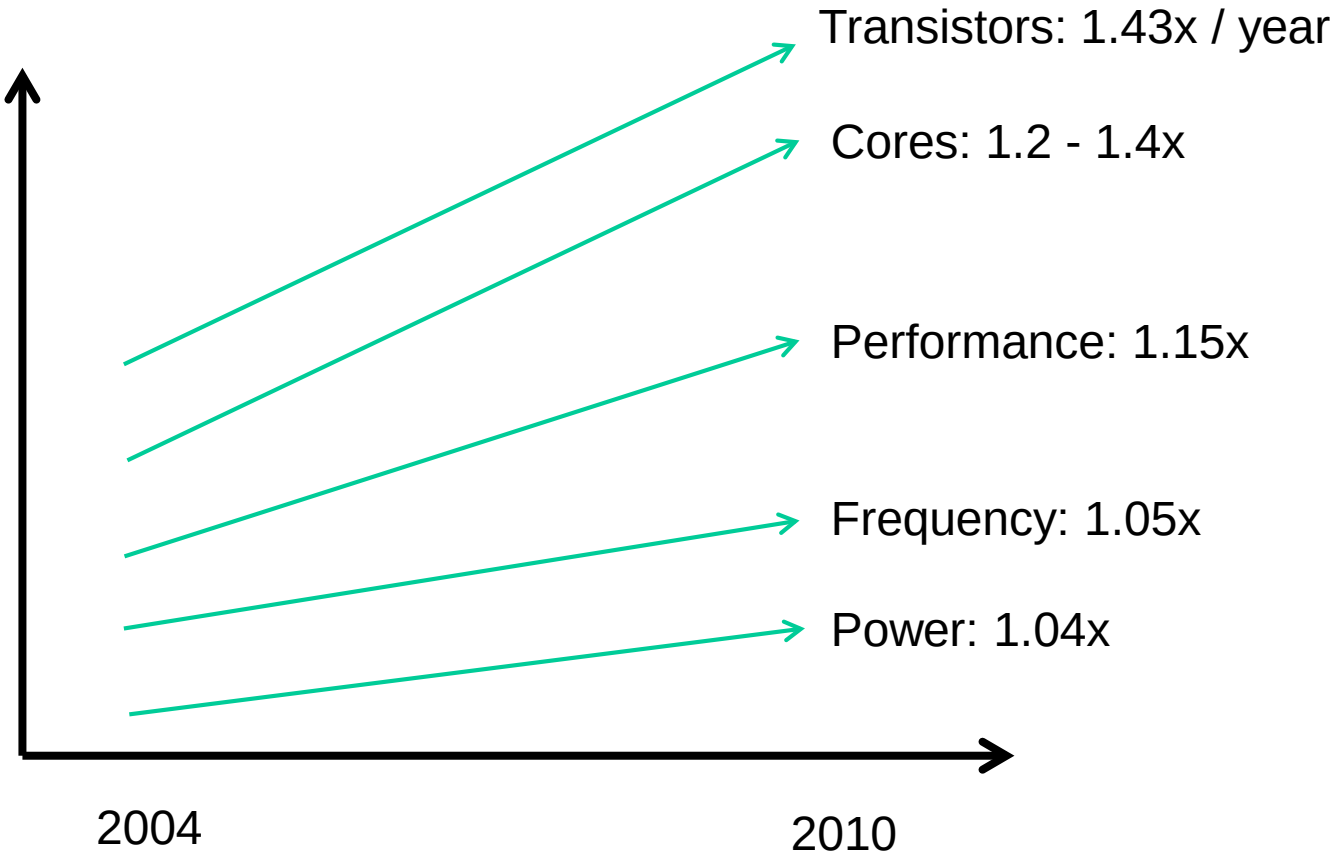
- The 52% growth per year is because of faster clock speeds and architectural innovations (led to 25x higher speed)
- Clock speed increases have dropped to 1% per year in recent years
- The 22% growth includes the parallelization from multiple cores
- End of Dennard scaling
- Moore's Law: transistors on a chip double every 18-24 months

Clock Speed Increases



Source: H&P textbook

Recent Microprocessor Trends



Source: Micron University Symp.

Processor Technology Trends

- Transistor density increases by 35% per year and die size increases by 10-20% per year… more functionality
- Transistor speed improves linearly with size (complex equation involving voltages, resistances, capacitances)… can lead to clock speed improvements!
- Wire delays do not scale down at the same rate as logic delays
- The power wall: it is not possible to consistently run at higher frequencies without hitting power/thermal limits (Turbo Mode can cause occasional frequency boosts)

What Helps Performance?

- Note: no increase in clock speed
- In a clock cycle, can do more work -- since transistors are faster, transistors are more energy-efficient, and there's more of them
- Better architectures: finding more parallelism in one thread, better branch prediction, better cache policies, better memory organizations, more thread-level parallelism, etc.

Title

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