Homework Assignment 2

CS/ECE 6810: Computer Architecture

January 31, 2018

Pipelining

Due Date: 2/13/2018

(90 points)

Important Notes:

- Solutions turned in must be your own. Please, mention references (if any) at the end of each question. Please refrain from cheating.
- All solutions must be accompanied by the equations used/logic/intermediate steps. Writing only the final answer will receive **zero** credit.
- All units must be mentioned wherever required.
- Late submissions (**after 11:59 pm on 02/13/2018**) will not be accepted
- All submissions must be in PDF only. Scanned copies of handwritten solutions will not be accepted as a valid submission.

1. **Pipelining Performance.** Consider a single-cycle processor in which the execution of every instruction completes in 10ns. The goal is to execute a user application that consists of 1000 instructions.
   i. If the single cycle processor can execute one instruction per cycle, find the CPU time. **(5 points)**
   ii. Assuming a 1ns additional delay for pipeline registers and perfect circuit partitioning and pipelining, find the speedup gained by making the processor 10-stage pipelined. Assume that 2 bubbles (NOPs) are necessary every 10 cycles for load and branch instructions.**(15 points)**

2. **Control Hazards.** Consider an in-order five-stage pipeline that determines the branch target by the end of the 3rd pipeline stage (i.e., the execute stage). To avoid branch-related stalls, the instruction set architecture (ISA) defines two branch delay slots. Assume that (a) all stalls in the processor are branch-related, (b) 20% of all instructions are branches, (c) a branch is taken 60% of the time, and (d) you could move two instructions from the taken side into the branch delay slot. What is the expected CPI for this processor? **(15 points)**

3. **Multi-cycle Instructions.** A pipelined architecture comprises instruction fetch (IF), instruction issue (IS), register read (RR), execute (EX), and write-back (WB) stages. Except EX, each stage requires one clock cycle to complete. The EX stage includes 4 functional units, each of which can perform a floating-point operation—e.g., ADD, SUB, MULT, DIV, load, and store. The table below shows the latency of the operations in terms of the number of clock cycles. The pipeline implements all necessary forwarding paths for the ALU operations.

	ADD	SUB	MULT	DIV	Load	Store
Latency	1	1	3	4	1	1

   i. Create a timing diagram for the following code showing the execution of the code in time (clock cycles). **(15 points)**
   ii. Identify all structural and data hazards in the following code. **(20 points)**

```
Load      F6, 20(R5)
Load      F2, 28(R5)
MUL       F0, F2, F4
SUB       F8, F6, F3
DIV       F10, F0, F6
ADD       F6, F8, F2
Store     F8, 50(R5)
```

4. **Points of Production and Consumption**. Consider an un-pipelined processor where it takes 36ns to go through the circuits and 0.5ns for the latch overhead. Assume that the point of production and point of consumption in the un-pipelined processor are separated by 12ns. Assume that half the instructions do not introduce a data hazard and half the instructions depend on their preceding instruction.
   i. What is the throughput of the processor with the un-pipelined architecture **(10 points)**
   ii. What is the throughput of the processor with a 12-stage pipeline? **(10 points)**