Homework Assignment 5

CS/ECE 6810: Computer Architecture

March 28, 2018

Cache Model, Address Translation and TLB

Due Date: 4/10/2018

(100 points)

Important Notes:

- Solutions turned in must be your own. Please, mention references (if any) at the end of each question. Please refrain from cheating.
- All solutions must be accompanied by the equations used/logic/intermediate steps. Writing only the final answer will receive **zero** credit.
- All units must be mentioned wherever required.
- Late submissions (**after 11:59 pm on 04/10/2018**) will not be accepted
- All submissions must be in PDF only. Scanned copies of handwritten solutions will not be accepted as a valid submission.

1. Virtually Indexed Caches (40 points)

Referring to the lecture slide on virtual address translation and TLB, explain the challenges if the number of bits in the page offset does not equal the number of bits in the sum of "Index" and "Byte" (Please see http://www.cs.utah.edu/~bojnordi/classes/6810/s18/slides/19-tlb.pdf). You are asked to identify the issues and their corresponding solutions from the literature.

Special Instructions for Question 1

- Strictly **NO** collaboration or brainstorming on this question is accepted.
- Mention **ALL** references used to answer this question. If no references are mentioned, **0 points** will be awarded.

2. Cache and Memory Model using CACTI (60 points)

CACTI(available at http://www.hpl.hp.com/research/cacti/) is an integrated cache and memory model for access time, cycle time, area, leakage, and dynamic power. You are asked to use CACTI 6.5 for investigating the impact of small and simple caches using a 32nm (0.032μm) CMOS technology node.

Consider a processor using 2 cache levels. **Level-1** cache is a 32KB direct-mapped cache with 16B blocks used for both instructions and data. **Level-2** is a 1MB, 4-way set associative cache with 64B cache lines. Assume that the processor can address up to 4GB of main memory

a. Compare the access time, energy, leakage power, and area of the caches mentioned above. Assume that both of the Level-1 and Level-2 caches are single bank.
b. Investigate the impact of varying associativity between 1 and 16 on the access time, energy, leakage, and area of the Level-2 cache.

Special Instructions for Question 2

- A table or graph with the results as well as a few lines of explanation on why the readings turn out to be so is required for full credit.