ECE/CS 6770 – Homework Assignment 2

Logical effort equations are summarized by the following:

- stage delay: $d = f + p$
- stage effort: $f = gh$
- path delay: $D = D_F + P \qquad D_F = \sum g_i h_i \qquad P = \sum p_i$
- path effort: $F = GBH \qquad G = \prod g_i \qquad B = \prod b_i$
- min path delay: $\hat{D} = NF^{\frac{1}{N}} + P$
- min stage effort: $\hat{f} = g_i h_i = F^{\frac{1}{N}}$
- transistor sizing: $C_{in_i} = \frac{g_i C_{out_i}}{\hat{f}}$

Now calculate logic optimizations, transistor sizing, effort, delay, and gate sizing in a path for the following.

1. Design three circuits for the function used in lab 1: $f = abcd + ae$. Draw the circuits. You can use logic symbols for NAND gates and inverters, otherwise draw the transistor level diagrams.
   - Use one three-input NAND gate and two two input NAND gates.
   - As a single complex gate plus an inverter, minimizing transistor counts.
   - As a footed domino gate and inverter. (Ignore the keeper.)
2. Find the logical effort for each of the gates in the above three designs.
3. Define the logical effort for each input in all three designs, including the precharge for the domino gate.
4. Assume the output load is equivalent to the load on input b. Assume the parasitics are the ceiling of the number of inputs divided by two.
   - Calculate the delay for each input for each of the gates. Rank them from fastest to slowest based on the worst case delay.
5. Calculate the gate sizes if the output load is equivalent to six times the load on input b.
6. Create a complex gate for the function $\overline{f} = ab + ac + bc$. Can you find a symmetrical design for the pullup and pulldown trees? Size the transistors.

1. Draw a domino gate for function $\overline{f} = ab + c$ that drives a fanout five load. Properly place and size the keeper relative to the domino function gates.
2. Does SRAM use ratioed logic?
3. How do you size the six transistors in an SRAM cell?
4. What is the activity factor of a domino pipeline?
5. Are there static gates in a domino pipeline?
6. What versions of domino pipelines do not have static gates? What are the advantages and disadvantages of these designs?
7. What is AOCV? At what technology nodes does it become important?
8. Design a domino pipeline that doesn't need a footer gate. How do you ensure that you don't get crowbar current?
9. What design styles favor pass transistor logic?
10. What design styles favor domino logic?
11. What is miller coupling, and how does it affect design robustness of dynamic gates?
12. What are the advantages and disadvantages of a sense amp when using pass transistor logic.
13. How can I reduce current in a sense amp?
14. What is single ended pass gate design?
15. How can you reduce variation using additional gates in a differential sense amp design?
16. How can I apply threshold voltages to improve pass gate design?
17. What are several **design** methods that can be used to mitigate variation in a gate?
18. What is a speed-independent design?
19. What is the difference between a bundled data asynchronous design and a delay insensitive asynchronous design?
20. Define the 1-of-4 encoding for delay insensitive handshaking.
21. What is the activity factor for dual rail design?
22. How is dynamic carrier injection mitigated?
23. Which protocol – 2 phase or 4 phase – would you use for long asynchronous communication links where most of the delay is in the wires?
24. How can I identify asynchronous logic from a design?