**Vikas Rao**

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**Subject:** Application for A. Richard Newton Young Student Fellow Program

**Motivation:** Explore research topics in design automation and verification of digital VLSI systems. Gain exposure in hardware formal verification, seek deeper knowledge of design-flows, CAD methodologies, core-technologies and their application in the semiconductor industry. Contribute my evaluations to the multidisciplinary field of EDA.

**Education/work:**

**Ph.D. Candidate, Computer Engineering, University of Utah, USA -** Fall 2016 - Present

- Advisor: Dr. Priyank Kalla

: +1-801-587-7617

: [kalla@ece.utah.edu](mailto:kalla@ece.utah.edu)

**Graphics Validation Engineer, Intel corporation, India** - 2009-2016

**M.S., VLSI, Manipal University, India -** 2008-2010

**B.E., Electronics and Communication Engineering, JSSATE, India** - 2004-2008

- Tezpur University B.Tech merit based scholarship

**Current Research Interest:**

**Design Automation and Hardware Verification**

- Computer algebra and algebraic geometry based formal hardware verification using symbolic computation.

Polynomial rings, finite fields, ideals, varieties, and Groebner basis.

- Automated debugging and correction of arithmetic circuits.

- Equivalence checking using miters and SAT/SMT tools.

**Related Projects:**

**Resolving Unknown Components In Arithmetic Circuits Using Computer Algebra Methods**

- This paper describes an algebraic approach to resolve the functionality of an unknown component in an arithmetic circuit so that the circuit implementation matches a given specification.

- Performed experiments on various finite field multipliers to demonstrate the efficiency of the approach against SAT-based implementation.

**Boolean Groebner Basis Reduction using Unate Cube Set Algebra for Verification**

- Co-authored the design and implementation of Groebner Basis reduction algorithms using Zero Suppressed Decision Diagrams.

- Performed experiments on Galois field multipliers which demonstrates the efficiency of the algorithms.

**Binate covering Problem**

- Implemented Binate covering problem algorithm for state minimization in asynchronous circuits using python.

**Bitcoin Hashing**

- Implemented the SHA-256 algorithm along with the bitcoin wrapper exercising crypto mining protocol.

- Performed synthesis and layout of the module with a custom-made library using Cadence Virtuoso, Synopsys design compiler,

Cadence SoC Encounter with a decent operating frequency meeting all design and timing constraints.

**Design & Characterization of Custom Cell Library**

**-** Developed a custom cell library for 0.6μ technology containing logic gates with varying drive strengths and inputs. Performed DRC, LVS, characterized the cells with Cadence ELC.

**Publications:**

- **Vikas Rao**, Utkarsh Gupta, Irina Ilioaea, Priyank Kalla, Florian Enescu, “**Resolving Unknown Components In Arithmetic Circuits Using Computer Algebra Methods**”(In review)

- Utkarsh Gupta, Priyank Kalla, **Vikas Rao**, “**Boolean Grobner Basis Reductions on Datapath Circuits Using the Unate Cube Set Algebra**”, International Workshop on Logic and Synthesis, 2017 (\*Best paper with student as first author award.\*)

- Utkarsh Gupta, Irina Ilioaea, Priyank Kalla, Florian Enescu, **Vikas Rao**, Arpitha Srinath “**Craig Interpolants in Finite Fields using Algebraic Geometry: Theory and Application**”(In review)

**Software Tools/Skills­­­:**

**Programming Languages:** C, Verilog, VHDL, Python, Ruby, Perl, Assembly, BASH, TCL

**Hardware Verification:**  ABC, Minisat, Picosat.

**Hardware Design:**  ISE, Cadence Virtuoso, Synopsys Design Compiler, SPICE, SIS.

**Other:**  Singular, LaTeX, Git, Modelsim, MS Office­­­

**Relevant Coursework:**

Testing & Verification of Digital Circuits Computer Architecture(spring 2018) Advanced Digital VLSI Design

Synthesis & Verification of Asynchronous VLSI Systems Advanced Algorithms

**Approximate Expense (June 24th -28th):**

Airfare from Salt Lake City to SFO – 250$-300$

Accommodation – 300$-350$