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**Goal**

Looking for challenging opportunities in the areas of Emulation/ASIC prototyping/post silicon validation and to be associated with a progressive organization that gives me scope to share my knowledge and technical skills and thrive in a hardworking team environment.

**Experience summary**

* **July 2008 – till date** working as **Senior Emulation Engineer** at **Intel Corporation, Bangalore, India**
* **Jan 2005 – June 2008** worked as **Component Design Engineer** at **Intel Corporation, Bangalore, India.**
* **June 2004 - Jan 2005** worked as **Component Design Engineer** at **Intel Corporation, Hillsboro, Oregon.**
* **Dec 2003 - March 2004** worked as **Student Intern** at **Intel Corporation, Folsom, California.**

**Combined 10 years experience in areas of Emulation / ASIC Prototyping and Post silicon System Validation:**

* ASIC prototyping with Mentor Graphics Veloce emulation platforms on Intel’s 22nm and 14nm GPU GFX core.
* Detailed experience in porting up to 70 million gates design on Veloce maximus emulation platform and Zebu ZSE1/ZSE2 emulators.
* Detailed experience in transaction based verification using Emulation.
* Hands on experience enabling Transaction based simulation acceleration (TBA) using Synopsys VCS simulator and Synopsys Zebu emulators.
* Experience with developing HDL Co-sim for simulation acceleration using Zebu emulators.
* Experience with using DINI based FPGA platforms with Virtex 5, Virtex 6 and Virtex 7 devices.
* Detailed knowledge of SCEMI and DPI based verification methodology and its implementation on Mentor Veloce and Synopsys Zebu Emulation platforms
* Experience in porting System Verilog Assertions and Coverage based methodology using transaction based verification on Emulation.
* Hands on experience with synthesis tools like Synplify Premier / Vivado / ISE / Precision.
* Hands on experience with Synopsys VCS RTL simulator.
* Exposure to System verilog, Test Bench development, trackers, checkers, assertions, and coverpoints.
* Experience with FPGA debug tools, Identify/Chipscope/ILA, CSA
* Platform validation experience on DDR2/DDR3 and PCI Express technologies for Intel Chipsets.
* Worked on Board level debug / signal integrity / system margin issues.
* Hands on experience in bring up of first silicon in the lab on multiple Intel Chipsets.
* Familiar with lab tools / Tektronics LA’s and O’scopes.

**Skill Set**

Languages: Verilog, C, VB, Perl, System Verilog

Operating Systems: UNIX, Windows

Technologies: SCEMI 2.0, PCIe, DDR, ZEMI3, TBX

Emulation platforms: Mentor Veloce, Eve Zebu-server

FPGA platforms: DINI DNV6-F2PCIE (V6 LX 330T), DINI DNV7F2B (V7- 2000T), Custom FPGA platforms (LX 760)

**Tools**

RTL Simulators: VCS, Modelsim

Synthesis tools: Synplify Premier, Xilinx ISE, Vivado , Zfast, Veloce RTLC

FPGA debug tools: Identify, Chipscope Pro, ILA 2.0 for V7 devices, ZPrd, CSA, Velwavegen

Other FPGA tools: Familiar with Certify for partitioning, Planahead, Coregen

Formal verification: 0in

Equivalence check: Conformal LEC

Post Silicon validation: Jtag based In-target-probe, Mem-stress,

Debug Equipment: Tektronics Logic analyzers, Oscopes, RST Pro

Statistical tool: JMP 5.1, Design of experiments (DOE)

**Academics**

* **California State University, Sacramento, California -** Masters of Science (Elec. Eng) - Graduated 05/2004
* **University of Mumbai, India -** Bachelors of Engineering - Graduated 06/2001

**Brief Project details**

**Simulation Acceleration using Transaction based Acceleration on Synopsys Zebu emulators**

**Duration:** Q1 2014 to current

**Location:** Bangalore

**Team Size:** 3

**Project details:** Intel 14nm and 10nm GFX IP for client/tablets.

PLI based simulation acceleration methods were yielding only a performance improvement in the range of 10 to 25x faster than simulation. Requirement from the RTL Verification team was at least 100x throughput on the emulator.

**Responsibilities:**

* Simulation profiling of sample set of test cases to identify the bottlenecks in the current simulation run.
* Re-architect driver component of the system verilog testbench to support DPI calls which in turn talk to transactor portion of the synthesizable HW by retaining the generator code with original functionality.
* Design of the software layer which handles DPI communication calls both from VCS to the DUT and DUT to VCS in the return path.
* Enabling zDPI based RTL checkers within the DUT for ease of debug and result checking.
* Responsible for the initial bring up and debug to make the design functional on the emulator.
* Single point of contact for co-coordinating various issues with Synopsys in the process of enabling this methodology for both emulator and VCS simulation problems.

**Achievements:**

* Transaction based simulation acceleration (TBA) using VCS simulator as the front end and the DUT mapped on the emulator gave a performance gain of approximately 150x faster than simulation.
* This helped maintain a cohesive environment across emulation and simulation whereby increasing the efficiency.
* This methodology was proven on a DUT of size approx 15 million ASIC gates using ZSE1 emulators.
* SCEMI 2.0 based streaming DPI calls were used for optimum performance.

**Impact to Org:**

This was one of the first projects at Intel to adopt TBA based simulation acceleration to enable early verification on GFX IP and thus helping the efficiency by providing verification engineers to run more cycles with random seeds and longer running test cases for better coverage resulting less bug proliferation to the emulation execution teams.

**Simulation Acceleration using Zebu platform on DUT > 10 million gates**

**Duration:** Q1 2013 to Q4 2013

**Location:** Bangalore

**Team Size:** 2

**Project details:** Intel 14nm and 10nm GFX IP for client/tablets

This requirement was driven from the RTL verification teams as the tests that they were executing on Simulation were taking multiple hours hence bringing down their efficiency.

**Responsibilities:**

* To deliver the HDL- CoSimulation solution using Zebu ZSE 1 emulators and VCS simulator.
* The average amount of gain in time as compared to simulation was around 10x to 25x using this solution.
* Hands on experience in designing the complete flow and integrating it in the current simulation environment with the least amount of impact to the existing regression infrastructure.
* Hands on the RTL synthesis using ZFast synthesis tool for ZSE1 emulation platform.
* Working knowledge in handling the clocks/ glue logic / testbench / static forces and optimizing pin count for optimum PLI communication across DUT and VCS simulator.
* Debugging of multiple issues using Zebu’s CSA debug methodology.
* Providing suggestions and feedback to the testbench teams through multiple level of simulation profiling to achieve the best throughput and performance gains on the emulator.

**Achievements:**

* Delivered 2 IP blocks of 12 million gates capacity to the verification team. Currently test is running approx 25x faster the regular simulation model.
* Quick turnaround time possible due to reuse of generator and the driver component of the testbench code.

**Impact to Org:**

Enabled early validation for the project there by enabling a Shift Left of the Verification Schedule by a quarter.

**ASIC prototyping for cluster level GFX IP’s on DINI FPGA platforms for < 5 million gates**

**Duration:**  Q3 2011 to Q4 2012

**Location:** Bangalore

**Team Size:** 3

**Project details:** Intel’s 22nm and 14nm GFX IP for client CPU’s

**Responsibilities:**

* Responsible to deliver a low cost ASIC prototyping solution to the GFX validation organization which could be scalable across multiple IP’s within the GFX Core.
* Complete ownership of RTL synthesis using Synplify premier and then porting edif for backend place and route on ISE or Vivado depending on the target device.
* Modeling non-synthesizable code into FPGA friendly RTL without impacting functionality.
* In-Circuit debug and design bring up of the DUT on the DINI Virtex 6 or DINI Virtex 7 FPGA platform.
* Weekly model spins for the new RTL drop for that particular DUT.
* Replicating suspected FPGA only failures on RTL simulation for ease of debug.
* Working with end users and stakeholders for debug needs on the FPGA platforms as and when requested.
* Coordinating with Interns for enabling automation based model build approach promoting reuse and efficiency.

**Achievements:**

* Able to deliver 5 IP blocks ported on DINI FPGA platforms to internal validation teams
* The IP blocks are in the range of 2 to 5 million ASIC gates and critical components of the GFX engine.

**Impact to Org:**

This low cost FPGA platform was able to find RTL bugs one quarter before the big box emulation models were ready, thus enabling an overall shift left for the project schedule.

**GPU emulation for Intel’s 22nm and 32nm processors**

**Duration:** Q4 2008 to Q3 2011

**Location:** Bangalore/Folsom, CA

**Team Size:** 2

**Design bring up on emulators**

**Responsibilities:**

* Hands on experience in porting 3d/media RTL on the Mentor Veloce emulators and releasing the emulation models for use of internal validation teams for 2 GPU projects.
* Successfully managed to bring up the design on emulation within 2 weeks from the simulation pass point. The success criterion was to get same basic tests passing on the emulator as compared to the simulations.

**Achievements:**

* These emulation models were extensively used by the GFX validation teams to run their post silicon GFX validation content on the emulators enabling them to find functional RTL bugs much before silicon tape out.
* Total gate count was nearly equal to 90M gates.

**Impact to Org:**

280 unique functional RTL bugs were found exclusively on these emulator platforms using the targeted test content, hence resulting in bug free first silicon.

**Enabling Synthesizable Coverage to enhance functional validation efficiency on Emulators**

The main objective here was to extract functional coverage feedback from the actual hardware by system validation team during runtime on emulator.

**Responsibilities:**

* Used an Internal tool to pre synthesize System Verilog Cover Point modules into synthesizable code and then porting the corresponding RTL instrumented into Veloce Emulation platform.
* With the help of enable based DPI calls, the effective runtime performance is also comparable.
* This enables an emulator end user to get real hardware feedback and assists in identifying plausible functional coverage gaps in the current test regression suite.
* Experience in completing end to end implementation of this project which included the initial Proof of Concept on smaller designs to understand and make sure this solution would work as expected.

**Impact to Org:**

This methodology is successfully used in validation across multiple GFX IP’s in emulation and is effective bringing down redundant test contents regression also yielding to better functional coverage across new features.

**Enabling SystemVerilog Assertions on emulation for enhanced debug capabilities.**

**Responsibilities:**

* Solely responsible for porting SV assertions in the emulation environment which would aid in the root cause of a functional issue.
* As part of the assertion enabling phase, enabled the flow to get the assertions from the RTL, porting them for making them synthesizable on Veloce emulation platform using the 0in SVA compiler and enabling the validation customers for debug and protocol verification.
* Successfully port 1,20,000 assertions and coverage instances on the emulators and this yielded in a huge improvement in the debug throughput time. In some instances, the debug time was brought down from weeks to a matter of minutes due to the accurate assertion firing exactly on the root of the failing unit.

**Achievement:**

This methodology has been taken as a standard procedure for the future emulation projects at Intel and is a huge success.

**Impact to Org:**

Using Assertions in emulation, the bug turnaround time to closure was reduced from couple of weeks to a few days due to the capability of assertion firing at the source for a complex pipe architecture.

**RTL debug and bug resolution**

**Responsibilities:**

* Primarily responsible for RTL debug and root causing multiple issues from emulation stand point.
* Worked closely with the GFX test content owners along with the RTL unit owners and validation teams to root cause several bugs at each stage of the project.

**Porting DPI compliant Trackers and Checkers on Mentor Veloce platforms.**

Trackers are basically Monitors which are written in verilog to track the transactions between units and modules. Checkers are basically extension of trackers and do a comparison of the tracker output with a golden reference as already defined. All the file I/O and system operations were done using DPI methodology based on SCEMI, where C functions were imported in the RTL and corresponding trackers or checkers dump were created as part of the emulation test logs.

**Responsibilities:**

* Synthesize and port the Gfx design RTL trackers and checkers into emulation by making them compatible and functional on emulators.
* Created a cohesive debug environment across the simulation and emulation ecosystem for ease and reuse of debug methodologies.

**Achievements:**

Totally close to 120+ tracker and checkers constructs were eventually supported over the total product cycle.

**Impact to Org:**

DPI checkers were extremely beneficial for the RTL validation teams as they could get real time visibility on the intra unit and inter module transactions and look for illegal or unsupported protocols without a capture thereby minimizing the use of trigger and waveform capture debug methodology resulting in efficiency improvement and better utilization of emulation cycles.

**System validation for Intel Centrino/ Centrino Duo 915/945/965 Mobile GMCH**

**Duration:** Q3 2005 to Q2 2008

**Location:** Bangalore/ Hillsboro, OR

**Team Size:** 4

**Brief project details:**

915/945/965 chipsets were predominantly mobile platform chipsets for the Intel Centrino and Intel Core 2 Duo generation platforms ranging from all thin and light and small form factor laptop designs.

* **DDR2 / DDR3:** I was part of the system validation team focusing on post silicon validation of Memory controller (MCH) of Intel’s mobility division. My main responsibilities were to work with junior engineers and run memory intensive test content on the validation platforms with various available DIMM loads across all possible combinations of Process/Voltage/Temperature conditions.
* Responsibilities included working with the firmware team to enable the First silicon boot up and subsequently characterize various timing parameters across multiple DIMM vendors supported on the platform in accordance with JEDEC Spec.
* Also characterized to failure, timing specs of DQ, DQS, Receven, Cmd, Ctrl, DIMMA/B ref, MCH ref to understand total System margin available at that particular PVT condition. We also used statistical analogies using Jump to find odd conditions and outliers which could hide a potential silicon bug.
* Worked closely with the design team right from the test plan development phase till product launch including support for Customer issues. Also owned the overall validation methodology and getting the tests working on automation using scripting so as to enable data collection on multiple platforms parallely.
* Also used LA and oscilloscopes for any debug as needed for root causing a memory corruption failure or an application hang and working with the design team for resolving and reverifcation of fix in the next silicon stepping.

**Tools used:** Trinity VB scripting compiler, ITP, Russian Mem stress, RST pro, O’scopes, LA

* **PCI Express Graphics/ DMI:** As part of the system validation team, my responsibilities were to verify the PHY layer for Intel’s mobile chipsets. Testing electrical characteristics of the PCI Express x 16 and x4 configs which included the differential eye capture and analysis. Use of Margin test mode to check the eye opening at the receiver using Intel Compliance Mode measurement standards. Also responsible for defining the exact bios default settings for the Icomp, Rcomp and the Analog Front End Load strobe. Also tested the tolerance on the margin DAC uptill data corruption for commercially available graphic cards.

**Tools used:** MARS- PEG/ DMI, ITP, commercial game stress tools, Oscopes, LA

* **Formal Verification:** I was responsible for complete formal verification activity of the PCI Express blocks for the Intel 945 chipsets. This consisted of 4 sub blocks which were Comp, PLL, DRC and Port. The Port blocks were basically the main PXP circuit blocks, others were the clock and the compensations circuit blocks for the Port. Tools used for this was Conformal Logic Error check (Lec) for the 1:1 comparisons with the schematic netlist and the corresponding RTL module. We used Alliance environment for the schematic and Motley was used for netlisting. Total number of bugs found totally were close to 30 including both RTL models and Schematic.
* **Functional Verification:** I was responsible for Functional verification of PCI Express sub blocks for Cantiga GMCH. The tools that we used were mainly Ultrasim from Cadence. We were provided with the Variable Change dump files (VCD) from the RTL model owners and we generated test benches using gentb in the ODIN environment. Netlist was done using genspice. Functions verified were like L0 to L0s to L1 state interchange, Active state power management, Squelch Entry + Exit, Digital Near end loop back on PCI Ex Graphics, Data Recovery Circuit Margin Mode entry + exit, Staggering validation for the 16 lanes.

**Conferences**

* Presented a paper in SNUG India 2014 (June 2014) in Bangalore, India on Novel Methods of Estimating Performance gain in simulation using Emulation.

**Communication Skills/Project Management**

* Exceptional organizing and planning skills with strong time management.
* Ability to adapt according to the situation and a quick learner.
* Dynamic team player who is consistently motivated toward success and completion of projects with an ability to work independently.
* Good communication skills with experience in working across multiple geo’s.
* Experience in resource mapping /training and ramp up of junior engineers and new hires.

**References**

* Available on request