**Vikas Rao**

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**Motivation:** Explore research topics in design automation and verification of digital VLSI systems. Gain exposure in hardware formal verification, seek deeper knowledge of design-flows, CAD methodologies, core-technologies and their application in the semiconductor industry. Contribute my evaluations to the multidisciplinary field of EDA.

**Education/work:**

**Ph.D. Candidate, Computer Engineering, University of Utah, USA -** Fall 2016 - Present

- Advisor: Dr. Priyank Kalla ([kalla@ece.utah.edu](mailto:kalla@ece.utah.edu))

: +1-801-587-7617

**Graphics Validation Engineer, Intel corporation, India** - 2009-2016

**M.S., VLSI, Manipal University, India -** 2008-2010

**B.E., Electronics and Communication Engineering, JSSATE, India** - 2004-2008

- Tezpur University B.Tech merit based scholarship

**Current Research Interest:**

**Design Automation and Hardware Verification**

- Computer algebra and algebraic geometry based formal hardware verification using symbolic computation.

Polynomial rings, finite fields, ideals, varieties, and Groebner basis.

- Automated debugging and correction of arithmetic circuits.

- Equivalence checking using miters and SAT.

**Related Projects:**

**Resolving Unknown Components in Arithmetic Circuits Using Computer Algebra Methods**

- This paper describes an algebraic approach to resolve the functionality of an unknown component in an arithmetic circuit such that the circuit implementation conforms to the given specification.

- Experimented with various finite field multipliers to demonstrate the efficiency of the approach against SAT-based implementation. Implemented the complete incremental SAT approach wrapper using python with picosat as underlying SAT-solver.

**Boolean Groebner Basis Reduction using Unate Cube Set Algebra for Verification**

- Co-authored the design and implementation of Groebner Basis reduction algorithms using Zero Suppressed Decision Diagrams.

- Conducted experiments on Galois field multipliers which demonstrates the efficiency of the algorithms.

**Binate covering Problem**

- Implemented the recursive Binate covering algorithm for state minimization of asynchronous circuits using python.

**Bitcoin Hashing**

- Implemented the SHA-256 algorithm with the bitcoin wrapper in Verilog to exercise crypto mining protocol.

- Performed synthesis and layout of the module with a custom-made library using Cadence Virtuoso, Synopsys design compiler,

Cadence SoC Encounter with a decent operating frequency meeting all design and timing constraints.

**Design & Characterization of Custom Cell Library**

- Developed a custom cell library for 0.6μ technology containing logic gates with varying drive strengths and inputs. Performed DRC, LVS, characterized the cells with Cadence ELC.

**Publications and Presentations:**

- **Vikas Rao**, Utkarsh Gupta, Irina Ilioaea, Priyank Kalla, Florian Enescu, “***Resolving Unknown Components in Arithmetic Circuits Using Computer Algebra Methods***”, International Workshop on Logic and Synthesis, 2018 (In review).

- Utkarsh Gupta, Priyank Kalla, **Vikas Rao**, “***Boolean Grobner Basis Reductions on Datapath Circuits Using the Unate Cube Set Algebra***”, International Workshop on Logic and Synthesis, 2017 (\* Best paper with student as first author award. \*) .

- Utkarsh Gupta, Priyank Kalla, **Vikas Rao**, “***Boolean Grobner Basis Reductions on Datapath Circuits Using the Unate Cube Set Algebra***”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018 (DOI 10.1109/TCAD.2018.2818726).

- Utkarsh Gupta, Irina Ilioaea, Priyank Kalla, Florian Enescu, **Vikas Rao**, Arpitha Srinath “***Craig Interpolants in Finite Fields using Algebraic Geometry: Theory and Application***” (In review).

- **Vikas Rao**, “***FPGA based Solutions for ASIC development***”, Intel India Innovation Day - 2012, poster presentation.

- **Vikas Rao**, Vijayakrishnan Rousseau, “***Scalable high-throughput FPGA Transactor***”, Intel DTTC conference – 2014, Author.

- Vijayakrishnan Rousseau, **Vikas Rao**, Sivakumar Seemakurti, “***Unified Validation Environment Across CLT Simulation & Emulation***”, Intel VPG Tech Summit - 2014, Co-presenter.

- Udaya K.S, Vijayakrishnan Rousseau, **Vikas Rao**, “***Software Framework for FPGA Based Validation of Gen Graphics***”, Intel DTTC conference, Oregon – 2013, co-author.

**Software Tools/Skills­­­:**

**Programming Languages:** Verilog, VHDL, Python, Ruby, C, C++, Perl, BASH.

**Hardware Verification:**  ABC, Minisat, Picosat, SIS.

**Hardware Design/Compilation:** Synopsys DC, VCS, Modelsim, ISE, VIVADO, Synplify Pro, Synplify premier, CoreGen.

**Other:**  Singular, LaTeX, Git, SVN, SPICE.

**Relevant Coursework:**

Testing & Verification of Digital Circuits Computer Architecture (spring 2018) Advanced Digital VLSI Design

Synthesis & Verification of Asynchronous VLSI Systems Advanced Algorithms