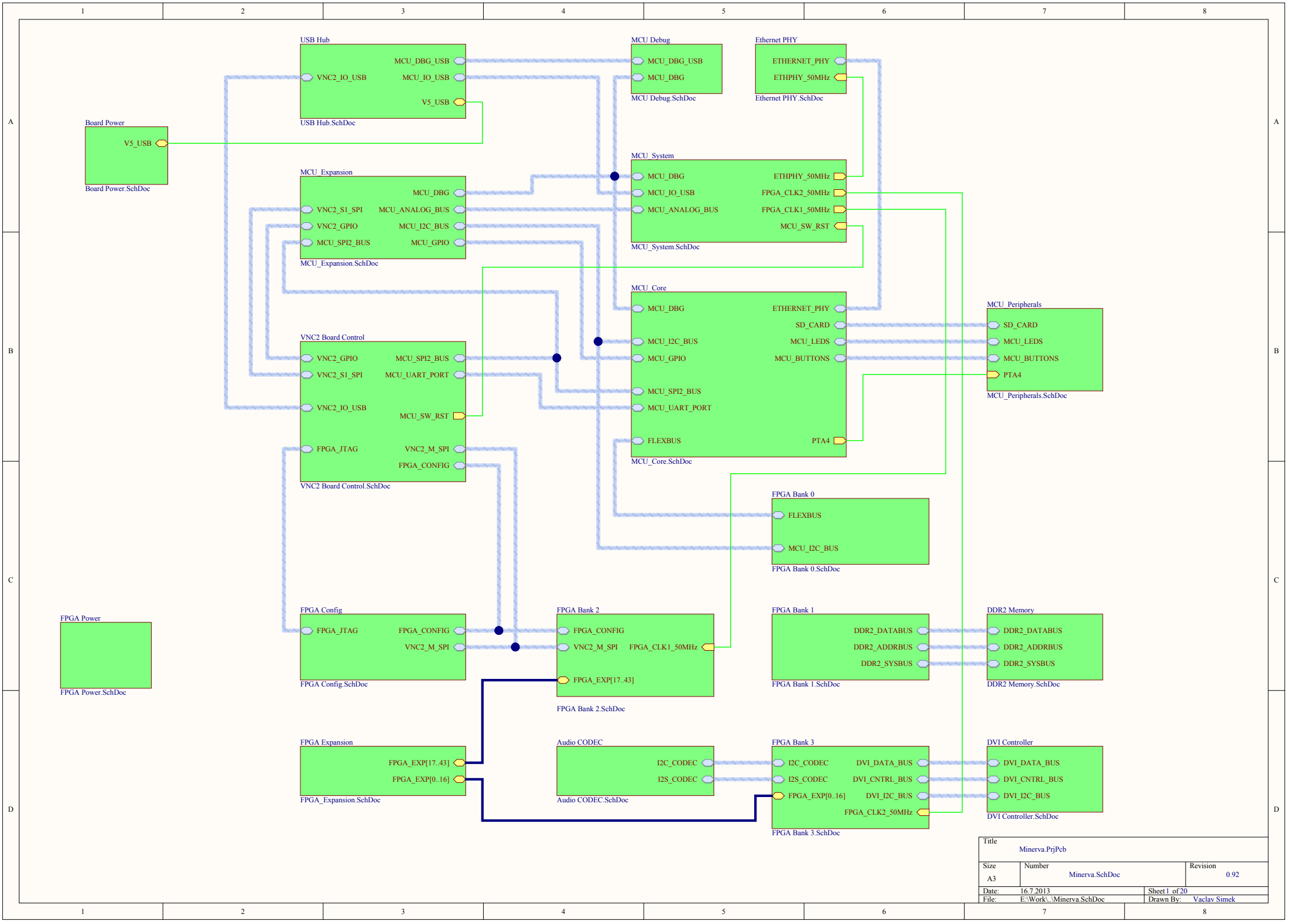
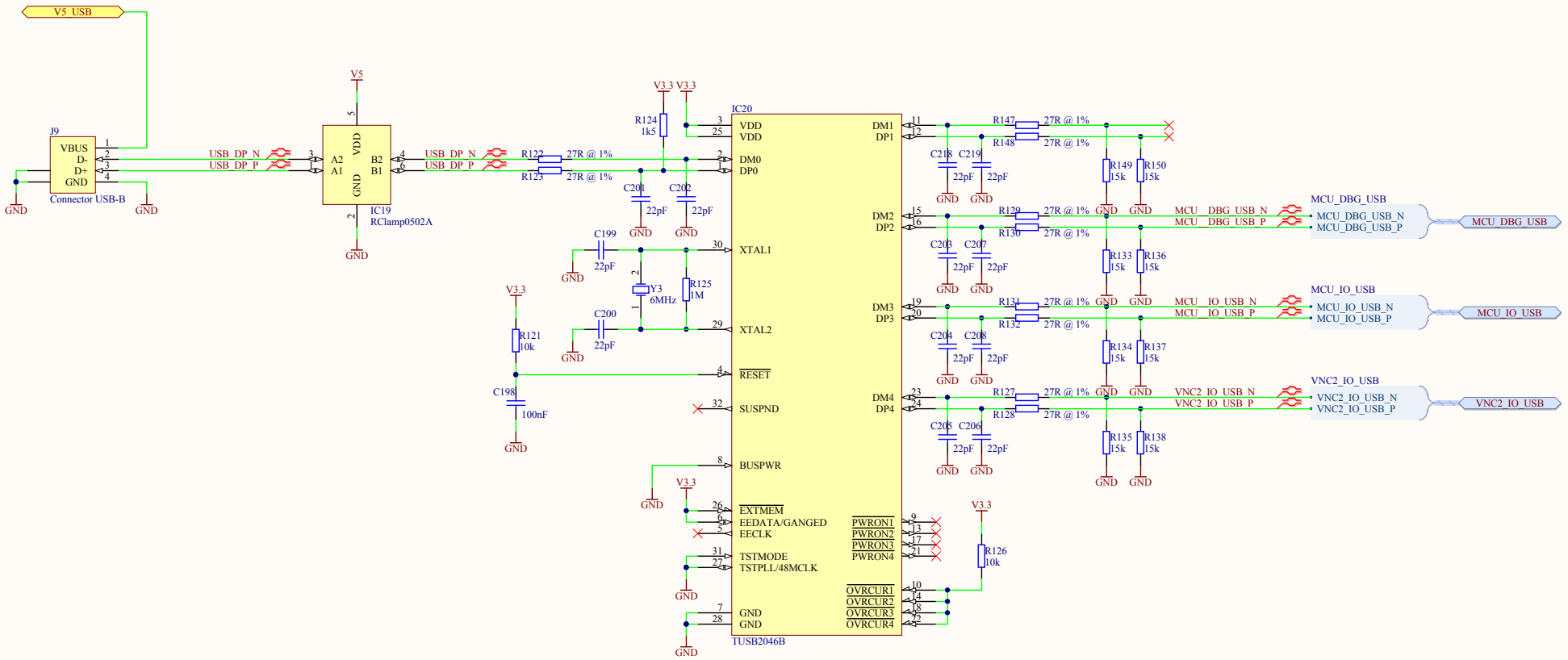

USB Hub
MCU_DBG_USB
VNC2_IO_USB
MCU_IO_USB
V5_USB
USB Hub.SchDoc
MCU Debug
MCU_DBG_USB
MCU_DBG
MCU Debug.SchDoc
Ethernet PHY
ETHERNET_PHY
ETHPHY_50MHz
Ethernet PHY.SchDoc
Board Power
V5_USB
Board Power.SchDoc
MCU_System
MCU_DBG
MCU_IO_USB
MCU_ANALOG_BUS
ETHPHY_50MHz
FPGA_CLK2_50MHz
FPGA_CLK1_50MHz
MCU_SW_RST
MCU_System.SchDoc
MCU_Expansion
MCU_DBG
VNC2_S1_SPI
MCU_ANALOG_BUS
VNC2_GPIO
MCU_I2C_BUS
MCU_SPI2_BUS
MCU_GPIO
MCU_Expansion.SchDoc
MCU_Core
MCU_DBG
ETHERNET_PHY
SD_CARD
MCU_I2C_BUS
MCU_LEDS
MCU_GPIO
MCU_BUTTONS
MCU_SPI2_BUS
MCU_UART_PORT
FLEXBUS
PTA4
MCU_Core.SchDoc
MCU_Peripherals
SD_CARD
MCU_LEDS
MCU_BUTTONS
PTA4
MCU_Peripherals.SchDoc
VNC2 Board Control
VNC2_GPIO
MCU_SPI2_BUS
VNC2_S1_SPI
MCU_UART_PORT
VNC2_IO_USB
MCU_SW_RST
FPGA_JTAG
VNC2_M_SPI
FPGA_CONFIG
VNC2 Board Control.SchDoc
FPGA Bank 0
FLEXBUS
MCU_I2C_BUS
FPGA Bank 0.SchDoc
FPGA Power
FPGA Power.SchDoc
FPGA Config
FPGA_JTAG
FPGA_CONFIG
VNC2_M_SPI
FPGA Config.SchDoc
FPGA Bank 2
FPGA_CONFIG
VNC2_M_SPI
FPGA_CLK1_50MHz
FPGA_EXP[17..43]
FPGA Bank 2.SchDoc
FPGA Bank 1
DDR2_DATABUS
DDR2_ADDRBUS
DDR2_SYSBUS
FPGA Bank 1.SchDoc
DDR2 Memory
DDR2_DATABUS
DDR2_ADDRBUS
DDR2_SYSBUS
DDR2 Memory.SchDoc
FPGA Expansion
FPGA_EXP[17..43]
FPGA_EXP[0..16]
FPGA_Expansion.SchDoc
Audio CODEC
I2C_CODEC
I2S_CODEC
Audio CODEC.SchDoc
FPGA Bank 3
I2C_CODEC
I2S_CODEC
FPGA_EXP[0..16]
DVI_DATA_BUS
DVI_CNTRL_BUS
DVI_I2C_BUS
FPGA_CLK2_50MHz
FPGA Bank 3.SchDoc
DVI Controller
DVI_DATA_BUS
DVI_CNTRL_BUS
DVI_I2C_BUS
DVI Controller.SchDoc
Title
Minerva.PrjPcb
Size
A3
Number
Minerva.SchDoc
Revision
0.92
Date:
16.7.2013
Sheet 1 of 20
File:
E:\Work\..\Minerva.SchDoc
Drawn By:
Vaclav Simek



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Size	Number		Revision
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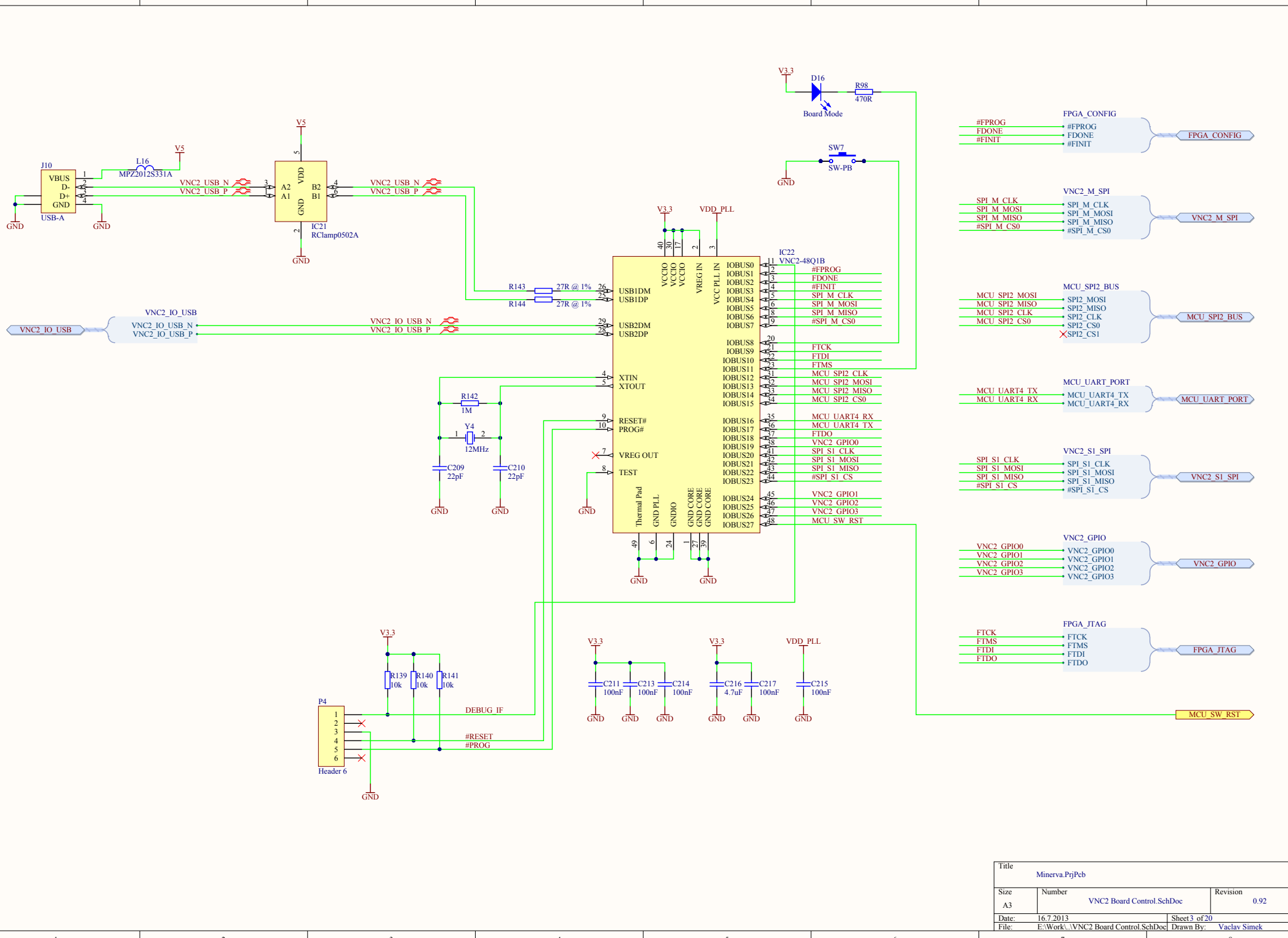
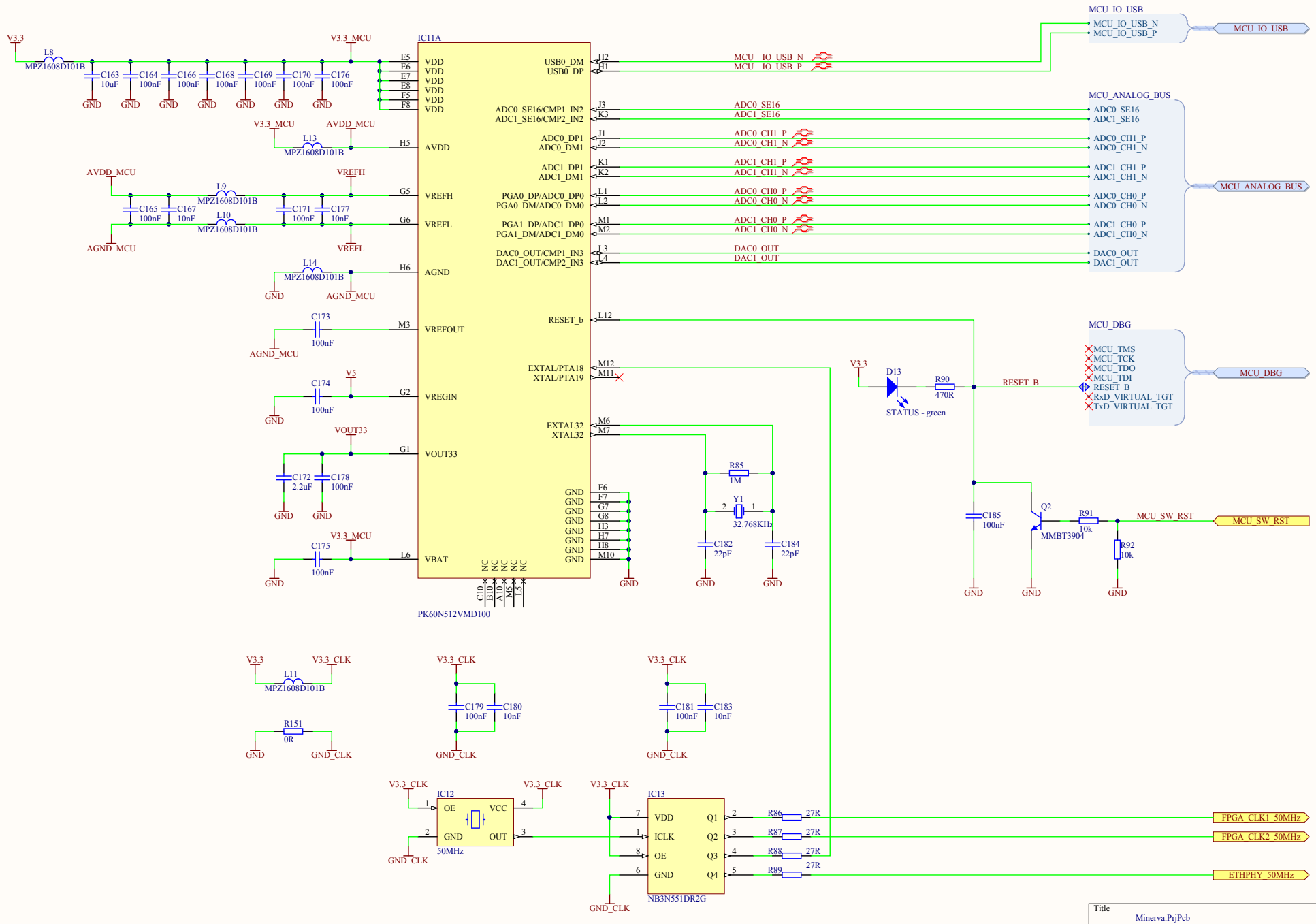
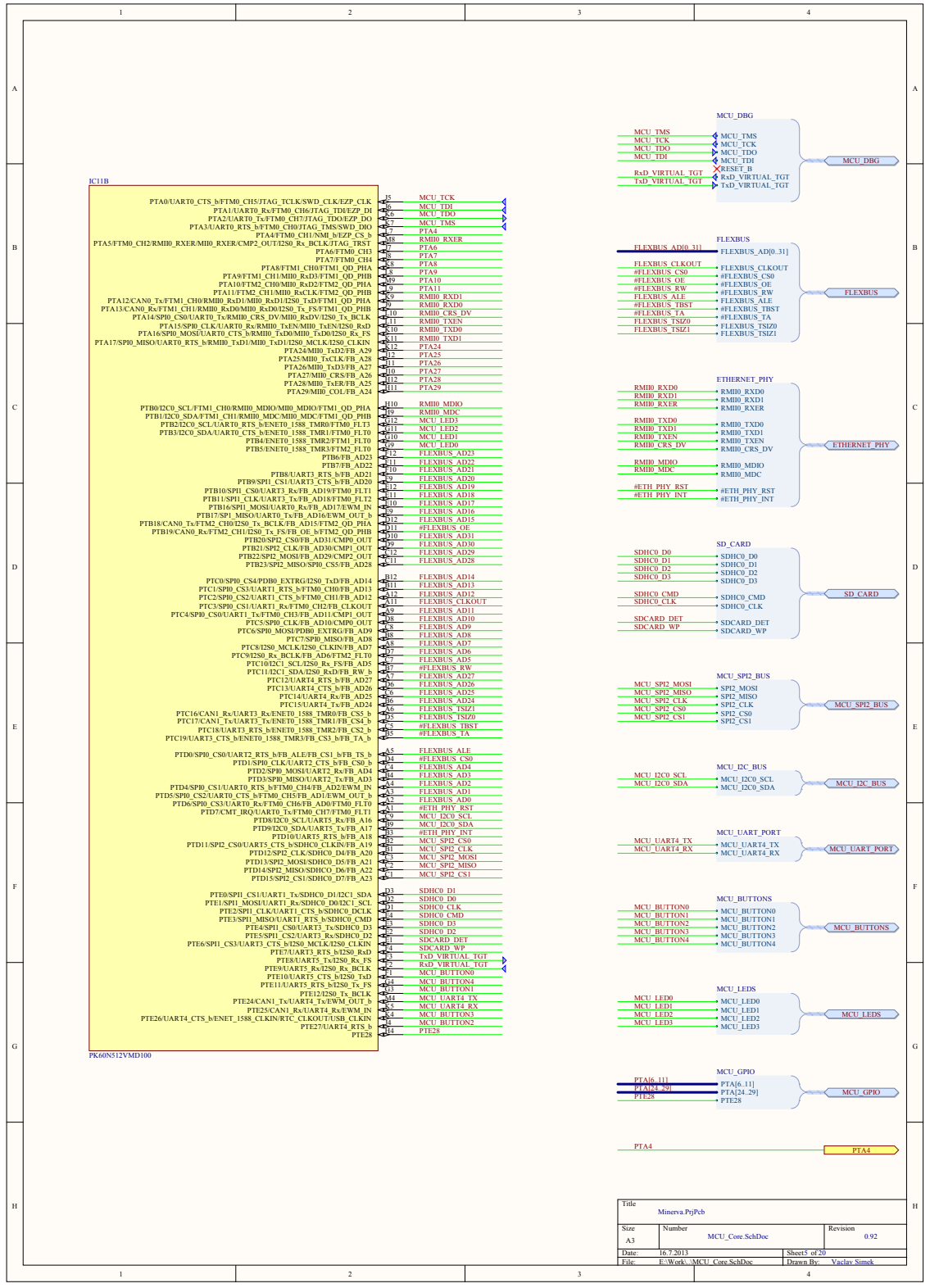
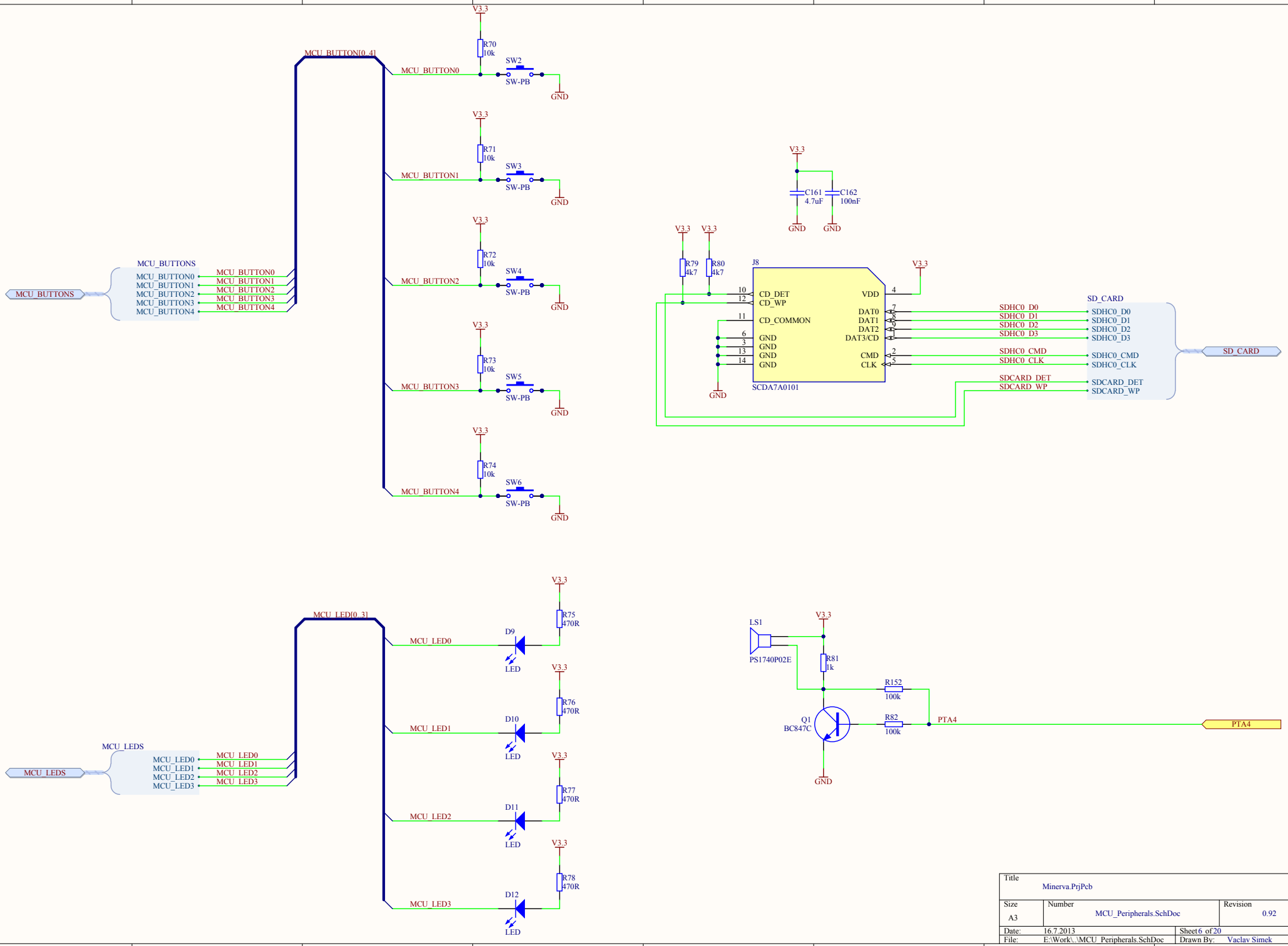
Date:	16.7.2013	Sheet of	2 20
File:	E:\Work\..\USB Hub.SchDoc	Drawn By:	Vaclav Simek


J10
VBUS
D-
D+
GND
USB-A
L16
MPZ2012S331A
V5
VNC2_USB_N
VNC2_USB_P
IC21
RClamp0502A
A2
A1
B2
B1
VDD
GND
D16
Board Mode
R98
470R
SW7
SW-PB
V3.3
VDD_PLL
IC22
VNC2-48Q1B
VCCIO
VREG IN
VCC PLL IN
IOBUS0
IOBUS1
IOBUS2
IOBUS3
IOBUS4
IOBUS5
IOBUS6
IOBUS7
IOBUS8
IOBUS9
IOBUS10
IOBUS11
IOBUS12
IOBUS13
IOBUS14
IOBUS15
IOBUS16
IOBUS17
IOBUS18
IOBUS19
IOBUS20
IOBUS21
IOBUS22
IOBUS23
IOBUS24
IOBUS25
IOBUS26
IOBUS27
#FPROG
FDONE
#FINIT
SPI_M_CLK
SPI_M_MOSI
SPI_M_MISO
#SPI_M_CS0
FTCK
FTDI
FTMS
MCU_SPI2_CLK
MCU_SPI2_MOSI
MCU_SPI2_MISO
MCU_SPI2_CS0
MCU_UART4_RX
MCU_UART4_TX
FTDO
VNC2_GPIO0
SPI_S1_CLK
SPI_S1_MOSI
SPI_S1_MISO
#SPI_S1_CS
VNC2_GPIO1
VNC2_GPIO2
VNC2_GPIO3
MCU_SW_RST
R143
R144
27R @ 1%
USB1DM
USB1DP
USB2DM
USB2DP
VNC2_IO_USB
VNC2_IO_USB_N
VNC2_IO_USB_P
XTIN
XTOUT
R142
1M
Y4
12MHz
C209
22pF
C210
22pF
RESET#
PROG#
VREG OUT
TEST
Thermal Pad
GND PLL
GNDIO
GND CORE
P4
Header 6
R139
10k
R140
10k
R141
10k
DEBUG_IF
#RESET
#PROG
C211
100nF
C213
100nF
C214
100nF
C216
4.7uF
C217
100nF
C215
100nF
FPGA_CONFIG
VNC2_M_SPI
MCU_SPI2_BUS
MCU_UART_PORT
VNC2_S1_SPI
VNC2_GPIO
FPGA_JTAG
Title
Minerva.PrjPcb
Size
A3
Number
VNC2 Board Control.SchDoc
Revision
0.92
Date:
16.7.2013
Sheet3 of20
File:
E:\Work\..\VNC2 Board Control.SchDoc
Drawn By:
Vaclav Simek


IC11A
PK60N512VMD100
MCU_IO_USB
MCU_IO_USB_N
MCU_IO_USB_P
MCU_ANALOG_BUS
MCU_DBG
MCU_TMS
MCU_TCK
MCU_TDO
MCU_TDI
RESET_B
RxD_VIRTUAL_TGT
TxD_VIRTUAL_TGT
MCU_SW_RST
STATUS - green
MMBT3904
IC12
50MHz
IC13
NB3N551DR2G
FPGA_CLK1_50MHz
FPGA_CLK2_50MHz
ETHPHY_50MHz
Minerva.PrjPcb
MCU_System.SchDoc
0.92
16.7.2013
Sheet4 of 20
E:\Work\..\MCU_System.SchDoc
Vaclav Simek


IC11B
PTA0/UART0_CTS_b/FTM0_CH5/JTAG_TCLK/SWD_CLK/EZP_CLK
PTA1/UART0_Rx/FTM0_CH6/JTAG_TDI/EZP_DI
PTA2/UART0_Tx/FTM0_CH7/JTAG_TDO/EZP_DO
PTA3/UART0_RTS_b/FTM0_CH0/JTAG_TMS/SWD_DIO
PTA4/FTM0_CH1/NMI_b/EZP_CS_b
PTA5/FTM0_CH2/RMII0_RXER/MII0_RXER/CMP2_OUT/I2S0_Rx_BCLK/JTAG_TRST
PTA6/FTM0_CH3
PTA7/FTM0_CH4
PTA8/FTM1_CH0/FTM1_QD_PHA
PTA9/FTM1_CH1/MII0_RxD3/FTM1_QD_PHB
PTA10/FTM2_CH0/MII0_RxD2/FTM2_QD_PHA
PTA11/FTM2_CH1/MII0_RxCLK/FTM2_QD_PHB
PTA12/CAN0_Tx/FTM1_CH0/RMII0_RxD1/MII0_RxD1/I2S0_TxD/FTM1_QD_PHA
PTA13/CAN0_Rx/FTM1_CH1/RMII0_RxD0/MII0_RxD0/I2S0_Tx_FS/FTM1_QD_PHB
PTA14/SPI0_CS0/UART0_Tx/RMII0_CRS_DV/MII0_RxDV/I2S0_Tx_BCLK
PTA15/SPI0_CLK/UART0_Rx/RMII0_TxEN/MII0_TxEN/I2S0_RxD
PTA16/SPI0_MOSI/UART0_CTS_b/RMII0_TxD0/MII0_TxD0/I2S0_Rx_FS
PTA17/SPI0_MISO/UART0_RTS_b/RMII0_TxD1/MII0_TxD1/I2S0_MCLK/I2S0_CLKIN
PTA24/MII0_TxD2/FB_A29
PTA25/MII0_TxCLK/FB_A28
PTA26/MII0_TxD3/FB_A27
PTA27/MII0_CRS/FB_A26
PTA28/MII0_TxER/FB_A25
PTA29/MII0_COL/FB_A24
PTB0/I2C0_SCL/FTM1_CH0/RMII0_MDIO/MII0_MDIO/FTM1_QD_PHA
PTB1/I2C0_SDA/FTM1_CH1/RMII0_MDC/MII0_MDC/FTM1_QD_PHB
PTB2/I2C0_SCL/UART0_RTS_b/ENET0_1588_TMR0/FTM0_FLT3
PTB3/I2C0_SDA/UART0_CTS_b/ENET0_1588_TMR1/FTM0_FLT0
PTB4/ENET0_1588_TMR2/FTM1_FLT0
PTB5/ENET0_1588_TMR3/FTM2_FLT0
PTB6/FB_AD23
PTB7/FB_AD22
PTB8/UART3_RTS_b/FB_AD21
PTB9/SPI1_CS1/UART3_CTS_b/FB_AD20
PTB10/SPI1_CS0/UART3_Rx/FB_AD19/FTM0_FLT1
PTB11/SPI1_CLK/UART3_Tx/FB_AD18/FTM0_FLT2
PTB16/SPI1_MOSI/UART0_Rx/FB_AD17/EWM_IN
PTB17/SPI1_MISO/UART0_Tx/FB_AD16/EWM_OUT_b
PTB18/CAN0_Tx/FTM2_CH0/I2S0_Tx_BCLK/FB_AD15/FTM2_QD_PHA
PTB19/CAN0_Rx/FTM2_CH1/I2S0_Tx_FS/FB_OE_b/FTM2_QD_PHB
PTB20/SPI2_CS0/FB_AD31/CMP0_OUT
PTB21/SPI2_CLK/FB_AD30/CMP1_OUT
PTB22/SPI2_MOSI/FB_AD29/CMP2_OUT
PTB23/SPI2_MISO/SPI0_CS5/FB_AD28
PTC0/SPI0_CS4/PDB0_EXTRG/I2S0_TxD/FB_AD14
PTC1/SPI0_CS3/UART1_RTS_b/FTM0_CH0/FB_AD13
PTC2/SPI0_CS2/UART1_CTS_b/FTM0_CH1/FB_AD12
PTC3/SPI0_CS1/UART1_Rx/FTM0_CH2/FB_CLKOUT
PTC4/SPI0_CS0/UART1_Tx/FTM0_CH3/FB_AD11/CMP1_OUT
PTC5/SPI0_CLK/FB_AD10/CMP0_OUT
PTC6/SPI0_MOSI/PDB0_EXTRG/FB_AD9
PTC7/SPI0_MISO/FB_AD8
PTC8/I2S0_MCLK/I2S0_CLKIN/FB_AD7
PTC9/I2S0_Rx_BCLK/FB_AD6/FTM2_FLT0
PTC10/I2C1_SCL/I2S0_Rx_FS/FB_AD5
PTC11/I2C1_SDA/I2S0_RxD/FB_RW_b
PTC12/UART4_RTS_b/FB_AD27
PTC13/UART4_CTS_b/FB_AD26
PTC14/UART4_Rx/FB_AD25
PTC15/UART4_Tx/FB_AD24
PTC16/CAN1_Rx/UART3_Rx/ENET0_1588_TMR0/FB_CS5_b
PTC17/CAN1_Tx/UART3_Tx/ENET0_1588_TMR1/FB_CS4_b
PTC18/UART3_RTS_b/ENET0_1588_TMR2/FB_CS2_b
PTC19/UART3_CTS_b/ENET0_1588_TMR3/FB_CS3_b/FB_TA_b
PTD0/SPI0_CS0/UART2_RTS_b/FB_ALE/FB_CS1_b/FB_TS_b
PTD1/SPI0_CLK/UART2_CTS_b/FB_CS0_b
PTD2/SPI0_MOSI/UART2_Rx/FB_AD4
PTD3/SPI0_MISO/UART2_Tx/FB_AD3
PTD4/SPI0_CS1/UART0_RTS_b/FTM0_CH4/FB_AD2/EWM_IN
PTD5/SPI0_CS2/UART0_CTS_b/FTM0_CH5/FB_AD1/EWM_OUT_b
PTD6/SPI0_CS3/UART0_Rx/FTM0_CH6/FB_AD0/FTM0_FLT0
PTD7/CMT_IRQ/UART0_Tx/FTM0_CH7/FTM0_FLT1
PTD8/I2C0_SCL/UART5_Rx/FB_A16
PTD9/I2C0_SDA/UART5_Tx/FB_A17
PTD10/UART5_RTS_b/FB_A18
PTD11/SPI2_CS0/UART5_CTS_b/SDHC0_CLKIN/FB_A19
PTD12/SPI2_CLK/SDHC0_D4/FB_A20
PTD13/SPI2_MOSI/SDHC0_D5/FB_A21
PTD14/SPI2_MISO/SDHCO_D6/FB_A22
PTD15/SPI2_CS1/SDHC0_D7/FB_A23
PTE0/SPI1_CS1/UART1_Tx/SDHC0_D1/I2C1_SDA
PTE1/SPI1_MOSI/UART1_Rx/SDHC0_D0/I2C1_SCL
PTE2/SPI1_CLK/UART1_CTS_b/SDHC0_DCLK
PTE3/SPI1_MISO/UART1_RTS_b/SDHC0_CMD
PTE4/SPI1_CS0/UART3_Tx/SDHC0_D3
PTE5/SPI1_CS2/UART3_Rx/SDHC0_D2
PTE6/SPI1_CS3/UART3_CTS_b/I2S0_MCLK/I2S0_CLKIN
PTE7/UART3_RTS_b/I2S0_RxD
PTE8/UART5_Tx/I2S0_Rx_FS
PTE9/UART5_Rx/I2S0_Rx_BCLK
PTE10/UART5_CTS_b/I2S0_TxD
PTE11/UART5_RTS_b/I2S0_Tx_FS
PTE12/I2S0_Tx_BCLK
PTE24/CAN1_Tx/UART4_Tx/EWM_OUT_b
PTE25/CAN1_Rx/UART4_Rx/EWM_IN
PTE26/UART4_CTS_b/ENET_1588_CLKIN/RTC_CLKOUT/USB_CLKIN
PTE27/UART4_RTS_b
PTE28
J5 MCU_TCK
J6 MCU_TDI
K6 MCU_TDO
J7 MCU_TMS
L7 PTA4
M8 RMII0_RXER
L7 PTA6
J8 PTA7
K8 PTA8
L8 PTA9
M9 PTA10
K9 PTA11
L9 RMII0_RXD1
M9 RMII0_RXD0
L10 RMII0_CRS_DV
L11 RMII0_TXEN
K10 RMII0_TXD0
K11 RMII0_TXD1
K12 PTA24
L12 PTA25
L11 PTA26
J10 PTA27
H12 PTA28
H11 PTA29
H10 RMII0_MDIO
J9 RMII0_MDC
G12 MCU_LED3
G11 MCU_LED2
G10 MCU_LED1
G9 MCU_LED0
F12 FLEXBUS_AD23
F11 FLEXBUS_AD22
F10 FLEXBUS_AD21
E9 FLEXBUS_AD20
E12 FLEXBUS_AD19
E11 FLEXBUS_AD18
E10 FLEXBUS_AD17
D9 FLEXBUS_AD16
D12 FLEXBUS_AD15
D11 #FLEXBUS_OE
D10 FLEXBUS_AD31
C9 FLEXBUS_AD30
C12 FLEXBUS_AD29
C11 FLEXBUS_AD28
B12 FLEXBUS_AD14
B11 FLEXBUS_AD13
A12 FLEXBUS_AD12
A11 FLEXBUS_CLKOUT
A10 FLEXBUS_AD11
D8 FLEXBUS_AD10
C8 FLEXBUS_AD9
B8 FLEXBUS_AD8
A8 FLEXBUS_AD7
D7 FLEXBUS_AD6
C7 FLEXBUS_AD5
B7 #FLEXBUS_RW
A7 FLEXBUS_AD27
J6 FLEXBUS_AD26
C6 FLEXBUS_AD25
B6 FLEXBUS_AD24
A6 FLEXBUS_TSIZ1
D5 FLEXBUS_TSIZ0
C5 #FLEXBUS_TBST
B5 #FLEXBUS_TA
A5 FLEXBUS_ALE
D4 #FLEXBUS_CS0
C4 FLEXBUS_AD4
B4 FLEXBUS_AD3
A4 FLEXBUS_AD2
A3 FLEXBUS_AD1
A2 FLEXBUS_AD0
A1 #ETH_PHY_RST
C9 MCU_I2C0_SCL
B9 MCU_I2C0_SDA
B3 #ETH_PHY_INT
B2 MCU_SPI2_CS0
B1 MCU_SPI2_CLK
C3 MCU_SPI2_MOSI
C2 MCU_SPI2_MISO
C1 MCU_SPI2_CS1
D3 SDHC0_D1
D2 SDHC0_D0
D1 SDHC0_CLK
E4 SDHC0_CMD
E3 SDHC0_D3
E2 SDHC0_D2
E1 SDCARD_DET
F4 SDCARD_WP
F3 TxD_VIRTUAL_TGT
F2 RxD_VIRTUAL_TGT
F1 MCU_BUTTON0
G4 MCU_BUTTON4
G3 MCU_BUTTON1
M4 MCU_UART4_TX
K5 MCU_UART4_RX
K4 MCU_BUTTON3
J4 MCU_BUTTON2
H4 PTE28
PK60N512VMD100
MCU_DBG
MCU_TMS
MCU_TCK
MCU_TDO
MCU_TDI
RxD_VIRTUAL_TGT
TxD_VIRTUAL_TGT
MCU_TMS
MCU_TCK
MCU_TDO
MCU_TDI
RESET_B
RxD_VIRTUAL_TGT
TxD_VIRTUAL_TGT
MCU_DBG
FLEXBUS
FLEXBUS_AD[0..31]
FLEXBUS_CLKOUT
#FLEXBUS_CS0
#FLEXBUS_OE
#FLEXBUS_RW
FLEXBUS_ALE
#FLEXBUS_TBST
#FLEXBUS_TA
FLEXBUS_TSIZ0
FLEXBUS_TSIZ1
FLEXBUS_AD[0..31]
FLEXBUS_CLKOUT
#FLEXBUS_CS0
#FLEXBUS_OE
#FLEXBUS_RW
FLEXBUS_ALE
#FLEXBUS_TBST
#FLEXBUS_TA
FLEXBUS_TSIZ0
FLEXBUS_TSIZ1
FLEXBUS
ETHERNET_PHY
RMII0_RXD0
RMII0_RXD1
RMII0_RXER
RMII0_TXD0
RMII0_TXD1
RMII0_TXEN
RMII0_CRS_DV
RMII0_MDIO
RMII0_MDC
#ETH_PHY_RST
#ETH_PHY_INT
RMII0_RXD0
RMII0_RXD1
RMII0_RXER
RMII0_TXD0
RMII0_TXD1
RMII0_TXEN
RMII0_CRS_DV
RMII0_MDIO
RMII0_MDC
#ETH_PHY_RST
#ETH_PHY_INT
ETHERNET_PHY
SD_CARD
SDHC0_D0
SDHC0_D1
SDHC0_D2
SDHC0_D3
SDHC0_CMD
SDHC0_CLK
SDCARD_DET
SDCARD_WP
SDHC0_D0
SDHC0_D1
SDHC0_D2
SDHC0_D3
SDHC0_CMD
SDHC0_CLK
SDCARD_DET
SDCARD_WP
SD_CARD
MCU_SPI2_BUS
MCU_SPI2_MOSI
MCU_SPI2_MISO
MCU_SPI2_CLK
MCU_SPI2_CS0
MCU_SPI2_CS1
SPI2_MOSI
SPI2_MISO
SPI2_CLK
SPI2_CS0
SPI2_CS1
MCU_SPI2_BUS
MCU_I2C_BUS
MCU_I2C0_SCL
MCU_I2C0_SDA
MCU_I2C0_SCL
MCU_I2C0_SDA
MCU_I2C_BUS
MCU_UART_PORT
MCU_UART4_TX
MCU_UART4_RX
MCU_UART4_TX
MCU_UART4_RX
MCU_UART_PORT
MCU_BUTTONS
MCU_BUTTON0
MCU_BUTTON1
MCU_BUTTON2
MCU_BUTTON3
MCU_BUTTON4
MCU_BUTTON0
MCU_BUTTON1
MCU_BUTTON2
MCU_BUTTON3
MCU_BUTTON4
MCU_BUTTONS
MCU_LEDS
MCU_LED0
MCU_LED1
MCU_LED2
MCU_LED3
MCU_LED0
MCU_LED1
MCU_LED2
MCU_LED3
MCU_LEDS
MCU_GPIO
PTA[6..11]
PTA[24..29]
PTE28
PTA[6..11]
PTA[24..29]
PTE28
MCU_GPIO
PTA4
PTA4
Title
Minerva.PrjPcb
Size
A3
Number
MCU_Core.SchDoc
Revision
0.92
Date:
16.7.2013
Sheet5 of 20
File:
E:\Work\...\MCU_Core.SchDoc
Drawn By:
Vaclav Simek



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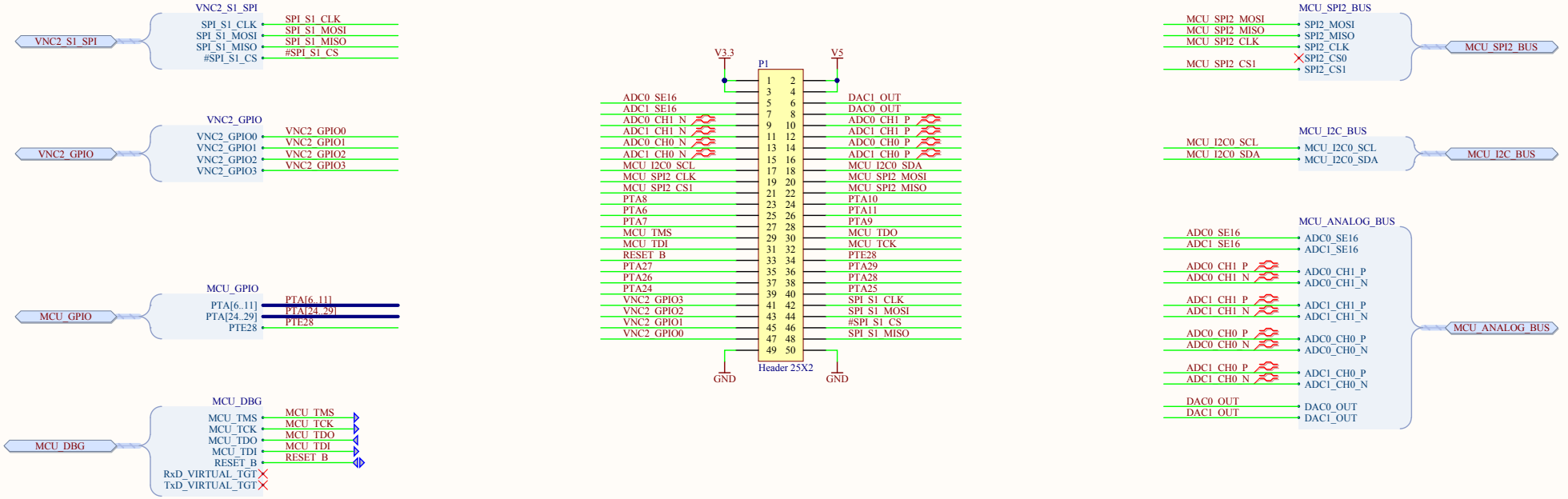
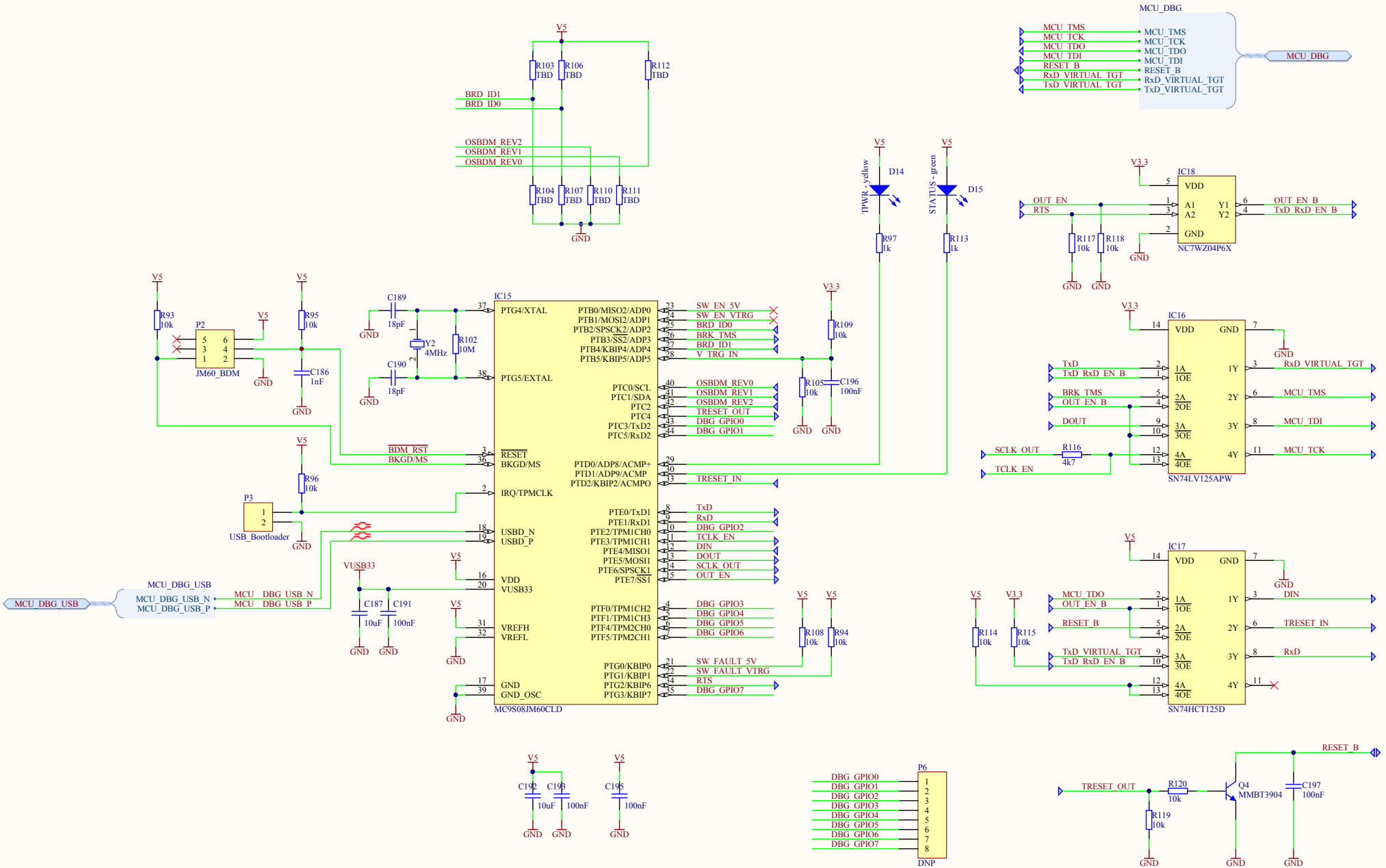
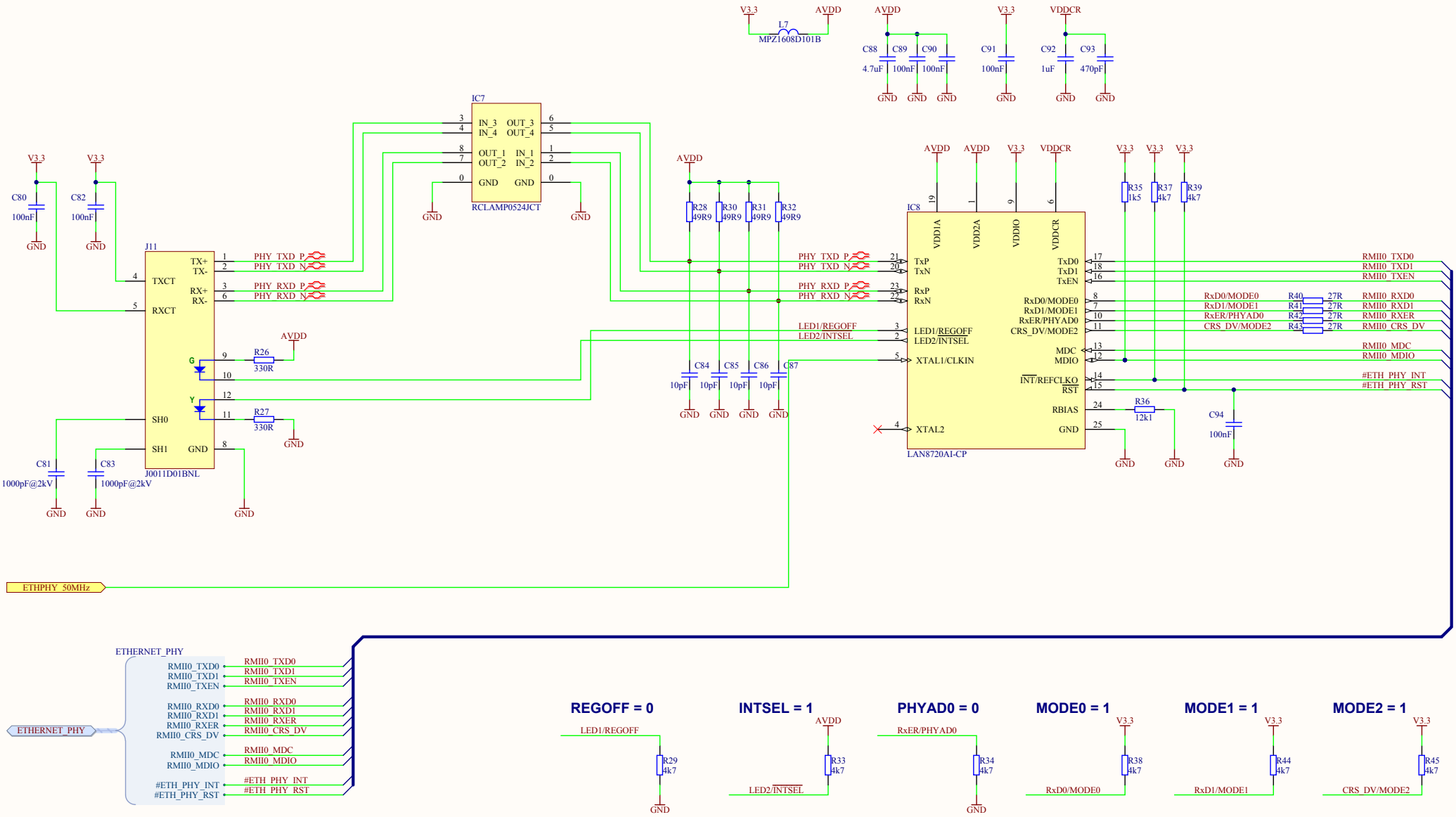
Date: 16.7.2013		Sheet 6 of 20
File: E:\Work\..\MCU_Peripherals.SchDoc		Drawn By: Vaclav Simek

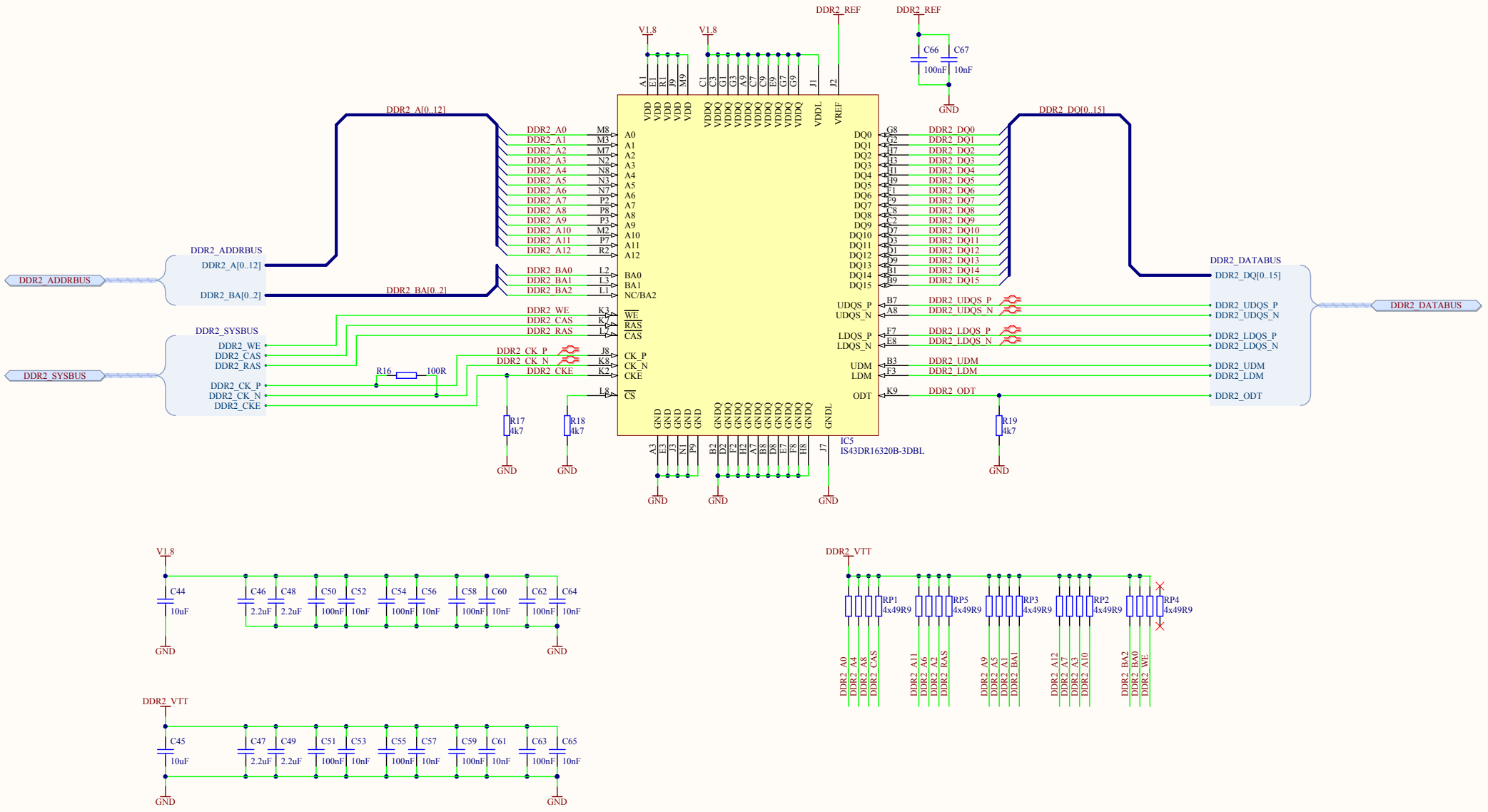


Title	Minerva.PrjPcb	
Size: A3	Number: MCU_Expansion.SchDoc	Revision: 0.92
Date: 16.7.2013	Sheet 7 of 20	
File: E:\Work\..\MCU_Expansion.SchDoc	Drawn By: Vaclav Simek	

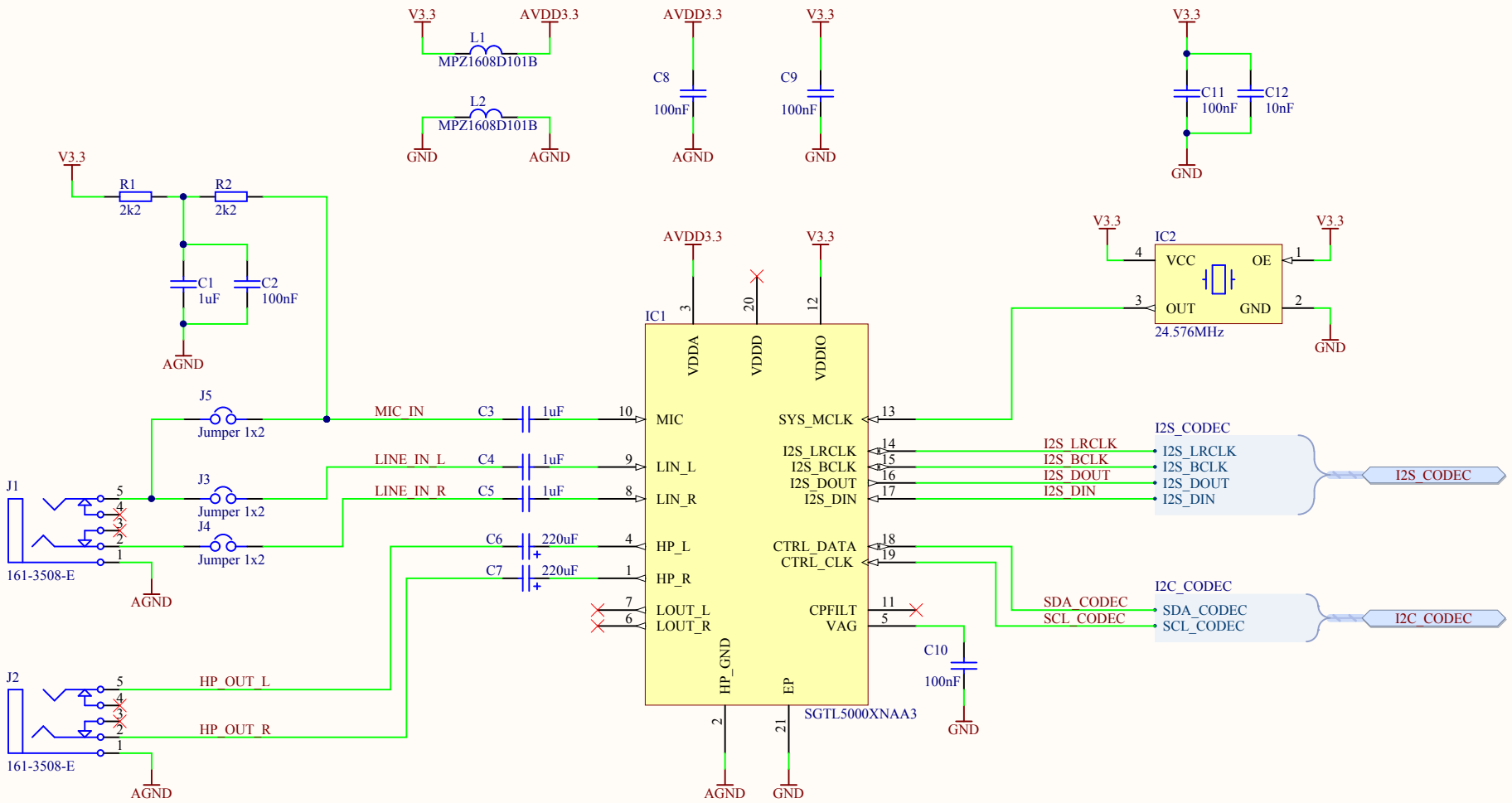

MCU_DBG
MCU_TMS
MCU_TCK
MCU_TDO
MCU_TDI
RESET_B
RxD_VIRTUAL_TGT
TxD_VIRTUAL_TGT
V5
R103 TBD
R106 TBD
R112 TBD
R104 TBD
R107 TBD
R110 TBD
R111 TBD
BRD_ID1
BRD_ID0
OSBDM_REV2
OSBDM_REV1
OSBDM_REV0
GND
D14
TPWR - yellow
D15
STATUS - green
R97 1k
R113 1k
V3.3
IC18
NC7WZ04P6X
OUT_EN
RTS
OUT_EN_B
TxD_RxD_EN_B
R117 10k
R118 10k
IC16
SN74LV125APW
TxD
TxD_RxD_EN_B
BRK_TMS
OUT_EN_B
DOUT
SCLK_OUT
TCLK_EN
R116 4k7
RxD_VIRTUAL_TGT
MCU_TMS
MCU_TDI
MCU_TCK
IC17
SN74HCT125D
MCU_TDO
RESET_B
TxD_VIRTUAL_TGT
DIN
TRESET_IN
RxD
R114 10k
R115 10k
IC15
MC9S08JM60CLD
PTG4/XTAL
PTG5/EXTAL
RESET
BKGD/MS
IRQ/TPMCLK
USBD_N
USBD_P
VDD
VUSB33
VREFH
VREFL
GND
GND_OSC
PTB0/MISO2/ADP0
PTB1/MOSI2/ADP1
PTB2/SPSCK2/ADP2
PTB3/SS2/ADP3
PTB4/KBIP4/ADP4
PTB5/KBIP5/ADP5
PTC0/SCL
PTC1/SDA
PTC2
PTC4
PTC3/TxD2
PTC5/RxD2
PTD0/ADP8/ACMP+
PTD1/ADP9/ACMP
PTD2/KBIP2/ACMPO
PTE0/TxD1
PTE1/RxD1
PTE2/TPM1CH0
PTE3/TPM1CH1
PTE4/MISO1
PTE5/MOSI1
PTE6/SPSCK1
PTE7/SS1
PTF0/TPM1CH2
PTF1/TPM1CH3
PTF4/TPM2CH0
PTF5/TPM2CH1
PTG0/KBIP0
PTG1/KBIP1
PTG2/KBIP6
PTG3/KBIP7
SW_EN_5V
SW_EN_VTRG
BRD_ID0
BRK_TMS
BRD_ID1
V_TRG_IN
OSBDM_REV0
OSBDM_REV1
OSBDM_REV2
TRESET_OUT
DBG_GPIO0
DBG_GPIO1
TRESET_IN
TxD
RxD
DBG_GPIO2
TCLK_EN
DIN
DOUT
SCLK_OUT
OUT_EN
DBG_GPIO3
DBG_GPIO4
DBG_GPIO5
DBG_GPIO6
SW_FAULT_5V
SW_FAULT_VTRG
RTS
DBG_GPIO7
C189 18pF
C190 18pF
Y2 4MHz
R102 10M
C186 1nF
C187 10uF
C191 100nF
C192 10uF
C193 100nF
C195 100nF
C196 100nF
R109 10k
R105 10k
R108 10k
R94 10k
R93 10k
R95 10k
R96 10k
P2
JM60_BDM
P3
USB_Bootloader
BDM_RST
BKGD/MS
MCU_DBG_USB
MCU_DBG_USB_N
MCU_DBG_USB_P
P6
DNP
R120 10k
R119 10k
Q4
MMBT3904
C197 100nF
Title
Minerva.PrjPcb
Size
A3
Number
MCU Debug.SchDoc
Revision
0.92
Date:
16.7.2013
Sheet 8 of 20
File:
E:\Work\..\MCU Debug.SchDoc
Drawn By:
Vaclav Simek



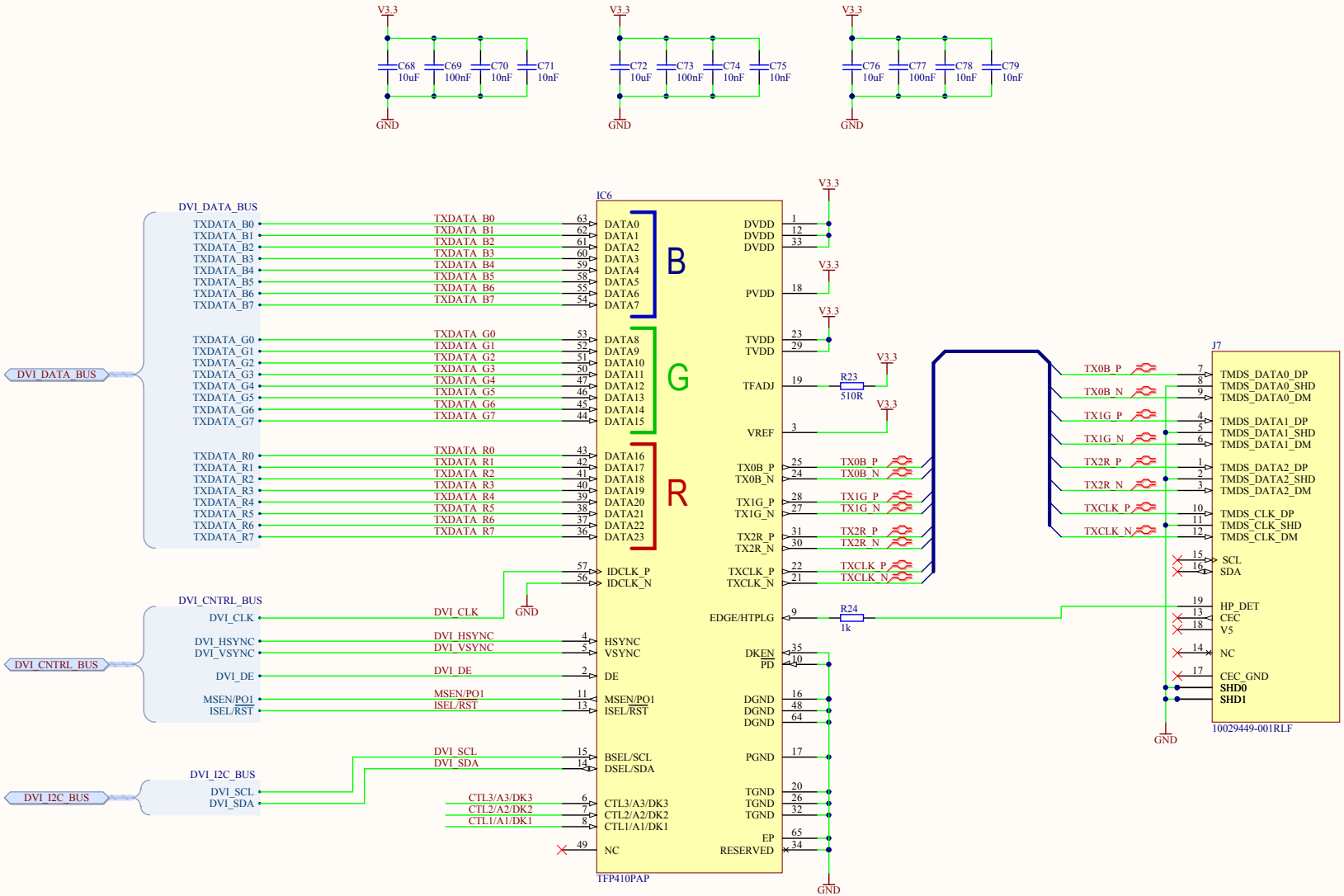
Title	Minerva.PrjPcb	
Size: A3	Number: Ethernet PHY.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet 9 of 20
File: E:\Work\..\Ethernet PHY.SchDoc		Drawn By: Vaclav Simek



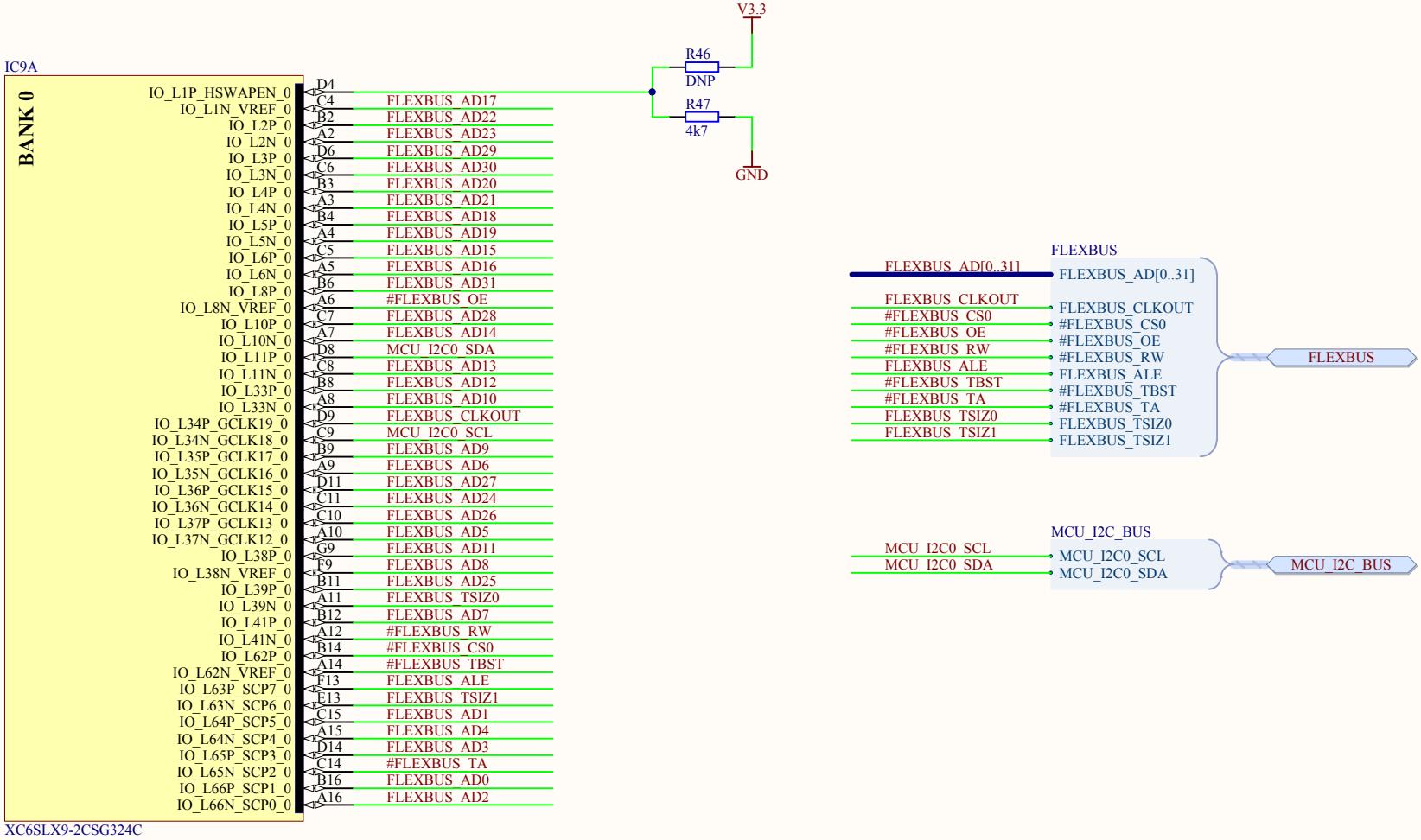
Title	Minerva.PrjPcb	
Size: A3	Number: DDR2 Memory.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet10of20
File: E:\Work\..\DDR2 Memory.SchDoc		Drawn By: Vaclav Simek



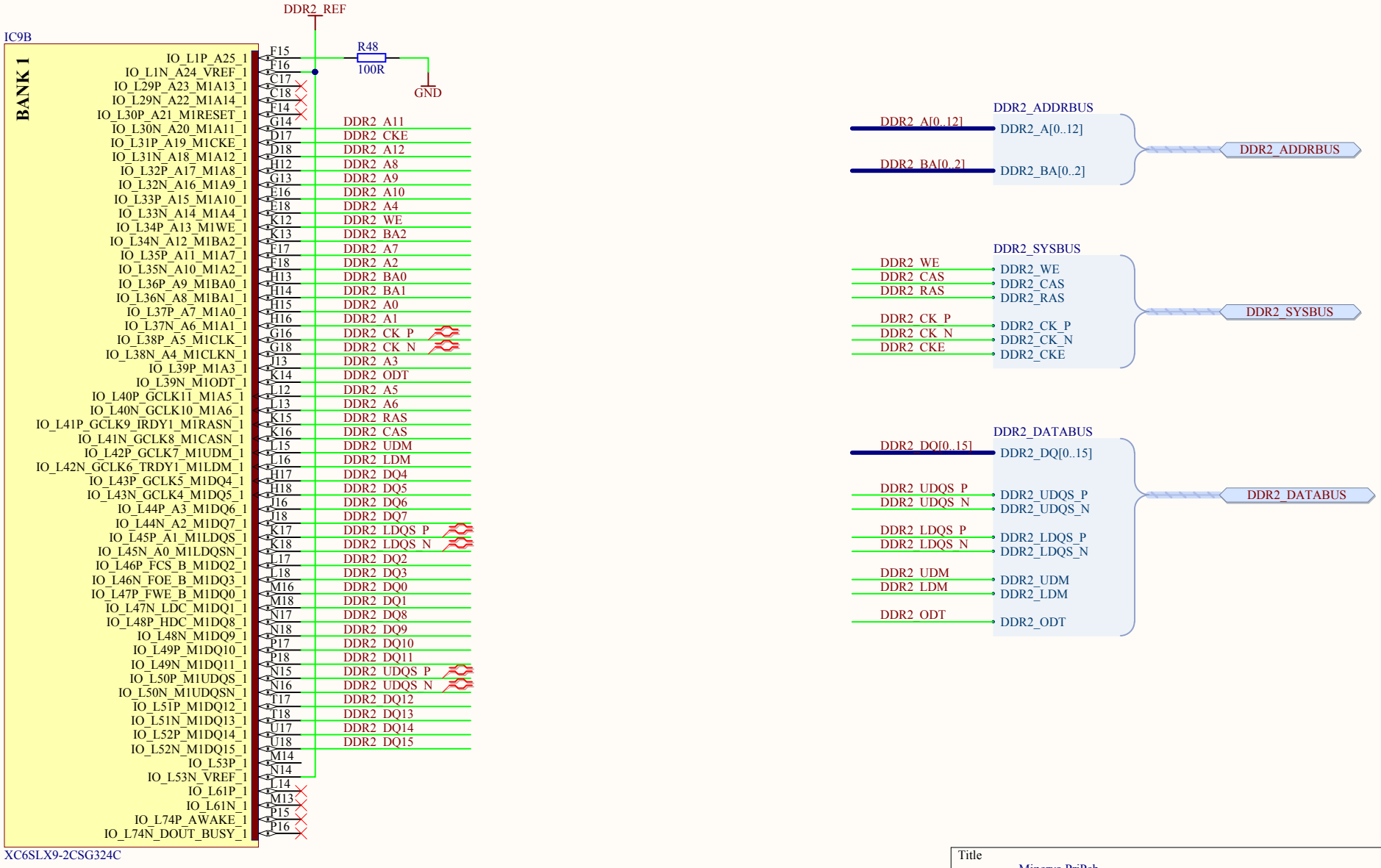
Title	Minerva.PrjPcb	
Size: A4	Number: Audio CODEC.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet11of20
File: E:\Work\..\Audio CODEC.SchDoc		Drawn By: Vaclav Simek



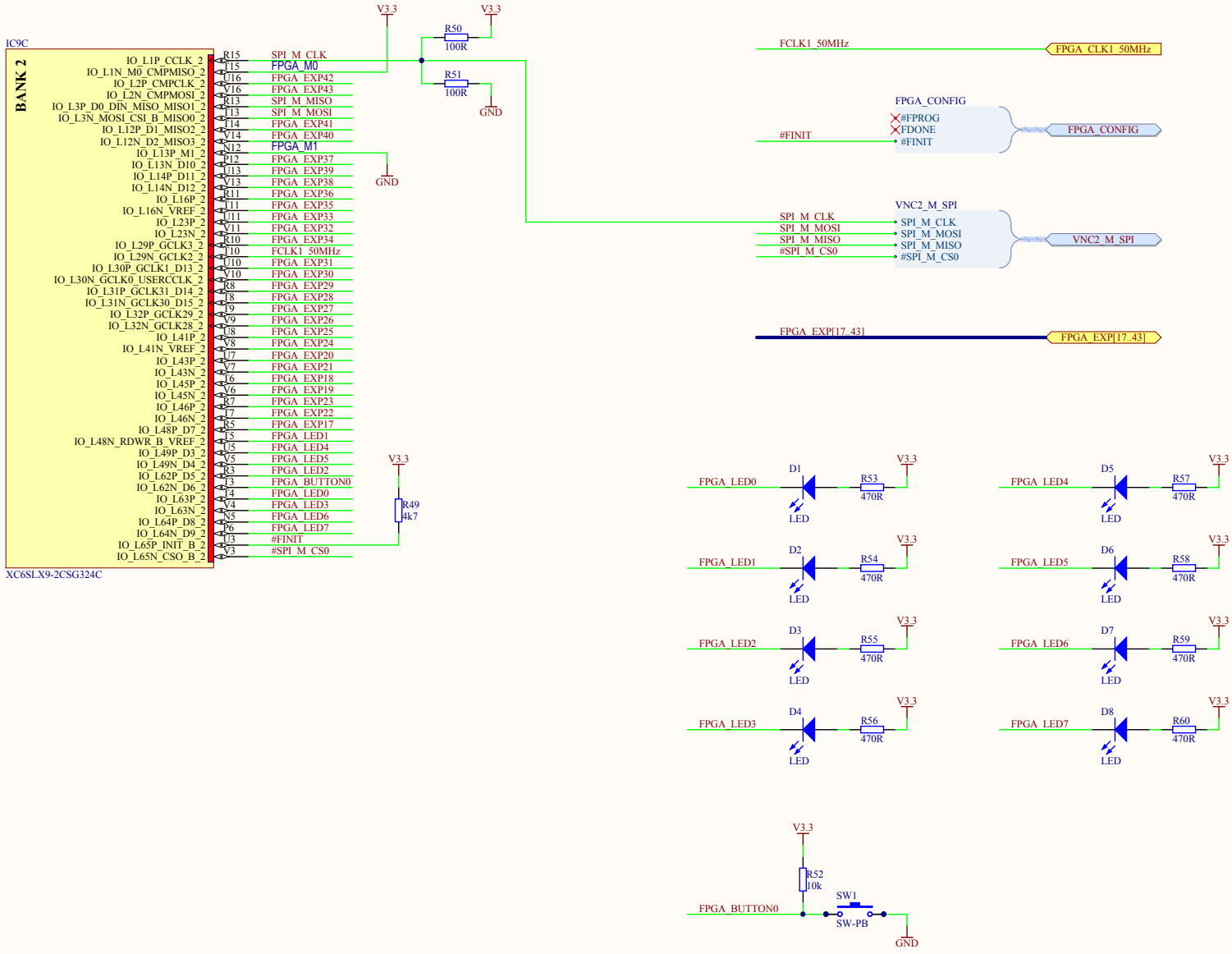
Title	Minerva.PrjPcb	
Size: A3	Number: DVI Controller.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet12of20
File: E:\Work\..\DVI Controller.SchDoc		Drawn By: Vaclav Simek



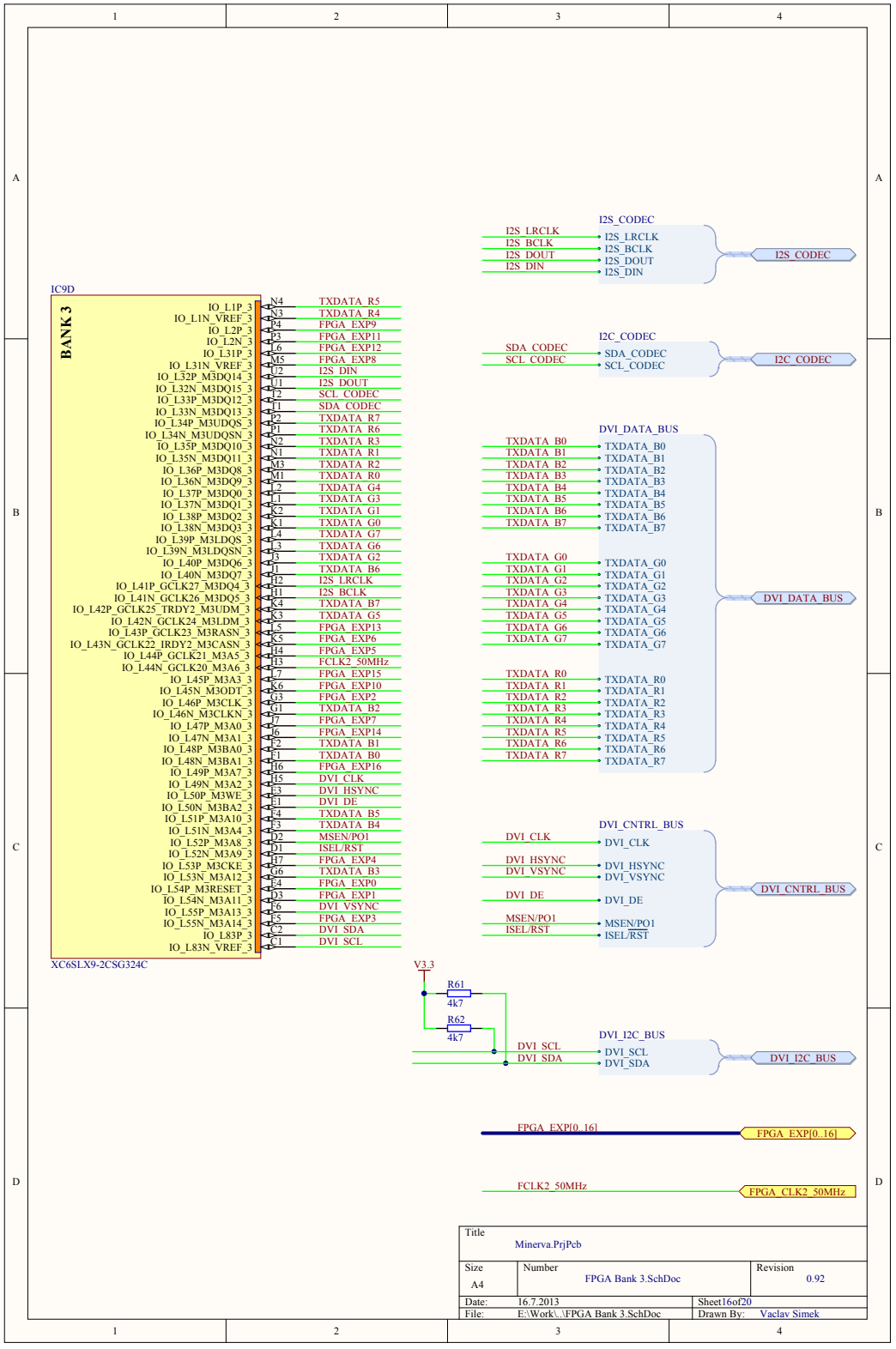
Title	Minerva.PrjPcb	
Size: A4	Number: FPGA Bank 0.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet 13 of 20
File: E:\Work\..\FPGA Bank 0.SchDoc		Drawn By: Vaclav Simek

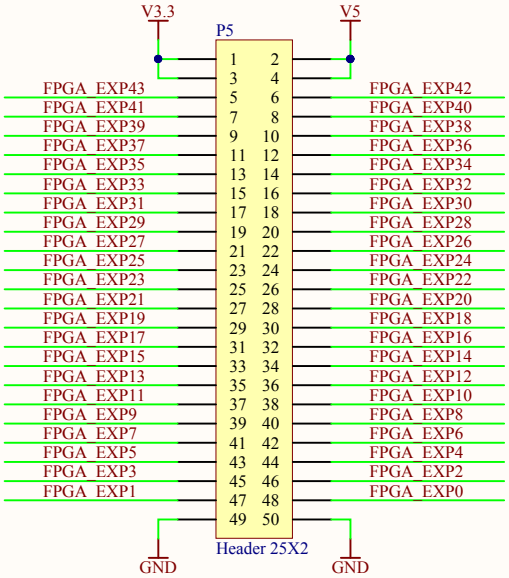


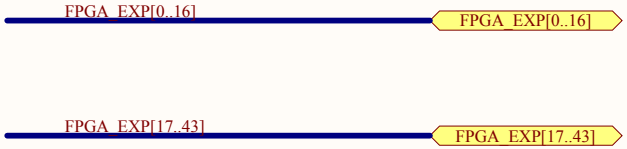
Title	Minerva.PrjPcb	
Size: A4	Number: FPGA Bank 1.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet14of20
File: E:\Work\..\FPGA Bank 1.SchDoc		Drawn By: Vaclav Simek



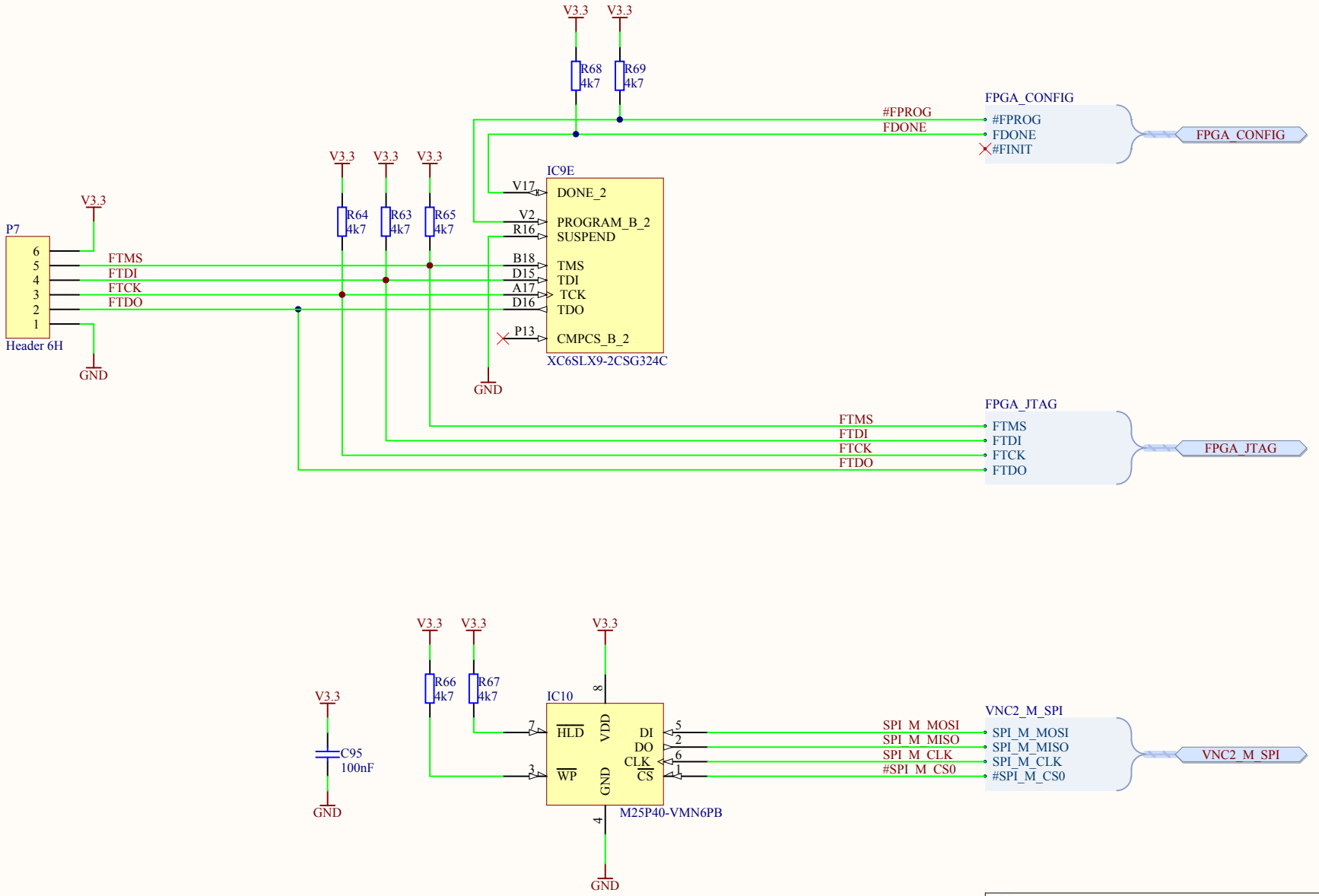
Title	Minerva.PrjPcb	
Size: A3	Number: FPGA Bank 2.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet15of20
File: E:\Work\..\FPGA Bank 2.SchDoc		Drawn By: Vaclav Simek


IC9D
BANK 3
IO_L1P_3
IO_L1N_VREF_3
IO_L2P_3
IO_L2N_3
IO_L31P_3
IO_L31N_VREF_3
IO_L32P_M3DQ14_3
IO_L32N_M3DQ15_3
IO_L33P_M3DQ12_3
IO_L33N_M3DQ13_3
IO_L34P_M3UDQS_3
IO_L34N_M3UDQSN_3
IO_L35P_M3DQ10_3
IO_L35N_M3DQ11_3
IO_L36P_M3DQ8_3
IO_L36N_M3DQ9_3
IO_L37P_M3DQ0_3
IO_L37N_M3DQ1_3
IO_L38P_M3DQ2_3
IO_L38N_M3DQ3_3
IO_L39P_M3LDQS_3
IO_L39N_M3LDQSN_3
IO_L40P_M3DQ6_3
IO_L40N_M3DQ7_3
IO_L41P_GCLK27_M3DQ4_3
IO_L41N_GCLK26_M3DQ5_3
IO_L42P_GCLK25_TRDY2_M3UDM_3
IO_L42N_GCLK24_M3LDM_3
IO_L43P_GCLK23_M3RASN_3
IO_L43N_GCLK22_IRDY2_M3CASN_3
IO_L44P_GCLK21_M3A5_3
IO_L44N_GCLK20_M3A6_3
IO_L45P_M3A3_3
IO_L45N_M3ODT_3
IO_L46P_M3CLK_3
IO_L46N_M3CLKN_3
IO_L47P_M3A0_3
IO_L47N_M3A1_3
IO_L48P_M3BA0_3
IO_L48N_M3BA1_3
IO_L49P_M3A7_3
IO_L49N_M3A2_3
IO_L50P_M3WE_3
IO_L50N_M3BA2_3
IO_L51P_M3A10_3
IO_L51N_M3A4_3
IO_L52P_M3A8_3
IO_L52N_M3A9_3
IO_L53P_M3CKE_3
IO_L53N_M3A12_3
IO_L54P_M3RESET_3
IO_L54N_M3A11_3
IO_L55P_M3A13_3
IO_L55N_M3A14_3
IO_L83P_3
IO_L83N_VREF_3
N4 TXDATA_R5
N3 TXDATA_R4
P4 FPGA_EXP9
P3 FPGA_EXP11
L6 FPGA_EXP12
M5 FPGA_EXP8
J2 I2S_DIN
J1 I2S_DOUT
L2 SCL_CODEC
L1 SDA_CODEC
P2 TXDATA_R7
P1 TXDATA_R6
N2 TXDATA_R3
N1 TXDATA_R1
M3 TXDATA_R2
M1 TXDATA_R0
K2 TXDATA_G4
K1 TXDATA_G3
J2 TXDATA_G1
G1 TXDATA_G0
J4 TXDATA_G7
J3 TXDATA_G6
J1 TXDATA_G2
H1 TXDATA_B6
H2 I2S_LRCLK
H1 I2S_BCLK
K4 TXDATA_B7
K3 TXDATA_G5
L5 FPGA_EXP13
K5 FPGA_EXP6
H4 FPGA_EXP5
H3 FCLK2_50MHz
L7 FPGA_EXP15
K6 FPGA_EXP10
G3 FPGA_EXP2
G1 TXDATA_B2
F7 FPGA_EXP7
J6 FPGA_EXP14
F2 TXDATA_B1
F1 TXDATA_B0
H6 FPGA_EXP16
H5 DVI_CLK
E3 DVI_HSYNC
E1 DVI_DE
F4 TXDATA_B5
F3 TXDATA_B4
D2 MSEN/PO1
D1 ISEL/RST
H7 FPGA_EXP4
G6 TXDATA_B3
E4 FPGA_EXP0
D3 FPGA_EXP1
E6 DVI_VSYNC
E5 FPGA_EXP3
C2 DVI_SDA
C1 DVI_SCL
XC6SLX9-2CSG324C
I2S_CODEC
I2S_LRCLK
I2S_BCLK
I2S_DOUT
I2S_DIN
I2S_LRCLK
I2S_BCLK
I2S_DOUT
I2S_DIN
I2S_CODEC
I2C_CODEC
SDA_CODEC
SCL_CODEC
SDA_CODEC
SCL_CODEC
I2C_CODEC
DVI_DATA_BUS
TXDATA_B0
TXDATA_B1
TXDATA_B2
TXDATA_B3
TXDATA_B4
TXDATA_B5
TXDATA_B6
TXDATA_B7
TXDATA_G0
TXDATA_G1
TXDATA_G2
TXDATA_G3
TXDATA_G4
TXDATA_G5
TXDATA_G6
TXDATA_G7
TXDATA_R0
TXDATA_R1
TXDATA_R2
TXDATA_R3
TXDATA_R4
TXDATA_R5
TXDATA_R6
TXDATA_R7
DVI_DATA_BUS
DVI_CNTRL_BUS
DVI_CLK
DVI_HSYNC
DVI_VSYNC
DVI_DE
MSEN/PO1
ISEL/RST
DVI_CLK
DVI_HSYNC
DVI_VSYNC
DVI_DE
MSEN/PO1
ISEL/RST
DVI_CNTRL_BUS
V3.3
R61
4k7
R62
4k7
DVI_SCL
DVI_SDA
DVI_I2C_BUS
DVI_SCL
DVI_SDA
DVI_I2C_BUS
FPGA_EXP[0..16]
FPGA_EXP[0..16]
FCLK2_50MHz
FPGA_CLK2_50MHz
Title
Minerva.PrjPcb
Size
A4
Number
FPGA Bank 3.SchDoc
Revision
0.92
Date:
16.7.2013
Sheet16of20
File:
E:\Work\..\FPGA Bank 3.SchDoc
Drawn By:
Vaclav Simek



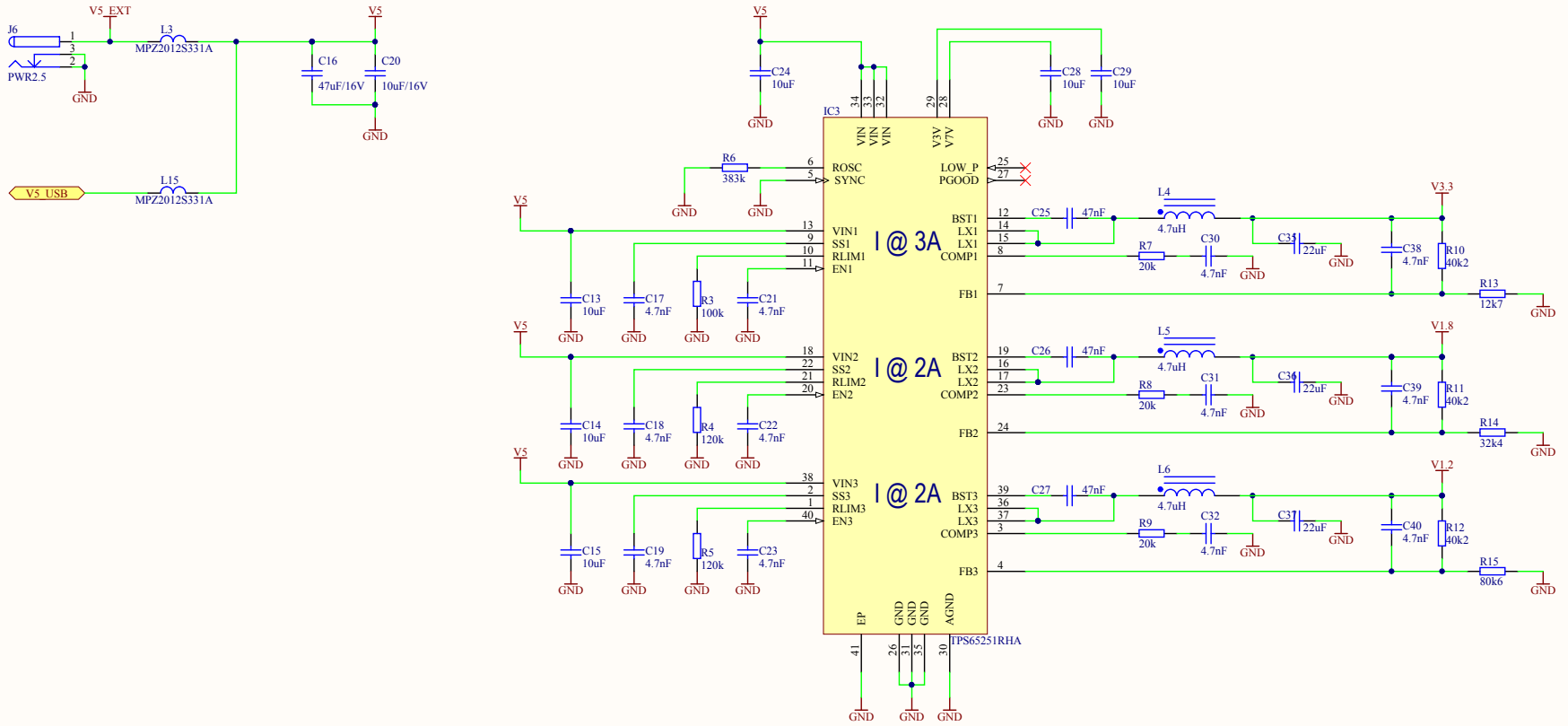


Title: Minerva.PrjPcb		
Size: A4	Number: FPGA_Expansion.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet 17 of 20
File: E:\Work\..\FPGA_Expansion.SchDoc		Drawn By: Vaclav Simek



Title	Minerva.PrjPcb	
Size: A4	Number: FPGA Config.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet 18 of 20
File: E:\Work\..\FPGA Config.SchDoc		Drawn By: Vaclav Simek

Title	Minerva.PrjPcb	
Size A3	Number FPGA Power.SchDoc	Revision 0.92
Date: 16.7.2013		Sheet 19 of 20
File: E:\Work\..\FPGA Power.SchDoc		Drawn By: Vaclav Simek



Title	Minerva.PrjPcb	
Size: A3	Number: Board Power.SchDoc	Revision: 0.92
Date: 16.7.2013		Sheet20of20
File: E:\Work\..\Board Power.SchDoc		Drawn By: Vaclav Simek