Mechtron 3TB4: Embedded Systems Design II
Tutorial Lab 1

Introduction to Quartus Prime and DE1-SoC (Jan. 22nd - Jan. 26th)

Reports Due: On Avenue, 1 minute prior to the start of Lab 1 sessions in the week of Jan. 29th (along with the pre-lab report)

Goals

- Introduce the Quartus Prime software
- Learn how to describe simple circuitry in Verilog HDL Note: **The following documents may help you with your lab. Please go over them at your convenience, in addition to the class notes.**
- Introduction to the software. Go to ALTERA's web site at: `https://www.altera.com/products/design-software/fpga-design/quartus-prime/overview.html`
- After you install the software (see "Activities" below) you may fiand more help topics under the "Help" menu.
- You may also wish to consult `http://www.asic-world.com/verilog/index.html` for lessons and references on Verilog HDL.

Lab Equipment and Software

In this tutorial you will be introduced to the new development board that we will use for future labs. Altera's DE1-SoC development board is built around an FPGA device that can be programmed to implement arbitrary logic circuits. The FPGA is connected to many on-board peripherals, as shown in Figure 1

Peripheral connections

This device contains many peripherals that can be used with the FPGA. The file DE1-SoC.qsf provides a pin-map to connect the FPGA's output ports to the surrounding peripherals. For this lab, you will be required to use the DE1-SoC pin assignments to interface with the peripherals of the DE1-SoC development board.

Cyclone V FPGA

The Cyclone V FPGA will be used to implement the hardware logic.

Software Environment

The software environment consists of the Quartus Prime CAD tool.
As a part of your preparation, you will complete a tutorial that will introduce you to the Quartus Prime user interface.

Activities

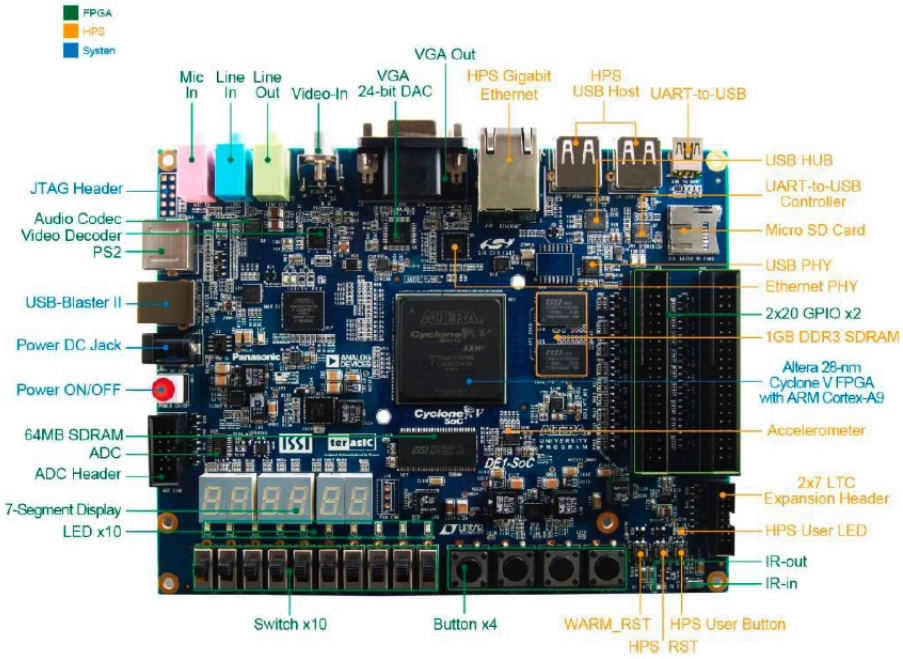

Figure 1: Altera DE1-SoC Board

Pre-tutorial

The following activities must be completed by each student independently before attending this tutorial.

1) Install either the Standard Edition or the Lite Edition of Quartus Prime on your personal computer, available from Altera's website (`https://www.altera.com/downloads/download-center.html`)

   It is recommended to download and install version 17.1 Please install the Standard Edition, and set up the license.
   To do so, click `Tools | License Setup...`
   from Quartus, input
   `"27000@alteralm.mcmaster.ca"` (without quotation marks) in the
   "License File" box. You will need a VPN connection to use the license file.

   You need to download 1) Quartus Prime (includes Nios II EDS). 2) ModelSim-Intel FPGA Edition (includes Starter Edition). 3) Cyclone V device support.

2) Look at the tutorial videos posted at Avenue in the folder "Labs/Tutorial Videos".

   - *"1 - How to Create a Project.mp4"*
   - *"2 - Module syntax.mp4"*
   - *"3 - Gate level model.mp4"*

3) The FAQ for SE2DA4 at `http://www.cas.mcmaster.ca/~leduc/FAQ.html` contains some useful information about the DE1-SoC board. This FAQ also provides details for setting up the license and some instructions for programming the board and simulating a project. Reading this FAQ should help you with your labs.

4) Complete the tutorial `Quartus Prime Introduction Using Verilog Designs` available on the course web page.

In the Lab

In the lab you need to work in groups. Using one of the computers in the lab, create a new Quartus project, as you learned in the "Quartus Prime Introduction Using Verilog Designs" tutorial.

1) Connect the DE1-SoC board to its power supply.

2) Follow Section 7 of the tutorial for pin assignment (`Quartus Prime Introduction Using Verilog Designs`). **Alternatively**, you can import pin assignments from the `DE1-SoC.qsf` file provided on the course web page. To assign pins by importing the file `DE1-SoC.qsf`, you need to use the DE1-SoC peripheral names as in the file `DE1-SoC.qsf` In the pin assignment file `DE1-SoC.qsf`, the pins are assigned by sentences like: `"set location assignment PIN AB12 -to SW[0]"`. In this sentence, the pin is **"PIN AB12"**, the peripheral name is **"SW[0]"**, which is the first toggle switch on the DE1-SoC board.

3) **Before compiling, make sure that all unused pins are reserved as "Input tri-stated"**. This option is available under
`Assignments | Device > Device and Pin Options > Unused Pins`.

4) Complete Sections 8 and 10 of the `Quartus Prime Introduction Using Verilog Designs` tutorial.

5) Submit your compiled circuit (the .sof file located in `project_name\noutput_files)` to the Avenue dropbox and request a demo from your TA. Take a screenshot of the compilation report for inclusion in your report.

6) Use functional simulation to verify the intended function of the circuit.
Note: The steps in this document: "DE1 SoC Quartus17 Simulation Notes.pdf" need to be completed before simulating. The same steps are shown in the video *"3 - Gate level model.mp4"* from (6m:10s).
Note: For Quartus Prime version 17.1, **timing simulations are not supported** for the Cyclone V FPGA. For a project that is set up for Cyclone V, the result of running a timing simulation will be identical to the functional simulation.

7) Complete the tutorial `"Introduction to Simulation of Verilog Designs"` available on the course web page.
Please Note: In some situations, some nodes may be "synthesized away" during the synthesis and analysis process, as a result it is not possible to observe these nodes during simulation or the signal probing process. Verilog HDL provides some synthesis attributes to direct Analysis & Synthesis to keep them intact. These attributes include "/*synthesis keep */", "/*synthesis preserve */" and "/*synthesis noprune */". For more details about these three synthesis attributes, please read the appropriate Quartus help files or other materials available on the web. With Quartus version 17.1 and the Modelsim-Altera simulator, the above mentioned synthesis attributes and directives appear to not work well. To correctly simulate some nets or regs in your modules that would be "synthesized away", please temporarily declare them as output ports. In this lab project, there is no node that will be "synthesized away", but it may happen with your later lab projects.

8) Show the result of your simulation to one of the TAs and take screenshots for your report.

Report

Describe what you did in this tutorial, and include the screen shots taken during various experiments. You are also required to submit the pre-lab report as described in the Lab 1 document. This material must be submitted to Avenue 1 minute prior to the start of Lab 1.