

Design and Implementation (in Verilog) of Pong Game

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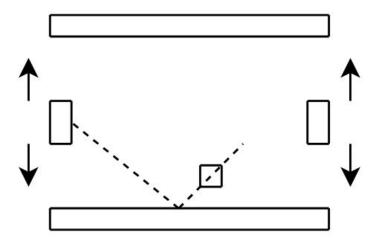
ECE Department, WPI

Outline

- Purpose.
- Hierarchy of Modules.
- Block Diagram.
- IP Cores.
- Custom Hardware Modules.
- FPGA resource usage.
- Video of the Implementation of the Design.

Purpose

- ☐ To design Pong Game in Verilog:
 - the 2-player mode.



Hierarchy of Modules

```
∨ □ Design Sources (2)

√ ● ∴ top (top.v) (5)

        > 🗗 🔳 mmcm_ip:clk_wiz_0 (clk_wiz_0.xci)

✓ ● game: game_logic (game_logic.v) (4)
              paddle_1: paddle_ctrl (paddle_ctrl.v)
              paddle 2 : paddle ctrl (paddle ctrl.v)
              borders : borders_ctrl (borders_ctrl.v)
              ball : ball_ctrl (ball_ctrl.v)
          vga_ctrl_ip: vga_controller_640_60(Behavioral) (vga_controller_640_60.vhd)

✓ ● sev_seg: seven_seg_4(Behavioral) (seven_seg_4.vhd) (4)

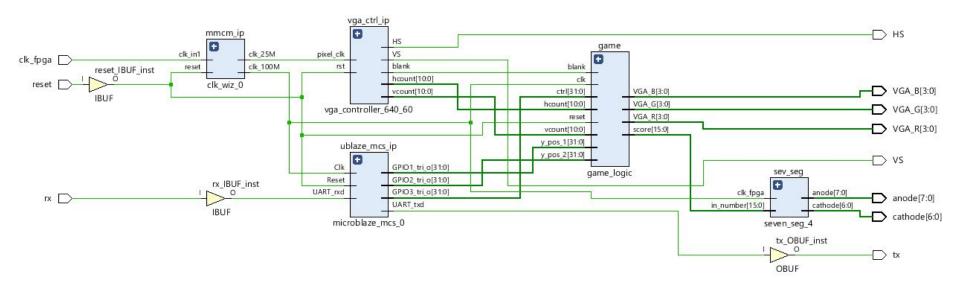
                 decoder0: decoder(Behavioral) (decoder.vhd)
              decoder1 : decoder(Behavioral) (decoder.vhd)
              decoder2 : decoder(Behavioral) (decoder.vhd)
              decoder3 : decoder(Behavioral) (decoder.vhd)
        > 🗗 🔳 ublaze_mcs_ip : microblaze_mcs_0 (microblaze_mcs_0.xci)
   ∨ 🗁 ELF (1)
          pong_game.elf

∨ □ Constraints (1)

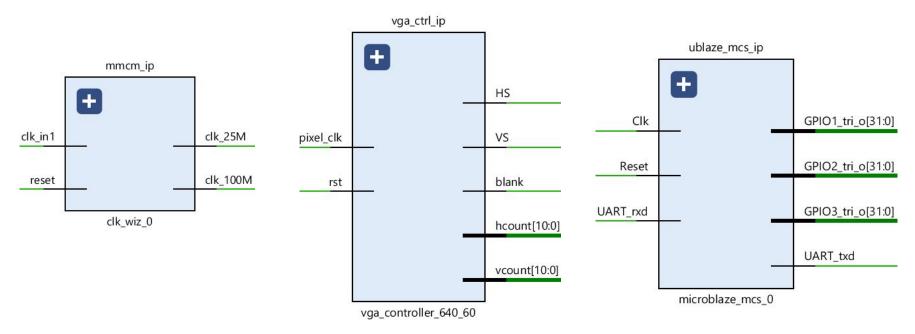
∨ □ constrs_1 (1)

          vga_verilog.xdc (target)
```

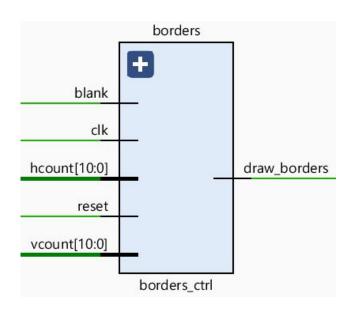
Block Diagram: top.v



IP Cores: Clock Wizard, VGA Controller, MicroBlaze

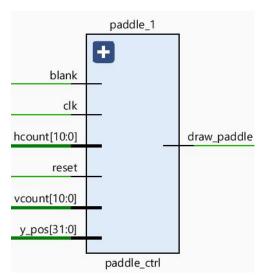


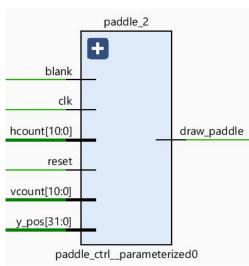
Custom Modules: borders_ctrl.v



```
module borders ctrl
    # (//dimensions of the game field
        parameter BORDER WIDTH
                                 = 4'd10,
        parameter X LEFT BORDER = 10'd19,
        parameter X RIGHT BORDER = 10'd620,
        parameter Y_UP_BORDER
                                 = 10'd19,
        parameter Y DOWN BORDER
                                 = 10' d460)
        input clk,
        input reset,
        input[10:0] hcount,
        input[10:0] vcount,
        input blank,
        output reg draw borders
    );
```

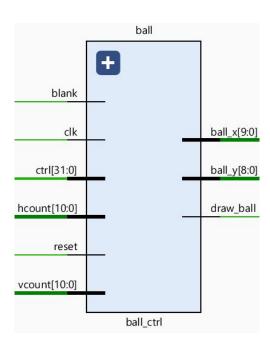
Custom Modules: paddle_ctrl.v





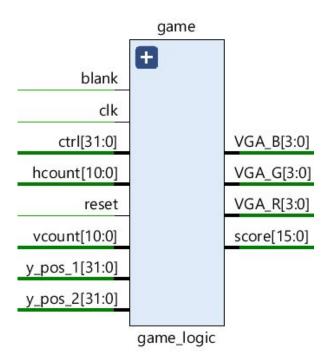
```
module paddle_ctrl
    #(//the upper left corner of the paddle in pixels
    parameter PADDLE_X = 10'd616,
    //paddle's width and height in pixels
    parameter PADDLE_WIDTH = 10'd5,
    parameter PADDLE_HEIGHT = 10'd48)
(
    input clk,
    input reset,
    input[10:0] hcount,
    input[10:0] vcount,
    input[31:0] y_pos,
    output reg draw_paddle
);
```

Custom Modules: ball_ctrl.v



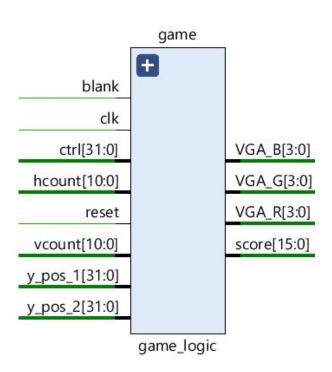
```
module ball ctrl
    #(//screen resolution in pixels
     parameter SCREEN WIDTH = 10'd640,
     parameter SCREEN HEIGHT = 9'd480,
      //dimensions of the game field in pixels
     parameter BORDER WIDTH = 4'd10,
     parameter Y UP BORDER = 10'd19,
     parameter Y DOWN BORDER = 10'd460,
      //the positions of the paddle 1 and paddle 2
     parameter PADDLE X 1 = 5'd19,
     parameter PADDLE X 2 = 10'd616,
      //paddle's width in pixels
     parameter PADDLE WIDTH = 10'd5,
      //ball's speed
     parameter BALL SPEED = 20'd1 000 000,
      //ball's width and height in pixels
     parameter BALL SIZE = 4'd10)
       input clk,
       input reset,
       input[10:0] hcount,
       input[10:0] vcount,
       input blank,
       input[31:0] ctrl,
       output reg draw ball,
       output reg[9:0] ball x,
       output reg[8:0] ball y
   );
```

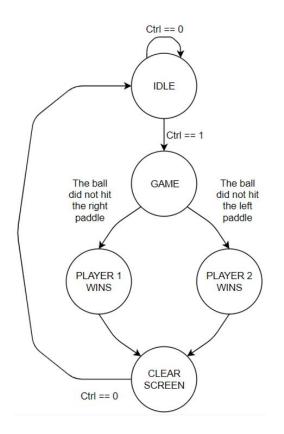
Custom Modules: game_logic.v



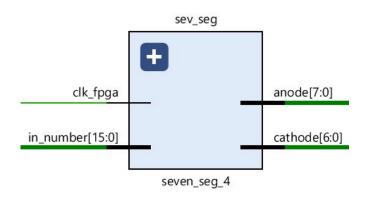
```
module game logic (
    input clk,
    input reset,
    input[10:0] hcount,
    input[10:0] vcount,
    input blank,
    input[31:0] y pos 1,
    input[31:0] y pos 2,
    input[31:0] ctrl,
    output [3:0] VGA R,
    output [3:0] VGA G,
    output [3:0] VGA B,
    output wire [15:0] score
    );
```

Custom Modules: game_logic.v





Custom Modules: seven_segment_4.vhd



```
entity seven_seg_4 is
    Port(
        in_number : in std_logic_vector(15 downto 0);
        clk_fpga : in std_logic;
        cathode : out std_logic_vector(6 downto 0);
        anode : out std_logic_vector(7 downto 0)
        );
end seven_seg_4;
```

```
decoder0 ... decoder3

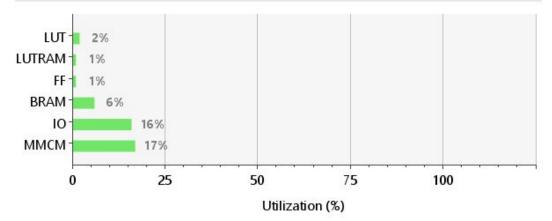
binary_number[3:0] hex_symbol[6:0]

decoder
```

```
entity decoder is
    port (
        binary_number : in std_logic_vector(3 downto 0);
        hex_symbol : out std_logic_vector(6 downto 0)
        );
end decoder;
```

FPGA Resource Usage

Resource	Utilization	Available	Utilization %	
LUT	1122	63400	1.77	
LUTRAM	182	19000	0.96	
FF	1056	126800	0.83	
BRAM	8	135	5.93	
IO	33	210	15.71	
MMCM	1	6	16.67	



FPGA Resource Usage

Name 1	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	Block RAM Tile (135)	Bonded IOB (210)	BUFGCTRL (32)	MMCME2_ADV (6)
∨ N top	1122	1056	32	8	33	3	1
✓ ■ game (game_logic)	257	81	0	0	0	0	0
■ ball (ball_ctrl)	107	59	0	0	0	0	0
■ borders (borders_ctrl)	0	1	0	0	0	0	0
<pre>paddle_1 (paddle_ctrl)</pre>	20	1	0	0	0	0	0
■ paddle_2 (paddle_ctrl_parameter	20	1	0	0	0	0	0
> I mmcm_ip (clk_wiz_0)	0	0	0	0	0	3	1
sev_seg (seven_seg_4)	9	20	0	0	0	0	0
> I ublaze_mcs_ip (microblaze_mcs_0)	776	930	32	8	0	0	0
vga_ctrl_ip (vga_controller_640_60)	92	25	0	0	0	0	0

Thank you!