ECE 574: Modeling and synthesis of digital systems using Verilog and VHDL
Fall Semester 2019

Simple Combinational Project – due ASAP

Complete the VHDL Decoder tutorial for the Nexys4DDR/Nexys-A7 board and modify as follows:

- Change from a 3 to 8 decoder to a 4 to 16 decoder (using four slider switches and 16 LEDs)
- Add a new module called 'seven_seg' in a new file. This should have a 4-bit input and a 7-bit output.
    - Instantiate this module in your top-level module using *named* association.
- The 7-bit output should drive one of the seven segment displays.
- Connect four of the slider switches to the input of the seven_seg module so that the seven segment display shows the value of the switches (from 0 to F)
- Add logic to drive only one of the seven segment displays (turn the other seven displays off).
- Load the design into the serial FLASH (so the board can be powered up with it running)

No lab report is required for this exercise but you need to hand in a hard copy of your two VHDL files (make sure you add the header with your name and ECE box number, and comments) and demo your system to the TA as soon as possible (by week 3 at the latest). You do not need to print out your XDC file.

(If you find this easy then modify the design so you can display a number in the range 00 to FF on two of the seven segment displays. This will require a clock to multiplex the digits)

Reference Material

Read the *Seven Segment* section and other material in the Nexys4DDR/Nexys-A7 (depending on your board) Reference Manual.