

ECE 574: Modeling and synthesis of digital systems using Verilog and VHDL
Fall Semester 2019

**Design and implementation (in Verilog) of a memory interface along
with a Microblaze embedded processor**
Presentation Week 13 (December 4) and
Report Week 14 (December 11)

This project involves the design and implementation of a digital system design using Verilog. You are free to choose to implement any design; but should be complex and include a Microblaze, State Machine and should be written in Verilog.

You will prepare a presentation (about 15 min) that explains the details of your design:

- Aim of the project
- Block Diagram
- State Machine (simple one is enough since there is Microblaze)
- Explanation on the use of Microblaze and hardware (purpose of each unit)
- FPGA resource usage

The bullet points above are couple topics that you need to cover in your presentation. You can include more if you think it is necessary. Please also include a video of your implementation in your presentation. Depending on the project, one to two minutes of video should be satisfactory.

Grading Guidelines

- [30 pts] Presentation
- [30 pts] Implementation
 - Design works on board and meets requirements
- [20 pts] Source Code – Verilog and C program in Appendix
 - Code style and comments (well-commented and tab-indented code!)
 - Use of *case* vs. *if*, spaghetti code vs. structured, etc.
 - Recognizable implementation of "standard" elements (state machines, counters, clock dividers, decoders)
 - Sensible use of modularity
 - No latches or other synthesis problems
- [20 pts] Lab Report
 - [5 pts] Brief Introduction / Problem Statement
 - [10 pts] General Overview of approach to solution and description (include Block and State Diagrams with descriptions).
 - [5 pts] FPGA Resource usage (# flip-flops with explanation) and listing and explanation of warning messages (don't copy all the Xilinx reports – just the relevant sections)
 - [5 pts] Conclusions
 - Problems faced in implementation
 - Solutions used to solve problems
 - Lessons learned from the project