Worcester Polytechnic Institute

ECE 5723: Methodologies for System Level Design and Modeling

SystemC RTL Design

by

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Laboratory Report

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1. Introduction

In this work, a circuit producing the average of the 8 serial byte-data on its input (Fig. 1) is designed in SystemC:

- The circuit starts its operation with a complete pulse on *start* (0-1-0).
- After that, the next eight bytes on *data* will be received and the average of the eight will be calculated.
- When this is completed, the *avg* output will contain the integer part of the calculated average, and the *rdy* signal becomes 1. This signal remains active until the next time that *start* becomes 1.

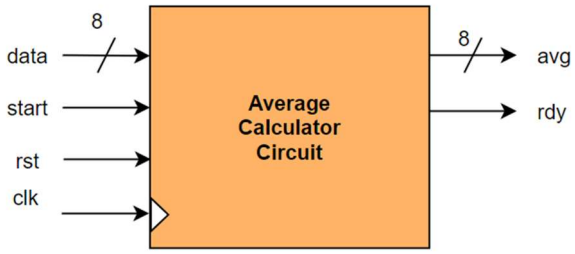


Fig. 1 – Diagram of Average Calculator Circuit

2.Analysis of the Task

Based on the information given in the introduction, the graph shown in Fig. *2* for the waveforms was derived

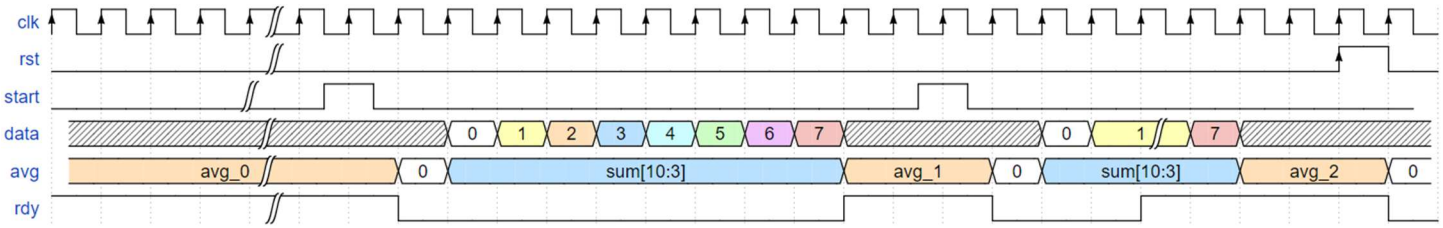


Fig. 2 – The waveforms demonstrate the operation of the average calculator

3. Schematic Diagram of Datapath and Controller

In this chapter, the diagrams of the data path and the controller for the circuit are presented in Fig. 3.

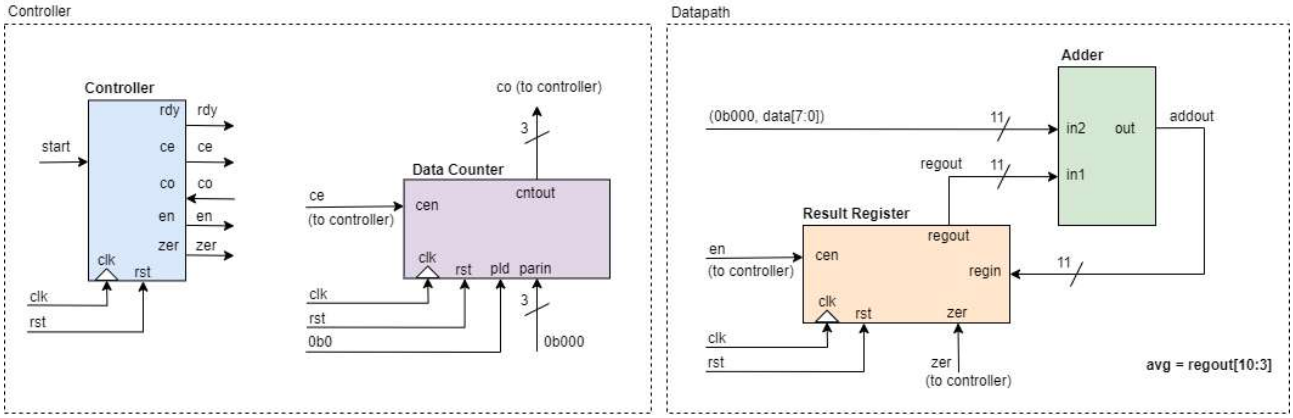


Fig. 3 – The schematic diagram of average calculator

Here, the division by 8 is implemented by dropping three least significant bits of the 11-bit output register.

4. Controller State Diagram

In this chapter, the controller state diagram of the designed circuit is shown in **Fig. 4**.

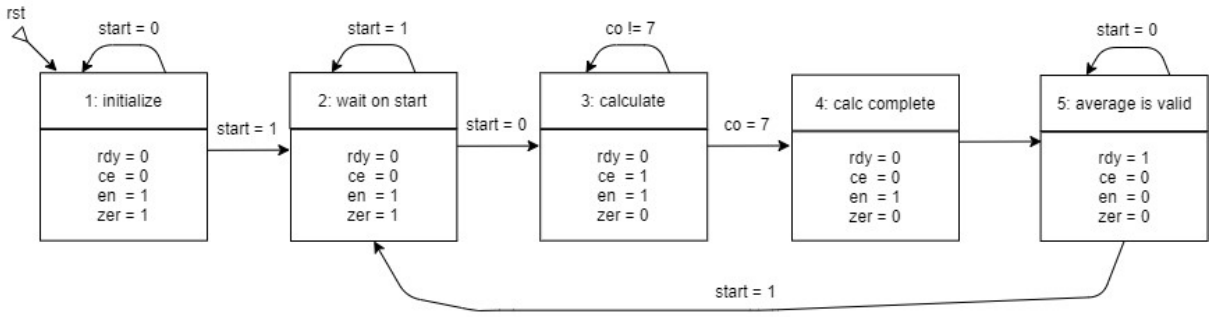
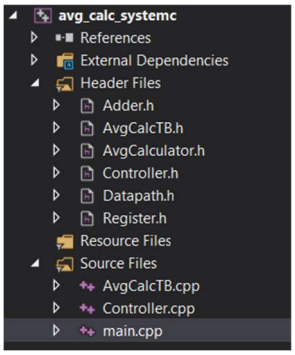


Fig. 4 *– The state diagram of the average calculator circuit*

The controller unit is developed using *Huffman model.*

5. Schematic Development in SystemC

For implementing the design, separate source files for the data path and for the controller were written first. Then, they were interconnected in the average calculator module. After that, the average calculator was placed in the testbench. Finally, the testbench was instantiated inside the main() function:

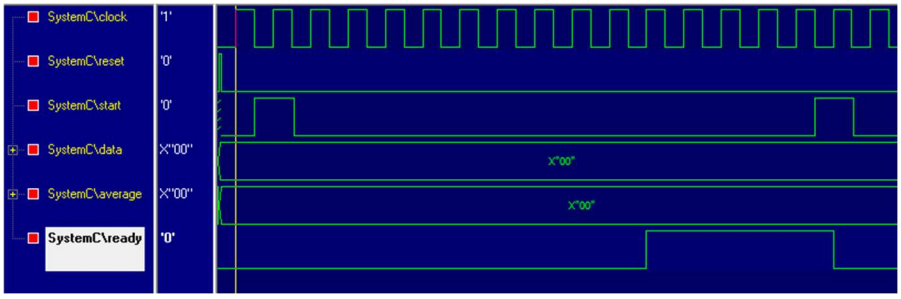


6. Testing the Average Calculator

In this chapter, the results of the verification of designed circuit are provided for four different scenarios.

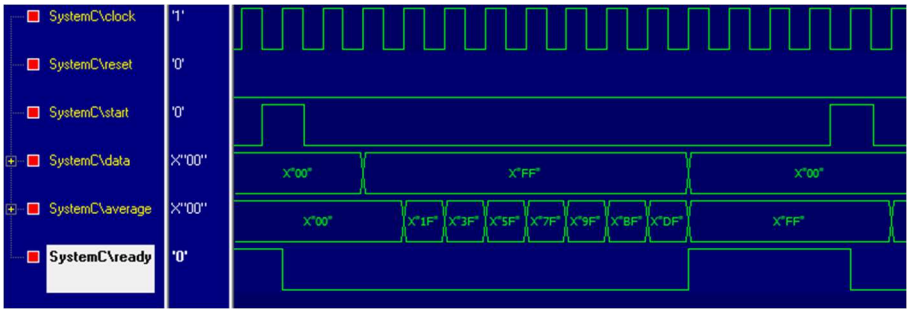
6.1. Scenario 1

In this test scenario, all the 8 bytes of input data are 0x00. Expected average = 0x00.



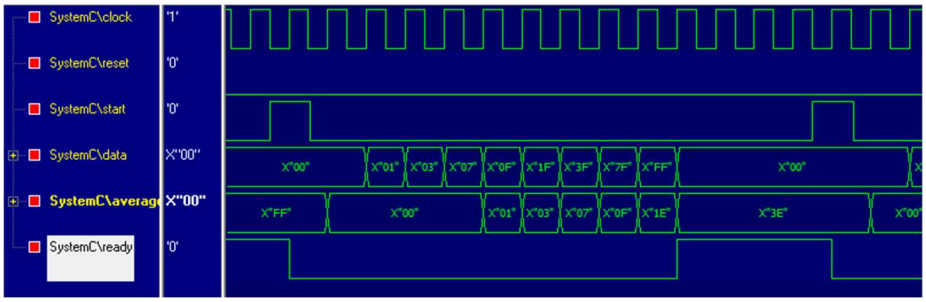
6.2. Scenario 2

In this test scenario, all the 8 bytes of input data are 0xFF. Expected average = 0xFF.



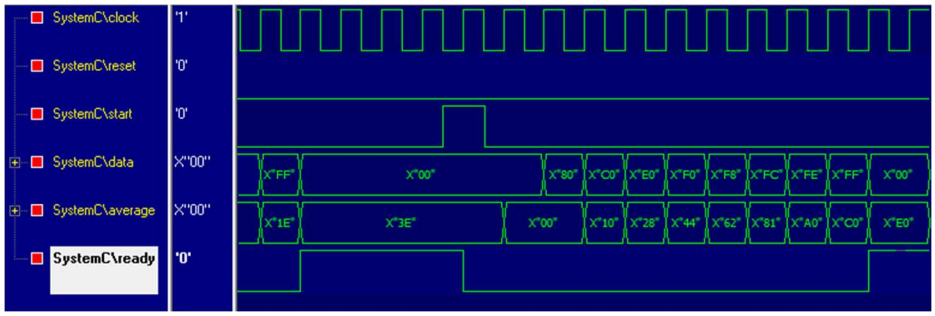
6.3. Scenario 3

In this test scenario, the input data bytes are 0x01, 0x03, 0x07, ..., 0xFF.Expected average = 0x3E.



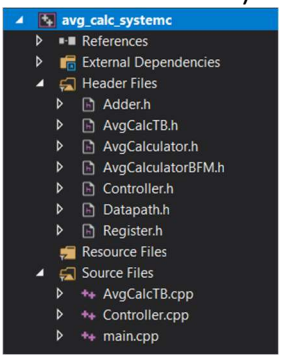
6.4. Scenario 4

In this test scenario, the input data bytes are 0x80, 0xC0, 0xE0, ..., 0xFF. Expected average = 0xE0.



7. Bus Functional Model (BFM) of the Average Calculator

A cycle-accurate behavioral model (BFM: Bus Functional Model) for the circuit was developed:



The model was tested with the same scenarios as in chapter 6. The results of the tests for the model were the same as for the actual design (Fig. 5).

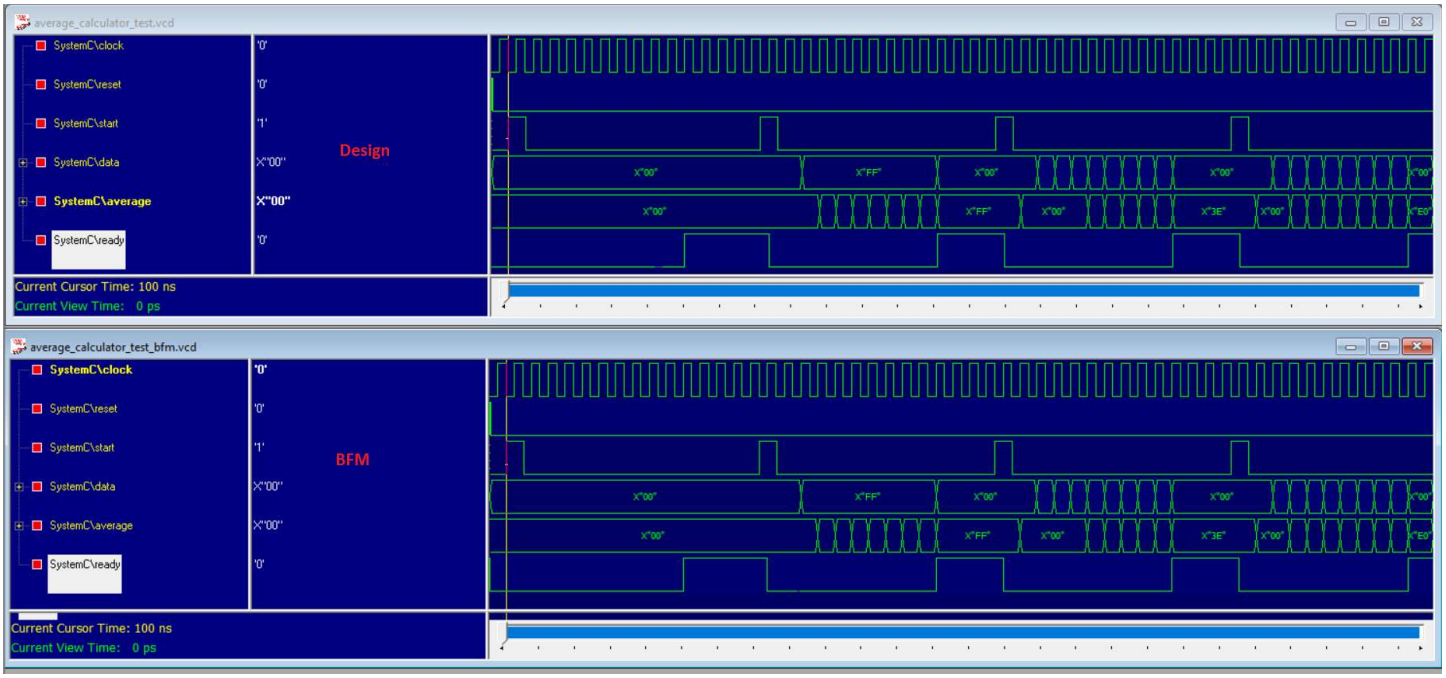


Fig. 5 *– Comparison of the simulation results for the design and its BFM*

8. Conclusions

In this work, a circuit producing the average of the 8 serial bytes on its input and its bus functional model were designed and tested in SystemC.