Worcester Polytechnic Institute

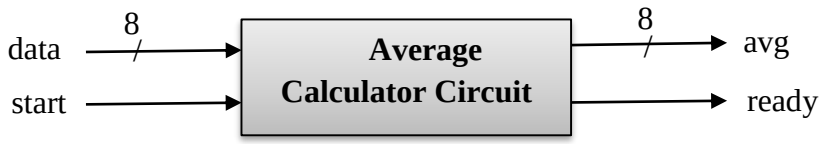
Electrical and Computer Engineering Department

Methodologies for System Level Design and Modeling - ECE 5723
Online Offering – Fall 2020
Homework 4: SystemC RTL design
Due Date: October 18

Description:

You have already done C++ modeling of the average calculator circuit that produces the average of its serial 8-bit data received on its input. The circuit starts its operation with a complete pulse on *start* (0-1-0). After that, the next eight bytes on *data* will be received and the average of the eight will be calculated. When this is completed, the *avg* output will contain the integer part of the calculated average, and the *ready* signal becomes 1. This signal remains active until the next time that *start* becomes 1. Implementation of division by 8 can be performed by dropping three least significant bits.

In this homework, you are to model the circuit using SystemC in two ways (Parts A, B and Part D). You can use the design provided for the Homework 2 solution.



A. Show the schematic diagram of the datapath of this circuit and then implement the datapath (DP) of the circuit using SystemC RTL components.
B. Show the controller state diagram of the circuit and then develop the controller unit (CU) using **Huffman model**.
C. Complete the design of the average calculator circuit by wiring CU and DP in a top-level module and write a testbench to verify your design using four different scenarios.
D. Develop a cycle-accurate behavioral model (BFM: Bus Functional Model) for the circuit and test it with the same scenarios as in Part C.

Attention:

This homework covers “Topic 4 - SystemC RTL Modeling” module on Canvas.

Deliverables:

All your SystemC codes and a complete report containing all parts of the assignment. Make sure that your deliverable follows all mentioned rules in the assignment part of the "*ECE5723 - Comprehensive Syllabus 2020.pdf*" file. The file has been posted on Canvas.