Worcester Polytechnic Institute

Electrical and Computer Engineering Department

Methodologies for System Level Design and Modeling - ECE 5723
Online Offering – Fall 2020
Homework 1: Logic design, VHDL modeling, and testbench
Due Date: September 13

Description:

1. Write RT-level VHDL description for an 8-bit up counter with rising-edge clock, asynchronous reset, count-enable, load-enable, carry-in, carry-out, 8-bit parallel input, and 8-bit parallel output. All control inputs are active high.

2. Use a Toggle Flip-Flop (T-FF) and the counter in Part 1 to build a circuit that divides the clock frequency by 462 with a 50 percent duty cycle. For dividing the clock frequency (*cf*) by number *d* (here *d* is 462), you are to use a modulo-*n* counter (here *n* is 256) that starts counting from *n-(d/2)* and goes up to *n-1*. In this case, the frequency of the carry-out signal becomes *cf/(d/2)*. To achieve this, take the carry-out and run it into the counter load input. For the parallel input use *n-(d/2)*. When the count reaches *n-1*, carry-out becomes 1 that causes *n-(d/2)* to be loaded into the counter on the next clock. Then the count continues until the count reaches *n-1* again. In the next step, you should add a T-FF to the carry-out signal of the counter to produce the frequency *cf/d* with a 50 percent duty cycle. As you know, T-FF behaves as a "divide-by-2" counter.

When the counter first starts, it starts with 0. The first time around, divide by *d* will not happen and the counter counts *n*. You do not have to worry about this case, but you will get a bonus if you provide an initialization signal to take care of this situation.

A. Show the schematic diagram of the frequency divider.
B. Write the VHDL description of the frequency divider.
C. Write a testbench for the circuit in VHDL that tests the correctness of your circuit.
D. Show the results of the simulation including the counter clock, the carry-out signal, and the generated clock frequency (the output of the T-FF) in your report.

Attention:

This homework covers “Topic 0.1 - Logic review” and “Topic 0.2 - HDL Background” modules on Canvas.

Deliverables:

All your VHDL codes and a complete report containing all parts of the assignment. Make sure that your deliverable follows all mentioned rules in the assignment part of the "*ECE5723 - Comprehensive Syllabus 2020.pdf*" file. The file has been posted on Canvas.