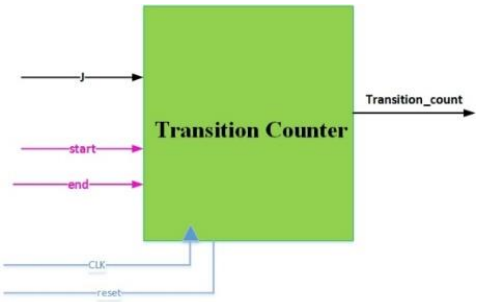
Worcester Polytechnic Institute

Electrical and Computer Engineering Department

Methodologies for System Level Design and Modeling - ECE 5723
Online Offering – Fall 2020
Homework 3: C++ RT-level design and modeling
Due Date: October 04

Description:

You are to design a circuit that counts the number of transitions that occur on its serial input. The circuit is a clocked circuit with a serial input, *J*. There is a *start* pulse and an *end* pulse. After the *start* pulse (0-1-0, guaranteed one pulse), the counting begins and continues until a pulse is detected on *end*. During this time, clocked-synchronous transitions are detected and counted on the *J* input. An 8-bit counter is used here and counting beyond 256 rolls over back to 0. Provide an asynchronous reset.



A. Show the schematic diagram of the datapath of this circuit.
B. Show the controller **state diagram** of the circuit.
C. Develop the controller (CU) using C++ and the *bus* library discussed in class (Chapter 3). Use **Huffman model**.
D. Implement the datapath (DP) of the circuit using *bus*-based components.
E. Complete the design of the average calculator circuit by wiring CU and DP in a top-level module that properly orders the datapath and controller.
F. Write a testbench and verify your design using four different scenarios.

Attention:

This homework covers “Topic 3 - RT level modeling with C++ procedural language” module on Canvas.

Deliverables:

All your C++ codes and a complete report containing all parts of the assignment. Make sure that your deliverable follows all mentioned rules in the assignment part of the "*ECE5723 - Comprehensive Syllabus 2020.pdf*" file. The file has been posted on Canvas.