Worcester Polytechnic Institute

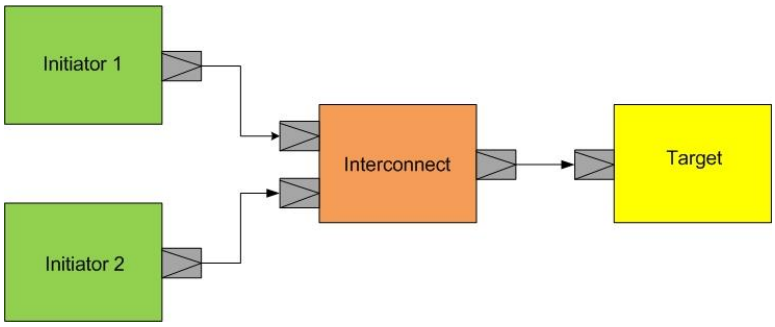
Electrical and Computer Engineering Department

Methodologies for System Level Design and Modeling - ECE 5723
Online Offering – Fall 2020
Homework 6: SystemC Transaction Level Modeling
Due Date: November 22

Description:

In this problem, you are to design the system shown below using the TLM2.0 standard. You can base this work on the blocking example done in the lectures. Use the same data and TLM sockets and implementations, except that you have two initiators here, instead of only one. This necessitates the use of an interconnect that you will develop in this problem.

You should model two initiator modules wanting to read/write from/to a target (memory) using the *b_transport* interface. For this purpose, the initiators must connect to an interconnect module that internally uses *sc_mutex* for arbitration of the target between the initiators. The interconnect then connects to the target memory.
You can use the SystemC codes of Example 2 in the lectures on the SystemC TLM. The example is: *blockingSocketbasedMemoryRW* in SystemC TLM codes file.



A. Write SystemC TLM description of this system.
B. Write a testbench and verify your design.

Attention:

This homework covers “Topic 8 - SystemC Transaction Level Modeling (TLM)” module on Canvas.

Deliverables:

All your SystemC codes and a complete report containing all parts of the assignment. Make sure that your deliverable follows all mentioned rules in the assignment part of the "*ECE5723 - Comprehensive Syllabus 2020.pdf*" file. The file has been posted on Canvas.