Worcester Polytechnic Institute

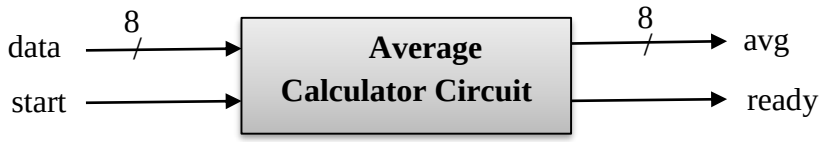
Electrical and Computer Engineering Department

Methodologies for System Level Design and Modeling - ECE 5723
Online Offering – Fall 2020
Homework 2: RT Level design and C++ logic modeling
Due Date: September 27

Description:

You are to design a circuit, producing the average of the serial 8-bit data on its input. The circuit starts its operation with a complete pulse on *start* (0-1-0). After that, the next eight bytes on *data* will be received and the average of the eight will be calculated. When this is completed, the *avg* output will contain the integer part of the calculated average, and the *ready* signal becomes 1. This signal remains active until the next time that *start* becomes 1.

Hint: Implementation of division by 8 can be performed by dropping three least significant bits.



A. Show the schematic diagram of the datapath of this circuit.
B. Show the controller **state diagram** of the circuit.
C. Develop the controller (CU) using C++ and the vector format of the *wire* library discussed in class (Chapter 2). Use **Huffman model**.
D. Implement the datapath (DP) of the circuit using *wire*-based components.
E. Complete the design of the average calculator circuit by wiring CU and DP in a top-level module that properly orders the datapath and controller.
F. Write a testbench and verify your design using four different scenarios.

Attention:

This homework covers “Topic 2 - Object Oriented Logic Modeling” module on Canvas.

Deliverables:

All your C++ codes and a complete report containing all parts of the assignment. Make sure that your deliverable follows all mentioned rules in the assignment part of the "*ECE5723 - Comprehensive Syllabus 2020.pdf*" file. The file has been posted on Canvas.