

# VHF-Transmitter

Hardware section

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VERSION 1.02

# Foreword

This document was created during the “COVID-19” quarantine times in countries which may be marked as “heart of the Europe”. The main scope of the document is hardware proposal of the VHF-Transmitter supporting FM broadcast and necessary software implementation. The main goal is not to create industrially manufactured product, but to extend my knowledge so far acquired during school and work experiences upon the obstacles faced during the development.

Therefore, some design approaches may be considered as not fully professional. However, was placed emphasis to solve all the problems as well as possible. The VHF-Transmitter deserves to be called as the RF – project thus, often was needed very precise way of issue solving. It is expected, that person who reads the document has formal engineer education (or radio-amateur experiences) otherwise, may not understand as many things are not described from scratch. On the other hand, some parts are described in details for my future needs to refresh the specific knowledge, because may be applicable for everyone “you don’t use – you lose”.

The hardware documentation guides through system requirements/proposal and contains several debug results often depicted as the oscilloscope/VNA capture.

At the end, I would strongly emphasize, that any attempt to reproduce the system and its behavior may be in some countries illegal. Everyone who tries to make anything similar should consider laws and regulation for FM transmitting of the country, to do not exceed its legal constrains. Especially, usage of the amplifier and its testing should be done only in anechoic chamber or any safe way, to do not affect any infrastructure.

MSc. Vladimir Sustek in Graz (Austria), spring 2021

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# History

Each technical book starts with some historical story behind the actual scope. The first successful attempts for wireless transmit may be mapped into various experiments in the end of the 19<sup>th</sup> century (such as the famous Italian – G. Marconi). The first radio station KDKA (AM) was launched in 1920 in Pittsburg, Pennsylvania. The KDKA transmitted in frequency 1020kHz and its first broadcasted content was US president election, which won Warren G. Harding.

The FM modulation was invented by an American engineer Edwin H. Armstrong in 1933, but the first FM station called WSM-FM was launched in 1941 in Nashville, Tennessee. The WSM-FM started operation in 44.1MHz frequency. Observation of atmospheric phenomena such as tropospheric propagation and the sporadic E-propagation, which are causing extending the range of waves behind the horizon, pushed the broadcast to range 88-108MHz in order to decrease the risk of interference. Note that the tropospheric propagation is successfully used by radio-amateurs to reach up to 1800km receiving path distance. The FM broadcast started to be widely used in 1960s, almost after 30 years of its invention. The main reason why stations moved into the FM is its higher resilience against interference and much better fidelity for sound signals.

Nowadays, the DAB (Digital Audio Broadcasting) invented in 1995 is becoming to be successor of the FM broadcast. Intended frequency range is 174.928MHz - 239.200MHz, 1452.960MHz - 1490.625MHz respectively, when the OFDM modulation used. This sophisticated system allows higher usage of the bandwidth for data transmission in compare to the FM. Anyway, the FM broadcast and its complementary RDS service seems to be still sufficient, as the DAB as the broadcast successor will need to fight its way through until definitely replaces its ancestors – the FM and AM broadcast.

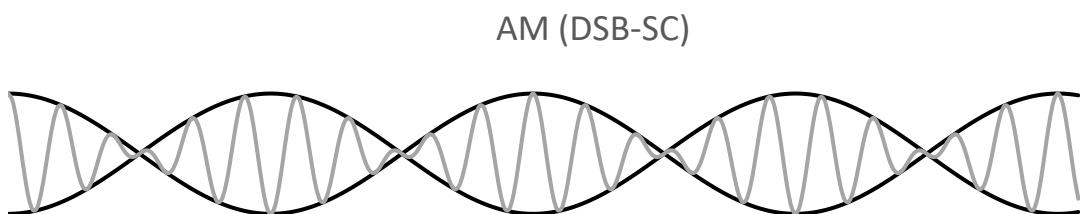


Figure 1 AM-DSBSC modulation (double sideband suppressed carrier)

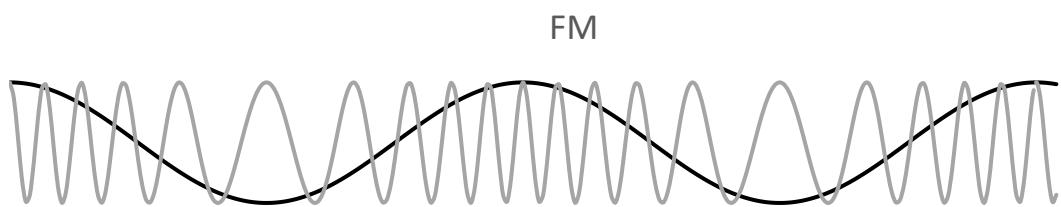


Figure 2 FM modulation

# VHF-Transmitter System Requirements

1. The VHF-Transmitter shall broadcast FM mono audio signal.
2. The VHF-Transmitter shall broadcast FM stereo audio signal.
3. The VHF-Transmitter shall be sufficiently supplied by USB (5V, 0.5A).
4. The VHF-Transmitter shall feature with selectable FM broadcast channel within 88-108MHz.
5. The VHF-Transmitter shall not interfere other frequencies than used channel.
6. The VHF-Transmitter shall feature with basic FM broadcast RDS (station name, song name).
7. The VHF-Transmitter shall feature with the full FM broadcast RDS.
8. The VHF-Transmitter shall be fully controlled via UART.
9. The VHF-Transmitter shall provide maximal possible broadcast power for 5V/50Ω.

## Solution using an FPGA SPARTAN S6

The technical requirements described upper leads into embedded design utilizing fast MCU or smaller FPGA as the system core. An FPGA was chosen rather than MCU due to its speed capabilities and overall possibility of “parallel processing”. The used FPGA is the development module Digilent CMOD S6, which is equipped by Xilinx SPARTAN S6 (Figure 4). The vendor of the module declares usage in frequency even beyond 200MHz using the FPGA’s PLL. If the FPGA can generate frequency 217MHz and drive parallel DAC of speed 217MSPS, it is obvious maximal generated signal may be 108MHz, what is enough to cover whole FM broadcast frequency range. Note that speed such as mentioned are not normally achieved by generally available MCUs. Also, driving the DAC is not the only task for the system core as there is need to sample stereo audio, user control as well as displaying the device status. All in one, the FPGA usage is justified approach. Figure 3 depicts block diagram of the system which is proposed to meet requirements listed upper.

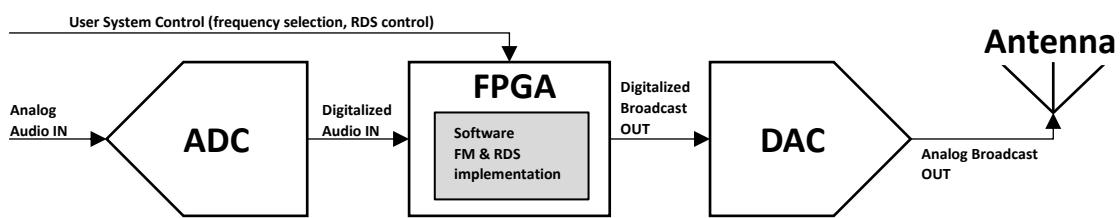


Figure 3 VHF-Transmitter block diagram

The hierarchy of Figure 3 processes an analog audio input signal via the ADC and provides discrete samples into the FPGA. The FPGA upon the user parameters (broadcast frequency) transfers the audio into FM modulated signal represented as digital samples. Finally, the DAC transfers FM signal into analog signal, which is capable to be transmitted by the antenna. The User System Control shall modify all the possible attributes of broadcast as well as the broadcast frequency channel and also the RDS data and so for instance broadcasted station’s name.



Figure 4 CMOD S6 Spartan S6 FPGA module

# System proposal

Following chapter refers to Figure 5, which is the detailed system block diagram. The left and the bottom side of the FPGA block may be understood as the system input section. The right part of Figure 5 is functionally detailed RF transmitting chain for FM broadcast – system output. Note that the upper-right part contains optional output understood as LEDs for signalizing states or the LCD display to provide detailed info.

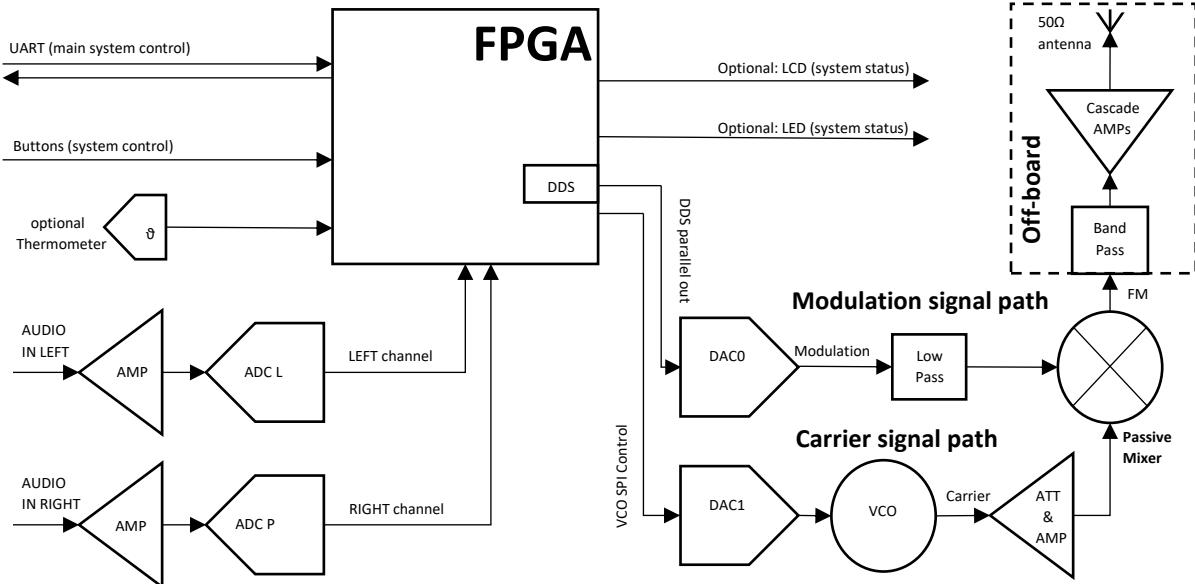


Figure 5 Detailed VHF-Transmitter block diagram

In the following text is explained functionality and expected behavior of each block of Figure 5. All the parts are described just straightforwardly, but the RF output section (DDS parallel out/VCO SPI Control) is explained together with discussing possible other approach and justifying the output circuit complexity.

## System Control (UART, buttons)

The main attributes to be controlled is the already mentioned broadcast frequency adjust (set the broadcast channel), but also for usage of the RDS is needed user input data (station name or played song string). System control takes the upper-left part of Figure 5.

As the FPGA board contains two buttons, they might be used as simple input interface, but complexity of information is limited. There are two options for enhancement, the first is adding mechanical keyboard allowing to write down and send number/letter information into device such as an old mobile phones, or use more generic and fast UART (or any other) interface. The advantage of having keyboard is immediate control of the system, however is needed external hardware what is not always the best approach. Utilizing an UART is more professional and allows faster control and even certain data streaming directly from PC, but this is also disadvantage because PC and USB-UART converter is needed. In addition, the Spartan S6 has neither any UART hardware peripheral, nor is UART part of the Spartan S6 default package, so the peripheral have to be written as the SW module by the engineer.

In the middle left of Figure 5 is also present optional thermometer which has no real reason except ambient temperature measurement.

# Audio input

The audio input is in this case basically main payload to be transmitted. The section responsible for audio processing is the bottom-left part of Figure 5. The FM broadcast audio is normally stereo, so each channel must be sampled extra. The main reason for using the amplifier is to offset the AC sound signal into levels 0 up to  $V_{DD}$ , because typically ADC cannot convert negative voltages. Note that voltage provided by the sound sources such as phone or laptop is not sufficient for sampling without further quality loss during signal reconstruction. Generally, higher voltage is sampled, less is conversion affected by noise and better is the final signal after the reconstruction. Thus, role of amplifier is also to amplify the input signal. As the transmitting frequency is intended to be in band 88-108MHz and audio signals cover band with maximally 20Hz-20kHz, still must be taken in account correct noise/interference decoupling, otherwise may the sampling circuit produce very bad quality audio samples.

# System status

To indicated the state of the system parameters might be used LCD display. There is available VHDL library to use a 16x2 Alphanumeric display, however need for display may be unnecessary, if there is real-time access into system via UART. At least, 4 LEDs which are available on the CMODS6 module may indicate some generic state such as an error, transmitting, initializing or other useful state.

## DDS parallel out, SPI VCO control (RF output)

The audio samples acquired by the audio input circuitry and modulated as the FM in the FPGA are transferred as the DDS parallel out. The role of the DDS is to create sinus signal with frequency adjustment upon the input audio sample (FM). Therefore, the FPGA's DDS provides samples and clock what is enough drive a parallel-driven DAC. The DAC0 of speed 210MSPS might produce signal of frequency 105MHz, however there is a risk, if the circuitry is not proposed well, that the maximal limit cannot be reached. That's why is not implemented way of the direct single DAC usage to generate FM broadcast, although it is theoretically possible (up to 105MHz, omitting channels 105-108MHz). This straightforward way of FM broadcast is depicted on Figure 6.

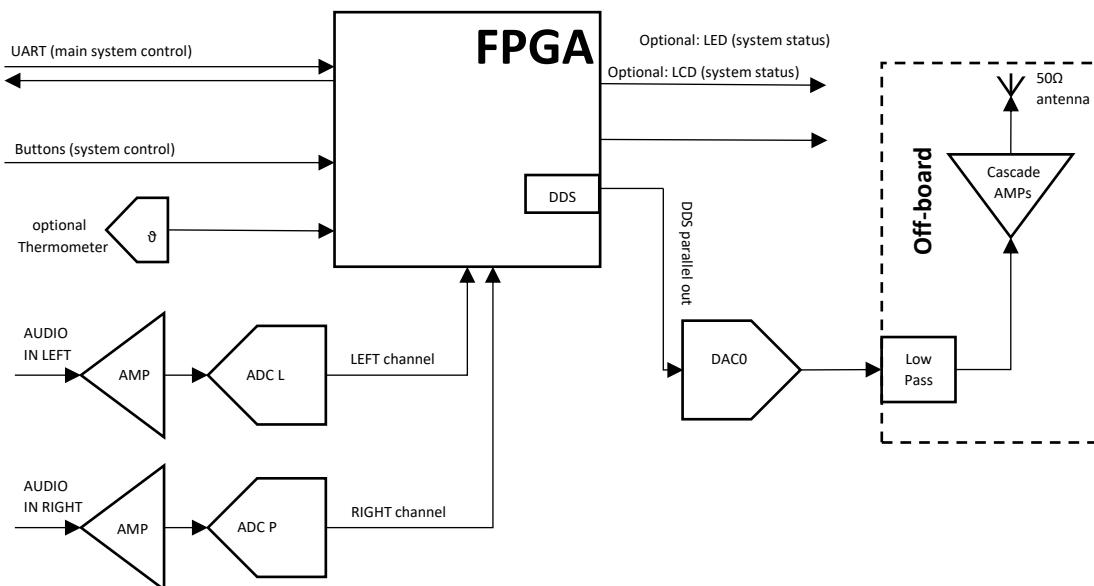


Figure 6 Detailed VHF-Transmitter block diagram – direct method (NOT USED IN THIS DESIGN)

As direct method of FM synthesis was not chosen due to operation of the DAC0 on the limit edge, following text explains approach when two frequencies are merged together in order to reach high frequency output. The approach when carrier is mixed with baseband signal is called heterodyne. Thus, the role of the passive mixer in the proposal is to mix the DAC signal (driven by DDS) with the carrier produced by the VCO. In the easiest case, the signal might be in the baseband (in case of FM sound broadcast 20Hz-20kHz) and is mixed just by adjustable carrier 88-108MHz. Note that the mixer operation in frequency domain may be described as:

$$f_{out} = (f_2 + f_1) + (f_2 - f_1)$$

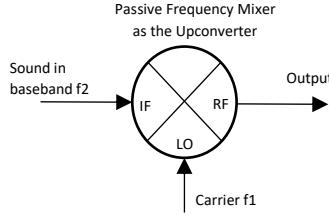


Figure 7 Frequency mixer operation

Normally, only one product of mixing is needed (e.g. only  $f_{LO} + f_{IF}$ ) and rest must be filtered. In case of very small IF frequency would be the RF result two mirrored signals around the LO. This would cause unwanted broadcast in two mirrored channels. Note that except major two frequencies arises also their  $n^{\text{th}}$  combination in the RF output (not expressed in formula above).

However, typical mixer has specified minimal operational frequency, which is the design case 2MHz, what does not allow to use input audio signal in baseband. That's why is the baseband signal already in the frequency level of the inter-frequency. The DAC0 might generate inter-frequency in range 2-60MHz. Note that 2MHz limit is specified by the mixer's  $f_{MIN}$ , meanwhile 60MHz is the maximal possible generated frequency, when used 120MHz clock for the DAC0 and the DDS.

The carrier circuitry path contains VCO, an analog IC which produces HF sinewave. This specific VCO has analog input terminal  $V_{TUNE}$  to adjust the output frequency in range 65-83MHz. The DAC1 is lower data-rate DAC, basically not capable to generate signal way beyond the sound frequency range. Arises an idea to include any FM payload in the carrier (using the DAC1) instead of use the FPGA DDS – DAC0 path.

All in one, except the mixer frequency requirements, there are also power requirements for effective passive mixer operation. That's why is listed amplifier bringing the RF signal (carrier) into level, where the mixer works most efficiently. Still, cost of frequency passive mixing is up to 70% power loss of the input signals. Also, mixer produces not only sum and subtraction of the input signals, but also multiples of these products, so an output bandpass filter is needed (to do not interfere this system by itself as well as the entire ambient environment).

The reason why the bandpass and the back-end amplifier stage are shown as the "Off-board" is, that for other than the FM broadcast range would be the Band-Pass not suitable. Thus, the "Off-board" section shall be replaceable upon the system output requirements.

Finally, the output power should be enough to transmit broadcast within the room, but for longer distances is needed any RF amplifier or their cascade. The antenna as the last chain interface is intended to be small antenna matched to  $50\Omega$  to prevent additional matching.

# Detailed RF-out proposal

This chapter describes the proposed RF circuit in detail, as brief functional description of the design way was already explained in the chapter System Block Proposal. However, at the first is explained theory behind the DDS (Direct Digital Synthesis) which is driving the parallel DAC0 and is responsible for the FM modulation.

Also note that the whole RF part is desired to be in  $50\Omega$  mode, so thickness of all traces connecting the analog RF parts and all the matching between components is used in order to reach this impedance. Impedance mismatch causes signal reflection and so assumes overall power drop-off as well as generating unwanted frequency products.

## DDS (Direct Digital Synthesis)

The DDS may be understood as block providing sinus/cosine and their phases generated by feeding input clock. The DDS might be discrete IC as well as the software block and in case of this design is DDS the Xilinx IP-SoftCore (software block).

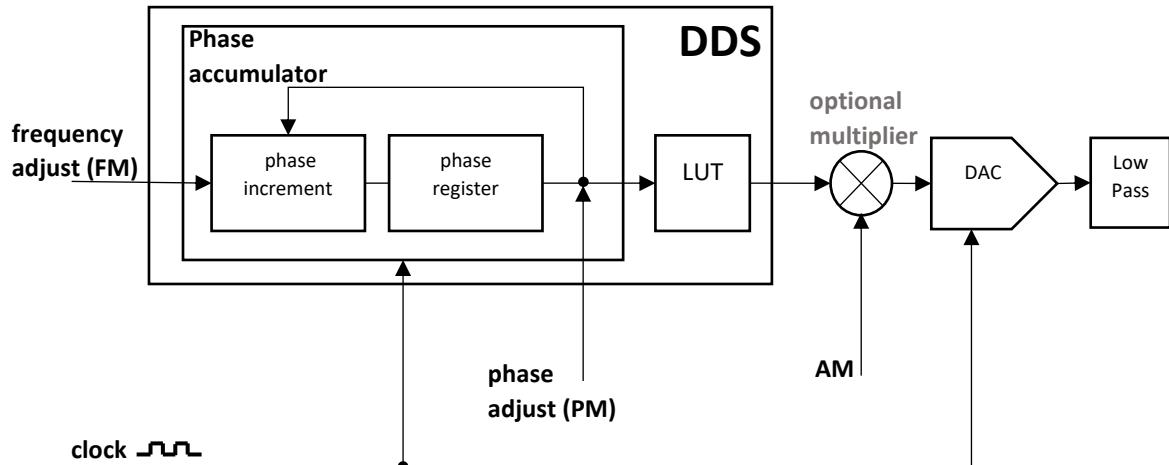


Figure 8 DDS simplified block diagram and usage for FM/PM/AM

### DDS principle

Figure 8 depicts simplified DDS for better explanation. The core of the DDS is the LUT (Look-up Table), what is basically memory containing for instance cosine samples. Note, that only  $\pi/2$  of the cosine is needed to describe the shape across the entire period  $2\pi$ . The LUT is designed to provide samples upon the input address.

The phase accumulator is an incremental logic block, where is gradually incremented phase (address for the LUT to get the sample) and so this block ensures, the output of the DDS is continual wave. Note that the incrementation happens each clock cycle. The phase accumulator is content of the phase registers (the value of the phase in time) and phase increment summing block. The phase increment specifies increments of the phase register and therefore may be understood as the DDS frequency control (bigger phase increment means faster phase rotation what results in higher DDS frequency).

The output of the DDS are digital samples of cosine related to clock cycles. Further utilized DAC needs except the samples also the same clock for wave reconstruction. Note that the wave will contain also other unwanted frequencies which occurred during conversion. Closer is the desired frequency to clock frequency, more secondary products arises. To eliminate secondary frequencies is always used the low-pass filter.

### *DDS as the modulator*

The explanation is enough to embed basic modulations into DDS. Changes of the frequency (phase increment) may be used as the frequency modulation - FM.

The changes of the phase register results in phase adjustment and so may be used as the phase modulation - PM.

If DDS output samples are multiplied by any signal, the result is Amplitude modulation AM (like the DSBSC AM modulation from [Figure 1](#)). Note that by the DSBSC is meant presence of points during the waveform, where the carrier signal modulated almost to zero.

### *Mathematical description (standard mode)*

The output frequency  $f_{OUT}$  of DDS is function of clock frequency  $f_{CLK}$ , phase bit-width  $B_\Theta$ , and phase the increment  $\Delta\Theta$ .

The equation is:

$$f_{OUT} = \frac{f_{CLK} \times \Delta\Theta}{2^{B_\Theta}}$$

to generate certain frequency is needed calculation of the phase increment  $\Delta\Theta$ :

$$\Delta\Theta = \frac{f_{OUT} \times 2^{B_\Theta}}{f_{CLK}}$$

The frequency and its precision is affected by the frequency resolution  $\Delta f$ :

$$\Delta f = \frac{f_{CLK}}{2^{B_\Theta}}$$

### *Example DDS*

As an example, lets calculate DDS parameters for  $f_{OUT} = 21\text{MHz}$ , when:

- system clock  $f_{CLK} = 120\text{MHz}$
- phase width  $B_\Theta = 25$  bits

At the first, calculate the  $\Delta\Theta$ :

$$\Delta\Theta = \frac{21 \times 10^6 \times 2^{25}}{120 \times 10^6} = 5872025.6$$

The phase increment is integer type:

$$\Delta\Theta_{INTEGER} = 5872025$$

Using the rounded  $\Delta\Theta$ , will be generated frequency:

$$f_{OUT} = \frac{120 \times 10^6 \times 5872025}{2^{25}} = 20.999997\text{MHz}$$

It is obvious, that rounding the  $\Delta\Theta$  is causing an  $f_{\text{OUT}}$  error, which is in this case negligible (0.00001%).

$$\Delta f = \frac{120 \times 10^6}{2^{25}} = 3.57 \text{ Hz}$$

### *Phase error of the DDS*

The error caused by the  $\Delta\Theta$  initial rounding is not the only error present in the DDS system. The scope of this document is not to describe fully the DDS block. For this purpose I would rather recommend the document LogiCORE IP DDS Compiler v4.0 [14].

For phase error explanation and correction let's add two another functional blocks into simplified DDS diagram of Figure 8. At the first, the Quantizer between Phase Accumulator and the LUT must be added. Secondary, the Tailor Series Adder must be added at the output of the LUT.

The reason, why is added the Quantizer is, that the depth of the LUT is not infinite. The Quantizer is block, which truncates very precise phase into nearest available sample in the LUT, because phase is often in fractional form, but LUT can be addressed only by integer. Also, vendors tries to shrink LUT as much as possible and typically LUT could be of depth e.g. 4096. This means 4096 addresses, so there are 4096 samples to describe one sine/cosine amplitude period). Truncating the phase causes phase error, because the truncated phase always differs from the real phase. This error is periodic through the one cycle of signal and the error has saw-teeth waveshape. This periodic error results in regular parasitic phase modulation and frequency spurs in the signal spectrum.

There is the technique called „phase dithering“, to reduce phase error. The noise is added to the phase LSB, what results in decreasing the spectral spurs approximately by 12dB. This technique is not very complex as there are several easy ways of noise signal acquisition.

More efficient way of eliminating the phase error is usage of the Taylor series. The Taylor series may describe function as the sum of function derivations at single point and thus simply approximate the processed function. The Taylor series adder adds the correction for otherwise phase errored signal at the output of the DDS's LUT. Basically, the truncated phase by the Quantizer is not just thrown away, but it is forwarded to Taylor Series Calculator, which calculates the signal correction and finally adds to output signal in order to fix it. The Taylor Series technique is more efficient by decreasing spectral spurs up to by 34dB. However, implementation is based on the DSP, so in compare to the phase dithering is more complex and so costs more resources.

## Power supply decoupling

Before any IC usage or active device circuitry is discussed is illustrated typical power supply decoupling circuit of Figure 9. Note that this circuit is used in the entire design several times, especially for digital circuits to reduce interference propagated from analog RF parts.

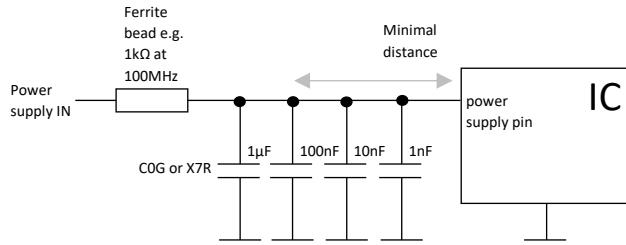


Figure 9 Power supply blocking circuit

The decoupling circuit works as Low-Pass L-C filter, whereas the ferrite bead works as frequency dependent impedance for high frequency. Typically, ferrite bead has specified impedance at 100MHz, so in this case is this parameter  $1\text{k}\Omega$  at 100MHz. Note that the ferrite bead impedances are normally within  $100\text{-}10\text{k}\Omega$ . Ferrite bead must pass DC signals without significant resistance. The cascade of capacitors should be sorted from higher to lower capacities in order to gradually bypass lower up to higher interference frequencies. The capacitors for filtering cannot be of random dielectric, but electrics which ensure “shortcut” for frequency to be filtered. At the best is the COG (NPO) suitable, eventually a bit worse X7R dielectrics, which are often recommended in typical application of any analog design. Should be emphasized that different value capacitors are used, because each value filters certain band of interference better than the other, due to real-physical construction with parasitic R and L.

The COG (NPO) dielectrics have stable capacity across the voltage and temperature. However, the best for RF would be MLCC capacitors (Multi-Layer-Ceramic-Capacitors), which features with minimal parasitic inductance in compare to others. However, do not understand that dielectrics such as discussed are suitable for every applications as for coupling the AC sound signal are not the X7R not well suitable, because features piezoelectric noise.

Further, dielectrics are distinguished in Class 1 up to Class 3, whereas to the Class 1 belongs the best capacitors e.g. of the COG dielectrics. The X7R is considered as the Class 2. The “worst” Class 3 is content out of dielectrics such as Y5V, which would be on the other hand good solution for the audio coupling mentioned upper (features with no parasitic piezo-noise).

# Carrier signal path

Refer to Figure 5, the carrier signal path begins with the digital bus VCO SPI control, going further through the VCO, then is content of the amplifier and the attenuator and finishes in the frequency mixer. Figure 10 describes the carrier circuit in detail. Note that the carrier circuitry is also border of two different grounds, thus the digital ground for DAC1 and the RF ground for the rest (all the analog RF parts).

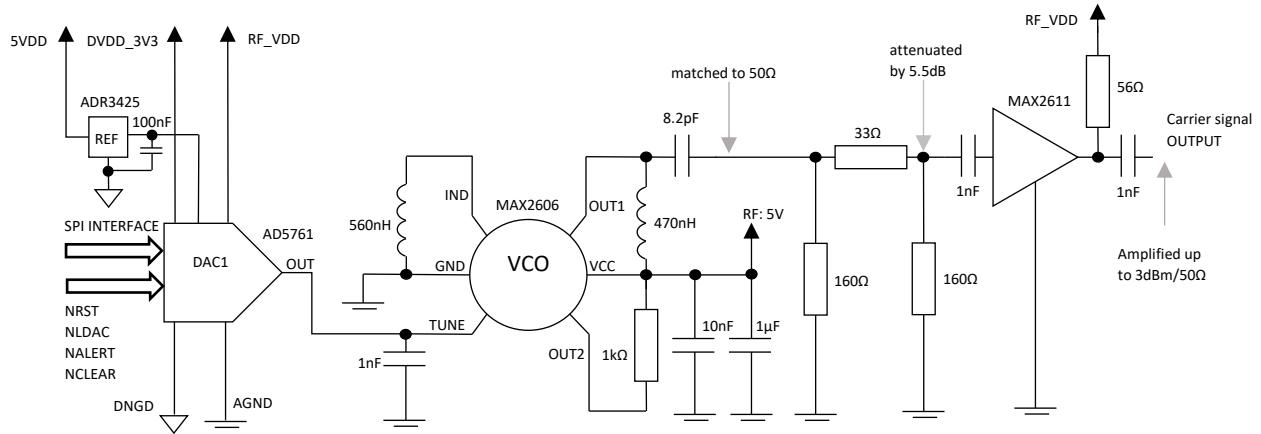


Figure 10 Carrier Circuitry (DAC1, VCO, Matching, Attenuator, Amplifier)

## DAC1 AD5761

The DAC1 is the AD5761 DAC converter controlled via SPI [1]. The AD5761 is designed to be used with 2.5V reference ( $V_{REFIN}$ ) such as the ADR3425 [11]. It should be definitely mentioned that the AD3425 needs for its operation the 100nF capacitor at the output, otherwise may not operate (X7R capacitor or better). Connection of the AD5761 with FPGA and ADR3425 is obvious from Figure 10.

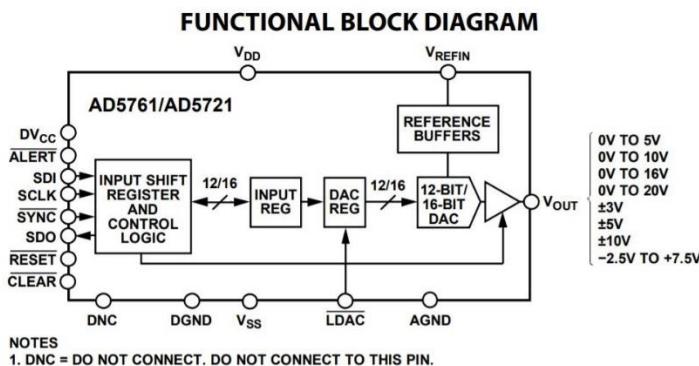


Figure 11 AD5761 Functional Block Diagram [1]

The AD5761 is supplied by two voltages in this design. The digital part is supplied by the  $DVDD\_3V3$  ( $DV_{CC}$ ), the analog part by the 5V RF\_VDD ( $V_{DD}$ ). The reason why is the digital part supplied by 3.3V is the maximal input/output voltage for the FPGA, which cannot handle voltage higher than 3.3V. The analog part is supplied by 5V, because the minimal AD5761 single ended analog supply voltage is 4.75V. The  $V_{SS}$  pin is connected to same point as the AGND determining the DAC as the single-ended supplied (RF GND). Note that both power supply voltages were decoupled using the similar circuit as in Figure 9.

Just remind, that the FPGA interfaces the DAC1 using the standard SPI interface ( $N\_SYNC$  = Chip Select,  $SCLK$ ,  $SDO$ ,  $SDI$ ). The DAC allows maximal SPI clock frequency 50MHz.

Additional digital output/inputs:

- $N\_ALERT$  (DAC output) – indicates special event occurred during the DAC operation
- $N\_RESET$  (DAC input) - resets the DAC into default state
- $N\_CLEAR$  (DAC input) – clears the DAC settings and sets DAC output into pre-set voltage
- $N\_LDAC$  (DAC input) – basically sets the output voltage upon the previously stored value

The AD5761 has timing restriction illustrated in Figure 12, which is obtained from the AD5761 official datasheet [1]. The important timings are:

- The minimal clock period  $t_1$ : 20ns
- The minimal  $N\_SYNC$  falling edge to first  $SCLK$  falling edge time  $t_4$ : 15ns
- The minimal  $SCLK$  falling edge to first  $N\_SYNC$  rising edge time  $t_5$ : 10ns
- The minimal  $N\_SYNC$  rising edge to  $N\_LDAC$  falling edge time  $t_{10}$ : 20ns
- The output settling time after  $N\_LDAC$  falling for 10V output  $t_{12}$ : 7.5 $\mu$ s

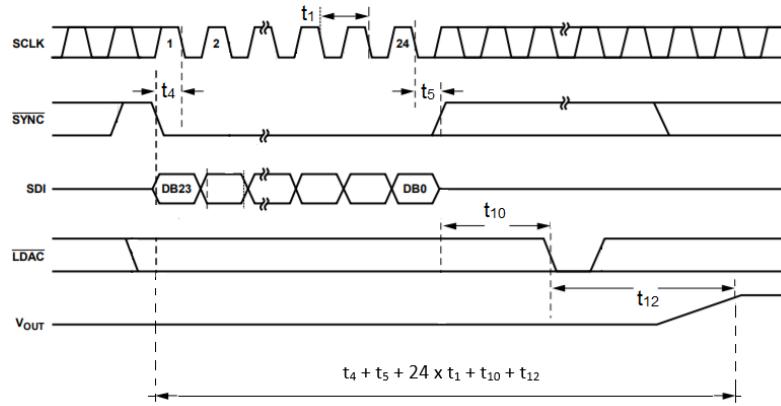


Figure 12 AD5761 Timing write operation [1]

$$t_{total} = t_4 + 24 \times t_1 + t_5 + t_{10} + t_{12}$$

$$t_{total} = 15\text{ns} + 24 \times 20\text{ns} + 10\text{ns} + 20\text{ns} + 7.5\mu\text{s} = 8.025\mu\text{s}$$

$$f_{max} = \frac{1}{t_{total}} = \frac{1}{8.025\mu\text{s}} = 124.6\text{kHz}$$

All in one, the time to set voltage from the beginning of the SPI write transaction up to the DAC output settling is to 8.025μs. The 8.025μs period is equal to frequency 124.6kHz, so higher frequency cannot be by the AD5761 generated and therefore the DAC1 cannot be used as the RF signal generator.

The DAC1 desired operational output voltage range is 0.6-2.4V due to VCO's V<sub>TUNE</sub> range. The DAC1 is 16-bit and it is intended to be set for 5V operation mode (max output voltage 5V).

The voltage resolution for 5V<sub>DD</sub> is

$$AD5761_{RESOLUTION} = \frac{V_{DD}}{2^{n-bit}} = \frac{5}{2^{16}} = 76\mu\text{V}/LSB$$

## VCO MAX2606

As was mentioned upper the VCO is controlled by the analog input interface transferring the input voltage (or current) into the output frequency  $f_{VCO}$ . The chosen VCO is the MAX2606, packaged in the SOT-23-6. The IC needs minimal external parts and it is dedicated be source of low-jitter sine signal (Figure 13).

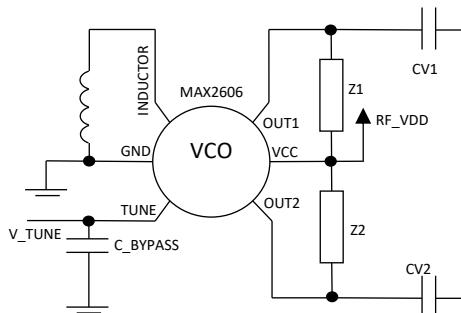


Figure 13 MAX2606 circuit

The output frequency  $f_{VCO}$  is based upon the model of the MAX260x and Inductor value [2]:

- MAX2605 (45 – 75MHz operational range for Inductor 2200nH – 680nH,  $Q_{INDUCTOR} = 35$ )
- MAX2606 (70 – 150MHz operational range for Inductor 820nH – 150nH,  $Q_{INDUCTOR} = 35$ )
- MAX2607 (150 – 300MHz operational range for Inductor 180nH – 39nH,  $Q_{INDUCTOR} = 35$ )
- MAX2608 (300 – 500MHz operational range for Inductor 47nH – 10nH,  $Q_{INDUCTOR} = 40$ )
- MAX2609 (500 – 650MHz operational range for Inductor 15nH – 3.9nH,  $Q_{INDUCTOR} = 40$ )

In fact, the MAX260x is the Colpitts oscillator with adjustable bias voltage  $V_{TUNE}$ . Changing the  $V_{TUNE}$  in range of 0.4V – 2.4V causes frequency adjusting by circa  $\pm 10\%$  (referred to initial frequency set by the Inductor) [2]. Note that the maximal  $V_{TUNE}$  voltage is 5V. Therefore, when the DAC1 (AD5761) operates in 5V output mode, definitely should not damage the VCO.

For the VCO operation is needed a High-Q inductor, so suitable are SMD ceramic inductor such as:

- Coilcraft Chip Inductor 0805HT
- Coilcraft Chip Inductor 0805HP

To bypass the  $V_{TUNE}$  and prevent parasitic frequency drifting (parasitic FM) is needed to use good  $C_{BYPASS}$ , which is stable across the operational voltage and frequency. The datasheet recommends the dielectrics NPO (equal with COG, discussed in the chapter Power Supply Decoupling) [2]. For the MAX2606 is recommended  $C_{BYPASS} \geq 820\text{pF}$ . Just note that datasheet considers the X7R dielectrics as not suitable.

The output stage of this VCO is open-collector current switch, so pull-up impedances and coupling capacitors are needed. For the good power and impedance matching is expected to use pullup impedances  $Z_1$  and  $Z_2$  (inductive or capacitive according to load impedance character). However, for basic operation with no special power demand may be the  $Z_1$  and  $Z_2$  replaced by the conventional  $1\text{k}\Omega$  resistors. Further, usage coil/inductor as the  $Z_1$  and  $Z_2$  must be followed by the well determined capacitor  $C_{V1}$ ,  $C_{V2}$  in order to reach desired impedance matching.

The MAX260x maximal output power is referred as -10dBm for single output, both outputs may provide up to -8dBm [2].

Using Figure 14 was determined Inductor 680nH in order to reach output frequency 75MHz. The desired 75MHz shall be further adjustable by circa  $\pm 10\%$ . and so, the estimated frequency range with usage of the  $V_{TUNE}$  shall be within 65-83MHz.

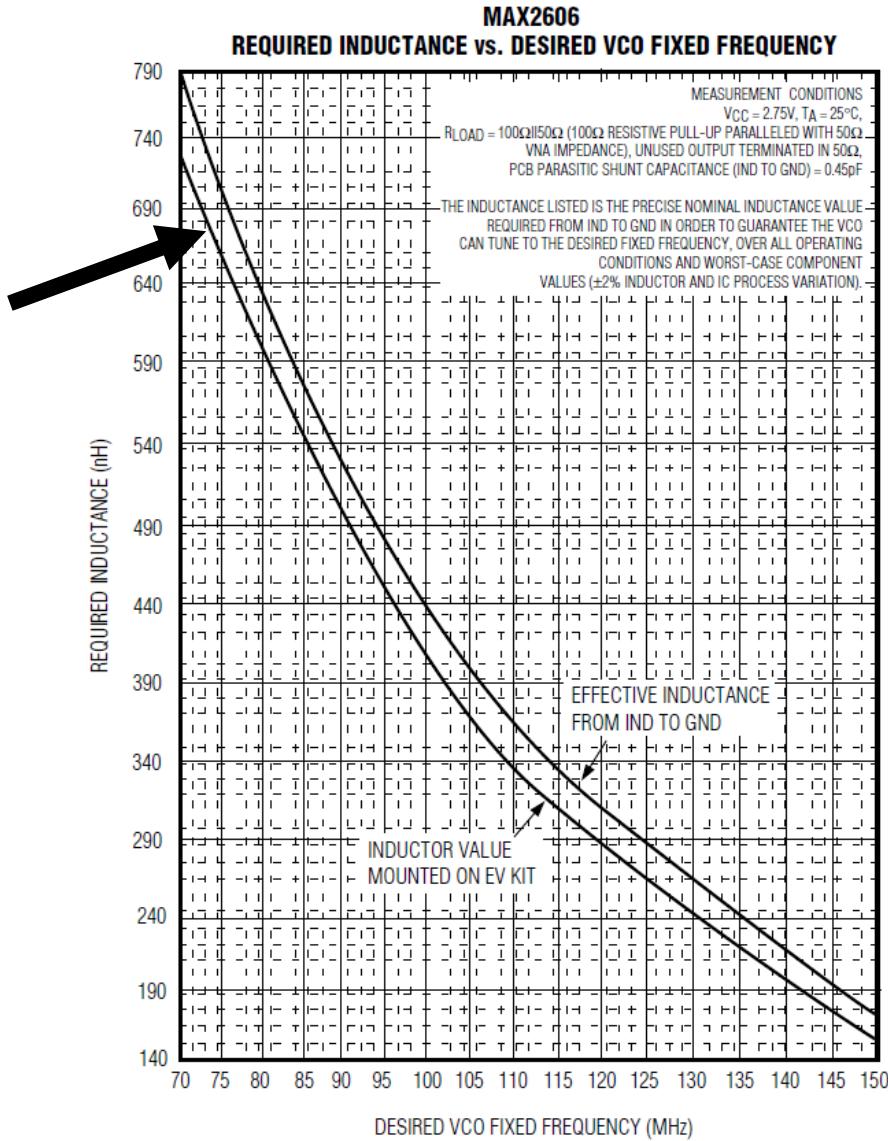


Figure 14 Frequency determining of the MAX2606 [2]

Further, to the output impedance there is the statement [2]:

*As the output stage is essentially a high-speed current switch, traditional linear impedance using techniques with [S] parameters do not apply. To achieve a reactive power match, start with the component values provided in the EV kit, and adjust values experimentally.*

This means, than the best practice is to use parts determined for the MAX2606 EV KIT [3], whereas are empirically set the  $Z_1$ ,  $Z_2$  and  $C_{V1}$ ,  $C_{V2}$  to match the  $50\Omega$  load usage.

For the MAX2606 -  $50\Omega$  matched operation at 122.5MHz were determined:

- $Z_1, Z_2 = 330\text{nH}$
- $C_{V1}, C_{V2} = 4.7\text{pF}$

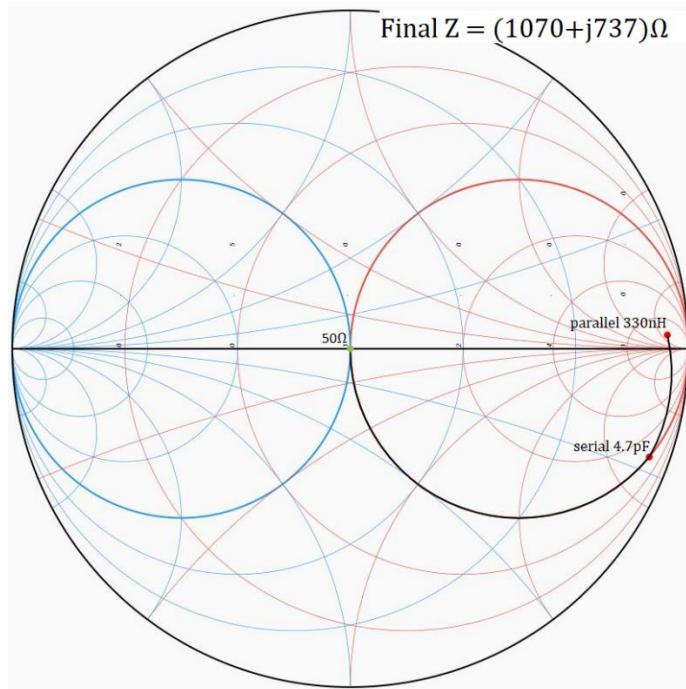


Figure 15 MAX2606 EVKIT Smith-chart matching for 122.5MHz and  $50\Omega$  load

The matching is graphically expressed using the Smith-chart in figure 15. The L-matching circuit of Figure 16 transfers VCO complex output impedance  $Z \approx 1.3\text{k}\Omega$  (illustrated as the  $Z_i$ ) into load impedance  $50\Omega$  for 122.5MHz. Note that the frequency 122.5MHz was found-out inserting the MAX2606 EVKIT Inductor value (290nH) into graph of Figure 14. Just remind that the L-matching is coupled resonance network and so, works as matching only for narrow frequency band.

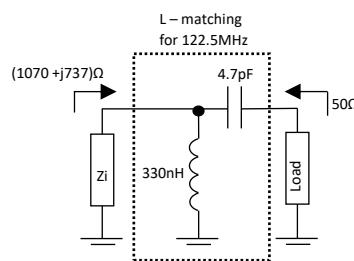


Figure 16 Impedance L-Matching circuit

For the design needs must the MAX2606 operate in different than 122.5MHz range, so also the L-matching network must be tuned accordingly. The MAX2065 EV KIT [3] uses the same network topology for 54MHz operational frequency with different values of inductors and capacitors.

For the MAX2605 -  $50\Omega$  matched operation at 54MHz were determined:

- $Z_1, Z_2 = 680\text{nH}$
- $C_{V1}, C_{V2} = 12\text{pF}$

The average of MAX2606 and MAX2065 matching values are:

- $Z_1, Z_2 = 470\text{nH}$  (nearest available value)
- $C_{V1}, C_{V2} = 8.2\text{pF}$
- Averaged frequency 88MHz

The 470nH coils were used into Smith-chart of Figure 17, however when optimizing the L-Circuit for 75MHz, the 560MHz inductor rather than 470nH was used.

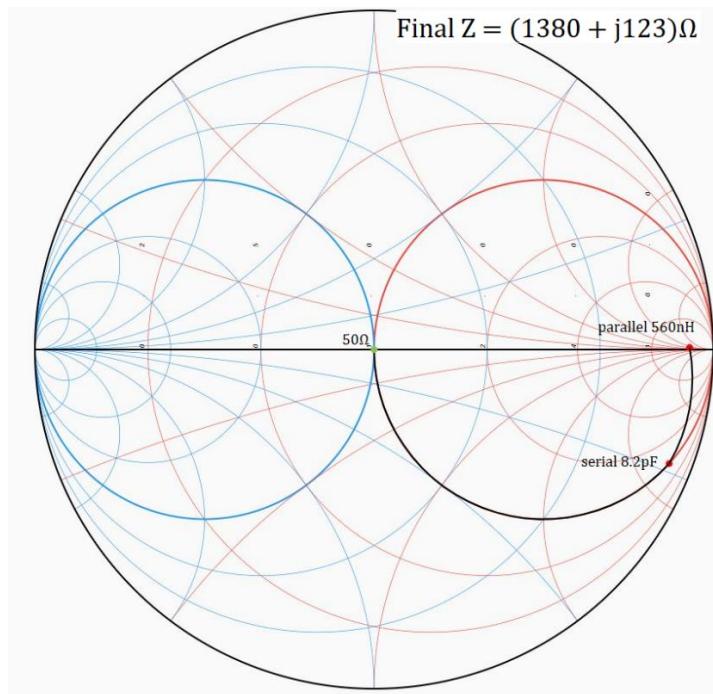


Figure 17 MAX2606 Smith-chart matching for 75MHz and  $50\Omega$  load

The main outcome of the VCO MAX2606 chapter is discrete part selection:

- Inductor =  $680\text{nH}$  (nearest value to set operational frequency 75MHz)
- $C_{\text{BYPASS}} \geq 820\text{pF}$  NPO, so 1000pF COG capacitor chosen
- Matching discrete parts  $C_{\text{SERIAL}} = 8.2\text{pF}$ ,  $L_{\text{PARALLEL}} = 560\text{nH}$  (or 470nH) to reach  $50\Omega$  output matching, when the L-matching circuit of Figure 16 is used.

Together with maximal expected power:

$$P_{VCO\_MAX} = -10\text{dBm}$$

At the end is necessary to mention, that the VCO MAX2606 may operate directly as an analog FM modulator. In this case, appropriate Inductor to set FM broadcast frequency range would be needed. Using Figure 14, the Inductor may be determined as 270-390nH. Then, the  $V_{\text{TUNE}}$  adjusts not only the FM broadcast channel, but also includes the payload analog signal. The character of  $V_{\text{TUNE}}$  for this purpose may be understood as very small AC signal (estimated 15mVpp) with DC offset of 0.4V-2.4V.

## Amplifier MAX2611 and Attenuator

The  $P_{VCO\_MAX} = -10\text{dBm}$  (eventually  $-8\text{dBm}$ ) is not good enough for efficient mixer usage (see in the chapter Passive Frequency Mixer). As the  $-10\text{dBm}$  at  $50\Omega$  is equal to  $200\text{mV}_{PP}$ , and  $-8\text{dBm}$  is equal to  $250\text{mV}_{PP}$  in the best, the LNA amplifier should be used. The middle frequency of amplifier operation is  $75\text{MHz}$  as was determined by the VCO.

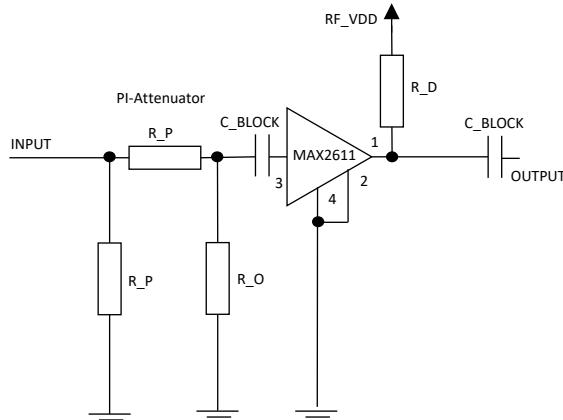


Figure 18 MAX2611 Amplifier circuit with input Attenuator

The MAX2611 is amplifier in SOT-143 package was selected [4]. Note that the SOT-143 is dimensionally similar to SOT-23-6. The IC features with following characteristics:

- OIP3:  $13\text{dBm}$
- NF:  $3.5\text{dB}$  (noise figure)
- Gain:  $18.5\text{dB}$
- OP<sub>1db</sub>:  $2.9\text{dB}$
- Frequency range DC-1GHz
- $50\Omega$  input/output

The scattering parameters for the MAX2611 shows, that for  $100\text{MHz}$  has IC best performance in compare to full frequency range [4]. For lower than  $100\text{MHz}$  may be similar behavior expected.

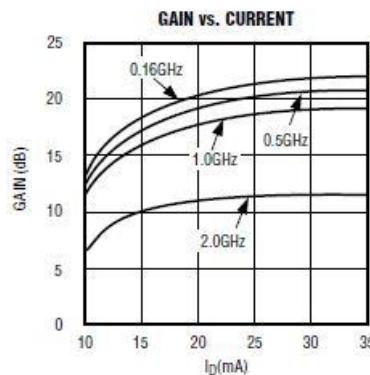


Figure 19 MAX2611 Operational bias current Figure [4]

The Figure 19 shows dependency of the MAX2611 output gain on bias current (current which flows through the pull-up resistor  $R_D$  of Figure 18). The  $I_D = 22\text{mA}$  was chosen as the stable area compromise. There is equation to calculate the  $R_D$  resistor value in datasheet [4], however it is not more than the Kirchhoff law:

$$R_D = \frac{V_{CC} - V_D}{I_D} = \frac{5V - 3.8V}{22\text{mA}} \approx 56\Omega$$

Also, there is empiric equation to specify the minimal  $C_{BLOCK}$  capacitor placed in the output and input of the Amplifier. As the IC may be understood as the common-emitter transistor amplifier, output capacitor is absolutely necessary to block the  $V_{CC}$  and provide only amplified AC signal in the output.

$$C_{BLOCK} = \frac{53000\text{pF}}{f[\text{MHz}]} = \frac{53000\text{pF}}{75} = 706\text{pF}$$

Figure 20 depicts typical input/output features of the RF amplifier. The black curve is the amplifier gain, showing the linear output power  $P_{OUT}$ , for specific range of the input power  $P_{IN}$ . If the  $P_{IN}$  is higher than value specified by point  $IP_{1\text{dB}}$ , the output power further does not increase linearly but stays almost flat. At the  $IP_{1\text{dB}}$  point is the output power compressed by 1dB in compare to expected interpolated curve what is the  $OP_{1\text{dB}}$  point.

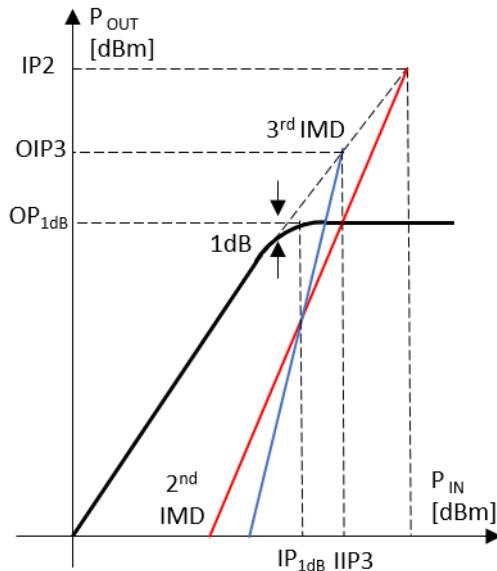


Figure 20 RF Amplifier  $P_{1\text{dB}}$ ,  $OIP3$  illustration

The red and blue curves are signalizing intermodulation distortion (IMD) and both of them are present across the whole operational range of amplifier. However, when an amplifier is used in linear operational point (up to  $OP_{1\text{dB}}$ ) the IMD may be almost negligible. If the input power  $P_{IN}$  is so high, that the  $P_{OUT}$  reaches  $OIP3$ , the output signal is significantly distorted, what is unwanted especially for application with demand of quality amplitude shape.

The well matched VCO may provide up to  $-8\text{dBm}$ , together with the MAX2611 is the carrier signal:

$$P_{CARRIER} = P_{VCO\_MAX} + G_{MAX2611} = -8\text{dBm} + 18\text{dBm} = 10\text{dBm}$$

The value 10dBm is close to the MAX2611 OIP3 +13dBm, so high distortion of the signal is expected. Also, the mixer needs for its operation +3dBm input power. So, the 7dB attenuation of the MAX2611 input signal is needed.

$$P_{CARRIER} = P_{VCO\_MAX} - L_{ATENNUTAOR} + G_{MAX2611} = -8dBm - 7dB - 18dBm = 3dBm$$

By the attenuator is meant a passive 3-resistor circuit with matched input/output to the system impedance ( $50\Omega$  in this case). Figure 18 contains resistive PI-Attenuator (exists also TEE equivalent). Theory behind the resistive attenuators is just the serial/parallel resistor calculation, so only final values for two attenuations are published. It is possible, that the attenuation may be trimmed in order to reach perfect power performance. Note that resistive attenuator is frequency independent circuit.

- PI- $50\Omega$  5.5dB attenuator:  $R_p = 160\Omega$ ,  $R_s = 33\Omega$
- PI- $50\Omega$  7.0dB attenuator:  $R_p = 130\Omega$ ,  $R_s = 130\Omega$

# Modulation signal path

Refer to [Figure 5](#), the FPGA modulation signal path begins with the digital bus DDS parallel out, going further through the fast parallel DAC0, which output is further filtered by a passive filter and this signal finishes in the mixer. Figures 21 and 22 are enough to describe the modulation circuit in detail. Note that the modulation circuitry is also border of three different grounds. At the first, DAC0 is interface between digital and intermediate-analog ground. The intermediate-analog ground is decoupled using a transformer to the final RF ground. Each of the mentioned grounds has its own power supply, however intermediate-analog and RF power supplies (and so grounds) may be coupled. This approach was done, to maximally reduce noise propagated from the RF part into DAC0 and vice versa (when needed).

## DAC0 AD9742

The DAC0 is fast 12-bit parallel TxDAC AD9742 with complementary current output [5]. The DAC was chosen especially for its maximal sample rate up to 210MSPS (capable to generate signal up to 105MHz). Figure 21 depicts its typical application obtained from the datasheet. As any signal DAC needs filter at the output, for sufficiently filtered output was proposed 5<sup>th</sup> order Chebyshev passive Low-Pass filter (Figure 22). The DAC0 output coupling by the 1:1 transformer was also recommended in for such application, where single ended voltage is demanded. For easier soldering, the DAC0 in bigger TSSOP-28 package was chosen (also smaller packages SOIC-28 and LFCSP-32 are available).

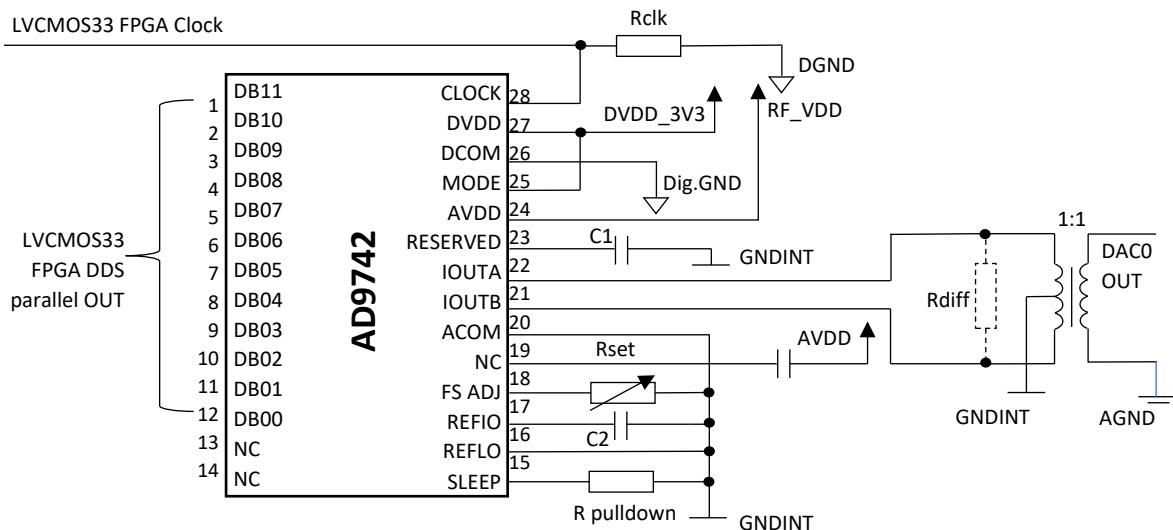


Figure 21 DAC0 AD9742 schematic with transformer at the output

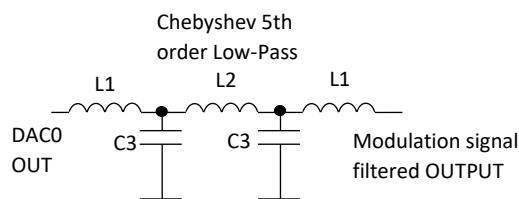


Figure 22 DAC0 Chebyshev 5th order Low-Pass passive filter

### DAC0 digital interface

The AD9742 digital interface supports LVCMS33 single ended levels, however AD9742 in the 32-LFCSP package features with LVDS clock interface (Low Voltage Differential Signal), which is much better for high speed signals. AD9742 in the TSSOP-28 package has only single ended clock, what may cause problem with DAC clock (jitter).

Clock for the parallel DAC is the most important signal and its quality reflects in the output signal. For instance jittered clock may cause unwanted PM and thus even FM modulation.

It is known, that copper signal trace 1cm long brings 0.1ns propagation delay. In worst case, if the digital inputs have mismatched lengths, the DAC can produce incorrect wave due to incorrect input timing. Generally, digital high-speed traces must be as short as possible (and have the same length) and should not be placed next to another signal. Inappropriate placement of high-speed traces next to similar signal may result in crosstalk and jitter. Especially, clock signal must be as least as possible affected by other interference signals. So, during the PCB design is needed, to match DAC digital trace lengths. To provide better clock signal at the AD9742 input is used resistor  $R_{CLK}$ . The  $R_{CLK}$  ensures enough power to be fed from the digital interface (FPGA) and so low-power interference signals should be limited. In other words  $R_{CLK}$  helps to match output of the FPGA with the DAC0.

Traces connecting inputs of the DAC0 to the FPGA must not have corners, but must be well shaped if right-angle curve needed. Any sharp transition on the high-speed trace causes parasitic antenna in the point (reflection and signal transmitting).

The DAC0 may work in straight binary or two's complement data input format. The format selection is done by the pin MODE. Connect to DGND for straight binary, DVDD for two's complement – the DAC is set to operate in two's complement mode.

### DAC0 reference and output power

The AD9742 features with on-chip 1.2V reference, which is enabled when the REFLO is connected to the GND (GNDINT). When the internal 1.2V reference set, loading the FS ADJ pin within allowed range  $2k\Omega - 20k\Omega$  sets the full output current it range  $20mA - 2mA$  (using the  $R_{SET}$ ).

The differential output voltage when both current outputs are in use is described as:

$$V_{DIFFERENTIAL} = \frac{2 \times DAC\ CODE - 4095}{4096} \times \frac{32 \times R_{LOAD}}{R_{SET}} \times R_{REFIO}$$

The maximal  $V_{DIFFERENTIAL}$  voltage, when  $R_{SET} = 2k\Omega$  and DAC CODE full resolution 4095 is:

$$V_{DIFFERENTIAL} = \frac{2 \times 4095 - 4095}{4096} \times \frac{32 \times 50\Omega}{2k\Omega} \times 1.2V = 0.96V$$

The  $V_{DIFFERENTIAL}$  may be understood as the  $V_{PP}$  so the  $V_{RMS}$  value:

$$V_{RMS} = \frac{V_{DIFFERENTIAL}}{2 \times \sqrt{2}} \times \frac{0.96V}{2 \times \sqrt{2}} = 0.354V$$

The  $V_{RMS}$  value is enough to specify maximal AD9742 output power for  $50\Omega$  load:

$$P_{DAC0[dBm]} = 10\log(P_{mW}) = 10\log\left(\frac{V_{RMS}^2}{R_{LOAD}} \times 1000\right) = 10\log\left(\frac{0.354^2}{50} \times 1000\right) = 4dBm$$

It is important to emphasize, that the power  $P_{\text{DAC0[dBm]}}$  is power calculated according to the maximal output amplitude with no regards to conversion noise and high frequency products.

The transformer output coupling is justified by better AC performance, lower signal distortion and noise suppression. The transformer coupling works well up to output voltage  $\pm 0.5V$  ( $1V_{\text{pp}}$ ), so previously calculated values meets this limit [5].

As the 1:1 Transformer was selected Coilcraft WBC-1TL [6], with 0.6dB insertion loss and 0.25MHz - 750MHz bandwidth. The theoretical maximal output of the DAC1 together with 1:1 Transformer is:

$$P_{\text{DAC[dBm]}} - L_{\text{TRANSFORMER}} = 4 - 0.6 = 3.4 \text{ dBm}$$

The role of the optional  $R_{\text{DIFF}}$  is to compensate difference between system and load impedance.

### *DAC0 workaround*

To finalize Figure 21 explanation must be discussed:

- RESERVED – shall be connected to AGND via  $0.1\mu\text{F}$  capacitor
- NOT CONNECTED – shall be connected to AVDD via  $0.1\mu\text{F}$  capacitor
- REFIO – reference input/output should be decoupled using  $0.1\mu\text{F}$  capacitor
- SLEEP – sets SLEEP mode, connecting via resistor AGND disables functionality

The AVDD and DVDD power supply shall be decoupled in the same way as was described in the chapter Power Supply Decoupling.

The DAC desired generated frequency is within values 5-40MHz in order to after summing with carrier signal, which was proposed to be in range 65-83MHz, reach FM broadcast frequency range 88-108MHz.

Partial overlap of DAC1 frequency range and VCO frequency range shall give more flexibility to experiment and find right DAC1 and VCO settings, in order to produce good output signal.

## Chebyshev Low-Pass filter

For any usage of DAC is needed output signal reconstruction filter. Without filter, clock propagated product as well as other unwanted frequencies would be present in the output signal. The Chebyshev filter belongs to family of standardized filters (Butterworth, Elliptic, Bessel etc.). The approach to propose the filter is to set the filter order (higher order, better filtering) and find filter coefficients to determine L and C parts for the desired cut-off frequency. Filter from Figure 23 was designed using online LC Filter Design Tool for cut-off frequency 40MHz (50Ω).

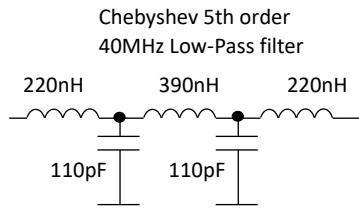


Figure 23 Chebyshev 40MHz/50Ω 5order Low-Pass filter

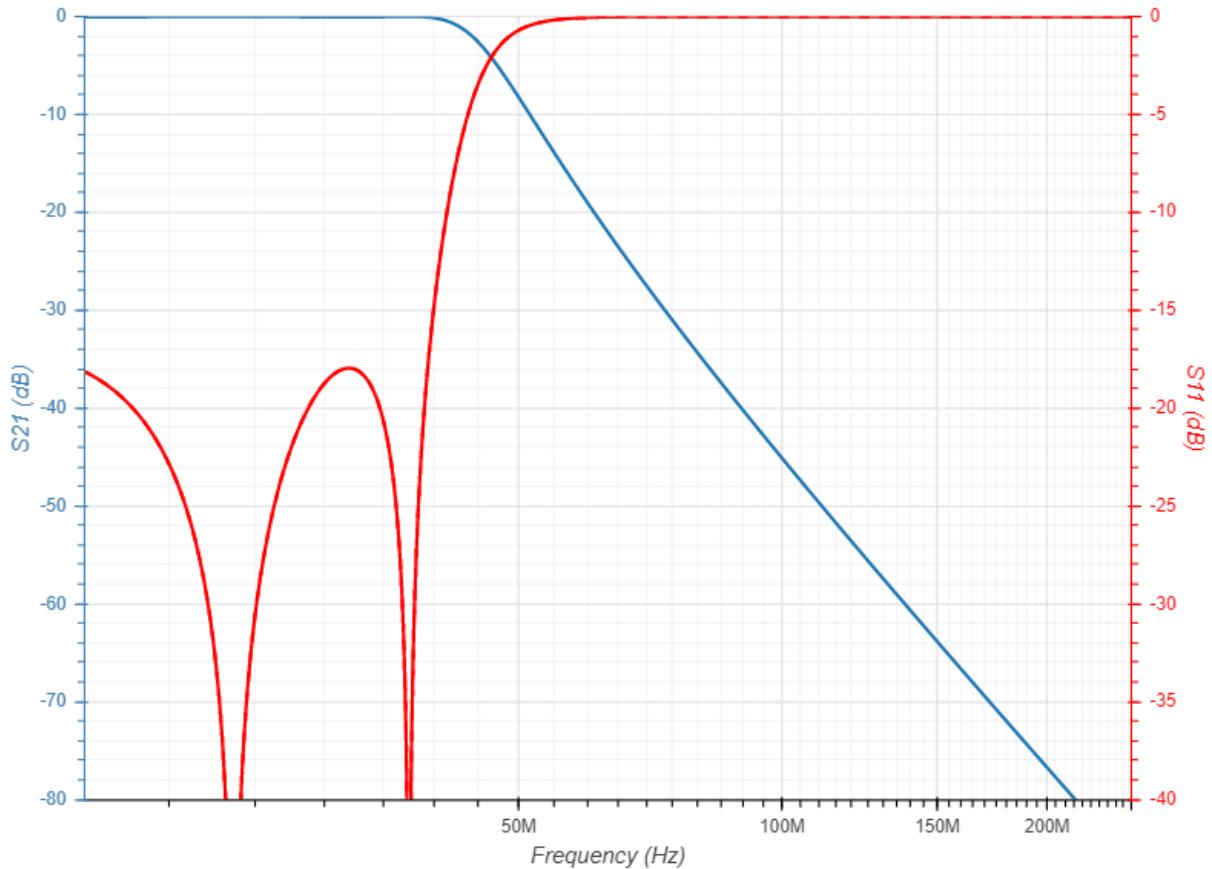


Figure 24 Chebyshev 40MHz 5order Low-Pass filter characteristics

# Passive Frequency Mixer

The role of the Passive Frequency Mixer was discussed already in the several chapters. Expected operation was explained in the System block proposal, section DDS parallel out. Also, the output frequency equation for mixer is in the chapters Carrier signal as well as the Modulation signal path. Mixer operates as frequency signal adder, whereas baseband signal must be summed with carrier signal.

## Passive Ring-Diode Mixer

The ADE-1L+ was selected as the mixer for this design [7]. At the first, principle of operation of a double-balanced diode-ring mixer is discussed. The mixer is designed for  $50\Omega$  operation.

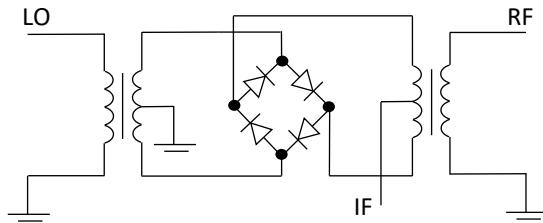


Figure 25 Diode-Ring Mixer internal schematic

General mixer terminals:

- LO (Local Oscillator) – always works as input, LO signal is added or subtracted from second input signal (RF or IF). For balanced diode-ring mixer, LO signal determines mixer output power.
- RF (High frequency input/output) – works as output for upconverter, but as input in case of downconverter.
- IF (Intermediate-frequency input/output) – works as input for upconverter, but as output for downconverter.

Remind the mixer mathematical expression for frequency mixer as upconverter is:

$$f_{RF} = (f_{LO} + f_{IF}) + (f_{LO} - f_{IF})$$

Meanwhile, for downconverter operation is:

$$f_{IF} = |f_{LO} - f_{RF}|$$

Always, only one product of mixing operation is needed:

- Sum of the signals for upconverter application
- Difference of the signal for downconverter application

Figure 25 illustrates internal schematics of a double balanced mixer. Basically, this mixer is content of a diode-ring and two transformers (baluns) with center tap. Arises an idea, to create mixer from discrete parts, but self-made mixer is not easily feasible, as mixer is an RF part and needs several internal matching and optimization.

Double-balance means, LO and RF inputs work in differential mode and their interferences are at output reduced. Single-balanced mixer have either LO or RF at output suppressed but not both together. Zero-balanced mixer have LO and RF signal propagated to the output.

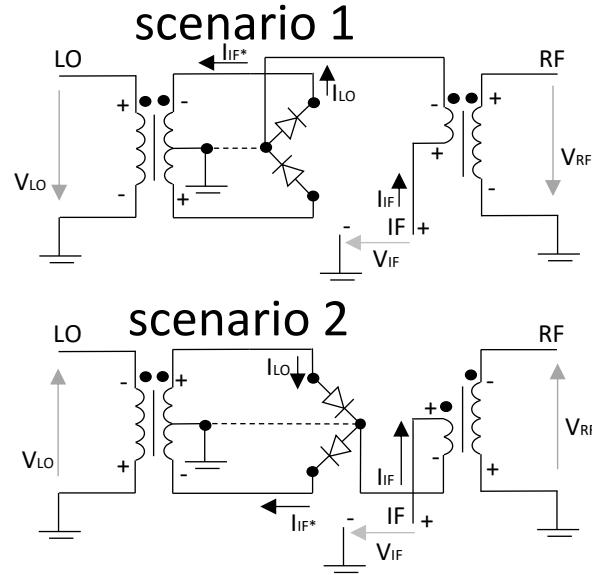


Figure 26 Double-balanced diode-ring mixer principle (upconverter)

Figure 26 depicts two main scenarios for explaining principle of operation. Both scenarios are based on figure 25. For both, parts which does not participate in operation cycle are omitted.

At the first scenario, the LO signal opens the left arm of the diode ring and so, current  $I_{LO}$  flows through those diodes. Further, polarity of the IF determines direction of the current  $I_{IF}$ , which flows towards the node, where are the diodes connected. The upper diode is the only possible way for the  $I_{IF^*}$  to flow. At the end, the  $I_{IF^*}$  flows to the center tap and further to the ground. Thus, whole describe path from the diodes node may be understood as virtual ground for the IF signal (dash line). The LO polarity determined polarity of the RF output, because of the current path selection. The right arm of diodes is not depicted, because works as negligible High-Z path (opened). Also, the bottom part of the right balun winding acts for the scenario 1 as disconnected. In this case, through the upper diode flows current  $I_{LO} + I_{IF}$ , meanwhile through the bottom only  $I_{LO}$ .

Other way around, the second scenario has reversed polarity of LO, thus the right arm of diode-ring is opened for the current  $I_{IF}$ . Further, the  $I_{IF}$  must flow through the bottom diode as the upper is reversed towards the left balun center tap (ground). This causes selection of the current path, that other part of right balun winding is used and so, RF signal polarity is reversed in compare to scenario 1.

It is obvious that circuit works only, when the LO and IF are alternating, otherwise balun transformer does not work . Alternating the LO and IF signals causes commutation in diode-ring and so, frequency upconverting. To be precise, there are another two scenarios of IF polarities, but they may be easily think-out when applied the two scenarios already disused.

## ADE-1L+

The ADE-1L+ is mixer based on principle described upper, the main characteristic are [7]:

- LO power level +3dBm
- Frequency range 2-500MHz
- Maximal RF Power 50mW (+17dBm when mixer works as downconverter)
- Maximal IF Current 40mA (+19dBm at 50Ω)
- Conversion loss 5.2dB

The LO power level was referred, because at this level operates the mixer with best power performance in compare to IMD products at the output. So, operation at +3dBm LO (carrier) is desired.

The VHF-Transmitter design meets frequency range 2-500MHz because:

1. carrier signal path frequency range 65-83MHz
2. modulation signal path frequency range 5-40MHz

To illustrate frequency operating range of the mixer in this design, use formula for upconverter:

- $f_{CARRIER} = 70\text{MHz}$
- $f_{MODULATION} = 21\text{MHz}$

$$f_{OUT1} = f_{CARRIER} - f_{MODULATION} = 70\text{MHz} + 21\text{MHz} = 91\text{MHz}$$

$$f_{OUT2} = f_{CARRIER} - f_{MODULATION} = 70\text{MHz} - 21\text{MHz} = 49\text{MHz}$$

Note that the  $f_{OUT2}$  is unwanted secondary product and therefore must be either Low-Pass, or more typically Bandpass filter used.

The maximal RF power limit may be in case of upconverter not taken in account, because no power will be to the RF terminal attached.

The Maximal IF current (Power 19dBm) will also not be exceeded, as the DAC0 circuit may provide maximally  $1V_{PP}$  signal (4dBm), thus 10mA peak current for  $50\Omega$  load.

Output power after mixing may be estimated using:

1. Carrier signal path maximal power 3dBm
2. Modulation signal path maximal power 4dBm
3. Mixer conversion loss 5.2dB

$$P_{MIXER\_SUM} = P_{CARRIER} + P_{MODULATION} + L_{CONVERSION} = 3\text{dBm} + 4\text{dBm} - 5.2\text{dB} = 1.8\text{dBm}$$

However, the  $P_{MIXER\_SUM}$  cannot be understand as power of desired signal within range 88-108MHz, as the  $P_{MIXER\_SUM}$  value is sum of two produced signals  $P_{f1} + P_{f2}$ . For sure, any additional not yet discussed losses will occur in the carrier signal path as well as in modulation signal path, so real output signal may be expected of lower level. Also, real mixer will not produce only the frequencies listed upper, but also their combination. Practically, when is added 1dBm loss to each part of the Modulation and Carrier path, output signal level shall be estimated as:

$$P_{MIXER\_fout1} \approx -5\text{dBm}$$

# Off-board

The carrier signal path summed with the modulation signal path by the mixer provides sufficient output for the broadcast + unwanted product generated during signal mixing. So, not only two frequency products are at the output expected (see Passive Frequency Mixer chapter). To suppress other than needed frequency product, Bandpass filter is needed. Further, expected output signal should be below 0dBm level, according to the calculation from the mixer's chapter. Thus, usage of back-end amplifier (or amplifying cascade) is justified. However, output power of the mixer is sufficient for experimental broadcast, so output filter and optional amplifiers will be created as an off-board module. Also, certain Band-Pass filter allows operation for narrow frequency range.

## Bandpass filter

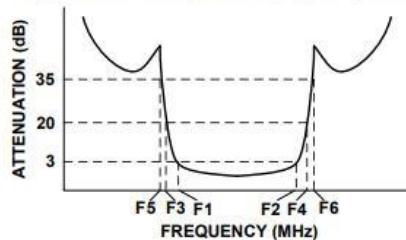
As the filter was selected passive lumped LC RBP-98+ [8]. This filter has following characteristics and it is dedicated for usage in  $50\Omega$  system.

- Lower cut-off frequency 75MHz
- Upper cut-off frequency 131 MHz
- Maximal input power 0.5W (+27dBm at  $50\Omega$ )
- Insertion loss in pass band 2dB

**Bandpass Filter Electrical Specifications ( $T_{AMB} = 25^\circ C$ )**

CENTER FREQ. (MHz)	PASSBAND (MHz) (Loss < 3dB) F1 - F2	STOPBANDS (MHz)				VSWR (:1)	
		Loss > 20dB F3 F4		Loss > 35dB F5 F6		Passband Max.	Stopband Typ.
103	75 - 131	55	170	45	210 - 2000	1.7	18

**Typical Frequency Response**



**Functional Schematic**

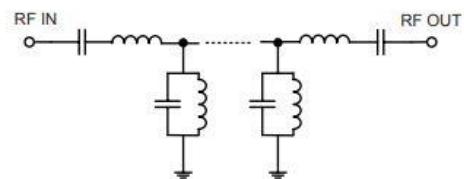


Figure 27 RBP-98+ characteristic [8]

Finally, filtered signal shall be within 75-131MHz and side bands shall be suppressed by 35dBm. If output of mixer is considered in level -5dBm, following calculation for output power and suppressed frequency may be applicable:

$$P_{BANDPASS} = P_{MIXER} - L_{BANDPASS} = -5dBm - 2dB = -7dBm$$

$$P_{BANDSTOP} = P_{MIXER} - L_{BANDSTOP} = -5dBm - 35dB = -40dBm$$

## Amplifier THS9001

Similarly, as the amplifier MAX2611 and the attenuator was used to increase the carrier signal strength for correct mixing, a back-end amplifier before the antenna may be demanded. Note that usage of the additional amplifier like is now described, may exceed allowed transmitted power and interfere other public/private broadcasting and so may be punished by law.

Usage of the THS9001 was chosen rather reuse of described MAX2611, because it is dedicated for higher output power [9]. THS9001 is manufactured in package SOT-23-6 (as well as the MAX2606 VCO). To understand meaning of following characteristic, see Figure 20.

- OIP3: 36dBm
- NF: 4.5dB (noise figure)
- Gain: 15dB
- OP<sub>1dB</sub>: 20dB
- Frequency range 50-750MHz

Because of the THS9001 high maximal output power is possible their cascade. Datasheet recommends following values of discrete parts for optimal performance as trade-off between current consumption and linearity and broadband 15dB gain within range 50 to 325MHz.

- R<sub>(BIAS)</sub> 237Ω
- L<sub>(COL)</sub> 470nH
- Not critical C<sub>(BYPASS)</sub> 100nF (X7R)
- Not critical C<sub>IN</sub>, C<sub>OUT</sub> 1nF (COG)
- 5V power supply

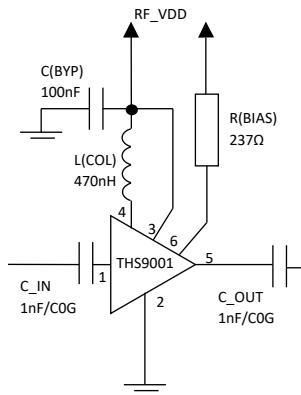


Figure 28 THS9001 amplifier typical circuit

Usage of this amplifier directly at the mixer output, after bandpass filtering, will results maximally in power level:

$$P_{THS9001} = P_{BANDPASS} + G_{THS9001} = -7dBm + 15dB = +8dBm$$

## Cascaded amplifier

As was discussed in the chapter Amplifier THS9001, utilizing the back-end amplifier may bring system into +8dBm power level. By 5V supplying and rail-to-rail operation, the amplifier reaches 5V<sub>PP</sub> output level and thus, maximal theoretical output power for 50Ω is:

$$P_{5V\_50\Omega} = \frac{5V^2}{(2\sqrt{2})^2 \times 50\Omega} = \frac{1.77V_{RMS}^2}{50\Omega} = +18dBm$$

Therefore, cascade of two amplifiers is justified in order to squeeze-out maximal power out of 5V supply. In other words, in compare to single THS9001, another 10dBm may be still provided. The scope of the work is testing both possibilities and privileging the better.

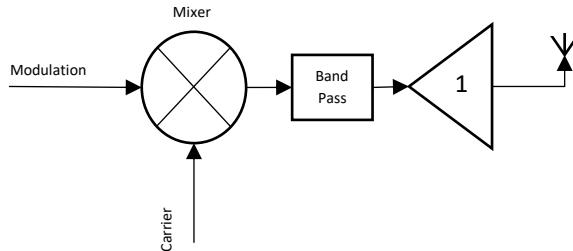


Figure 29 Single amplifier

### Single MAX2611

The first option, is single amplifier usage of Figure 29. As both the THS9001 and the MAX2611 amplifiers were described, also both may be used together.

The signal available to be fed into 50Ω antenna in case of the single MAX2611:

$$P_{ANT\_IN} = P_{MIXER\_REAL} - L_{BANDPASS} + G_{THS9001} = -5dBm - 2dB + 18dB = +11dBm$$

The output power +11dBm for the MAX2611 is too high compare to limits:

- OP<sub>1dB</sub> = 2.9dBm
- OIP3 = 13dBm

So, final output signal will be highly distorted by IMD3 because of saturation and thus, this is not the best approach

## Single THS9001

Using the THS9001 as the amplifier in Figure 29 will result in following power for 50Ω antenna:

$$P_{ANT\_IN} = P_{MIXER\_REAL} - L_{BANDPASS} + G_{THS9001} = -5dBm - 2dB + 15dB = +8dBm$$

The output power +8dBm fits into linear operational range for the THS9001:

- OP<sub>1dB</sub> = 20dBm
- OIP3 = 36dBm

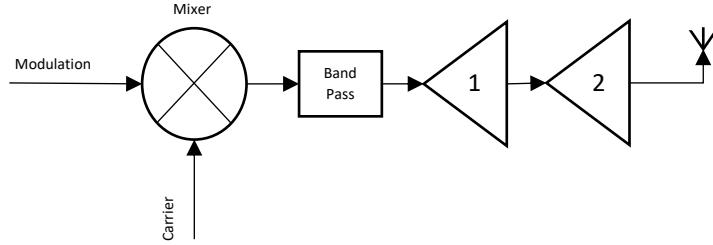


Figure 30 Cascaded amplifiers

## Cascaded MAX2611 + THS9001

When used topology of the MAX2611 + THS9001, output power for 50Ω antenna is calculated as:

$$\begin{aligned} P_{ANT\_IN} &= P_{MIXER\_REAL} - L_{BANDPASS} + G_{MAX2611} + G_{THS9001} = \\ &-5dBm - 2dB + 18dB + 15dB = +26dBm \end{aligned}$$

This output power will be as saturated and distorted as discussed in the Single MAX2611 case. Also, output level +26dBm is not reachable for 5V/50Ω system, as the maximal possible level is +18dBm. To meet maximal system output power +18dBm is for the cascade an 8dB attenuator needed. To prevent distortion of the first block (MAX2611), the best position of the attenuator is before this block.

Output power will result in:

$$\begin{aligned} P_{ANT\_IN} &= P_{MIXER\_REAL} - L_{BANDPASS} - L_{ATTENUATOR} + P_{MAX2611} + P_{THS9001} = \\ &-5dBm - 2dB - 8dB + 18dB + 15dB = +18dBm \end{aligned}$$

The noise figure added by the cascade is determined using the Friis formula:

$$\begin{aligned} F_{CASCADE} &= F_{BP} + \frac{F_{ATT} - 1}{G_{ATT}} + \frac{F_{MAX2611} - 1}{G_{BP} \times G_{ATT}} + \frac{F_{THS9001} - 1}{G_{BP} \times G_{ATT} \times G_{MAX2611}} = \\ 1.585 &+ \frac{6.310 - 1}{0.631} + \frac{2.239 - 1}{0.631 \times 0.158} + \frac{2.512 - 1}{0.631 \times 0.158 \times 70.795} = 22.641 \end{aligned}$$

$$NF_{CASCADE} = 10 \times \log(F_{BP}) = 10 \times \log(22.641) = 13.55dB$$

### Cascaded THS9001 + THS9001

When used topology of the THS9001 + THS9001, output power for 50Ω antenna is calculated as:

$$P_{ANT\_IN} = P_{MIXER\_REAL} - L_{BANDPASS} + G_{THS9001} + G_{THS9001} = \\ -5dBm - 2dB + 15dB + 15dB = +23dBm$$

The output level +26dBm is not reachable for 5V/50Ω system, as the maximal possible level is +18dBm. To meet maximal system output power +18dBm is for the cascade an 5dB attenuator needed. In compare to the MAX2611 + THS9001 case, both amplifiers are used in linear operational range.

Output power will result in:

$$P_{ANT\_IN} = P_{MIXER\_REAL} - L_{BANDPASS} - L_{ATTENUATOR} + G_{THS9001} + G_{THS9001} = \\ -5dBm - 2dB - 5dB + 18dB + 15dB = +18dBm$$

The noise figure added by the cascade is:

$$F_{CASCADE} = F_{BP} + \frac{F_{ATT} - 1}{G_{ATT}} + \frac{F_{THS9001} - 1}{G_{BP} \times G_{ATT}} + \frac{F_{THS9001} - 1}{G_{BP} \times G_{ATT} \times G_{THS9001}} = \\ 1.585 + \frac{6.310 - 1}{0.631} + \frac{2.512 - 1}{0.631 \times 0.158} + \frac{2.512 - 1}{0.631 \times 0.158 \times 35.481} = 25.6$$

$$NF_{CASCADE} = 10 \times \log(F_{BP}) = 10 \times \log(22.641) = 14.1dB$$

## Antenna

As the antenna, was selected the SMD antenna FR01-B3-W-0-055 (NN01-055) [10]. This antenna is basically multi-layer PCB with tuned traces to reach required wavelength. Unfortunately during the project development, both FR01-B3-W-0-055, NN01-055 antennas became obsolete.

The antenna features with following characteristics:

- Frequency range 78-108 MHz
- Gain 2dBi
- Impedance  $50\Omega$
- Length 32mm
- Width 11mm
- Height 1.6mm

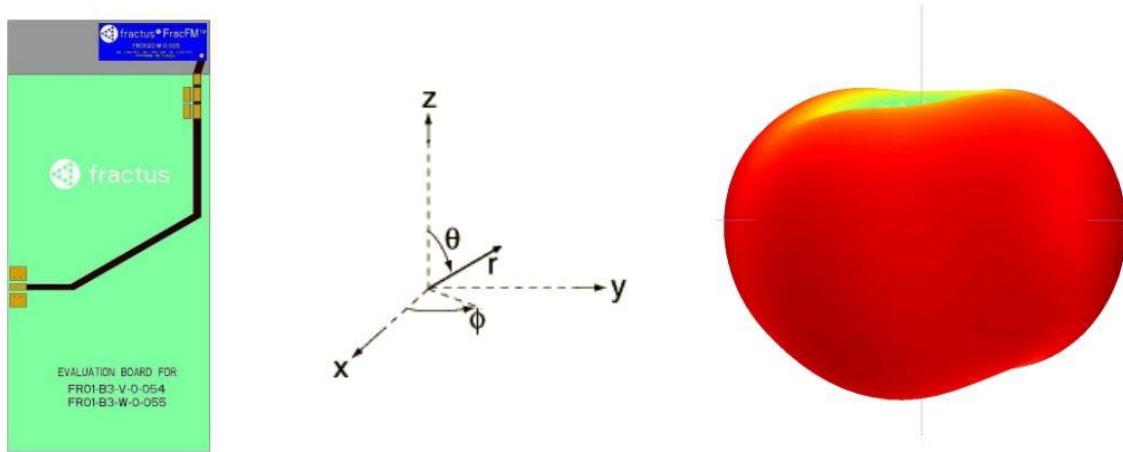


Figure 31 FR01-B3-W-0-055 module and radiation pattern [10]

The antenna is intended to be placed on the 2 - layer PCB, with sufficient ground plane working as the antenna ground. Figure 31 depicts radiation and typical PCB appearance.

The antenna as the part as only single terminal FEED, where the  $P_{ANT\_IN}$  should be fed. Regards to size of the antenna module, the PCB should be split into ground plane (green) and antenna part (gray) [10]. Note that the antenna part I meant as no - copper area.

The green rectangle area (copper ground) dimensions are:

- Height 112mm
- Width 60mm

The gray area (no-copper zone) dimensions are:

- Height 10mm
- Width 60mm

Note that the antenna shall have  $50\Omega$  microstrip or coplanar waveguide, otherwise additive matching on the antenna input. Also other than mentioned antenna may be used, but just ensure  $50\Omega$  matching.

# Detailed Audio-in proposal

Refer to the chapter System proposal section Audio input, an amplifier for audio input is needed. As one of the system requirement is stereo broadcast, two amplifier stages for each channel shall be utilized. Then, amplified signal might be sampled by conventional ADC operating within 0 to rail voltage 3.3V.

## Audio offset pre-amplifier LMV358

The first reason why an amplifier is used, the audio signal from devices such as PC or mobile phone does not have enough high voltage. For the iPhone XR is output voltage  $0.4V_{PP}$  at  $50\Omega$  load, when max volume playing 1kHz tone. This voltage could be sampled, however noise impact and minimal operational range of ADC would affect the quality of the digital processed signal. To reduce noise is better to run maximal voltage into the VHF-Transmitter Audio in pre-amplifier and amplify the signal as least as possible to reach 3.3V resolution. Anyway, amplifying the audio input to use full ADC resolution is justified. Also, each measurement device such as ADC does conversion with smaller error more the measured value is close maximal range.

Audio signal is an AC signal within 20-20kHz. But AC signal cannot be by a conventional ADC converted, because typically ADCs input voltage must be within 0 to rail, so DC offset must be into the AC audio signal added.

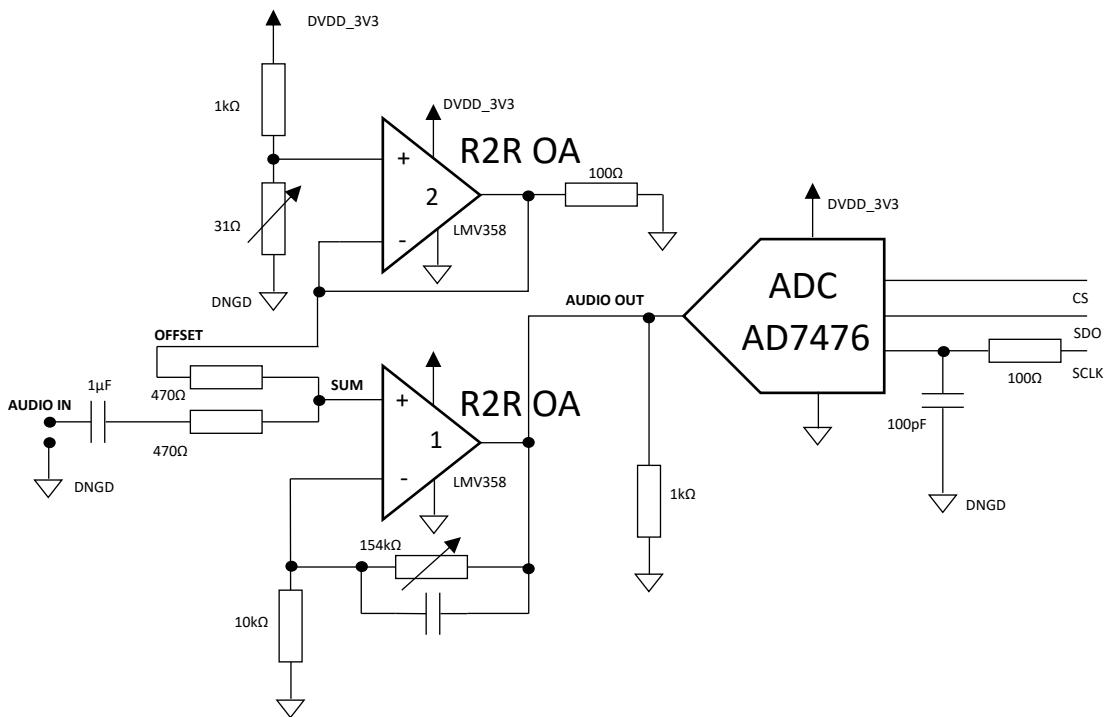


Figure 32 Audio-input circuitry for single channel

Figure 32 depicts the entire audio circuit including discrete parts selection. Basically, circuitry is content of two amplifiers and an ADC. The 1MHz LMV358 R2R OA (rail-to-rail operational amplifier) is used, because operation up to power supply rails is needed (usual amplifier cannot reach output voltages close to rails) [12]. The LMV358 in SOIC-8 disposes with two OAs in the package. Note that R2R OA typically features with lower maximal frequency than usual amplifier, however for AUDIO operation is the bandwidth sufficient. The small ADC is 12-bit converter with SPI digital output.

The audio circuit of Figure 32 is based on the non-inverting amplifier 1 and offset follower 2. The non-inverting amplifier has input signal represented as the SUM signal of the OFFSET voltage and AUDIO IN signal.

By simulating the circuit, optimal operational point for input:

$$V_{AUDIO\_IN} = 0.4V_{PP}$$

Is when the SUM signal is:

$$V_{SUM} = 0.2V_{PP}$$

Which is further amplified by non-inverting topology of gain:

$$G_{NON-INVERTING} = \frac{R_f}{R_g} + 1 = \frac{154k\Omega}{10k\Omega} + 1 = 16.4$$

What may result in ideal case in output voltage:

$$V_{AUDIO\_OUT} = V_{SUM} \times 15.4 = 0.2 \times 16.4 = 3.28V$$

However, output swing of the LMV358 may decrease the final  $V_{AUDIO\_OUT}$ :

- High level:  $VCC - 10mV$
- Low level:  $60mV$

The  $V_{SUM}$  signal  $0.2V_{PP}$  is created out of:

- $V_{AUDIO\_IN} = 0.4V_{PP}$
- $V_{OFFSET} = 0.1V$

Which are summed together by branches with:

- $V_{AUDIO\_IN}$ :  $470\Omega + 1\mu F$
- $V_{OFFSET}$ :  $470\Omega$

Note that function of the  $1\mu F$  capacitor is to block DC signals flowing within nodes AUDIO IN and OFFSET. The capacitor also balances branches, thus just the same weight average of both branches cannot be applicable as the formula for the  $V_{SUM}$  signal. If needed to mathematically determine the  $V_{SUM}$  voltage, the  $470\Omega$  input resistors could be replaced by values e.g.  $100k\Omega$  and thus, effect of the  $1\mu F$  capacitor would be negligible.

Both amplifiers are loaded by  $1k\Omega$  to ensure sufficient load at the outputs.

Also, the calculated values of resistors for the voltage divider ( $V_{OFFSET}$ ) as well as values for the weighted sum amplifier might be during tuning the real circuit adjusted, especially to reach maximal output performance of the LMV358 in order to provide signal converging to 0-3.3V for the ADC.

Figure 33 shows how circuit of Figure 32 looks when simulated. Three voltage waveforms  $V_{AUDIO\_OUT}$ ,  $V_{AUDIO\_IN}$ ,  $V_{AUDIO\_OFFSET}$  are depicted as during testing tone 1kHz  $0.4V_{PP}$ . Note that the 1kHz is typical testing tone for audio devices.

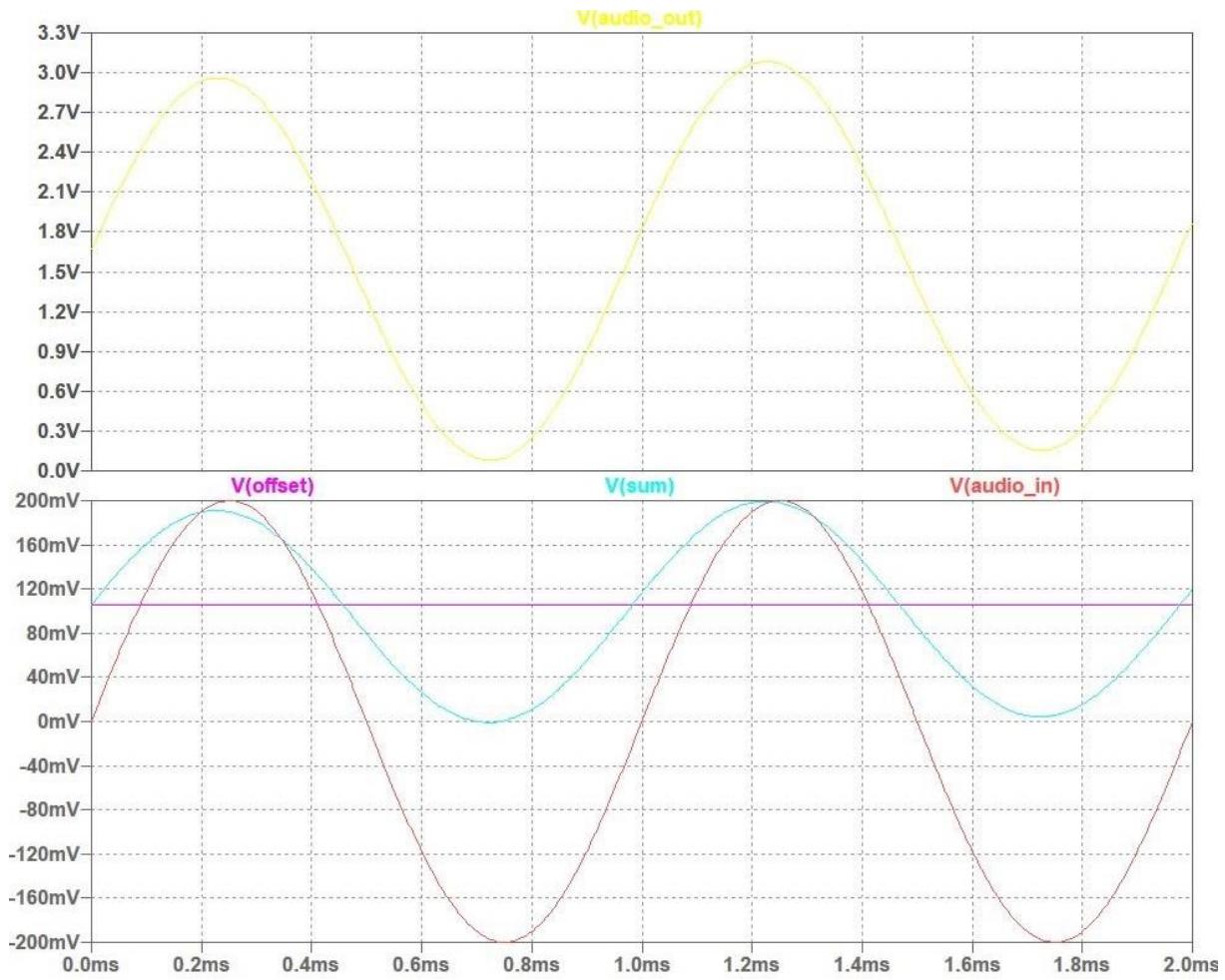


Figure 33 Audio input circuit simulated in LTSPICE (LMV358 model used)

## ADC AD7476

The AD7476 converter was selected because of following features:

- 12-bit conversion referenced to power supply voltage
- Straightforward SPI operation via CS, SDO and SCLK
- SOT-23-6 package.
- 1MSPS baudrate

The AD746 is lower power IC, which can be power supplied by voltage reference chip such, however in this case of implementation is no precise reference needed, as the description of the audio signal does not require precise level measurement. Interfacing via SPI is straightforward by activating the CS and data-out shifting 24 clock cycles to read conversion, whereas conversion takes first 4 cycles.

The ADC has RC filter on its CLOCK line to prevent signal ringing and thus crosstalk interference for other circuits e.g. audio input amplifier. In this case, serial resistor is placed to SPI master (FPGA), meanwhile blocking capacitor close to the ADC.

# PCB layout guidelines

In this chapter, several guidelines to design sufficiently good PCB are listed. As the design operates in high frequencies and contains several mixed-circuit parts, must be special approaches taken in account. For cost and complexity reasons, 2-layer PCB approach was selected.

## Grounding

Already in the chapters discussing the system proposal was mentioned, that several grounds for digital, analog (RF) and DAC0 are used. The reason why are grounds split is to minimize mutual interference. Very good approach is to use one layer of the multi-layer PCB as the ground layer.

Ground must be always high-conductive trace/part of circuit, so ground integral planes are nice solution to reach this. By the integral is meant, that ground is not disconnected by other traces. When is the ground disconnected, signal must flow through longer path and may get additional noise or interference. The best approach for RF is chassis-grounding, whereas is around and below the RF circuit "copper" fence blocking all the interference going-out or going-in. However, using this approach for several RF parts and different circuit discussed previously would result in too complex PCB.

In this design, usage of the Star ground topology was used to connect AGND, DGND and GNDINT.

- DGND – all the digital circuits such as audio input, DAC1 and DAC0, but also communication like UART, buttons
- GNDINT – output ground for the DAC0 (modulation parallel fast DAC) decoupled using transformer
- AGND – all the RF output circuitry including the carrier signal path and Modulation signal path

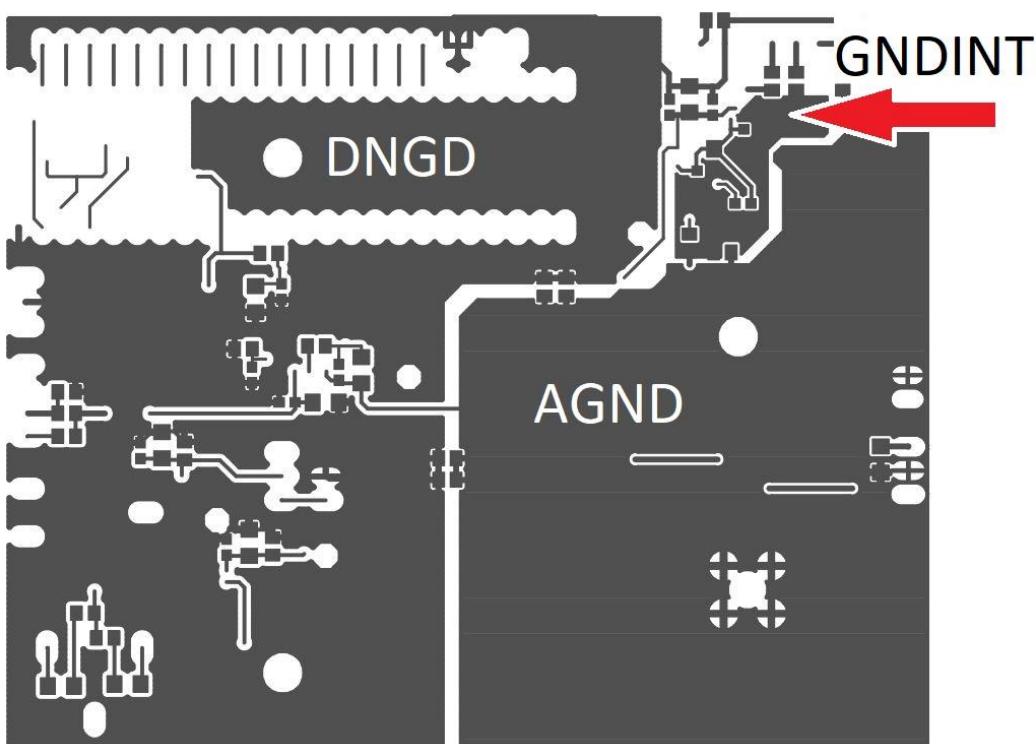


Figure 34 VHF-Transmitter PCB: AGND, DGND, GNDINT

Figure 34 shows, how were the grounds split in the design. The most of the PCB area is used for the DGND, because FPGA, input circuits and DAC1, DAC0 uses this ground as the reference. The AGND is on the right side of Figure 34 showing dimensions of the RF circuit (carrier, modulation, mixer). The smallest ground is GNDINT in the right-up corner which is reference only for the DAC0 output. Note that GNDINT may be connected to the AGND, just for sake of correctness possibility to split DAC1 complementary current output into DAC1 single ended output was this ground used.

Through the center of the PCB leads white line signalizing border of grounds and as well are obvious in the middle two double-spots for SMD parts to couple AGND and DGND together. This might be done using soldered amount of tin to connect the SMD pads as well as by the ferrite bead if needed (ferrite bead will block eventual interference going to other ground). The GNDINT may be connected directly only to the AGND using either single SMD part (ferrite bead) or soldered thin of the same dimension. The connection point is at the bottom of the GNDINT plane.

# Coplanar waveguide

The usage of waveguide is dedicated for high-speed analog designs to route parts with minimal distortion. The approach of waveguide is more common for microwave signals rather than VHF, but its usage has advantages of central ground plane and RF and rejection of interference in compare to microstrip. System contains several parts so if no waveguide technic used, system would probably not efficiently work.

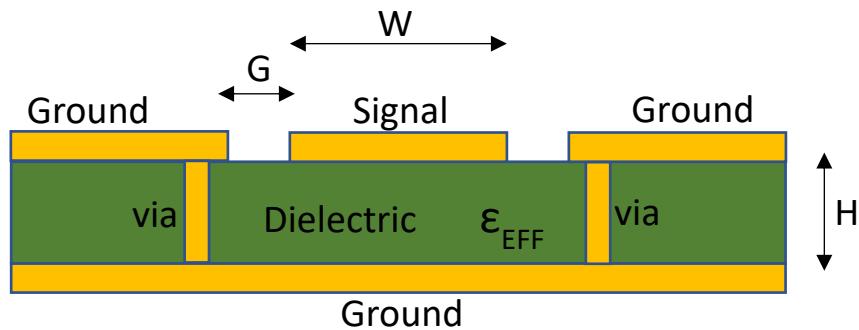


Figure 35 Coplanar waveguide

The coplanar waveguide characteristic impedance is dependent on the:

- Width (W)
- Gap Width (G)
- Dielectric Height (H)
- Dielectric effective constant  $\epsilon_{\text{EFF}}$  (based on  $\epsilon_R$  of the used dielectric)

Using online calculator was  $\epsilon_{\text{EFF}}$  and thus dimensions for  $50\Omega$  coplanar waveguide calculated:

- Width (W): 1.5mm
- Gap Width (G): 1.27mm
- Dielectric height (H): 1.6mm
- Dielectric effective constant calculated out of the FR4 dielectric ( $\epsilon_R=4.4$ ): 3.15

The calculated values are valid for the FR4 PCB of the 0.8mm thickness and thus, the entire VHF-Transmitter PCB is 0.8mm thick. Note that there are better dielectrics than FR4, but for this application is FR4 good enough.

To enhance the coplanar waveguide were used often via surrounding of the coplanar signal trace with clearances 2mm between each other.

# RF circuit used techniques

Several approaches taken in account in the design are disused. The approaches are widely known for RF as well as analog techniques, so no reference literature is enclosed.

## Bending for the 90° traces

Not only RF or analog designers avoid perpendicular trace. Correct trace bending is critical also for high speed digital designs such as clock or data lines. Instead of direct perpendicular bend are two 45° bends in order to avoid reflection as well as protentional radiation from the bend point.

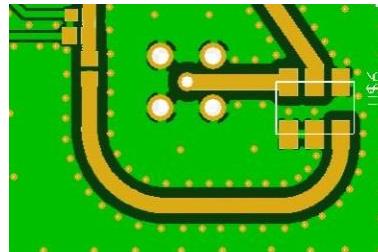


Figure 36 Trace bending using radius

Figure 36 shows, one approach to avoid perpendicular bend. For RF there is a way to calculate right angle without radius usage, however in the design was enough space to afford the radius way of bending the trace.

It is known, that trace bent with radius at least of:

$$r \geq 3 \times W_{TRACE} \geq 3 \times 1.5mm \geq 4.5mm$$

Has negligible impact on the signal radiation or signal reflecting. Therefore, bending with 4.5mm is used several times in the design.

## Trace width matching

As the width of the trace for the coplanar waveguide was calculated as 1.5mm not every part of the RF circuits has pin of this width. In this case, gradual width matching is needed to avoid sharp transitions and so possible reflection or radiation. Often, it is better to use e.g. resistor in the package which is similarly width as the trace width rather than use dimensionally unequal parts.

However, it is often referred that parts in the trace, which have not same width and thus also impedance, but the length of this unmatched trace part is smaller than:

$$\text{length}_{\text{UNMATCHED}} \leq 0.1 \times \lambda \leq 0.1 \times \frac{c_0}{f} \leq \frac{3 \times 10^8 \frac{m}{s}}{100 \text{MHz}} = 30 \text{cm}$$

May be negligible, because have no impact and are causing no reflection or radiation

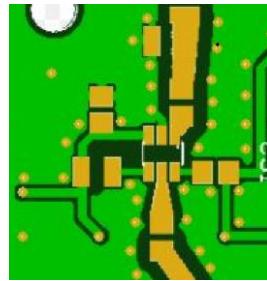


Figure 37 Width matching to match part and trace for SOT-23-6 (THS9001)

## RFVDD coupling to AGND using small gap

The ground plane should be not disconnected by other signal line. Finally, it was necessary in the design, to partially violate this rule and lead power supply line in the same layer as the AGND ground is. If this non-elegant approach is used, at least is good to ensure, the gap between the power supply line and surrounding ground plane is as small as possible. This fact will cause parasitic impedance, which may be in this case used as interference decoupling. Practically, minimal isolate gap is used when PCB is designed to reach power supply line decoupling, unlikely for the signal path would have this approach undesired effect

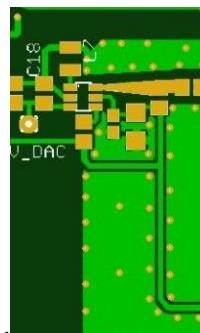


Figure 38 Coupling supply line with the AGND by small gap

# Proposed PCB

Proposed PCB of figure 39 shows entire design including the RF-out proposal, the Audio-in as well as the other parts discussed e.g. in the System proposal chapter.

The right part of the PCB is the RF-out part with obvious coplanar waveguide. The output of the board is the SMA connector in the bottom-right corner.

The left part of the PCB is the digital part converting the Audio in into digital signal with 3.5mm jack in the bottom-left corner.

The core of the system is the FPGA module CMODS6, which is the upper part with 48-pin THT package. The center-top shows connection of the parallel DAC0 to the FPGA using bent traces with compensated length to ensure synchronous clock and data arrival.

Three holes, two on the left and one on the right are dedicated for the future PCB mounting into box. Figure 39 shows only top layer of the PCB, meanwhile the bottom is in fact Figure 34.

Except all the mentioned see amount of vias used in the RF part to enhance RF AGND conductivity. For better appearance was used the ENIG (Electroless nickel immersion gold) surface PCB masking with for purpose restricted area of the coplanar waveguide trace to highlight it

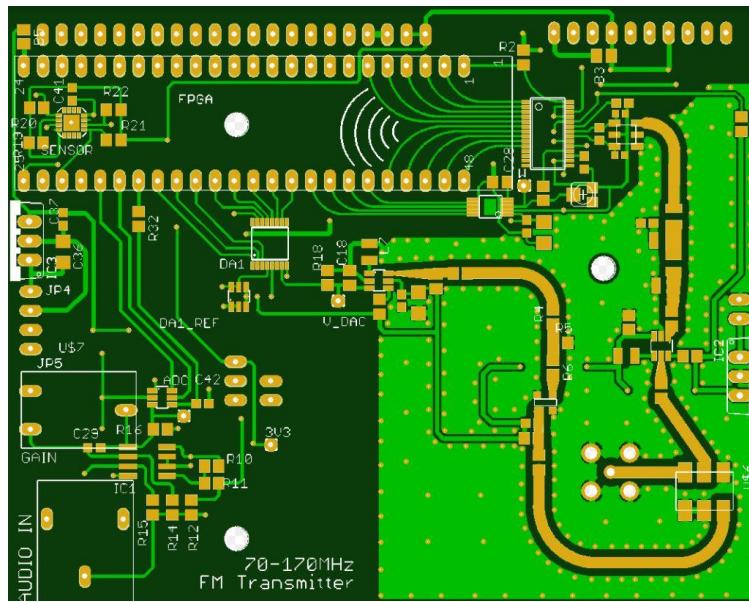


Figure 39 VHF-Transmitter PCB top layer

# HW Bring-up

The VHF-Transmitter contains several analog parts with determined voltage/current references, bias currents, attenuation and impedance matchings. These estimations may differ from really fitting values. Due to these facts, the system must be assembled gradually and all analog circuits well tested, one after another.

## Carrier signal path

Refer to [Figure 5](#), the critical part in the carrier signal path is the VCO. Although the first part of the carrier signal path is the DAC1, no unexpected behavior is for this IC expected so the VCO got yield to be soldered as the first.

### MAX2606

Figure 40 depicts the standalone VCO MAX2606 circuit matched to  $50\Omega$  including  $50\Omega$  load represented by measure device (oscilloscope/VNA). The  $V_{TUNE}$  is adjusted by an external power supply device. The figure 40 is derived out of [Figure 10](#). The measured board is photograph of figure 41.

The expected operational behavior is:

- Operational frequency adjusted by the  $V_{TUNE}$ : 65-83MHz
- Output power  $P_{OUT}$ : -10dBm

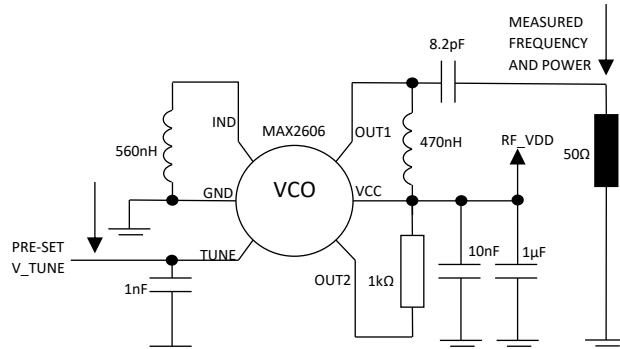


Figure 40 VCO MAX2606 testing circuit

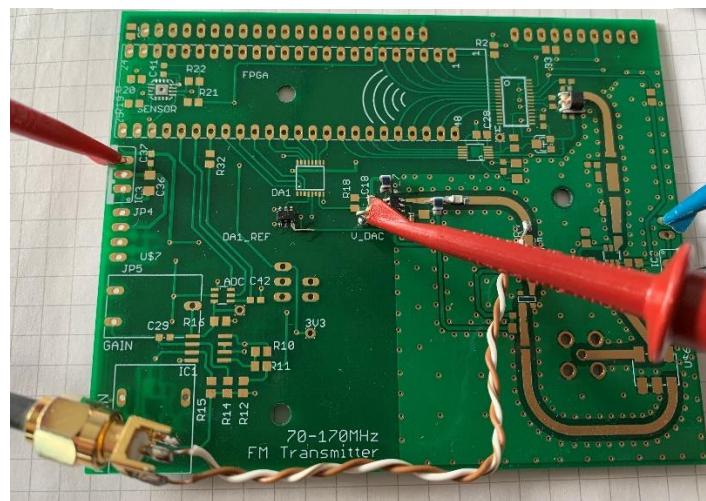
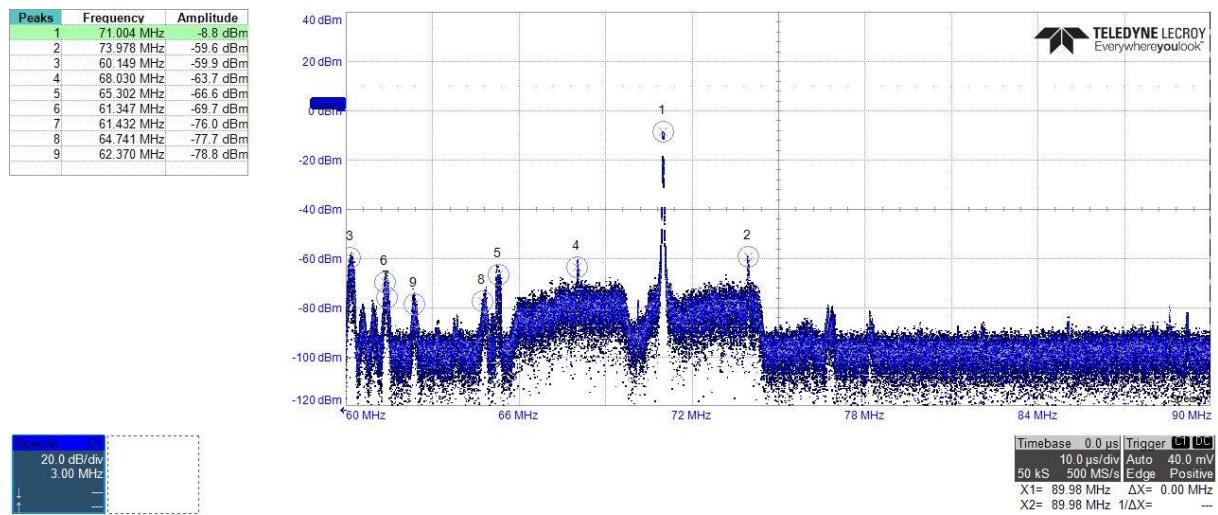
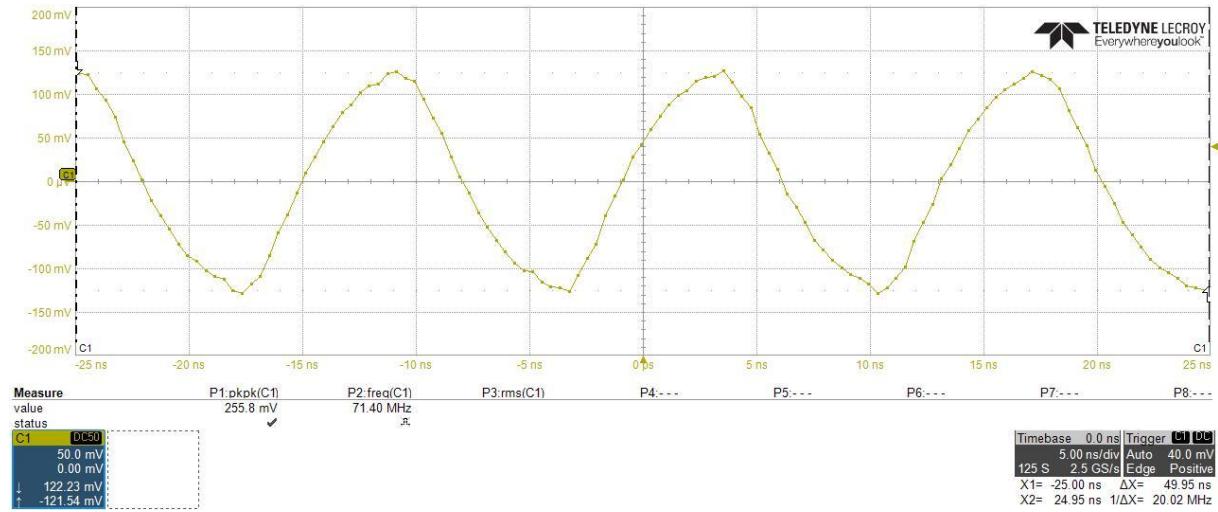


Figure 41 Measurement setup of the VCO MAX2606

## Testing $V_{TUNE} = 0.6V$



## Testing $V_{TUNE} = 1.85V$

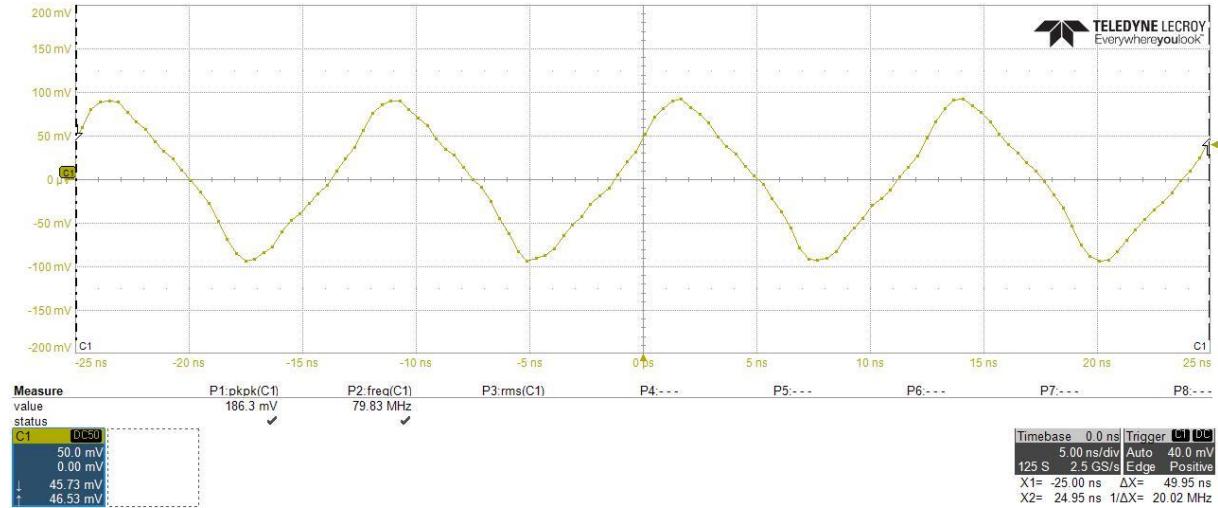


Figure 44 MAX2606 testing  $V_{TUNE} = 1.85V$ , shape detail

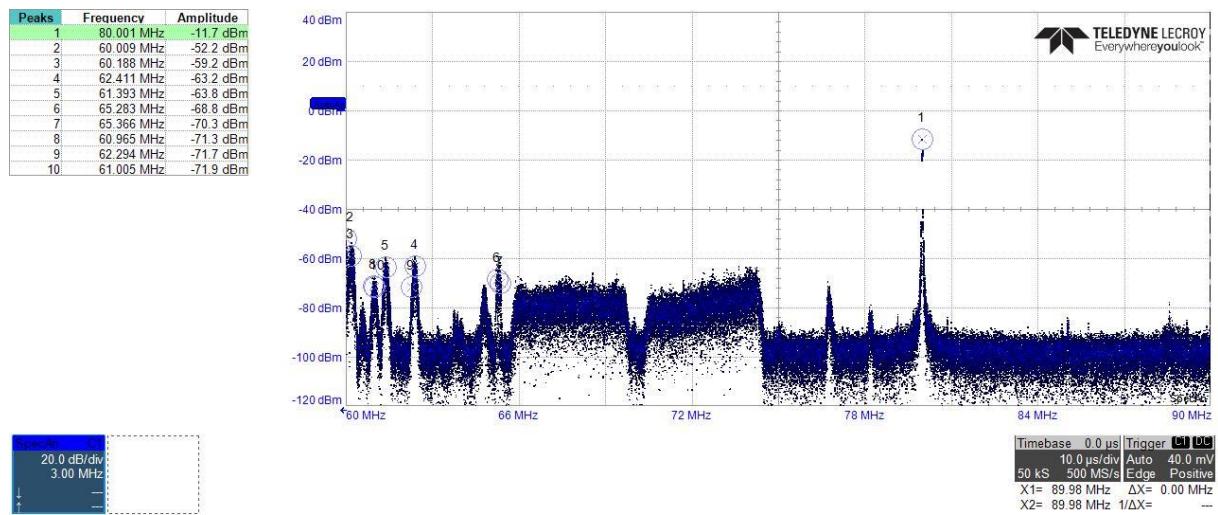


Figure 45 MAX2606 testing  $V_{TUNE} = 1.85V$ , spectrum detail

## Testing $V_{TUNE} = 2.4V$

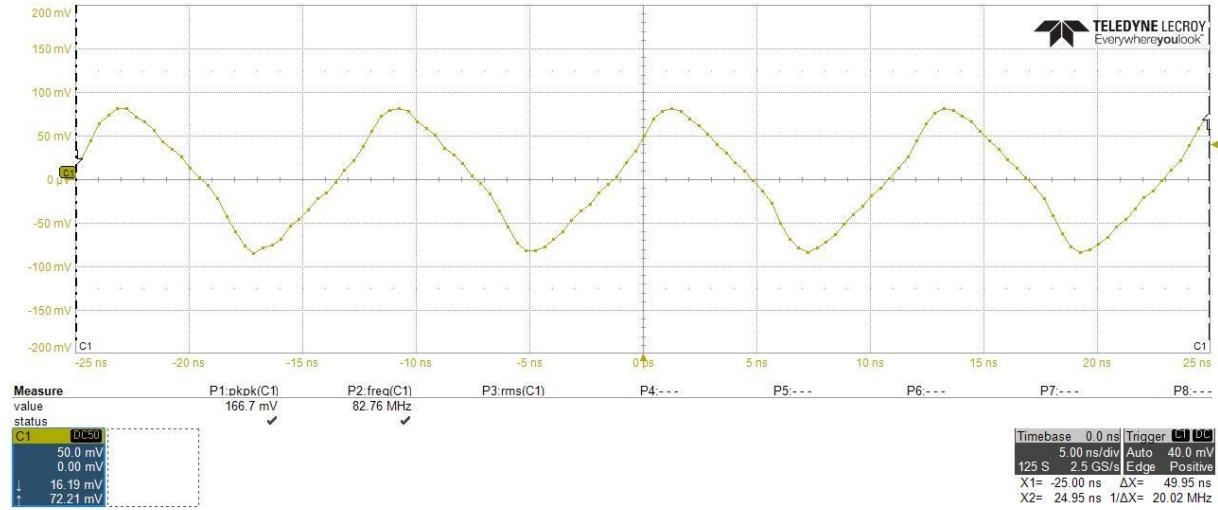


Figure 46 MAX2606 testing  $V_{TUNE} = 2.4V$ , shape detail

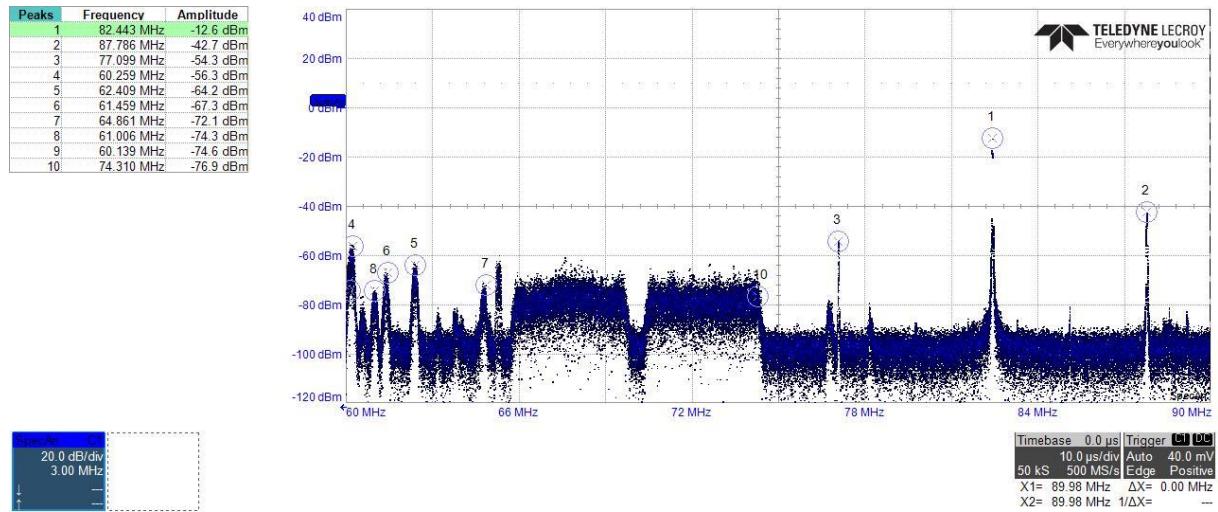


Figure 47 MAX2606 testing  $V_{TUNE} = 2.4V$ , spectrum detail

## Testing Extra: FM modulation

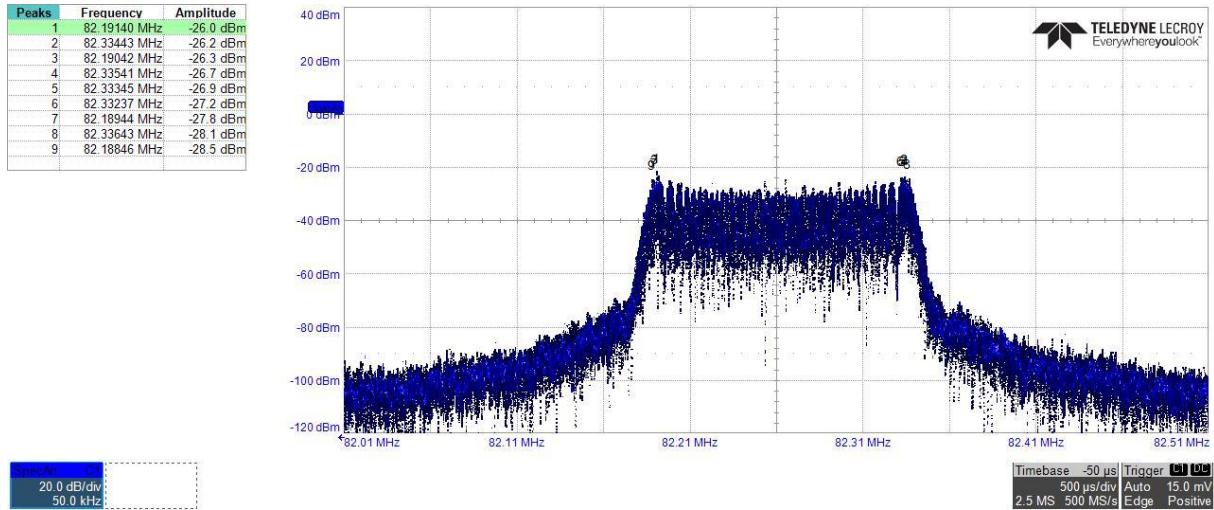


Figure 48 Testing Extra  $V_{TUNE} = 600\text{mV} + V_{MODULATION}$  15mVpp, 560nH Inductor

## Testing Extra, persistence measurement $V_{TUNE} = 1.85V$

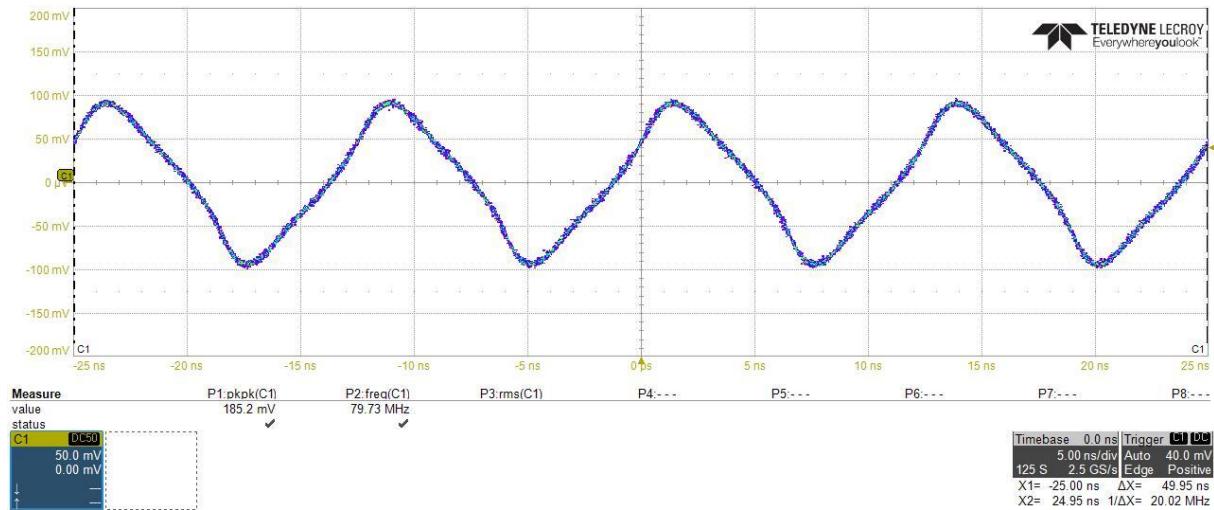


Figure 49 Figure  $V_{TUNE} = 1.8V$ , persistence shape detail

## *Conclusion*

- Expected frequency range 63-83MHz
  - Reached 71-83MHz (not measured below  $V_{TUNE} < 0.6V$ )
  - **Frequency operational frequency reached**
- Expected output power -10dBm
  - Reached -9dBm down to -12dBm for 71-83MHz
  - **Output stage of the VCO is well matched**
- Current consumption measured
  - 2mA at 5V – stable across frequency
- Low jitter obvious from Figure 49
- Extra: Figure 48 FM modulation using:
  - $V_{TUNE} = 0.6V_{DC} + 15mV_{PP\_AC\_1kHz}$
  - FM bandwidth  $\approx 20kHz$
  - Lower power reached due to unmatched operation

## MAX2606 + attenuator + MAX2611

Figure 50 depicts the VCO MAX2606 matched to  $50\Omega$ , attenuated and amplified using the MAX2611. The  $50\Omega$  output load is represented by measure device (oscilloscope/VNA). The  $V_{TUNE}$  is adjusted by the DAC1 AD5761 (already controlled by the FPGA via SPI). The figure 50 is basically [Figure 10](#), with simplified DAC1 + load. The measured board including the FPGA and DAC1 is photograph of figure 51.

The expected operational behavior is:

- Operational frequency adjusted by the  $V_{TUNE}$ : 65-83MHz
- Output range +3dBm

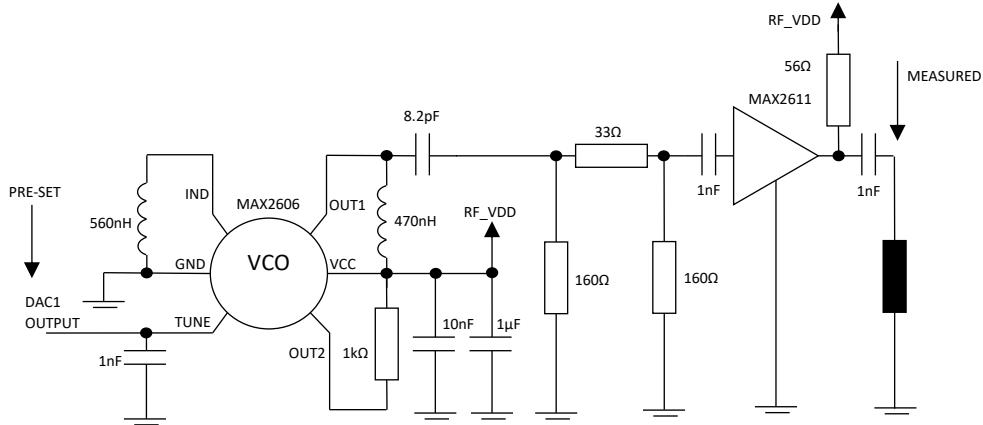


Figure VCO MAX2606 + the attenuator + the Amplifier MAX2611 testing circuit

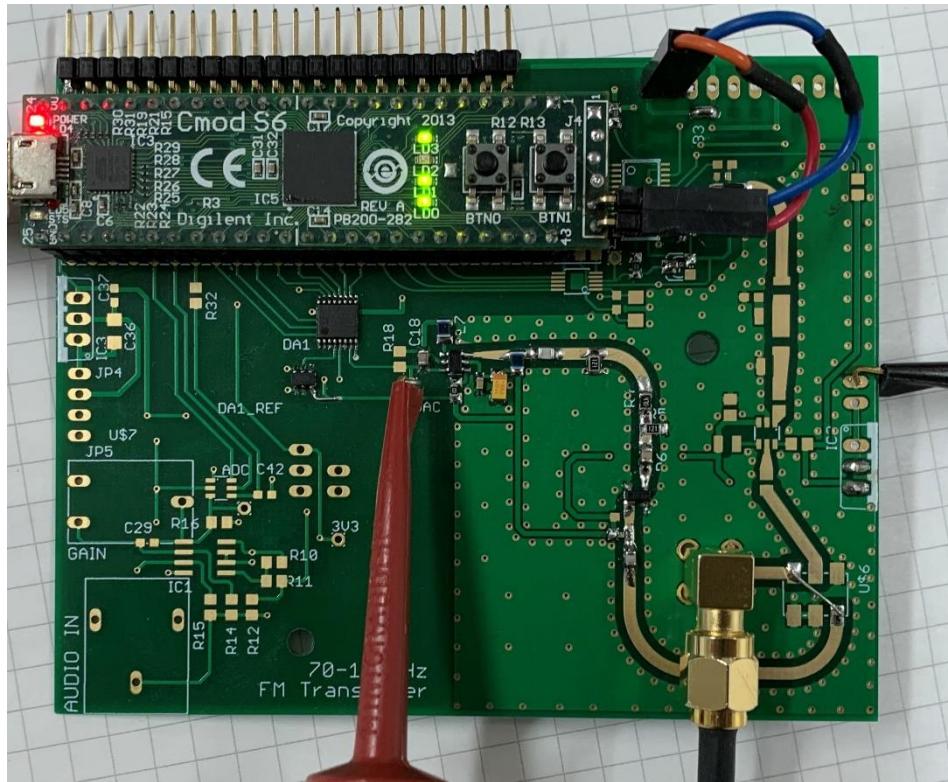
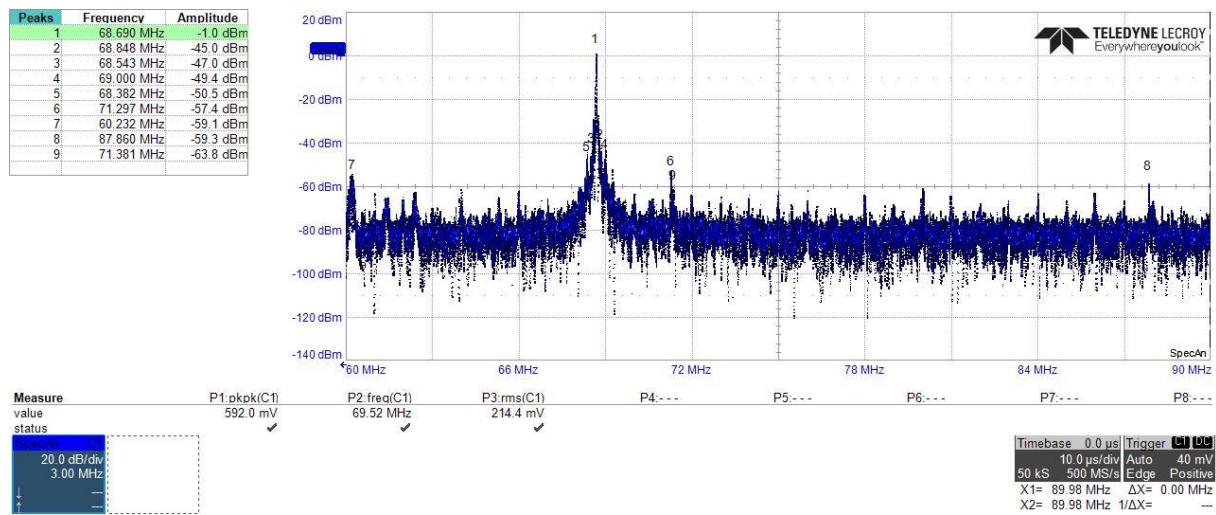
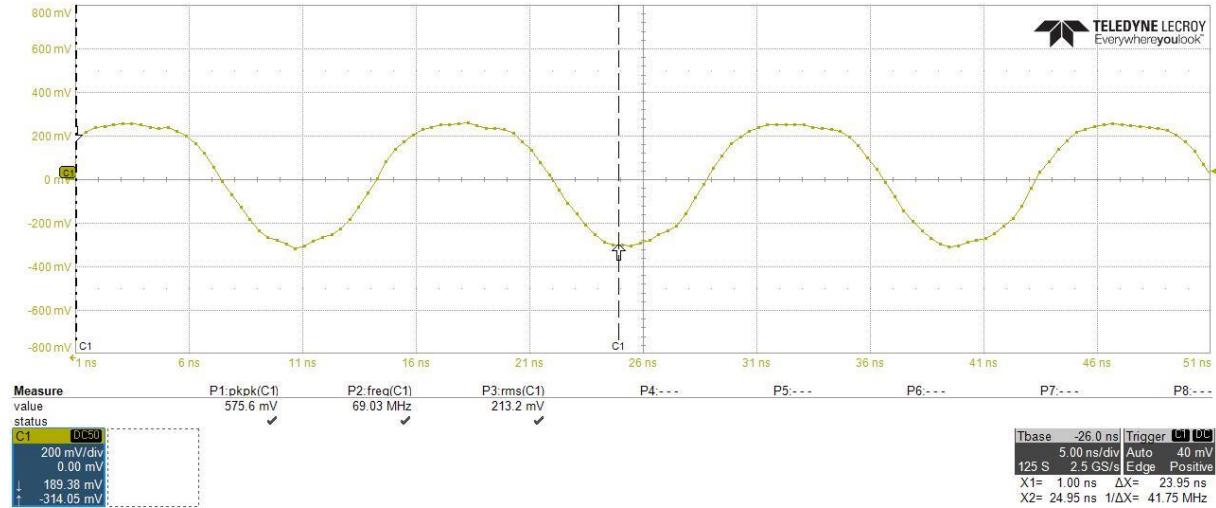


Figure 50 Measurement setup VCO MAX2606 + attenuator + MAX2611

## Testing $V_{TUNE} = 0.4V$



## Testing $V_{TUNE} = 0.6V$

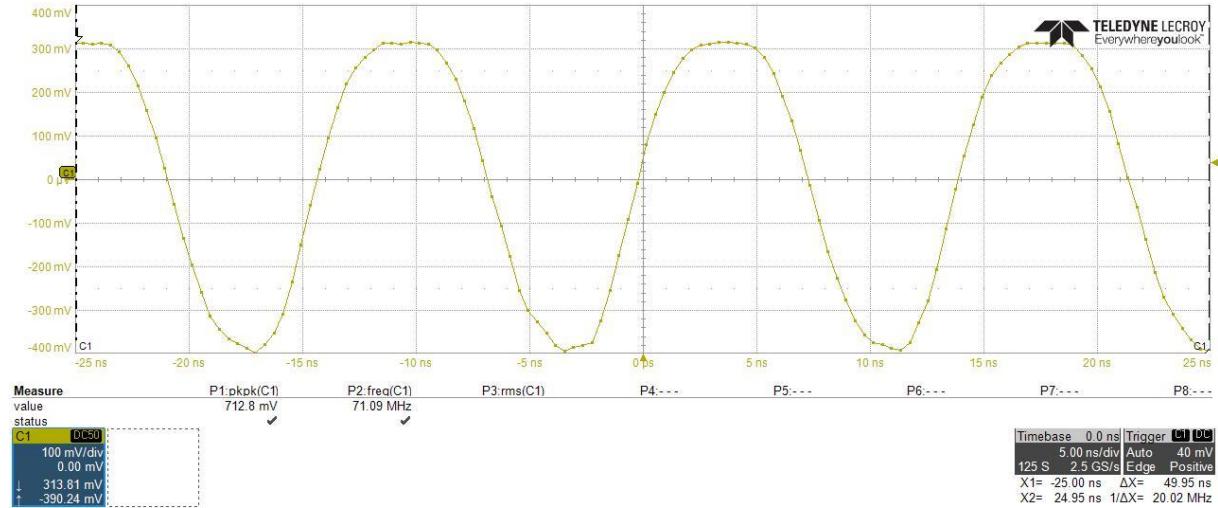


Figure 53 MAX2606 + attenuator + MAX2611 testing  $V_{TUNE} = 0.6V$ , shape detail

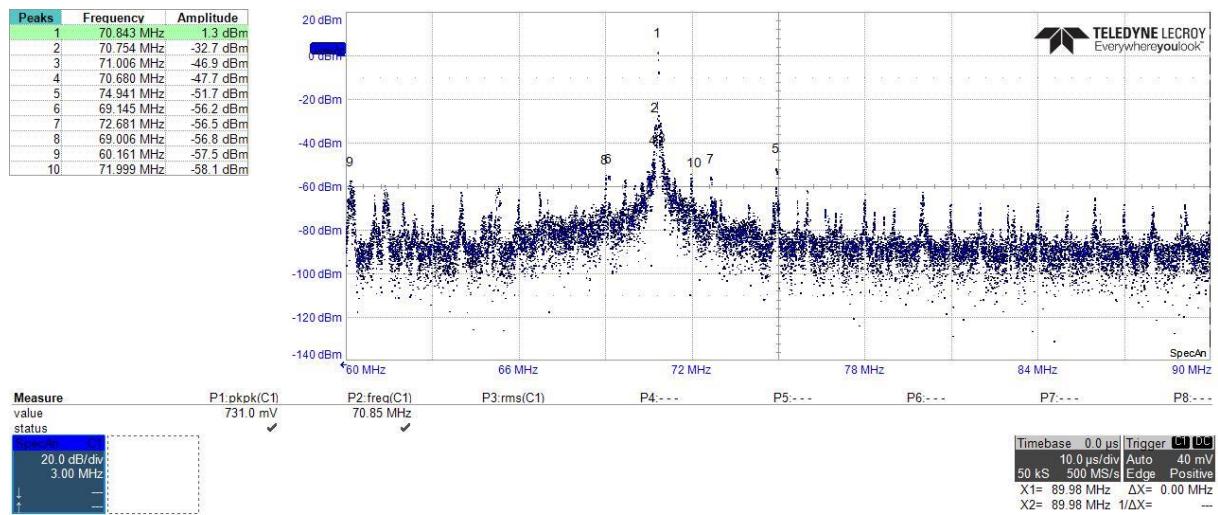
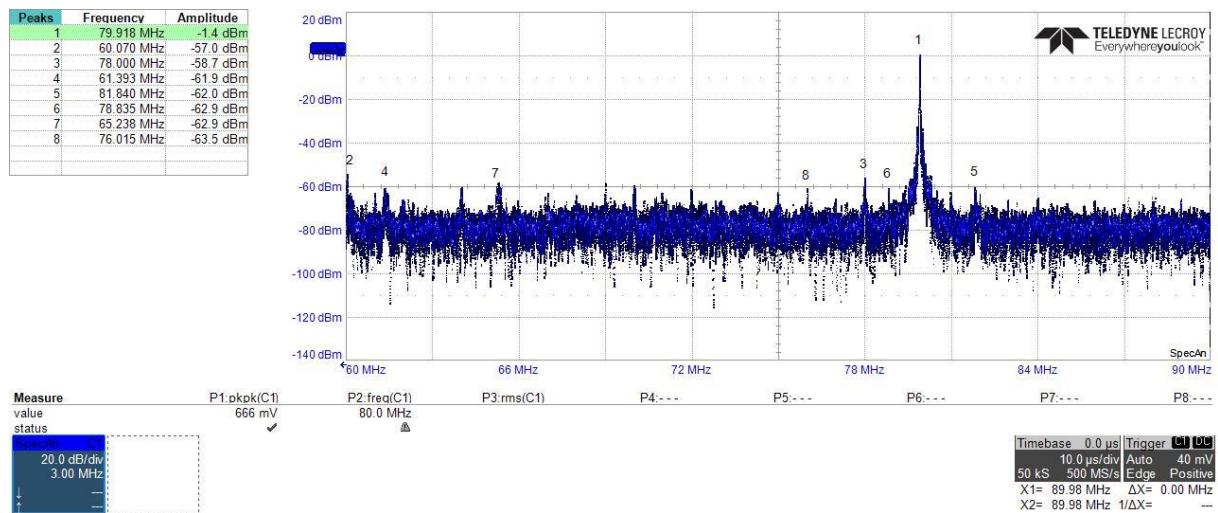
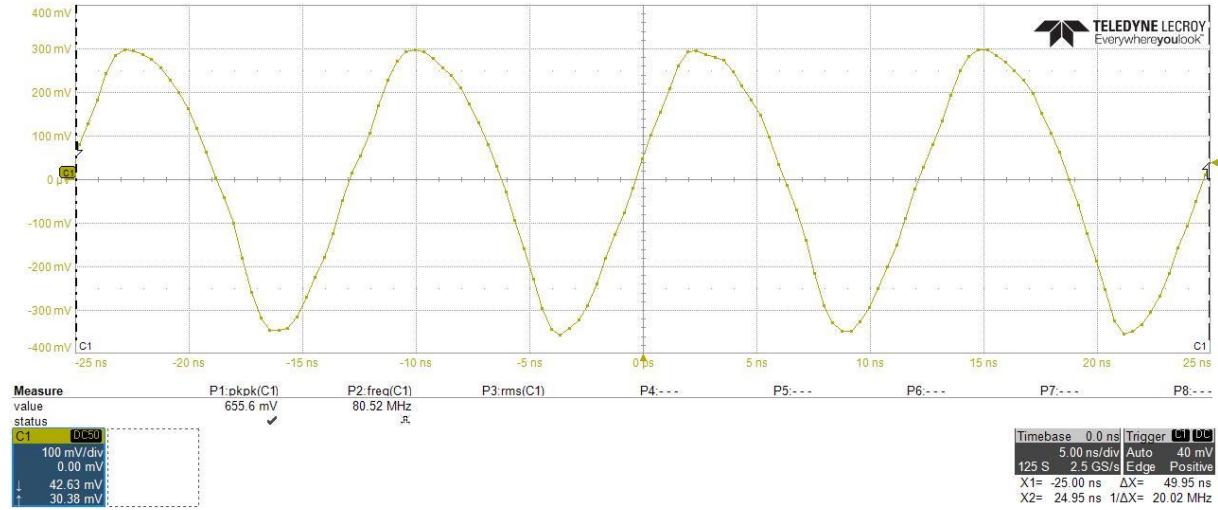
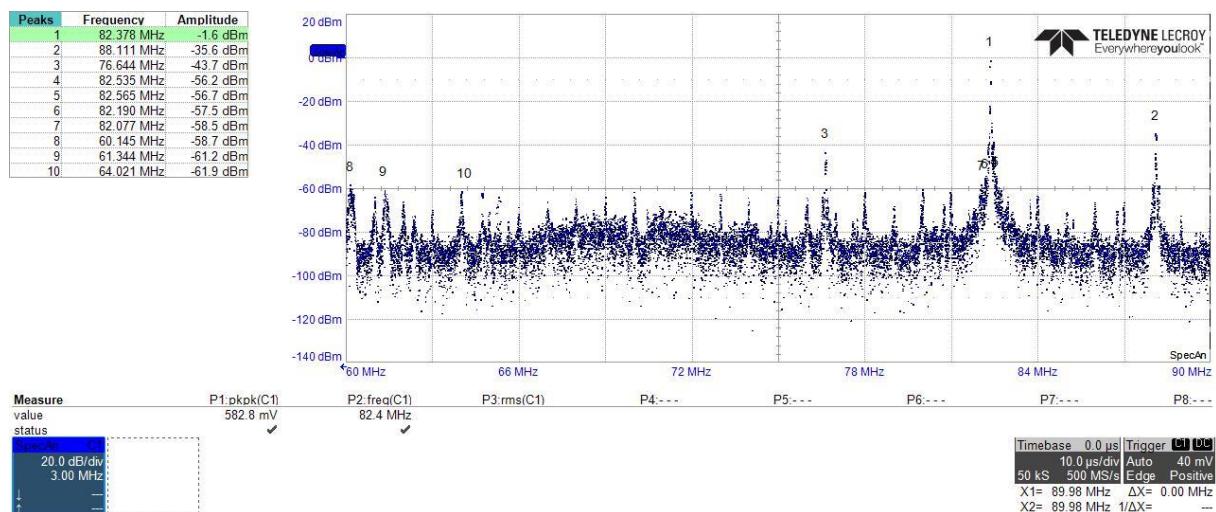
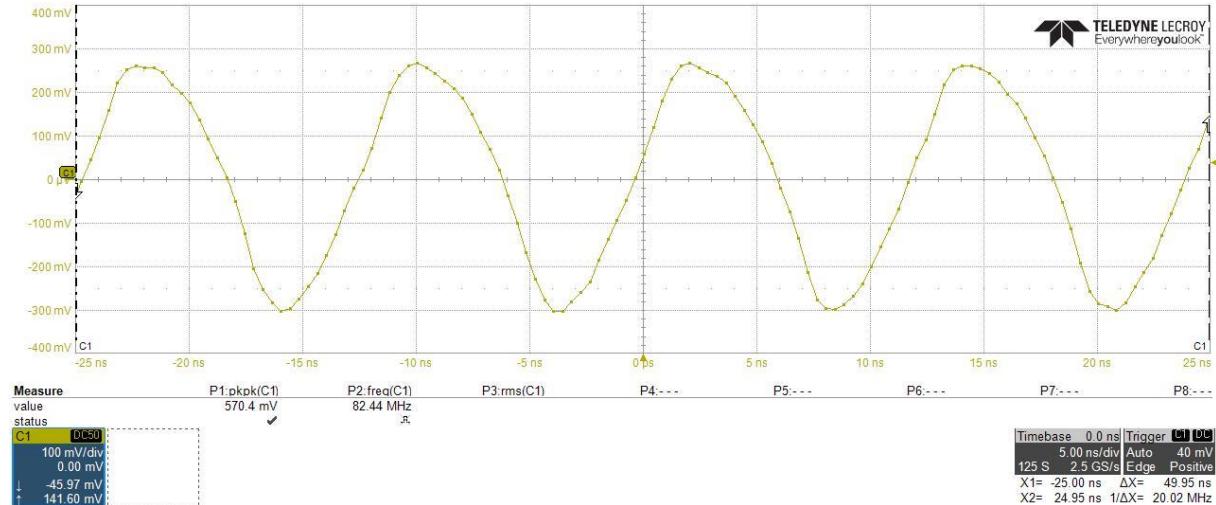


Figure 54 MAX2606 + attenuator + MAX2611 testing  $V_{TUNE} = 0.6V$ , spectrum detail

## Testing $V_{TUNE} = 1.85V$



## Testing $V_{TUNE} = 2.4V$



Testing whole setup with DAC1 voltage evaluation, MAX2611 distortion

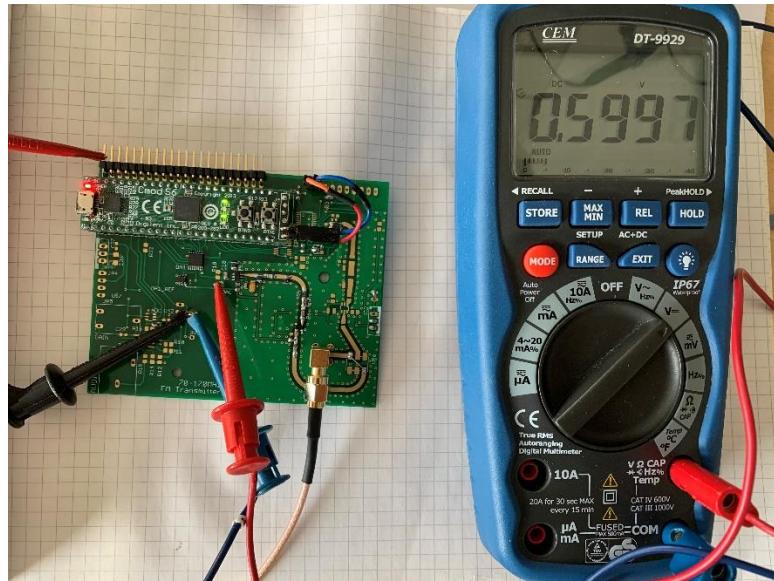


Figure 59 VCO MAX2606 + attenuator + MAX2611 + DAC1 AD5761 V\_TUNE = 0.6V evaluation

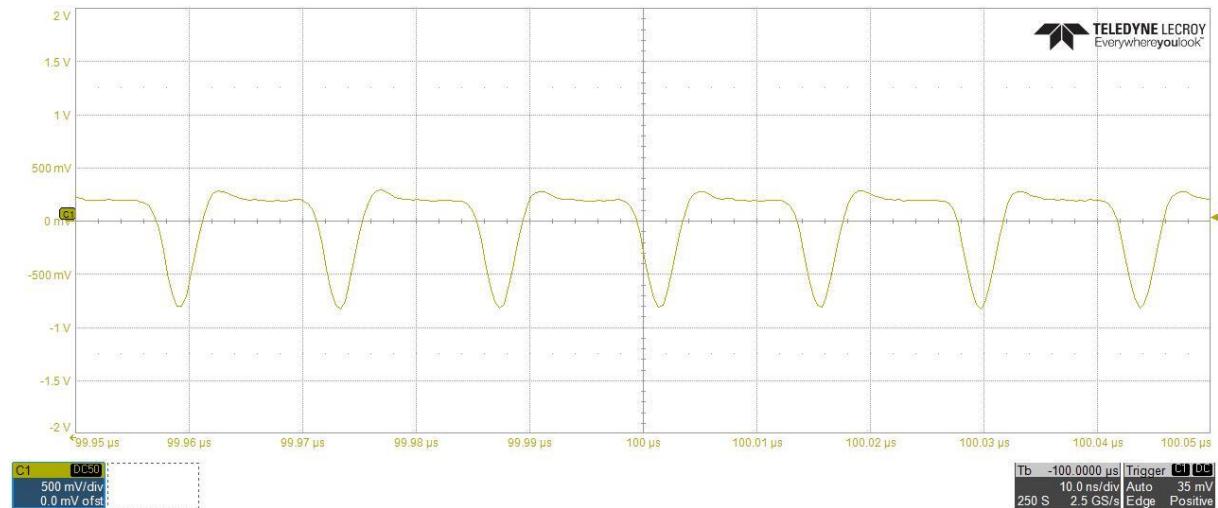


Figure 60 VCO MAX2606 + no attenuator + MAX2611 distortion reaching

## *Conclusion*

- Expected frequency range 63-83MHz
  - Reached 69-83MHz
  - Operational frequency not fully reached, only range 69-83MHz tuning
- Expected output power 3dBm
  - Reached +1.2dBm down to -1.6dBm for 69-83MHz
  - Output power lower by 1.8 – 2.8dB than expected
  - Optimal usage for frequency f
- Current consumption measured
  - 22mA at 5V – stable across frequency
- Extra: Figure 59 DAC1 AD5761  $V_{TUNE}$
- Extra: Figure 60 MAX2611 distortion
- Possible improvement using the filter for the MAX2611
  - Signal shape enhancement
  - Output power enhancement

# Modulation signal path

Refer to [Figure 5](#), the critical part in the Modulation signal path is the DAC0 AD9742, especially its highspeed parallel digital interface. The expected problematic point is the clock path for the DAC0 as the AD9742 in the TSSOP-28 package supports only single ended clock. Once the DAC0 provides deterministic output signal upon the DDS samples (generated by the FPGA), filtering the DAC0 is not assumed as big deal.

## AD9742 + WBC-1TL

Figure 61 depicts the standalone AD9742 circuit including  $50\Omega$  load represented by measure device (oscilloscope/VNA). The  $f_{OUT}$  is directly driven by the FPGA DDS. The figure 61 is derived out of [Figure 22](#). The measured board is photograph of figure 62.

The expected operational behavior for the DDS, DAC0  $f_{CLK} = 120\text{MHz}$  is:

- Operational frequency: 0.25MHz-60MHz
  - Bottom limit determined by the WBC-1TL  $f_{MIN} = 0.25\text{MHz}$
  - Upper limit determined by Nyquist theorem and  $f_{CLK} = 120\text{MHz}$
- Maximal amplitude  $V_{PP} = 0.96\text{V}$ 
  - Expected less due to the WLC-1TL 0.6dB insertion maximal loss
- Set maximal DAC0 output current 20mA via the  $2\text{k}\Omega$  FS\_ADJ
- Two's complement data input format

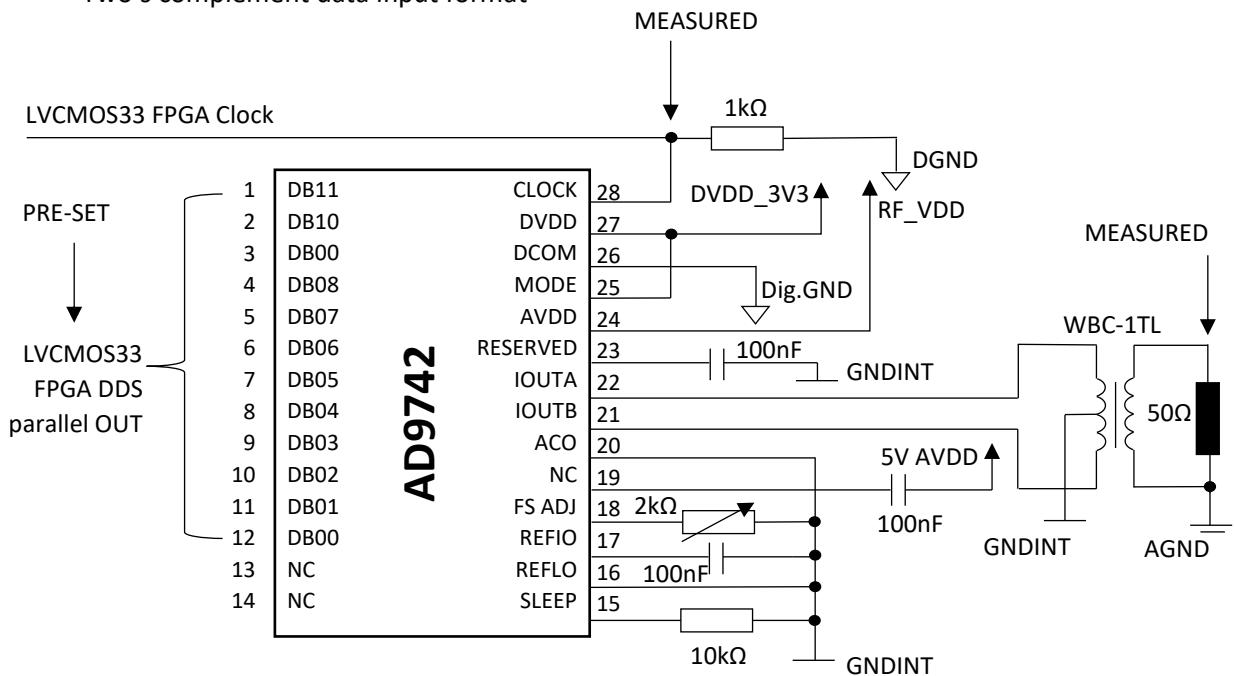


Figure 61 DAC0 AD9742 testing circuit

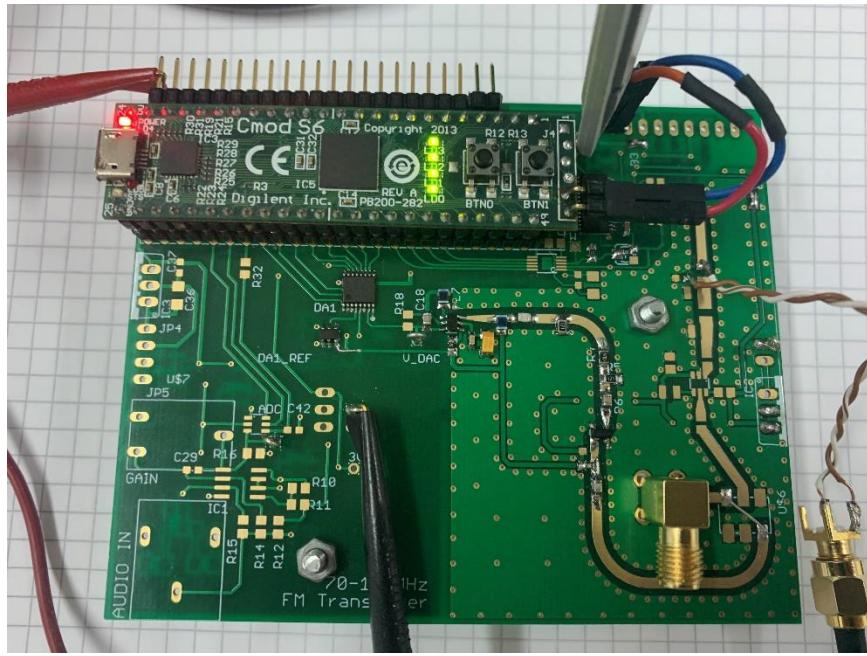


Figure 62 Measurement setup DAC0 AD9742 + WLC-1T

Testing  $f_{OUT} = 270\text{kHz}$

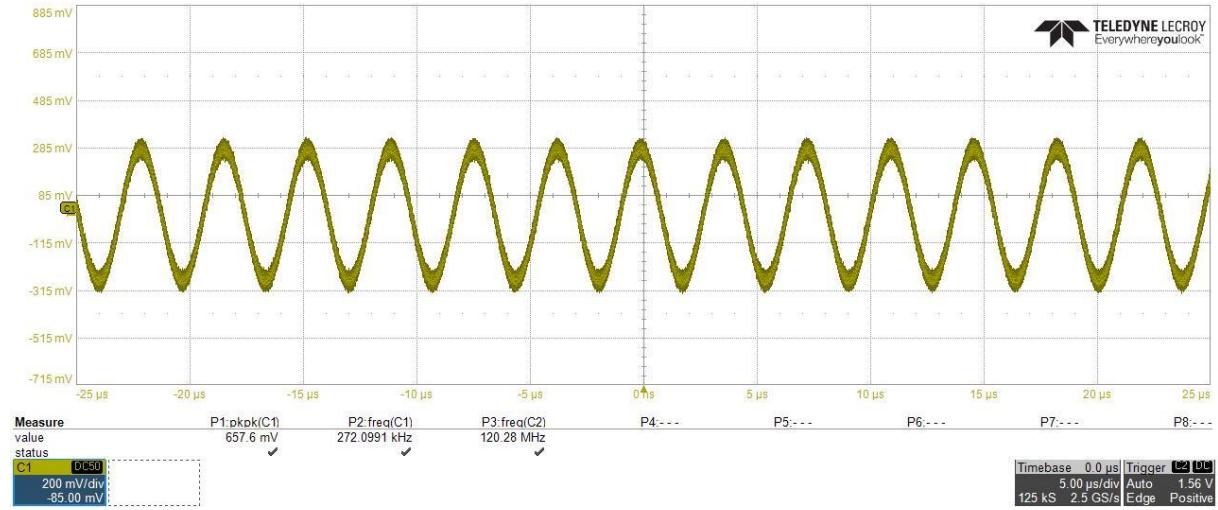


Figure 63 AD9742 + Low-Pass testing  $f_{OUT} = 270\text{kHz}$ , shape detail

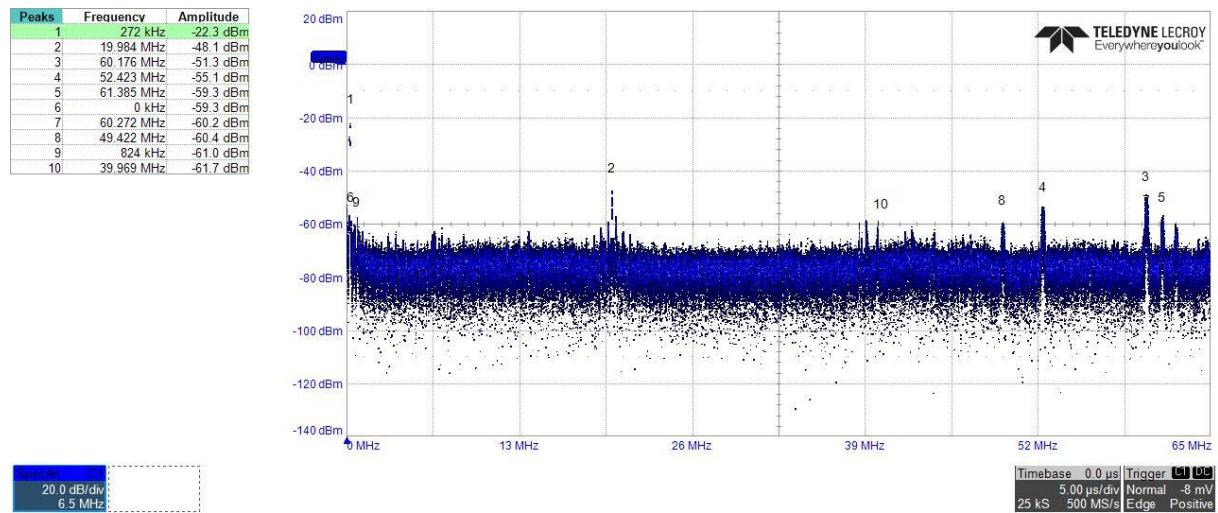


Figure 64 AD9742 testing  $f_{OUT} = 270\text{kHz}$ , spectrum detail

Testing  $f_{out} = 2.5\text{MHz}$

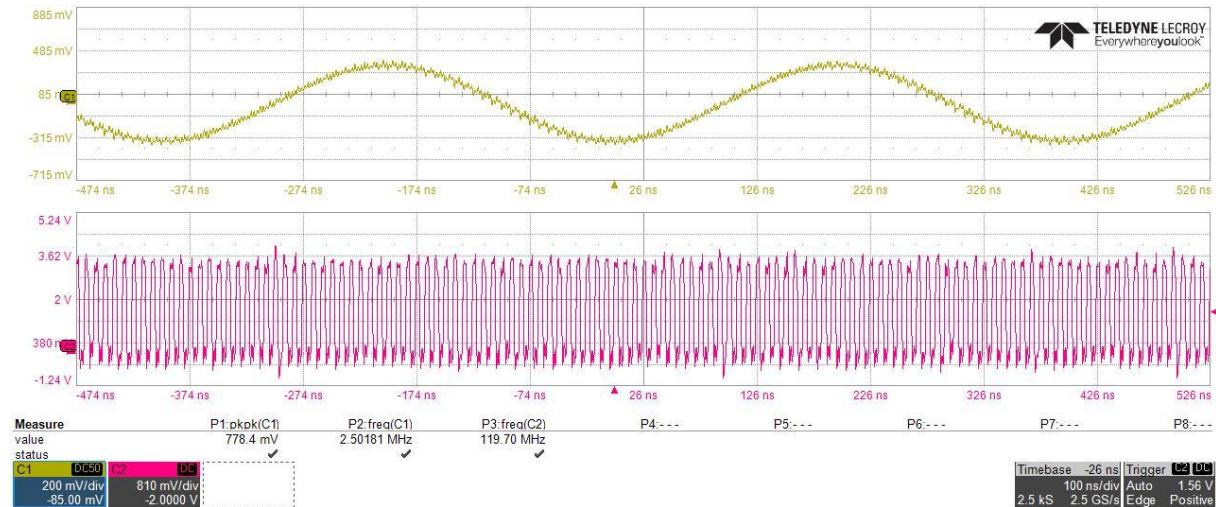


Figure 65 AD9742 testing  $f_{out} = 2.5\text{MHz}$ , shape + clock detail

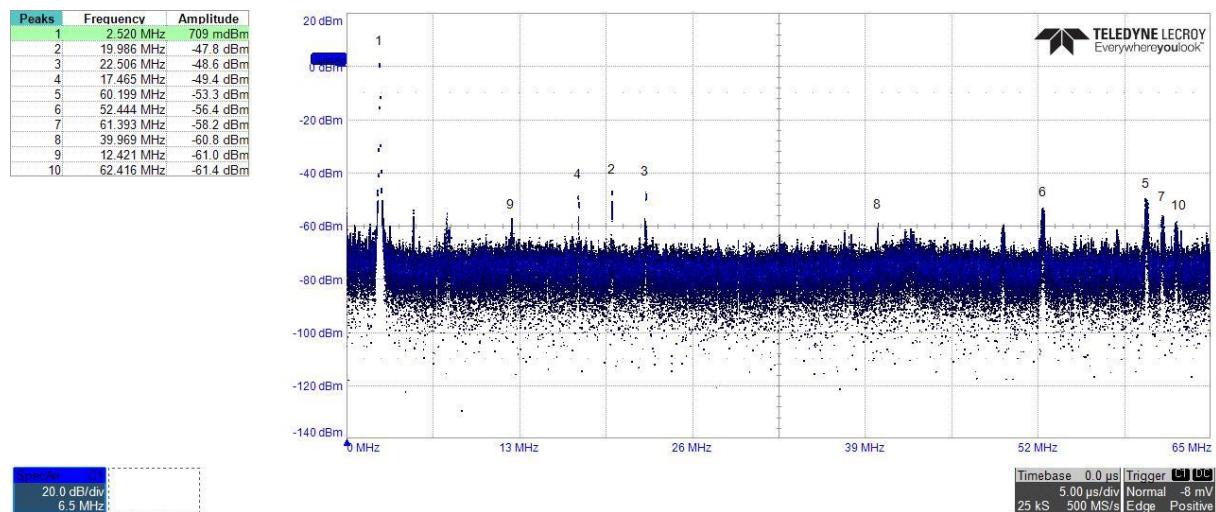


Figure 66 AD9742 testing  $f_{out} = 2.5\text{MHz}$ , spectrum detail

Testing  $f_{OUT} = 10\text{MHz}$

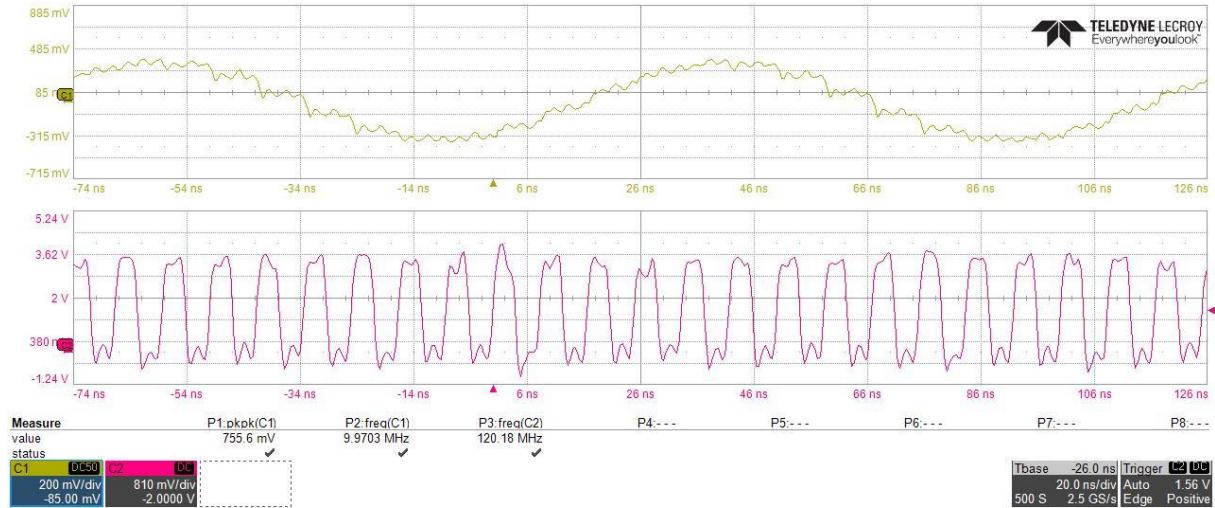


Figure 67 AD9742 testing  $f_{OUT} = 10\text{MHz}$ , shape + clock detail

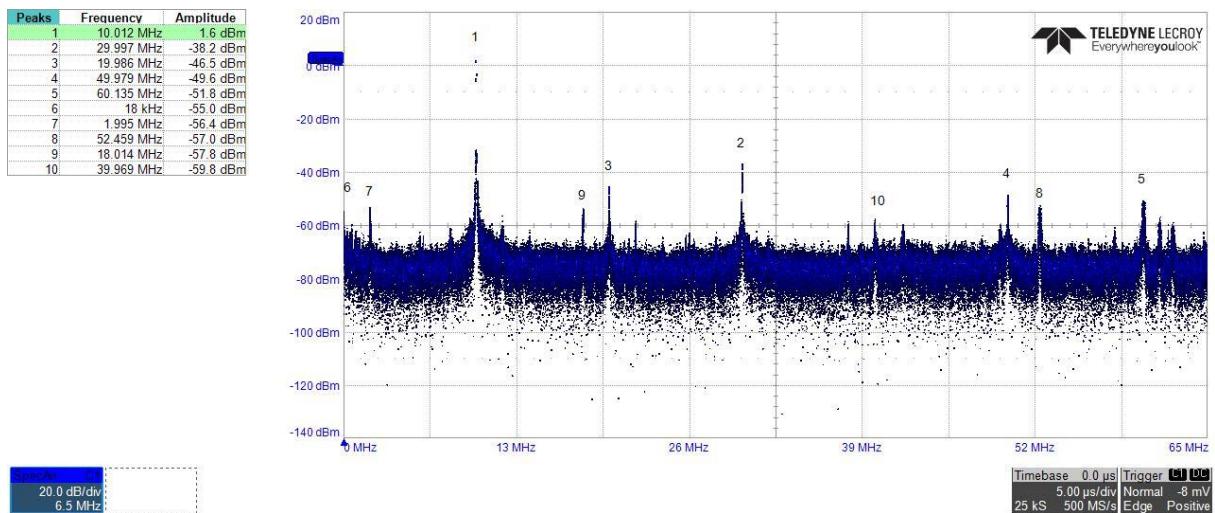


Figure 68 AD9742 testing  $f_{OUT} = 10\text{MHz}$ , spectrum detail

Testing  $f_{OUT} = 21\text{MHz}$

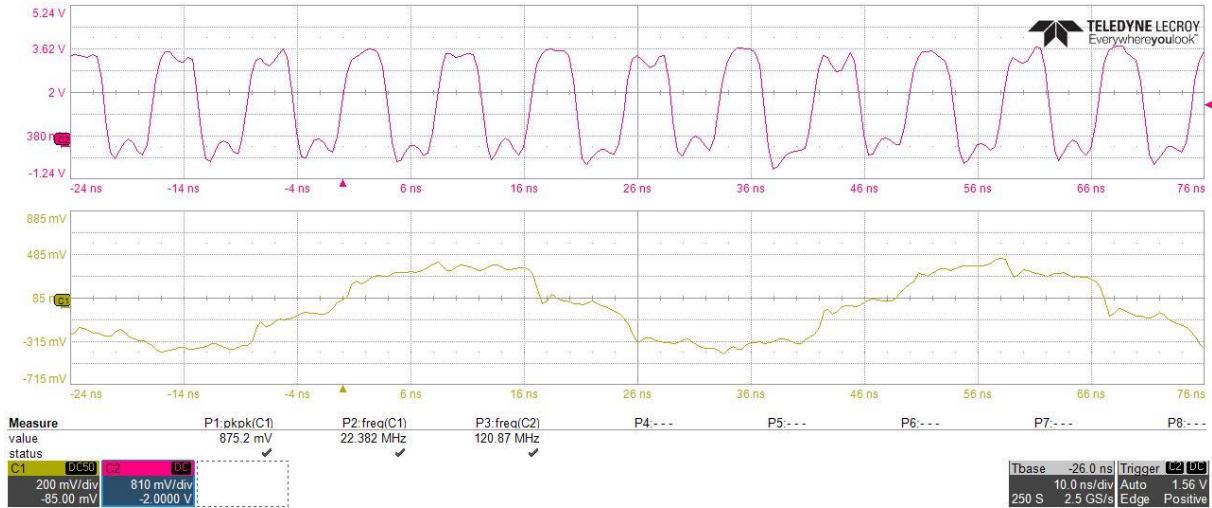


Figure 69 AD9742 testing  $f_{OUT} = 21\text{MHz}$ , shape + clock detail

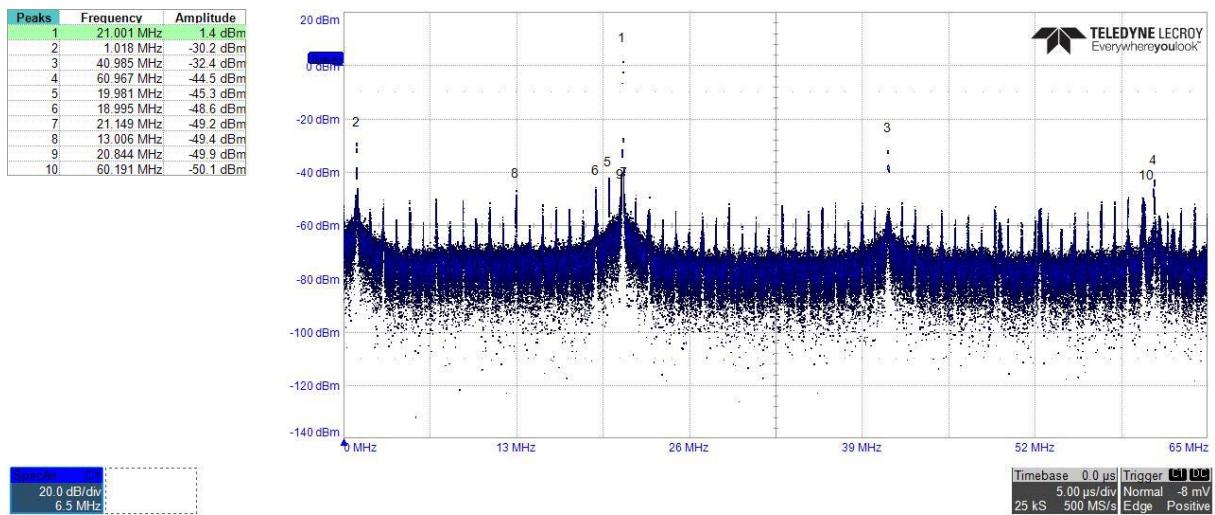


Figure 70 AD9742 testing  $f_{OUT} = 21\text{MHz}$ , spectrum detail

Testing  $f_{OUT} = 30MHz$

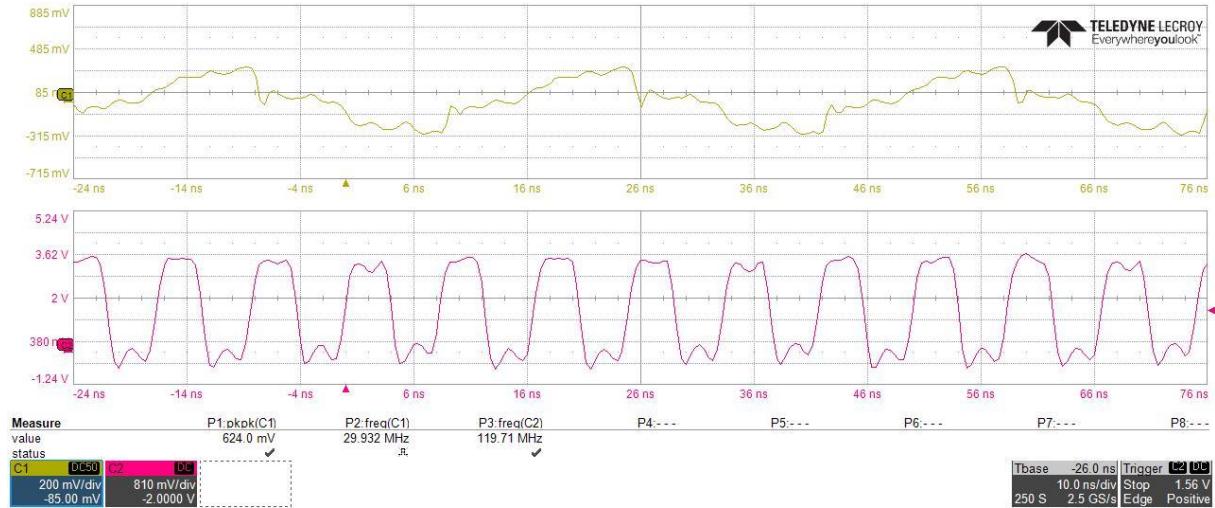


Figure 71 AD9742 testing  $f_{OUT} = 30MHz$ , shape + clock detail

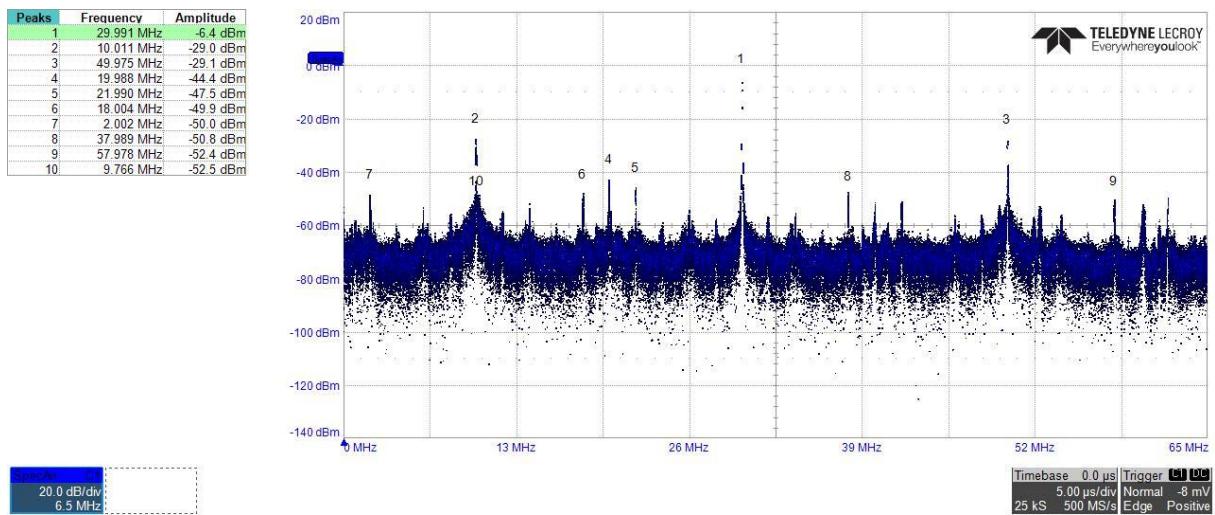


Figure 72 AD9742 testing  $f_{OUT} = 30MHz$ , spectrum detail

Testing  $f_{OUT} = 40\text{MHz}$

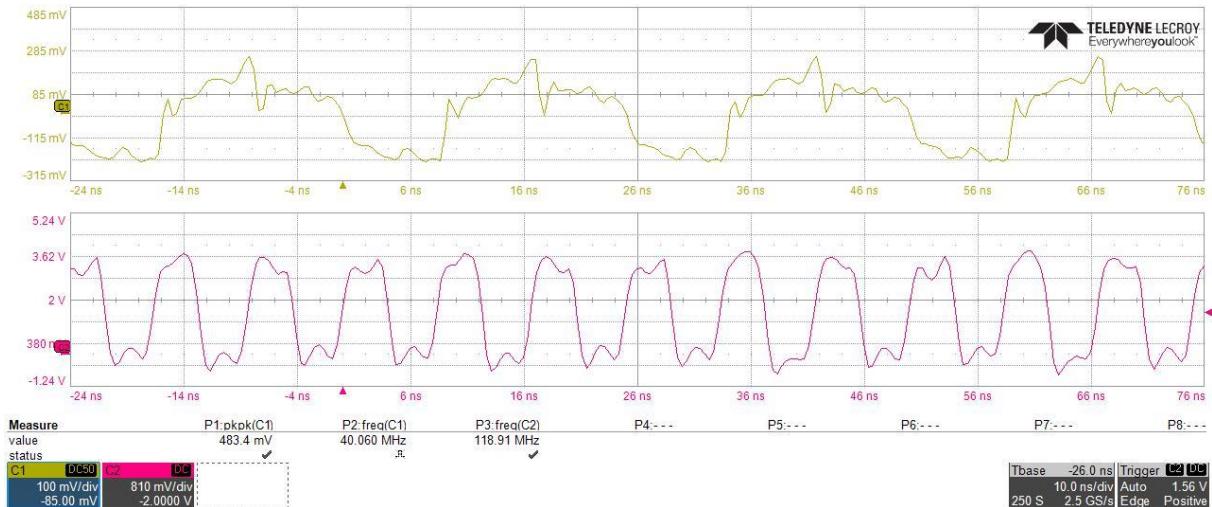


Figure 73 AD9742 testing  $f_{OUT} = 40\text{MHz}$ , shape + clock detail

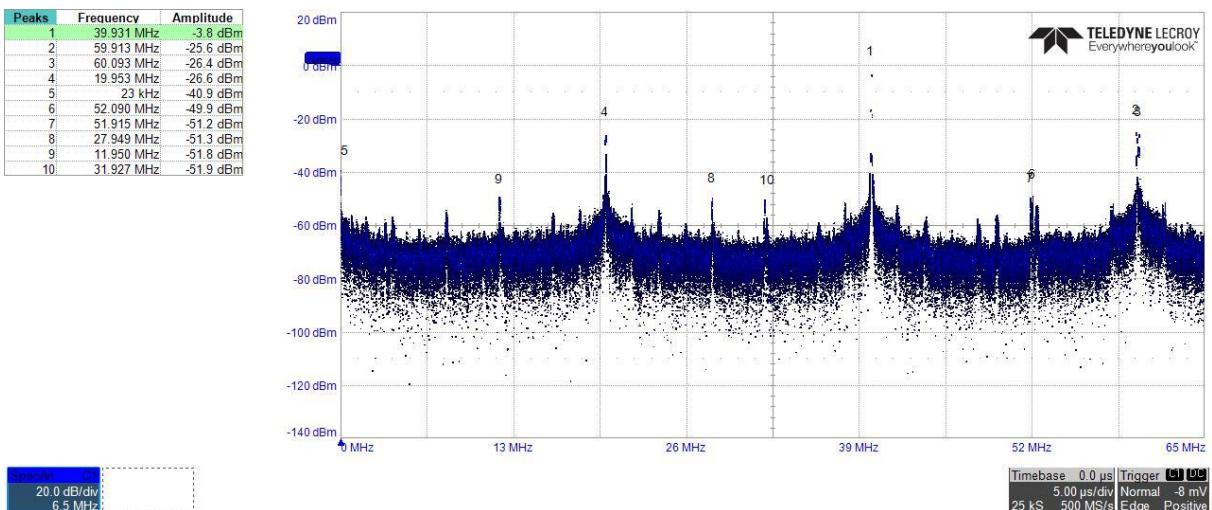


Figure 74 AD9742 testing  $f_{OUT} = 40\text{MHz}$ , spectrum detail

Testing  $f_{OUT} = 50\text{MHz}$

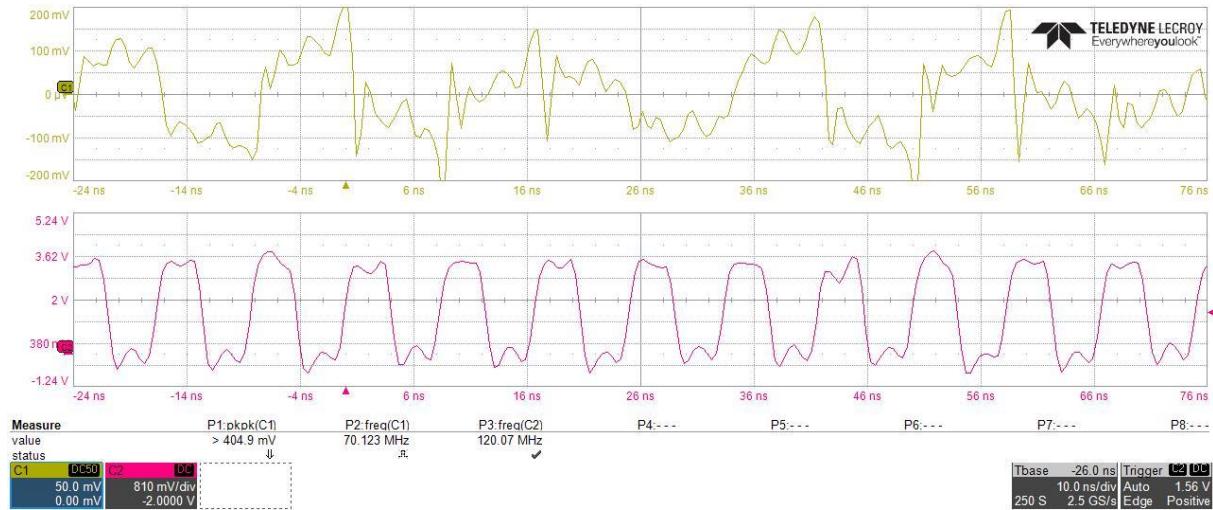


Figure 75 AD9742 testing  $f_{OUT} = 50\text{MHz}$ , shape + clock detail

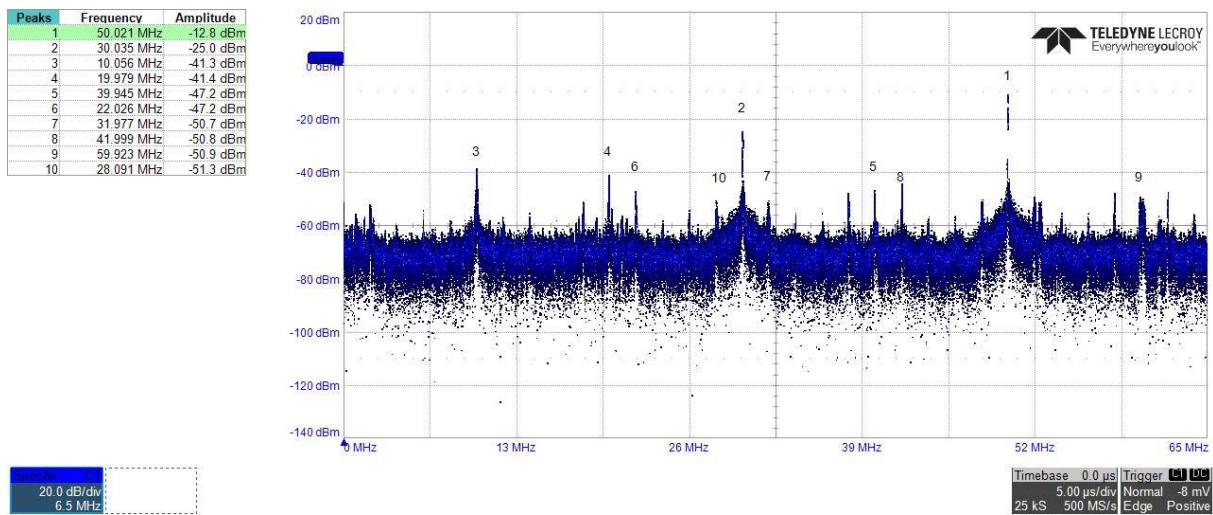


Figure 76 AD9742 testing  $f_{OUT} = 50\text{MHz}$ , spectrum detail

Testing  $f_{OUT} = 60\text{MHz}$

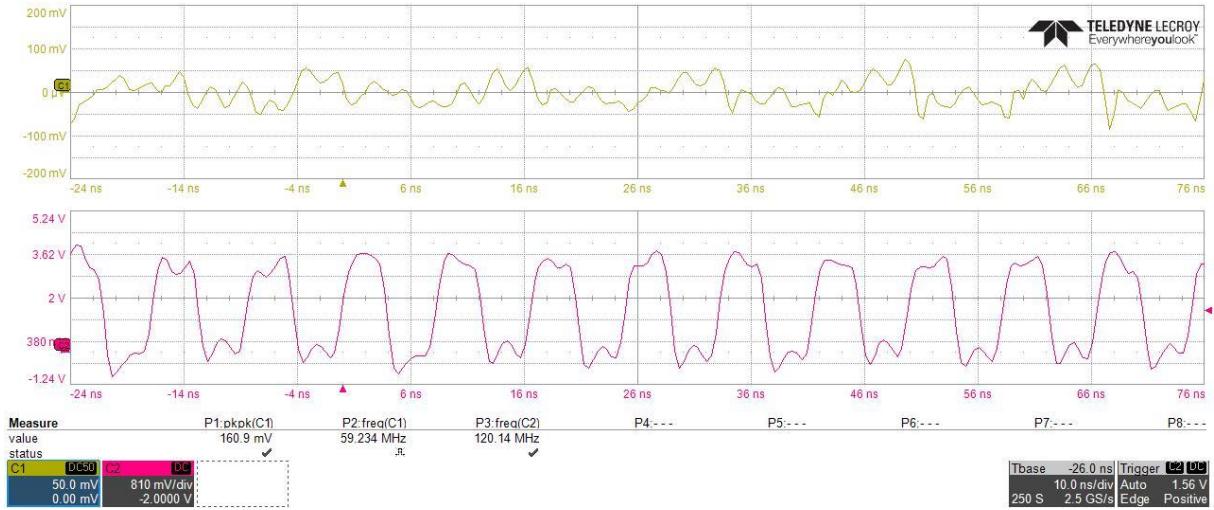


Figure 77 AD9742 testing  $f_{OUT} = 60\text{MHz}$ , shape + clock detail

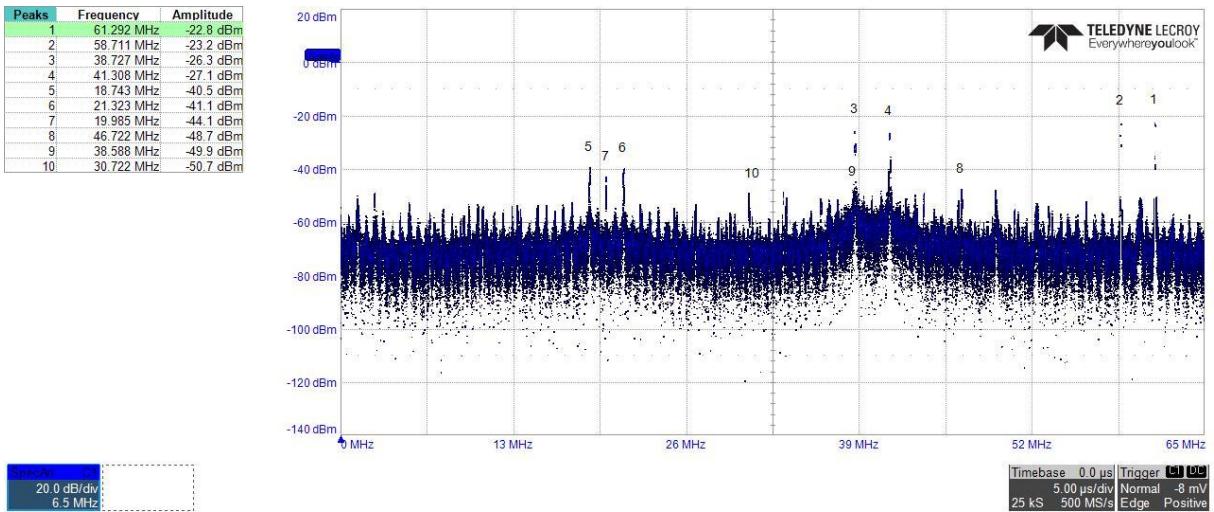


Figure 78 AD9742 testing  $f_{OUT} = 60\text{MHz}$ , spectrum detail

## *Conclusion*

- Expected frequency range 0.250MHz-60MHz
  - Reached for useful operation 0.270MHz-60MHz
  - Lowest tested  $f_{OUT} = 100\text{kHz}$ ,  $V_{PP} = 0.27V_{PP}$
- Maximally amplitude  $0.96V_{PP}$ 
  - Maximally Reached  $0.875V_{PP}$  for  $f_{OUT} = 21\text{MHz}$ 
    - 0.6dB WBC-1TL maximal loss may decrease  $0.96V_{PP}$  down to  $0.84V_{PP}$
  - Useful range 10-40MHz with amplitudes  $0.755V_{PP}$  down to  $0.483V_{PP}$ 
    - Total loss 3dB for 40MHz ( $0.48V_{PP}$ )
    - Total loss 0.9dB for 10MHz ( $0.755V_{PP}$ )
- Low-Pass filter needed
  - SNR enhancement (currently  $\approx 20\text{dB}$ )
  - Signal shape enhancement
- DAC0 AD9742 when feeding the  $50\Omega$  load by maximal 20mA output
  - consumes 44mA current at 5V operation (24mA internal loss)

## AD9742 + WTC-1TL + LOWPASS

Figure 79 depicts the DAC0 AD9742 circuit including the transformer WLC-1TL for single ended operation and the output is finally filtered by the Low-Pass filter. The  $50\Omega$  load represented by measure device (oscilloscope/VNA). The  $f_{\text{OUT}}$  is directly driven by the FPGA DDS. The figure 78 is derived out of [Figure 22](#) with simplified DAC0 symbol. The measured board is photograph of figure 79.

The expected operational behavior for the DDS, DAC0  $f_{\text{CLK}} = 120\text{MHz}$  is:

- Operational frequency: 0.25MHz-60MHz
  - Bottom limit determined by the WBC-1TL  $f_{\text{MIN}} = 0.25\text{MHz}$
  - Upper limit determined by Nyquist theorem and  $f_{\text{CLK}} = 120\text{MHz}$
- Insertion loss of the Low-Pass filter expected
  - Maximally 1.5dB
- Enhanced shape and SNR of the output signal expected
  - SNR expected at least 30dB
- Required low jitter on the single-ended LVCMOS33 FPGA clock line
  - Measured by 1GHz active probe

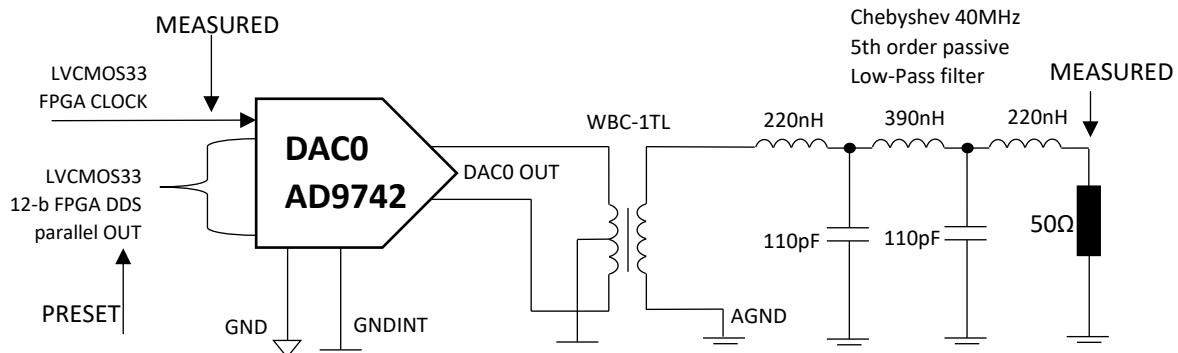


Figure 79 80 DAC0 AD9742 + WLC-1T + Low-Pass testing circuit

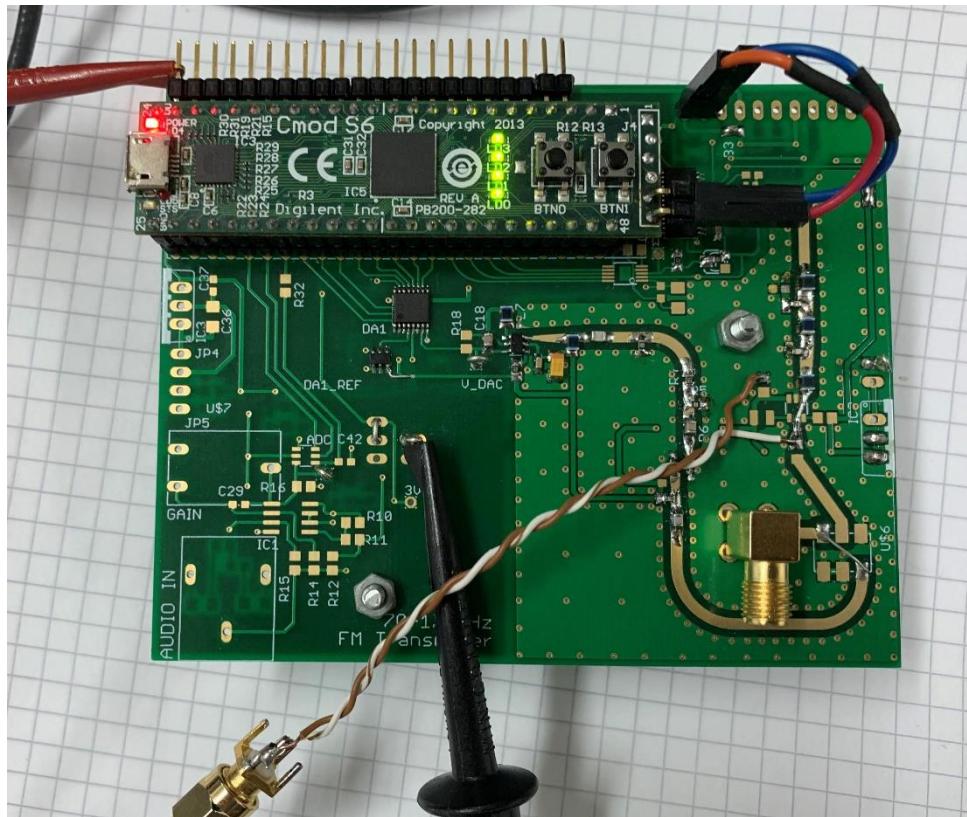


Figure 81 Measurement setup DAC0 AD942 + WLC-1TL + Low-Pass

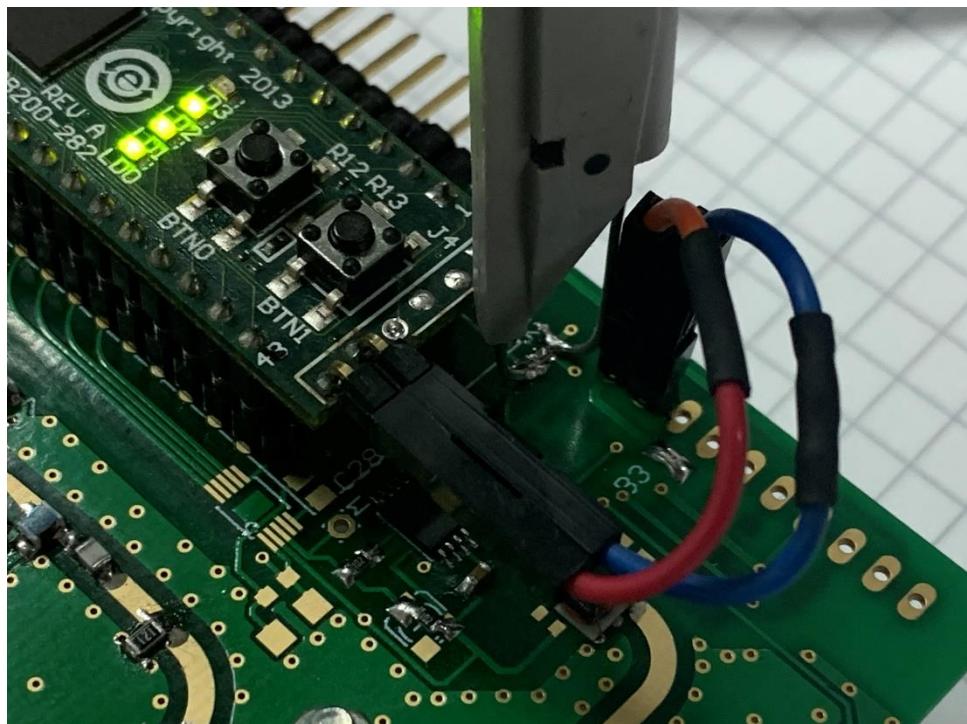


Figure 82 Measurement setup DAC0 AD942 + WLC-1TL + Low-Pass, Active Probe Clock

## Testing $F_{OUT} = 270\text{kHz}$

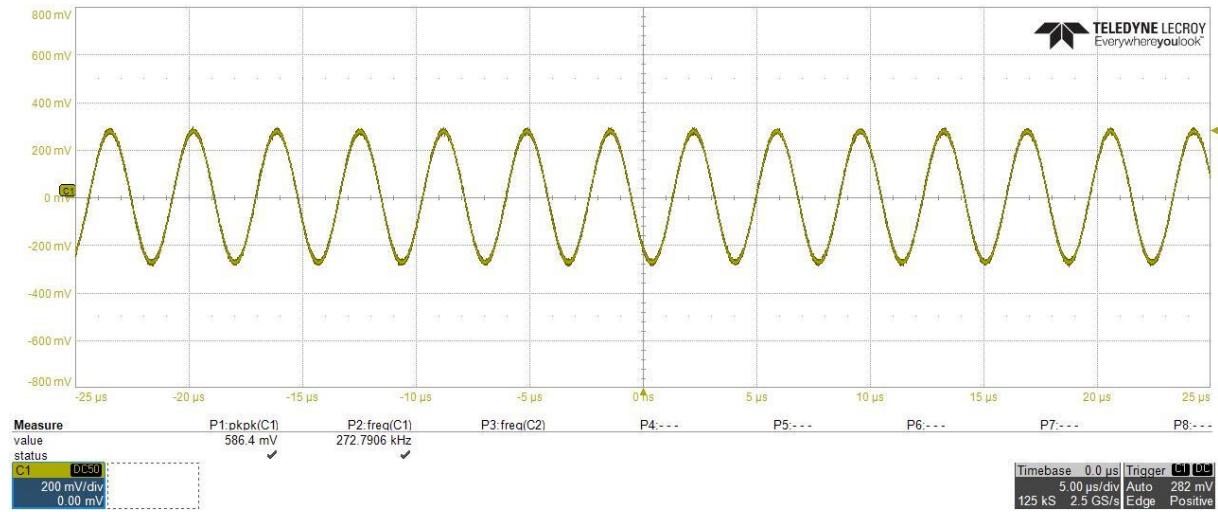


Figure 83 AD9742 + Low-Pass testing  $f_{OUT} = 270\text{kHz}$ , shape detail

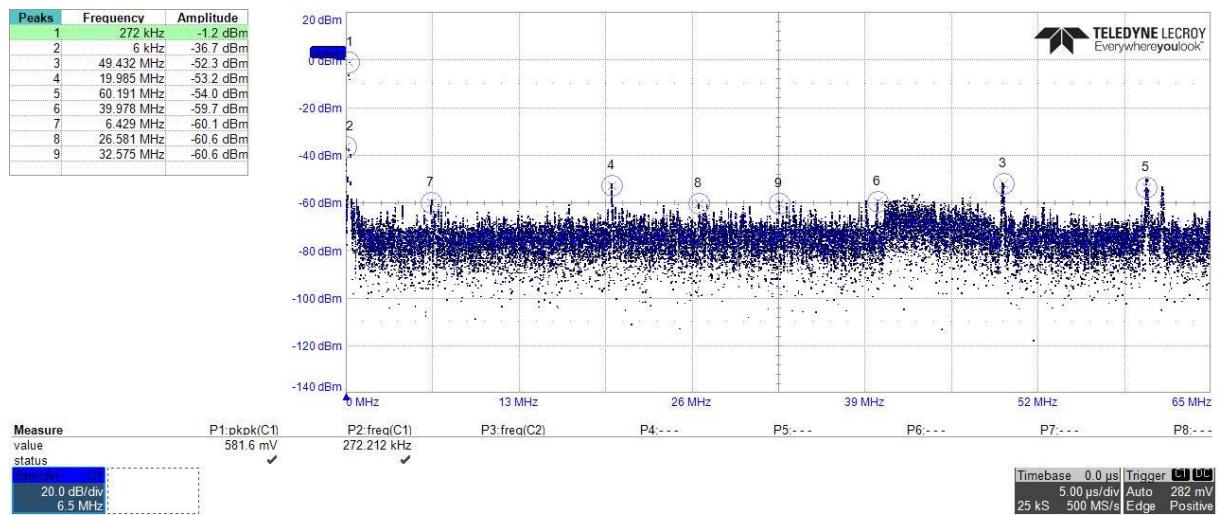


Figure 84 AD9742 + Low-Pass testing  $f_{OUT} = 270\text{kHz}$ , spectrum detail

Testing  $f_{OUT} = 2.5\text{MHz}$

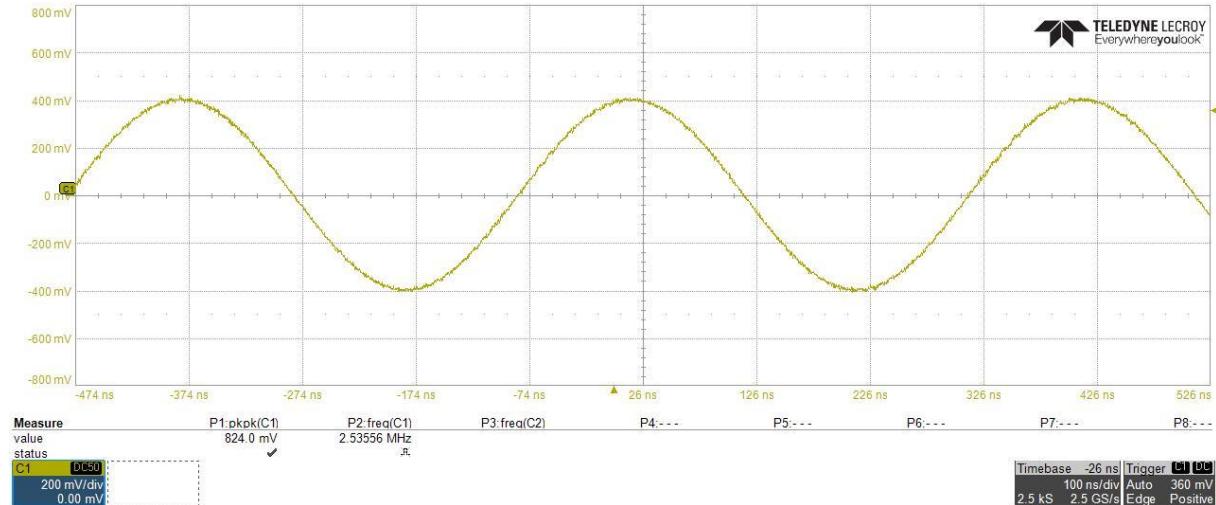


Figure 85 AD9742 + Low-Pass testing  $f_{OUT} = 2.5\text{MHz}$ , shape detail

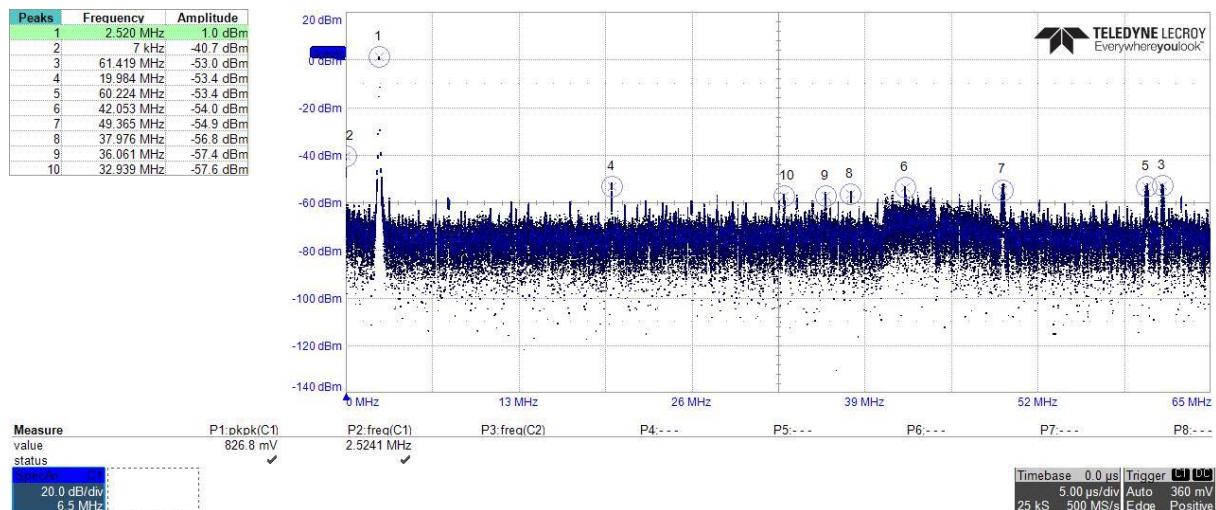


Figure 86 AD9742 + Low-Pass testing  $f_{OUT} = 2.5\text{MHz}$ , spectrum detail

## Testing $F_{OUT} = 10MHz$

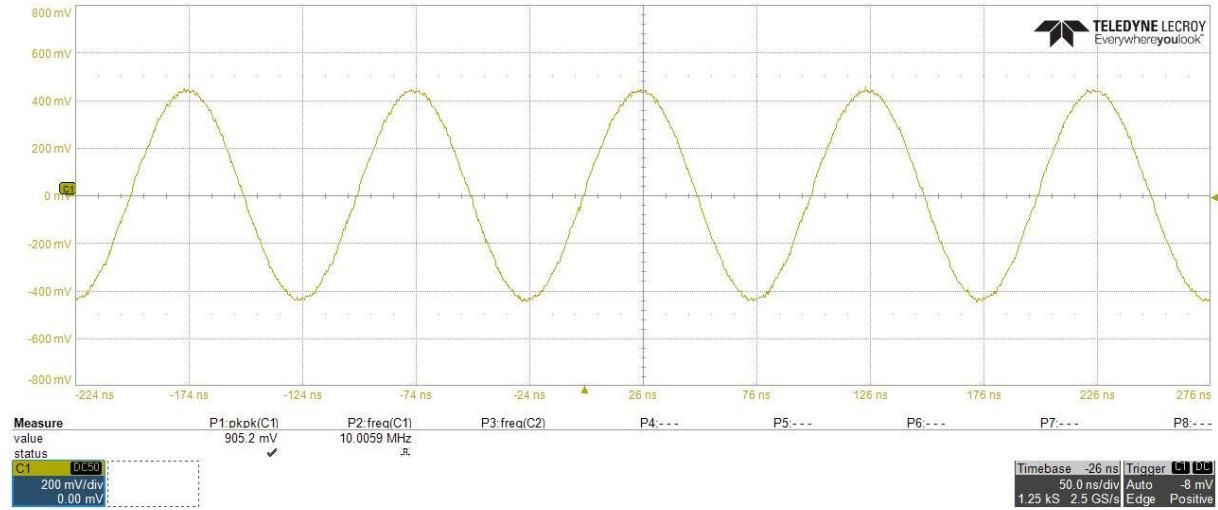


Figure 87 AD9742 + Low-Pass testing  $f_{OUT} = 10MHz$ , shape detail

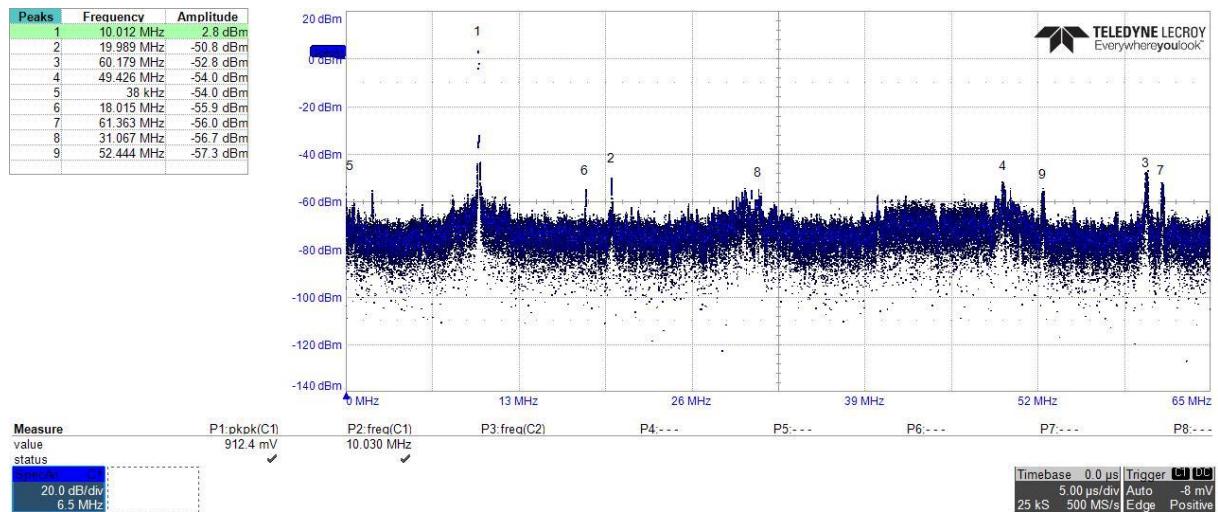


Figure 88 AD9742 + Low-Pass testing  $f_{OUT} = 10MHz$ , spectrum detail

## Testing $f_{OUT} = 20\text{MHz}$

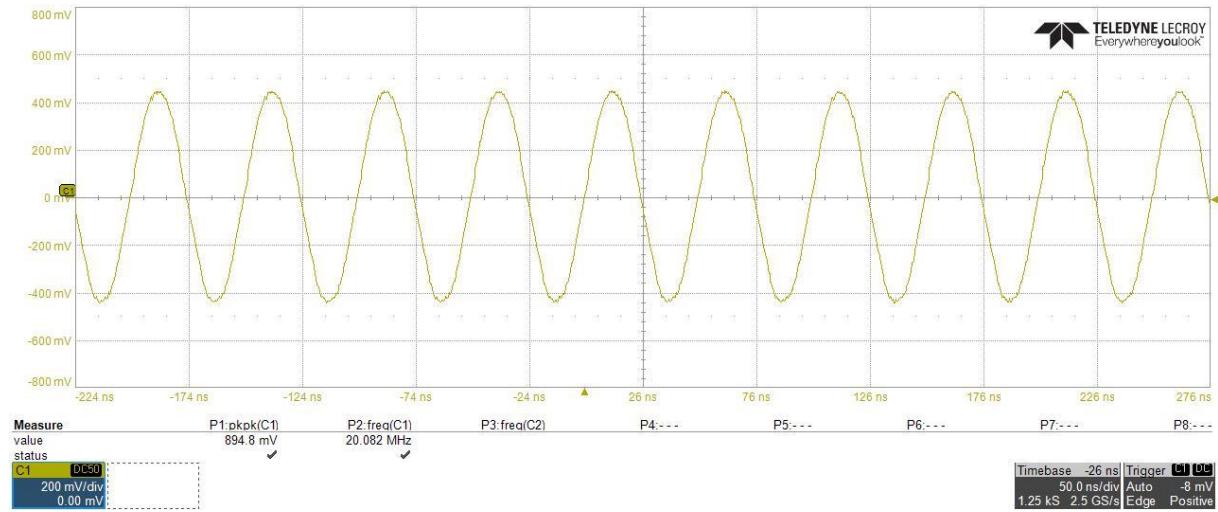


Figure 89 AD9742 + Low-Pass testing  $f_{OUT} = 20\text{MHz}$ , shape detail

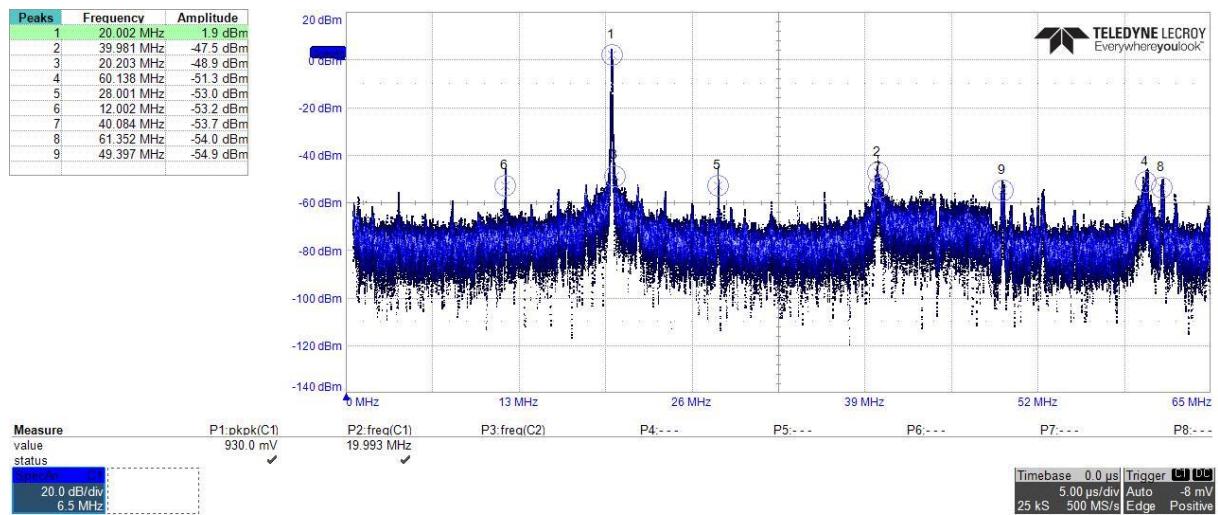


Figure 90 AD9742 + Low-Pass testing  $f_{OUT} = 20\text{MHz}$ , spectrum detail

Testing  $f_{OUT} = 30MHz$

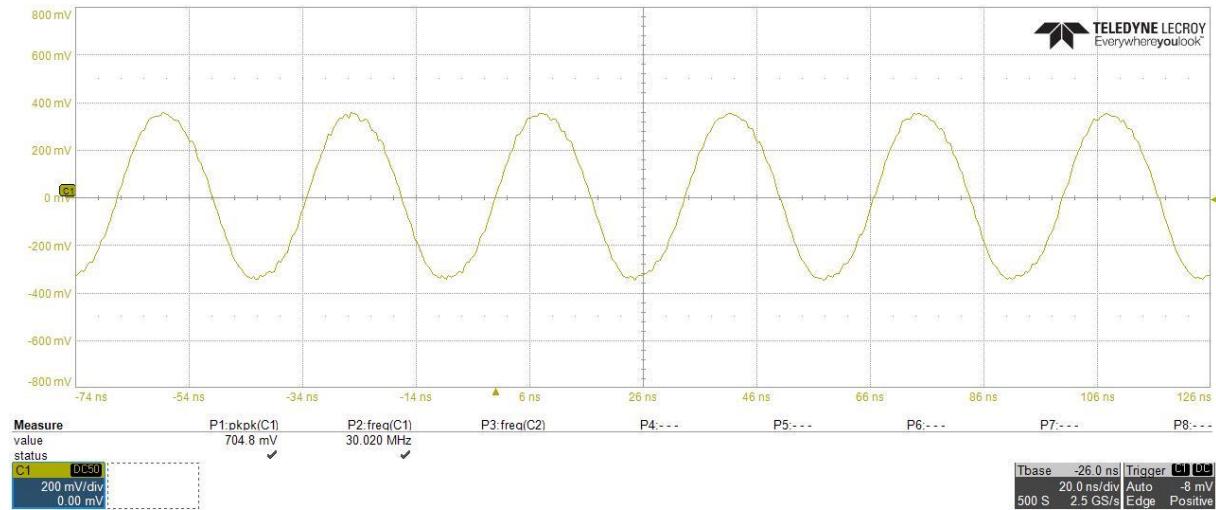


Figure 91 AD9742 + Low-Pass testing  $f_{OUT} = 30MHz$ , shape detail

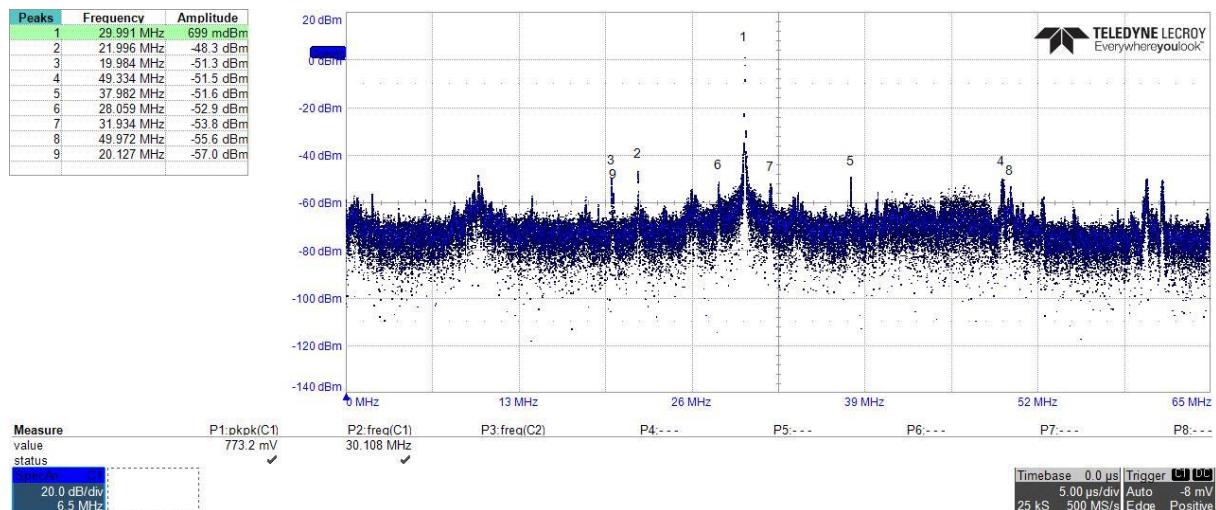


Figure 92 AD9742 + Low-Pass testing  $f_{OUT} = 30MHz$ , spectrum detail

Testing  $f_{OUT} = 40MHz$

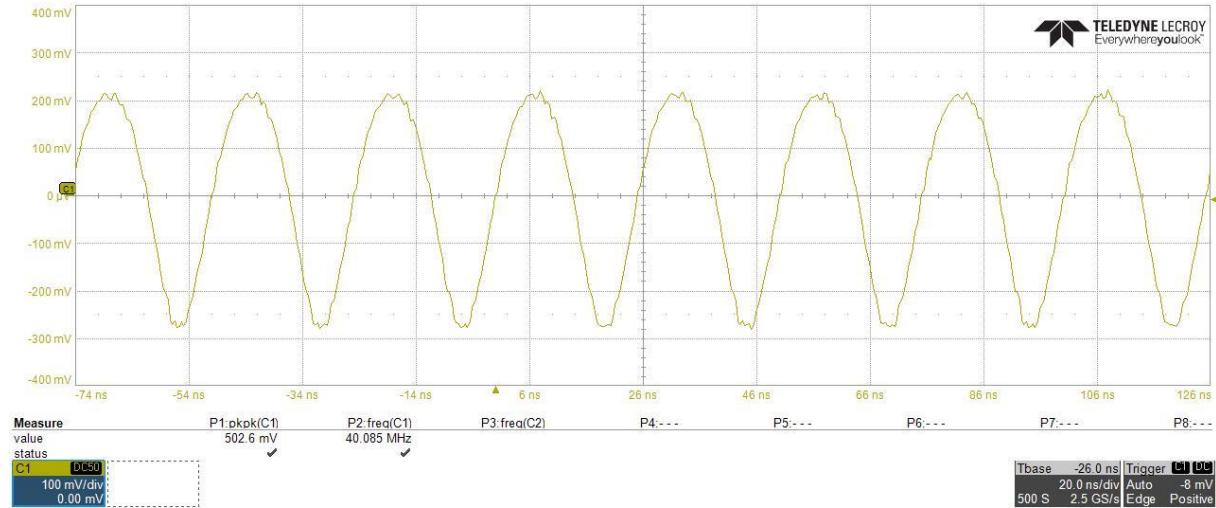


Figure 93 AD9742 + Low-Pass testing  $f_{OUT} = 40MHz$ , shape detail

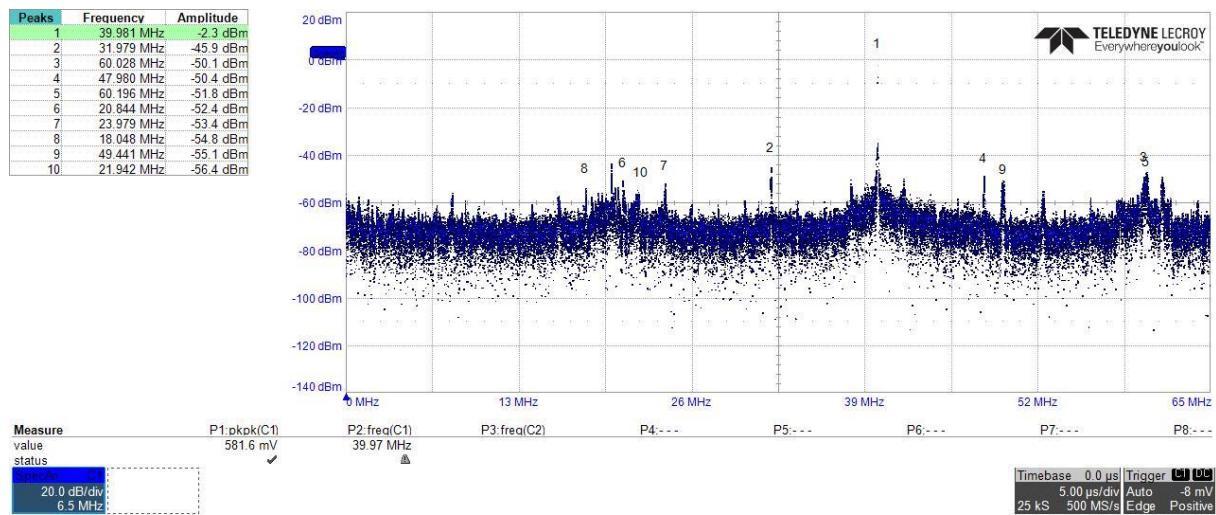


Figure 94 AD9742 + Low-Pass testing  $f_{OUT} = 40MHz$ , spectrum detail

Testing  $f_{OUT} = 50\text{MHz}$

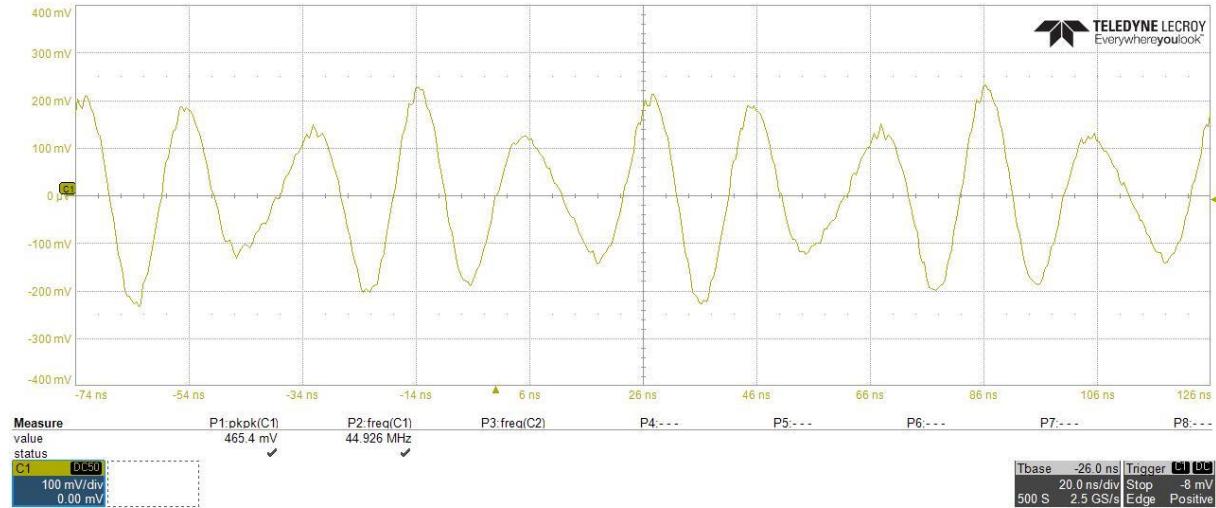


Figure 95 AD9742 + Low-Pass testing  $f_{OUT} = 50\text{MHz}$ , shape detail

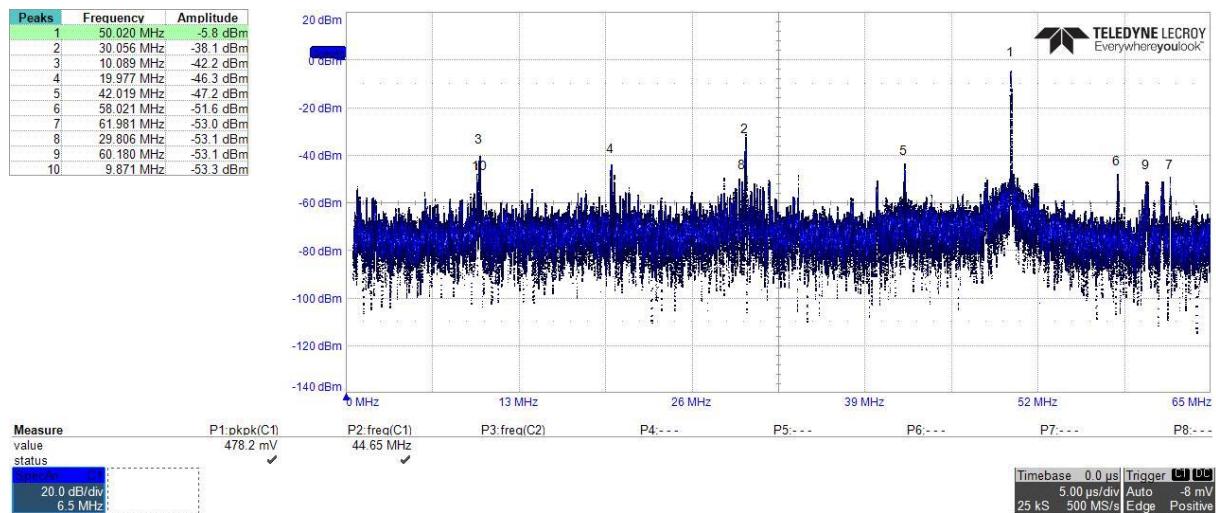


Figure 96 AD9742 + Low-Pass testing  $f_{OUT} = 50\text{MHz}$ , spectrum detail

Testing  $f_{OUT} = 60MHz$

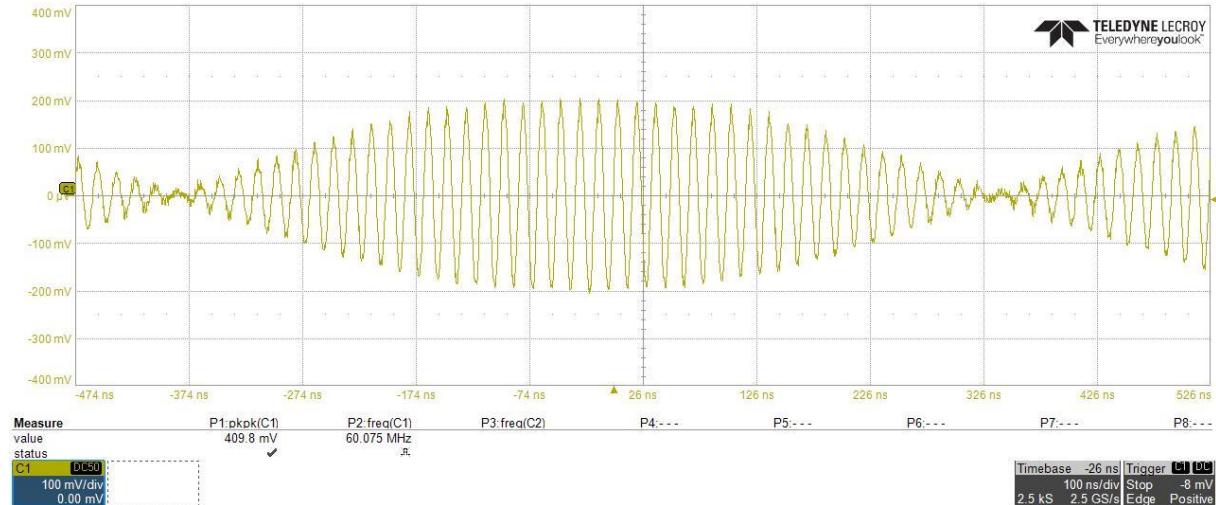


Figure 97 AD9742 + Low-Pass testing  $f_{OUT} = 60MHz$ , shape detail

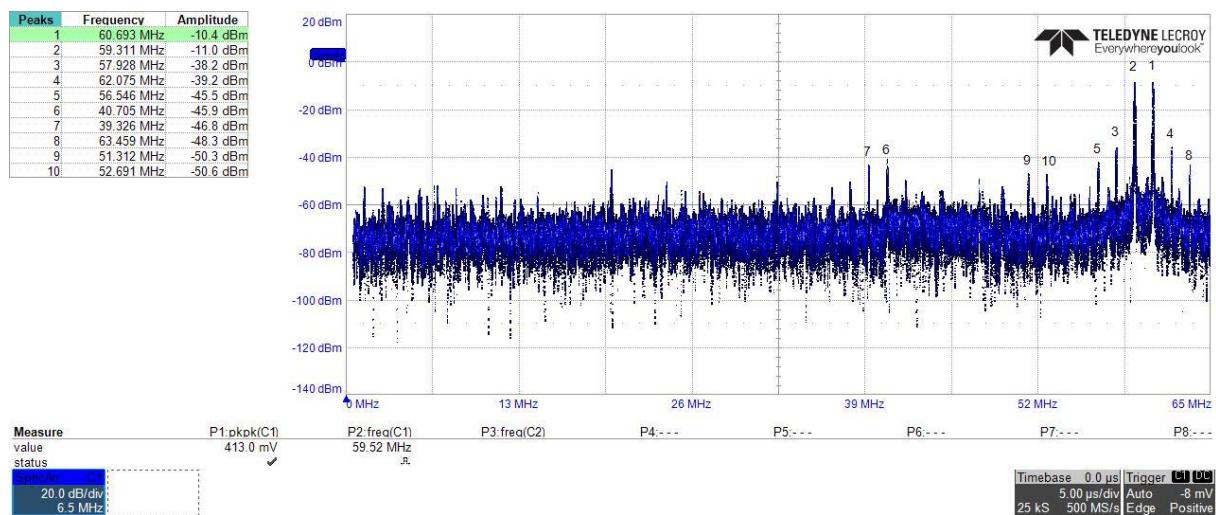


Figure 98 AD9742 + Low-Pass testing  $f_{OUT} = 60MHz$ , spectrum detail

Extra: DAC0 aliasing  $f_{OUT} = 63.4, 56.4\text{MHz}$ , when  $f_{CLK} = 120\text{MHz}$

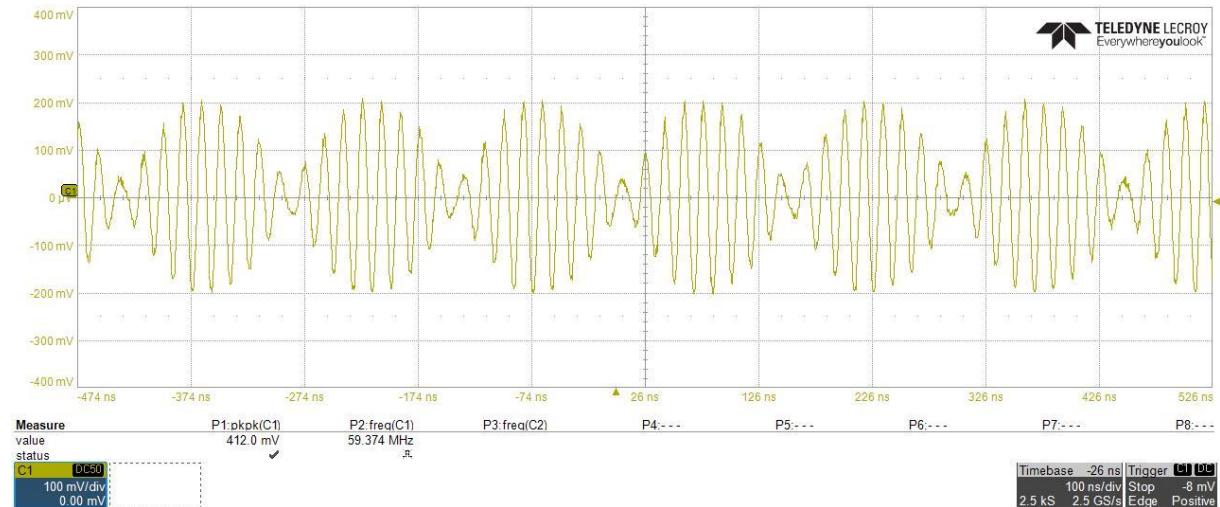


Figure 99 AD9742 + Low-Pass testing  $f_{OUT} = 63.4\text{MHz} + 56.4\text{MHz}$ ,  $f_{clk} = 120\text{MHz}$ , aliasing detail

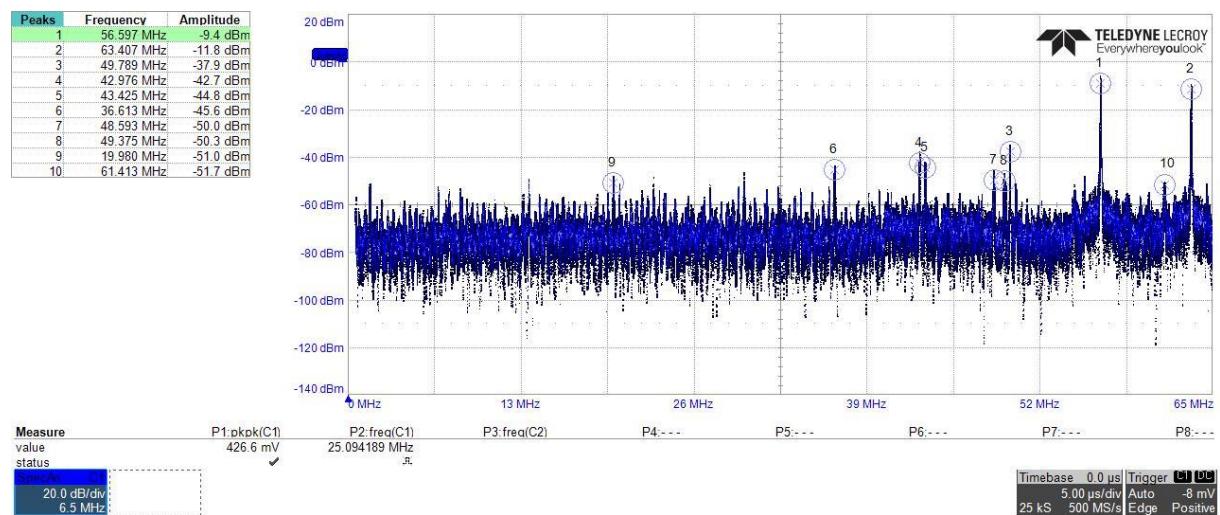


Figure 100 AD9742 + Low-Pass testing  $f_{OUT} = 63.4\text{MHz} + 56.4\text{MHz}$ ,  $f_{clk} = 120\text{MHz}$ , aliasing detail

## DAC0 LVCMOS33 Clock

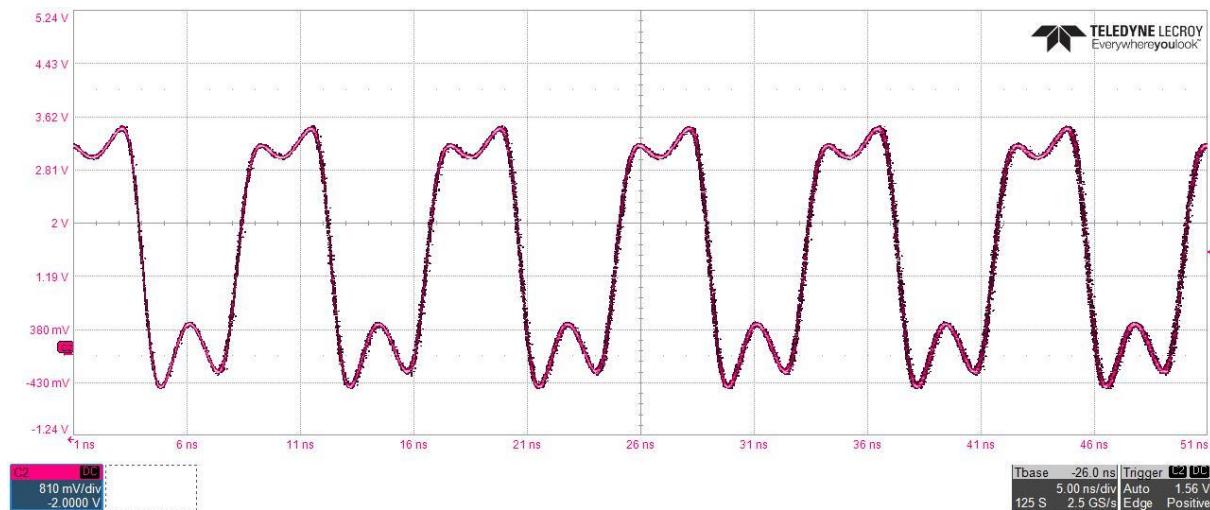


Figure 101 AD9742 + Low-Pass testing,  $f_{out} = 0\text{MHz}$  – no DAC0 DB11-DB00, 120MHz clock detail

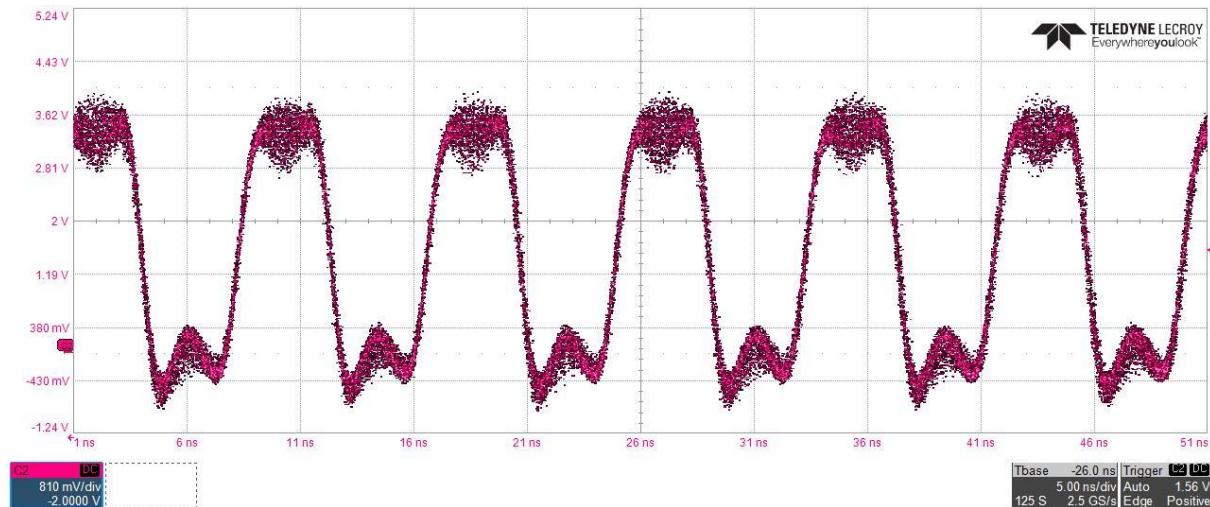


Figure 102 AD9742 + Low-Pass testing, DAC0 DB11-DB00 for  $f_{out} = 21\text{MHz}$ , 120MHz clock detail

## *Conclusion*

- Expected frequency range 0.250MHz-60MHz
  - Reached for useful operation 0.270MHz-60MHz
  - Lowest tested  $f_{OUT} = 120\text{kHz}$ ,  $V_{PP} = 0.38V_{PP}$
  - Meets requirement 4: The VHF-Transmitter shall feature with selectable FM broadcast channel within 88-108MHz.
- Maximally amplitude 0.96V<sub>PP</sub>
  - Maximally Reached 0.905V<sub>PP</sub> for  $f_{OUT} = 10\text{MHz}$ 
    - 0.6dB WBC-1TL maximal loss may decrease 0.96V<sub>PP</sub> down to 0.84V<sub>PP</sub>
  - Useful range 10-40MHz with amplitudes 0.902V<sub>PP</sub> down to 0.502V<sub>PP</sub>
    - Total loss 2.8dB for 40MHz (0.502V<sub>PP</sub>)
    - Total loss 0.2dB for 10MHz (0.902V<sub>PP</sub>)
  - Overall higher output voltage due to filtering unneeded product
- Output signal power
  - +2dBm 10MHz
  - -2.3dBm 40MHz
- Low-Pass filter improved SNR and shape
  - SNR enhancement (currently 38dB up to 51dB)
  - Signal shape enhancement from all the figures
- No consumption increase observed
- No significant influence of the operational on the CLOCK jitter,  
however observable difference for rail settled square areas (Figure 101, 102)

# Passive frequency mixer

Refer to [Figure 5](#), the mixer is frequency adder of the carrier signal path and the Modulation signal path. Also, the mixer is last part placed on the board of the basic transmitting chain. All the rest optional circuits such as the Band-Pass filter, the Cascaded amplifier and the Antenna are modules outside the board. Usage of the mixer is straightforward, only correct frequencies and power levels shall be according to the specifications.

## Mixer standalone test

As the mixer ADE-1L+ has specified only LO power level and maximal operating settings [7], the best approach to determine the appropriate IF (or RF) power level is test measurement. Just remind that the mixer is intended to operate as upconverter.

Unfortunately, only AWG with maximal  $f_{MAX} = 30\text{MHz}$  was available, what cannot simulate conditions for the VHF-Transmitter:

- LO (carrier signal path) 69-83MHz
- IF (modulation signal path) 10-40MHz

As the ration between desired LO and IF is circa 3:1, simulation of the same frequency ratio regards to generator  $f_{MAX}$ , may at least approximate mixer operational point:

- LO 30MHz
- IF 9 MHz

The ADE-1L+ is soldered directly on universal PCB with SMA connectors like shown in Figure 103. The goal of the test measurement is to find the ratio between LO and IF power, which results in high RF output power and low spurs.

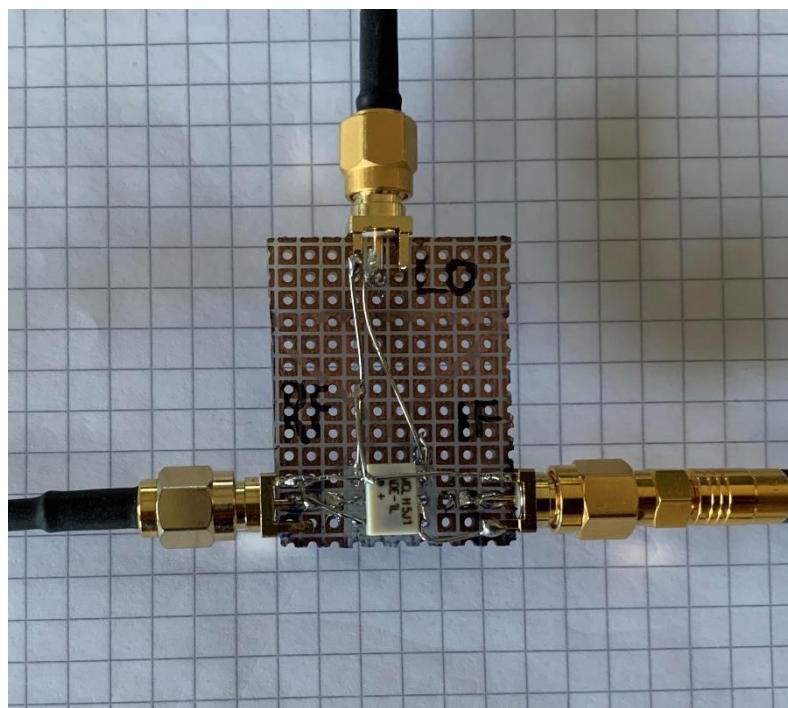


Figure 103 Testing ADE+1L mixer photograph

### Sweep IF ADE-1L+, LO +3dBm, IF -5dBm

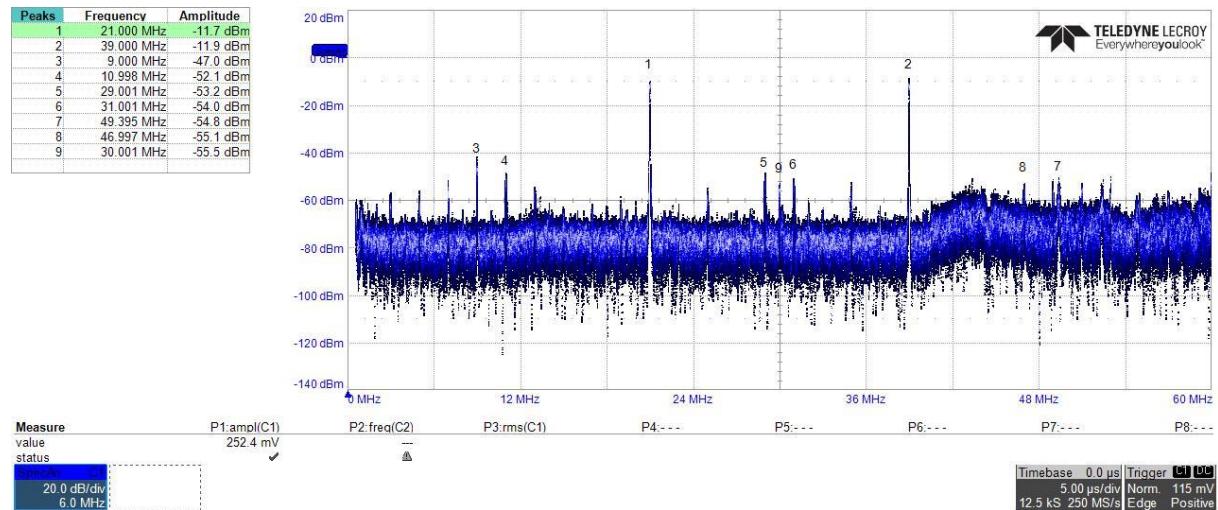


Figure 104 Testing ADE-1L+, LO +3dBm 30MHz, IF -5dBm 9MHz

### Sweep IF ADE-1L+, LO +3dBm, IF -3dBm

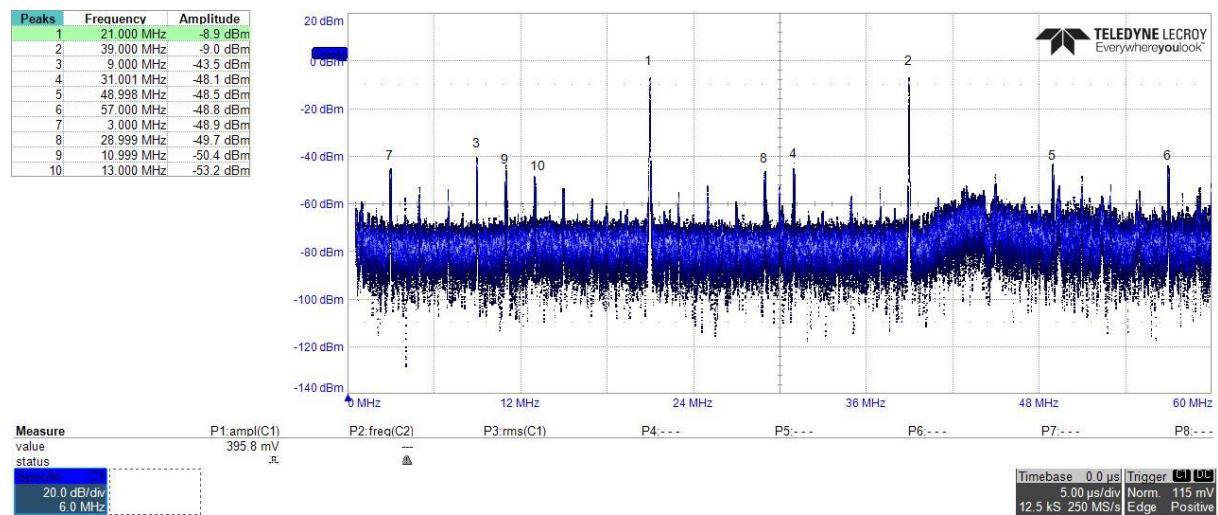


Figure 105 Testing ADE-1L+, LO +3dBm 30MHz, IF -3dBm 9MHz

## Sweep IF ADE-1L+, LO +3dBm, IF 0dBm

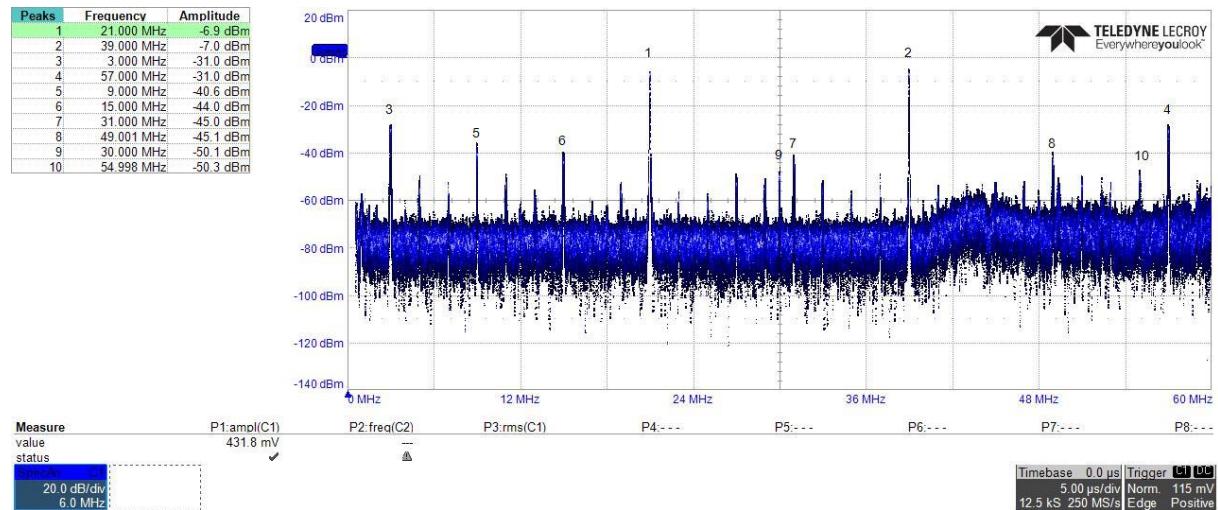


Figure 106 Testing ADE-1L+, LO +3dBm 30MHz, IF 0dBm 9MHz

## Sweep IF ADE-1L+, LO +3dBm, IF +2dBm

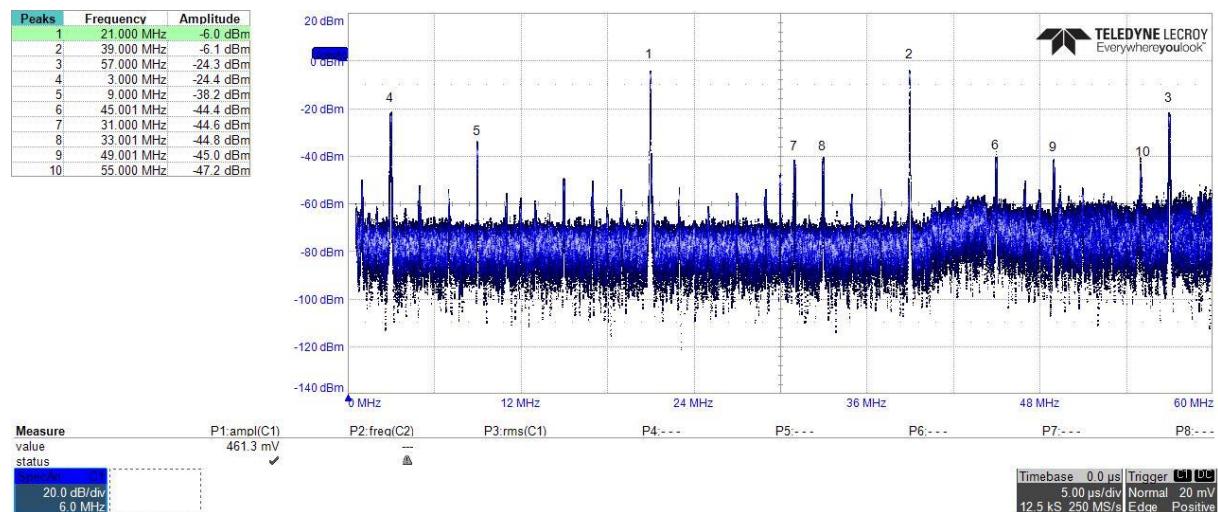


Figure 107 Testing ADE-1L+, LO +3dBm 30MHz, IF +2dBm 9MHz

### Sweep IF ADE-1L+, LO +3dBm, IF +3dBm

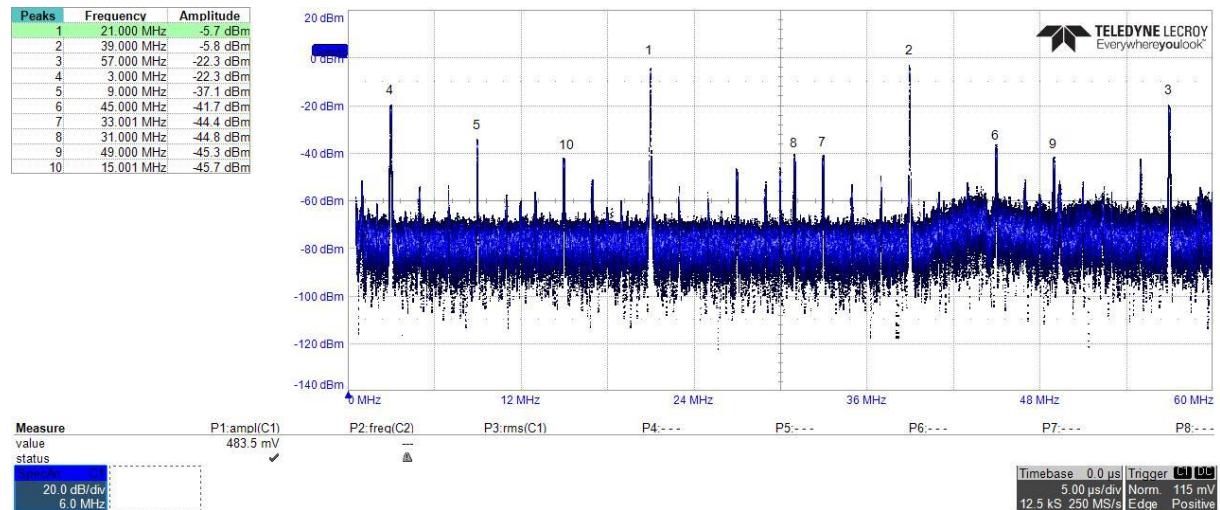


Figure 108 Testing ADE-1L+, LO +3dBm 30MHz, IF +3dBm 9MHz

### Sweep IF ADE-1L+, LO +3dBm, IF +3dBm

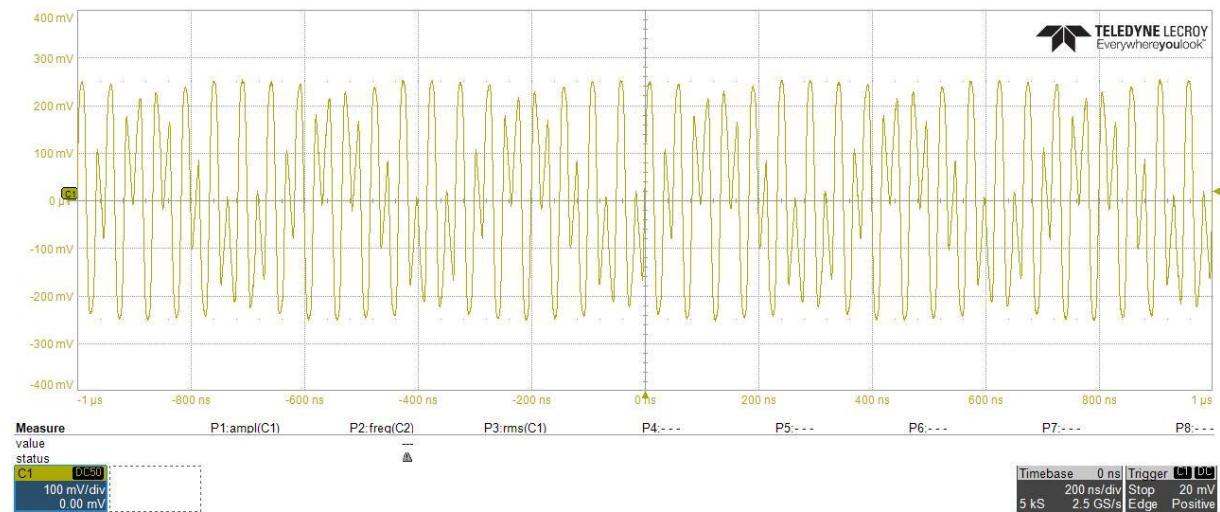


Figure 109 Testing ADE-1L+, LO +3dBm 30MHz, IF +3dBm 9MHz, shape

### Sweep IF ADE-1L+, LO +3dBm, IF +5dB

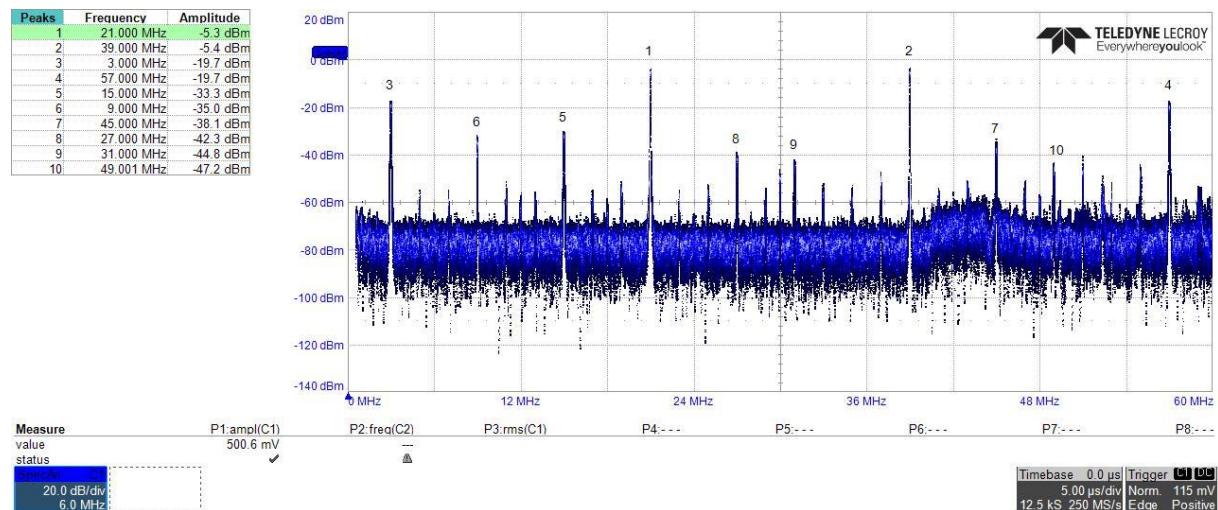


Figure 110 Testing ADE-1L+, LO +3dBm 30MHz, IF +3dBm 9MHz

### Sweep LO ADE-1L+, LO -5dBm, IF +2dBm

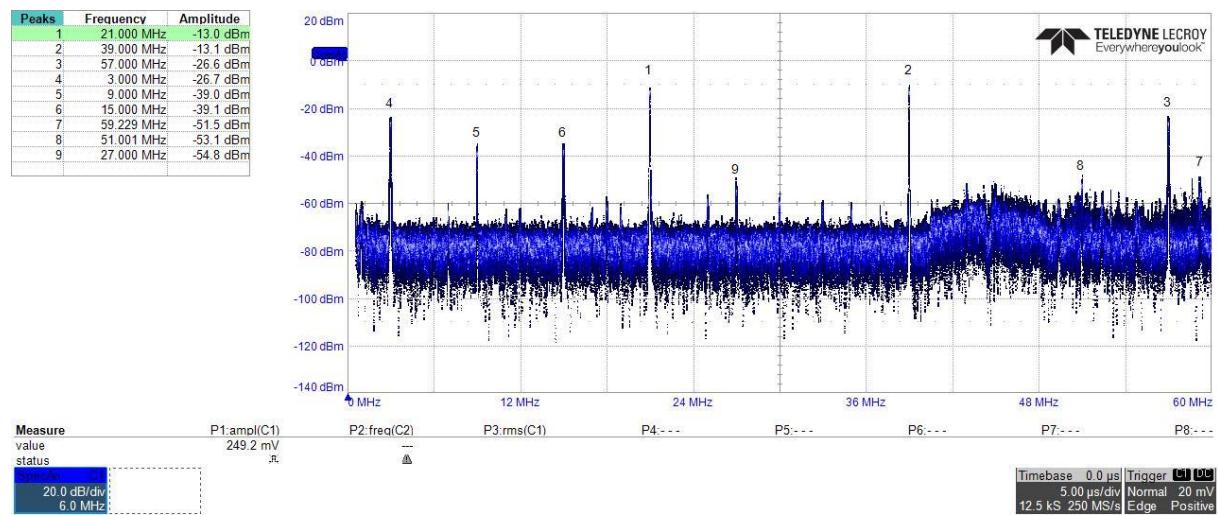


Figure 111 Testing ADE-1L+, LO -5dBm 30MHz, IF +2dBm 9MHz

*Sweep LO ADE-1L+, LO -3dBm, IF +2dBm*

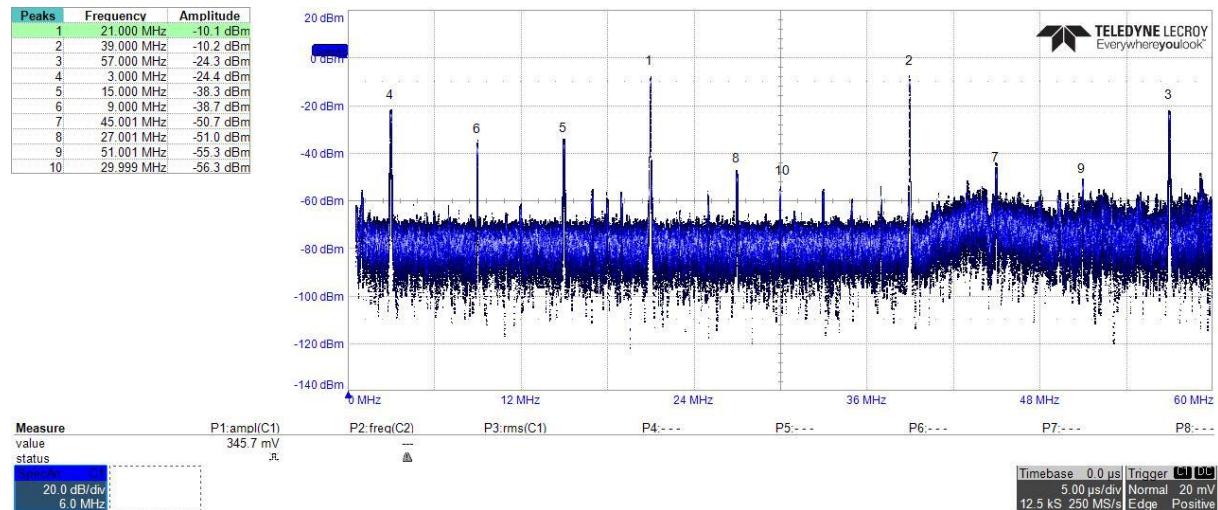


Figure 112 Testing ADE-1L+, LO -3dBm 30MHz, IF +2dBm 9MHz

*Sweep LO ADE-1L+, LO 0dBm, IF +2dBm*

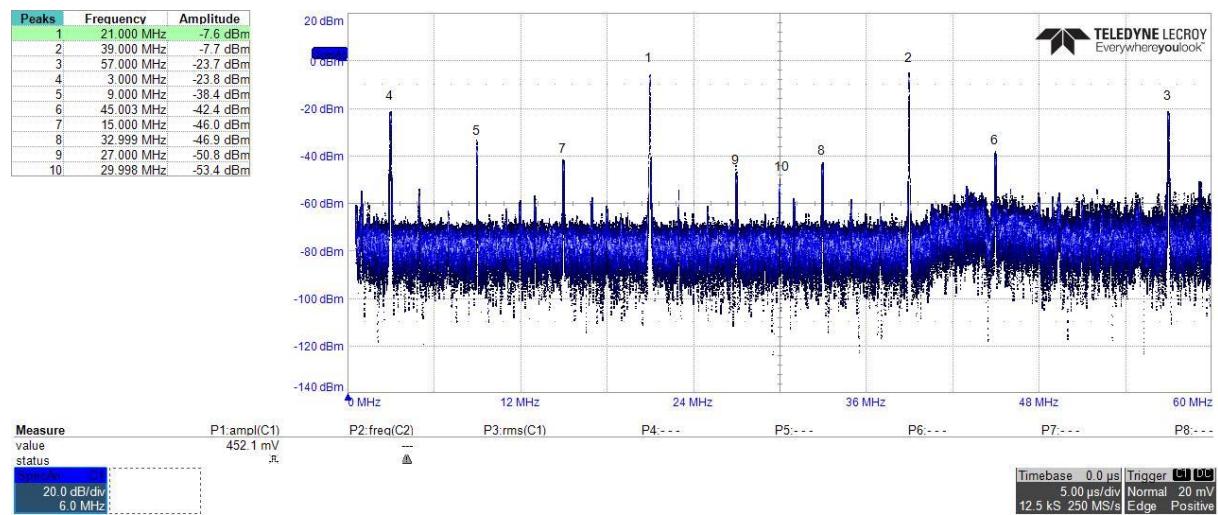


Figure 113 Testing ADE-1L+, LO 0dBm 30MHz, IF +2dBm 9MHz

Sweep LO ADE-1L+, LO +5dBm, IF +2dBm

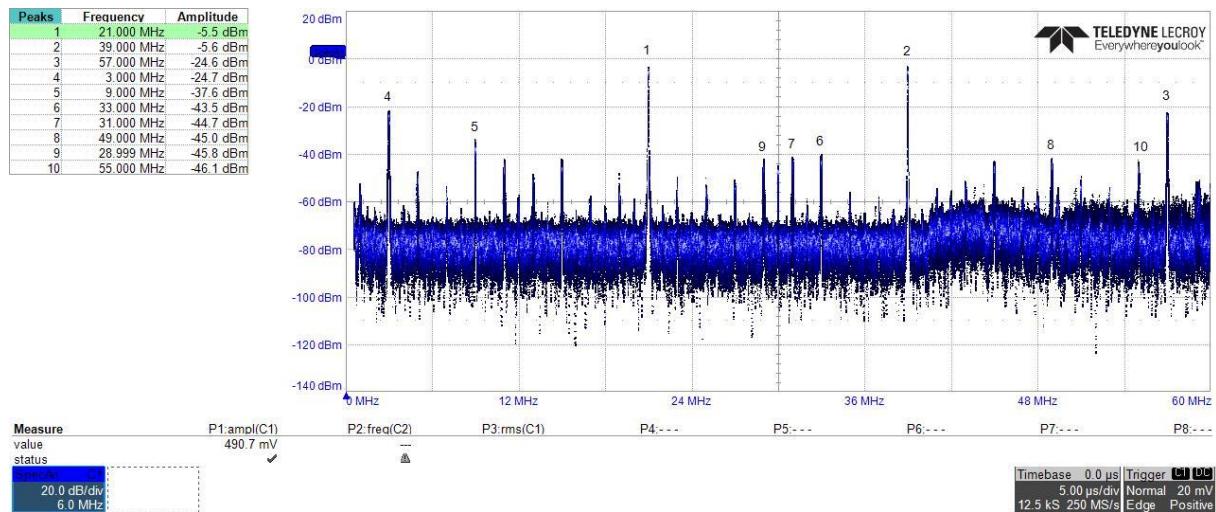


Figure 114 Testing ADE-1L+, LO 5dBm 30MHz, IF +2dBm 9MHz

## Conclusion

- Expected best operation for LO +3dBm
  - Evaluated in further points
- Lower is the IF level, lower spurs
  - LO +3dBm, IF -5dBm results in -12dBm output mirror frequencies and -47dBm spurs
    - IF -5dBm for the Modulation signal path may be easily reached by reducing the size of samples going out of the DDS (software implementation of amplitude adjustment)
- Higher is the IF level, higher spurs
  - LO -5dBm, IF +2dBm results in -13dBm output frequencies and -27dBm spurs
- The output power RF increases linearly only to certain level of the IF power
  - LO +3dBm, IF -3dBm results in -9dBm output mirror frequencies
  - LO +3dBm, IF 0dBm results in -7dBm output mirror frequencies
  - LO +3dBm, IF +2dBm results in -5.7dBm output mirror frequencies
  - LO +3dBm, IF +5dBm results in -5.3dBm output mirror frequencies
- The LO power level shall be fixed +3dBm, meanwhile the IF power level shall be adjustable to reach suppressed side spurs, maximal output power or mutual trade-off

Mixer for the Carrier and Modulation signal path

Upon the observation from the subchapter Mixer standalone testing may be chosen correct IF power level for optimal operation. The mixer testing circuit is simplified as the carrier signal path and modulation signal path were tested in previous chapters. The Figure 115 depicts the final testing schematic and as the  $50\Omega$  is meant measure device (oscilloscope/VNA).

- Frequency levels measured +2.5dBm estimated power level
    - LO 70MHz
    - IF 21.1MHz

However, the LO frequency as well as the IF frequency is adjustable, so it is subject of further investigation to find sweet spot to reach optimal power and low spurs for desired FM broadcast channels. Also, the IF (modulation signal path) signal amplitude and thus power is adjustable unlikely the LO power is fixed. The measurement setup is shown in Figure 116.

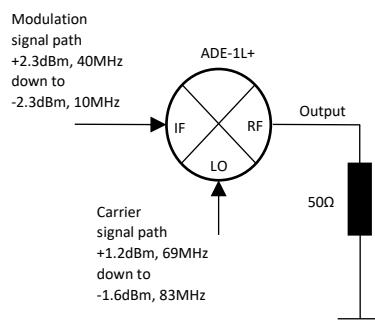
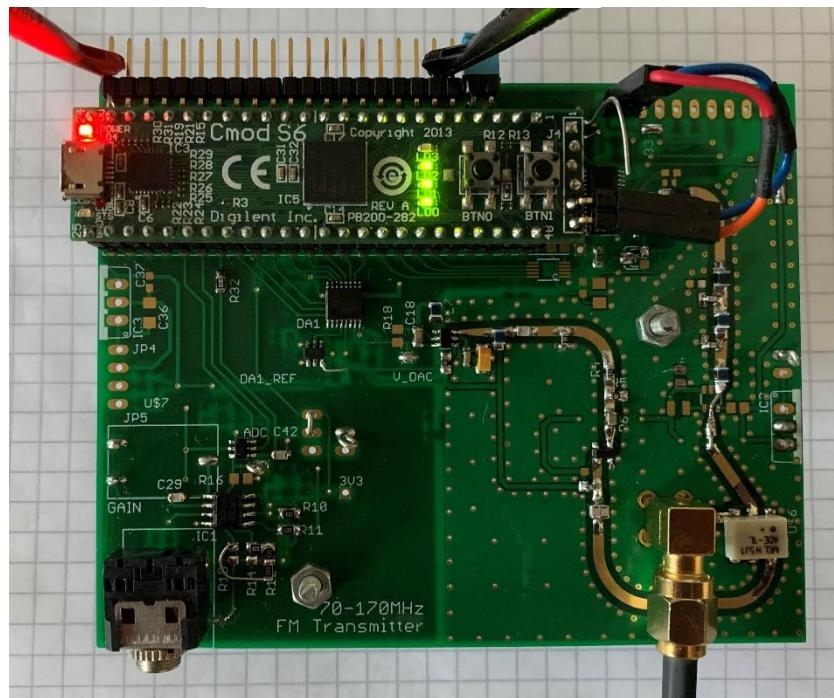


Figure 115 ADE+1L- testing circuit



*Figure 116 Measurement setup ADE-1L+*

Testing LO = +2dBm at 71.4MHz, IF +2dBm at 21MHz

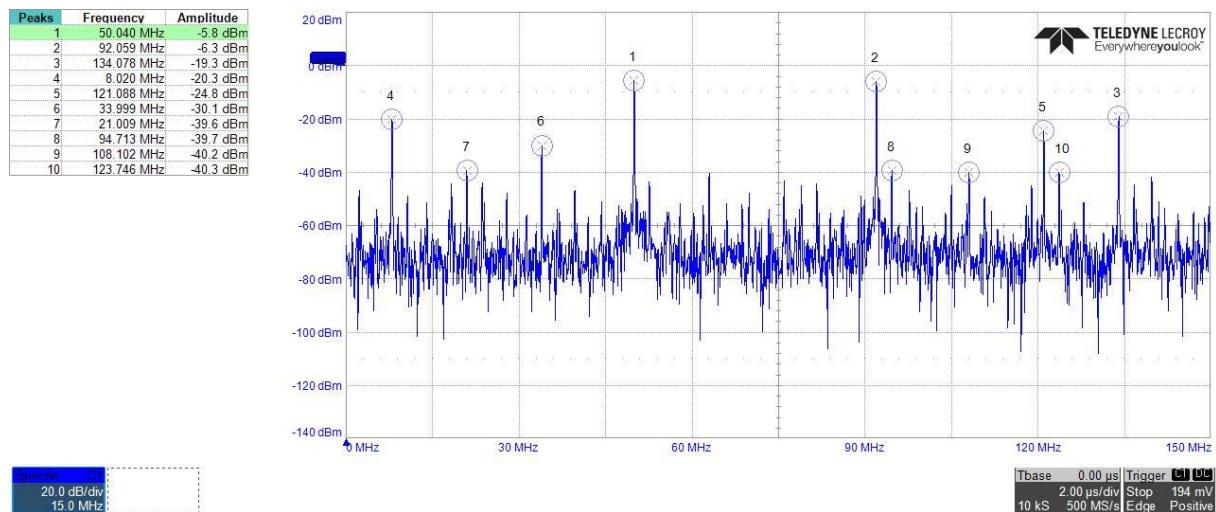


Figure 117 Testing ADE-1L+, spectrum (visible mirror frequencies)

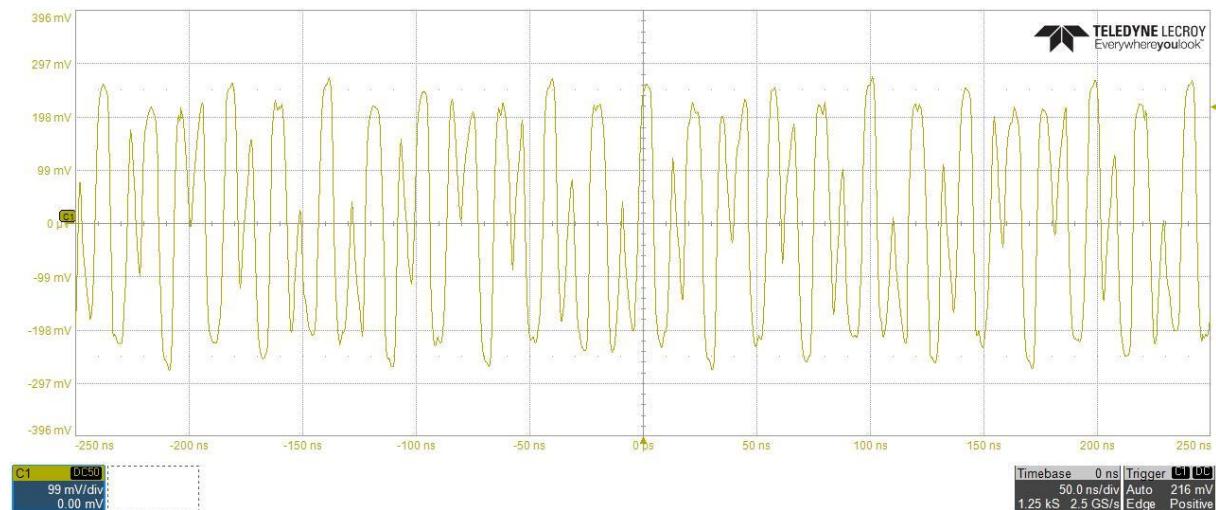


Figure 118 Testing ADE-1L+, shape detail (obvious mirror frequencies)

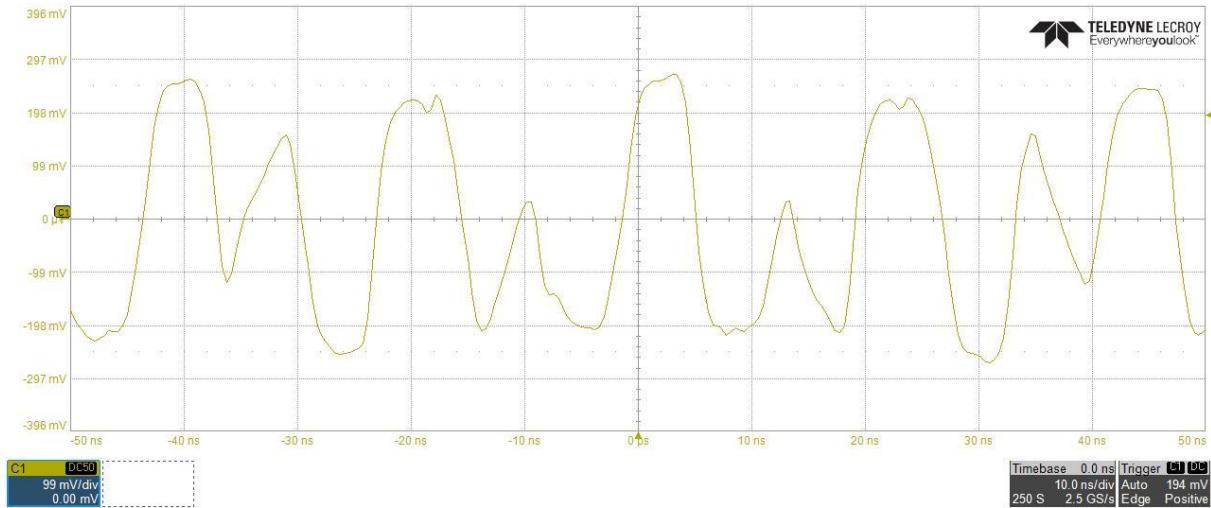


Figure 119 Testing ADE-1L+, shape more detail

## Conclusion

- Mixer signal power reached -6.3dB for desired frequency 91.4 MHz
- Mixer has obvious side spurs -> probably too high IF power
  - Spurs caused due to reflection and  $n^{\text{th}}$  products of mixing
  - Needed investigation to set right the IF power level (modulation signal path)
- Mixer definitely requires output Band-Pass filter

Theoretically, if the mixer divides power between 2 mirror frequencies and its loss  $L_{\text{MIXER}} = 5.2\text{dBm}$ :

$$P_{\text{MIXER\_TOTAL}} \approx P_{\text{LO}} + P_{\text{IF}} - L_{\text{MIXER}} = +3\text{dBm} + 3\text{dBm} - 5.2\text{dB} = +0.8\text{dBm}$$

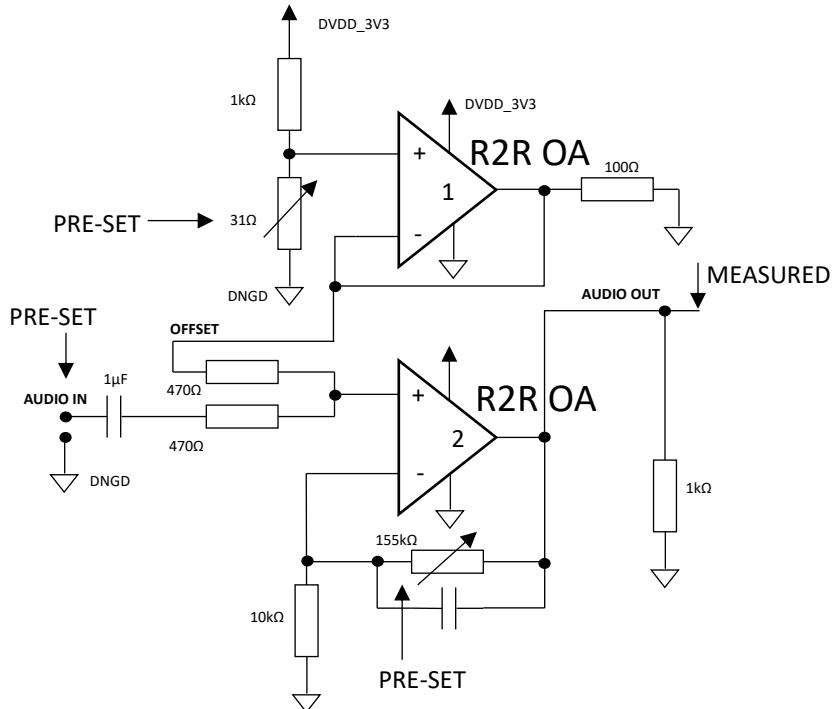
$$P_{\text{MIXER\_f1}} = \text{MIXER}_{\text{TOTAL}} - 3\text{dB} - 3\text{dB} = -5.2\text{dB}$$

$$P_{\text{MIXER\_f2}} \approx P_{\text{MIXER\_f1}}$$

What is close to the measured  $f_1 = -5.7\text{dBm}$  and  $f_2 = -6.3\text{dBm}$ . However, the formula is just estimation as the output power of diode ring mixer is not exactly sum of two input powers.

# Audio input circuit

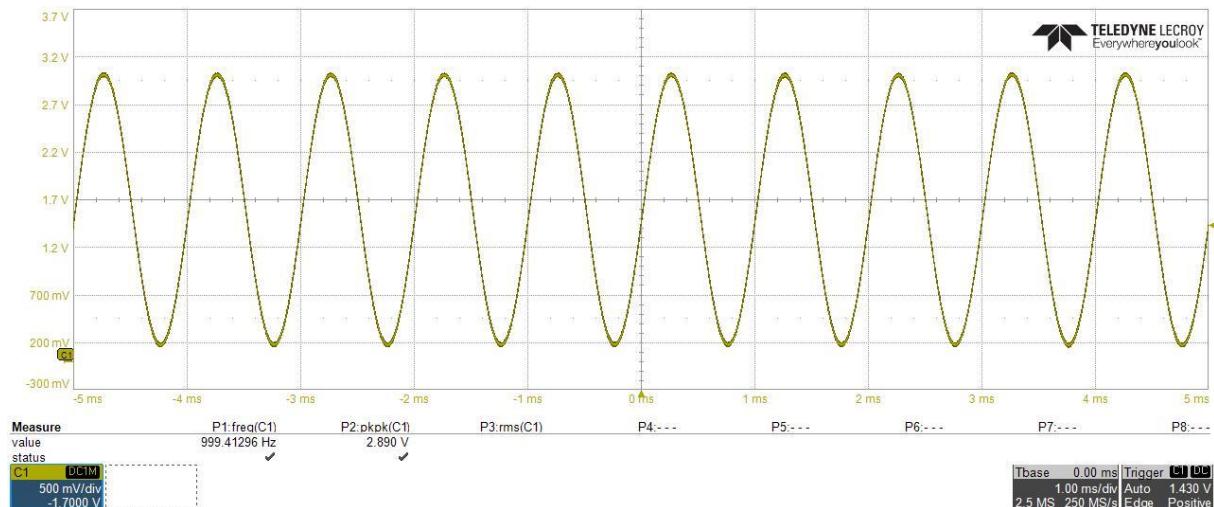
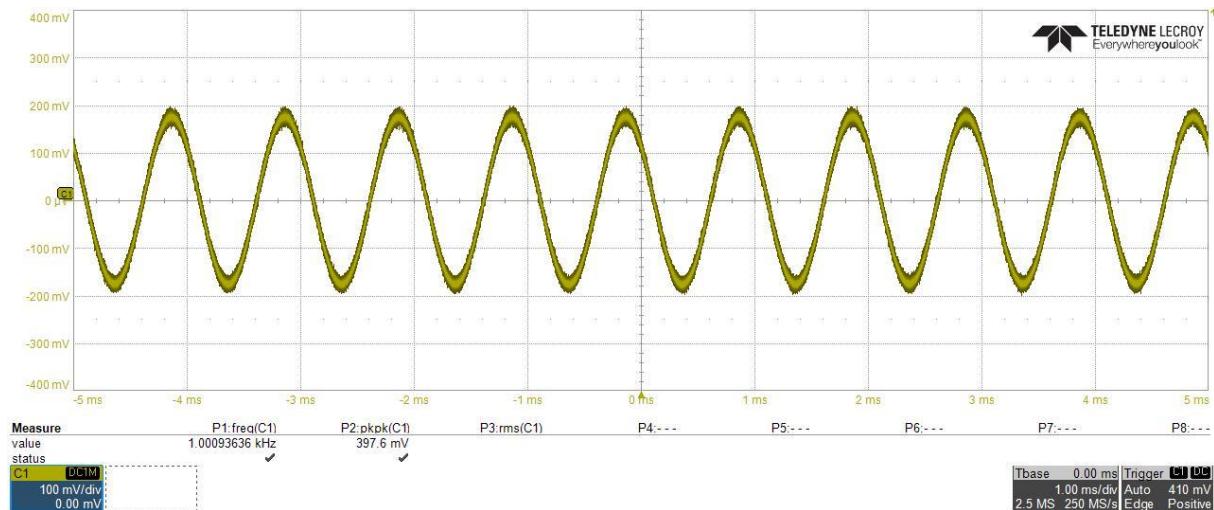
As the last part to be debugged is the audio amplifier stage. Basically, the weighted sum amplifier needs to be tested if converts correctly audio signal in range  $0.4V_{PP}$  into signal in range 0-3.3V for ADC fur resolution conversion. The testing circuit of Figure 120 is based on [Figure 32](#) as the ADC AD7476 is not needed. The AUDIO IN is fed by an iPhone XR phone (maximal volume) and the AUDIO OUT output is measured using oscilloscope, however also appropriate AWG may be used.



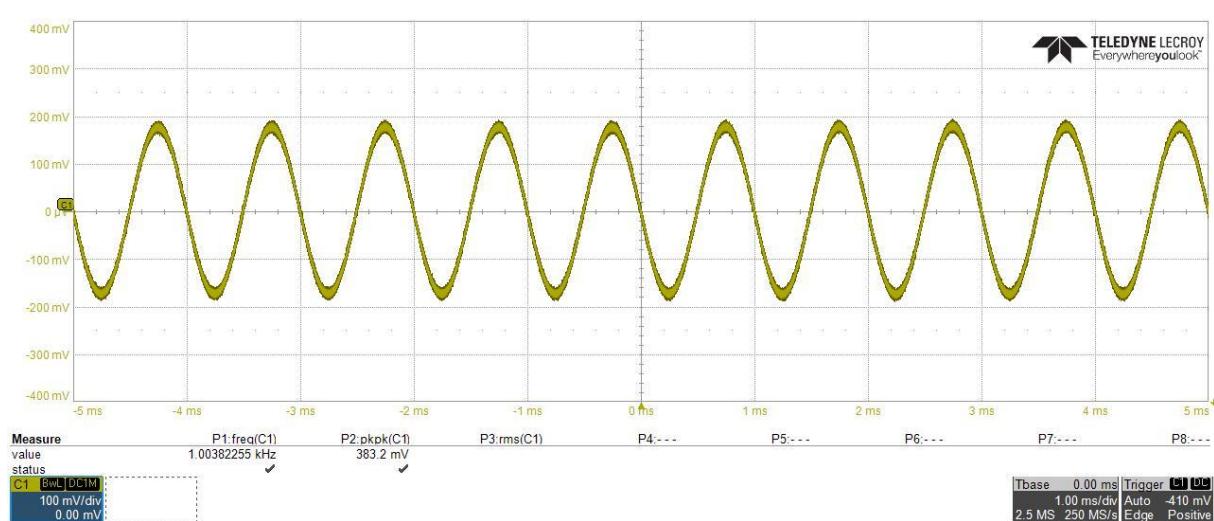
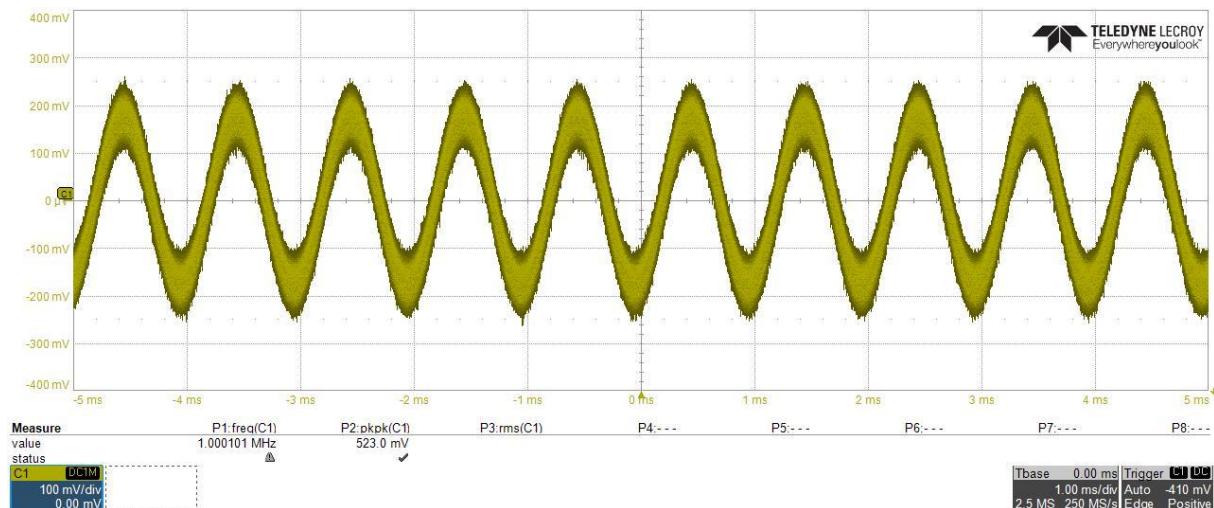
*Figure 120 Input audio Amplifier LMV358 testing circuit (mono)*

Typically, audio circuits are tested using 1kHz tone, in the case of the design with amplitude  $0.2V_{PP}$ . Following results shows voltages in node. The tone was generated by previously mentioned mobile phone playing YouTube 1kHz test video.

## Audio input circuit when RF disabled



## Audio input circuit when RF broadcast



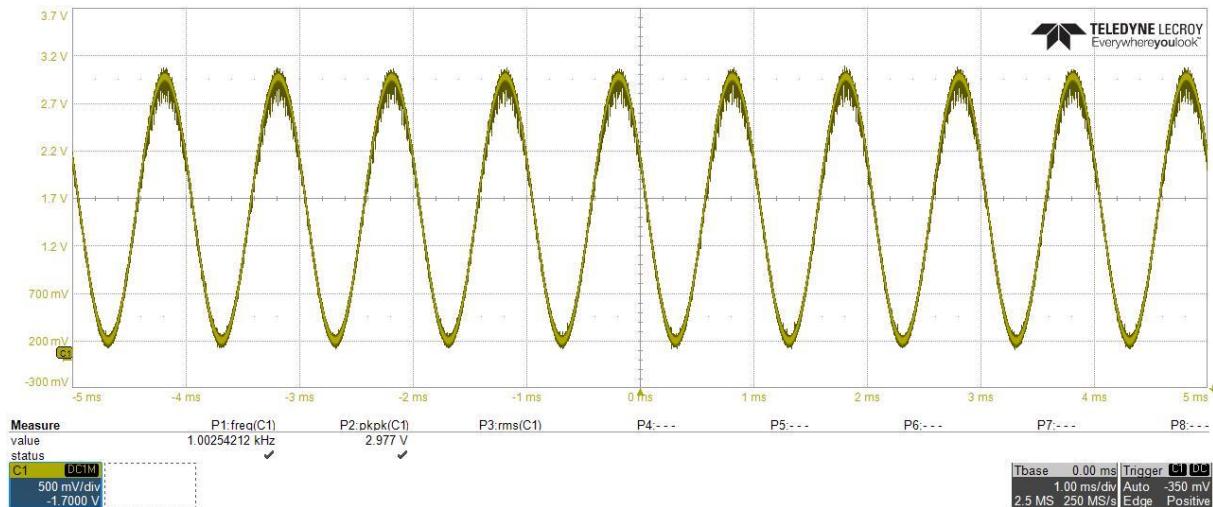


Figure 125 Testing Audio-out with the iPhone XR max volume, RF broadcast (full BW)

## Conclusion

- Amplifying the AUDIO\_IN 1kHz (RF disabled circuit):
  - AUDIO\_IN:  $397\text{mV}_{\text{PP}}$
  - AUDI\_OUT:  $2890\text{V}_{\text{PP}}$ 
    - $G_{\text{NON-INVERTING}}$  expected 16.4
    - $G_{\text{NON-INVERTING}}$  measured  $\approx 15$
- AUDIO\_OUT min-max:
  - AUDIO\_OUT Minimal value  $\approx 0.2\text{V}$
  - AUDIO\_OUT Maximal value  $\approx 3\text{V}$
  - Increasing the AUDIO\_IN voltage still should provide amplifying up to
    - AUDIO\_OUT Minimal value  $\approx 0.0\text{V}$
    - AUDIO\_OUT Maximal value  $\approx 3.2\text{V}$
  - Reserve for higher AUDIO\_IN signal source
- Significant AUDIO\_IN noise measured for RF broadcast setup
  - Shown 20MHz and full BW measurement
  - Noise spectrum 50-100MHz (output mixer frequencies)
  - Observed negligible impact on quality of the AUDIO\_OUT

# Cascaded amplifier

Refer to the chapter Off-board, section Cascade amplifier, an additional module in order to reach to transmitting range was used. Better figure noise is expected for the combination of the [Cascade MAX2611 + THS9001](#). All the measured signals are measured on the  $50\Omega$  load. The 4 measurement points are meant, when the following block is disconnected (e.g. output of the ADE-1L+ mixer is measured, when all the other blocks are disconnected).

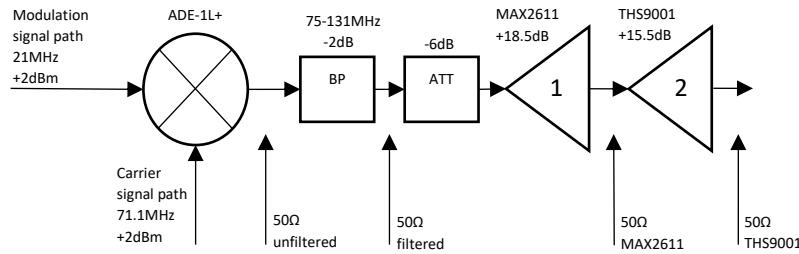


Figure 126 Cascaded amplifier testing circuit



Figure 127 Cascaded amplifier testing circuit photograph

## Unfiltered output of mixer

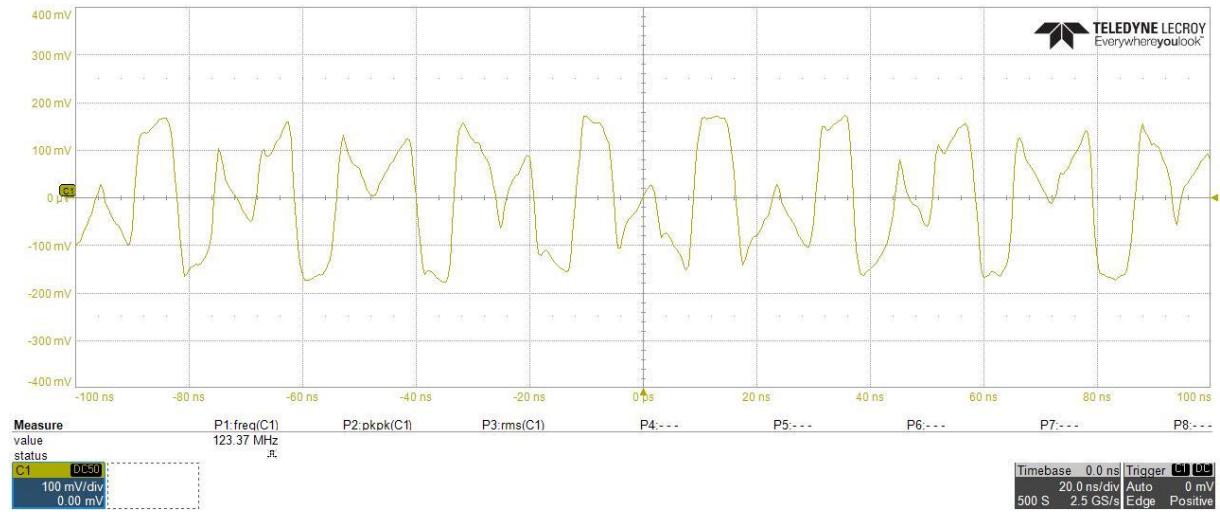


Figure 128 Unfiltered signal (mixer output), shape detail

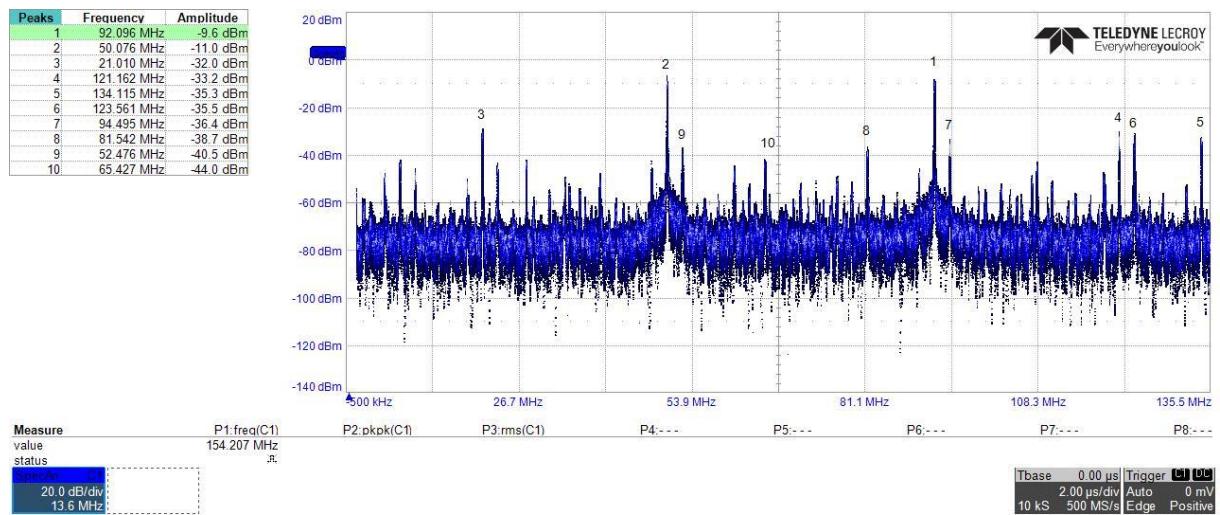


Figure 129 Unfiltered signal (mixer output), spectrum detail

## Filtered output of filter (Band-Pass 75MHz-131MHz)

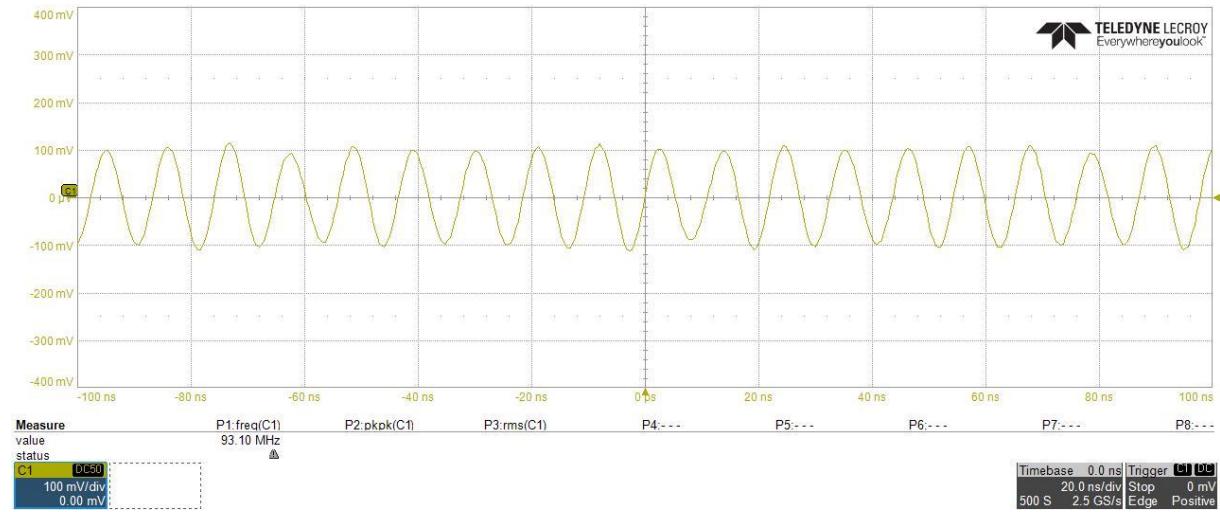


Figure 130 Filtered signal (Bandpass), shape detail

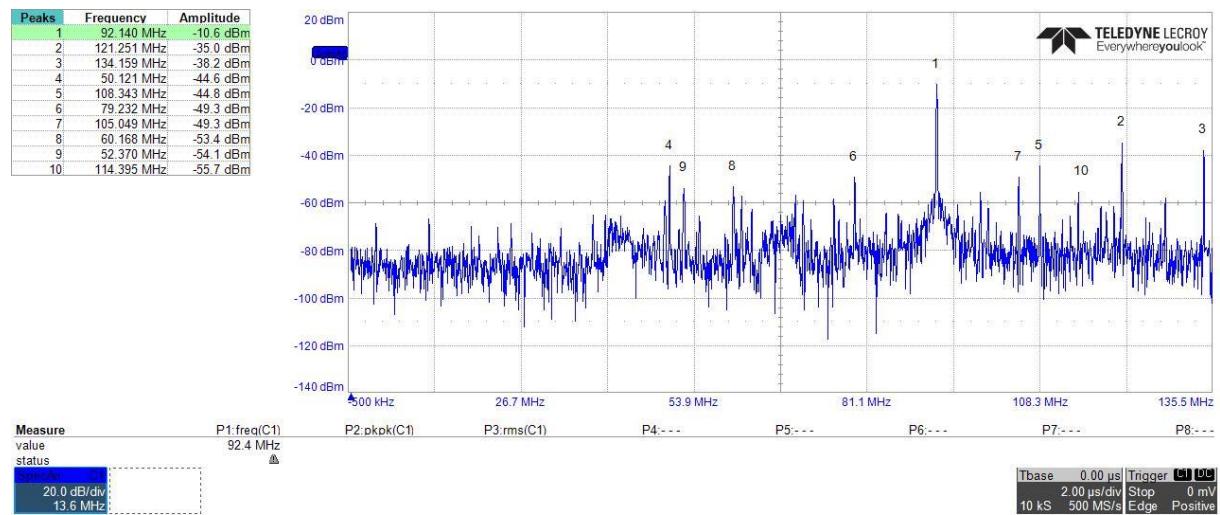


Figure 131 Filtered signal (Bandpass), spectrum detail

## Filtered + MAX2611

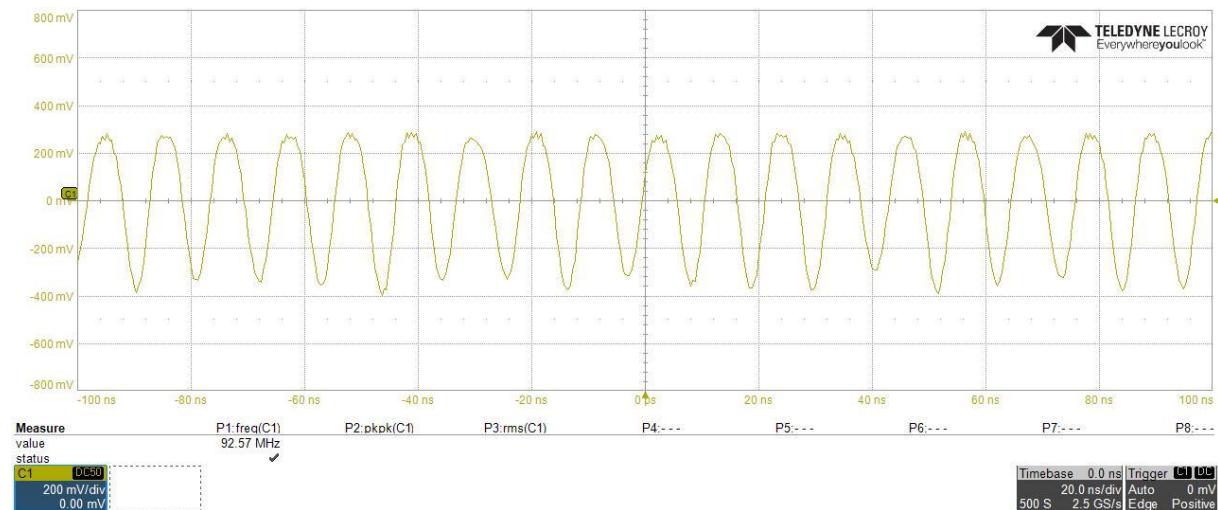


Figure 132 Filtered and amplified signal (MAX2611), shape detail

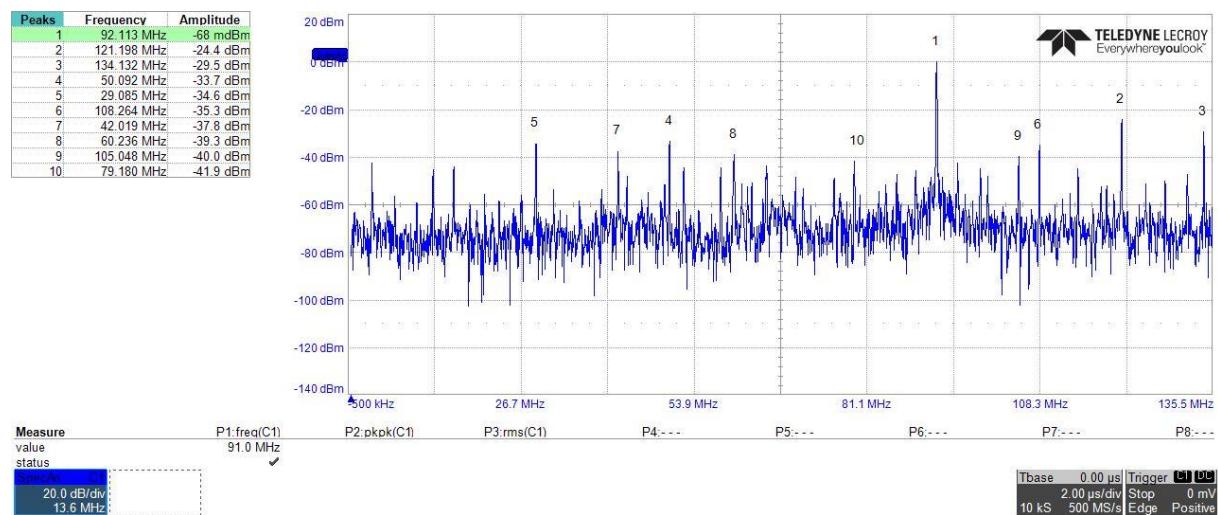


Figure 133 Filtered and amplified signal (MAX2611), spectrum detail

## Filtered + MAX2611 + THS9001

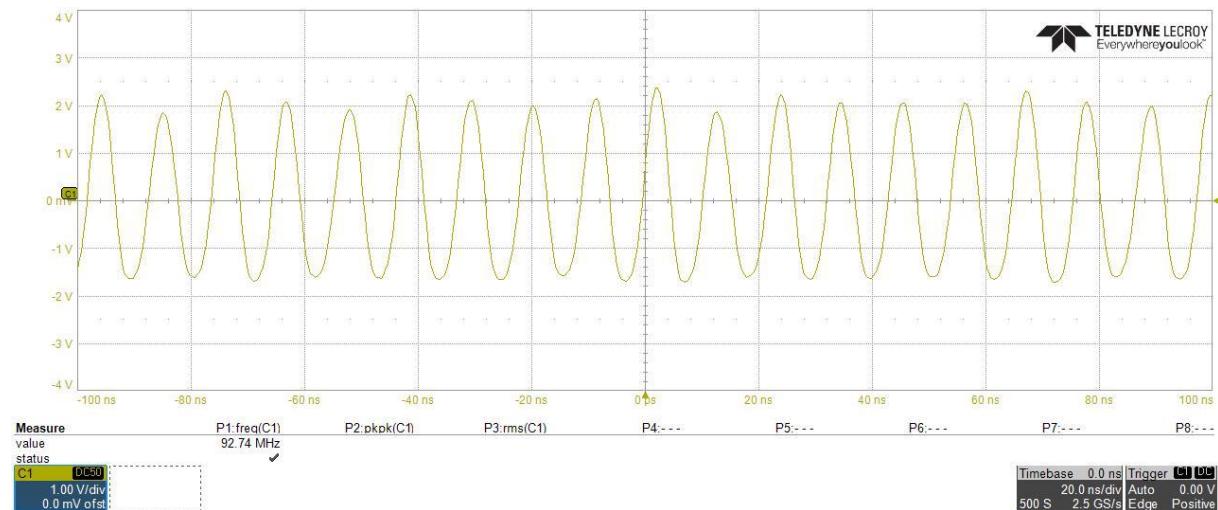


Figure 134 Filtered and cascade-amplified signal (THS9001), shape detail

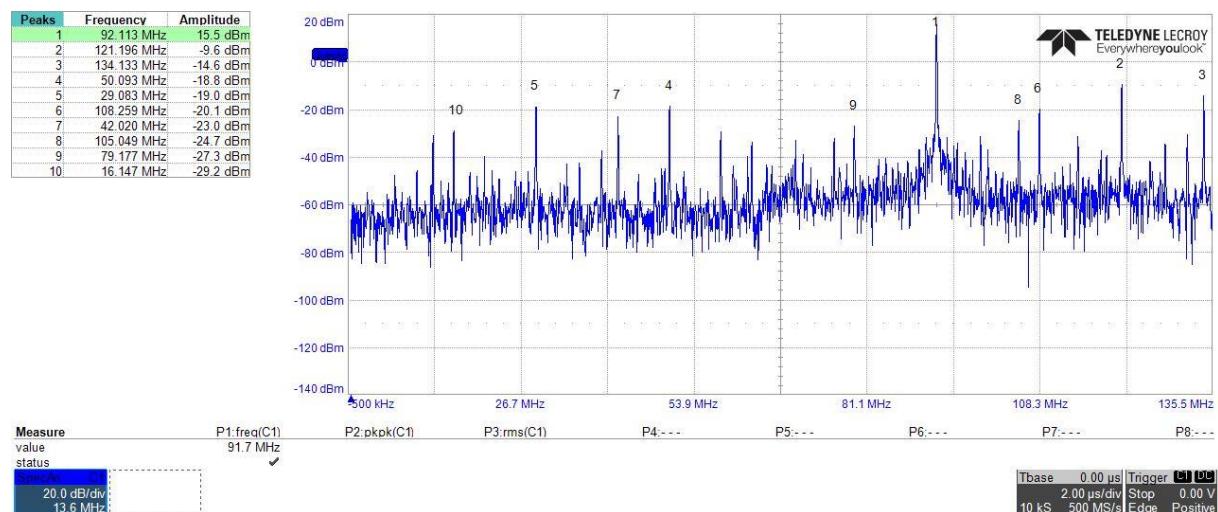


Figure 135 Filtered and cascade-amplified signal (THS9001), spectrum detail

## *Conclusion*

- Band-Pass filter limits the Band-Stop range by 33.4dB (expected 35dB suppression)
  - The 50.08MHz mirror frequency -11dBm suppressed to -44.6dBm
  - Results across Figure 130 up to 135 may confirm meeting the [requirement 4](#): The VHF-Transmitter shall not interfere other frequencies than used channel.
- Several spurs of frequency 121MHz, 134 MHz and others not eliminated, shall be object of further investigation.
- Amplifier MAX2611 with 6dB attenuated and filtered input reaches -0.068dBm

$$P_{BP+MAX2611} = P_{MIXER} - L_{BP} - L_{ATT} + A_{MAX2611}$$

$$P_{BP+MAX2611} = -11dBm - 1.5dB - 6dB + 18.5dB = 0.0dBm$$

- Amplifier MAX2611+THS9001 with 6dB attenuated and filtered input reaches +15.5dBm:  
 $P_{BP+MAX2611} = P_{MIXER} - L_{BP} - L_{ATT} + A_{MAX2611} + A_{THS9001}$

$$P_{BP+MAX2611} = -11dBm - 1.5dB - 6dB + 18.5dB + 15.5dB = +15.5dBm$$

- Amplifier MAX2611+THS9001 with 6dB attenuated and filtered input reaches +15.5dBm:
  - +15.5dBm (3.6V<sub>PP</sub>) is sufficient result for the [requirement 9](#): The VHF-Transmitter shall provide maximal possible broadcast power for 5V/50Ω.

# Workaround

## Bug in the Audio input amplifier circuitry

The AUDIO\_35MM\_F\_JACK ground was connected directly into the OFFSET amplifier output. This caused audio signal shortcut and the shortcut was followed by high sound distortion. Also, only one channel of the JACK input was used. For the original circuit are default values just tentative (especially R11 = 10k cannot be used).

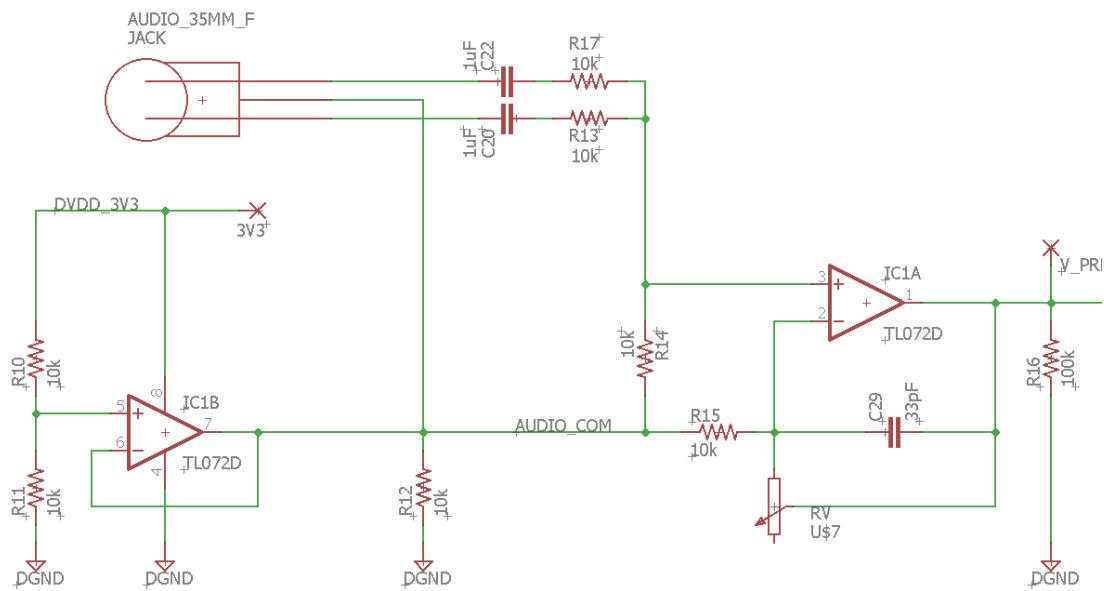


Figure 136 Original Audio-in circuit schematic

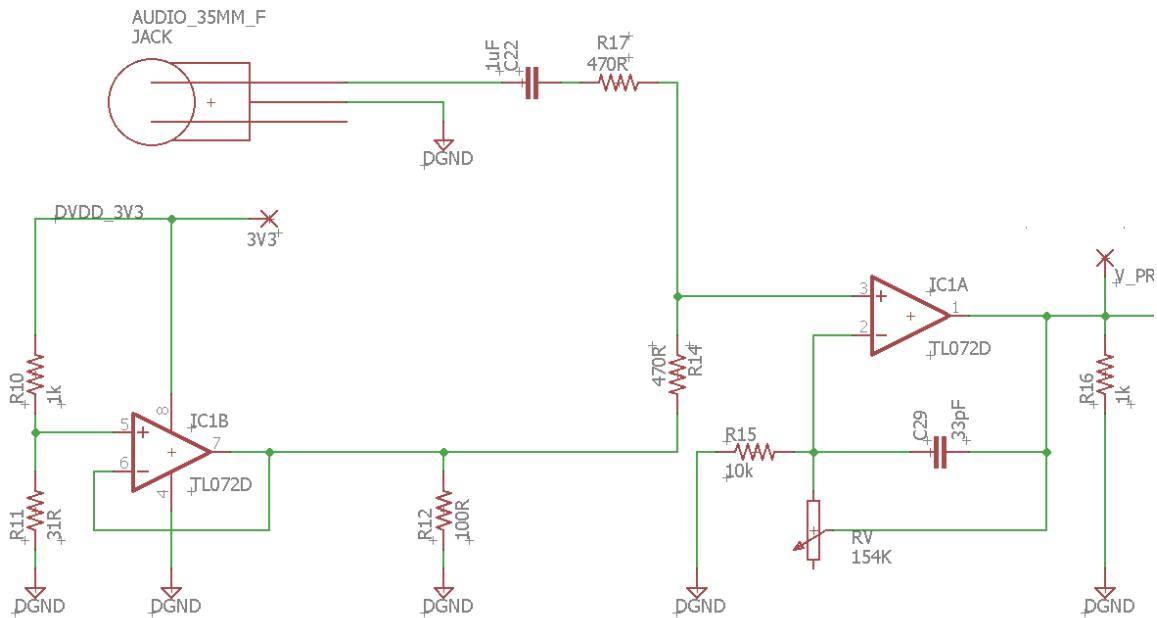


Figure 137 Modified Audio-in circuit schematic

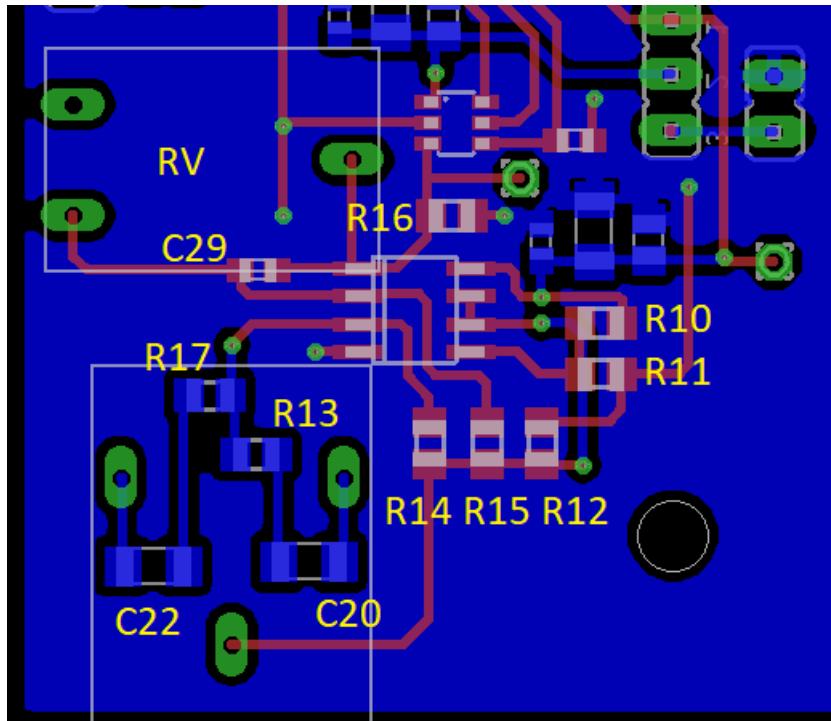


Figure 138 Original Audio-in circuit PCB layout

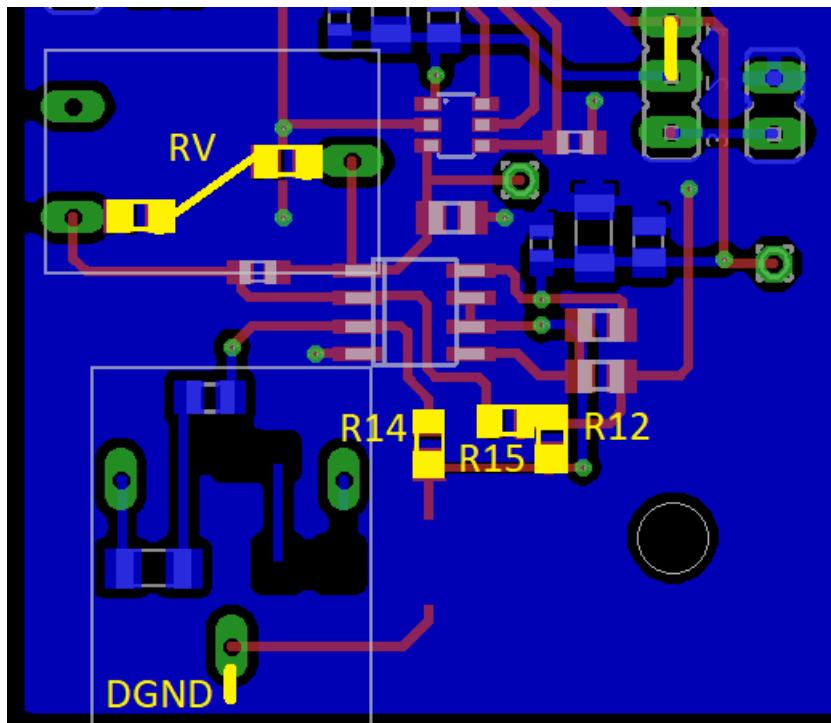


Figure 139 Modified Audio-in circuit PCB layout

For Figure 129, the upper yellow resistors in series are representing the RV U\$7 154k $\Omega$  and together with the R15 10k $\Omega$  sets the IC1A gain. The meaning of the R12 stays the same as for Figure 128 and loads the IC1B – OFFSET voltage. The R14 470 $\Omega$  resistor is used as second input for weighted sum amplifier. Necessary is to disconnect the JACK ground pin (middle) and connect it to ground plane (marked yellow). Figure 129 also missed C20 and R13 as only one sound channel is processed, note that for other board the C22 and R17 is omitted.

## Merging the 5VDD together with RF\_VDD

Originally, the system is designed to have several power supplies to enhance interference bottom. Anyway, when used single 5V source for 5VDD as well as RF\_VDD, good operation of the system was reached. The easiest way to merge these two power supplies is connection near to the ADR3425 voltage reference chip (the yellow wire in Figure 131).

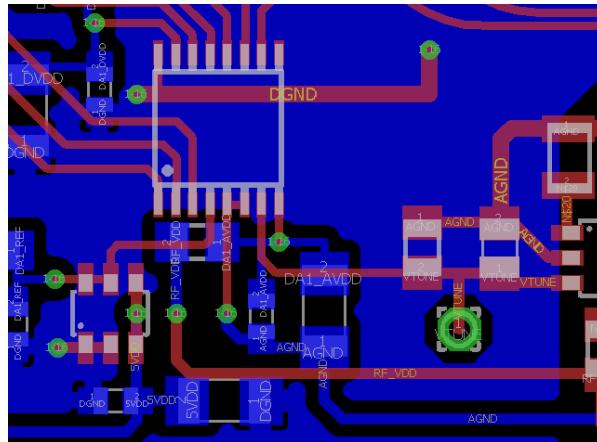


Figure 140 Original separated 5VDD and RF\_VDD PCB layout

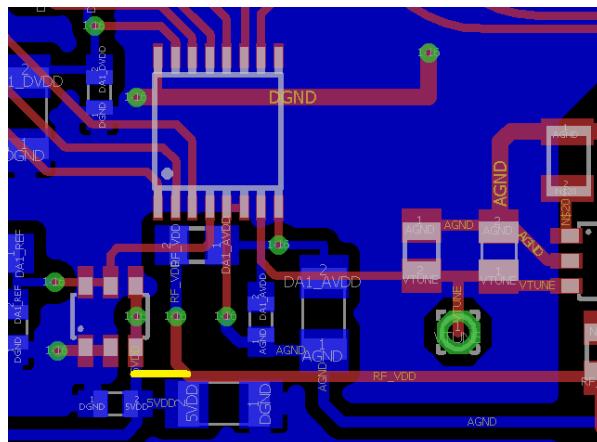


Figure 141 Merged 5VDD and RF\_VDD PCB layout

## 5VDD pin from the CMODS6

The CMODS6 may be supplied by the micro-USB or by the VU pin located on the module. When these two pins are connected, the conventionally shielded USB5V0 bus may be present at the VU pin of the CMODS6 (Figure 132, 133). This workaround is necessary to use the USB5V0 as the 5VDD. Modification of Figure 135 in compare to Figure 134 allows to connect external 5V source.

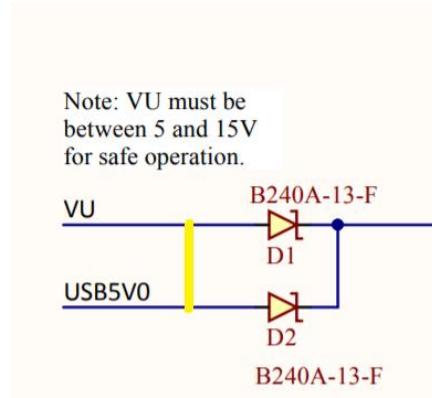


Figure 142 CMODS6 VU and USB5V0 Connection schematic [13]

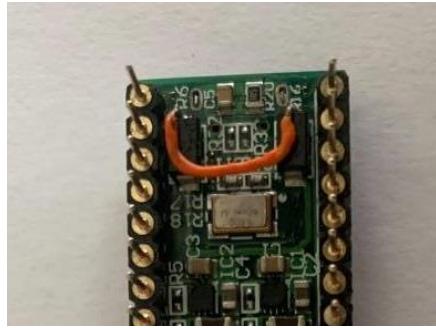


Figure 143 CMODS6 VU and USB5V0 Connection PCB photo [13]

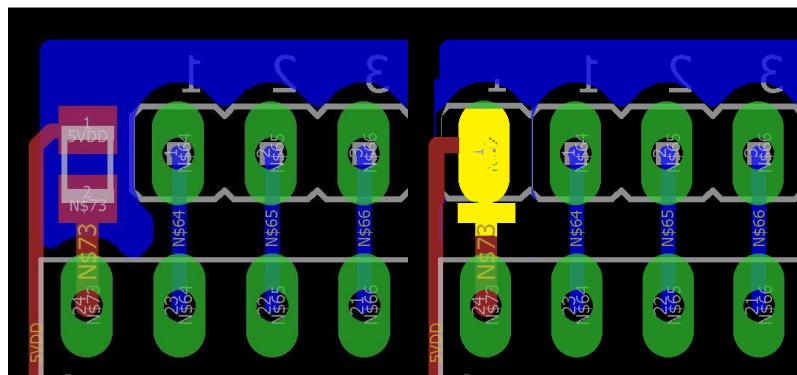


Figure 144 Power supply original PCB layout

Figure 145 Power supply modified PCB layout

# Conclusion

According to the measured results in the HW Bring-up chapter, the VHF-transmitter design has all assumptions to broadcast FM signal for all channels within 88-108MHz ([requirement 4](#)). The system was tested with several FM receivers and were reached clear mono sound transmission (for music as well as voice, meeting the [requirement 1](#)).

The carrier signal path may generate signal within 69MHz-83MHz with, but improvements to filter this signal prior to the MAX2611 amplifier may result in the higher LO signal and thus higher output power of the mixer. The frequency adjustment meets partially the [requirement 5](#). The weakest part of the carrier circuitry is missing feedback to measure the carrier frequency. This could be problem as the VCO MAX2006 operating point may a bit differ due to aging or ambient conditions. Direct measurement by converting the carrier signal into LVDS level or LVCMS level may be used rather than ADC conversion. Also, VCO MAX2606 may be replaced by any other from the MAX260x, what allows capability of broadcast beyond VHF range (MAX2609 705MHz). Roughly, the VCO MAX2606 may be controlled with 6kHz/mV resolution and even more precisely if needed as the VCO controlling DAC1 has maximal output resolution 0.076 $\mu$ V. Also, this signal may already contain payload via the DAC1 voltage. Note, that measurement observed that 15mV<sub>PP</sub> signal included 0.6V<sub>TUNE</sub> results in 15kHz BW signal of 88MHz.

The modulation signal path when operating in 120MSPS mode was evaluated as reliable signal path with low noise, high output power and frequency range 0-40MHz without significant power losses. The modulation path has very precisely controlled frequency with resolution 3.57Hz determined by the FPGA's DDS feeding the parallel DAC1. The maximal frequency is set by the 40MHz Low-Pass filter, which may be replaced for operation in higher frequency mode. Unfortunately, the FPGA CMODS6 module pinout cannot prevent signal crosstalk and therefore, jittered signals controlling the DAC1 are expected, especially when the DAC1 is operating in the 210MSPS maximal sampling. However, for operation where small jitter is affordable may be the DAC1 still used and generate signal up to 105MHz. Potential of the modulation circuitry is full digital control and thus, except the FM many other modulations and multi-band signals may be generated up to 40MHz bandwidth. Frequency adjustment of DAC1 within 2.5-40MHz meets fully the [requirement 5](#).

When evaluating the mixer, higher spurs were observed and thus the lower modulation signal path should be tried-out. The fact, that the mixer operates better with lower IF signal was observed in the chapter mixer standalone test. This can be done by decreasing the DAC1 maximal output voltage and so, setting the reference DAC1 current, or digitally by decreasing the sample values running the DAC1, which are generated by the DDS.

Once again, when the VCO is replaced by the MAX2609, 705MHz signal may be reached. On the other hand DAC1 may generate digitally determined signal of frequency up to 40MHz. However, summing of these signals (745MHz) is beyond the mixer ADE-1L+ maximal frequency (500MHz). For higher than maximal frequency are expected higher power losses and increased noise. As the VHF range is understood as 30-300MHz bandwidth, the design could be marked as VHF-transmitter.

Desired output RF frequency may be reached by lot of combinations of the carrier signal and modulation signal as both signals are digitally controlled. For optimal operation, an LUT containing values to set FM channel by using an appropriate VCO and DAC0 setting could be created. Also the LUT may be created during calibrating the VHF-Transmitter incorporating with digitally controlled FM-receiver module.

Measurement of the cascade brings interesting results in term of output power as well as interference. When single bandpass filter is used (75-131MHz), system reaches -10dBm output power in FM broadcast range and the mirror mixing frequency is suppressed down to -44.6dBm. However, spurs of frequency 121MHz, 134MHz and others observed. Mentioned spurs are always 20dB up to 30dB below the signal, but still investigation and elimination of the spurs shall be considered.

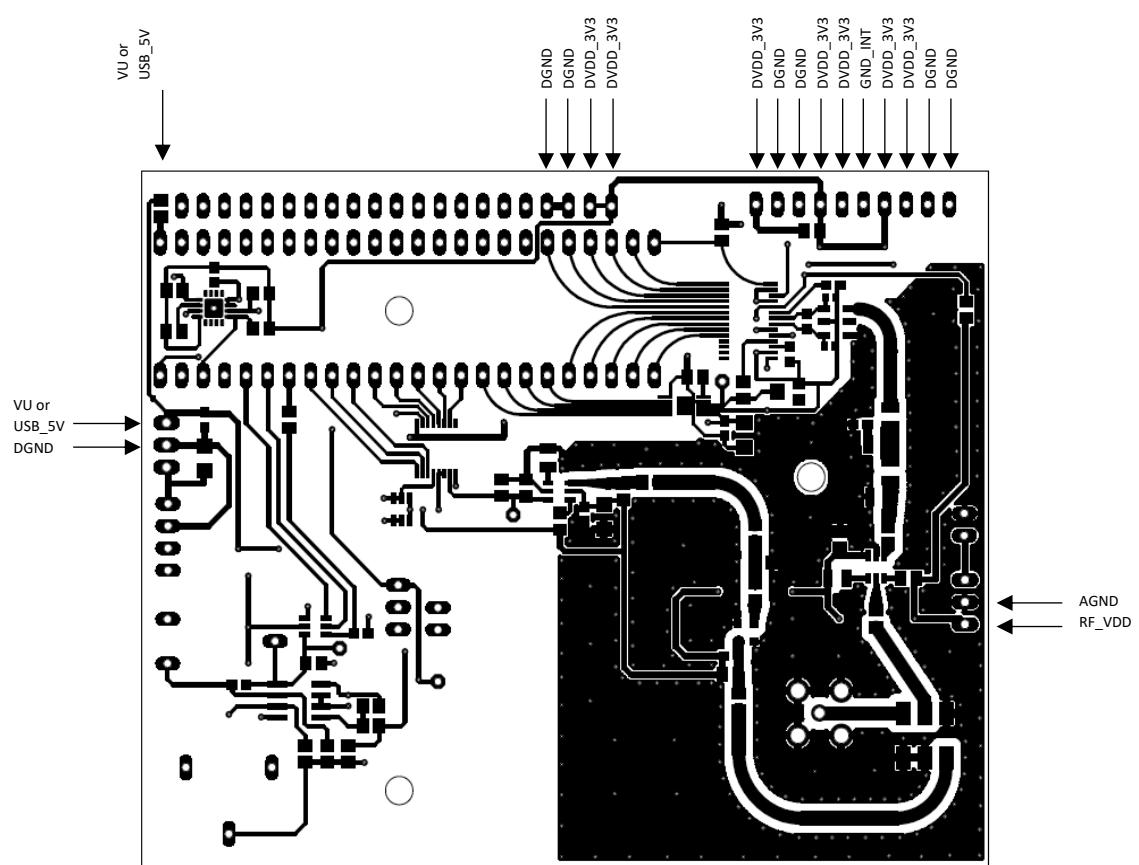
For single output amplifier (MAX2611), output power reaching 0dBm ( $630\text{mV}_{\text{PP}}$ ) was measured. For cascade of the MAX2611 and THS9001, output power of +15.5dBm ( $3.6\text{V}_{\text{PP}}$ ) was measured. Still, maximal possible power for  $5\text{V}/50\Omega$  is +18dBm ( $5\text{V}_{\text{PP}}$ ), but the value +15.5dBm is close enough to fulfill the [requirement 9](#).

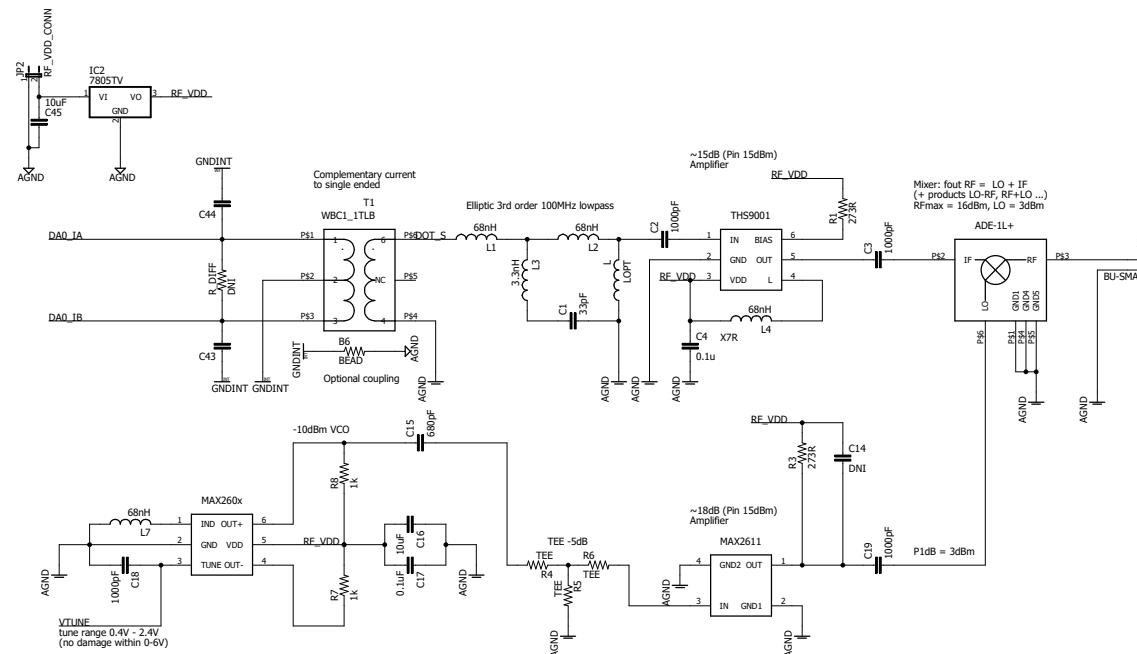
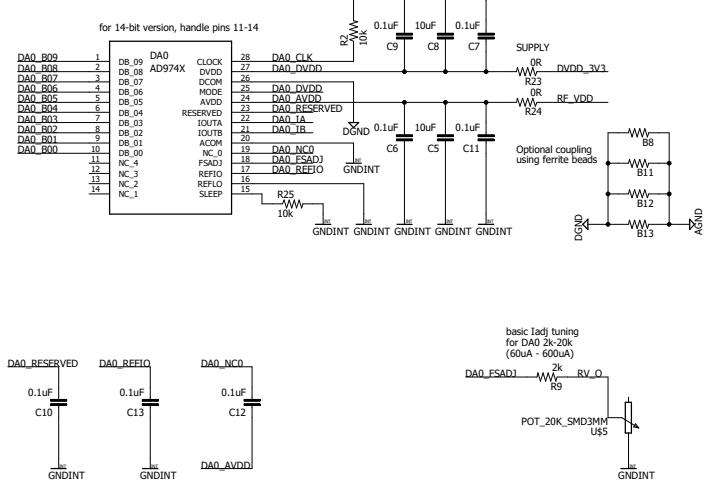
The audio input circuitry was tested with good assumptions to ensure sound broadcast operation. Also, the reserve for input signal was observed. Enough high AUDIO\_IN results directly in strength of broadcasted sound and normally, radio stations broadcast maximal volume by default. The designed PCB features only with single ADC, so two boards with two ADC are needed for stereo broadcast.

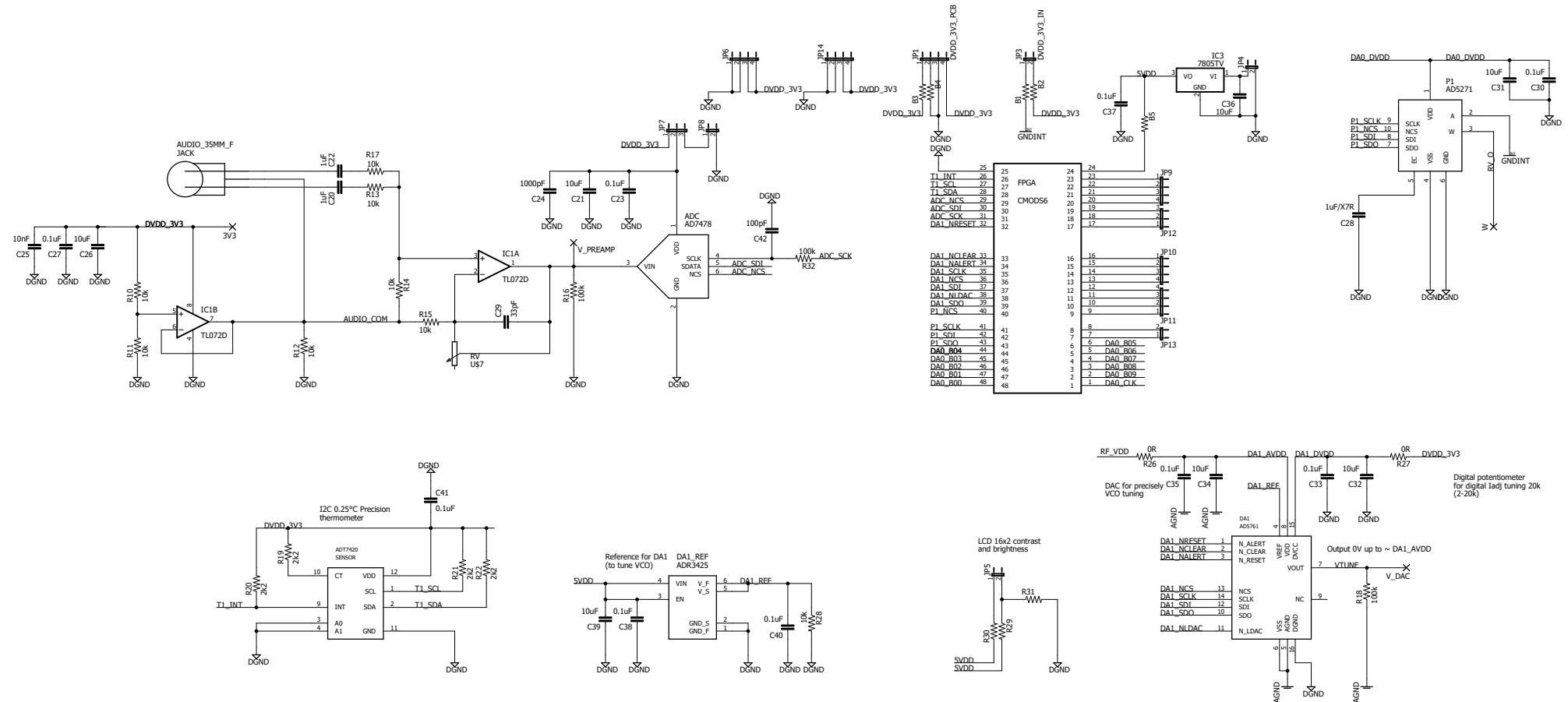
# References

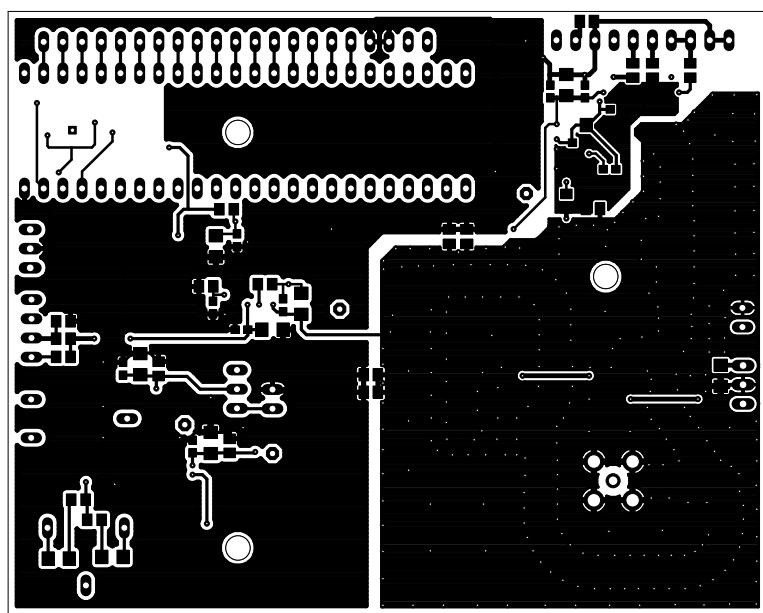
- [1] Datasheet AD5761/A5721  
[https://www.analog.com/media/en/technical-documentation/data-sheets/ad5761\\_5721.pdf](https://www.analog.com/media/en/technical-documentation/data-sheets/ad5761_5721.pdf)
- [2] Datasheet MAX2605-MAX2609  
<https://datasheets.maximintegrated.com/en/ds/MAX2605-MAX2609.pdf>
- [3] Datasheet EVKIT MAX2605-MAX2609  
<https://datasheets.maximintegrated.com/en/ds/MAX2605EVKIT-MAX2609EVKIT.pdf>
- [4] Datasheet MAX2611  
<https://datasheets.maximintegrated.com/en/ds/MAX2611.pdf>
- [5] Datasheet AD9742  
<https://www.analog.com/media/en/technical-documentation/data-sheets/AD9742.pdf>
- [6] Datasheet WBC1-1TL  
<https://www.coilcraft.com/getmedia/f685d903-2563-4c96-8ba6-f82a58883aeb/wbc.pdf>
- [7] Datasheet ADE-1L+  
<https://www.minicircuits.com/pdfs/ADE-1L.pdf>
- [8] Datasheet RBP-98+  
<https://www.minicircuits.com/pdfs/RBP-98+.pdf>
- [9] Datasheet THS9001  
[https://www.ti.com/lit/ds/symlink/ths9001.pdf?ts=1617578486830&ref\\_url=https%253A%252F%252Fwww.google.com%252F](https://www.ti.com/lit/ds/symlink/ths9001.pdf?ts=1617578486830&ref_url=https%253A%252F%252Fwww.google.com%252F)
- [10] Datasheet NN01\_055, FR01\_B3\_W\_0\_055  
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[https://ignion.io/files/DS\\_FR01-B3-W-0-055.pdf](https://ignion.io/files/DS_FR01-B3-W-0-055.pdf)
- [11] Datasheet ADR3425  
[https://www.analog.com/media/en/technical-documentation/data-sheets/ADR3412\\_ADR3420\\_ADR3425\\_ADR3430\\_ADR3433\\_ADR3440\\_ADR3450.pdf](https://www.analog.com/media/en/technical-documentation/data-sheets/ADR3412_ADR3420_ADR3425_ADR3430_ADR3433_ADR3440_ADR3450.pdf)
- [12] Datasheet LMV358  
<https://www.onsemi.com/pdf/datasheet/lmv358-d.pdf>
- [13] Schematics CMODS6 Rev A0  
[https://reference.digilentinc.com/\\_media/cmod\\_s6:cmods6\\_sch.pdf](https://reference.digilentinc.com/_media/cmod_s6:cmods6_sch.pdf)
- [14] LogiCore IP DDS Compiler v4.0  
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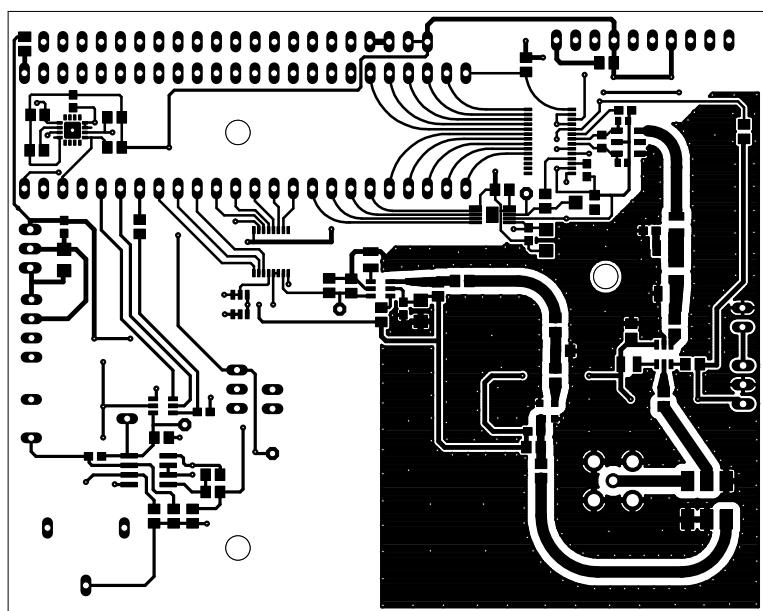
# System power supply pinout

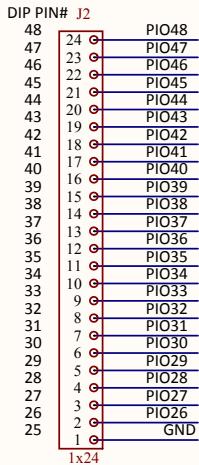
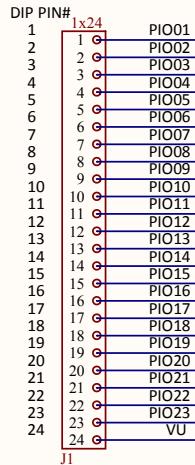




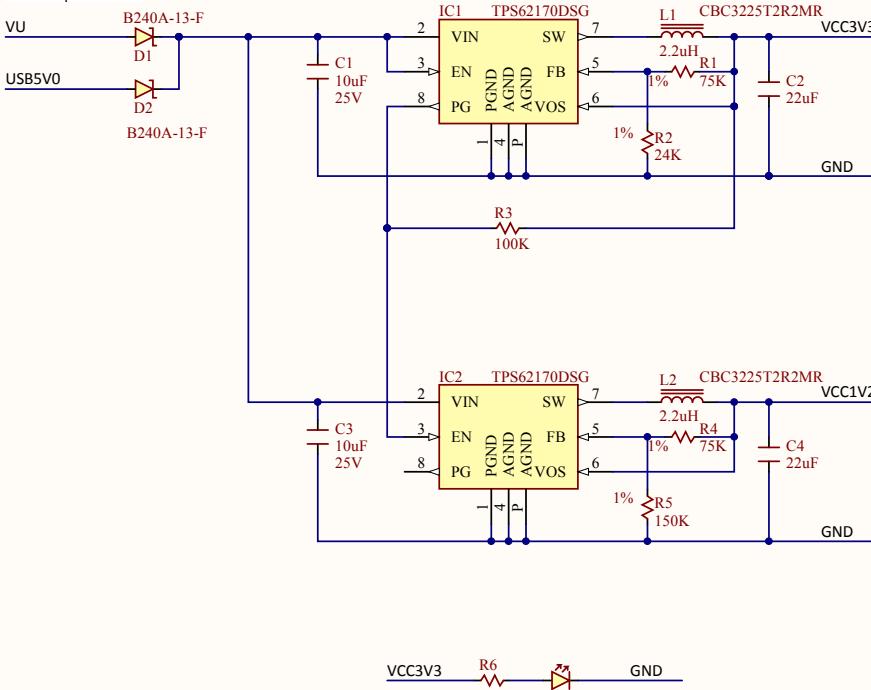




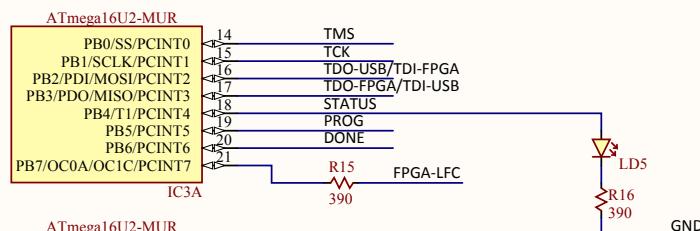




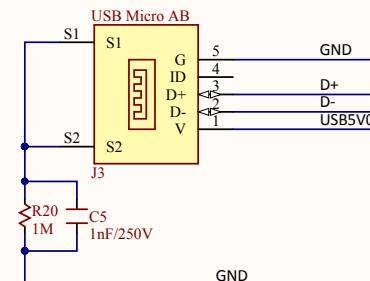
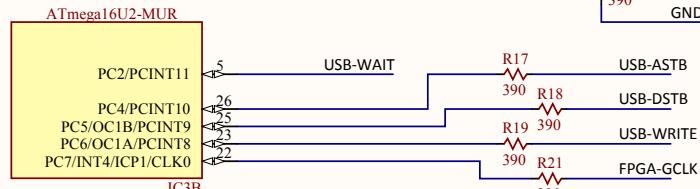
Note: VU must be between 5 and 15V for safe operation.



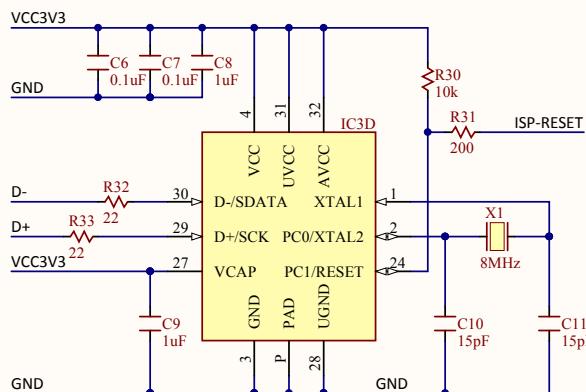
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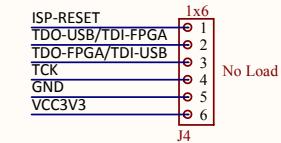
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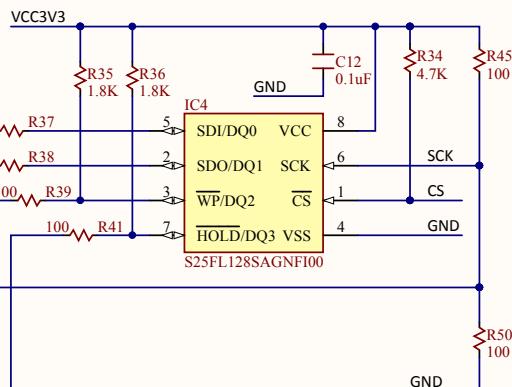
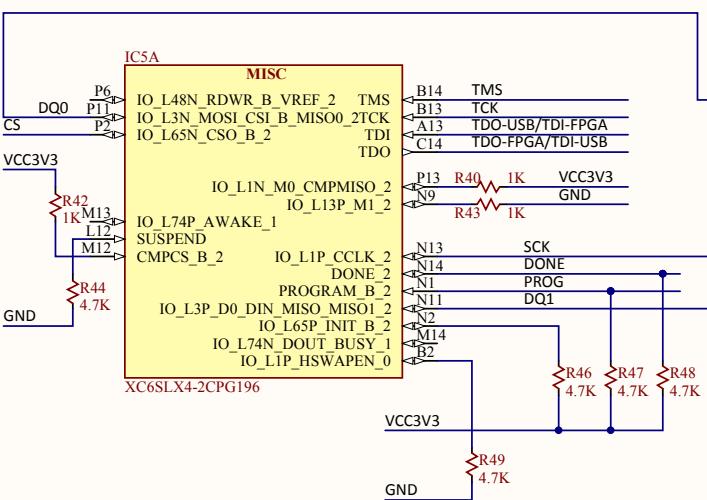


C



D



**MISC****IC5B****BANK0**

IO_LIN_VREF	A2	PIO28
IO_L2P	B3	PIO27
IO_L2N	A3	PIO26
IO_L3P	B4	
IO_L3N	A4	
IO_L4P	B5	
IO_L4N	A5	
IO_L34P_GCLK19	B6	USB-WAIT
IO_L34N_GCLK18	A6	USB-ASTB
IO_L35P_GCLK17	B7	USB-DSTB
IO_L35N_GCLK16	A7	USB-WRITE
IO_L36P_GCLK15	B8	
IO_L36N_GCLK14	C8	
IO_L37P_GCLK13	B8	
IO_L37N_GCLK12	A8	
IO_L62P	B9	USB-DB0
IO_L62N_VREF	B10	USB-DB1
IO_L63P_SCP7	A10	USB-DB2
IO_63N_SCP6	B11	USB-DB4
IO_64P_SCP5	A11	USB-DB5
IO_64N_SCP4	B12	USB-DB6
IO_65P_SCP3	A12	USB-DB7
IO_65N_SCP2	D11	
IO_66P_SCP1	C11	
IO_66N_SCP0		

XC6SLX4-2CPG196

**IC5C****BANK1**

IO_L1P	C12	
IO_LIN_VREF	C13	PIO23
IO_L32P	D13	PIO22
IO_L32N	D14	PIO21
IO_L33P	E13	PIO20
IO_L33N	E14	PIO19
IO_L34P	F11	
IO_L34N	F12	
IO_L40P_GCLK11	G13	PIO18
IO_L40N_GCLK10	G14	PIO17
IO_L41P_GCLK9_IRDY1	F13	PIO16
IO_L41N_GCLK8	F14	PIO15
IO_L42P_GCLK7	H13	PIO14
IO_L42N_GCLK6_TRDY1	H14	PIO13
IO_L43P_GCLK5	H11	
IO_L43N_GCLK4	H12	
IO_L45P	J13	PIO12
IO_L45N	J14	PIO11
IO_L46P	J11	
IO_L46N	J12	
IO_L47P	K13	PIO10
IO_L47N	L13	PIO09
IO_L53P	L14	PIO08
IO_L53N_VREF		PIO07

XC6SLX4-2CPG196

**IC5D****BANK2**

IO_L2P_CMPCLK	N12	PIO06
IO_L2N_CMPMOSI	P12	PIO05
IO_L12P_D1_MISO2	N10	DO2
IO_L12N_D2_MISO3	P10	DO3
IO_L13N_D10	P9	BTN1
IO_L14P_D11	M8	
IO_L14N_D12	N8	FPGA-GCLK
IO_L30P_GCLK1_D13	P8	BTN0
IO_L30N_GCLK0_USERCCLK	N7	FPGA-LFC
IO_L31P_GCLK31_D14	P7	PIO04
IO_L31N_GCLK30_D15	N6	PIO03
IO_L48P_D7	N5	PIO02
IO_L49P_D3	P5	PIO01
IO_L49N_D4	L4	
IO_L62P_D5	M4	
IO_L62N_D6	N4	LD2
IO_L63P	P4	LD3
IO_L63N	N3	LD0
IO_L64P_D8	P3	LD1
IO_L64N_D9		

XC6SLX4-2CPG196

**IC5E****BANK3**

IO_L1P	M2	PIO48
IO_LIN_VREF	M1	PIO47
IO_L2P	L2	PIO46
IO_L2N	K2	PIO44
IO_L36P	K1	PIO43
IO_L36N	J4	
IO_L37P	J3	
IO_L37N	J2	
IO_L41P_GCLK27	J1	PIO42
IO_L41N_GCLK26	G2	PIO40
IO_L42P_GCLK25_TRDY2	G1	PIO39
IO_L42N_GCLK24	H2	PIO38
IO_L43P_GCLK23	H1	PIO37
IO_L43N_GCLK22_IRDY2	G2	PIO36
IO_L44P_GCLK21	F1	PIO35
IO_L44N_GCLK20	E4	
IO_L49P	F3	
IO_L49N	E2	PIO34
IO_L50P	E1	PIO33
IO_L50N	D4	
IO_L51P	D3	
IO_L51N	D2	PIO32
IO_L52P	D1	PIO31
IO_L52N	C1	PIO30
IO_L83P	B1	PIO29
IO_L83N_VREF		

XC6SLX4-2CPG196

A

A

B

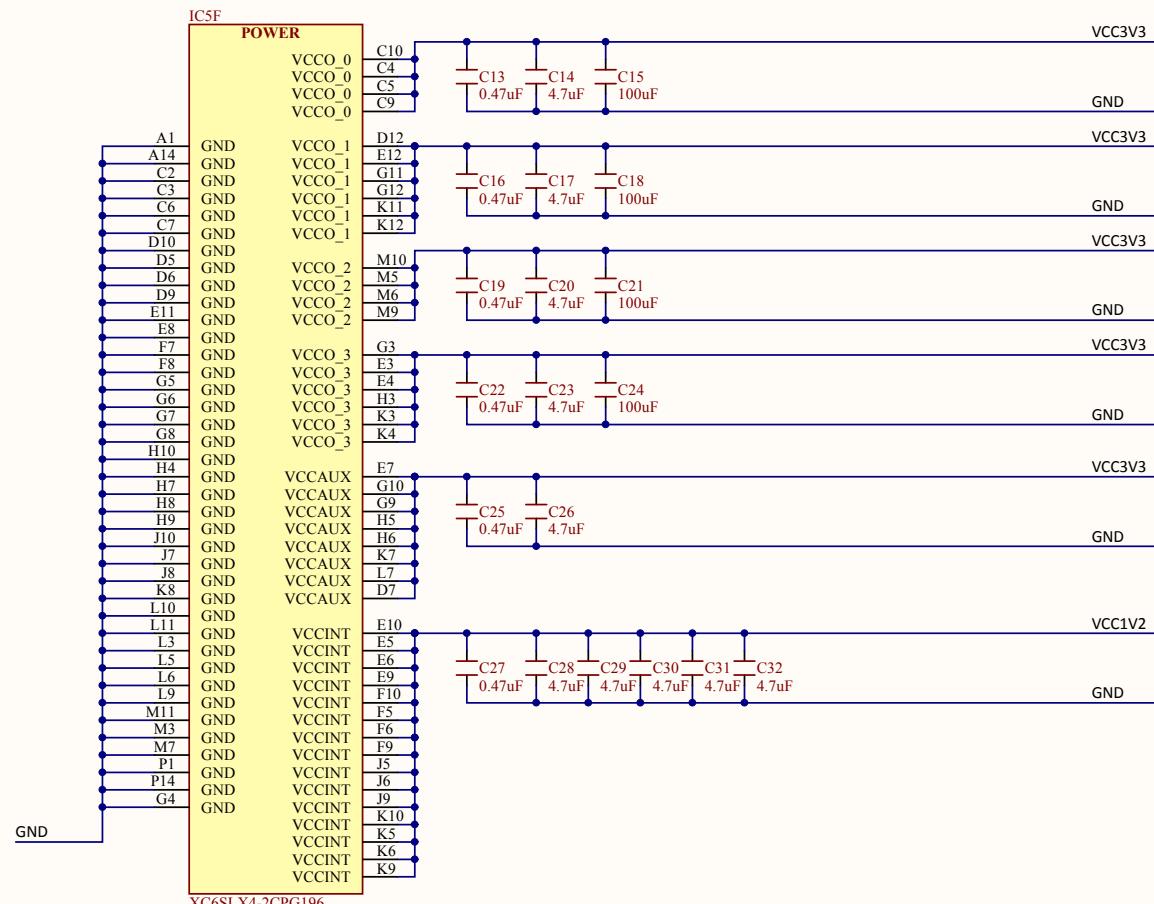
B

C

C

D

D



Title		Rev
Cmod S6		A.0
Circuit		Copyright 2013
FPGA Decoupling		
Doc#	500-282	
Engineer	MA	
Author	GMA	
Date	5/9/2013	
Sheet#	4 out of 4	

**DIGILENT**  
BEYOND THEORY