8Kx8 bit Low Power CMOS Static RAM

FEATURE SUMMARY

- Process Technology : CMOS
- Organization : 8K x 8
- Power Supply Voltage : Single 5V ± 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-DIP, 28-SOP

GENERAL DESCRIPTION

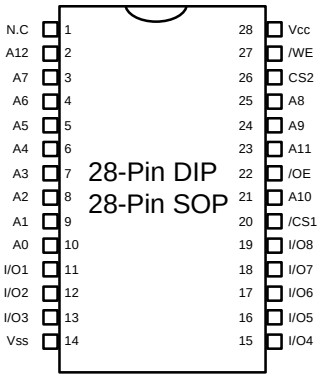
The KM6264B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operations with low data retention current.

PRODUCT FAMILY

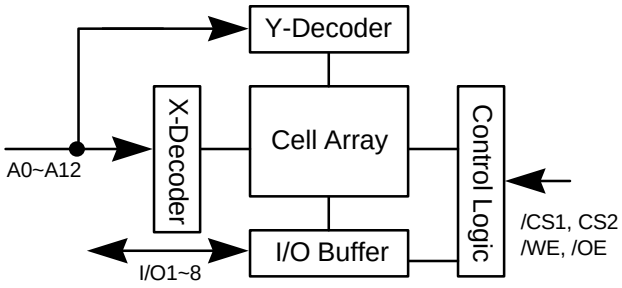
Product Family	Operating Temperature	Speed	PKG Type	Power Dissipation	
				Standby(Isb1, Max)	Operating(Icc2)
KM6264BL	Commercial (0~70 °C)	70/100/120ns	28-DIP, 28-SOP	100uA	55mA
KM6264BL-L				10uA	
KM6264BLE	Extended (-25~-85 °C)	100*ns	28-SOP	100uA	
KM6264BLE-L				50uA	
KM6264BLI	Industrial (-40~85 °C)	100*ns	28-SOP	100uA	
KM6264BLI-L				50uA	

* measured with 30pF test load

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



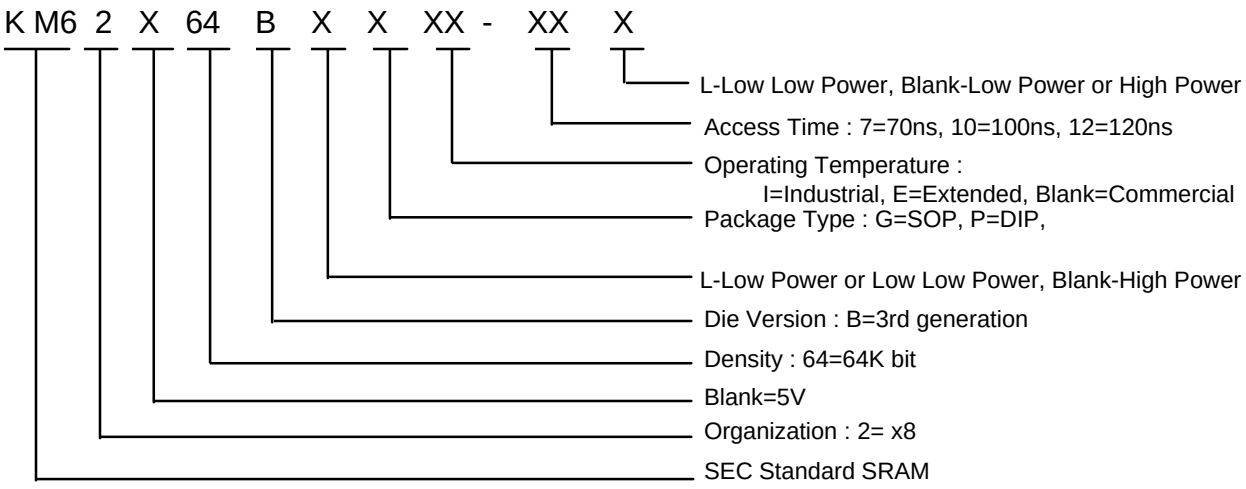
Pin Name	Function
A0~A12	Address Inputs
/WE	Write Enable Input
/CS1, CS2	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power(5V)
Vss	Ground
N.C	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Extended Temp Products (-25~85 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
KM6264BLP-7	28-DIP, 70ns, L-pwr	KM6264BLGE-10	28-SOP, 100ns, L-pwr	KM6264BLGI-10	28-SOP, 100ns, L-pwr
KM6264BLP-7L	28-DIP, 70ns, , LL-pwr	KM6264BLGE-10L	28-SOP, 100ns, LL-pwr	KM6264BLGI-10L	28-SOP, 100ns, LL-pwr
KM6264BLP-10	28-DIP, 100ns, , L-pwr				
KM6264BLP-10L	28-DIP, 100ns, LL-pwr				
KM6264BLP-12	28-DIP, 120ns, , L-pwr				
KM6264BLP-12L	28-DIP, 120ns, LL-pwr				
KM6264BLG-7	28-SOP, 70ns, L-pwr				
KM6264BLG-7L	28-SOP, 70ns, LL-pwr				
KM6264BLG-10	28-SOP, 100ns, L-pwr				
KM6264BLG-10L	28-SOP, 100ns, LL-pwr				
KM6264BLG-12	28-SOP, 120ns, L-pwr				
KM6264BLG-12L	28-SOP, 120ns, LL-pwr				

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM6264BL/L-L
		-25 to 85	°C	KM6264BLE/LE-L
		-40 to 85	°C	KM6264BLI/LI-L
Soldering temperature and time	Tsolder	260 °C, 10sec(Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.5	V
Input low voltage	Vil	-0.5***	-	0.8	V

* 1) Commercial Product : Ta=0 to 70 ° C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 ° C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 ° C, unless otherwise specified
** Ta=25 ° C
*** Vil(min)=-3.0V for ¡ Â50ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS1=Vih or CS2=Vil or /WE=Vil Vi/o=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS1=Vil, CS2=Vih		-	7	15	mA
Average operating current		Icc1	Vin=Vil or Vih, Ii/o=0mA Cycle time=1us, 100% duty /CS1¡ Ø0.2V, CS2 ¡ Ý Vcc-0.2V		-	-	10	mA
		Icc2	Min cycle, 100% duty /CS1=Vil, CS2=Vih, Ii/o=0mA		-	-	55	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh= -1.0mA		2.4	-	-	V
Standby Current(TTL)		Isb	/CS1=Vih or CS2=Vil		-	-	1	mA
Standby Current (CMOS)	KM6264BL	Isb1	/CS1¡ Ý Vcc-0.2V CS2¡ Ý Vcc-0.2V or CS2 ¡ Ø0.2V Others 0~Vcc	L	-	2	100	uA
	KM6264BL-L			LL	-	1	10	uA
	KM6264BLE			L	-	-	100	uA
	KM6264BLE-L			LL	-	-	50	uA
	KM6264BLI			L	-	-	100	uA
	KM6264BLI-L			LL	-	-	50	uA

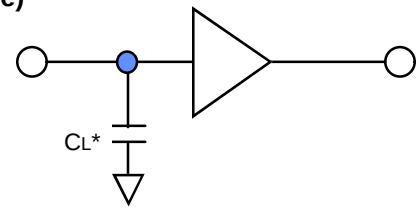
* 1) Commercial Product : Ta=0 to 70 ° C, Vcc=5V+/-10%, unless otherwise specified
2) Extended Product : Ta=-25 to 85 ° C, Vcc=5V+/-10%, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 ° C, Vcc=5V+/-10%, unless otherwise specified
** Ta=25 ° C

A.C CHARACTERISTICS

TEST CONDITIONS (1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL	-

* See test condition of DC and AC Operating characteristics



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM6264BL/L-L	0~70 °C	5V +/- 10%	70/100/120ns	Commercial
KM6264BLE/LE-L	-25~85 °C	5V +/- 10%	100*ns	Extended
KM6264BLI/LI-L	-40~85 °C	5V +/- 10%	100*ns	Industrial

* measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			70ns		100ns		120ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	100	-	120	-	ns
	Address access time	tAA	-	70	-	100	-	120	ns
	Chip select to output	tCO	-	70	-	100	-	120	ns
	Output enable to valid output	tOE	-	35	-	50	-	60	ns
	Chip select to low-Z output	tLZ	5	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	30	0	35	0	40	ns
	Output disable to high-Z output	tOHZ	0	30	0	35	0	40	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	70	-	100	-	120	-	ns
	Chip select to end of write	tCW	60	-	80	-	85	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	80	-	85	-	ns
	Write pulse width	tWP	40	-	60	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	30	0	30	0	30	ns
	Data to write time overlap	tDW	30	-	40	-	50	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	10	-	ns

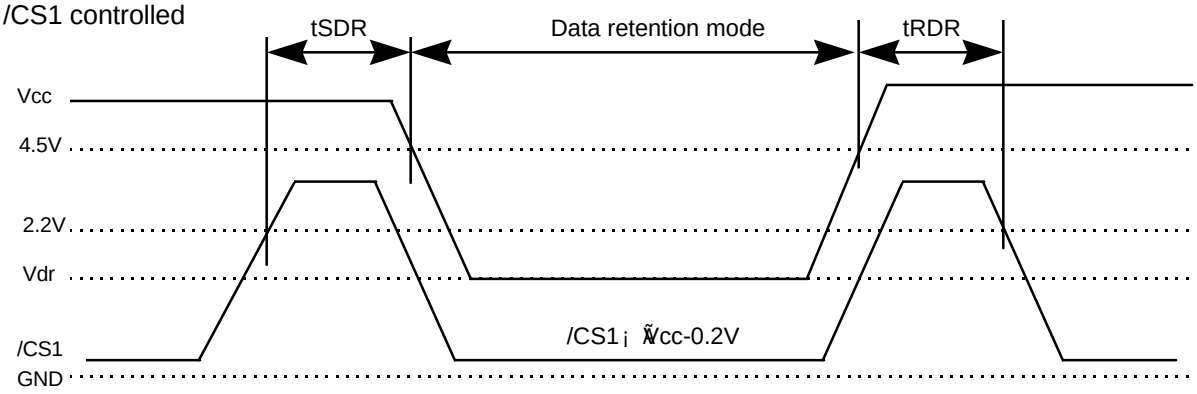
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS*** ¡ ÑVcc-0.2V		2.0	-	5.5	V
Data retention current	Idr	KM6264BL	Vcc=3.0V	L-Ver	-	1	50	uA
		KM6264BL-L	/CS ¡ ÑVcc-0.2V	LL-Ver	-	0.5	5	
		KM6264BLE		L-Ver	-	-	50	
		KM6264BLE-L		LL-Ver	-	-	25	
		KM6264BLI		L-Ver	-	-	50	
		KM6264BLI-L		LL-Ver	-	-	25	
Data retention set-up time	tSDR		See data retention		0	-	-	ms
Recovery time	tRDR		waveform		5	-	-	

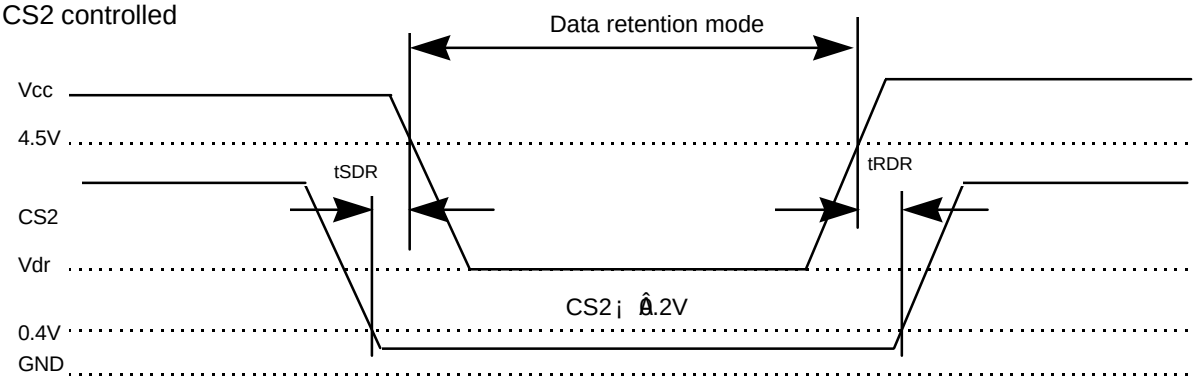
* 1) Commercial Product : Ta=0 to 70 ° C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 ° C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 ° C, unless otherwise specified
** Ta=25 ° C
*** /CS1 ¡ ÑVcc-0.2, CS2 ¡ ÑVcc-0.2(/CS1 Controlled) or CS2 ¡ Ñ0.2(CS2 Controlled)

DATA RETENTION TIMING DIAGRAM

1) /CS1 controlled



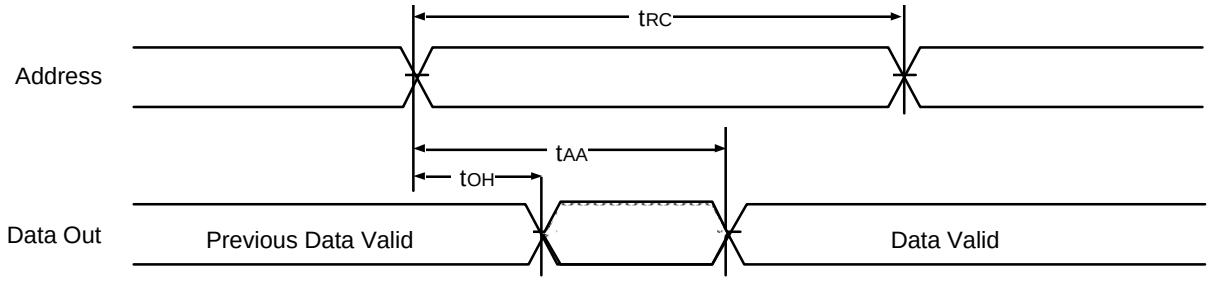
2) CS2 controlled



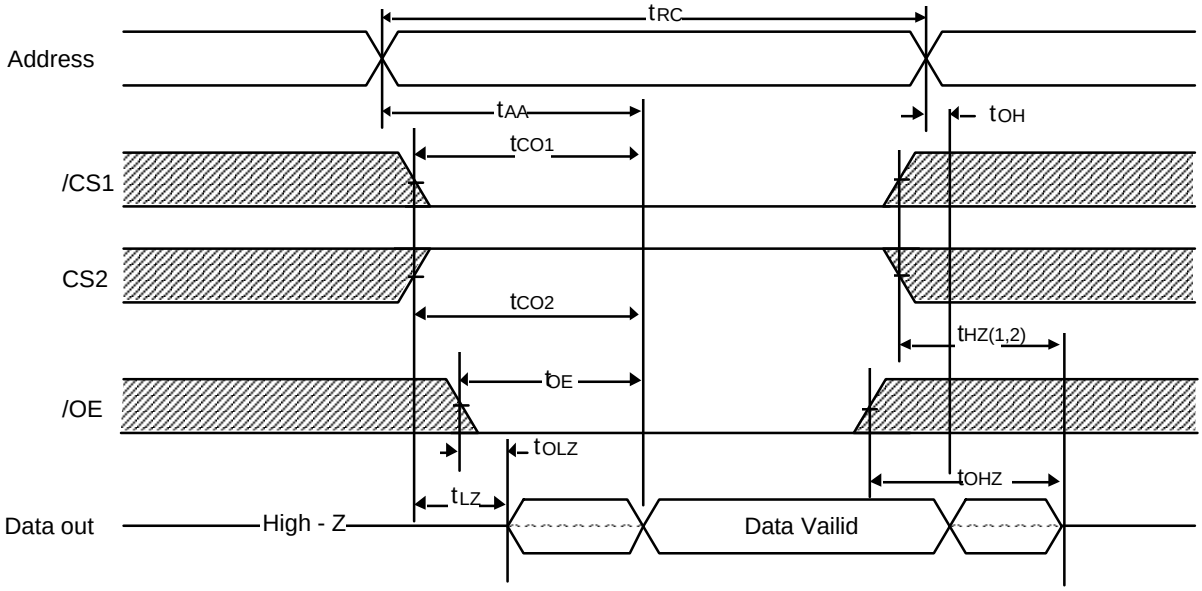
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, CS2=/WE=Vih)



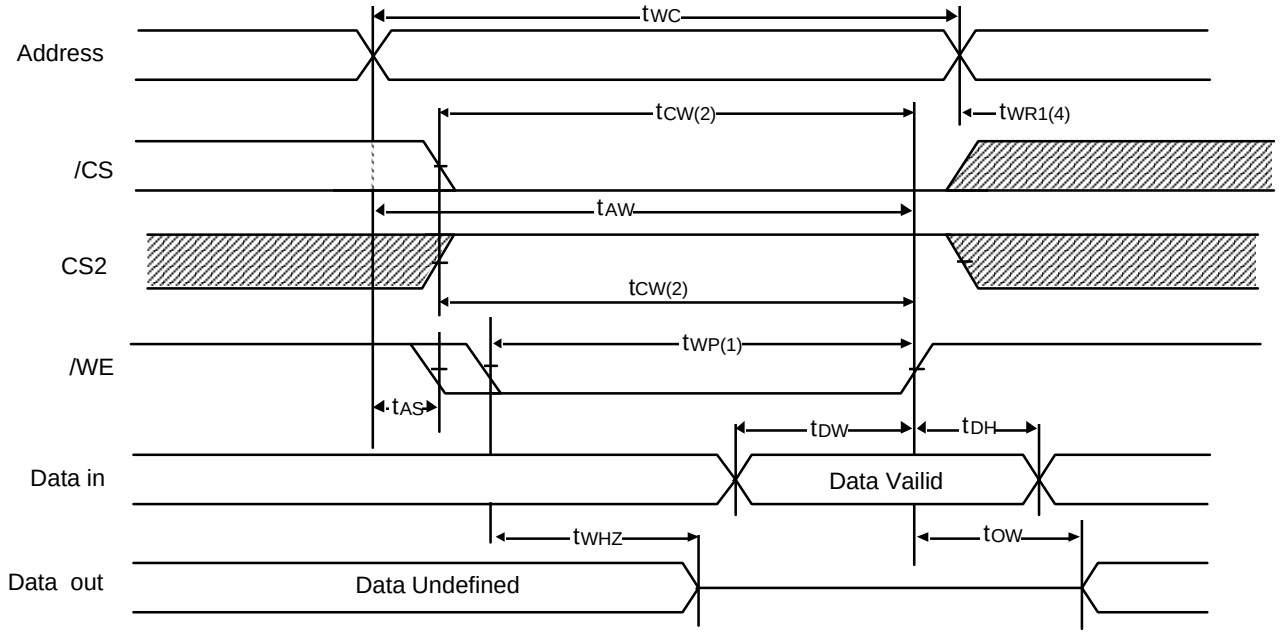
TIMING WAVEFORM OF READ CYCLE(2) (/WE= VIH)



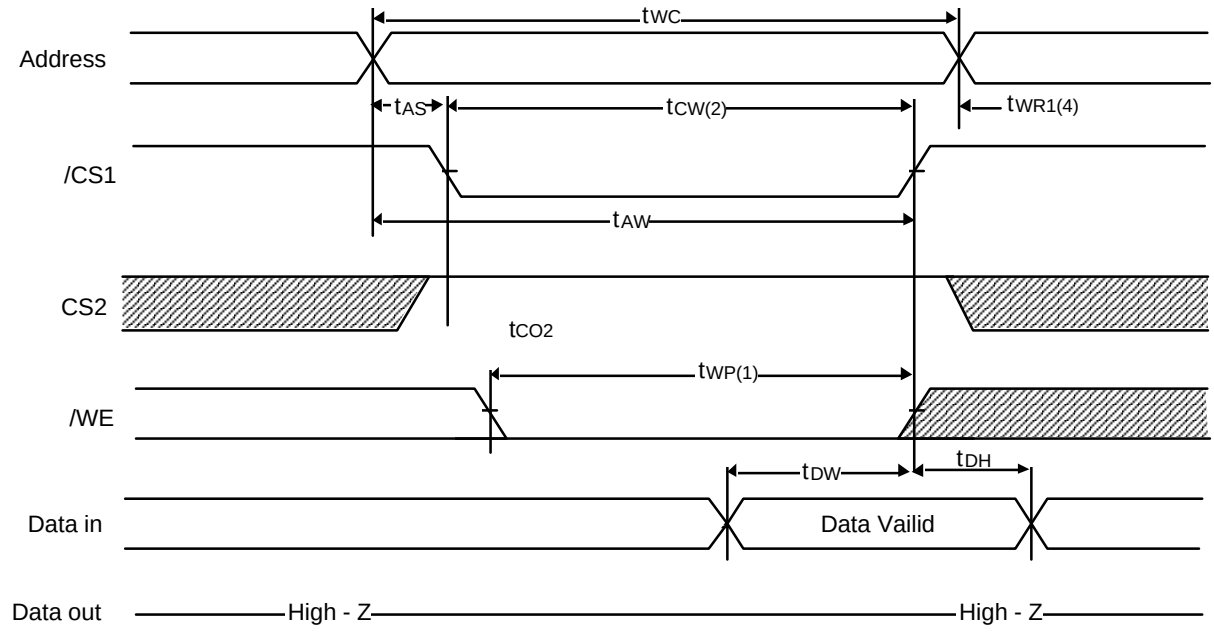
Notes(Read Cycle)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max) is less than tLZ(Min) both for a given device and device to device interconnection.

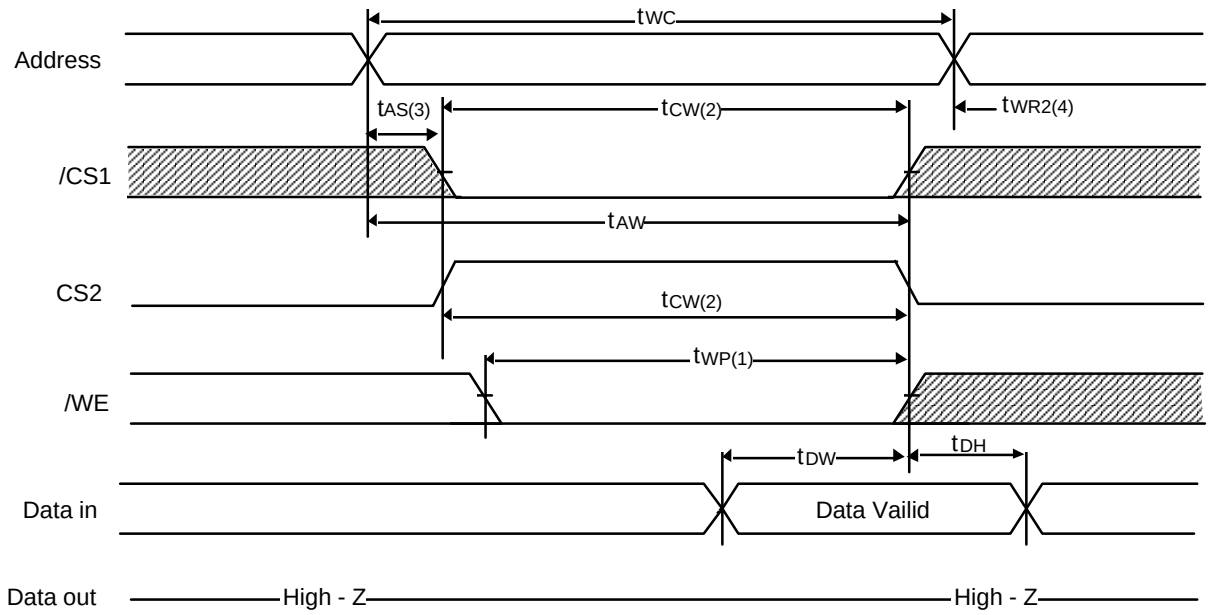
TIMING WAVEFORM OF WRITE CYCLE(1) (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (/CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



Notes(Write Cycle)

1. A write occurs during the overlap of a low /CS1, a high CS2 and a low /WE. A write begins at the latest transition among /CS1 going low, CS2 going high and /WE going low. A write ends at the earliest transition among /CS1 going high, CS2 going low and /WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends at /CS1, or /WE going high, tWR2 applied in case a write ends at CS2 going to low.

FUNCTIONAL DESCRIPTION

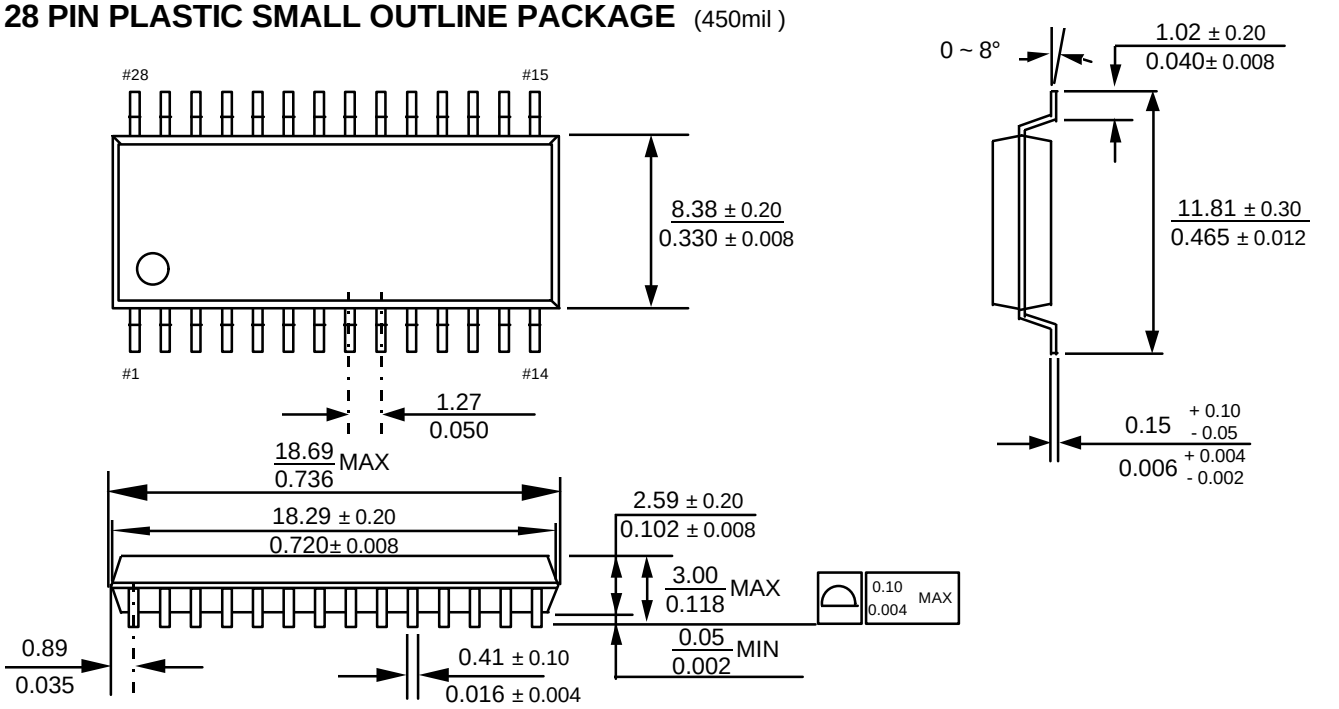
/CS1	CS2	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	Isb, Isb1
X	L	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	H	Output Disable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc

* X means don't care

PACKAGE DIMENSION

Unit : Millimeters (Inches)

28 PIN PLASTIC SMALL OUTLINE PACKAGE (450mil)



28 PIN PLASTIC DUAL INLINE PACKAGE (600mil)