```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.numeric_std.all;
4
5   entity moduldac_tb is
6   end moduldac_tb;
7
8   architecture beexam of moduldac_tb is
9
10  component moduldac_wrap is
11
12
13  port (
14        o_clock_dac     : out  std_logic := '1';
15        o_data_dac      : out  std_logic := '0';
16        o_sync_dac      : out  std_logic := '1';
17        o_ldac_dac      : out  std_logic := '1';
18        o_clr_dac       : out  std_logic := '1';
19        i_clk           : in   std_logic := '0';
20        i_rst           : in   std_logic := '0';
21        i_update        : in   std_logic := '0';
22        i_data_att1_dac : in std_logic_vector(11 downto 0) := (others=> '0');
23        i_data_att2_dac : in std_logic_vector(11 downto 0) := (others=> '0');
24        i_data_maam_i   : in std_logic_vector(11 downto 0) := (others=> '0');
25        i_data_maam_g   : in std_logic_vector(11 downto 0) := (others=> '0');
26        i_channel       : in std_logic_vector(2 downto 0) := (others=> '0')
27  );
28
29  end component;
30
31  signal clk_100_mhz,update  : std_logic := '0';
32  signal channel             : std_logic_vector(2 downto 0) := (others=> '0');
33  signal data_att1_dac       :  std_logic_vector(11 downto 0) := (others=> '0');
34  signal data_att2_dac       :  std_logic_vector(11 downto 0) := (others=> '0');
35  signal data_maam_i         : std_logic_vector(11 downto 0) := (others=> '0');
36  signal data_maam_g         : std_logic_vector(11 downto 0) := (others=> '0');
37
38  begin
39
40  data_init : process
41  begin
42
43  wait for 70000 ns;
44
45  data_att1_dac <= "010101010101";
46  data_att2_dac <= (others=> '0');
47  data_maam_i <= (others=> '0');
48  data_maam_g <= (others=> '0');
49
50  wait for 17710 ns;
51
52  data_att1_dac <= "111111111110";
53  data_att2_dac <= "000011110000";
54  data_maam_i <="001100110011";
55  data_maam_g <="110011111111";
56
57  wait for 80000 ns;
58
59  data_att1_dac <= (others=> '0');
60  data_att2_dac <= (others=> '0');
61  data_maam_i <= (others=> '0');
62  data_maam_g <= "000011110000";
63
64  wait for 100 ms;
65
66  end process;
67
68  clk_100mhz_init : process
69  begin
70      clk_100_mhz <= '0';
71
72      wait for 80 ns;
73      loop
74          wait for 5 ns;
75              clk_100_mhz <= '1';
76          wait for 5 ns;
77              clk_100_mhz <= '0';
78      end loop;
79  end process;
80
81  update_init : process
```

```
 82    begin
 83       update <= '0';
 84       wait for 70000 ns;
 85
 86       --loop
 87             update <= '1';
 88          wait for 10 ns;
 89             update <= '0';
 90          wait for 17700 ns;
 91             update <= '1';
 92          wait for 10 ns;
 93             update <= '0';
 94          wait for 700 ns;
 95             update <= '1';
 96          wait for 10 ns;
 97             update <= '0';
 98
 99
100
101          wait for 100 ms;
102       --end loop;
103    end process;
104
105
106    channel_init : process
107    begin
108          channel <= "111";
109       wait for 70000 ns;
110          channel <= "000";
111       wait for 17710 ns;
112          channel <= "100";
113       wait for 80000 ns;
114          channel <= "011";
115
116       wait for 12710 ms;
117    end process;
118
119
120    moduldac: moduldac_wrap
121    port map (
122       i_clk => clk_100_mhz,
123       i_update => update,
124       i_channel => channel,
125       i_data_att1_dac => data_att1_dac,
126       i_data_att2_dac => data_att2_dac,
127       i_data_maam_i => data_maam_i,
128       i_data_maam_g => data_maam_g
129    );
130
131    end beexam;
132
```